ATLAS MUCTPI
Serial Link Test Report
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Chapter 1

Initial considerations

1.1 IBERT configuration

Table 1.1: IBERT configuration for 6.4 Gb/s runs

Name	Pattern	TX Pre/Pos	TX Diff Swing	DFE	Loopback	RX Common	Termination	TXUSRCLK	RXUSRCLK
MSP to MSP minipods	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Programmable	800 mV	80.18	80.25
TRP to MSP minipod	PRBS 31-bit	0.00 dB (00000)	950 mV (1100)	0	None	Programmable	800 mV	160.35	80.25
TRP QSFP loopback	PRBS 31-bit	0.00 dB (00000)	950 mV (1100)	0	None	Programmable	800 mV	160.35	160.35
TRP SFP loopback	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Programmable	800 mV	80.20	80.20
MSPA to TRP on-board links	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Floating	800 mV	80.20	160.35
MSPC to TRP on-board links	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Floating	800 mV	80.20	80.20

Table 1.2: IBERT configuration for 12.8 Gb/s runs

Name	Pattern	TX Pre/Pos	TX Diff Swing	DFE	Loopback	RX Common	Termination	TXUSRCLK	RXUSRCLK
MSP to MSP minipods	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Programmable	800 mV	160.35	160.35
TRP to MSP minipod	PRBS 31-bit	0.00 dB (00000)	950 mV (1100)	0	None	Programmable	800 mV	320.68	160.35
TRP QSFP loopback	PRBS 31-bit	0.00 dB (00000)	950 mV (1100)	0	None	Programmable	800 mV	320.68	320.68
TRP SFP loopback	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Programmable	800 mV	160.35	160.35
MSPA to TRP on-board links	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Floating	800 mV	160.35	320.68
MSPC to TRP on-board links	PRBS 31-bit	0.00 dB (00000)	846 mV (11000)	0	None	Floating	800 mV	160.35	160.35

1.2 Eye diagram mask

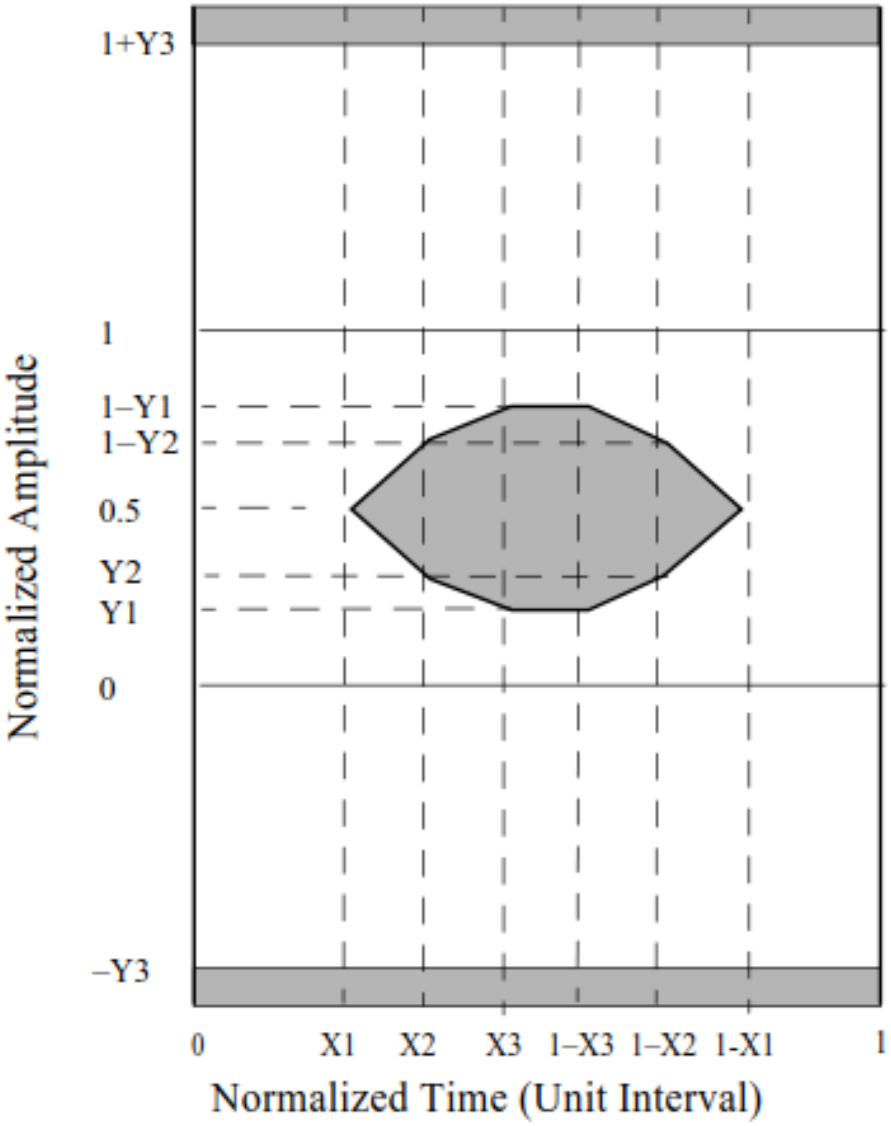


Figure 1.1: Transmitter eye mask definition

Figure 1.1 shows the eye mask parameters X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.40, 0.45, 0.25, 0.28, 0.80 extracted from the Table 68-3—10GBASE-LRM transmit characteristics part of the IEEE Std 802.3-2015 SECTION 5.

Chapter 2

Summary plots

2.1 Vertical and horizontal openning scatter plots

2.1.1 Scatter plot MUCTPI V2 6.4 Gbps

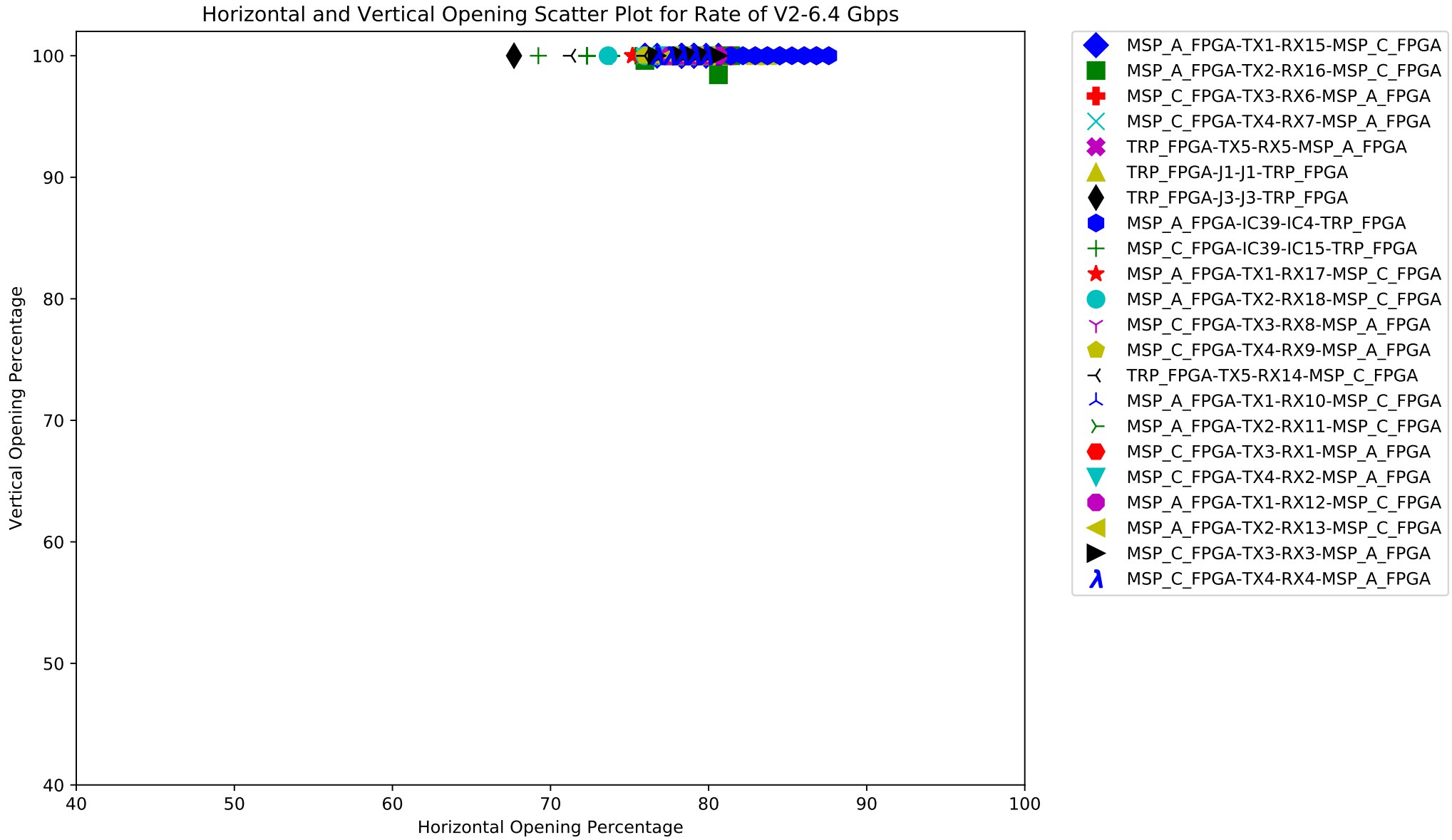


Figure 2.1: Scatter plot MUCTPI V2 6.4 Gbps

2.1.2 Scatter plot MUCTPI V2 12.8 Gbps

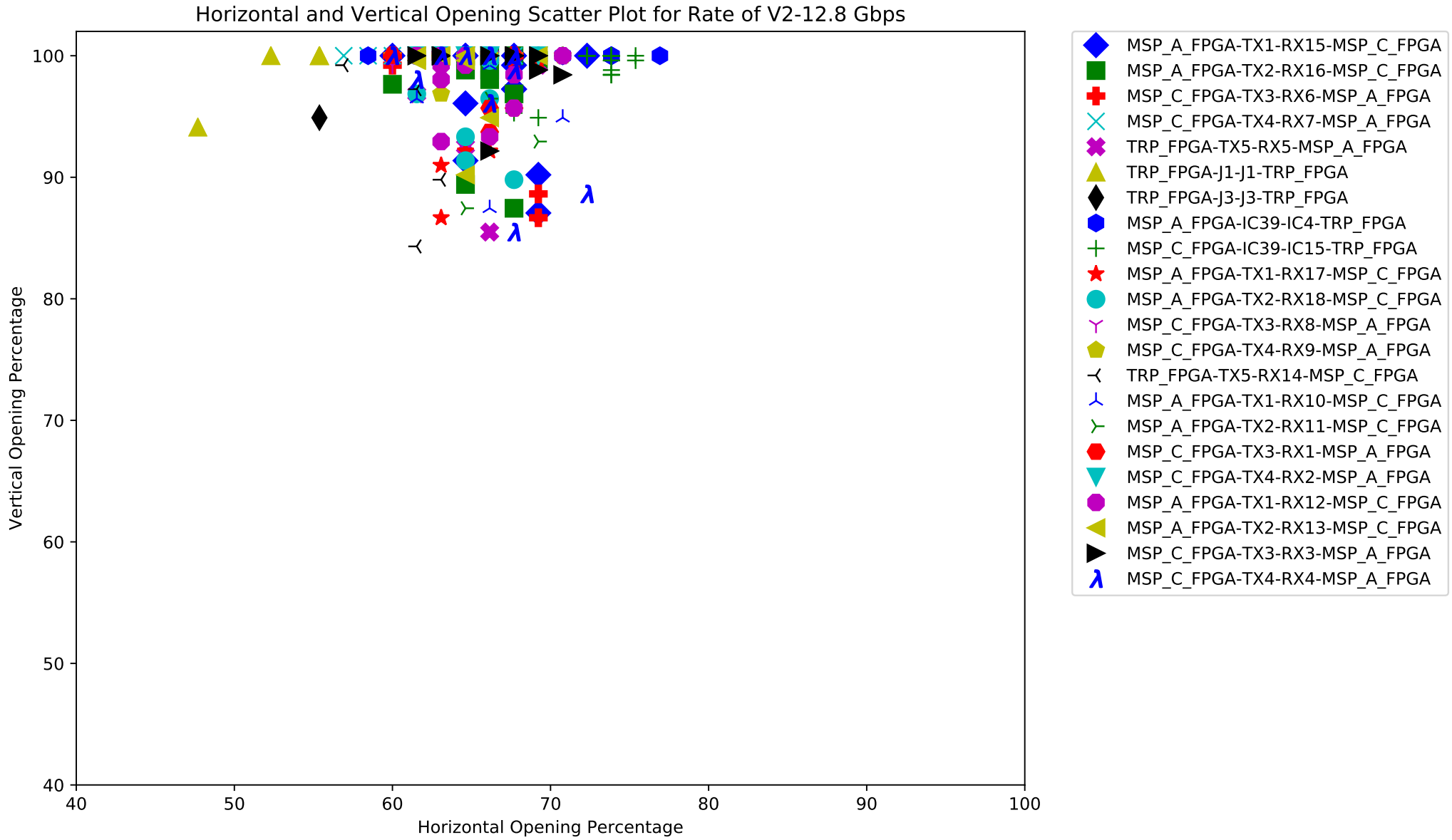


Figure 2.2: Scatter plot MUCTPI V2 12.8 Gbps

2.1.3 Scatter plot MUCTPI V3 6.4 Gbps

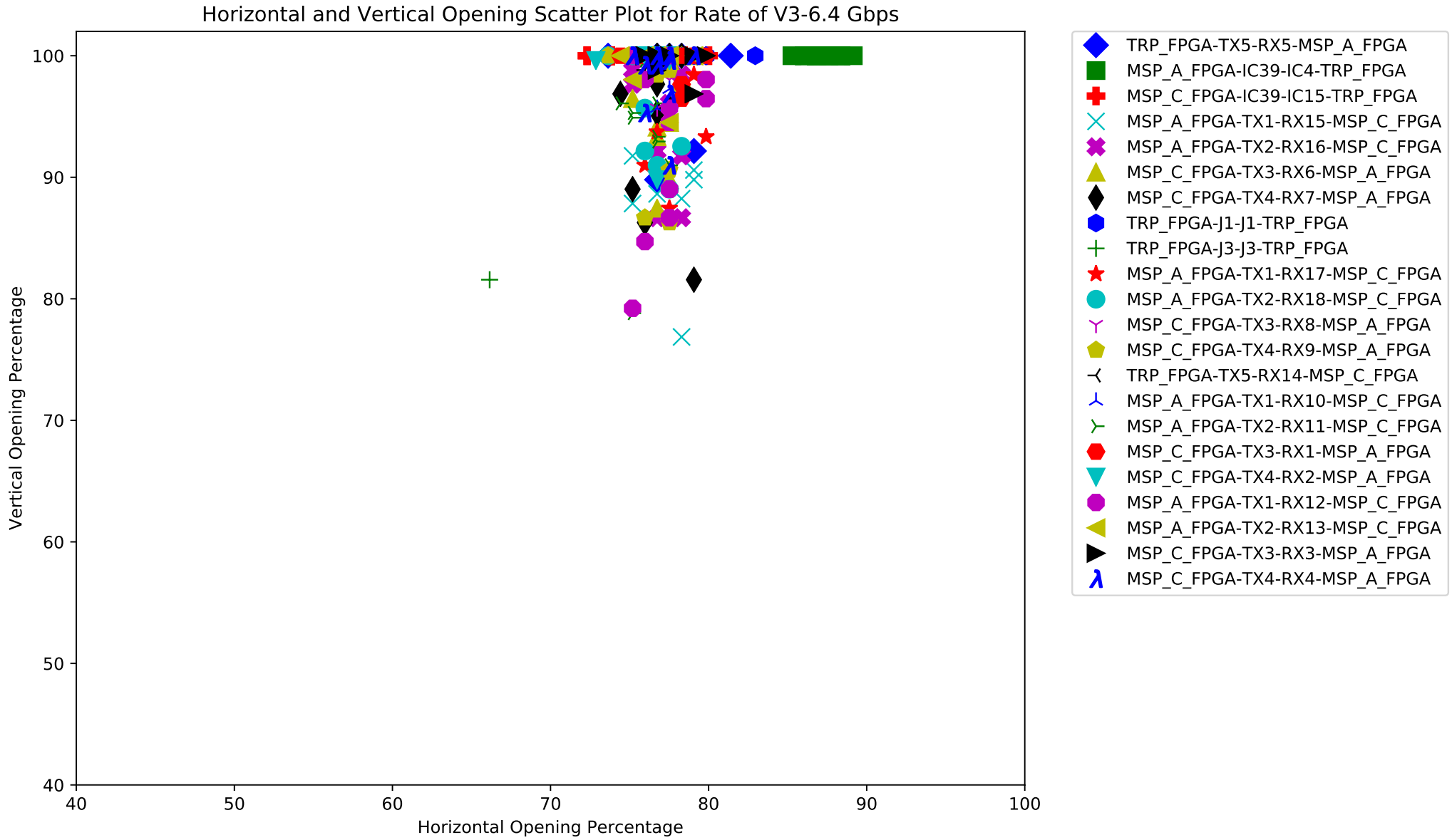


Figure 2.3: Scatter plot MUCTPI V3 6.4 Gbps

2.1.4 Scatter plot MUCTPI V3 12.8 Gbps

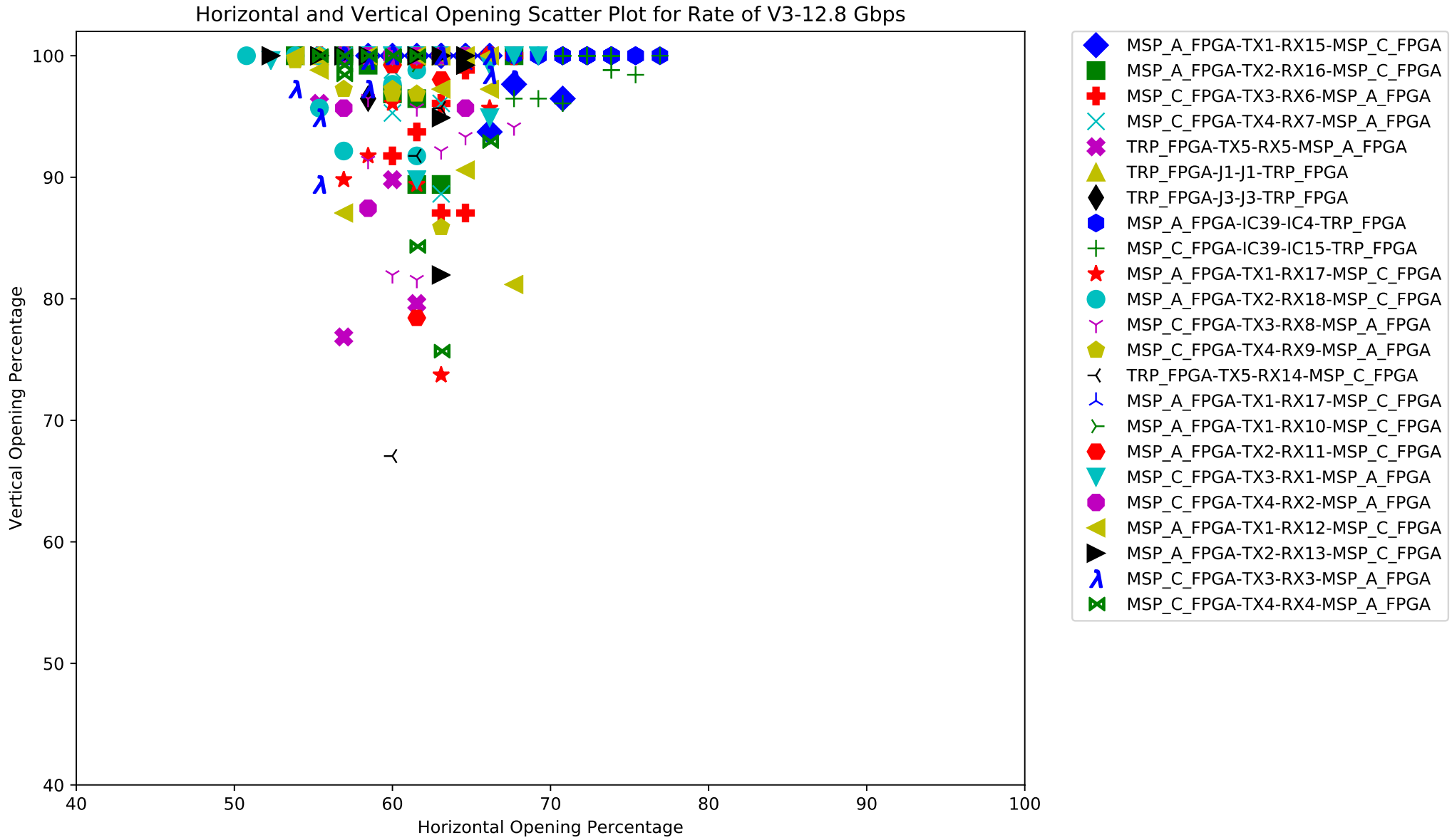


Figure 2.4: Scatter plot MUCTPI V3 12.8 Gbps

2.2 Vertical openning histograms

2.2.1 Vertical openning MUCTPI V2 6.4 Gbps

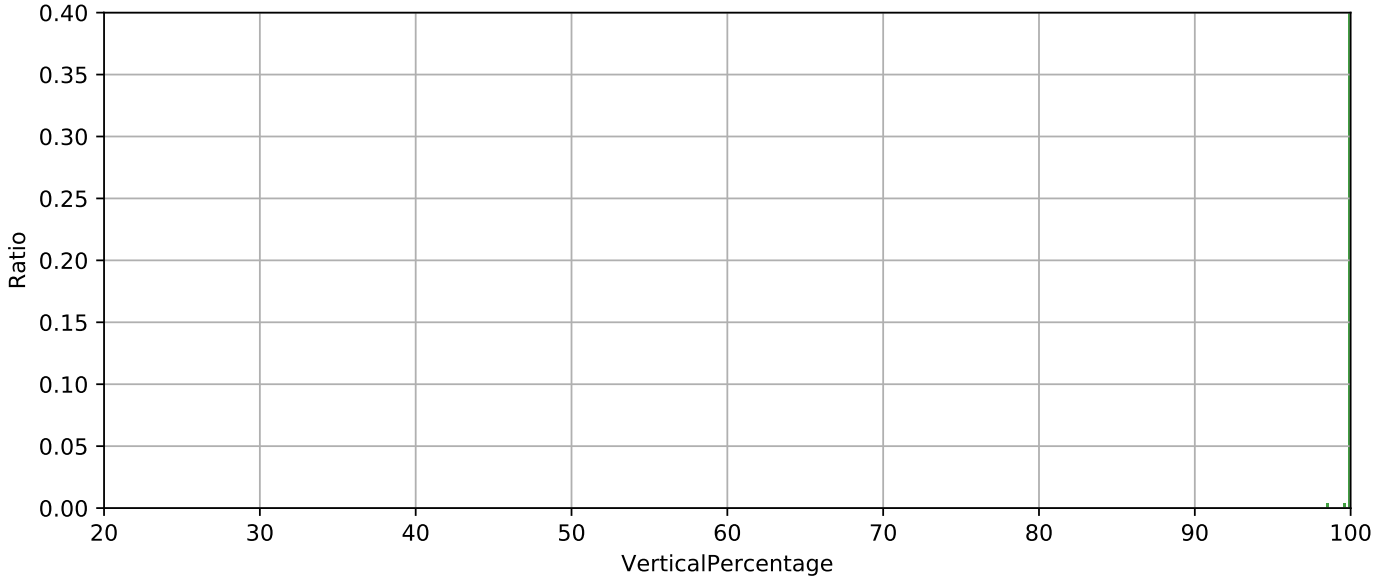


Figure 2.5: Vertical openning MUCTPI V2 6.4 Gbps

2.2.2 Vertical openning MUCTPI V2 12.8 Gbps

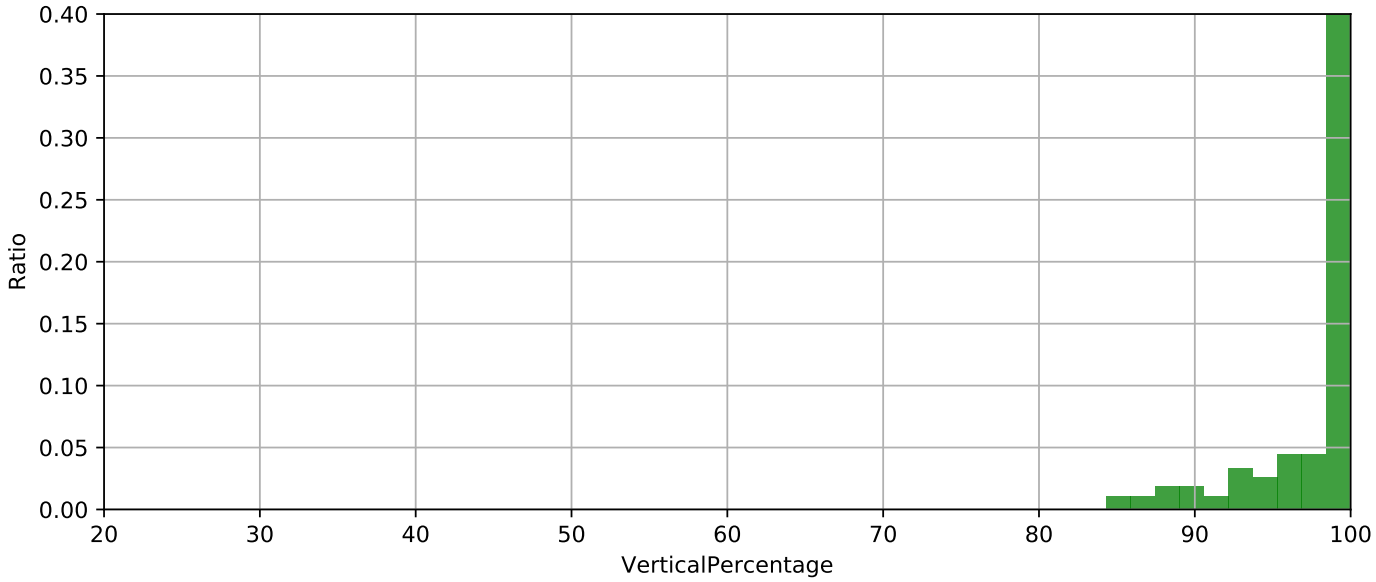


Figure 2.6: Vertical openning MUCTPI V2 12.8 Gbps

2.2.3 Vertical openning MUCTPI V3 6.4 Gbps

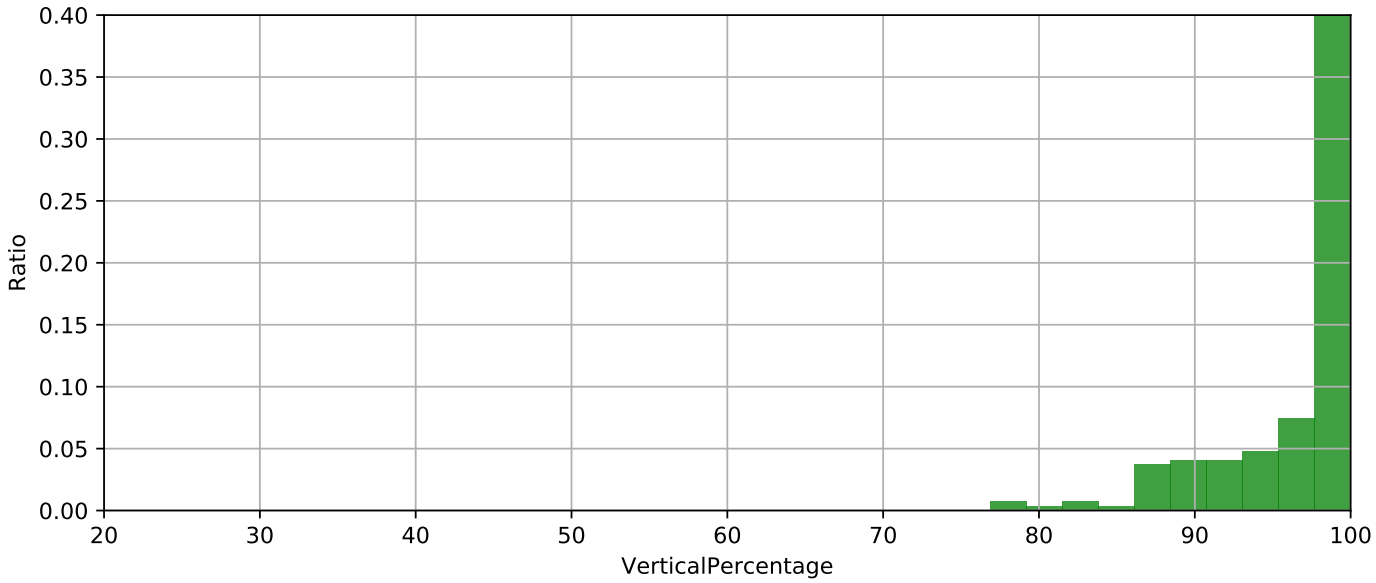


Figure 2.7: Vertical openning MUCTPI V3 6.4 Gbps

2.2.4 Vertical openning MUCTPI V3 12.8 Gbps

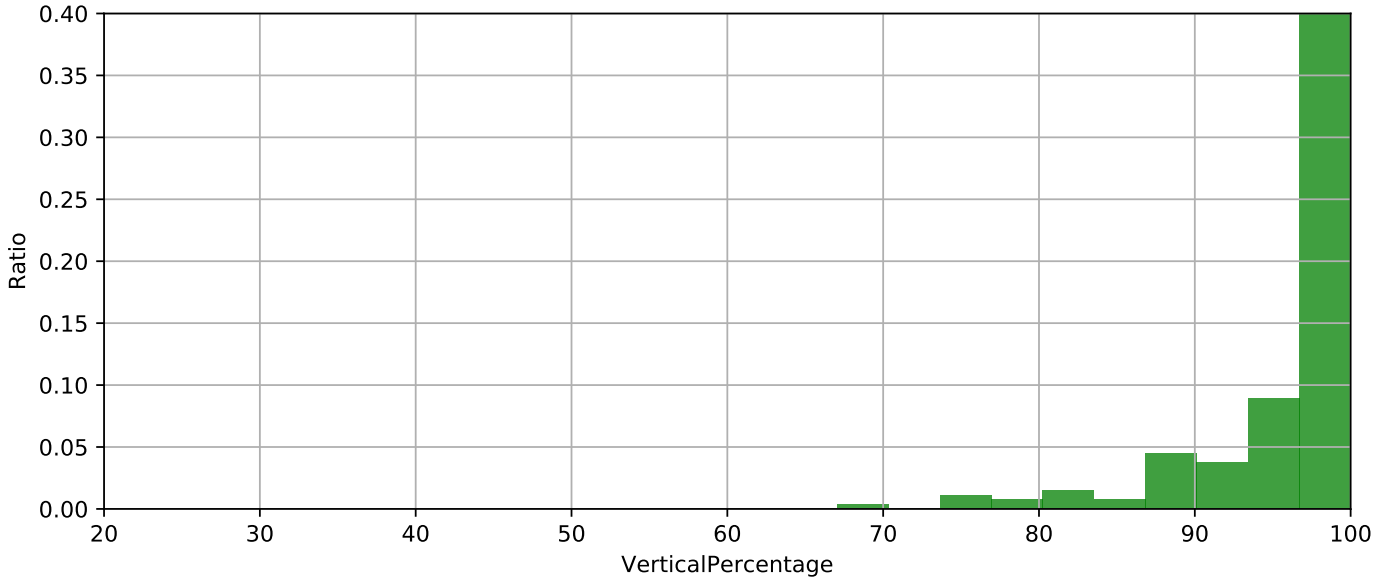


Figure 2.8: Vertical openning MUCTPI V3 12.8 Gbps

2.3 Horizontal openning histograms

2.3.1 Horizontal openning MUCTPI V2 6.4 Gbps

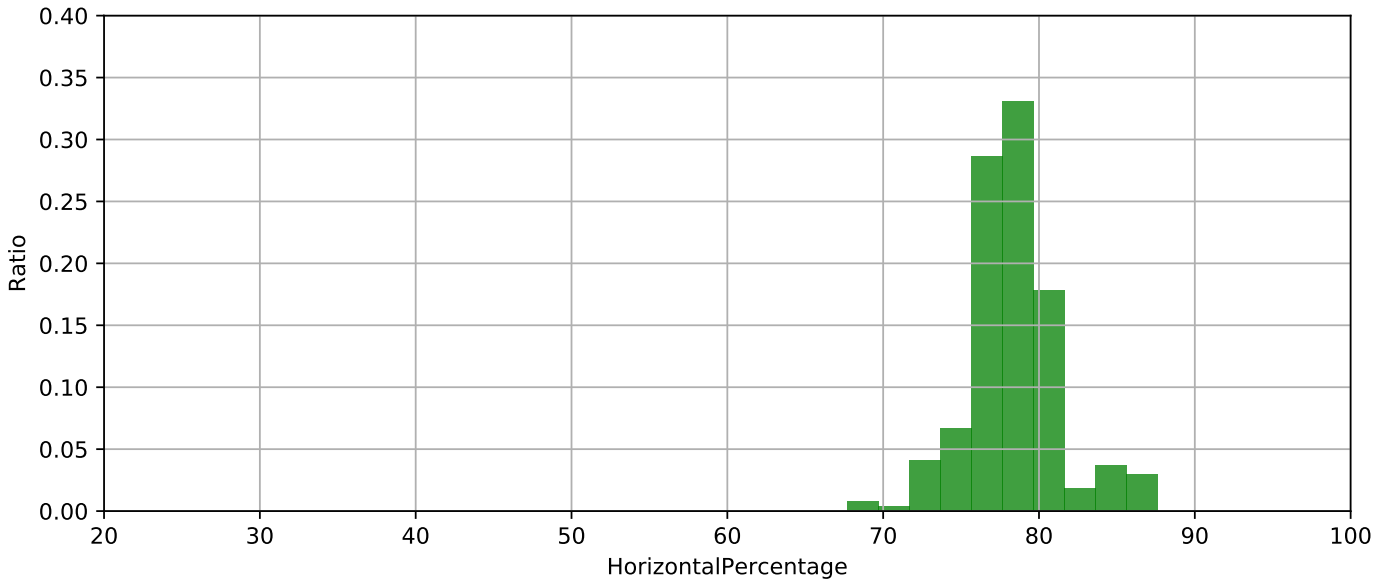


Figure 2.9: Horizontal openning MUCTPI V2 6.4 Gbps

2.3.2 Horizontal openning MUCTPI V2 12.8 Gbps

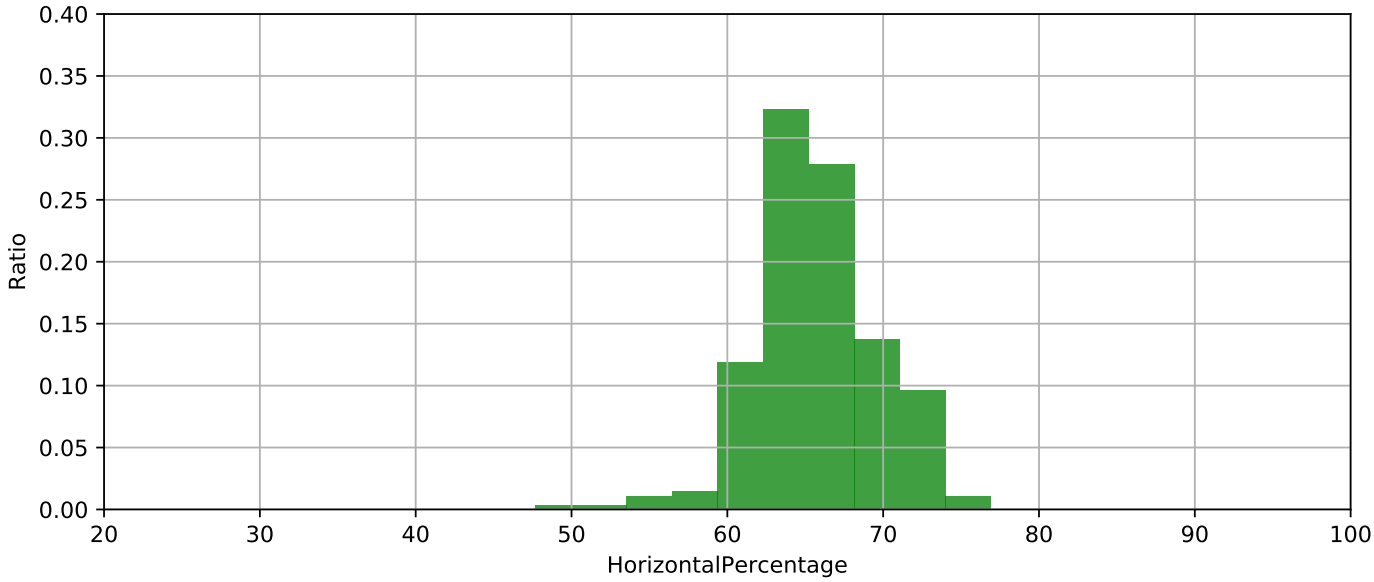


Figure 2.10: Horizontal openning MUCTPI V2 12.8 Gbps

2.3.3 Horizontal openning MUCTPI V3 6.4 Gbps

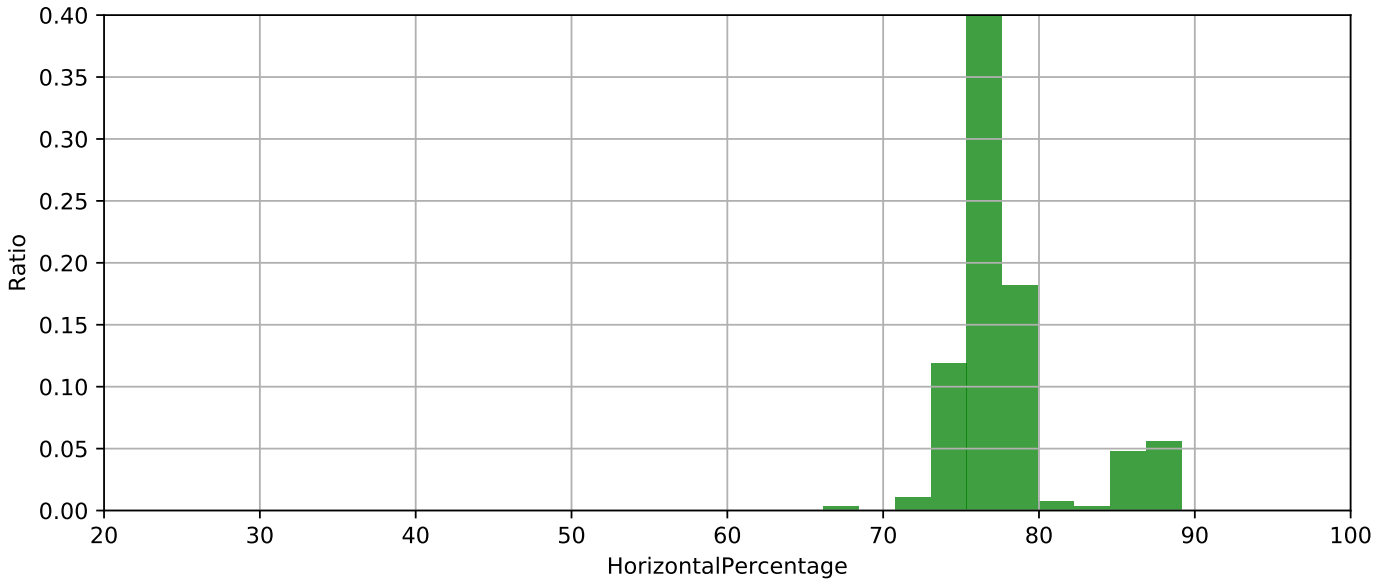


Figure 2.11: Horizontal openning MUCTPI V3 6.4 Gbps

2.3.4 Horizontal openning MUCTPI V3 12.8 Gbps

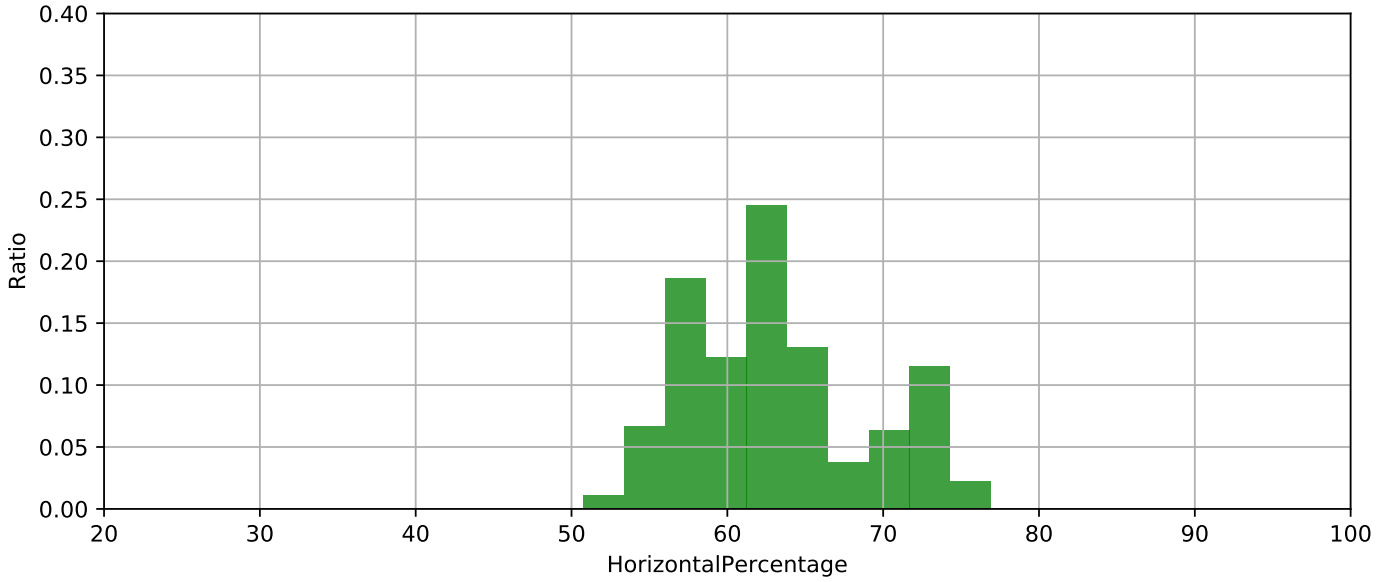


Figure 2.12: Horizontal openning MUCTPI V3 12.8 Gbps

2.4 Openning Area histograms

2.4.1 Area openning MUCTPI V2 6.4 Gbps

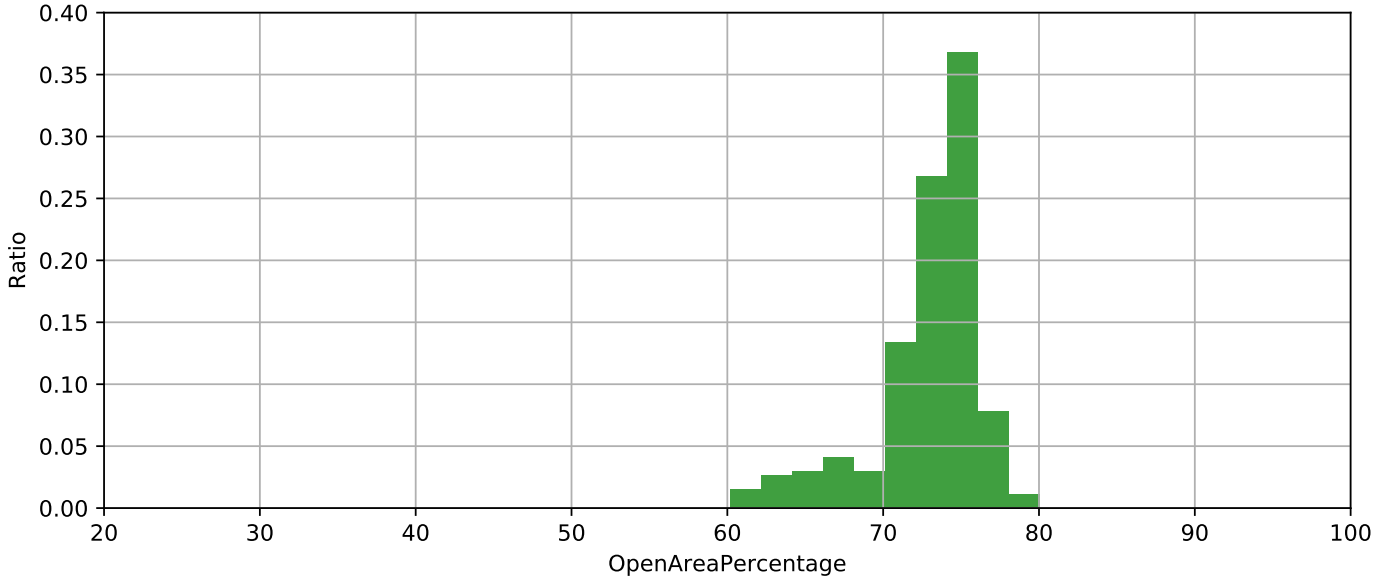


Figure 2.13: Area openning MUCTPI V2 6.4 Gbps

2.4.2 Area openning MUCTPI V2 12.8 Gbps

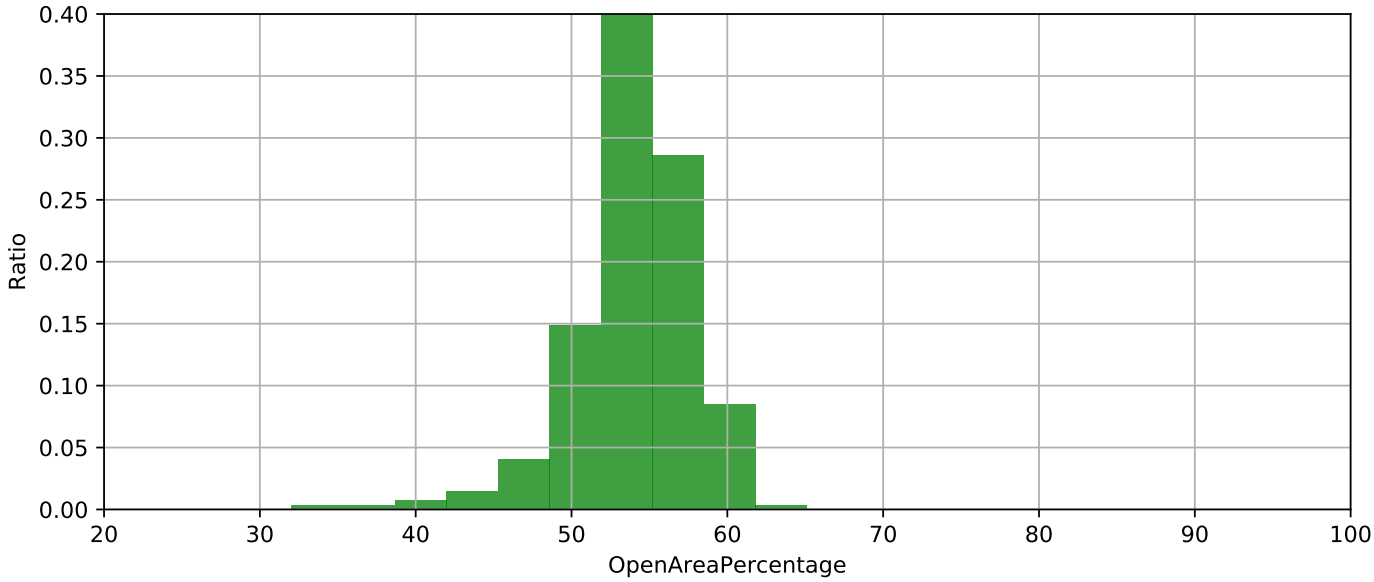


Figure 2.14: Area openning MUCTPI V2 12.8 Gbps

2.4.3 Area openning MUCTPI V3 6.4 Gbps

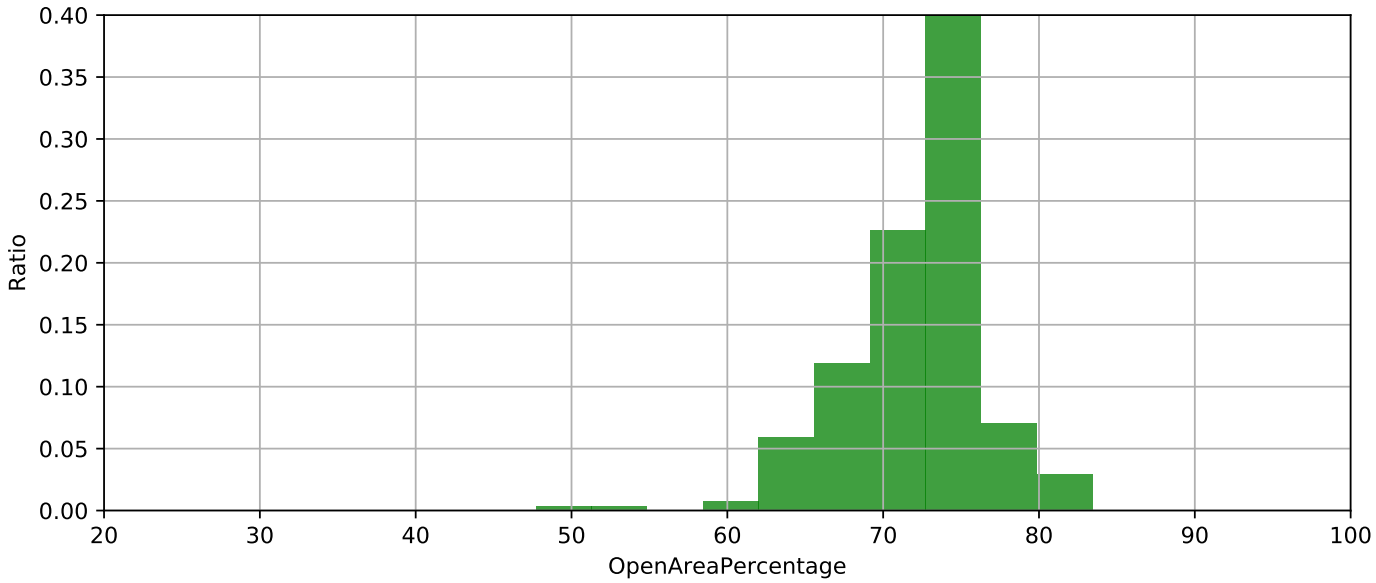


Figure 2.15: Area openning MUCTPI V3 6.4 Gbps

2.4.4 Area openning MUCTPI V3 12.8 Gbps

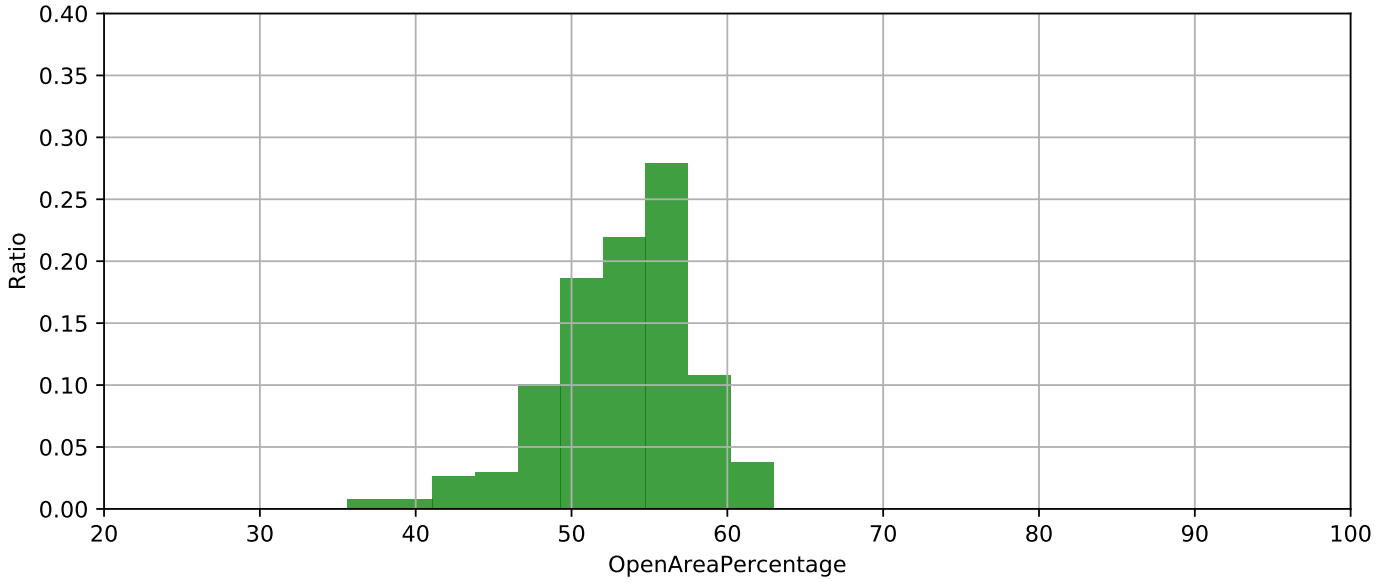


Figure 2.16: Area openning MUCTPI V3 12.8 Gbps

Chapter 3

MUCTPI V2 6.4 Gbps

3.1 MSP_A TX1 MSP_C RX15 Minipod Loopback

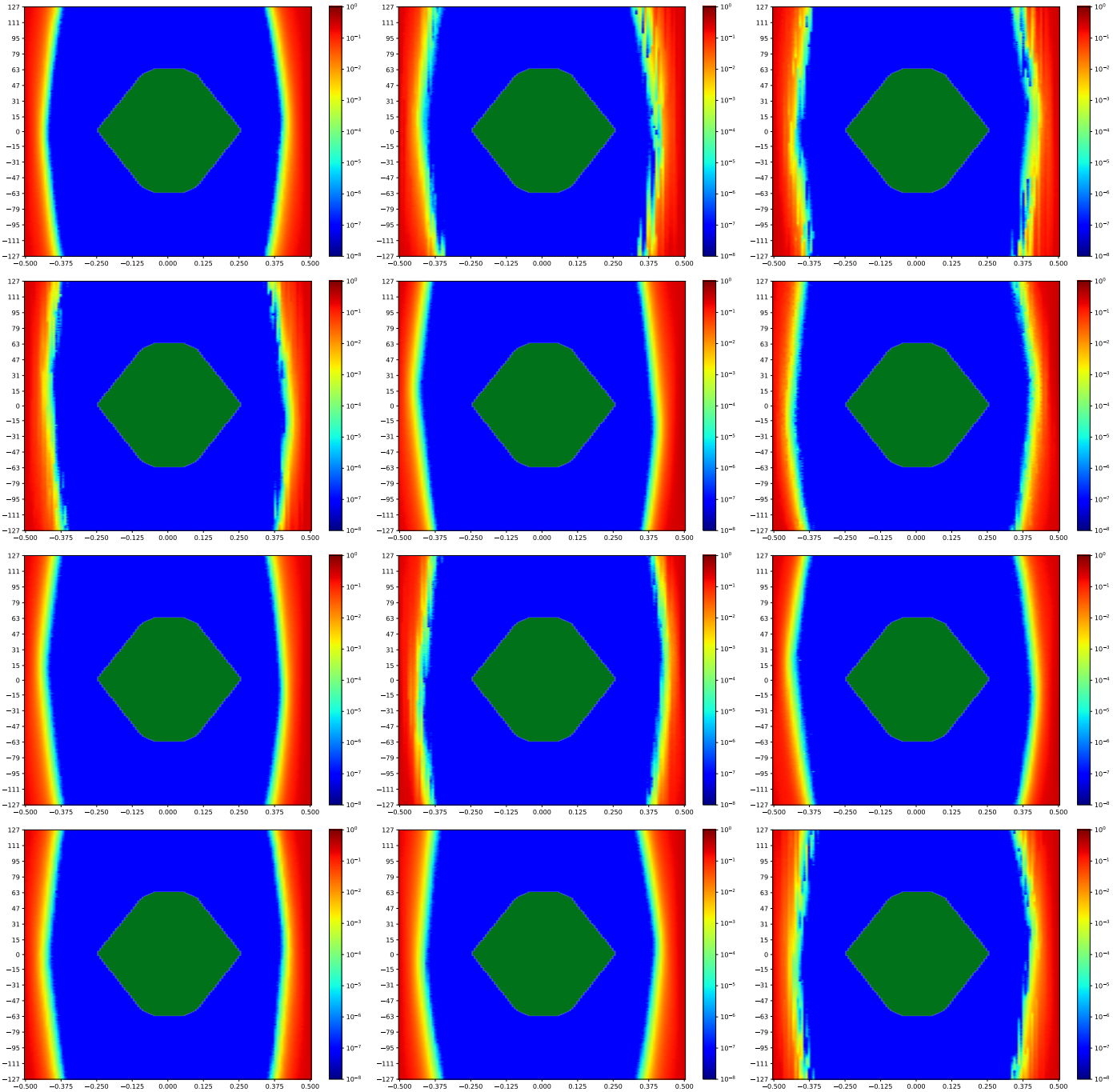


Figure 3.1: MSP_A TX1 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.14.

3.1.1 MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Table 3.1: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:44:28		2018-Sep-26 16:45:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24704	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

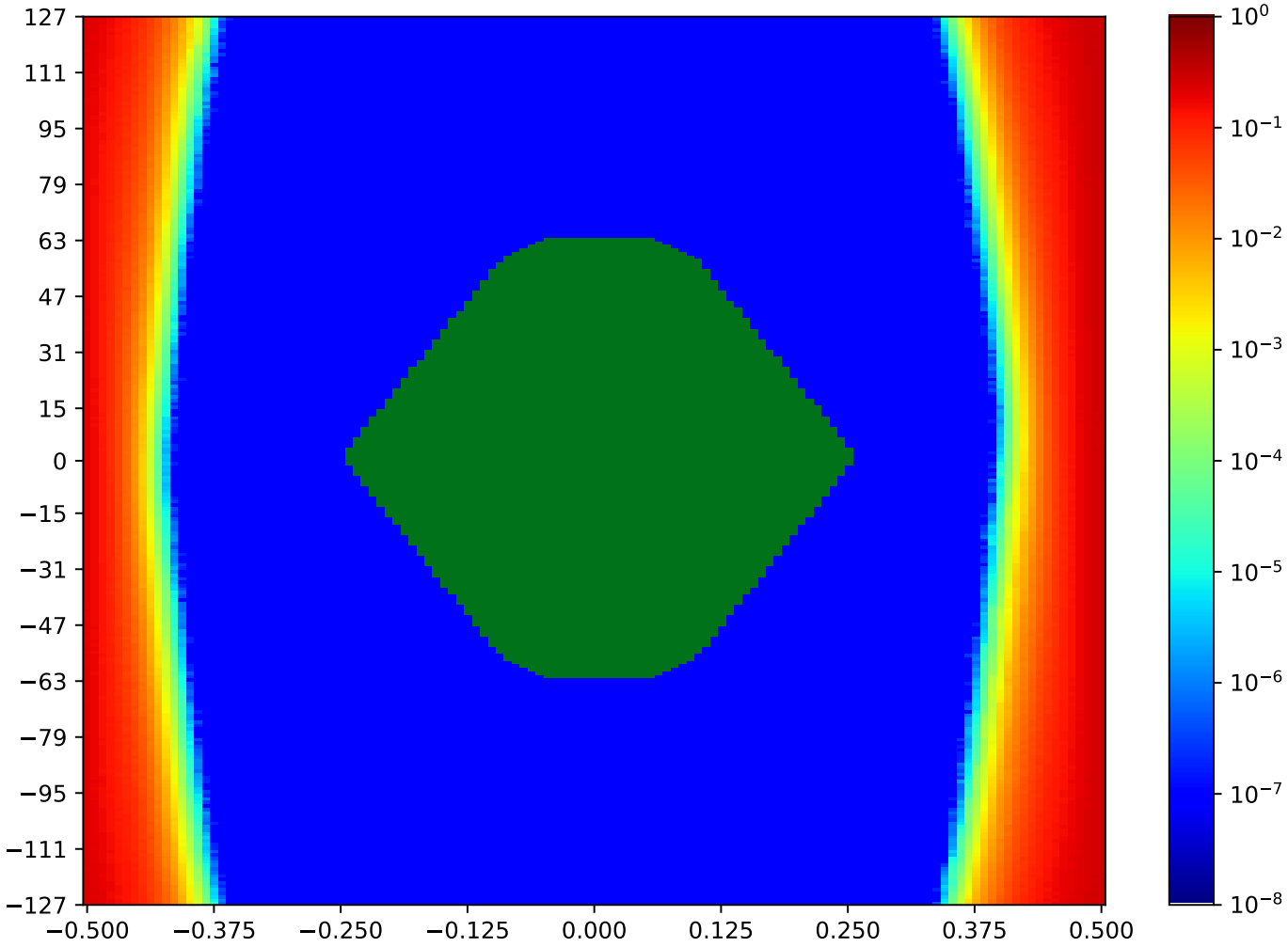


Figure 3.2: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.2 MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Table 3.2: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:46:58		2018-Sep-26 16:48:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23680	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

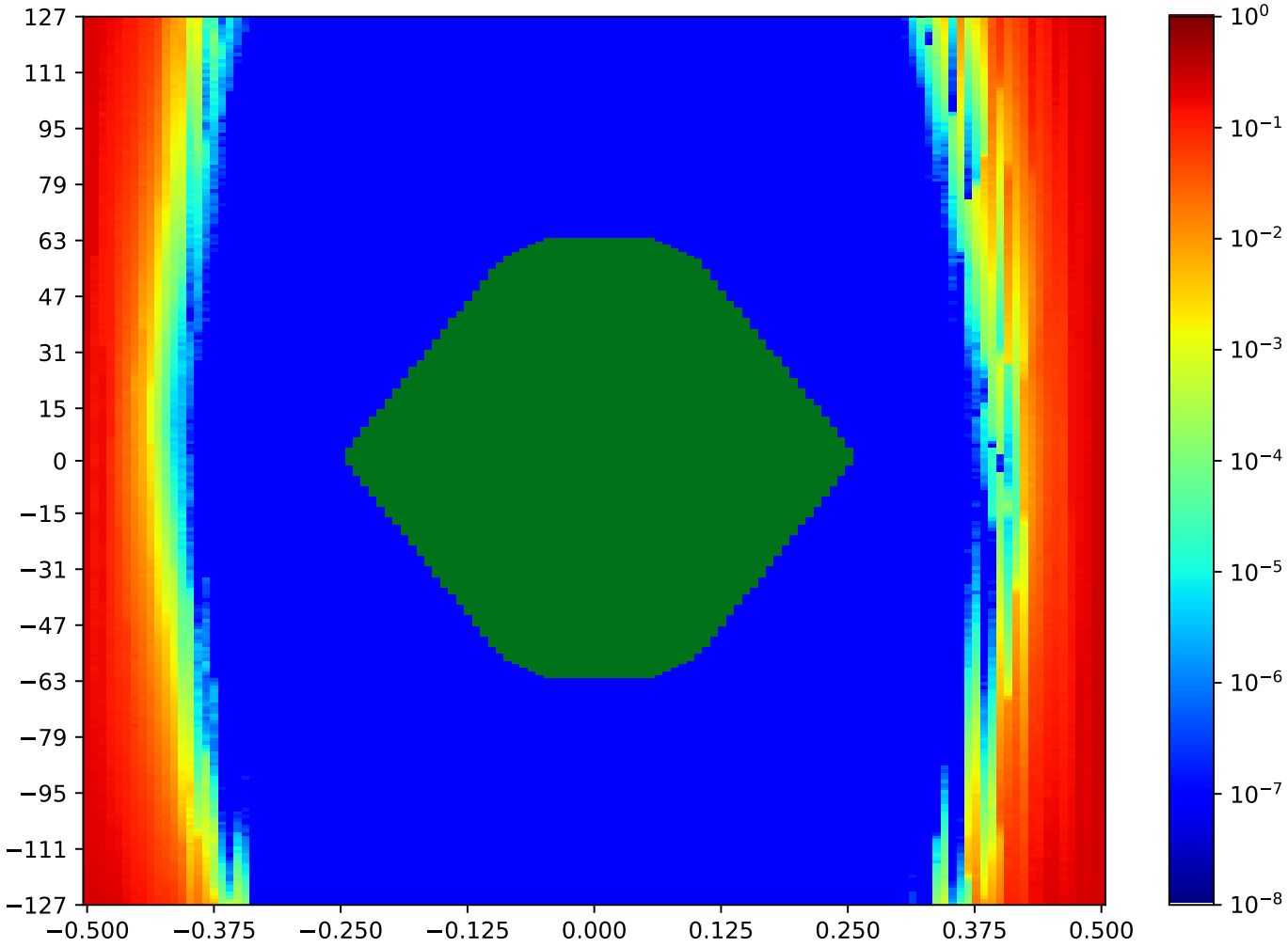


Figure 3.3: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.3 MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Table 3.3: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:48:12		2018-Sep-26 16:49:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24026	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

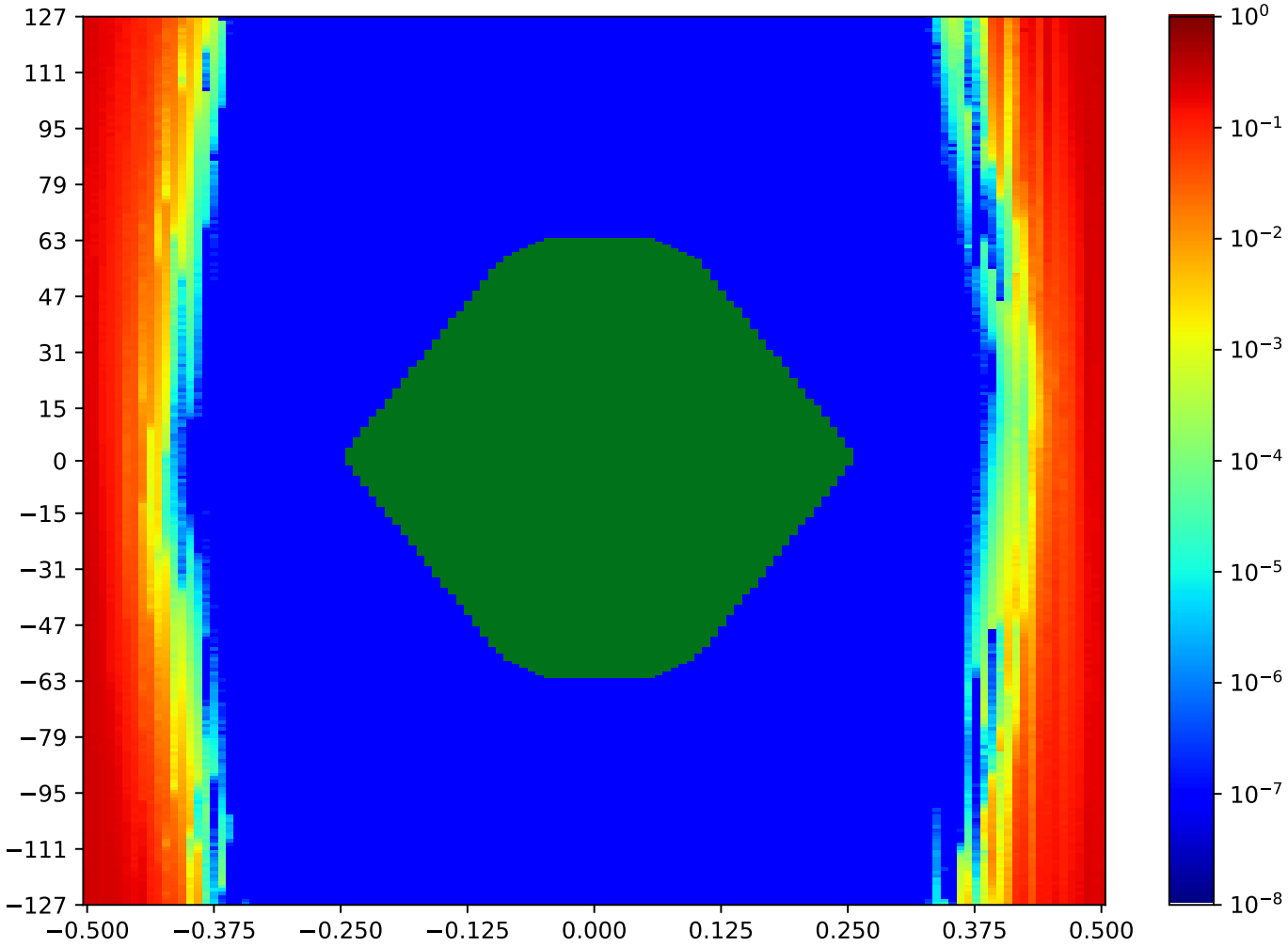


Figure 3.4: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.4 MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Table 3.4: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:41:59		2018-Sep-26 16:43:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24702	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

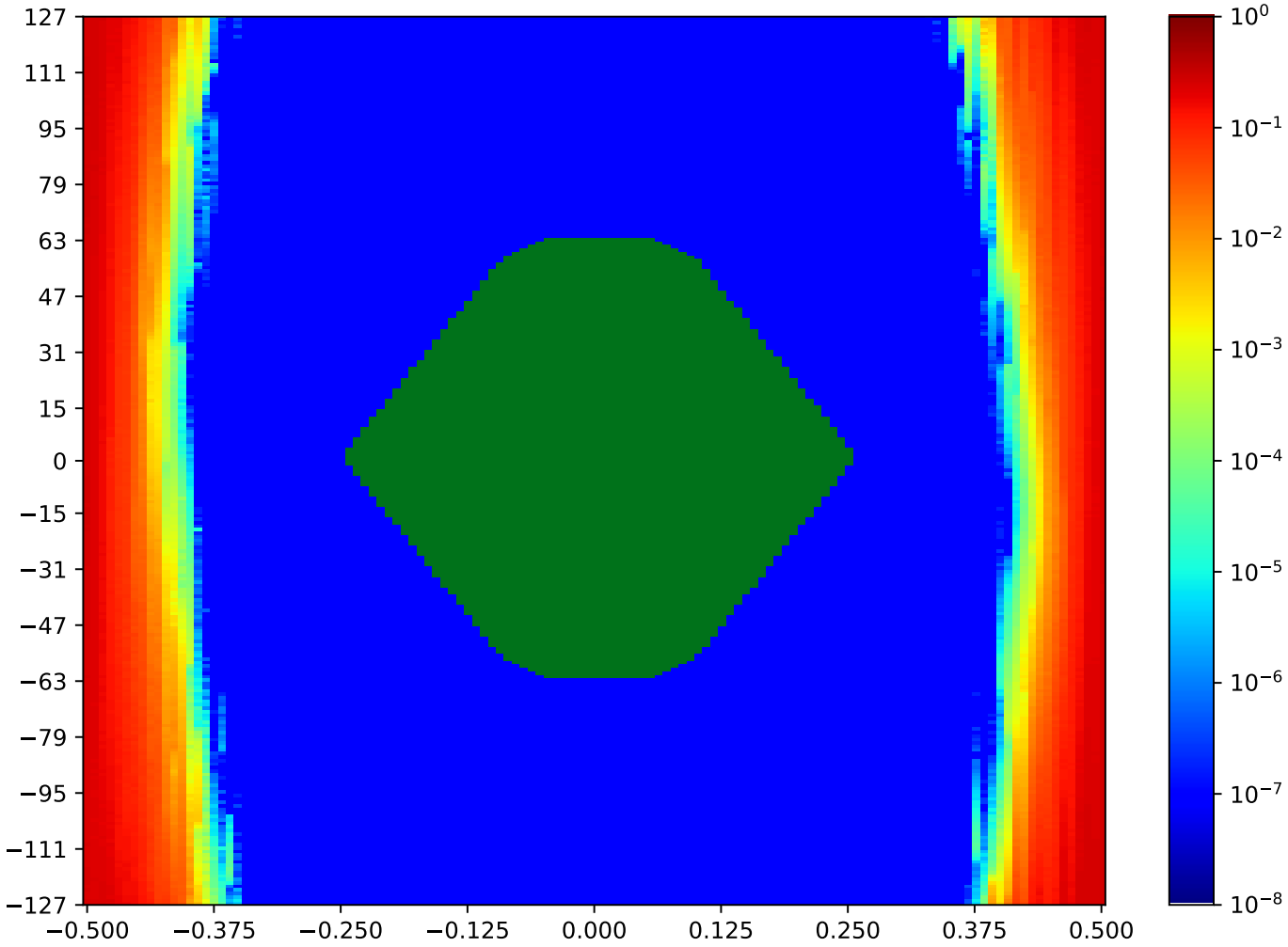


Figure 3.5: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.5 MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Table 3.5: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:51:55		2018-Sep-26 16:53:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24615	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

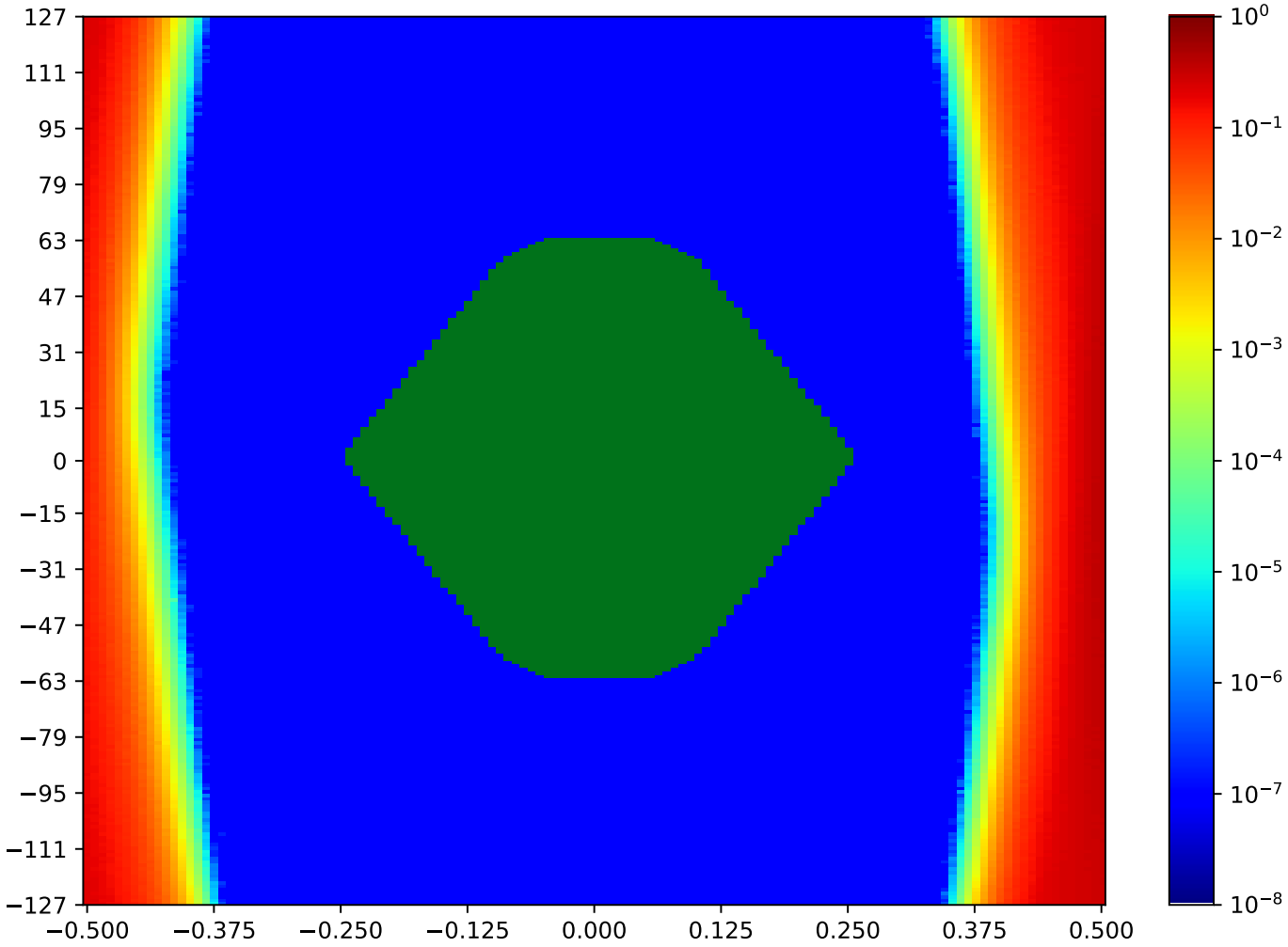


Figure 3.6: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.6 MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Table 3.6: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:40:45		2018-Sep-26 16:41:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24643	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

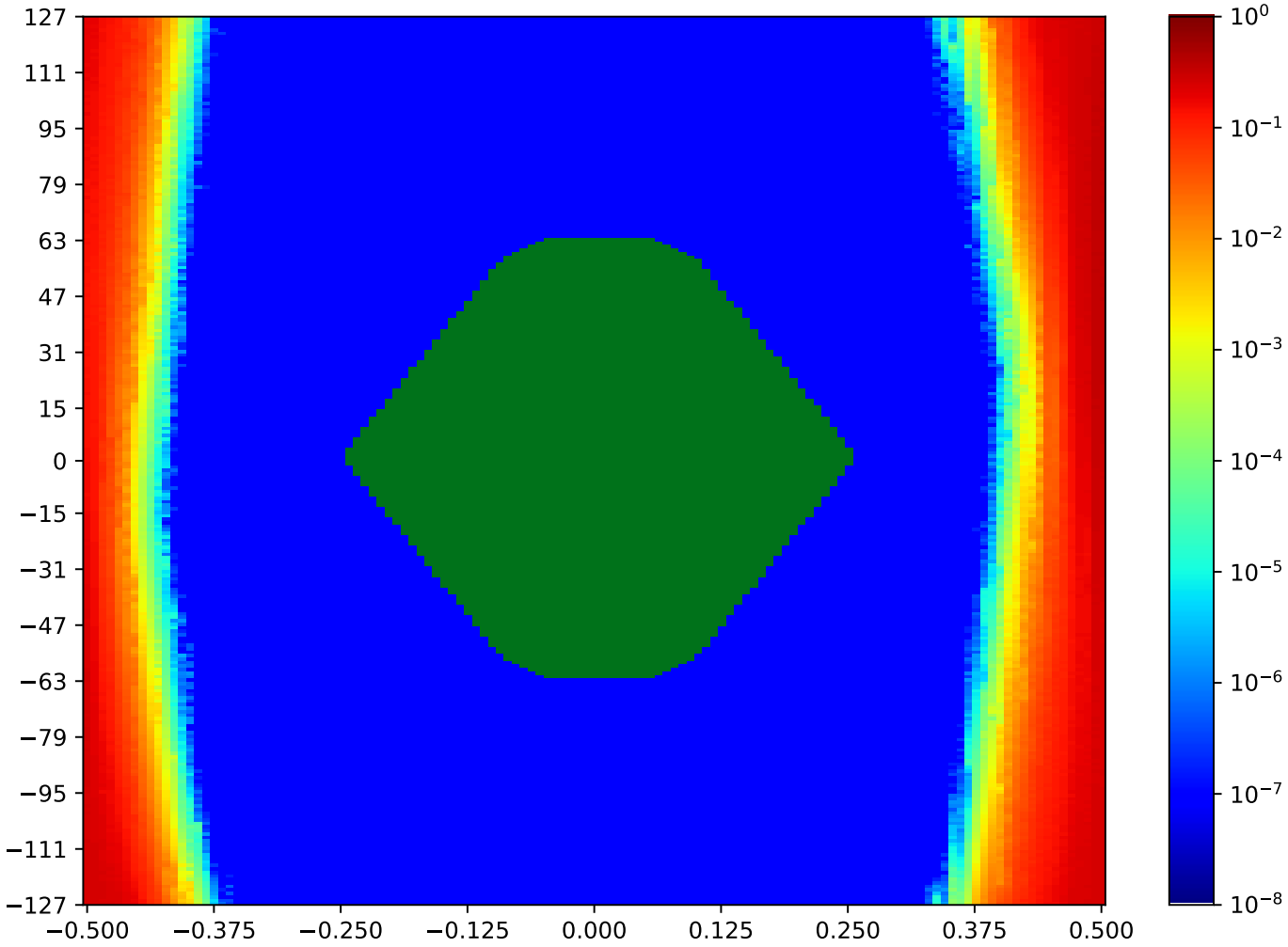


Figure 3.7: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.7 MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Table 3.7: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:54:24		2018-Sep-26 16:55:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24542	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

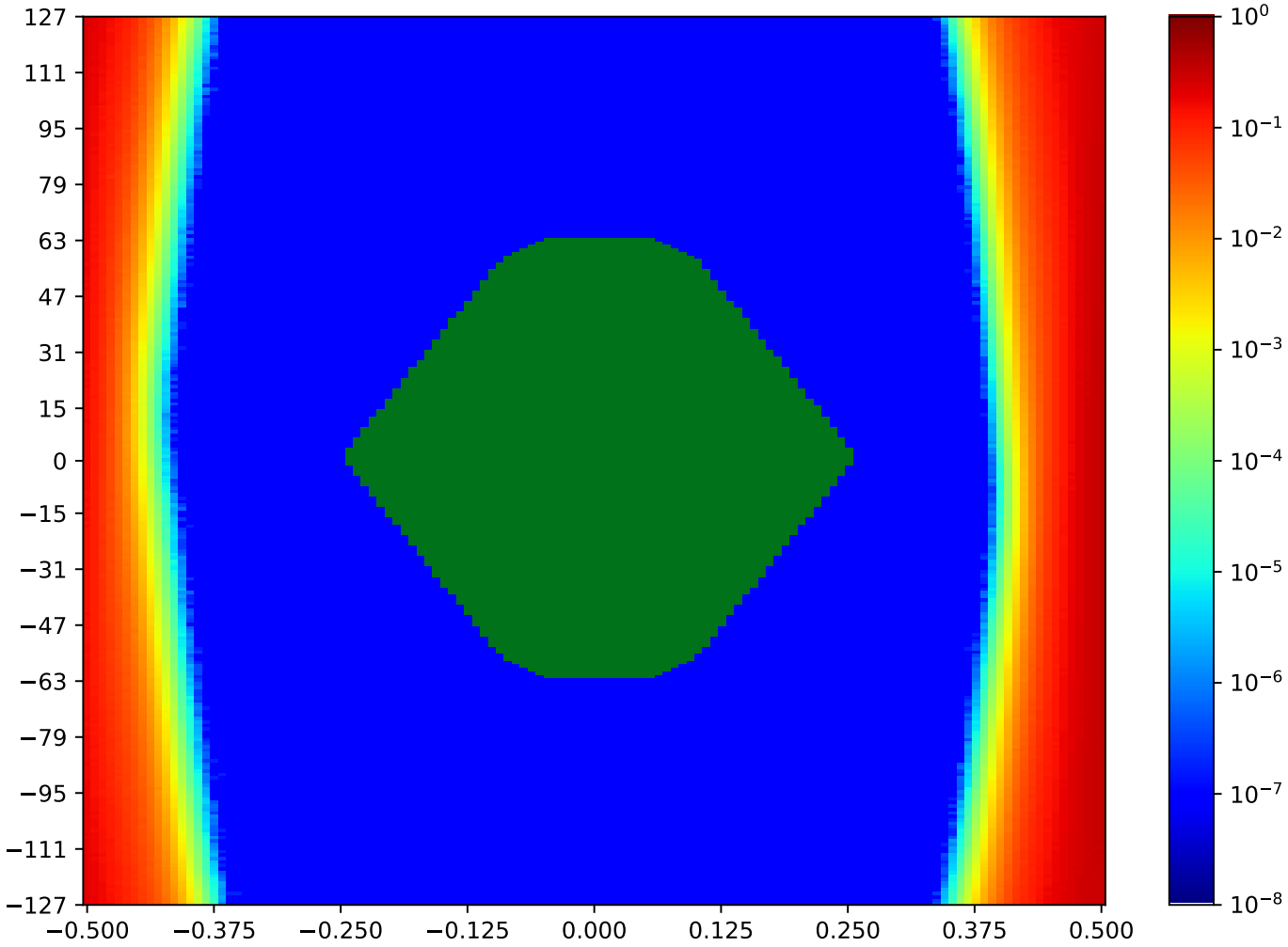


Figure 3.8: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.8 MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Table 3.8: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:43:14		2018-Sep-26 16:44:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25354	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

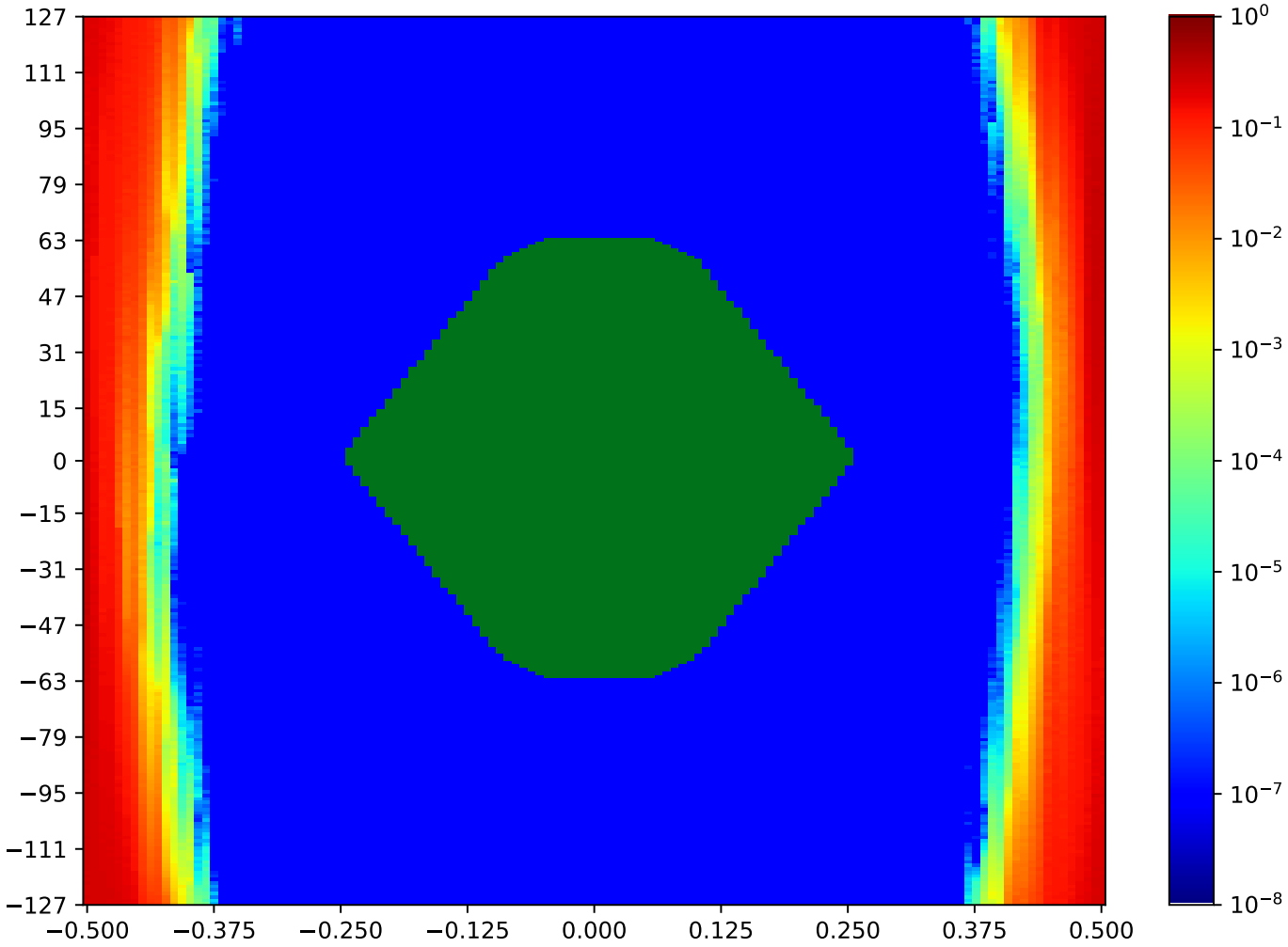


Figure 3.9: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.9 MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Table 3.9: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:53:09		2018-Sep-26 16:54:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24555	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

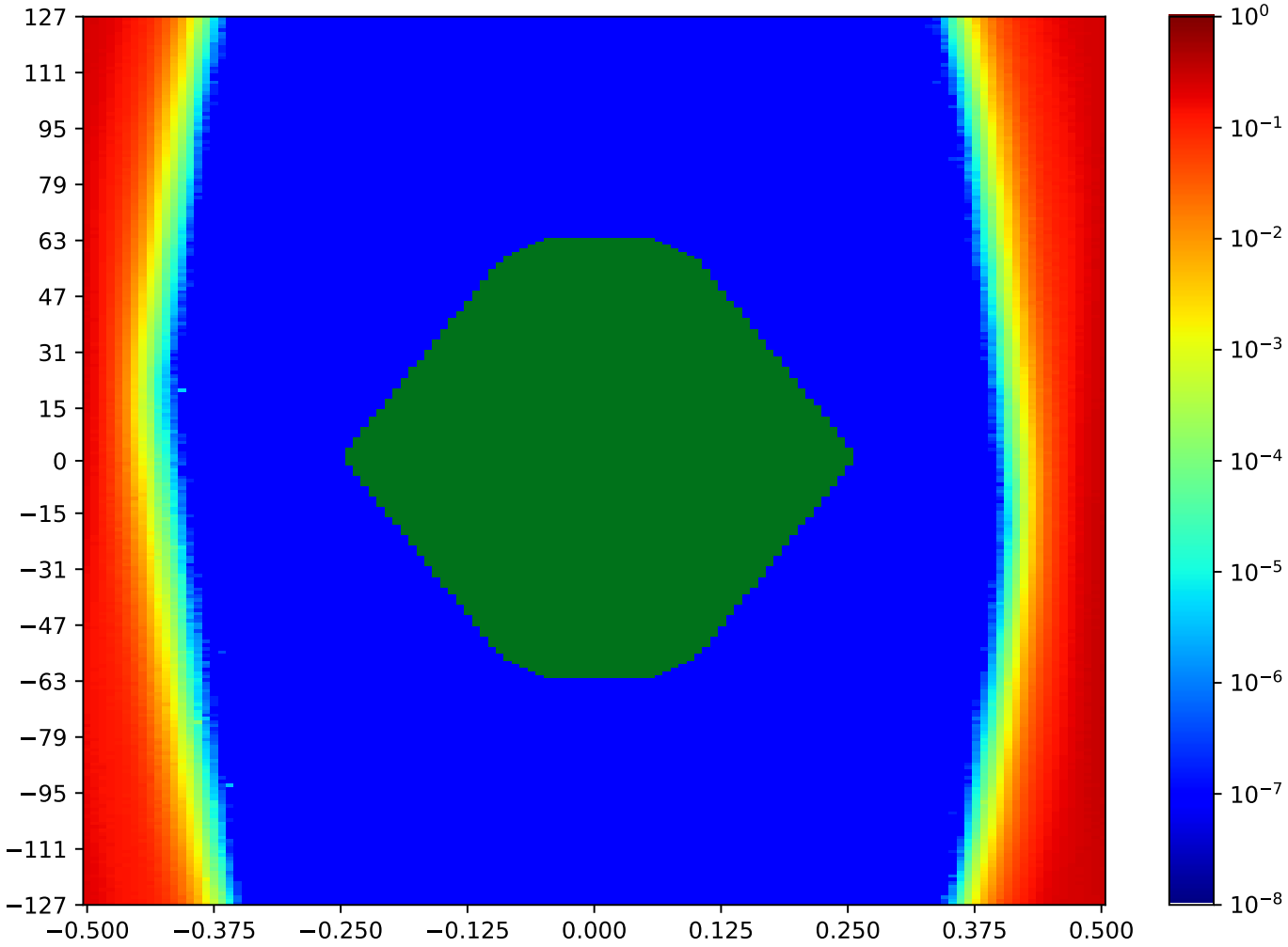


Figure 3.10: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.10 MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Table 3.10: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:45:43		2018-Sep-26 16:46:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24620	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

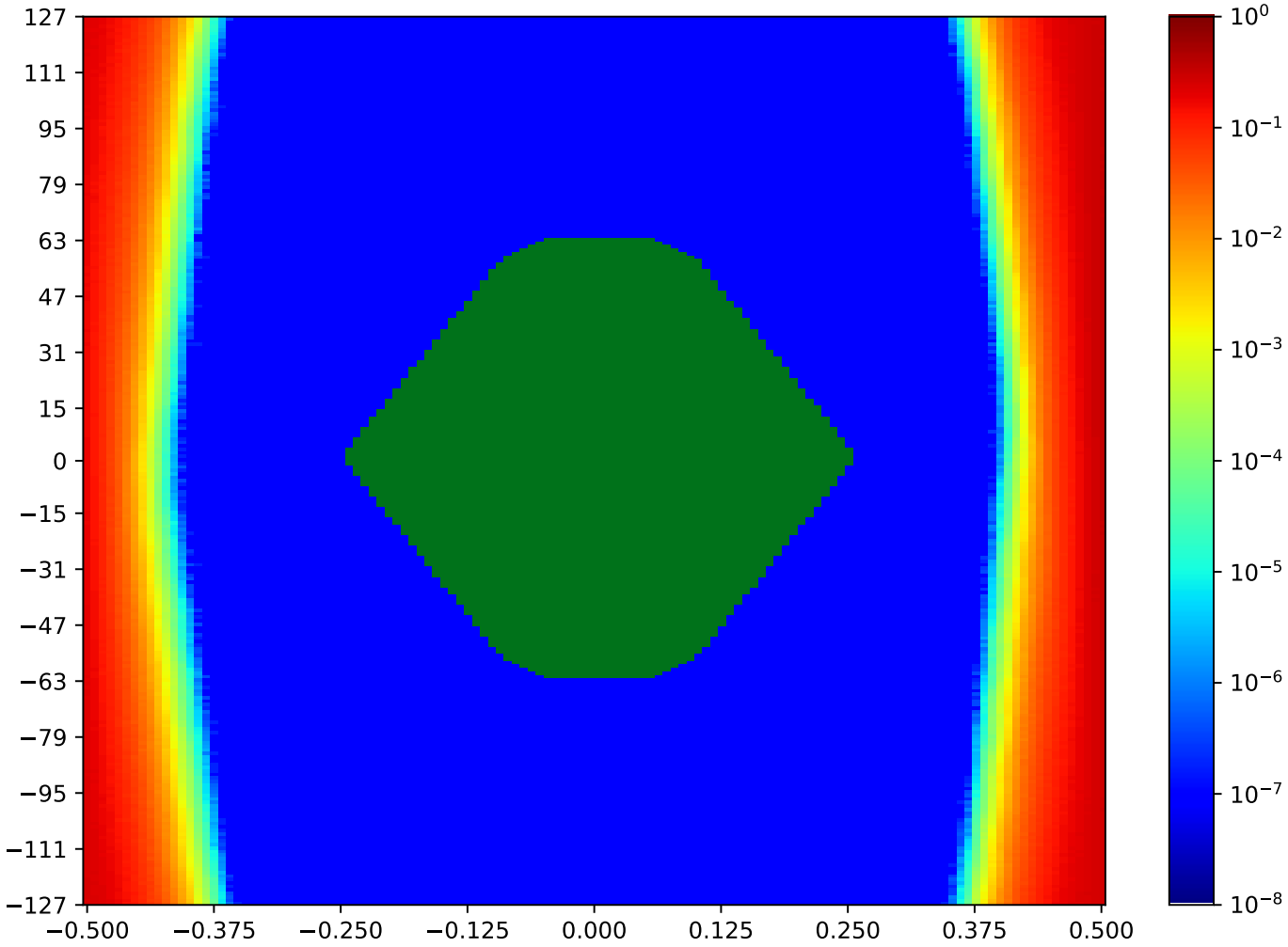


Figure 3.11: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.11 MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Table 3.11: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:50:41		2018-Sep-26 16:51:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23820	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

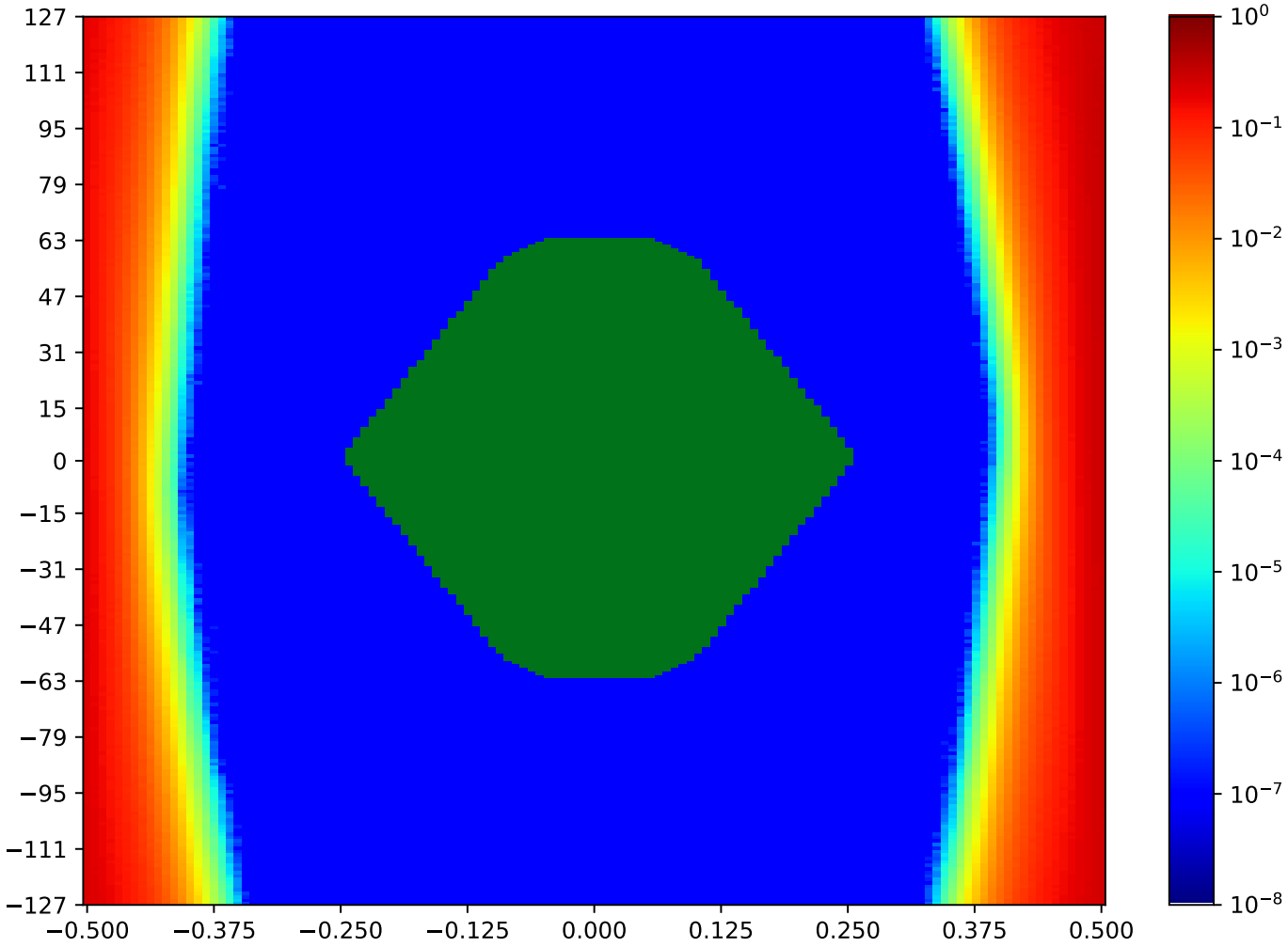


Figure 3.12: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.1.12 MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Table 3.12: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:49:27		2018-Sep-26 16:50:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24230	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

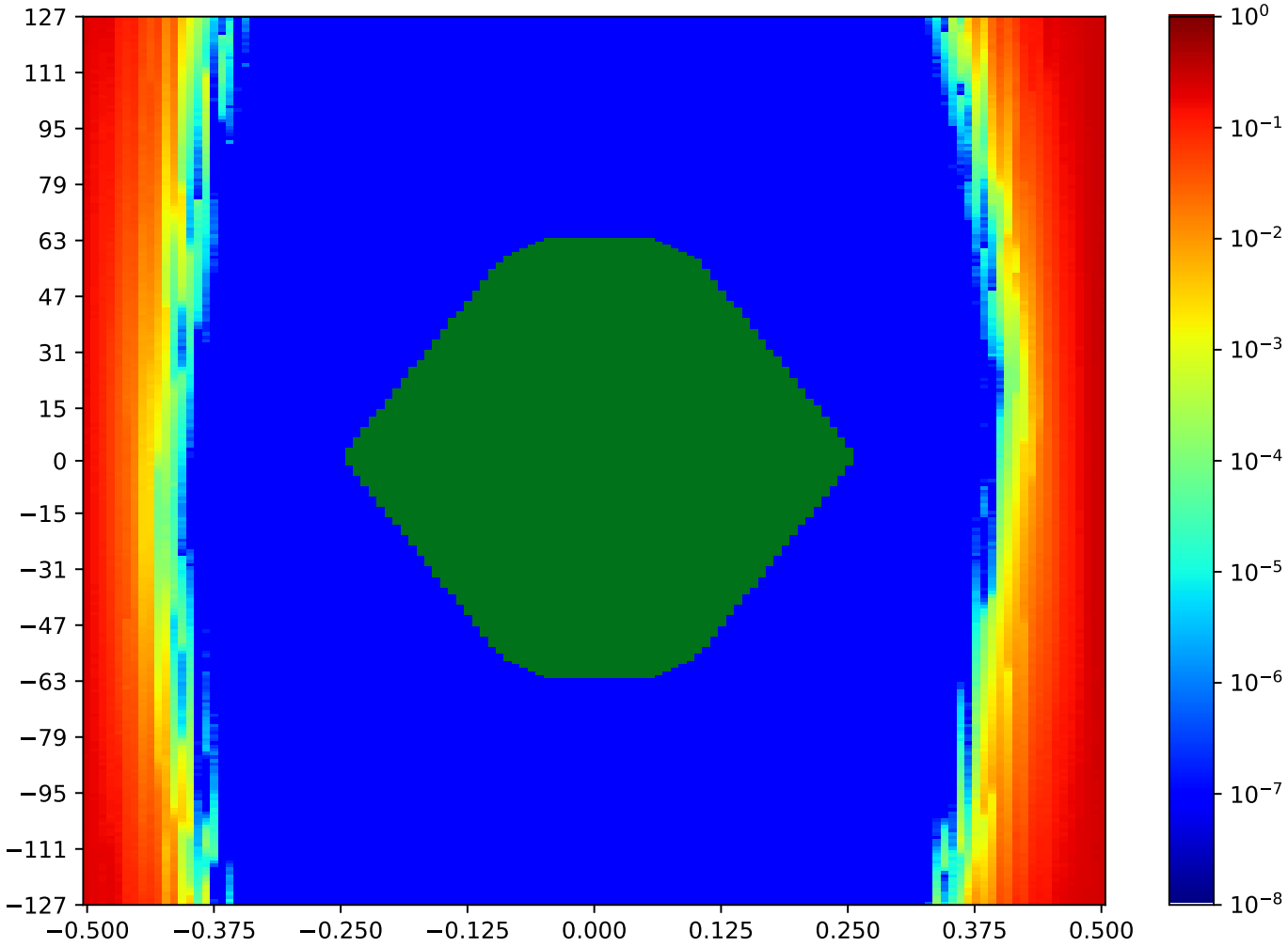


Figure 3.13: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2 MSP_A TX2 MSP_C RX16 Minipod Loopback

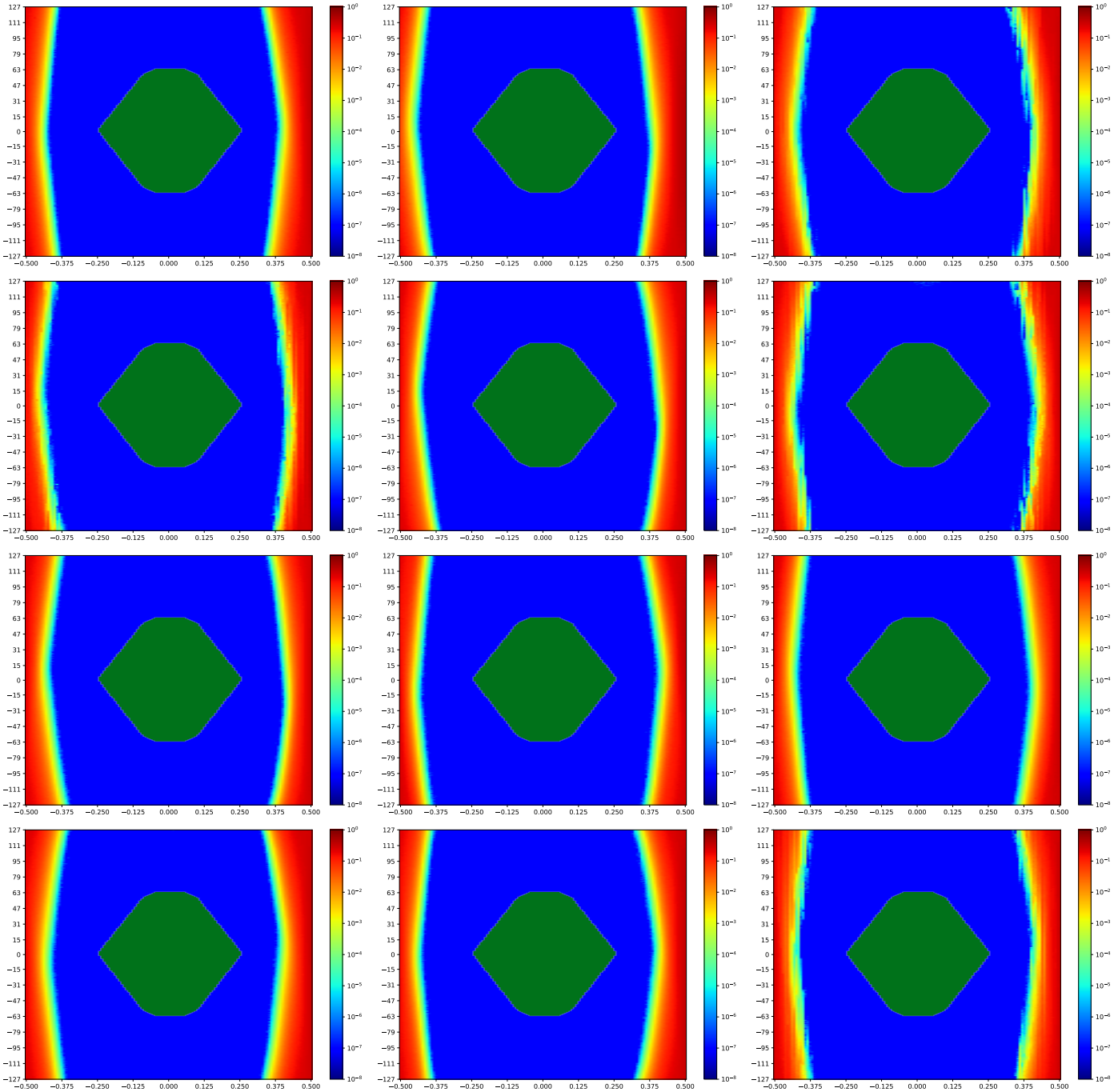


Figure 3.14: MSP_A TX2 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.27.

3.2.1 MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Table 3.13: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:59:24		2018-Sep-26 17:00:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24312	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

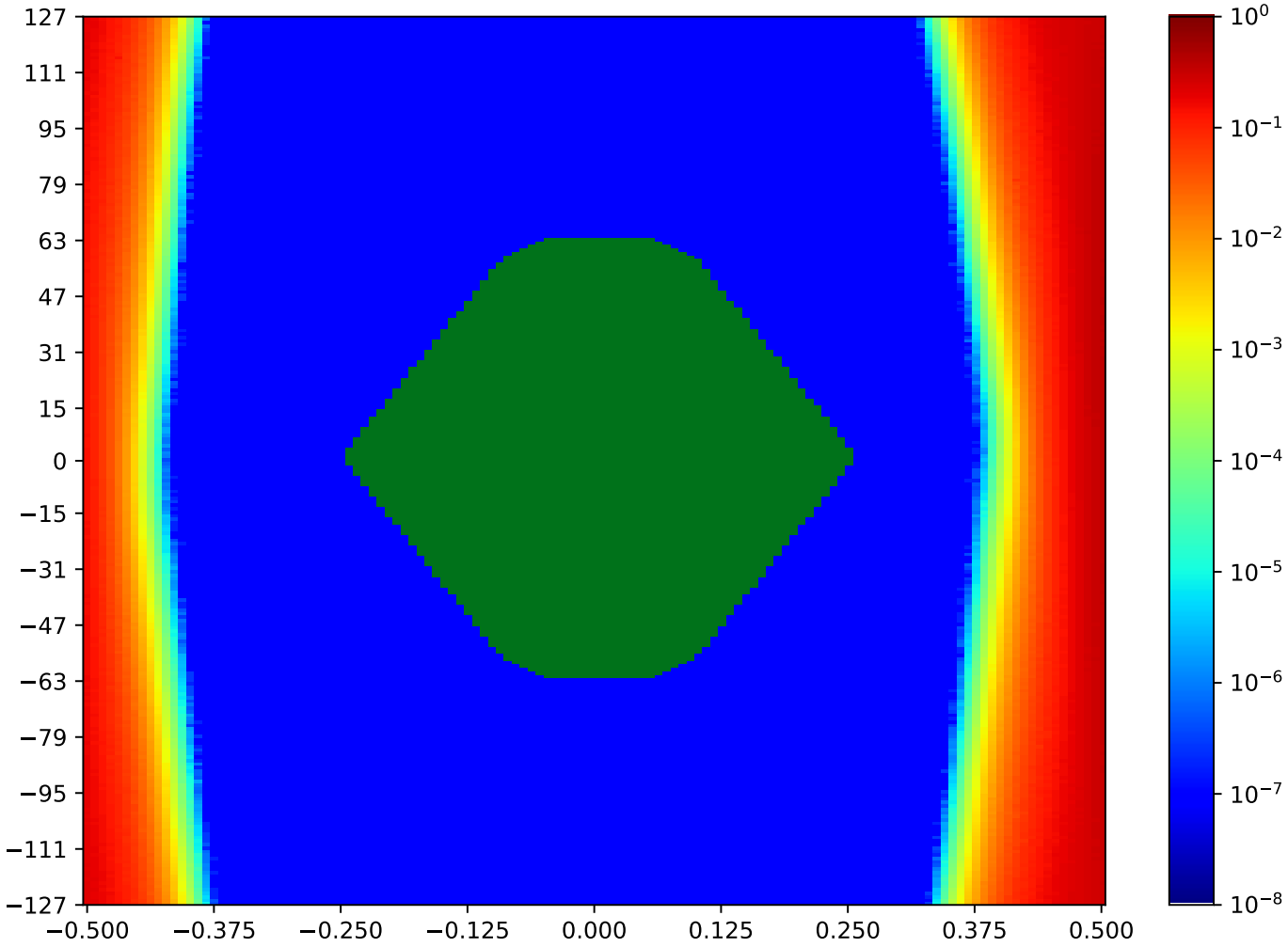


Figure 3.15: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.2 MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Table 3.14: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:56:54		2018-Sep-26 16:58:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24387	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

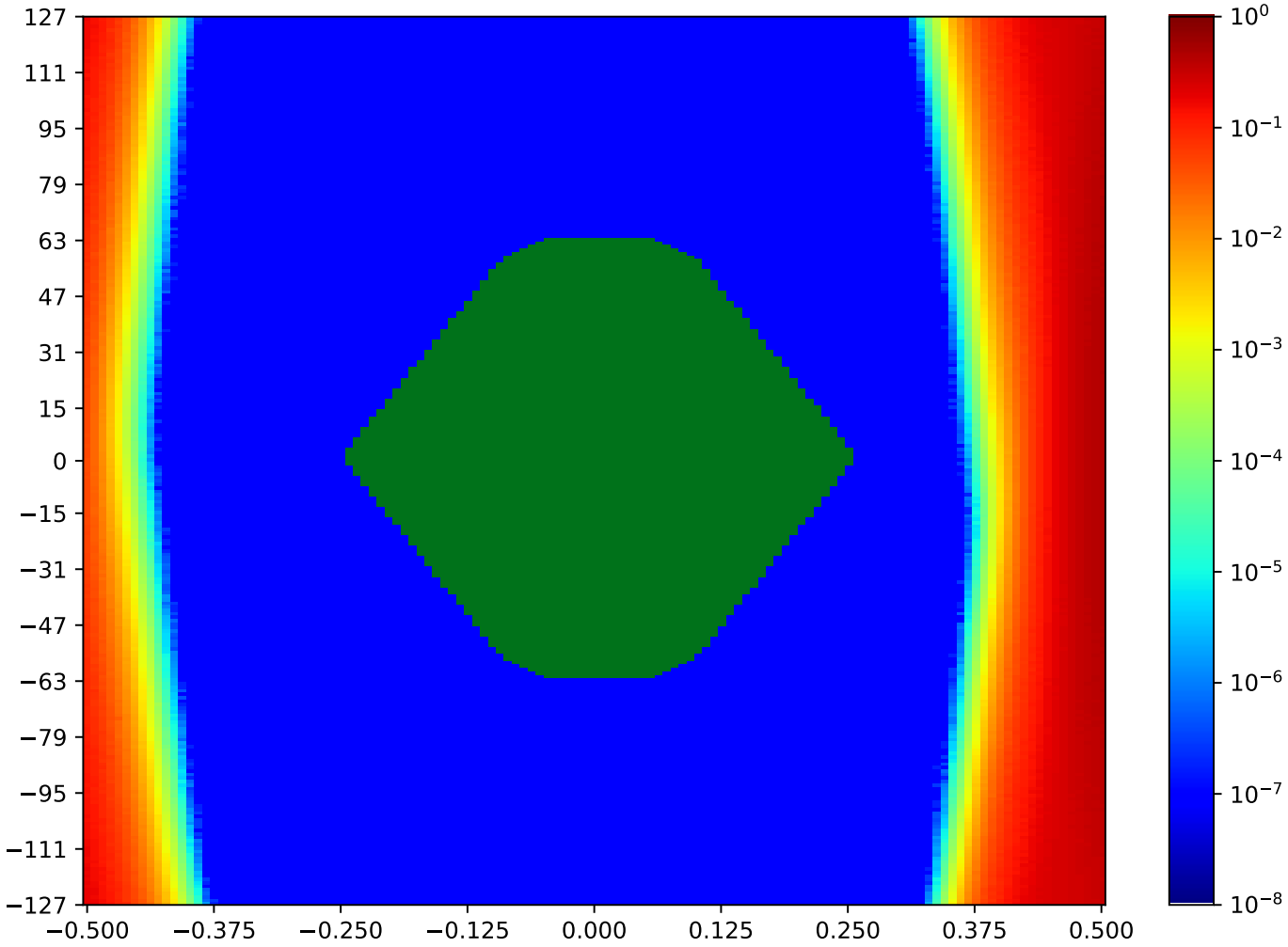


Figure 3.16: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.3 MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Table 3.15: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:03:09		2018-Sep-26 17:04:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24119	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

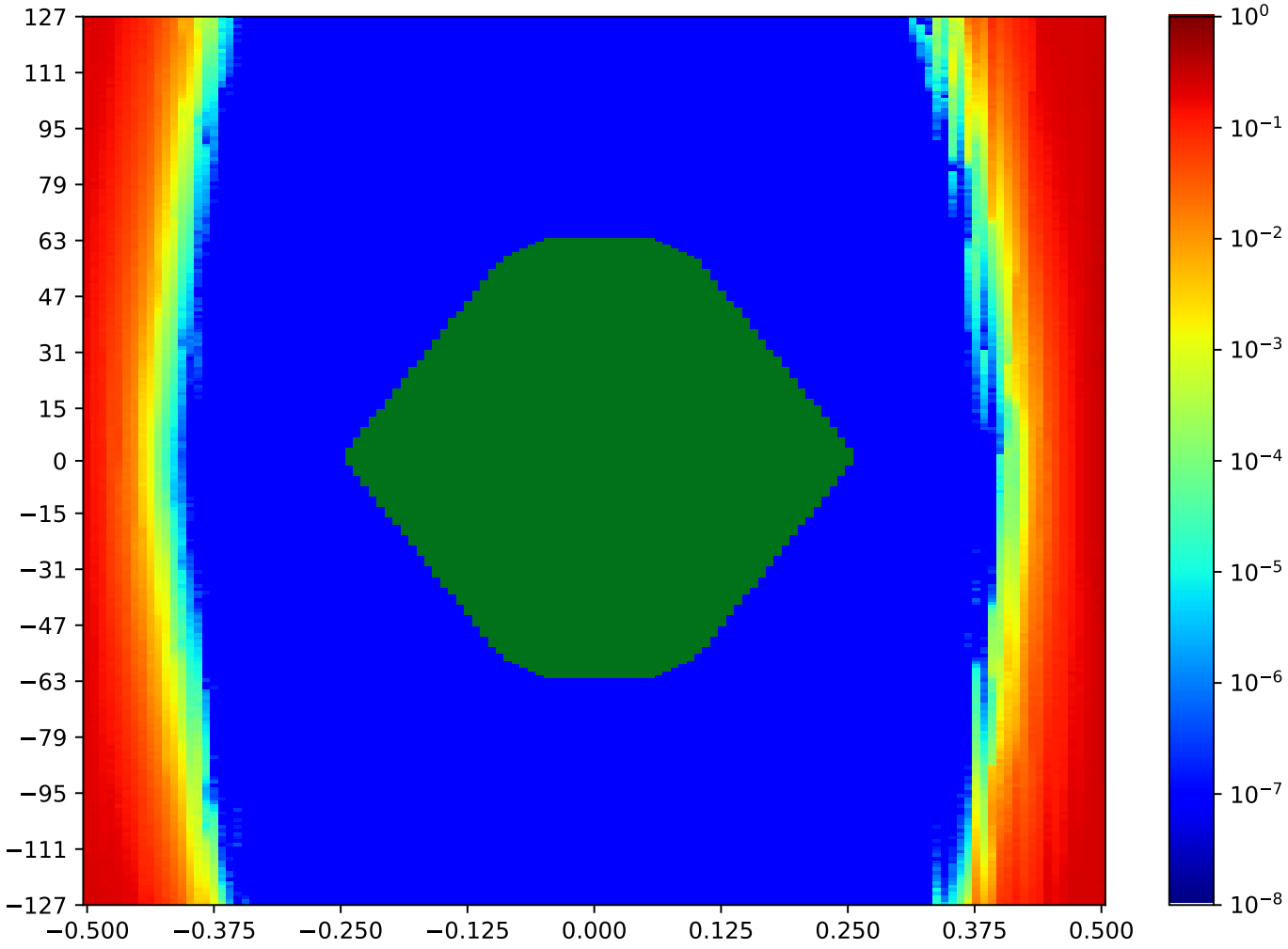


Figure 3.17: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.4 MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Table 3.16: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:55:39		2018-Sep-26 16:56:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25382	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

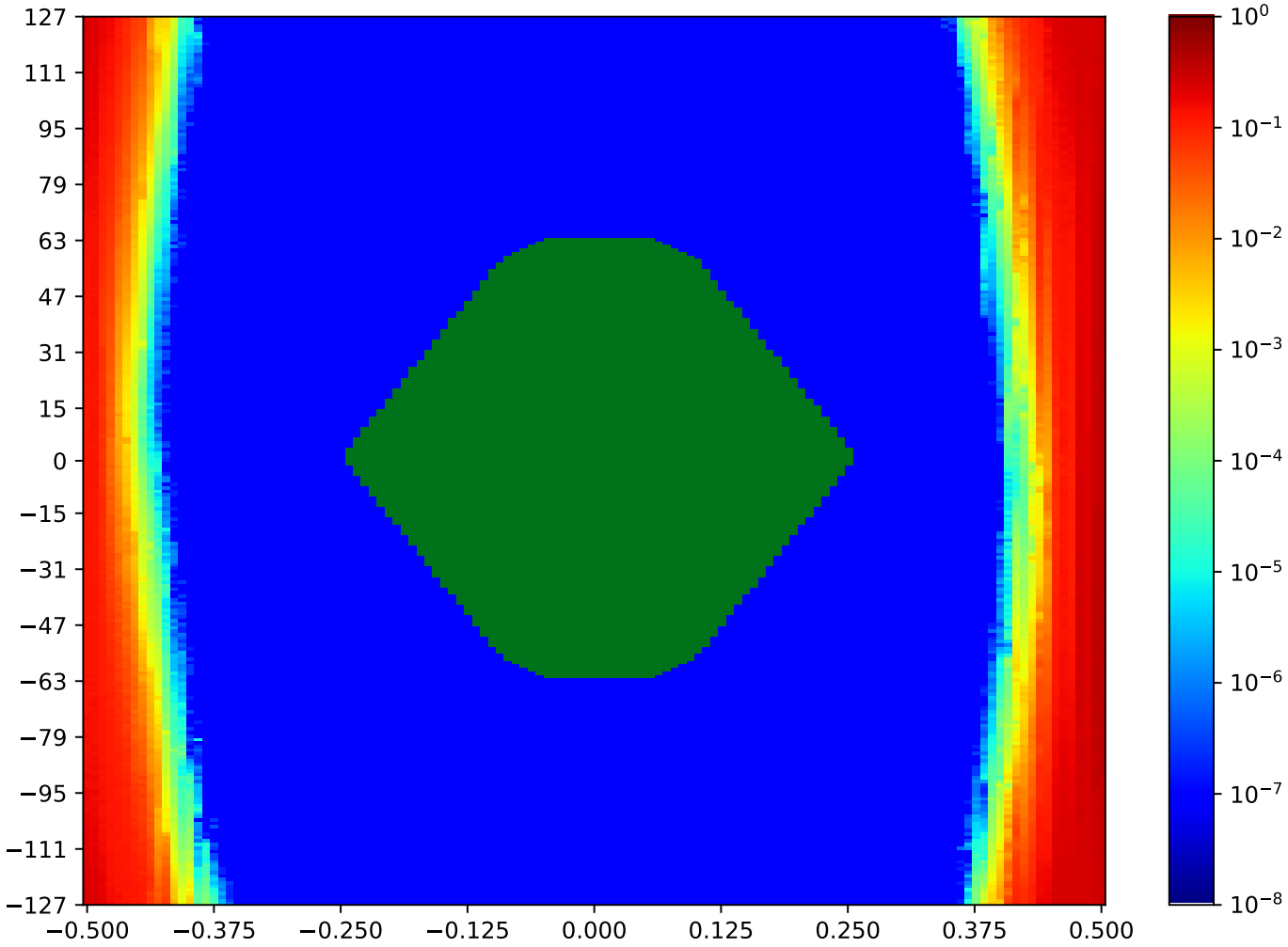


Figure 3.18: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.5 MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Table 3.17: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:06:55		2018-Sep-26 17:08:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24484	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

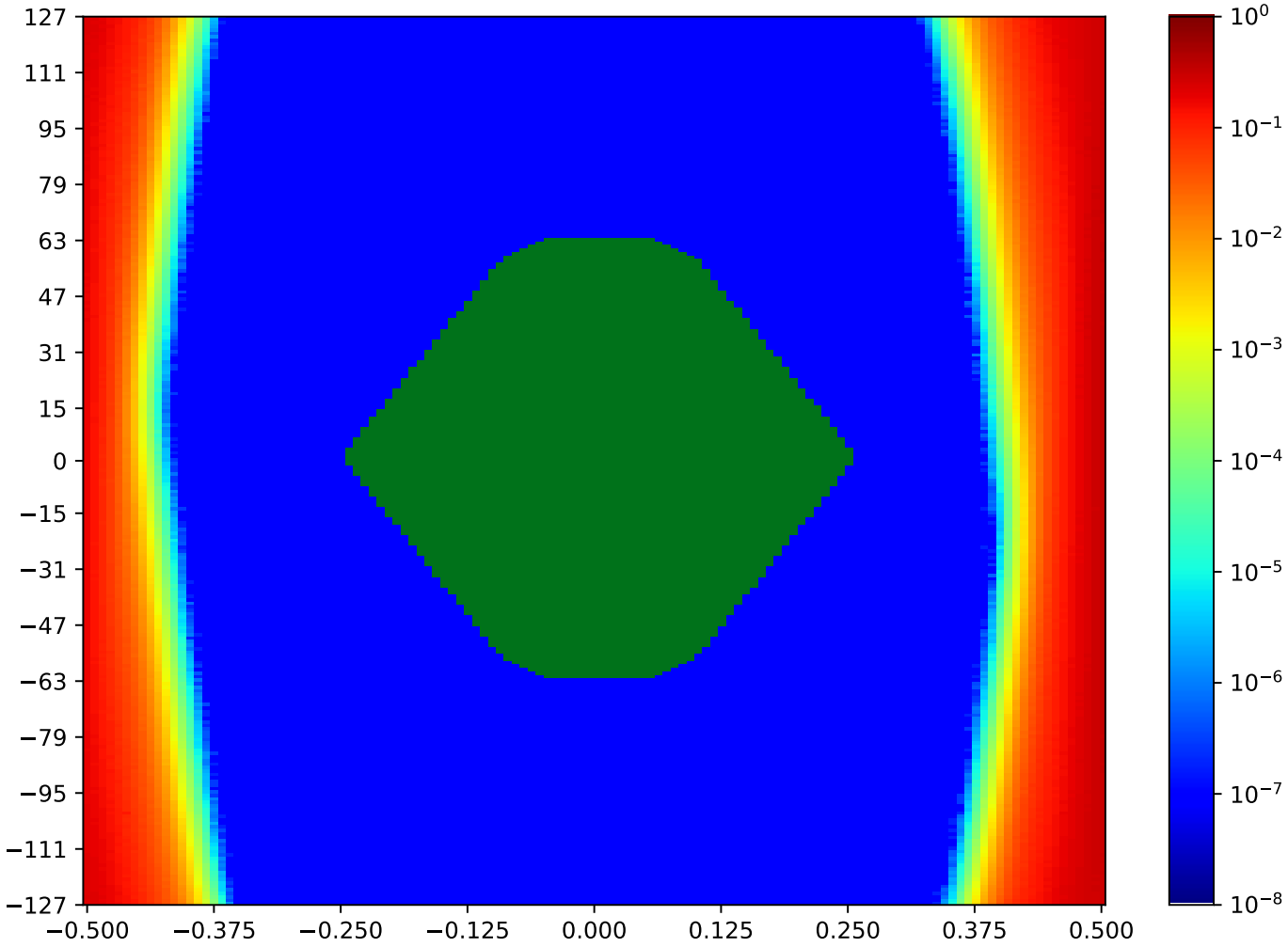


Figure 3.19: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.6 MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Table 3.18: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:58:08		2018-Sep-26 16:59:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24436	104	80.62%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

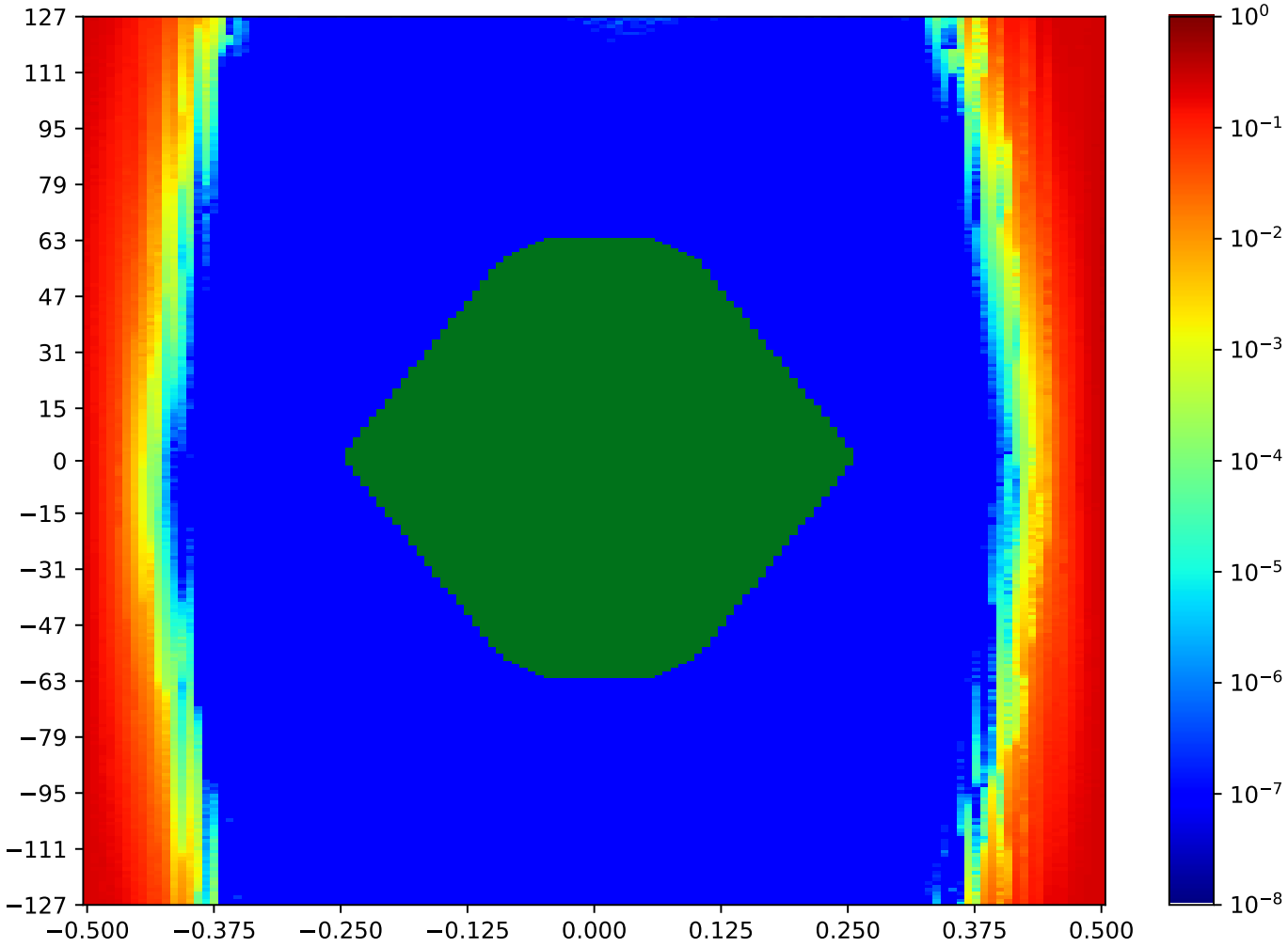


Figure 3.20: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.7 MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Table 3.19: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:09:26		2018-Sep-26 17:10:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24497	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

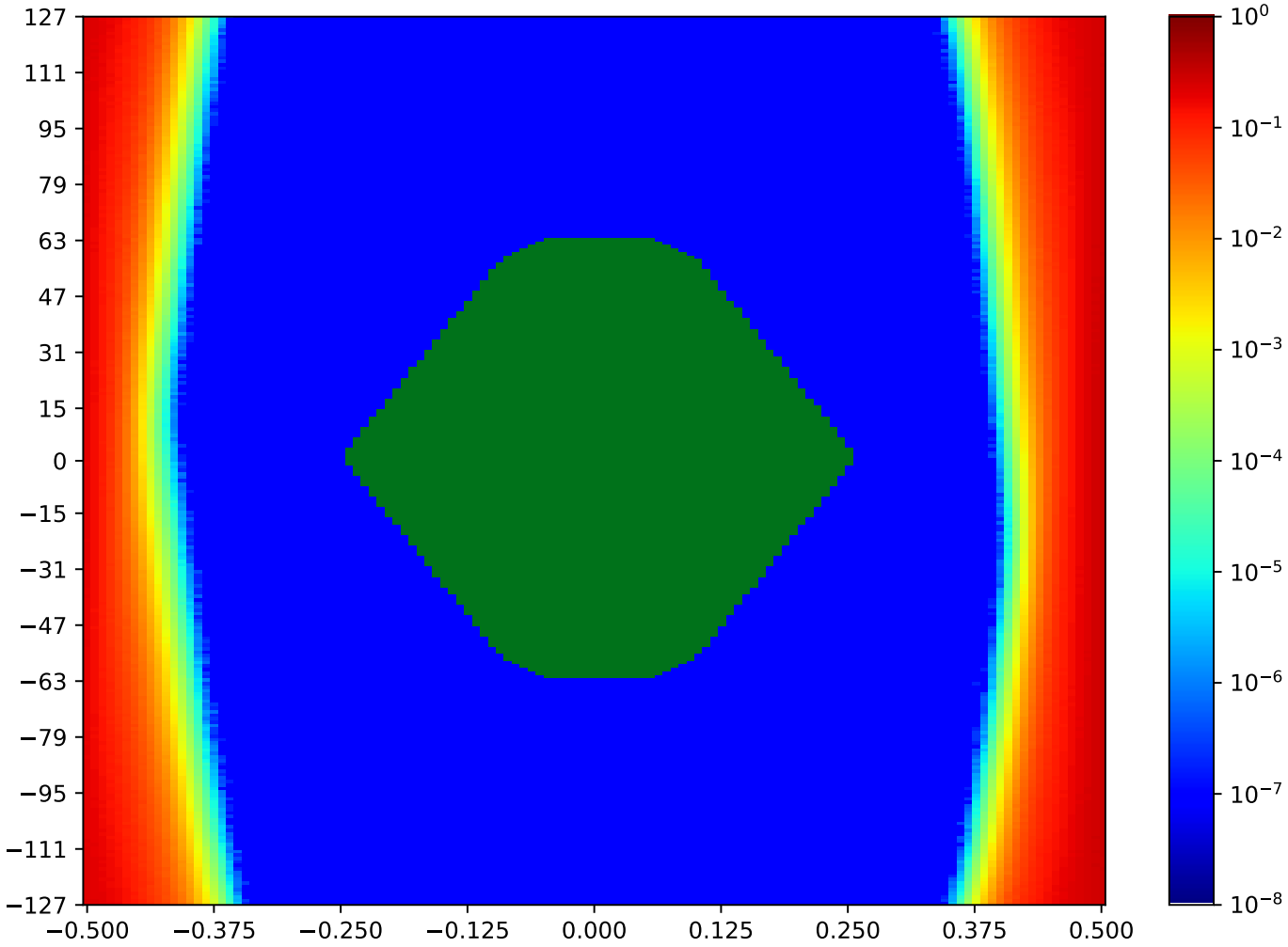


Figure 3.21: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.8 MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Table 3.20: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:00:39		2018-Sep-26 17:01:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24939	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

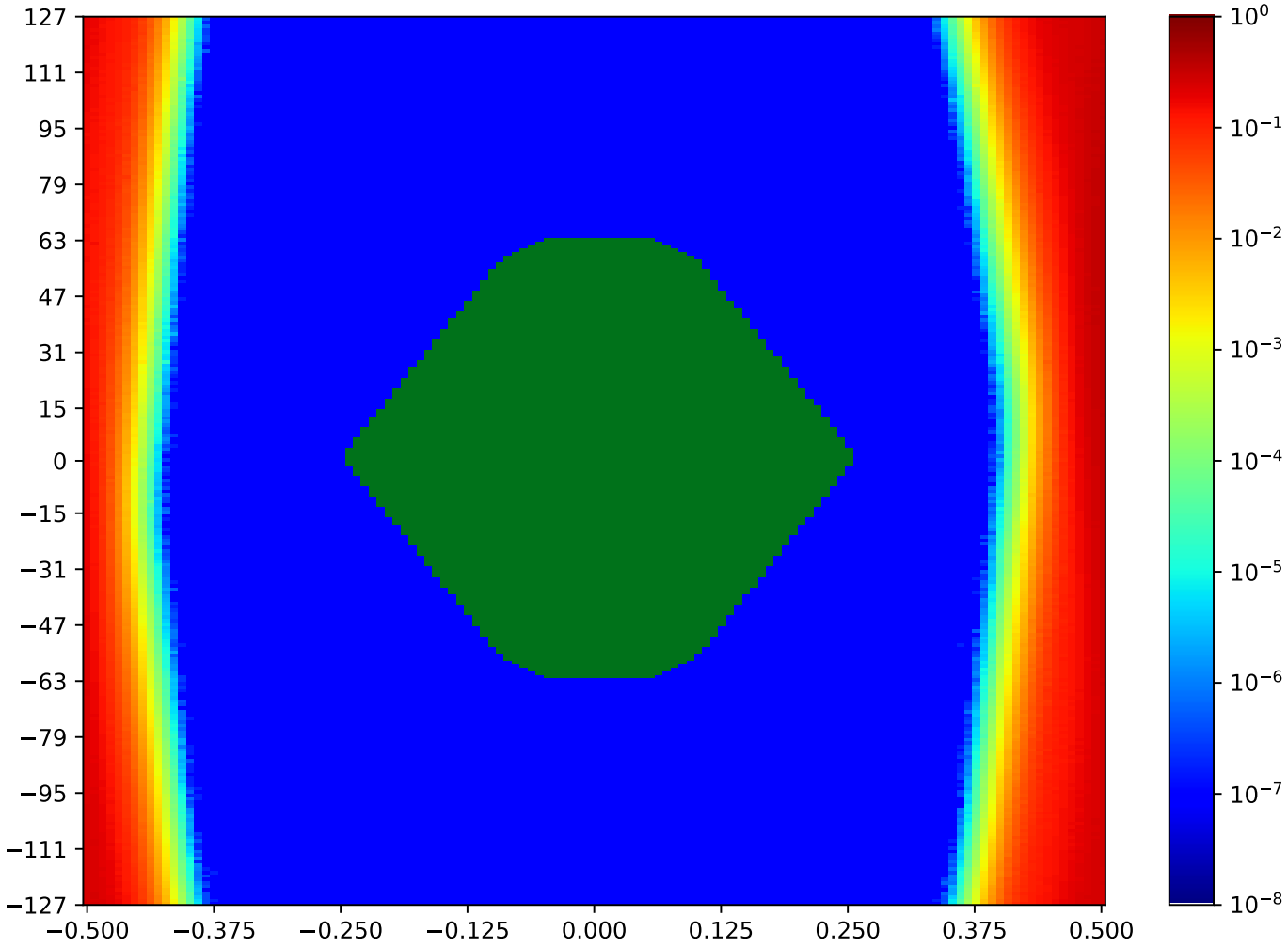


Figure 3.22: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.9 MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Table 3.21: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:08:10		2018-Sep-26 17:09:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24383	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

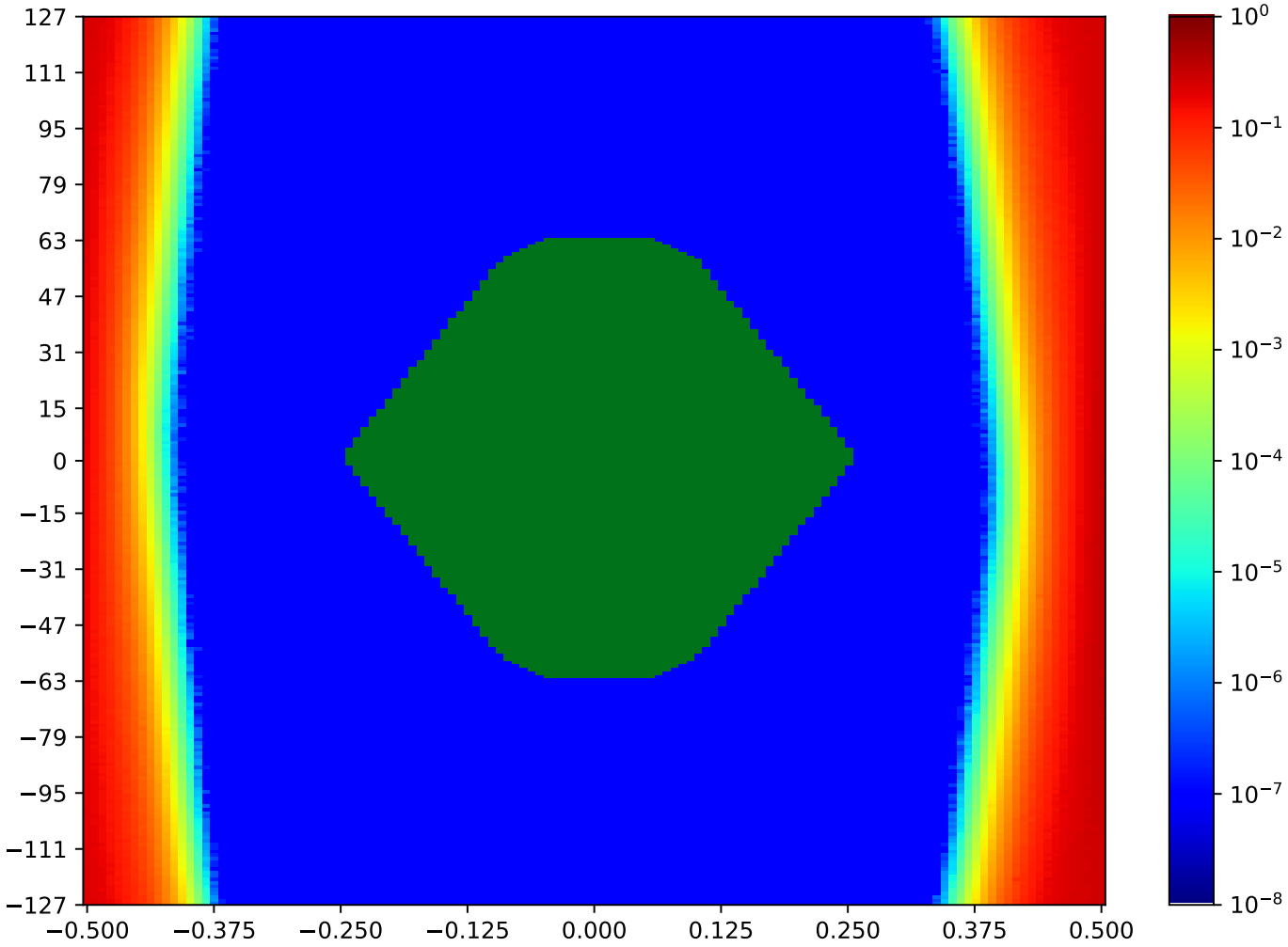


Figure 3.23: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.10 MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Table 3.22: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:01:54		2018-Sep-26 17:03:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23606	98	75.97%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

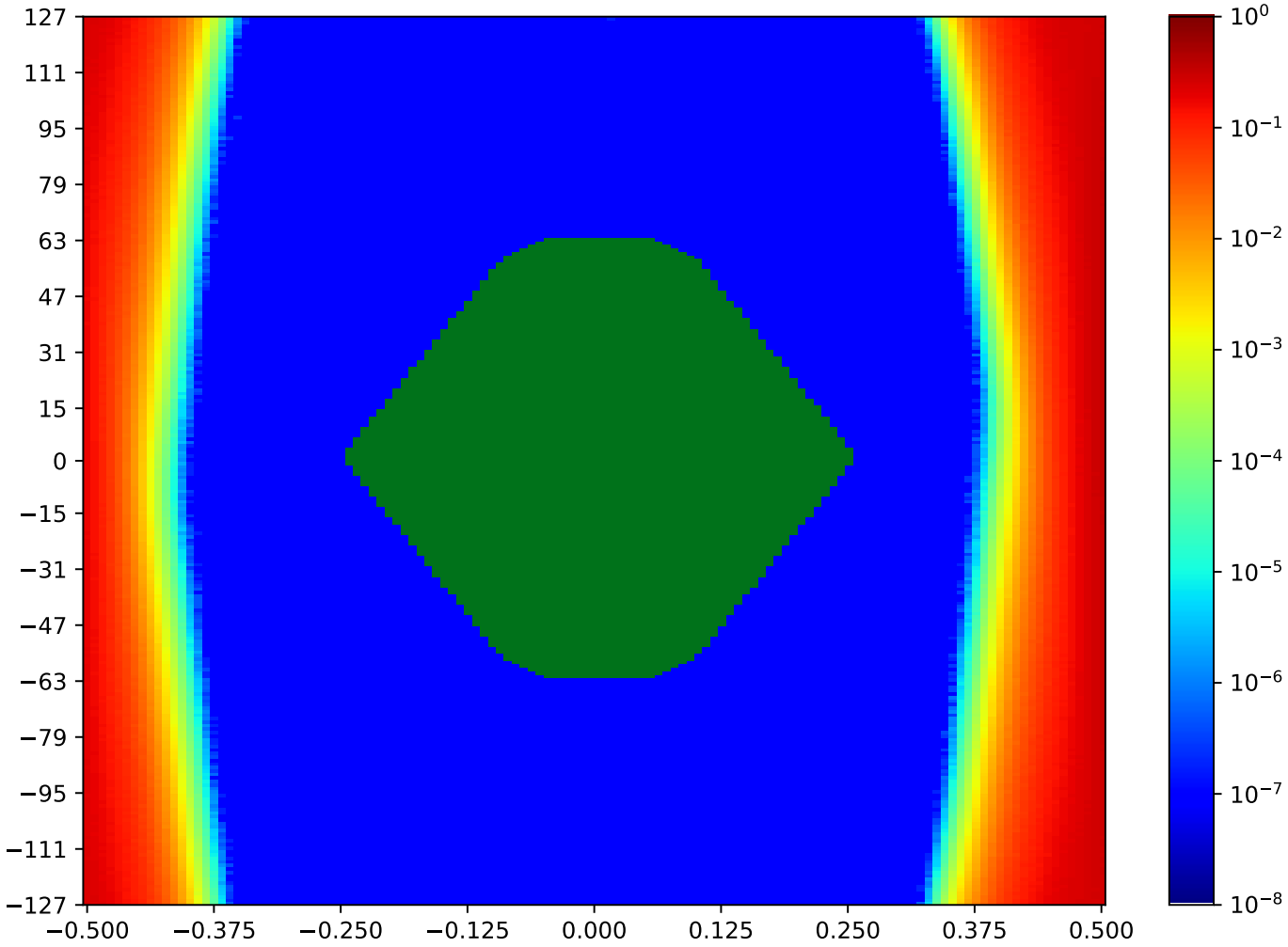


Figure 3.24: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.11 MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Table 3.23: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:05:40		2018-Sep-26 17:06:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24310	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

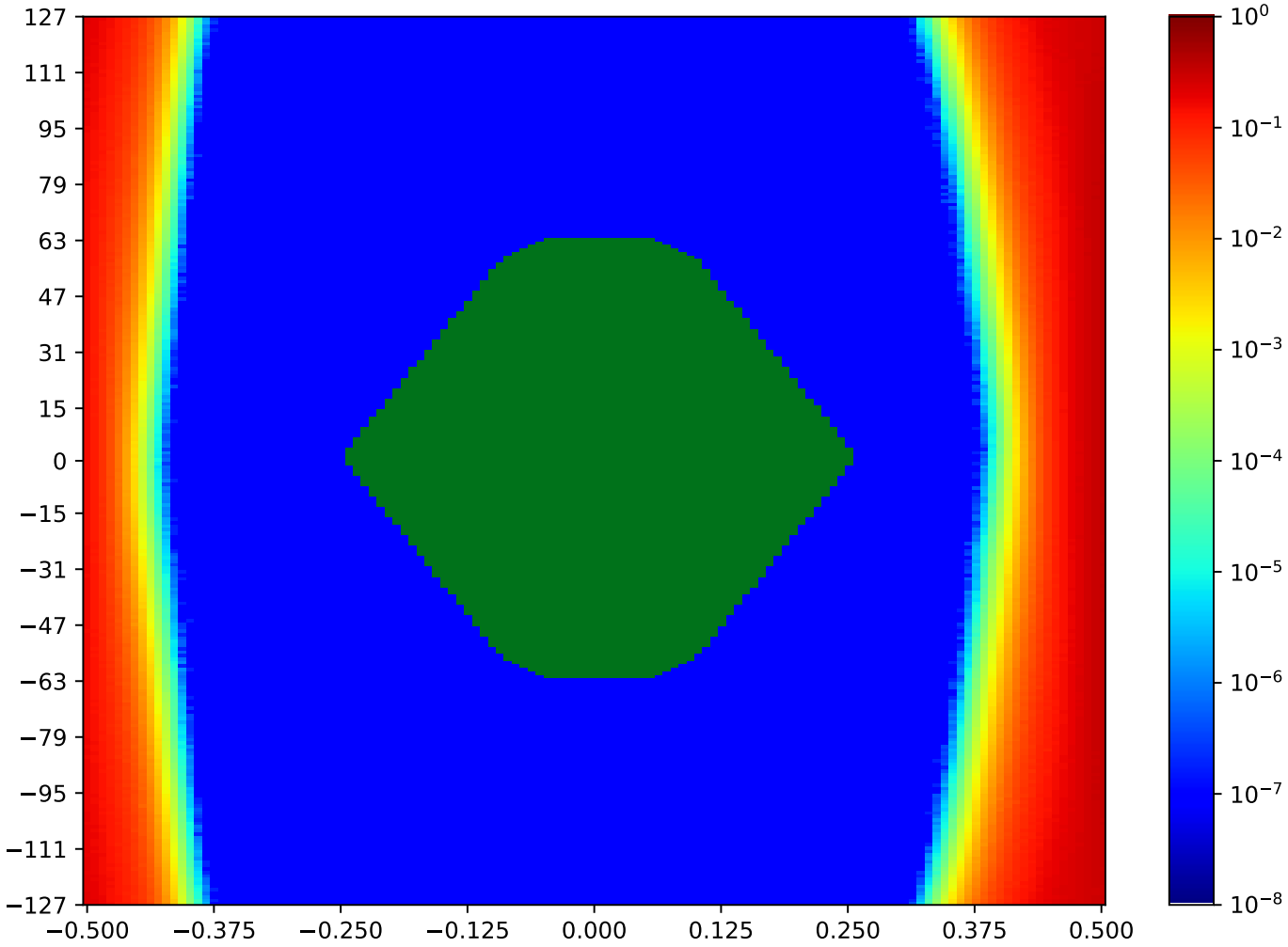


Figure 3.25: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.2.12 MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Table 3.24: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:04:24		2018-Sep-26 17:05:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24496	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

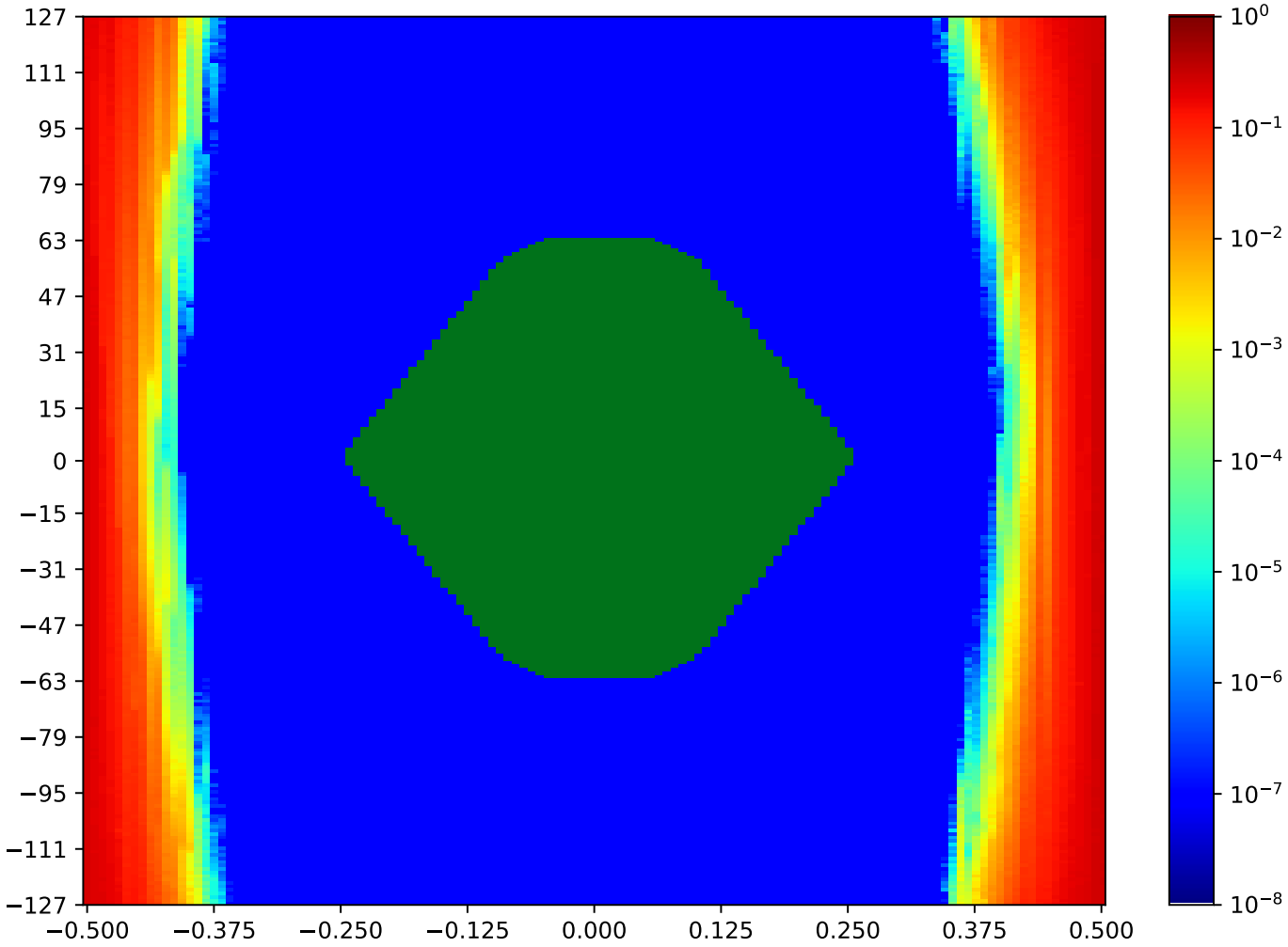


Figure 3.26: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3 MSP_C TX3 MSP_A RX6 Minipod Loopback

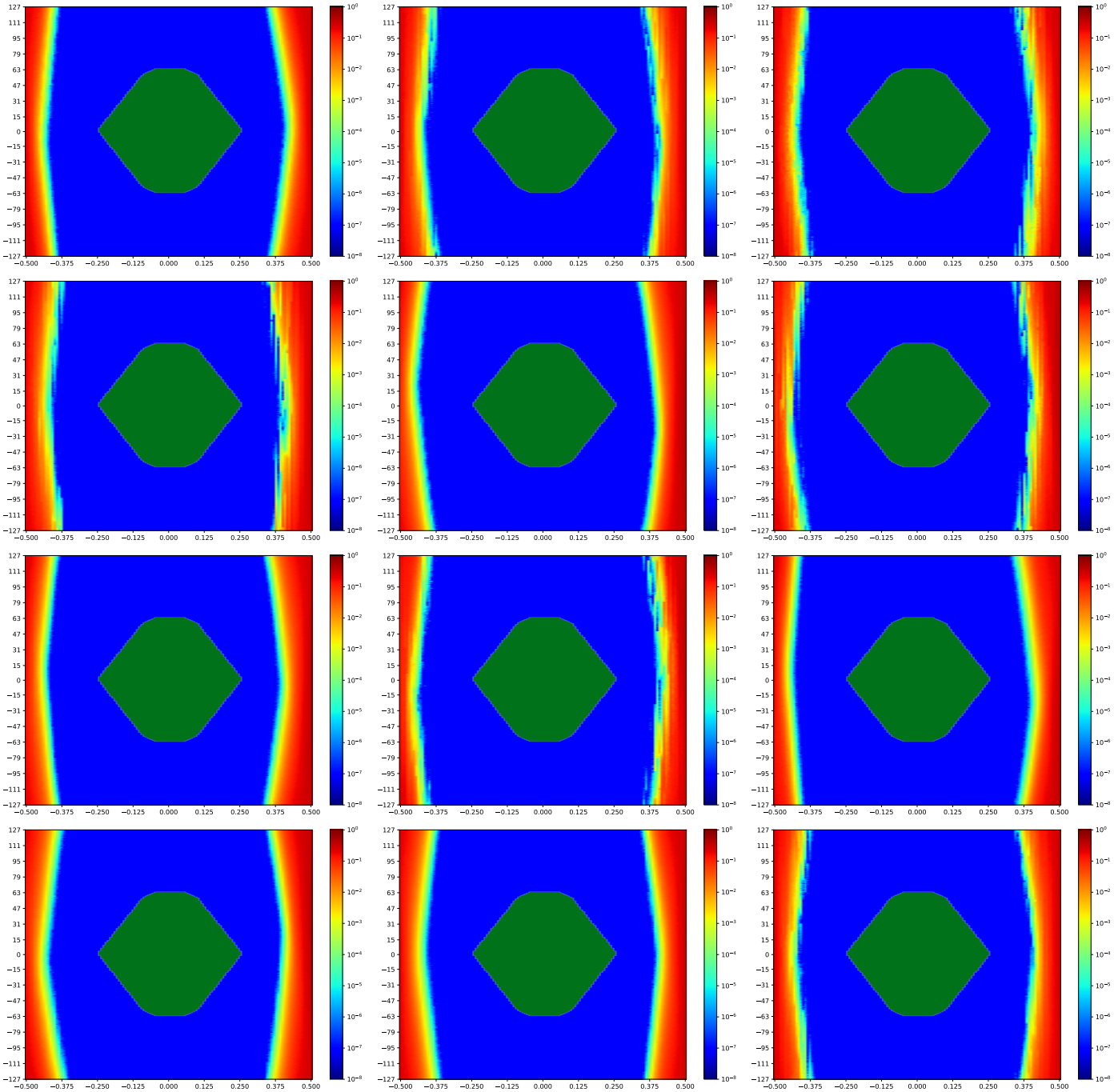


Figure 3.27: MSP_C TX3 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.40.

3.3.1 MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Table 3.25: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:14:31		2018-Sep-26 17:15:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25021	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

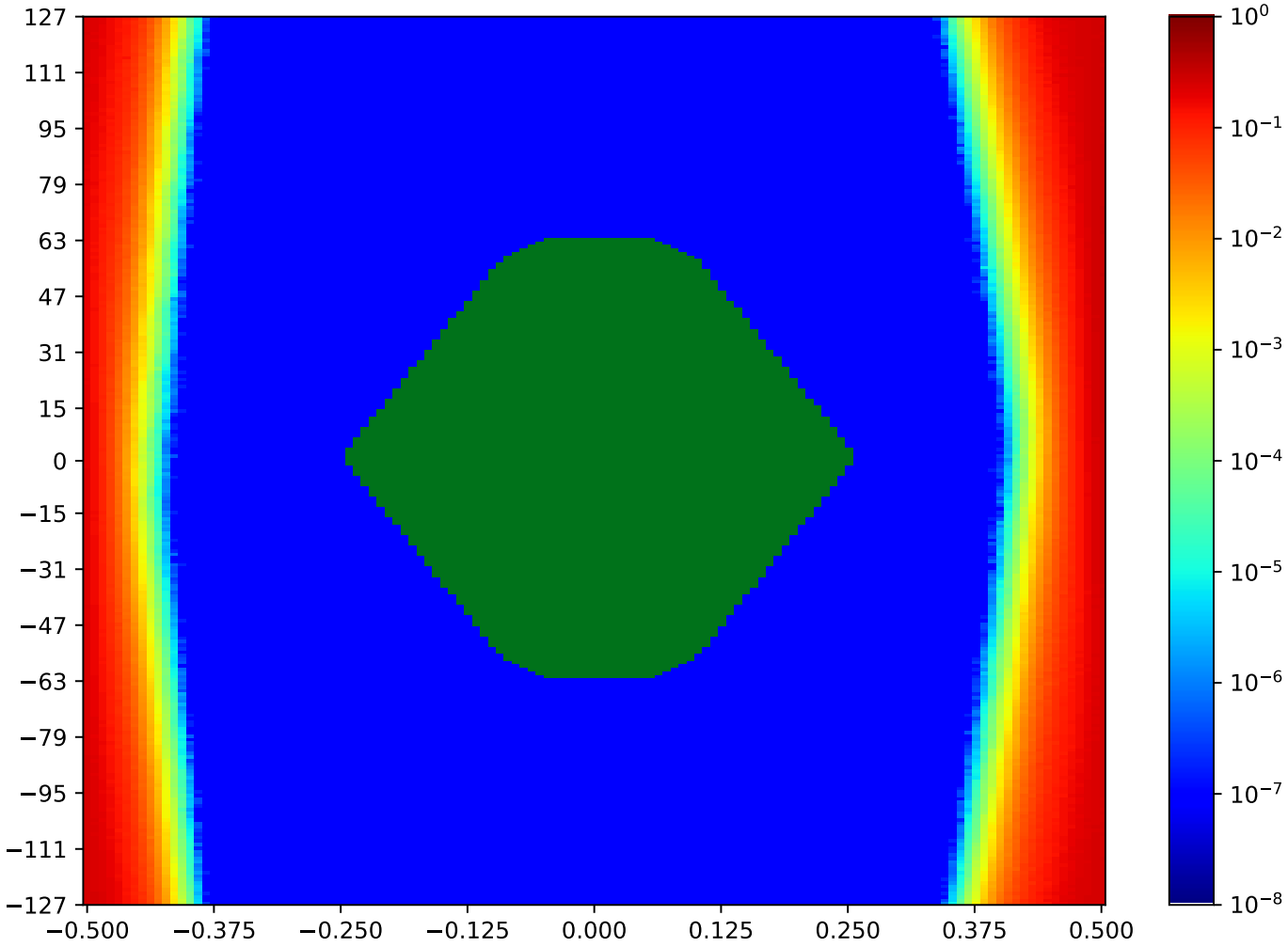


Figure 3.28: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.2 MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Table 3.26: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:17:03		2018-Sep-26 17:18:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24435	102	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

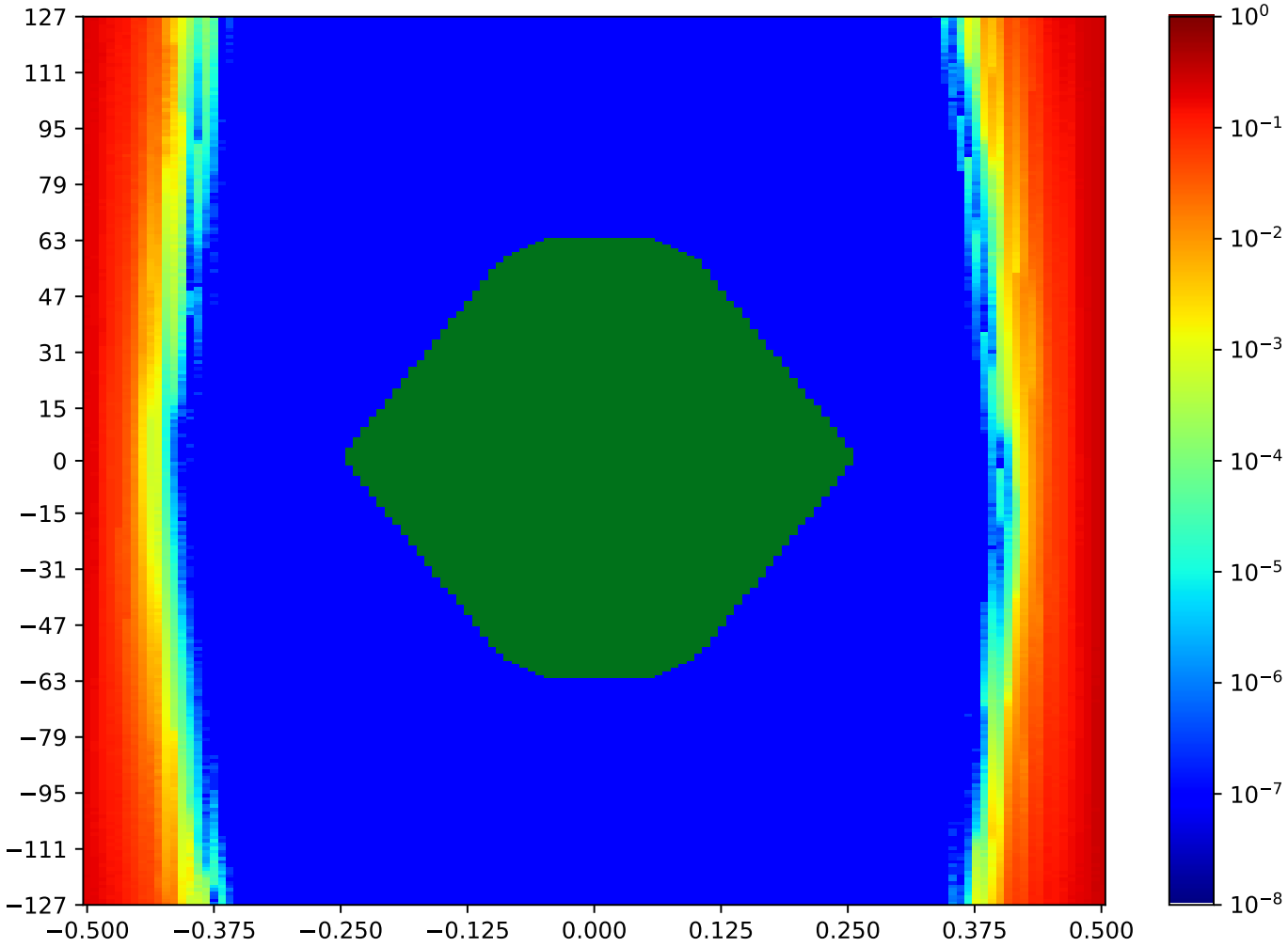


Figure 3.29: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.3 MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Table 3.27: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:18:19		2018-Sep-26 17:19:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24560	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

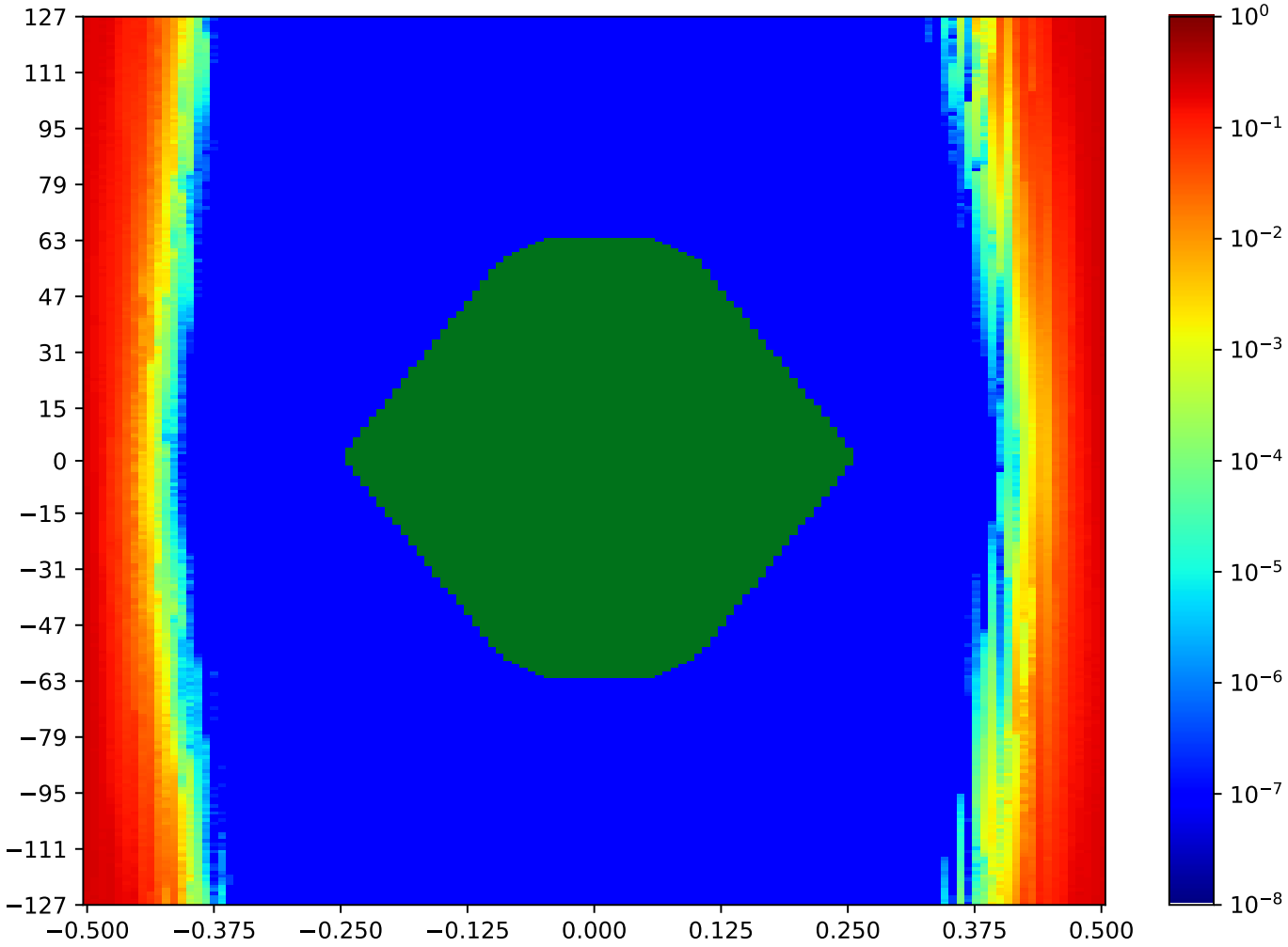


Figure 3.30: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.4 MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Table 3.28: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:11:58		2018-Sep-26 17:13:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24559	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

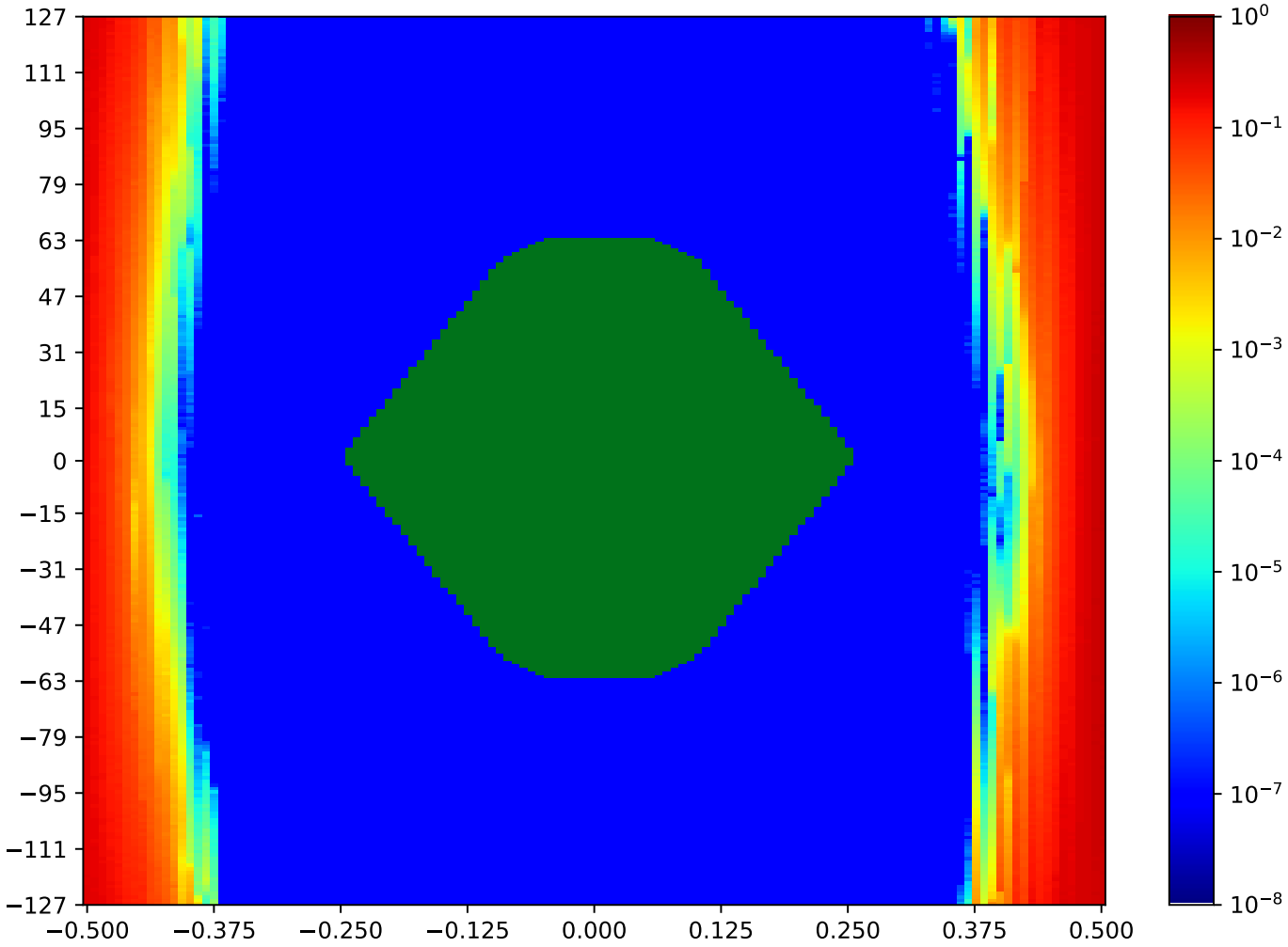


Figure 3.31: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.5 MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Table 3.29: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:22:04		2018-Sep-26 17:23:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24910	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

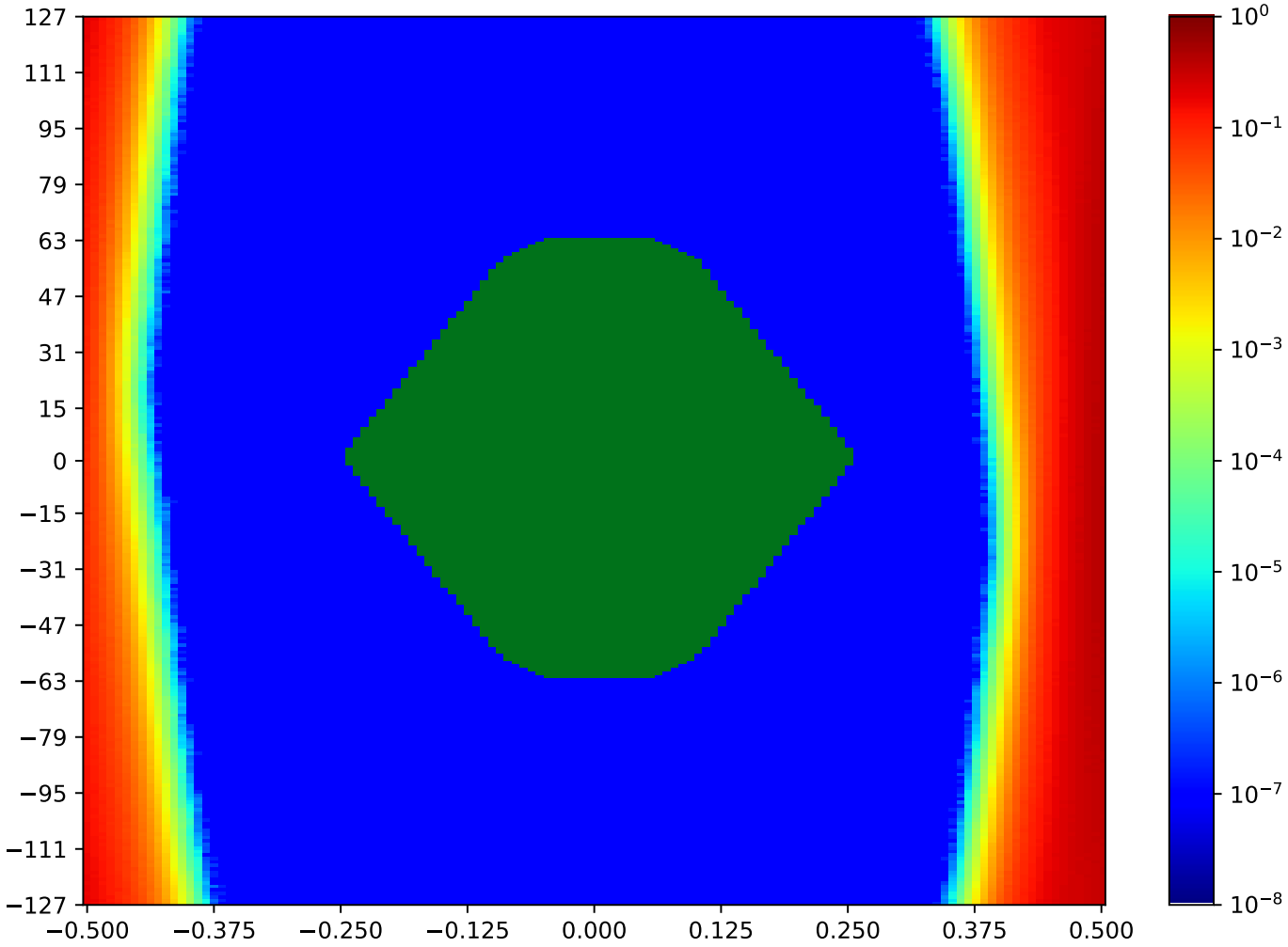


Figure 3.32: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.6 MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Table 3.30: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:10:42		2018-Sep-26 17:11:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24910	104	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

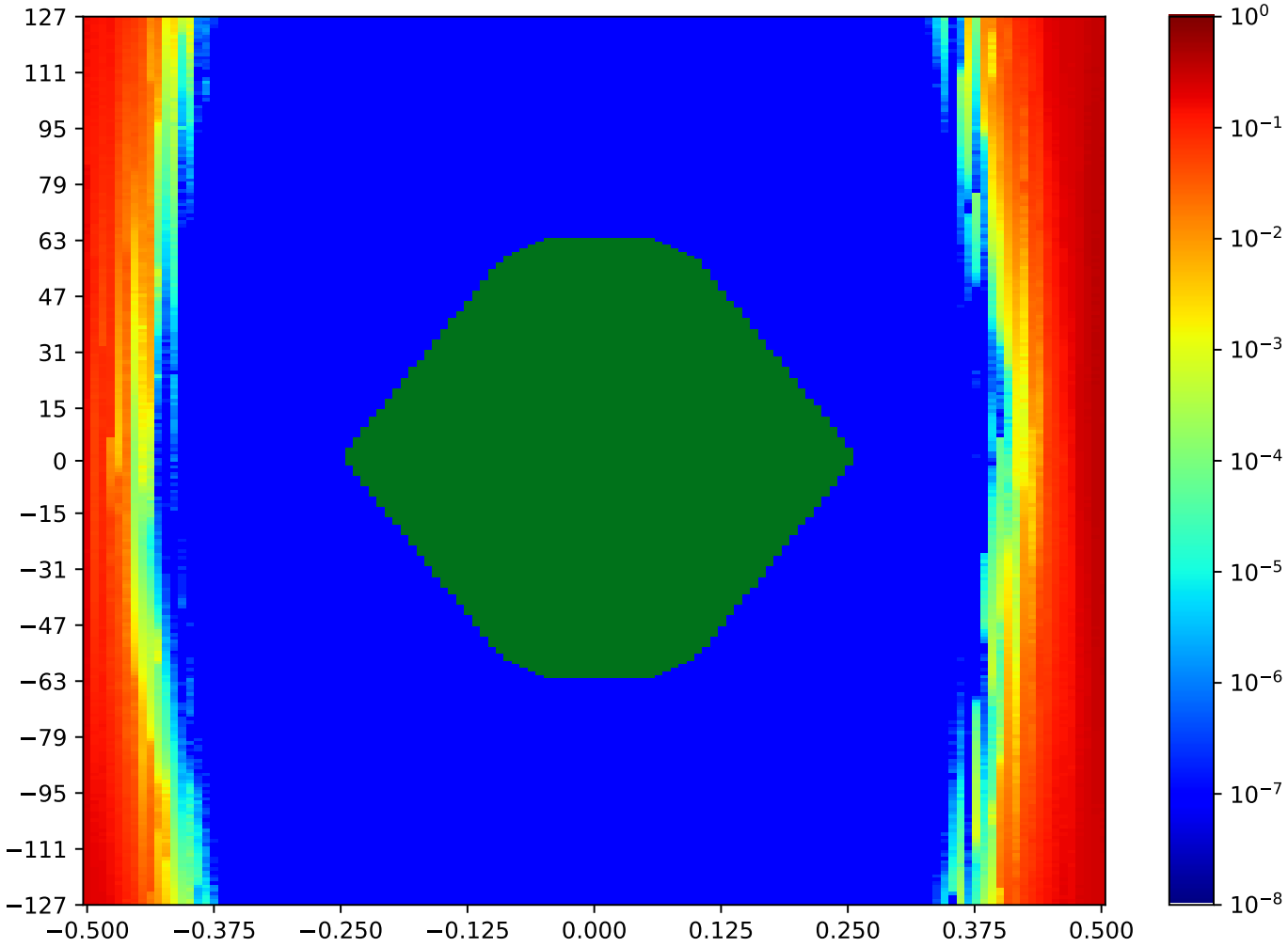


Figure 3.33: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.7 MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Table 3.31: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:24:35		2018-Sep-26 17:25:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24588	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

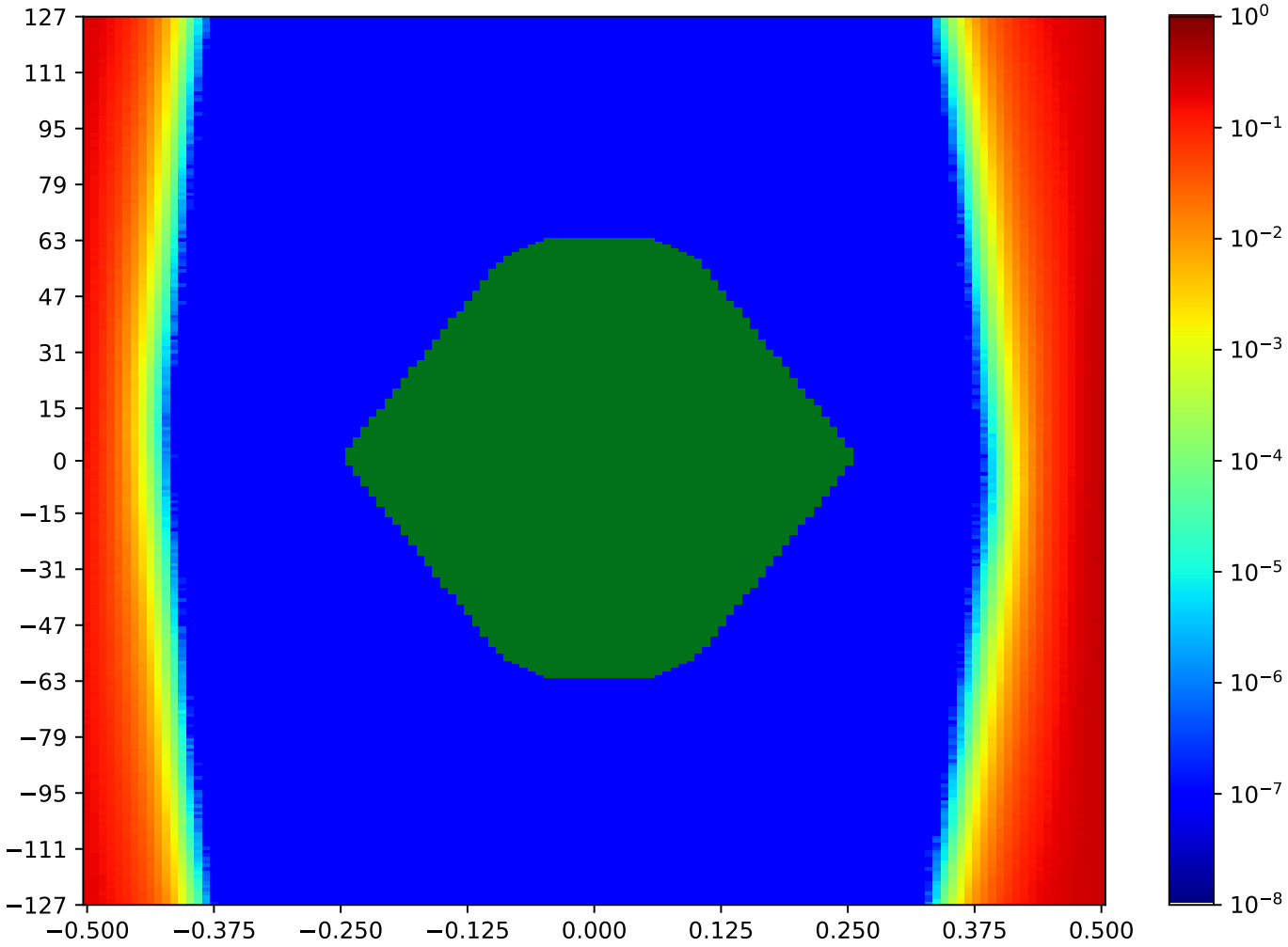


Figure 3.34: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.8 MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Table 3.32: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:13:14		2018-Sep-26 17:14:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25525	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

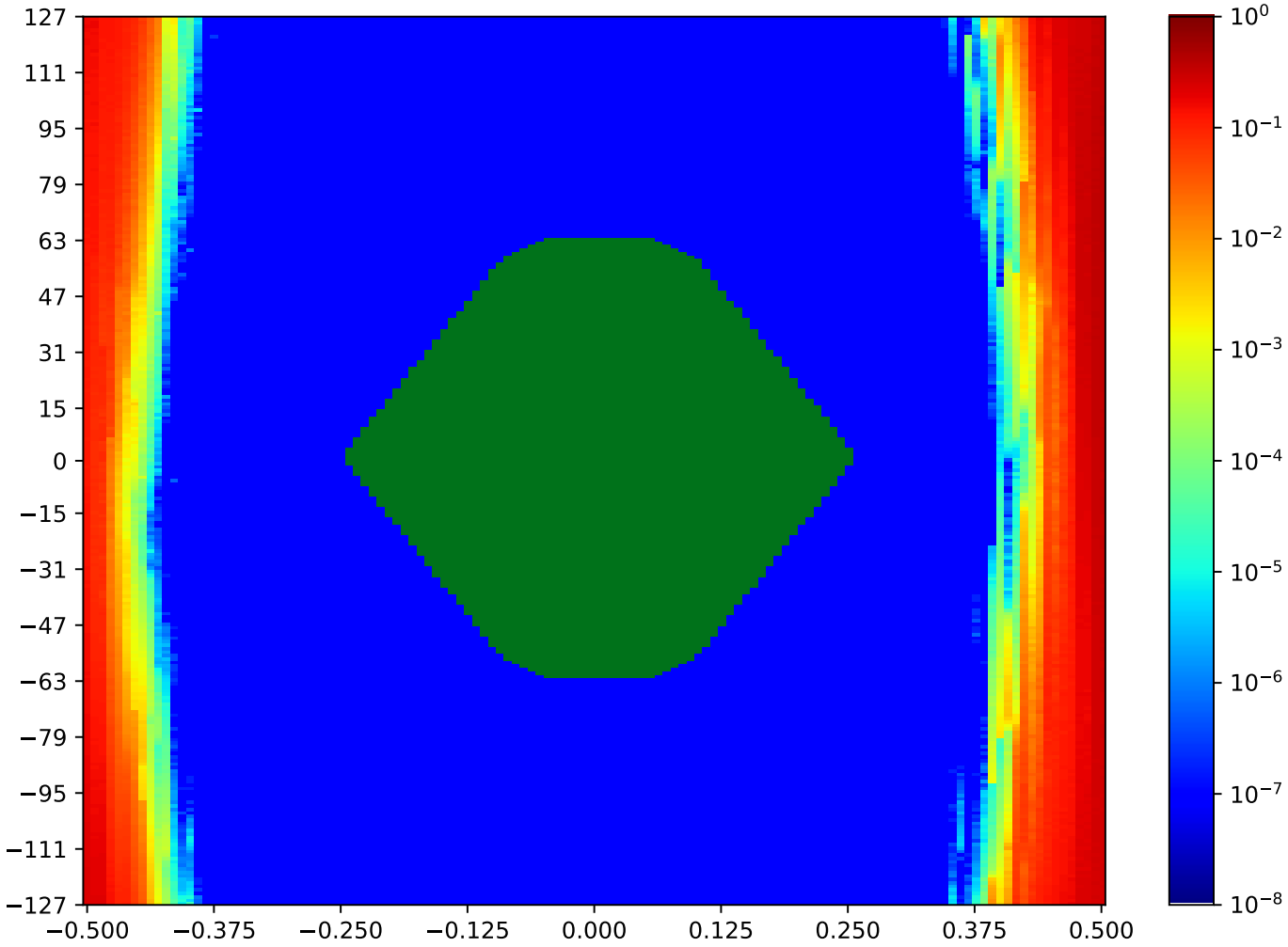


Figure 3.35: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.9 MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Table 3.33: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:23:19		2018-Sep-26 17:24:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25074	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

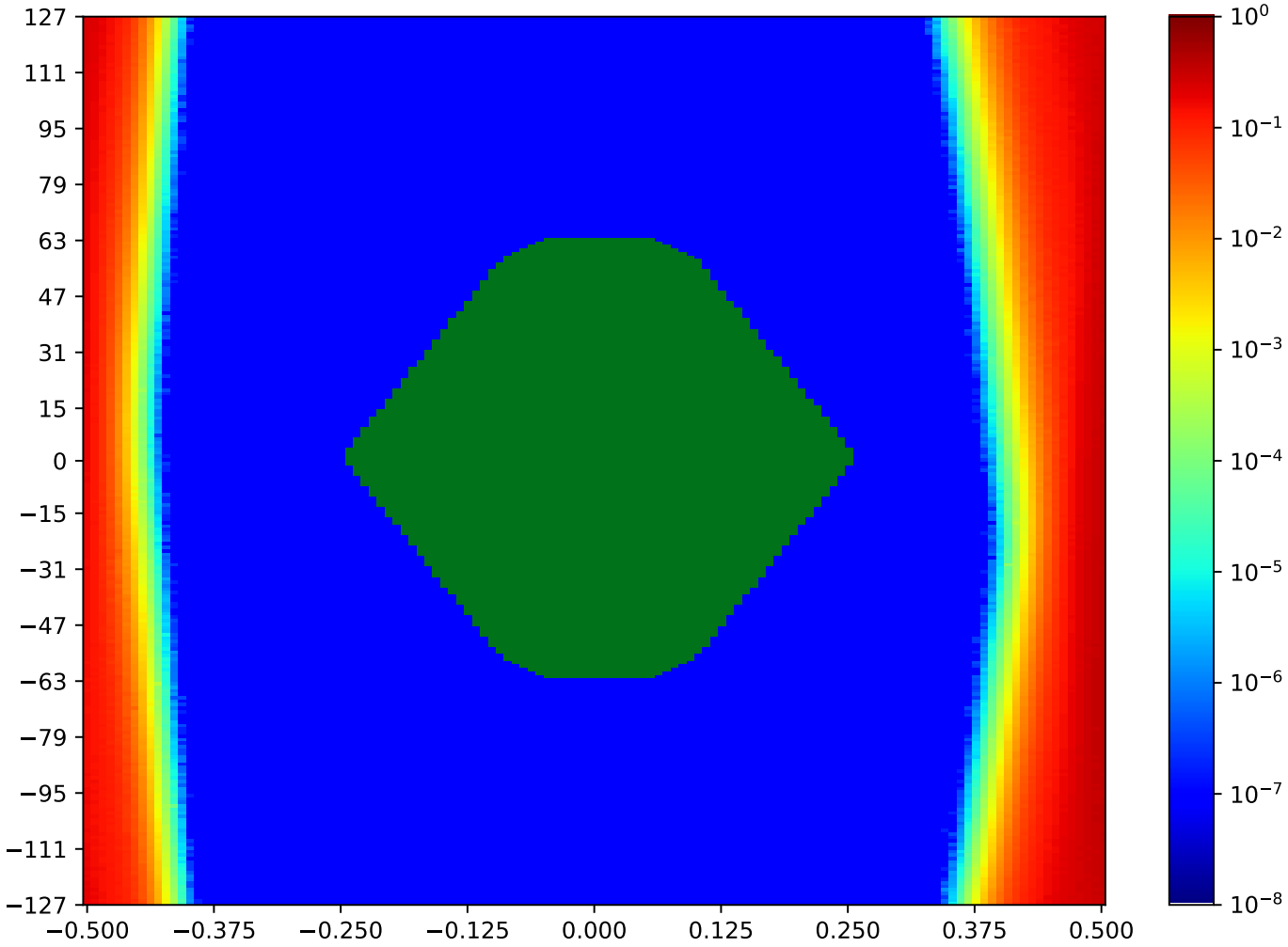


Figure 3.36: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.10 MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Table 3.34: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:15:47		2018-Sep-26 17:17:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24341	101	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

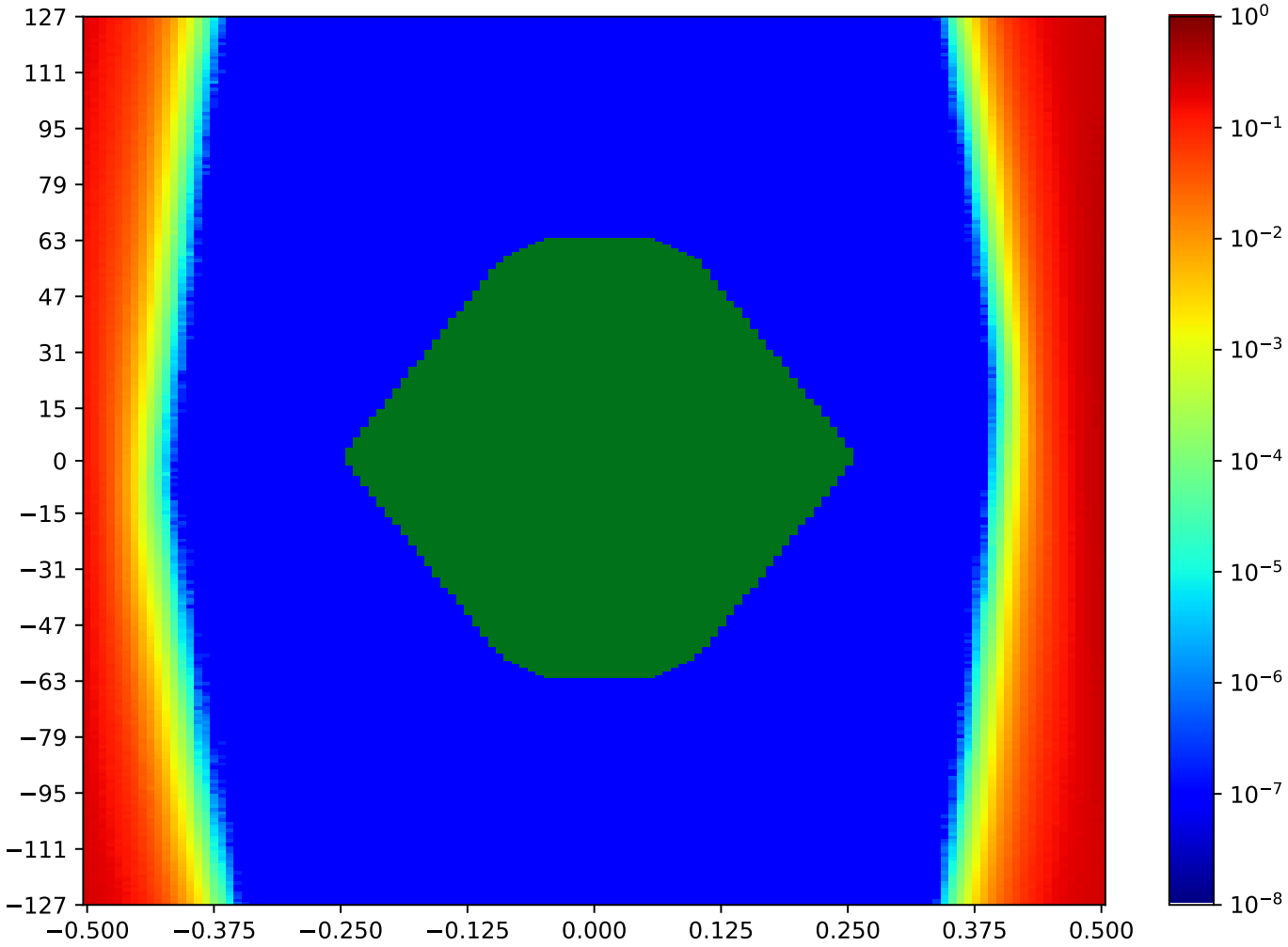


Figure 3.37: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.11 MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Table 3.35: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:20:50		2018-Sep-26 17:22:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24235	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

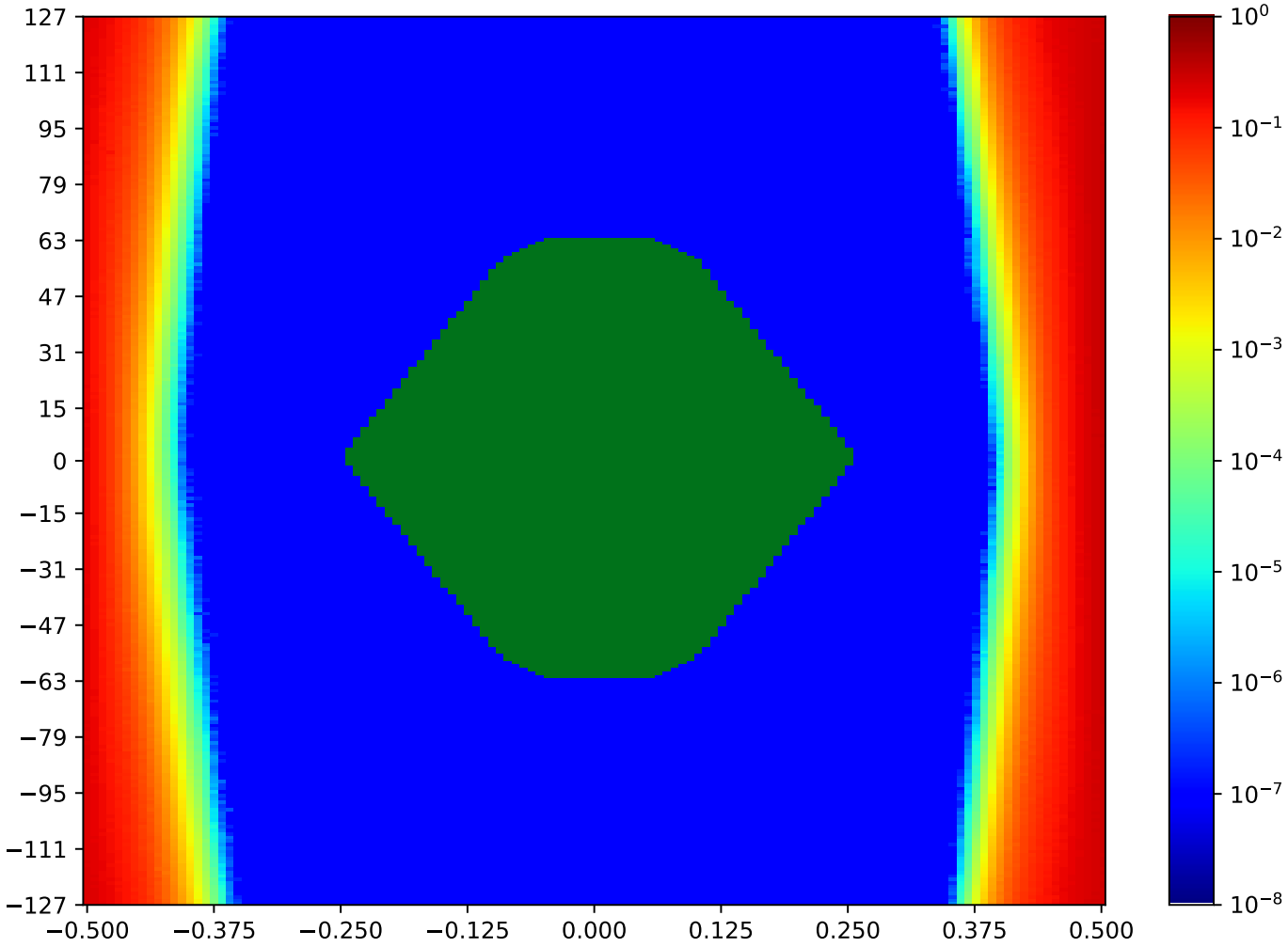


Figure 3.38: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.3.12 MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Table 3.36: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:19:35		2018-Sep-26 17:20:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24756	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

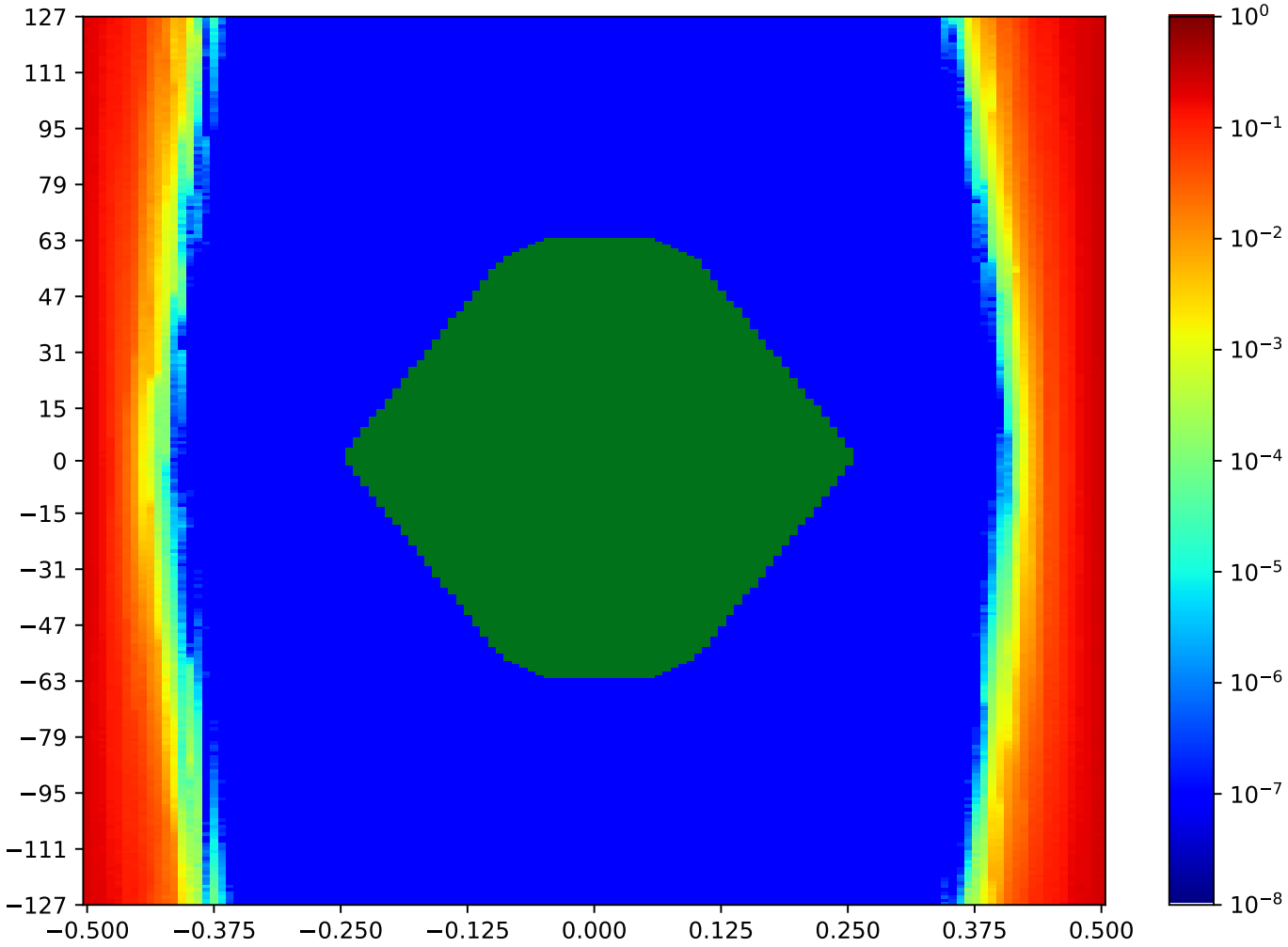


Figure 3.39: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4 MSP_C TX4 MSP_A RX7 Minipod Loopback

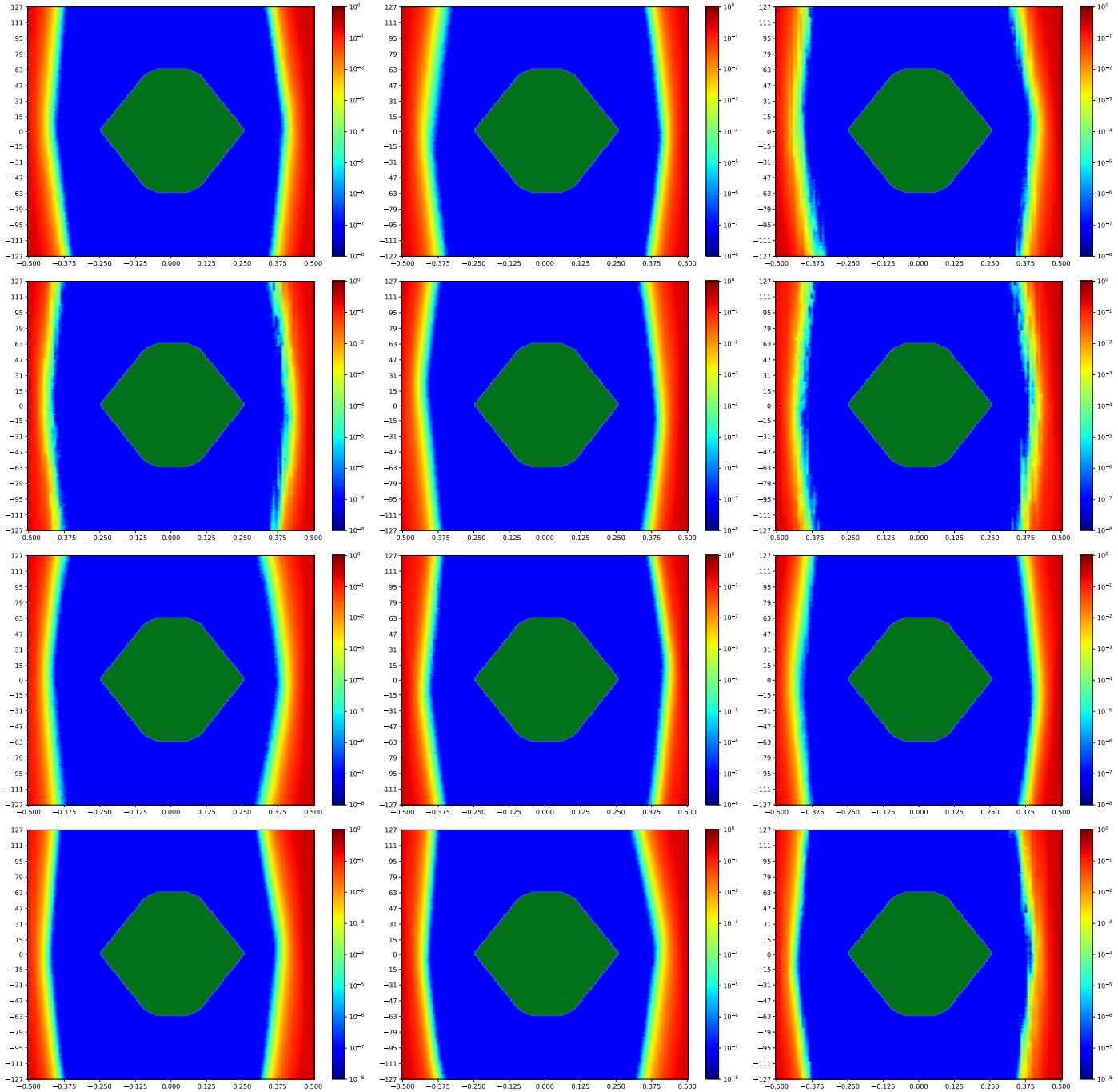


Figure 3.40: MSP_C TX4 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.53.

3.4.1 MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Table 3.37: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:29:35		2018-Sep-26 17:30:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23933	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

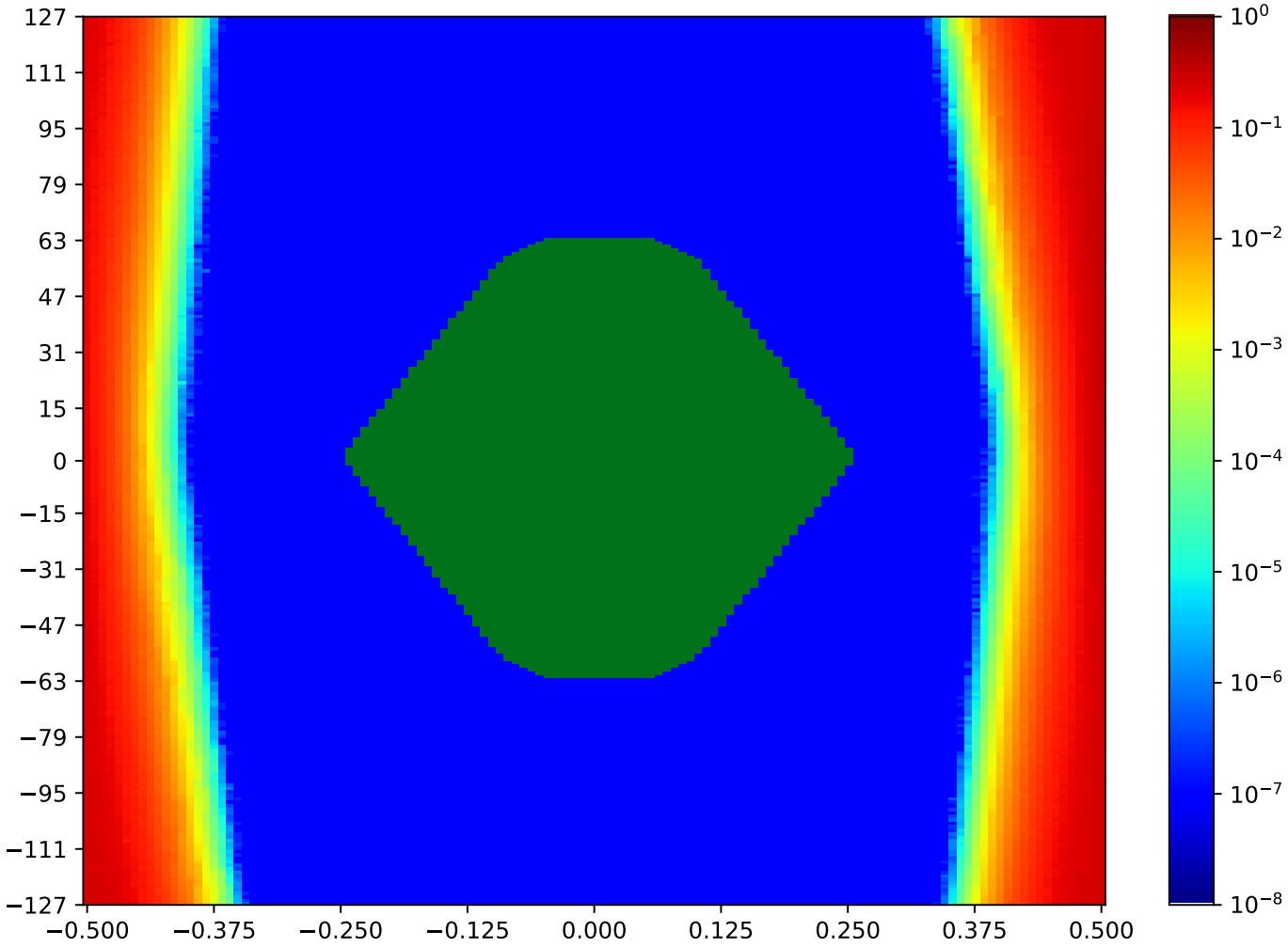


Figure 3.41: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.2 MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Table 3.38: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:27:05		2018-Sep-26 17:28:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23686	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

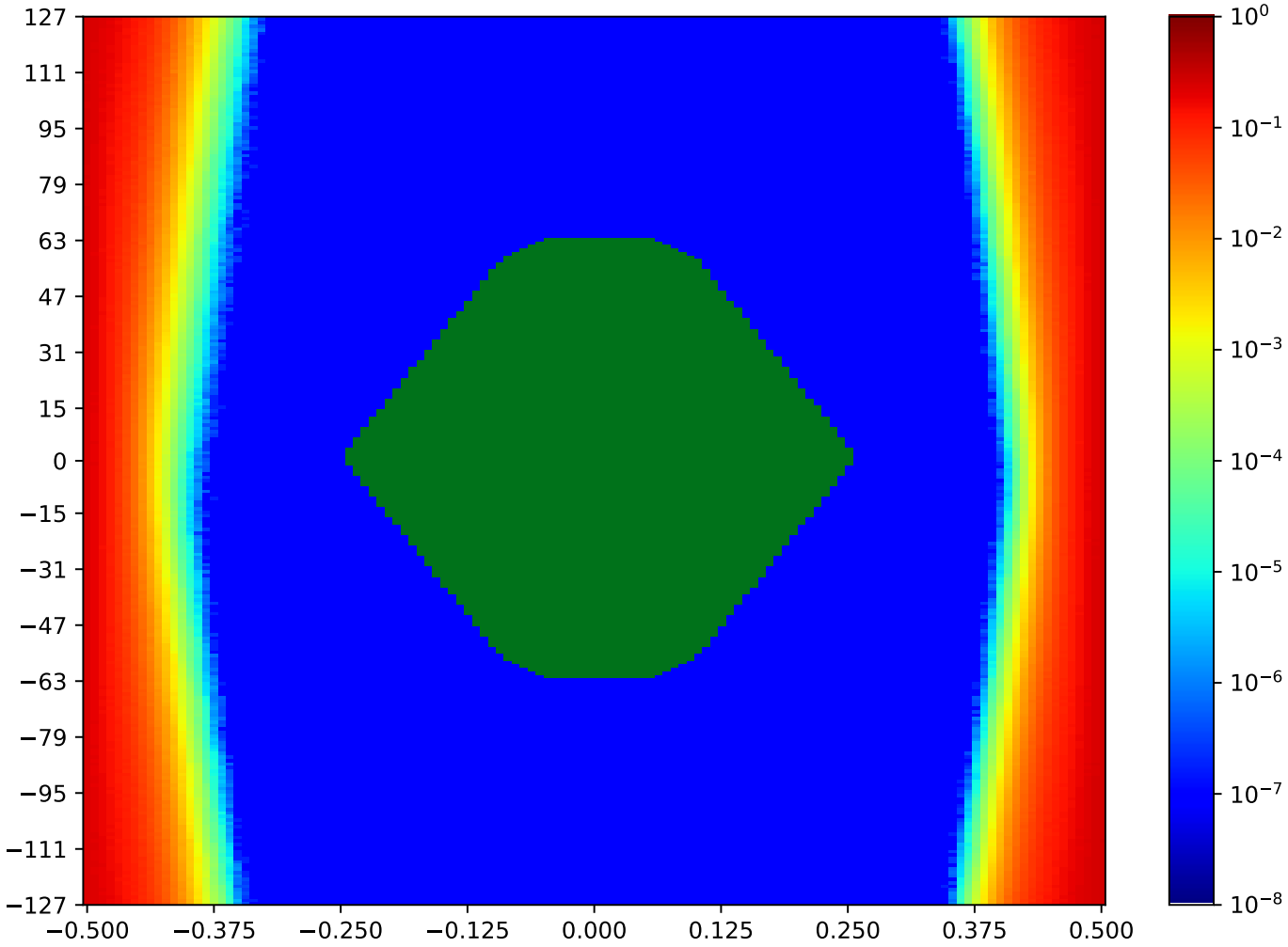


Figure 3.42: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.3 MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Table 3.39: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:33:21		2018-Sep-26 17:34:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23610	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

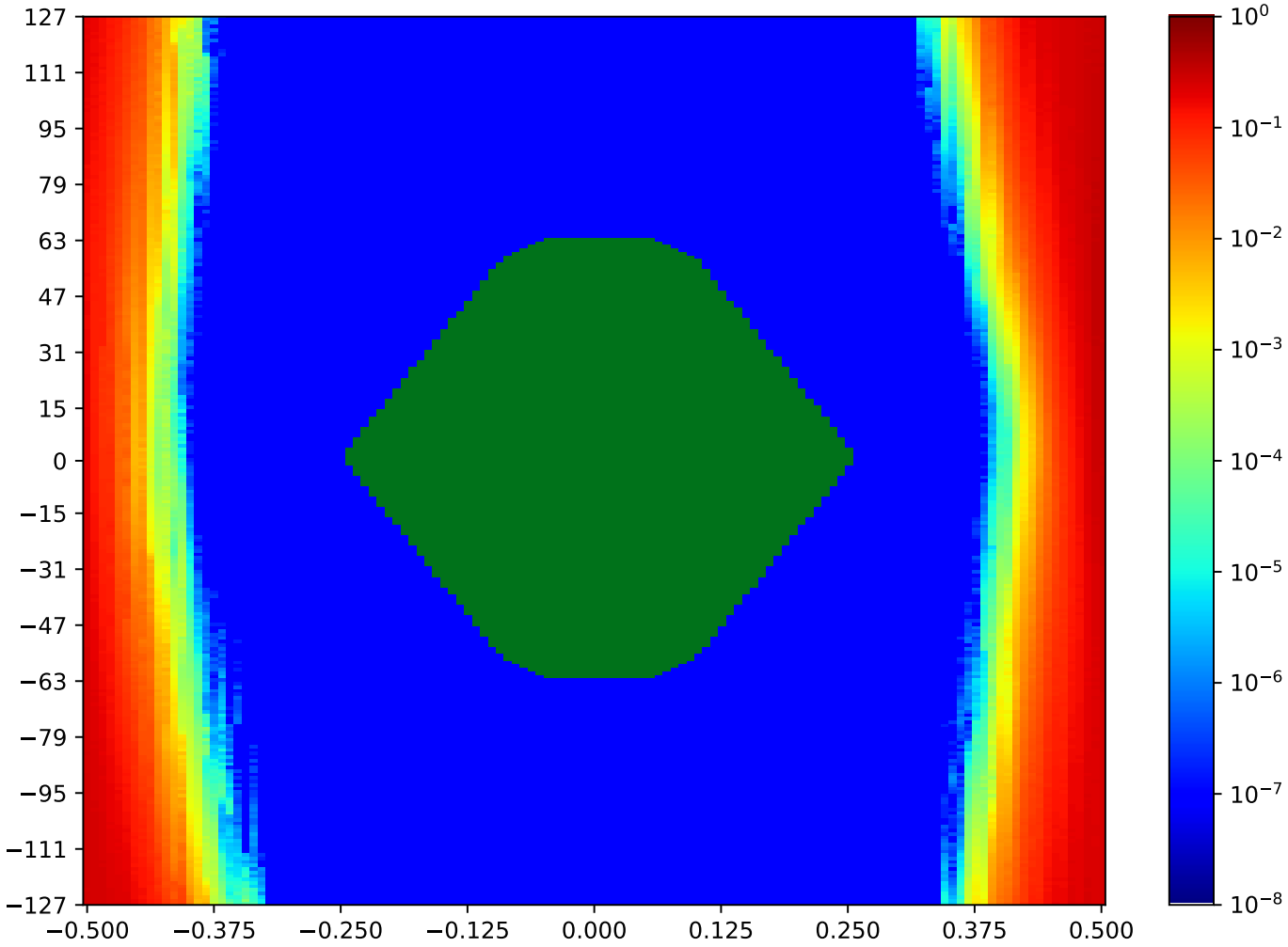


Figure 3.43: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.4 MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Table 3.40: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:25:50		2018-Sep-26 17:27:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24552	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

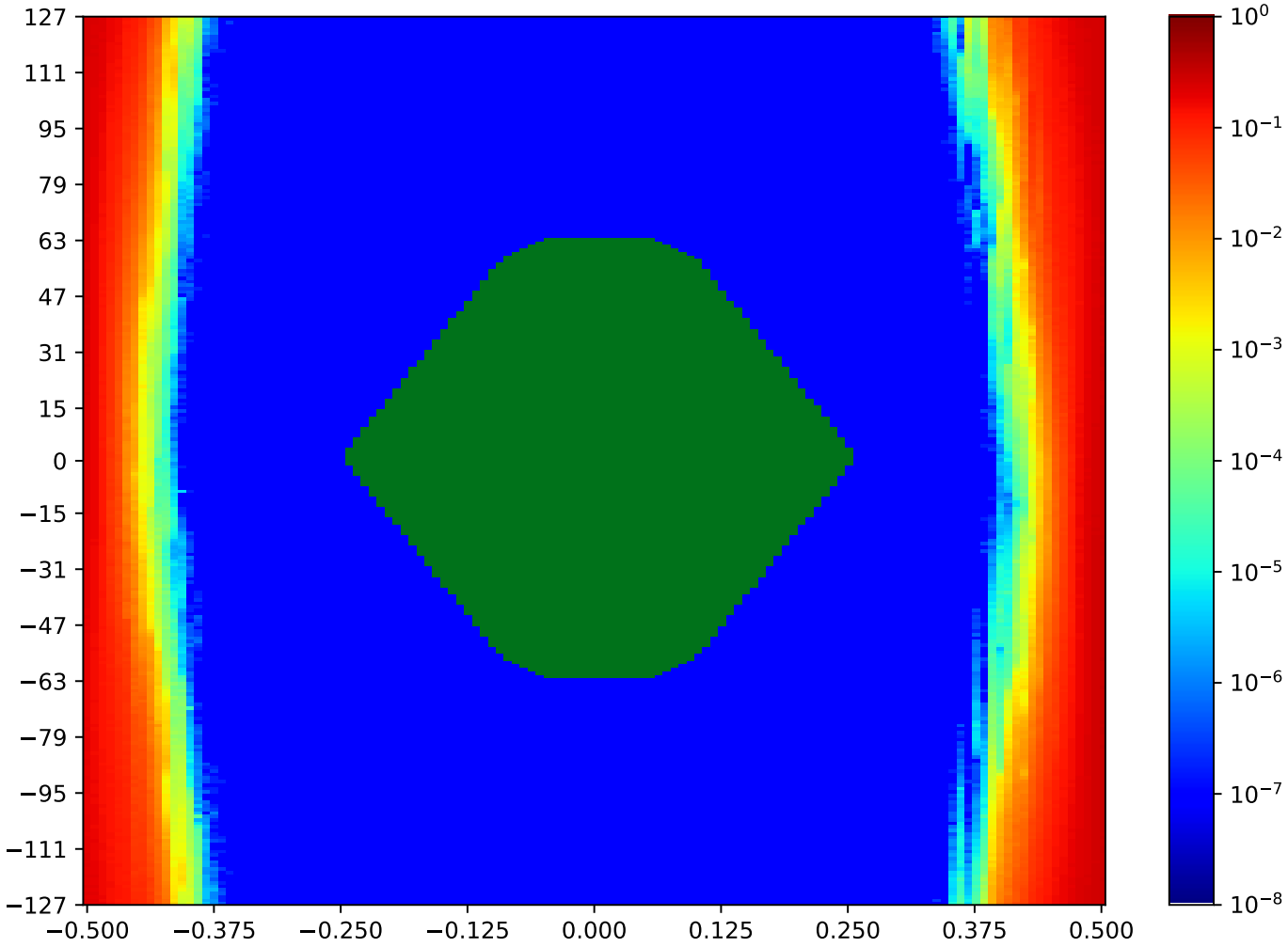


Figure 3.44: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.5 MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Table 3.41: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:37:06		2018-Sep-26 17:38:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24029	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

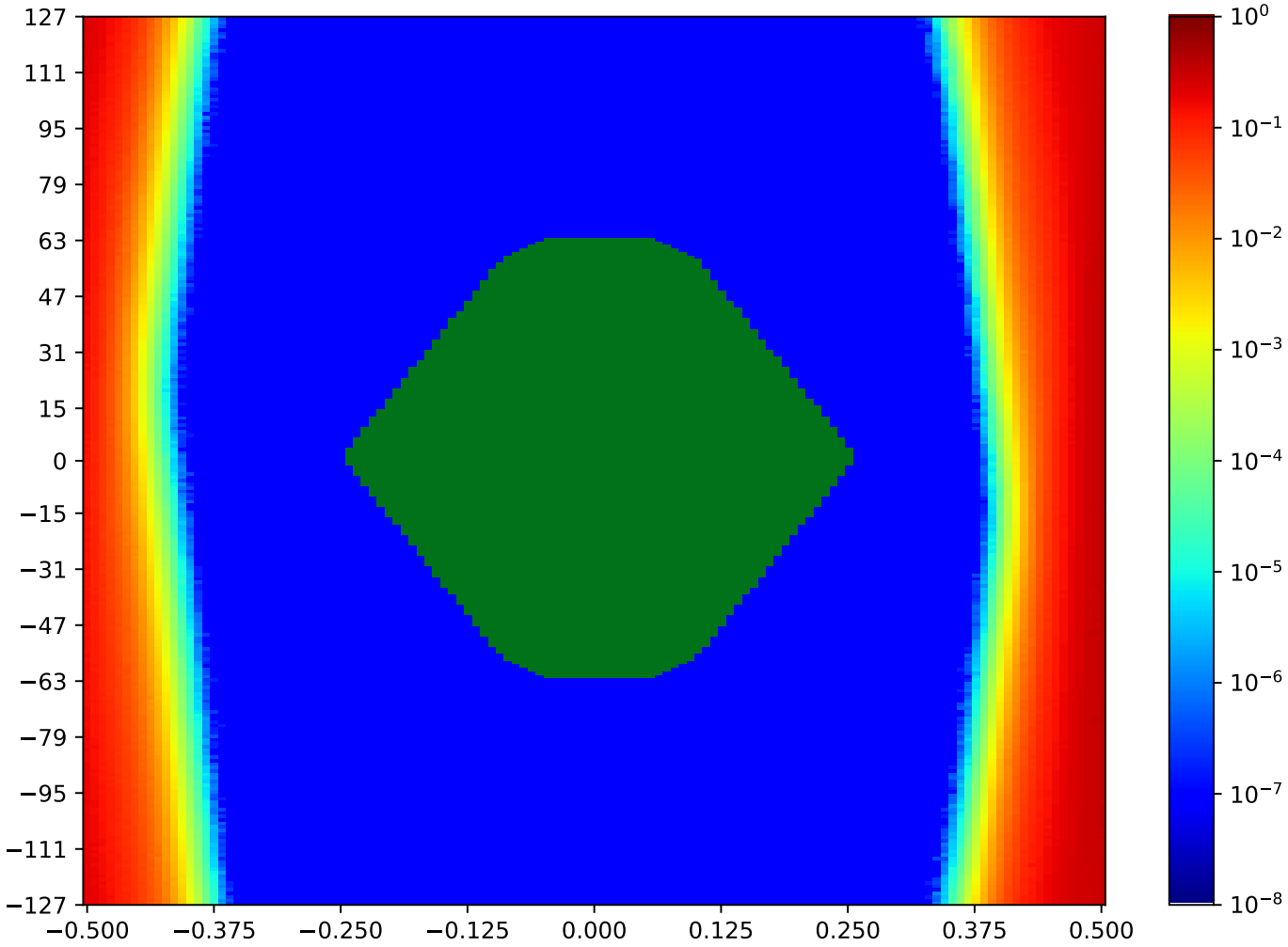


Figure 3.45: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.6 MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Table 3.42: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:28:20		2018-Sep-26 17:29:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23714	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

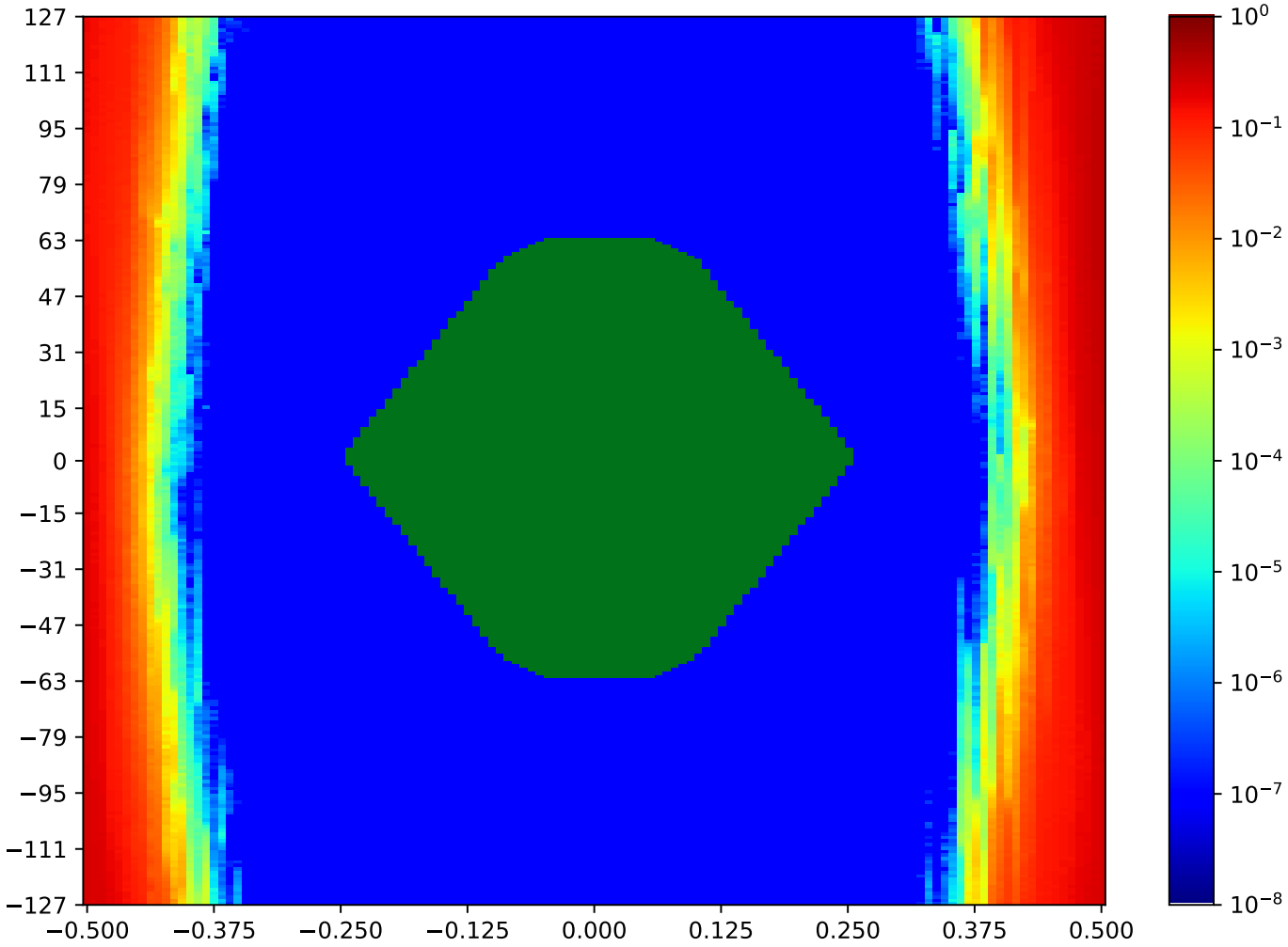


Figure 3.46: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.7 MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Table 3.43: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:39:35		2018-Sep-26 17:40:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23313	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

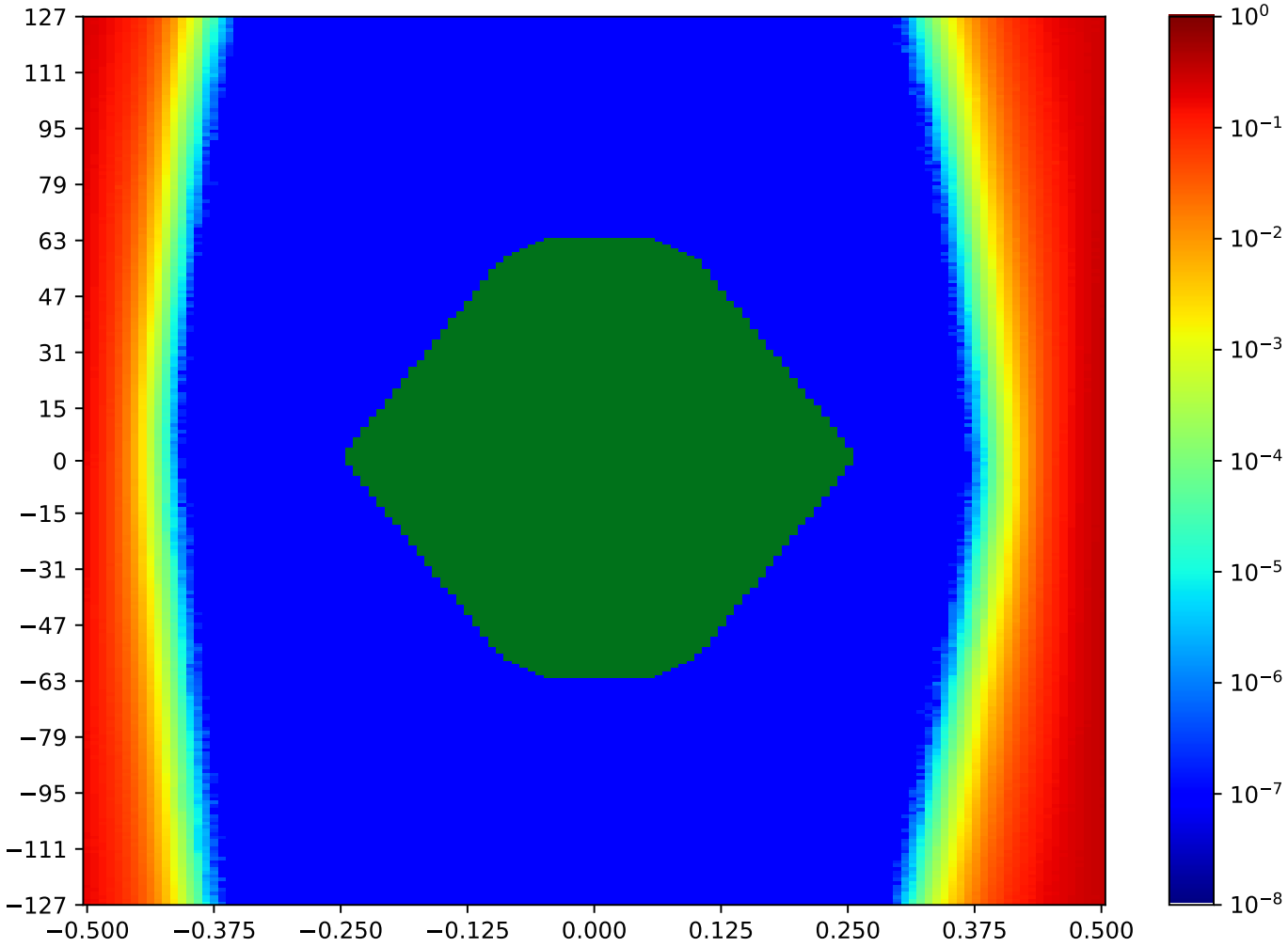


Figure 3.47: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.8 MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Table 3.44: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:30:50		2018-Sep-26 17:32:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24507	102	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

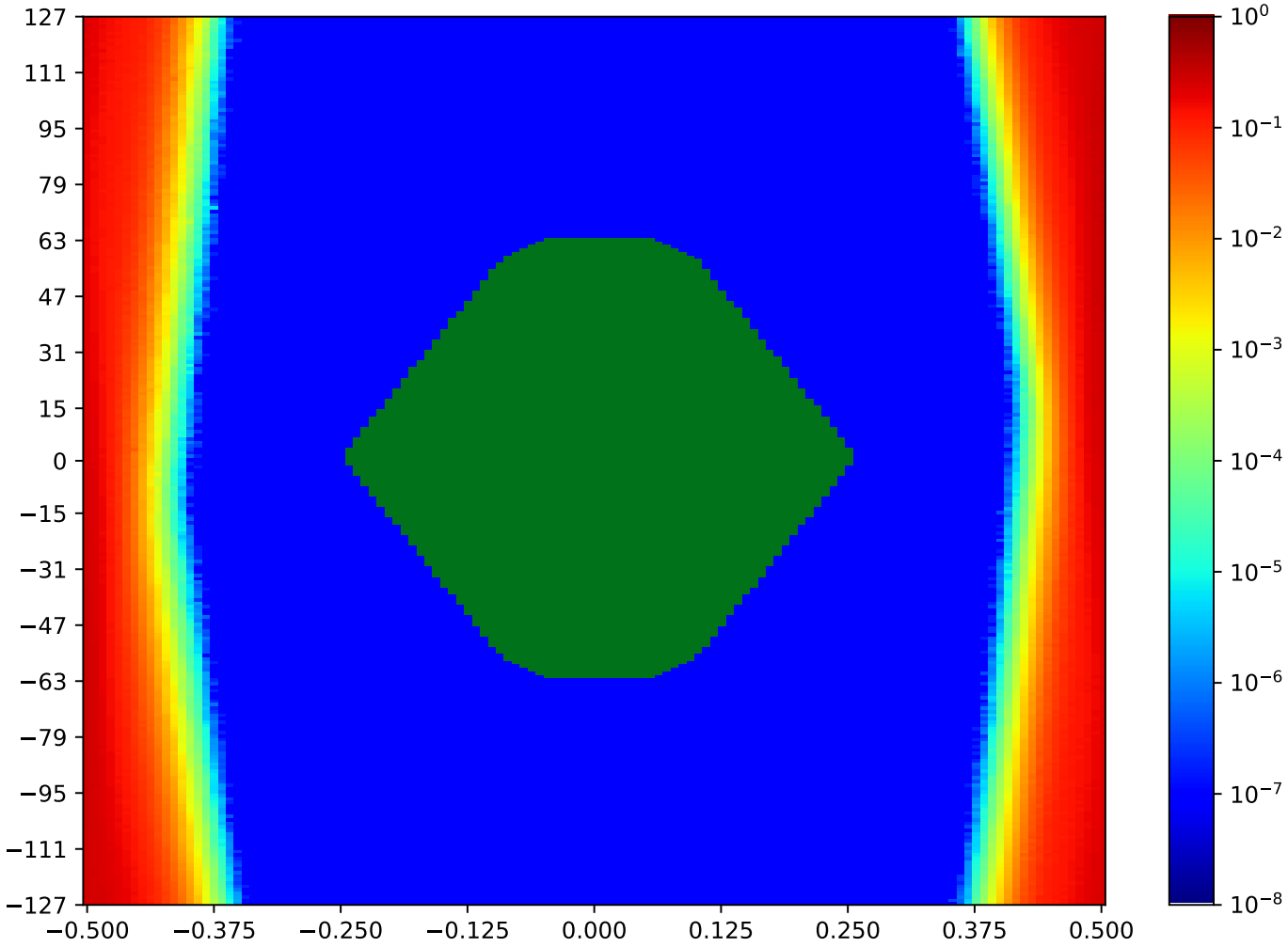


Figure 3.48: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.9 MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Table 3.45: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:38:20		2018-Sep-26 17:39:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24391	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

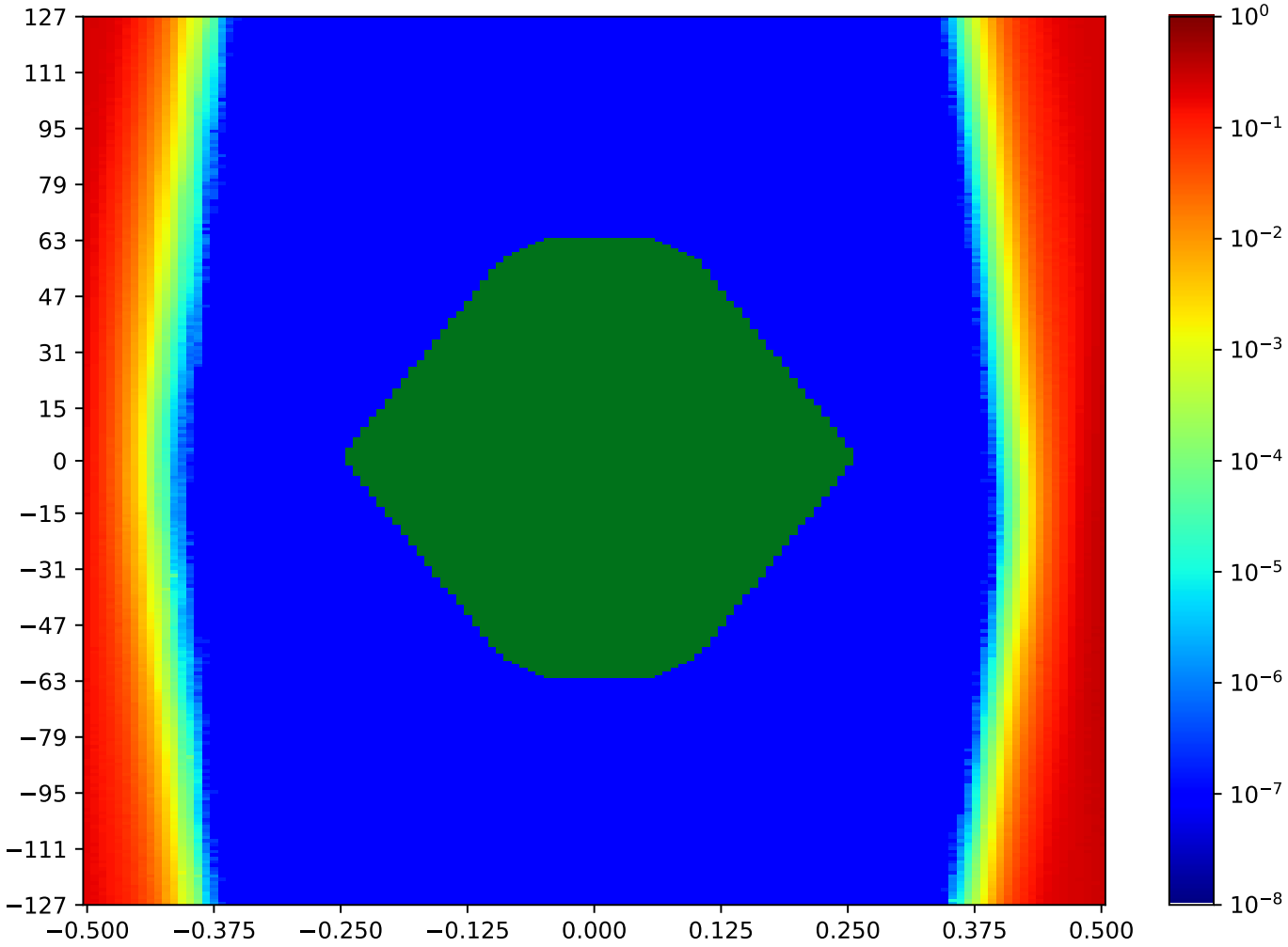


Figure 3.49: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.10 MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Table 3.46: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:32:05		2018-Sep-26 17:33:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23734	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

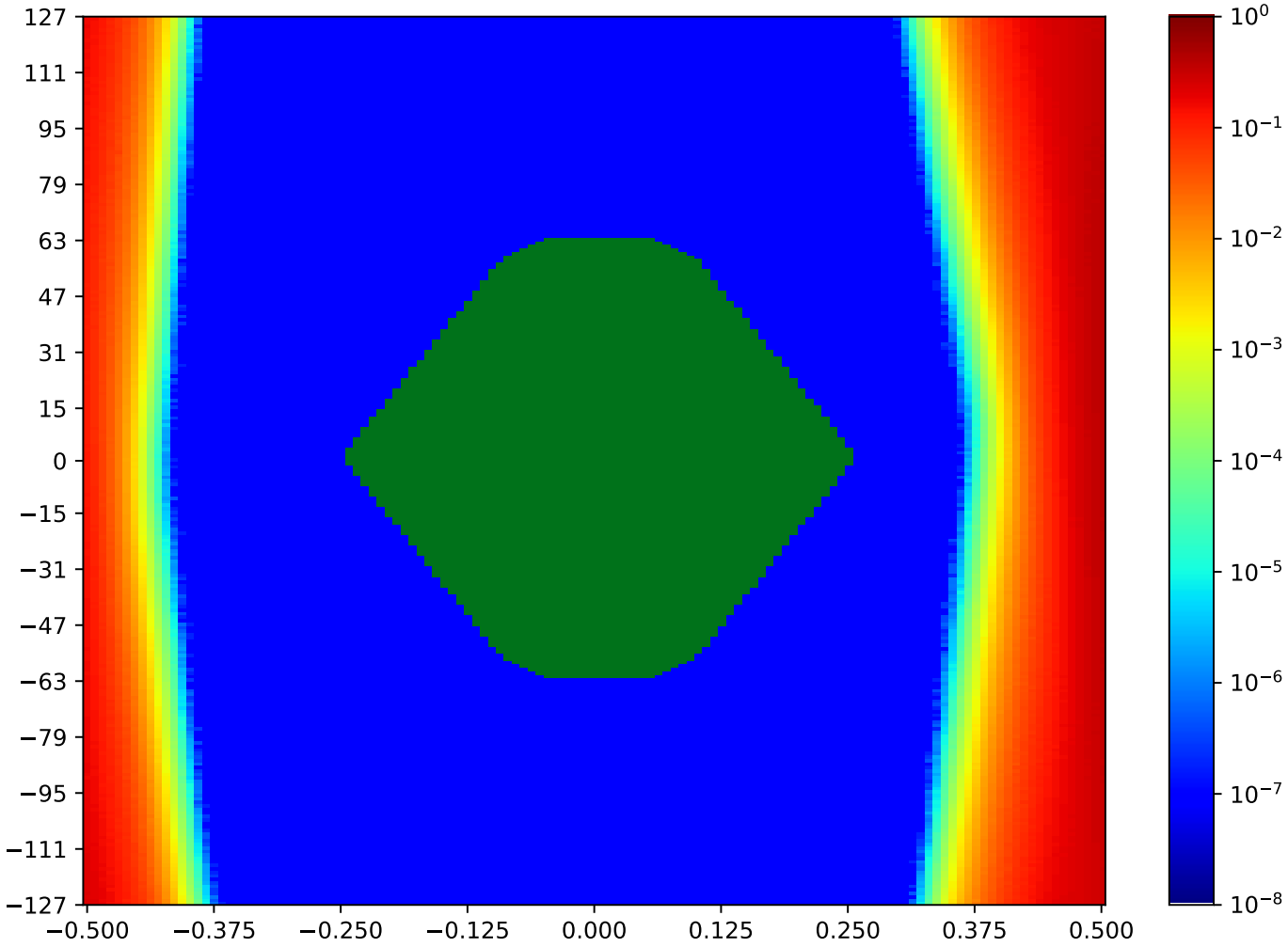


Figure 3.50: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.11 MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Table 3.47: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:35:51		2018-Sep-26 17:37:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23627	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

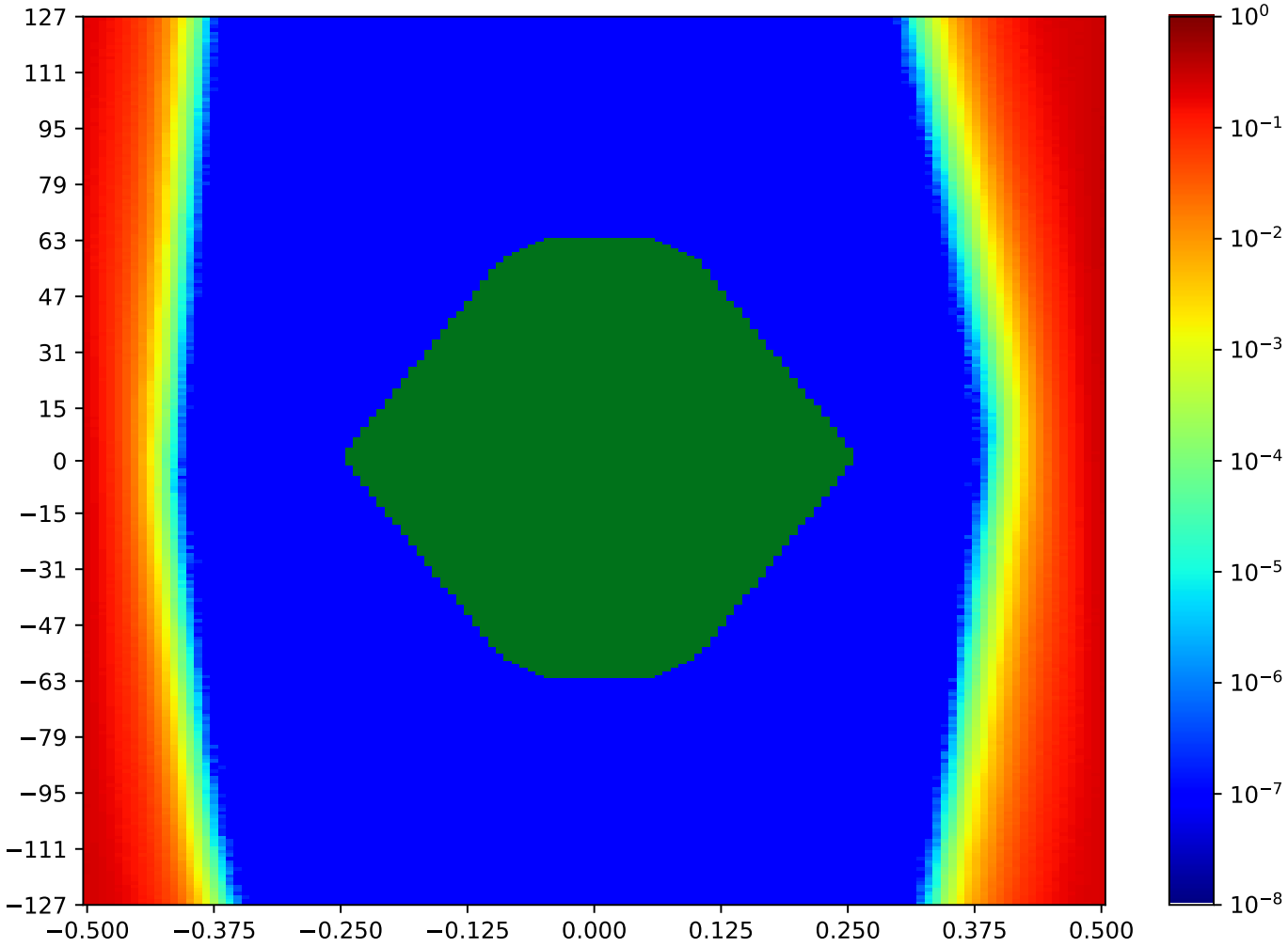


Figure 3.51: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.4.12 MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Table 3.48: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:34:36		2018-Sep-26 17:35:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24622	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

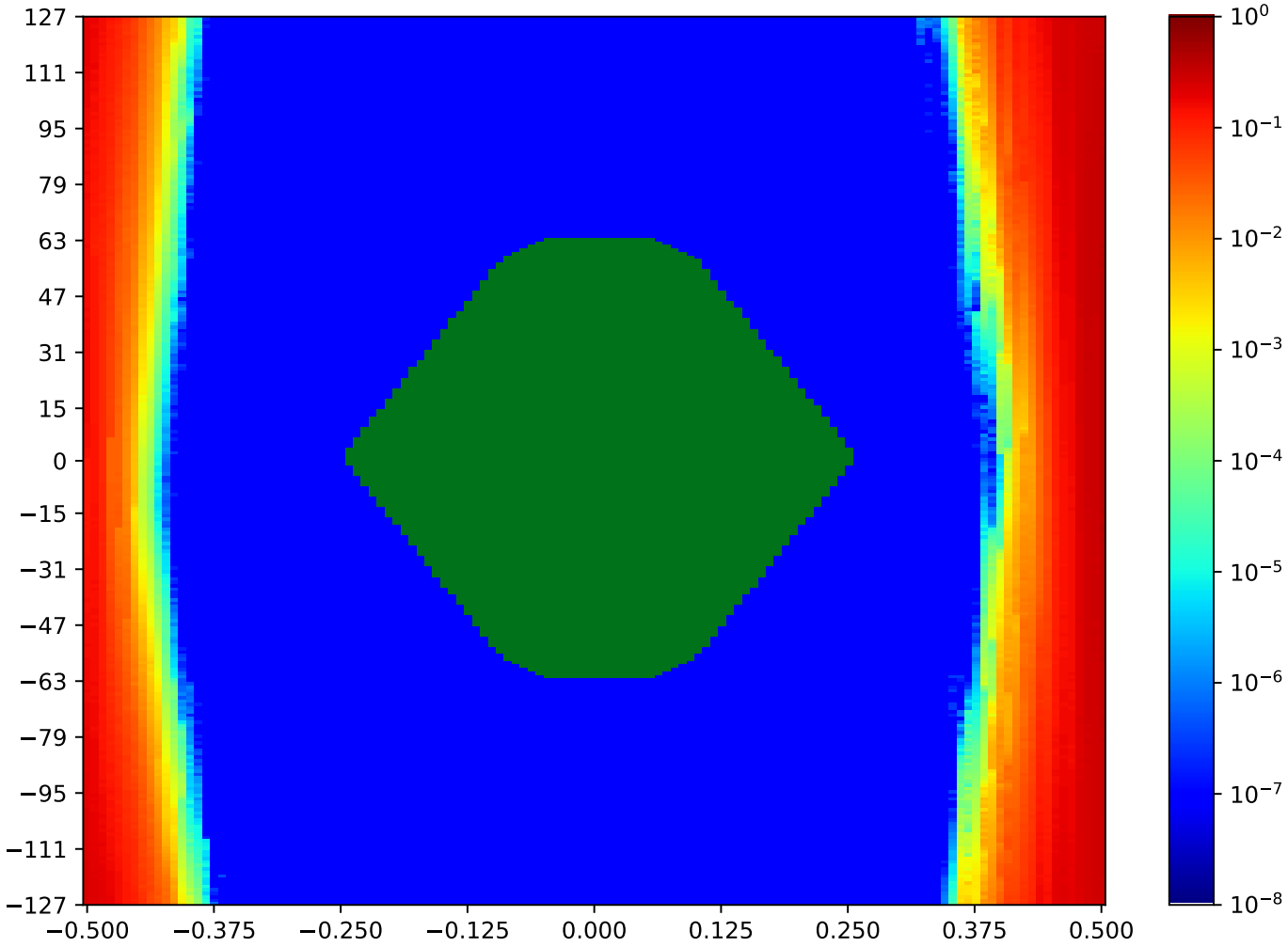


Figure 3.52: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.62.

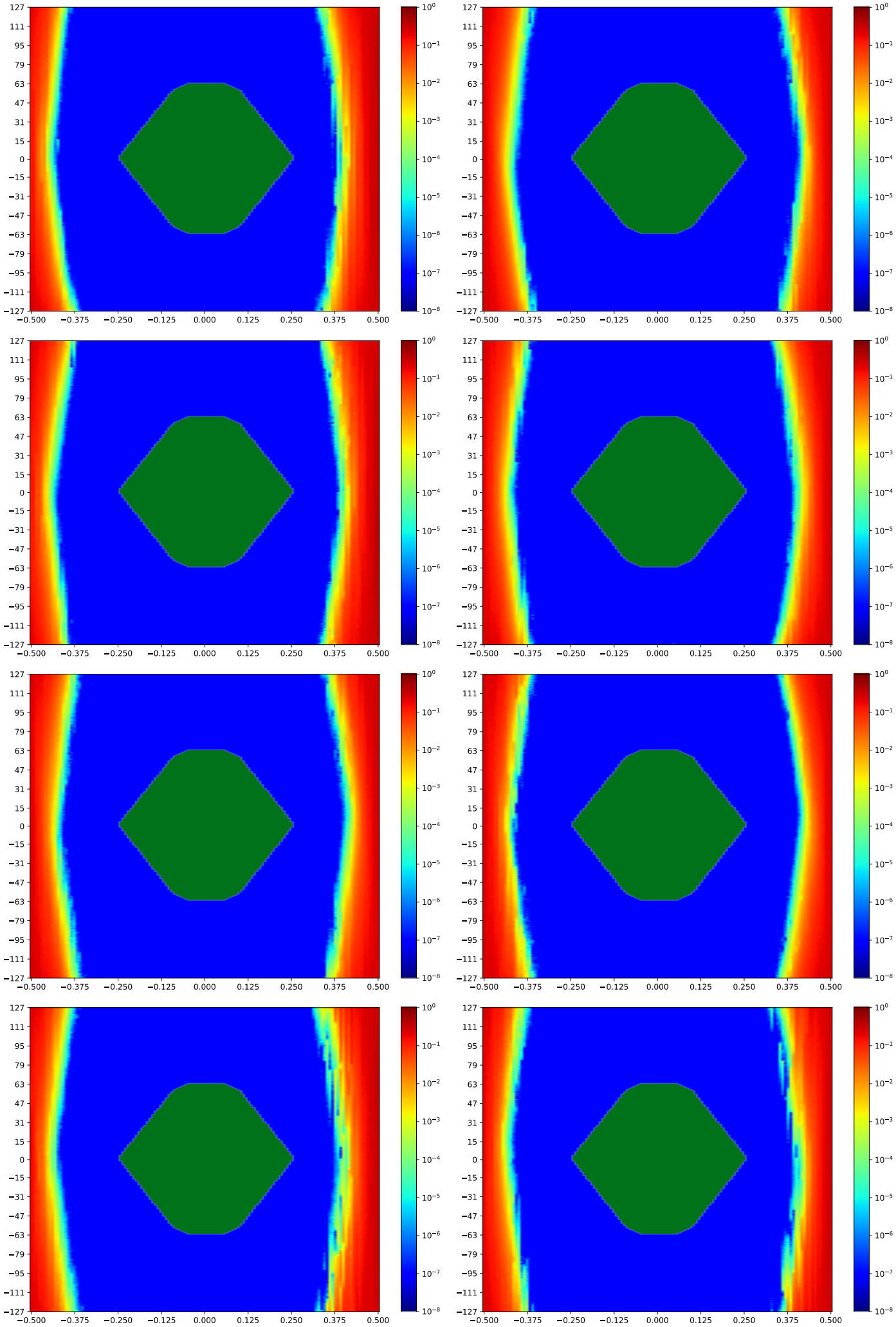


Figure 3.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

3.5.1 TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Table 3.49: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:44:34		2018-Sep-26 17:45:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24485	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

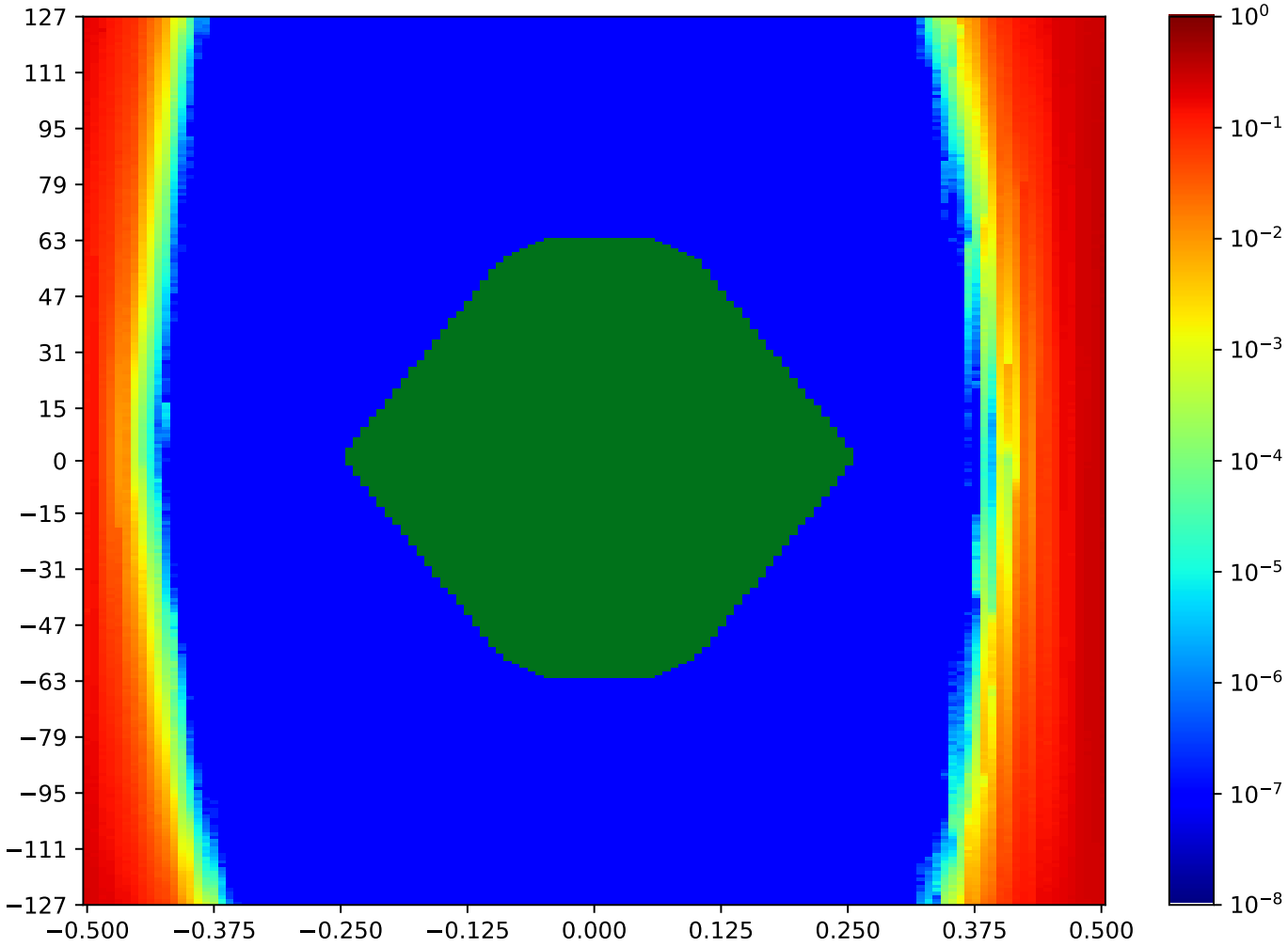


Figure 3.54: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.2 TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Table 3.50: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:42:05		2018-Sep-26 17:43:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24335	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

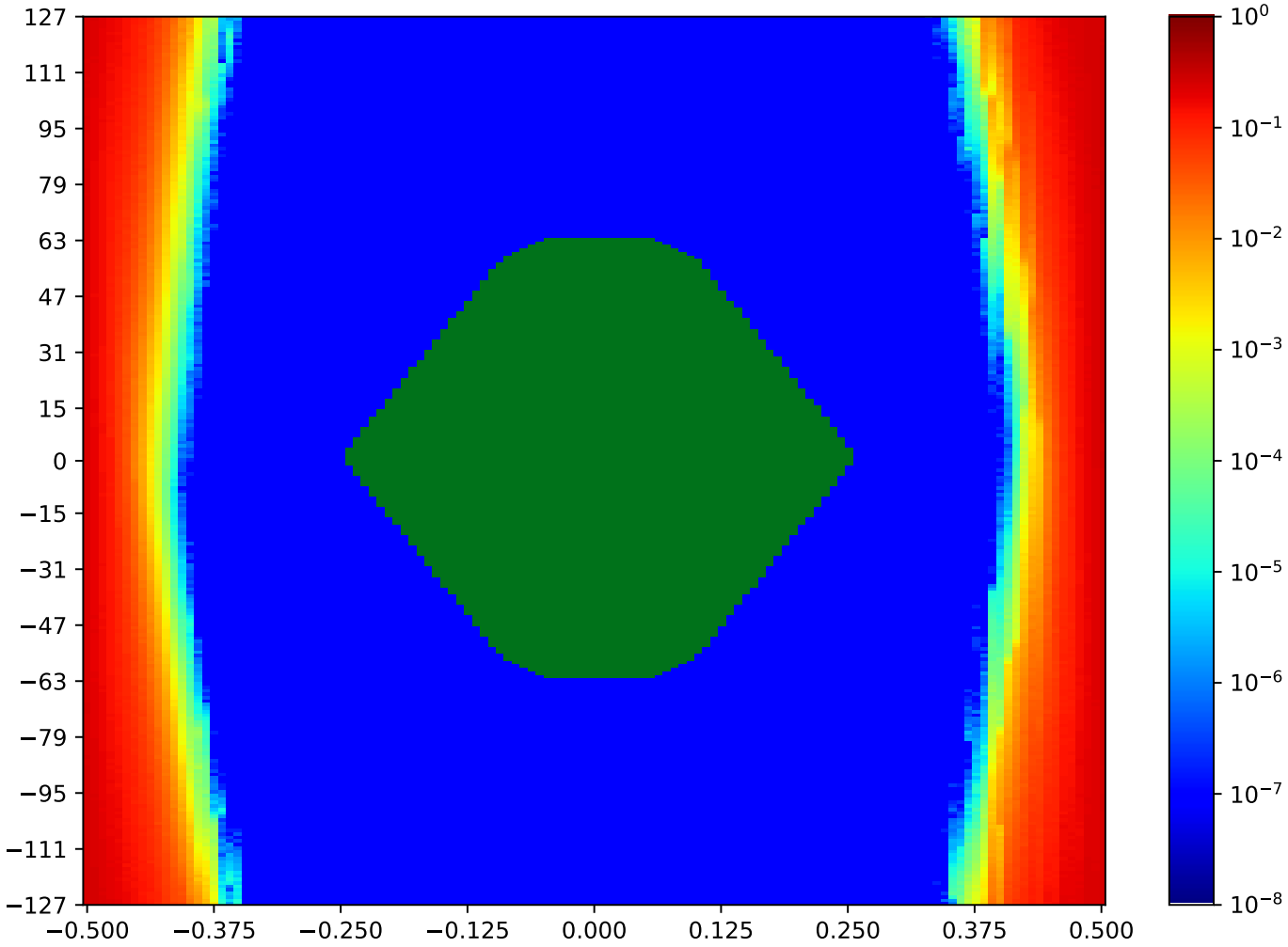


Figure 3.55: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.3 TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Table 3.51: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:47:03		2018-Sep-26 17:48:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24509	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

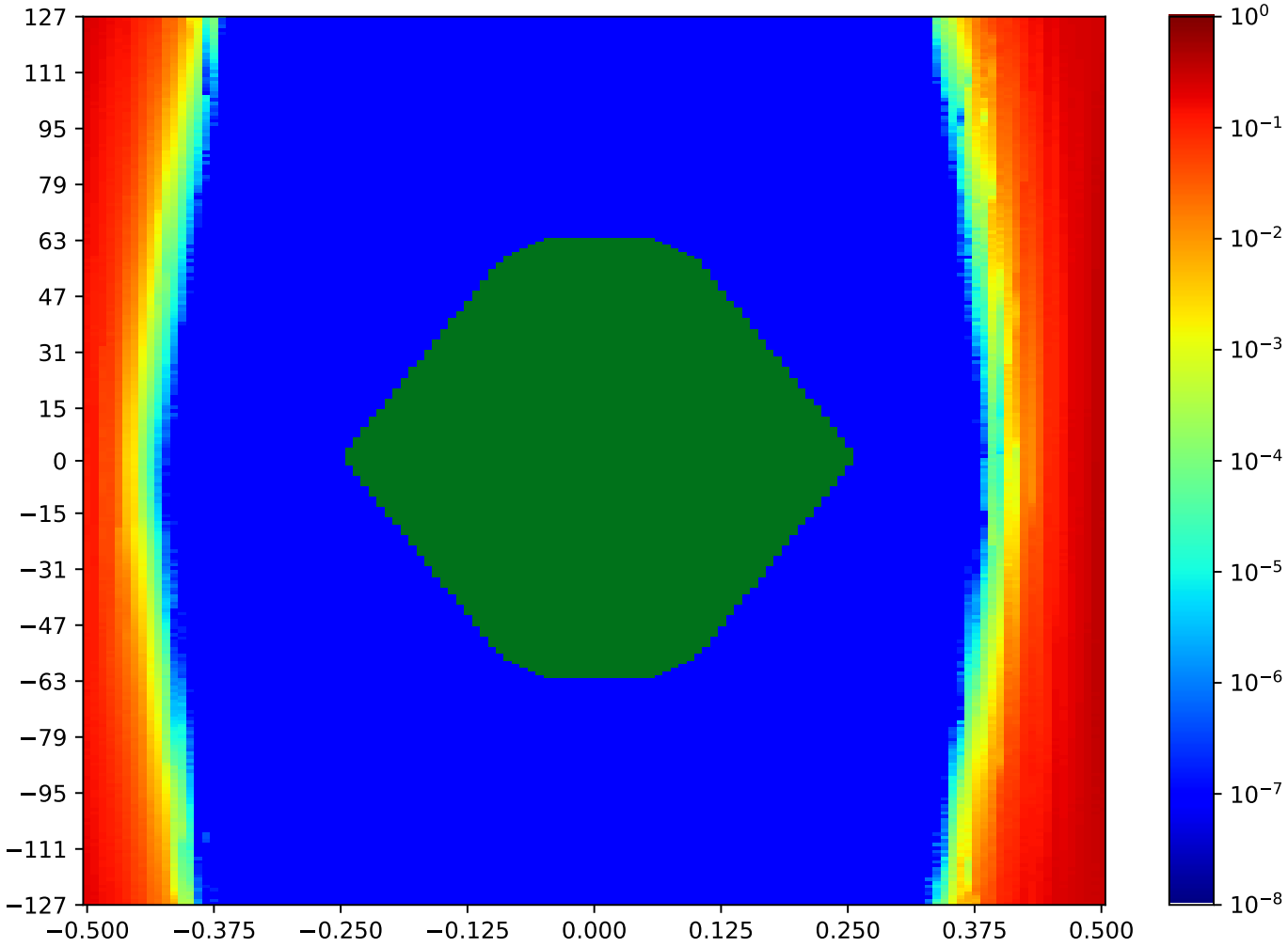


Figure 3.56: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.4 TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Table 3.52: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:43:20		2018-Sep-26 17:44:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24171	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

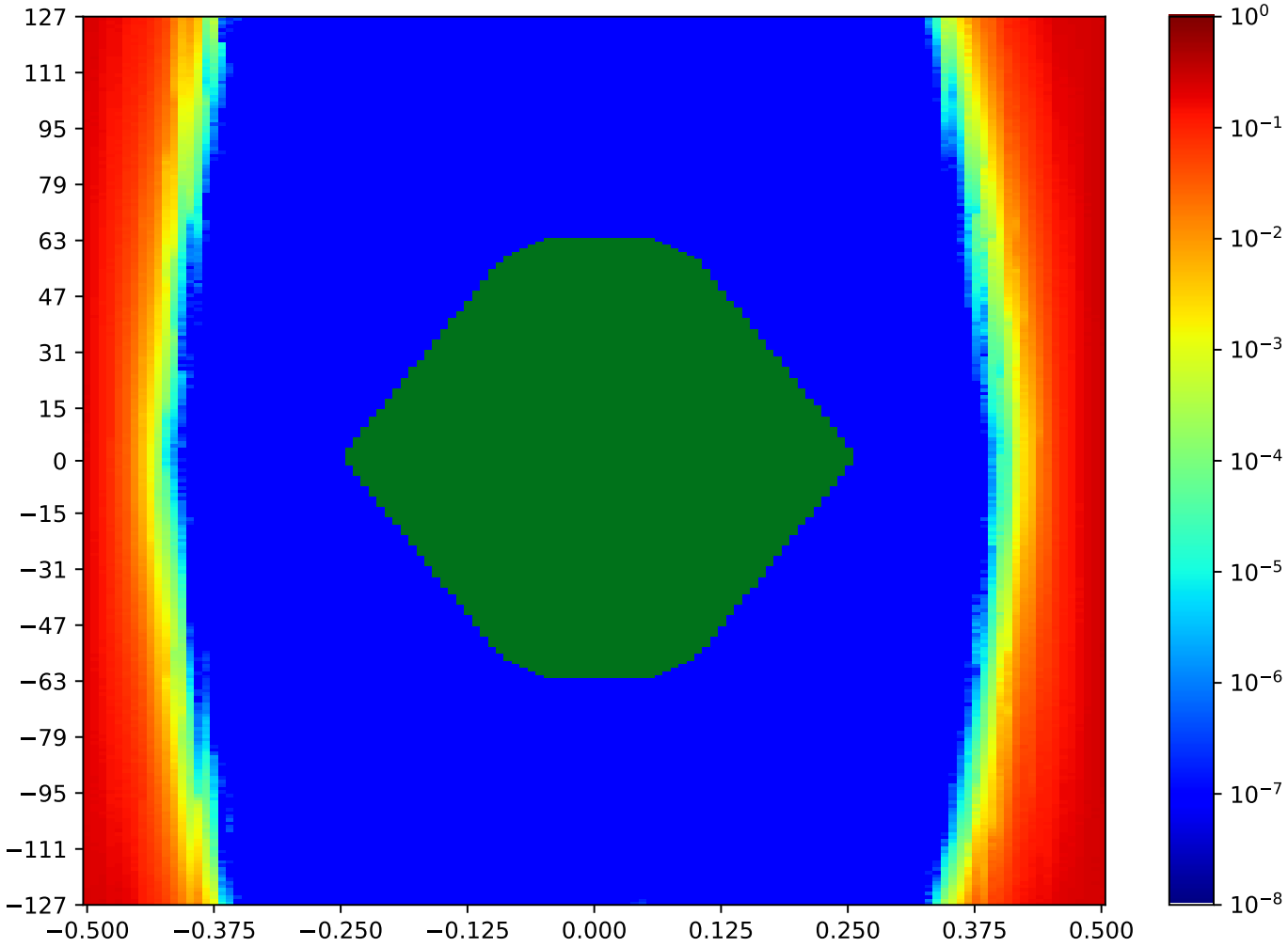


Figure 3.57: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.5 TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Table 3.53: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:49:32		2018-Sep-26 17:50:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24322	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

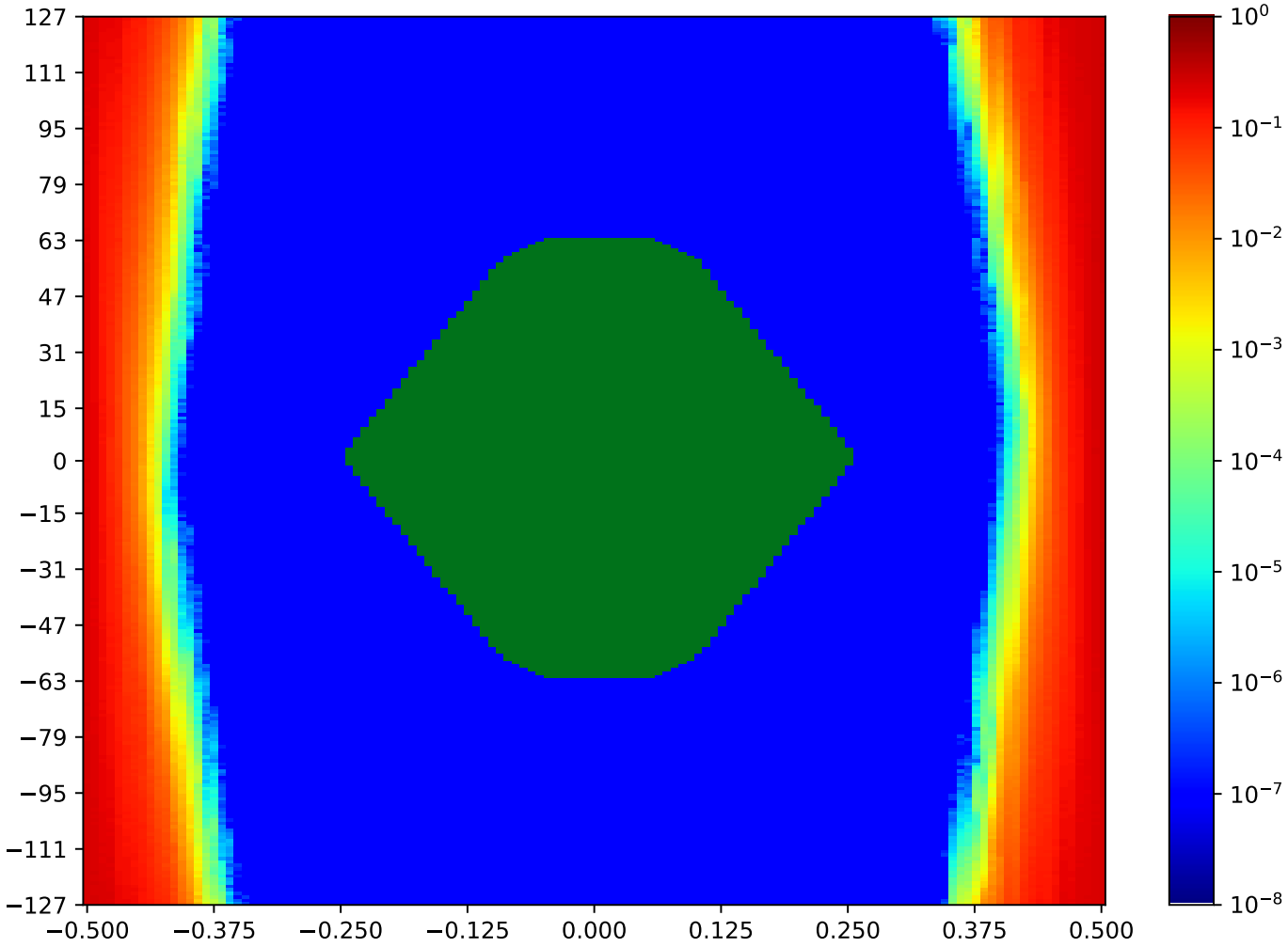


Figure 3.58: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.6 TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Table 3.54: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:40:50		2018-Sep-26 17:42:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24489	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

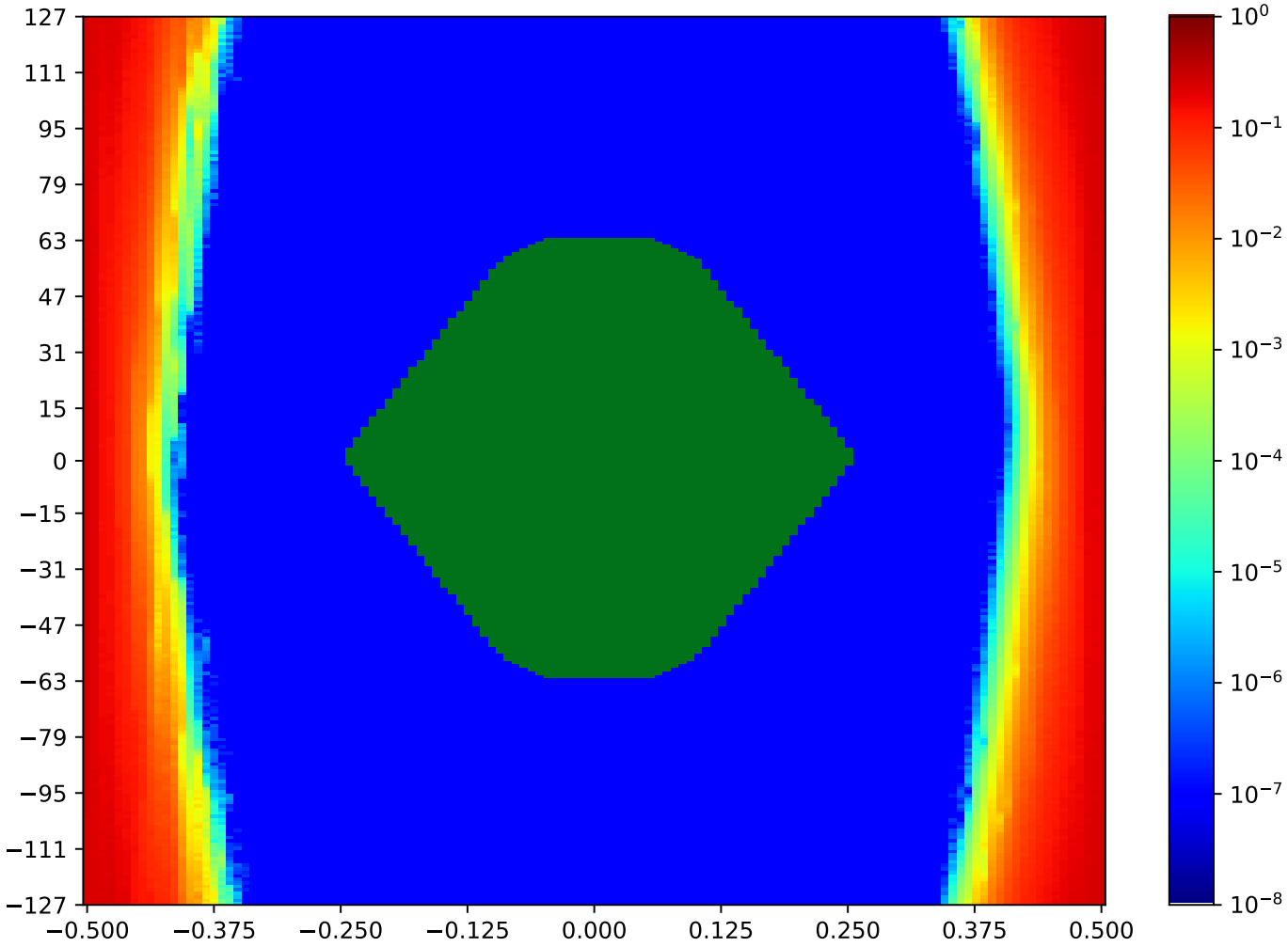


Figure 3.59: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.7 TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Table 3.55: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:45:49		2018-Sep-26 17:47:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24001	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

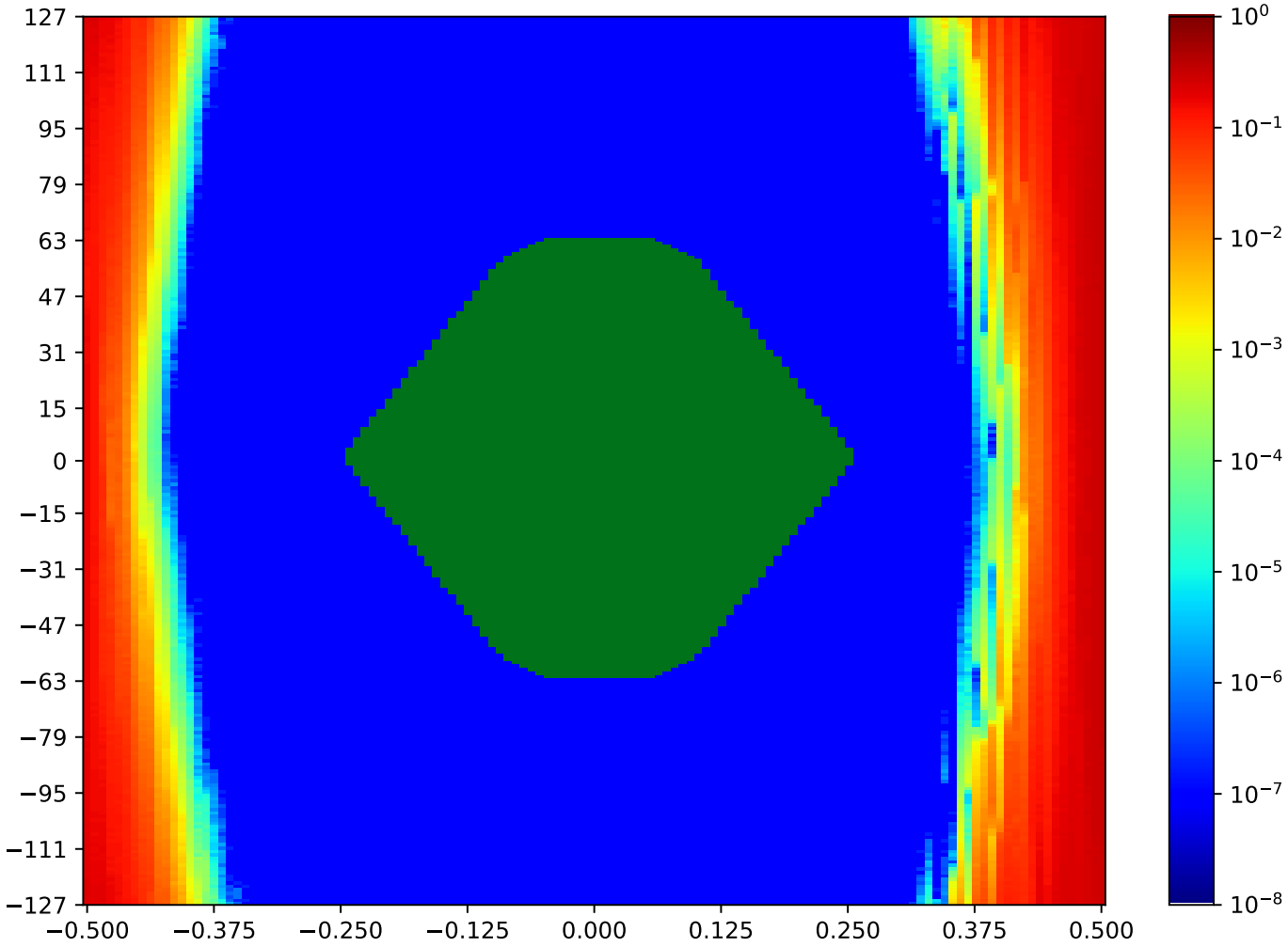


Figure 3.60: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.5.8 TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Table 3.56: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:48:18		2018-Sep-26 17:49:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24492	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

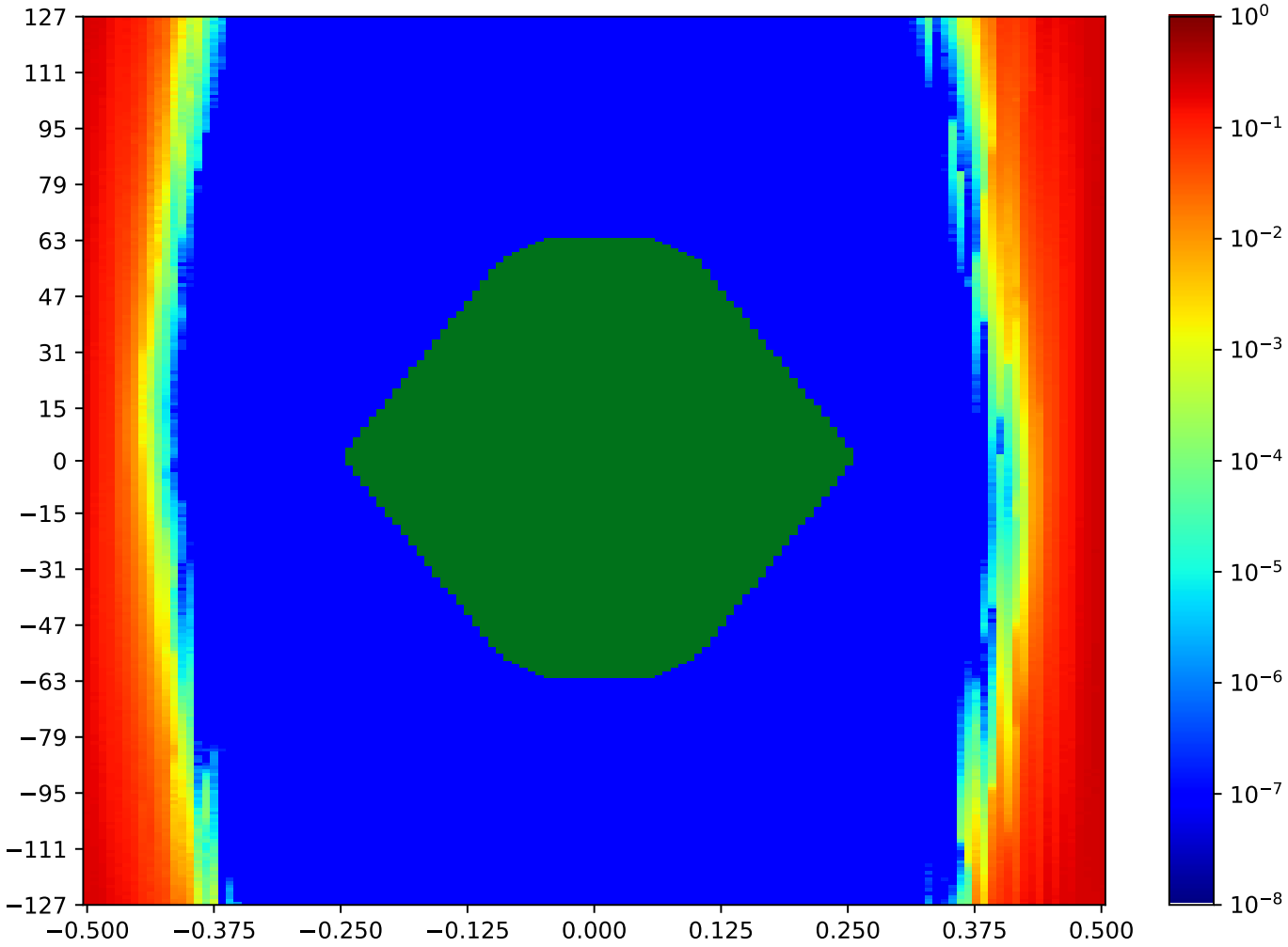


Figure 3.61: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.6 TRP J1 QSFP Loopback

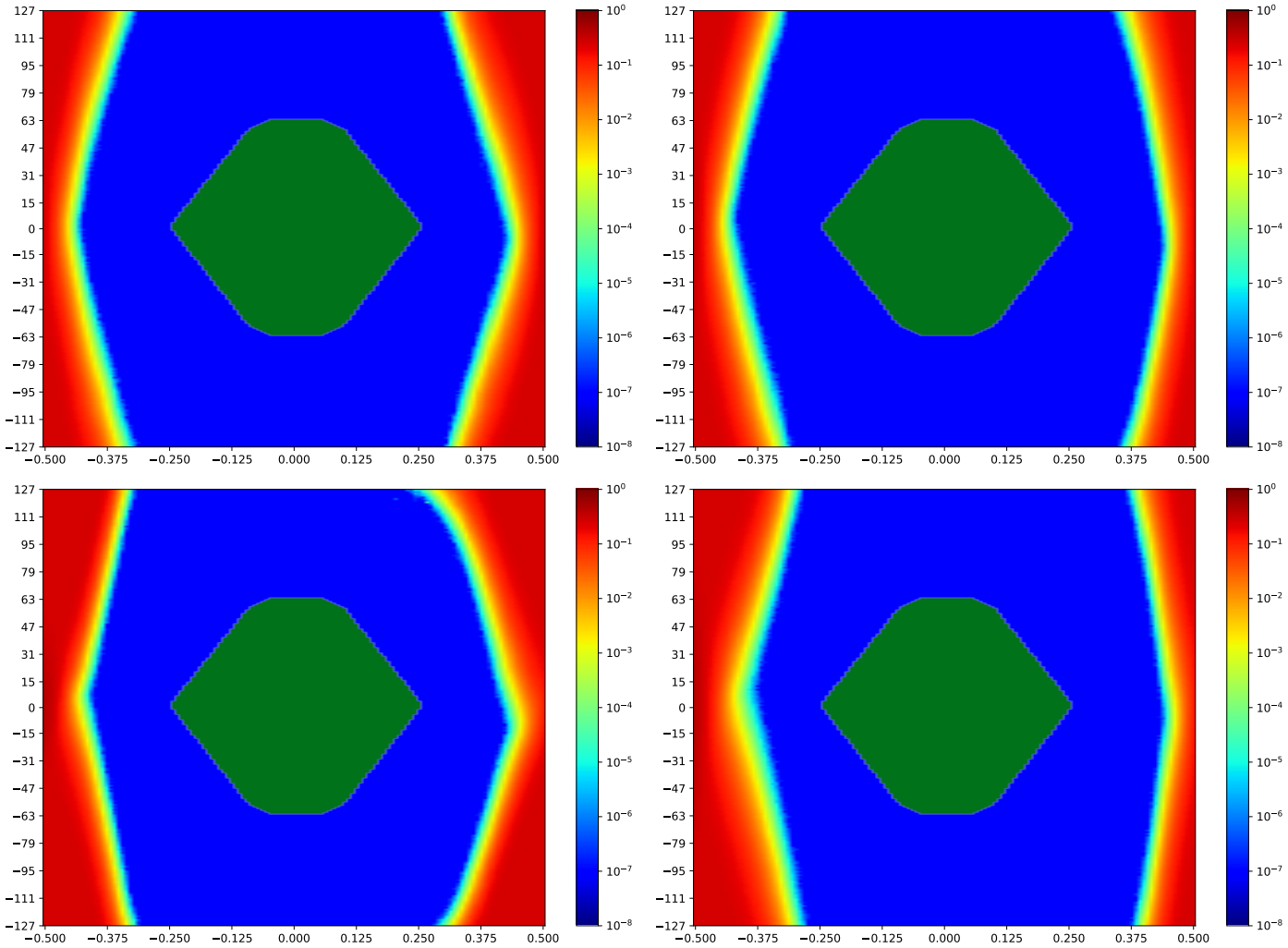


Figure 3.62: TRP J1 QSFP Loopback

A cross-reference to Figure 3.62. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.67.

3.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 3.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:50:47		2018-Sep-26 17:51:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23744	108	83.72%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

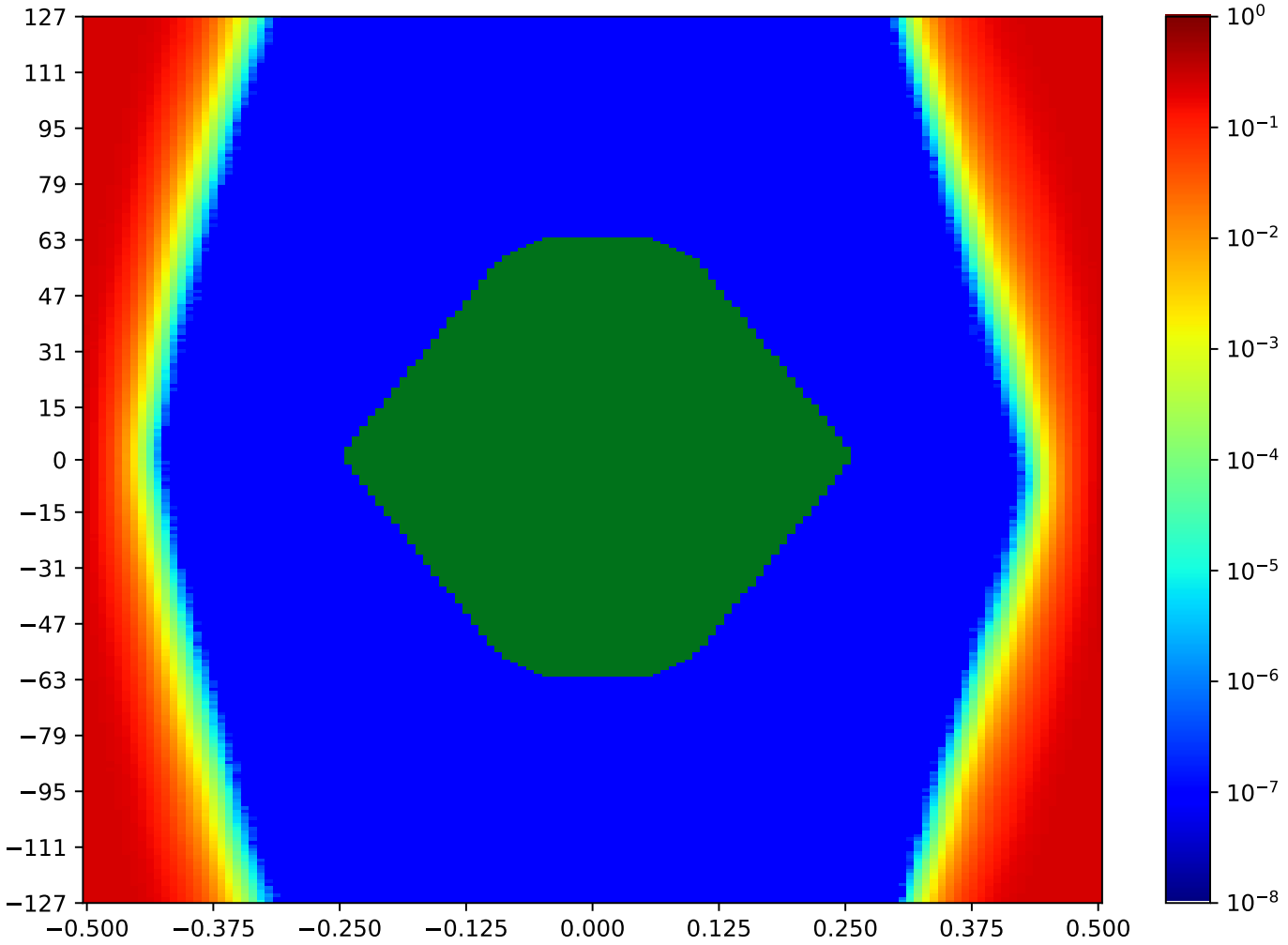


Figure 3.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 3.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:51:59		2018-Sep-26 17:53:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24532	107	82.95%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

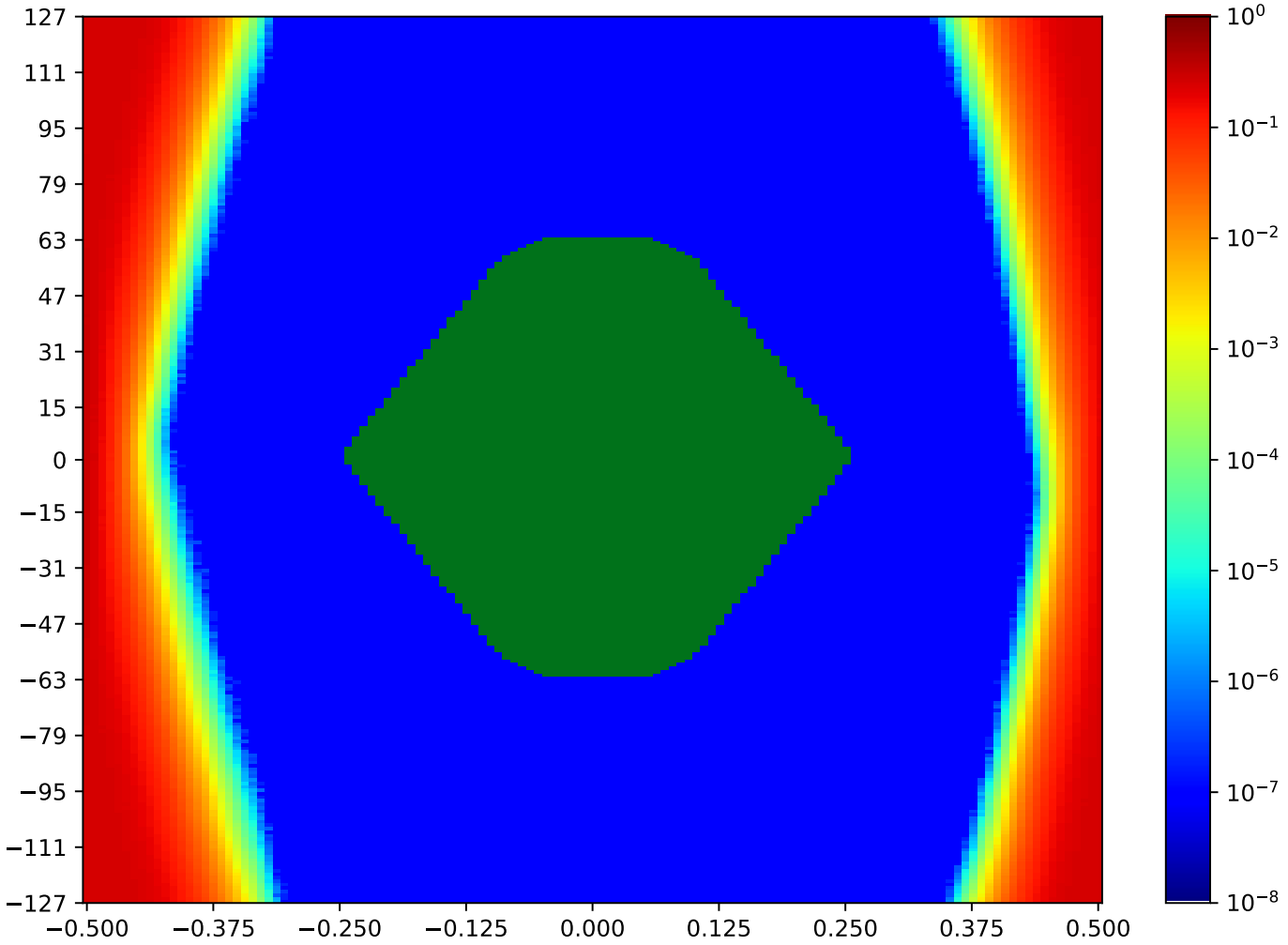


Figure 3.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 3.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:53:12		2018-Sep-26 17:54:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23141	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

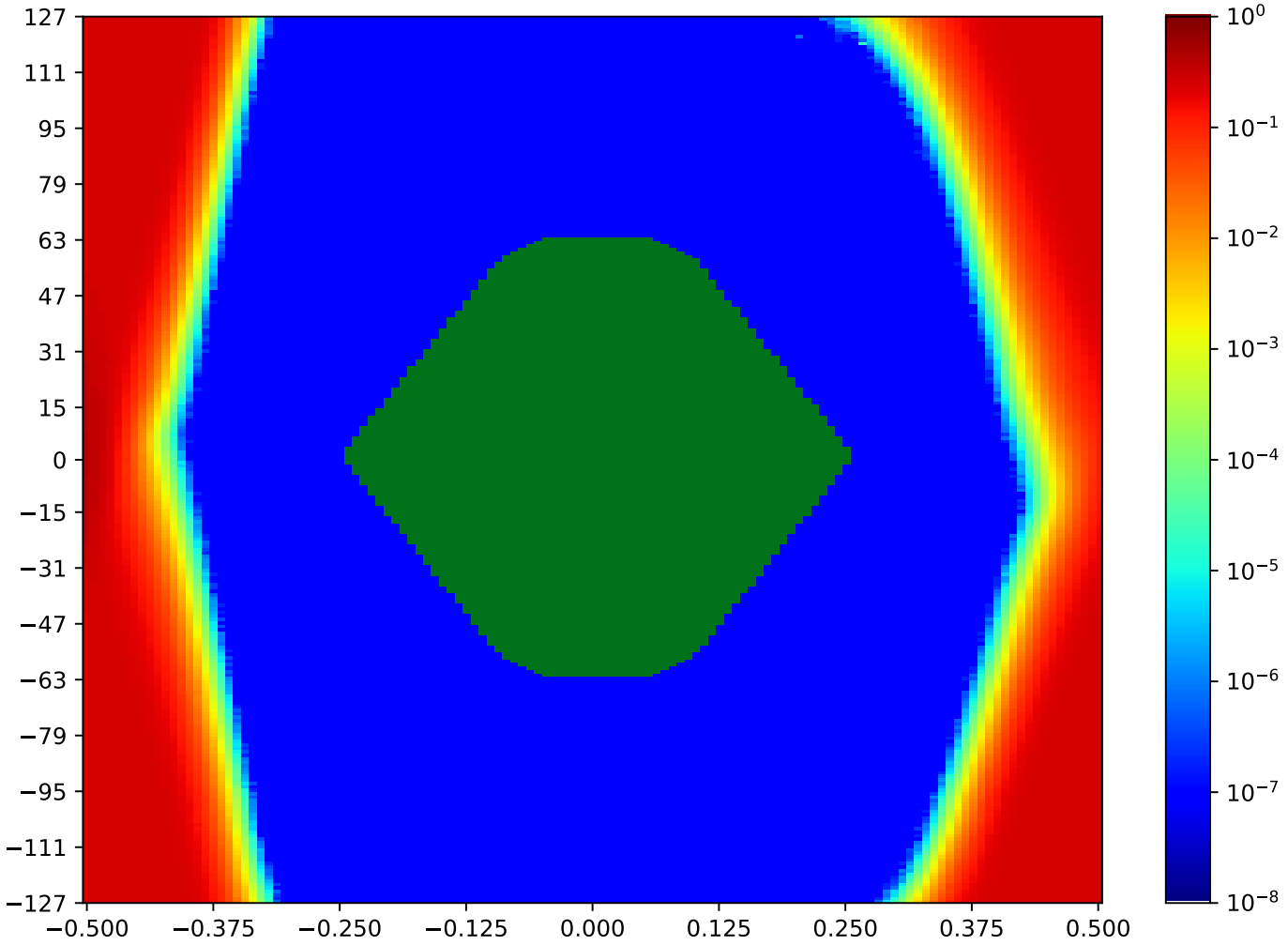


Figure 3.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 3.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:54:22		2018-Sep-26 17:55:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23546	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

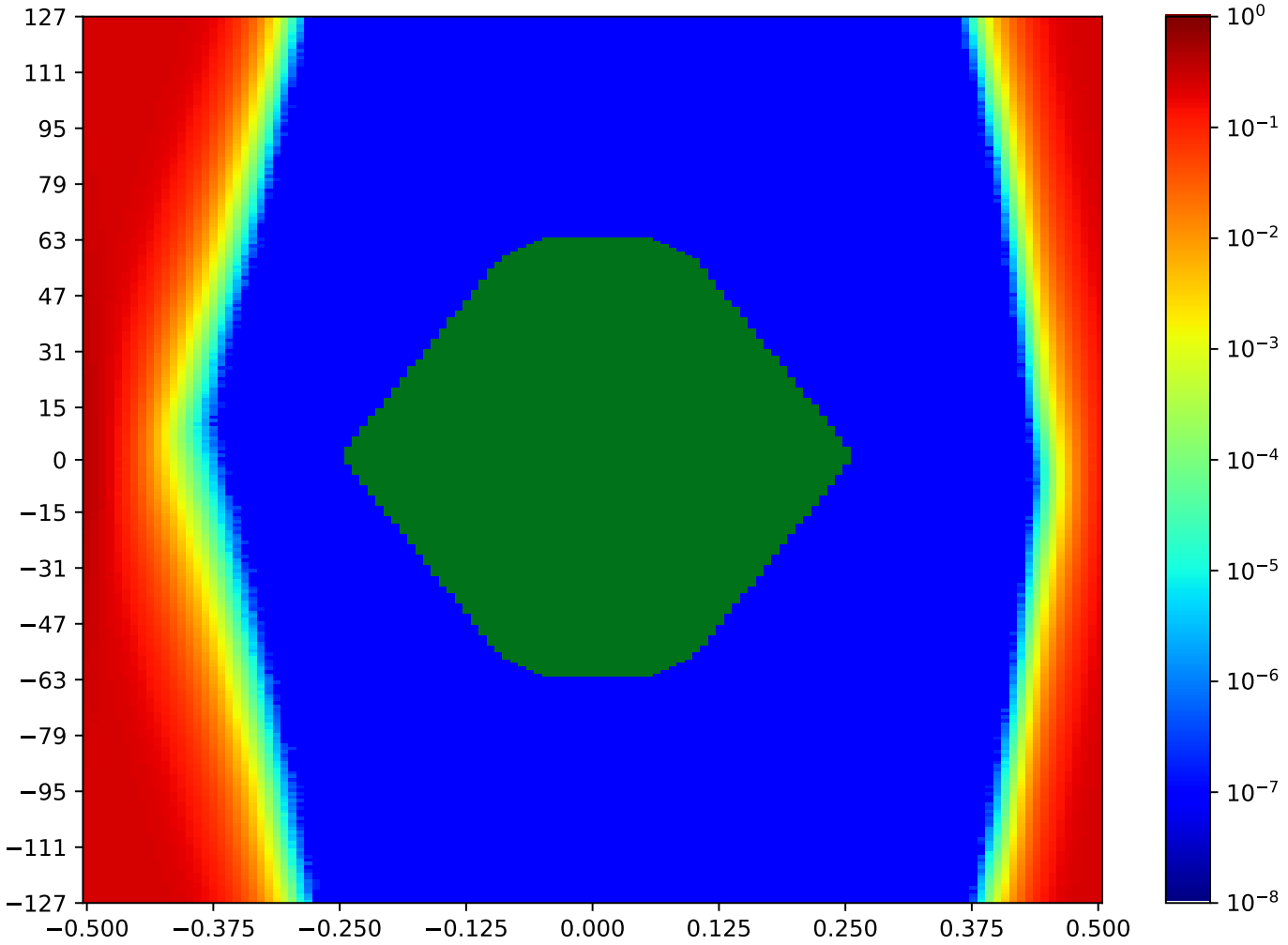


Figure 3.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.7 TRP J3 SFP Loopback

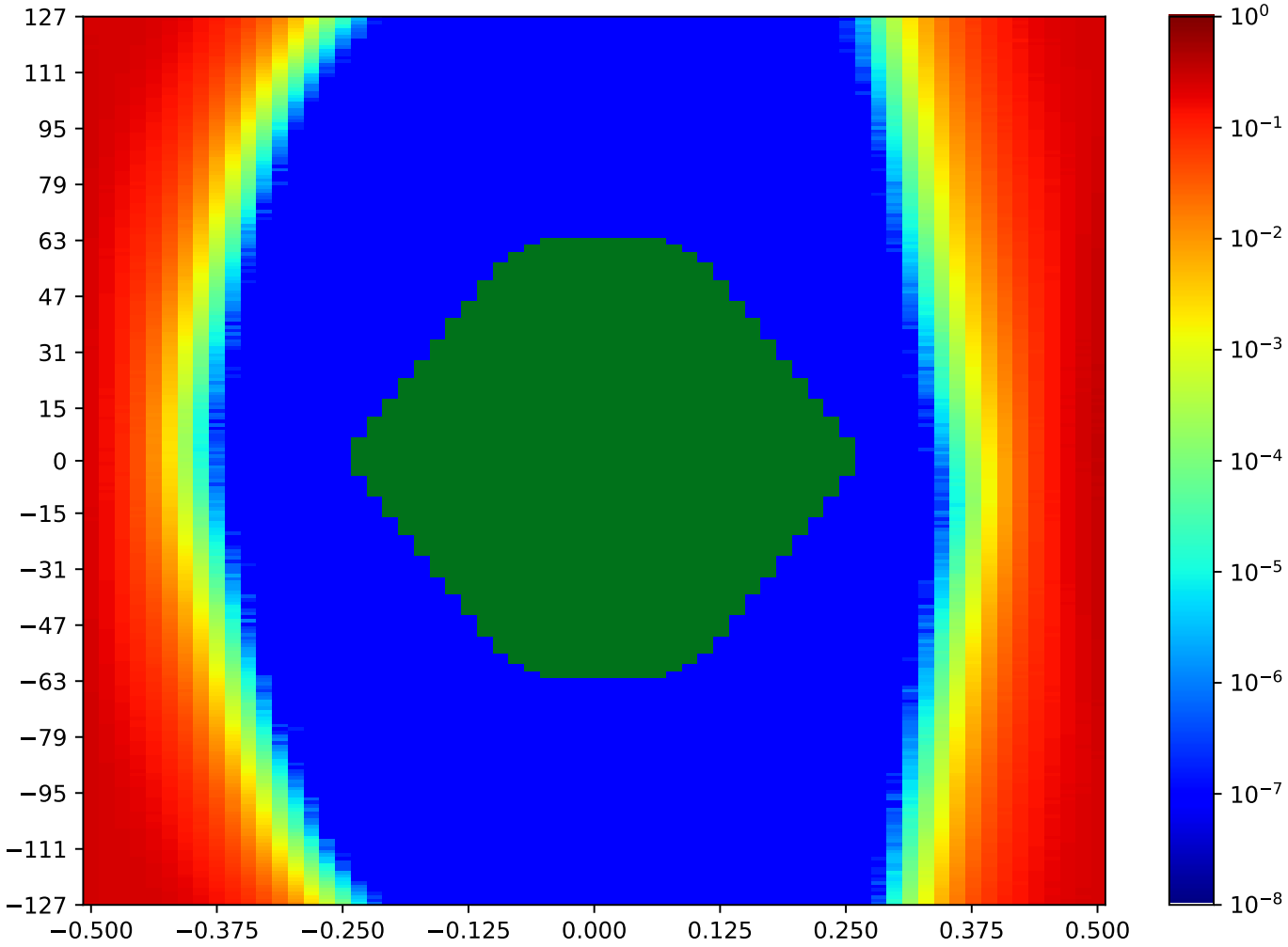


Figure 3.67: TRP J3 SFP Loopback

A cross-reference to Figure 3.67. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.69.

3.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 3.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 17:55:33		2018-Sep-26 17:56:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9992	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

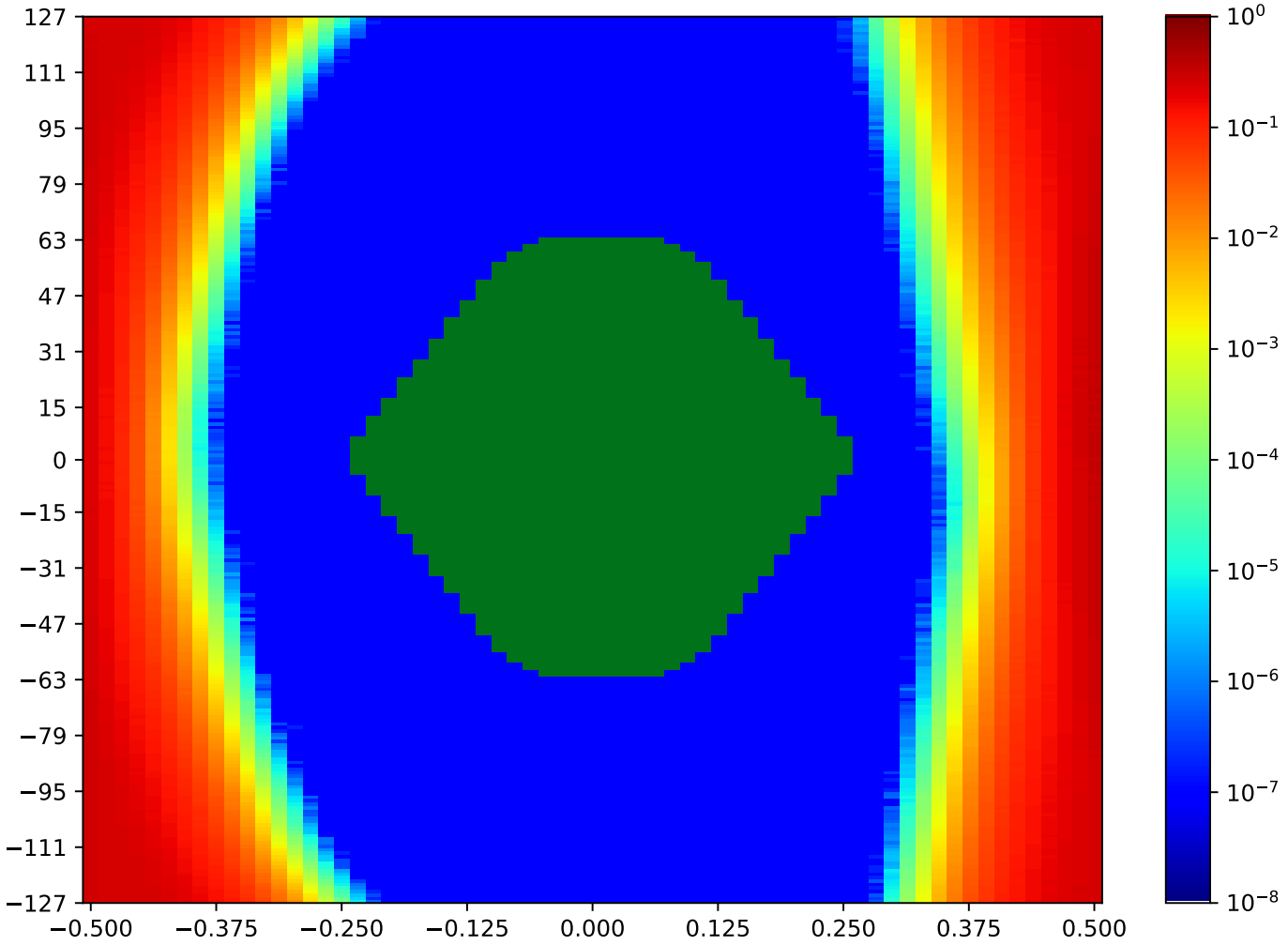


Figure 3.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 3.67. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8 MSP_A TRP On board links

A cross-reference to Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.98.

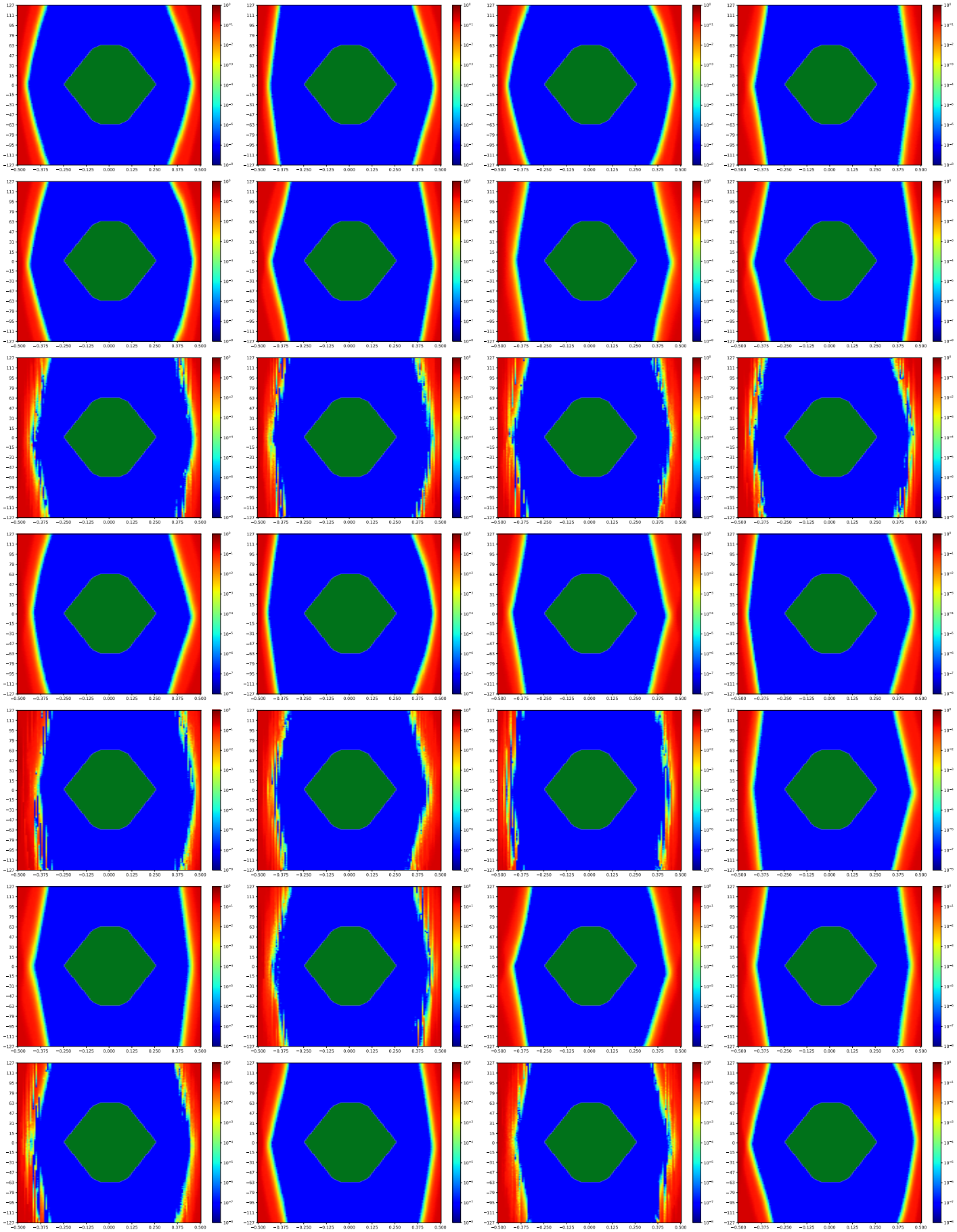


Figure 3.69: MSP_A TRP On board links

3.8.1 MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Table 3.62: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:56:10		2018-Sep-26 17:57:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24960	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

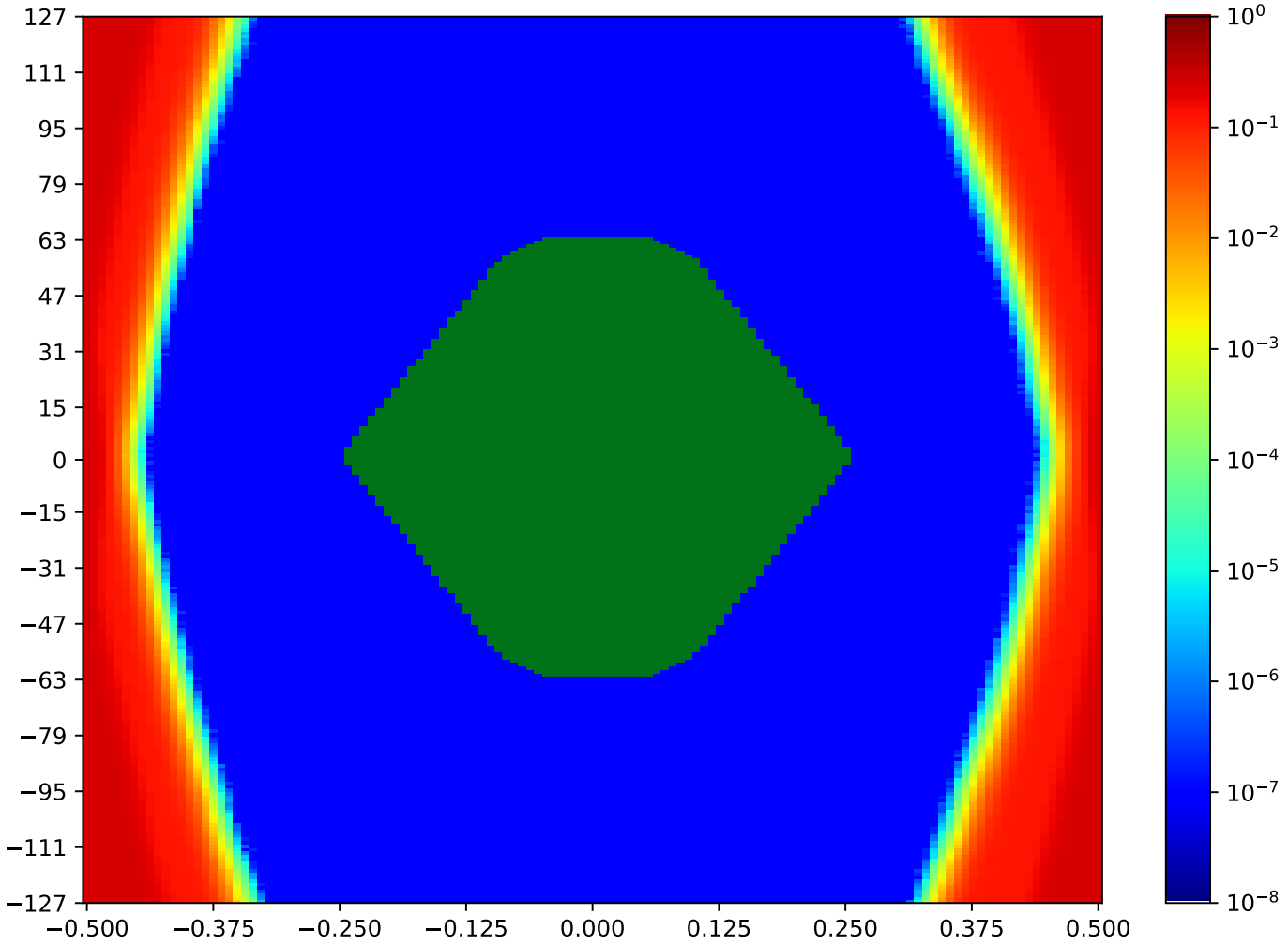


Figure 3.70: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.2 MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Table 3.63: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:57:23		2018-Sep-26 17:58:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25874	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

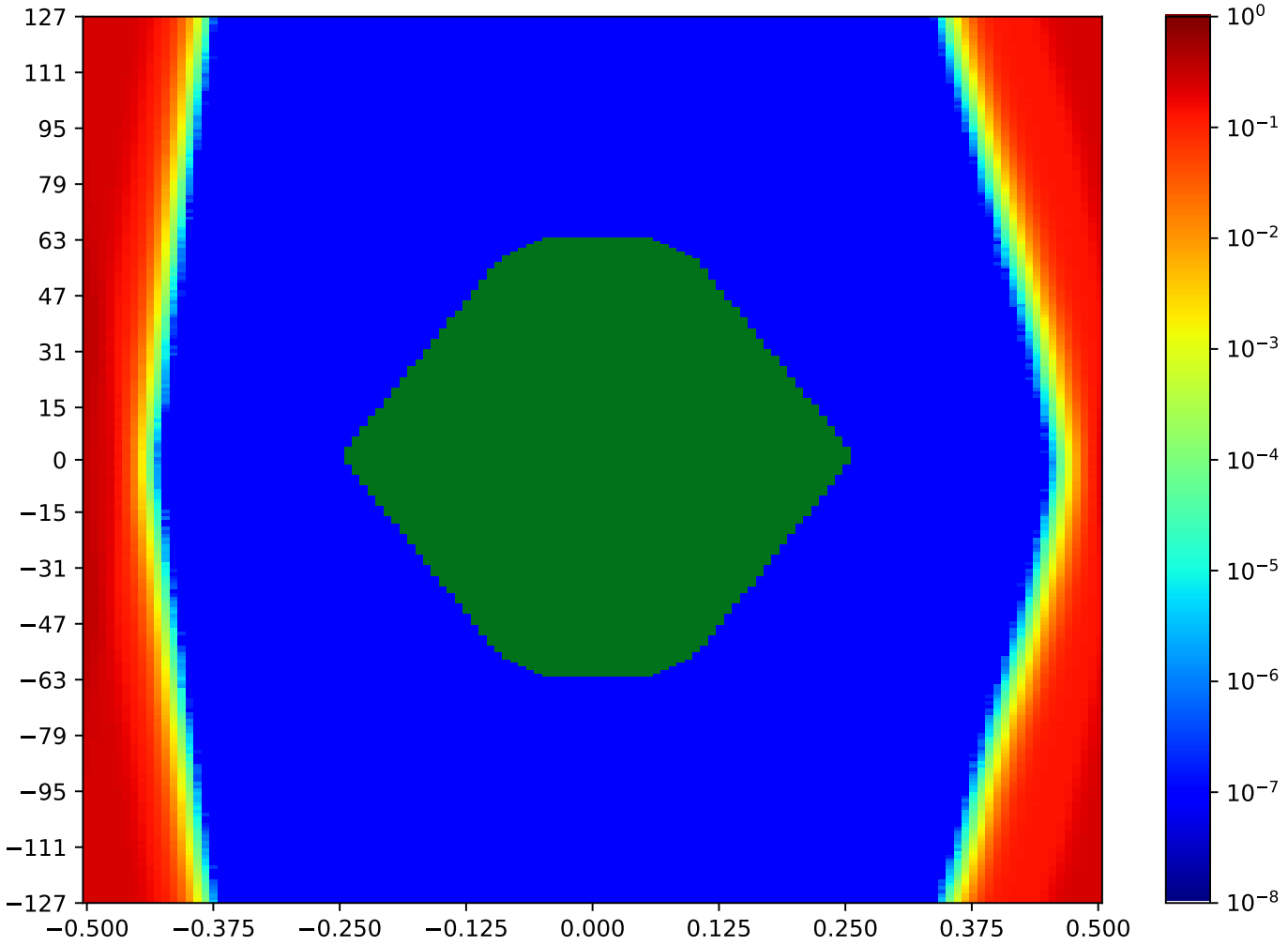


Figure 3.71: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.3 MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Table 3.64: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:58:36		2018-Sep-26 17:59:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25279	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

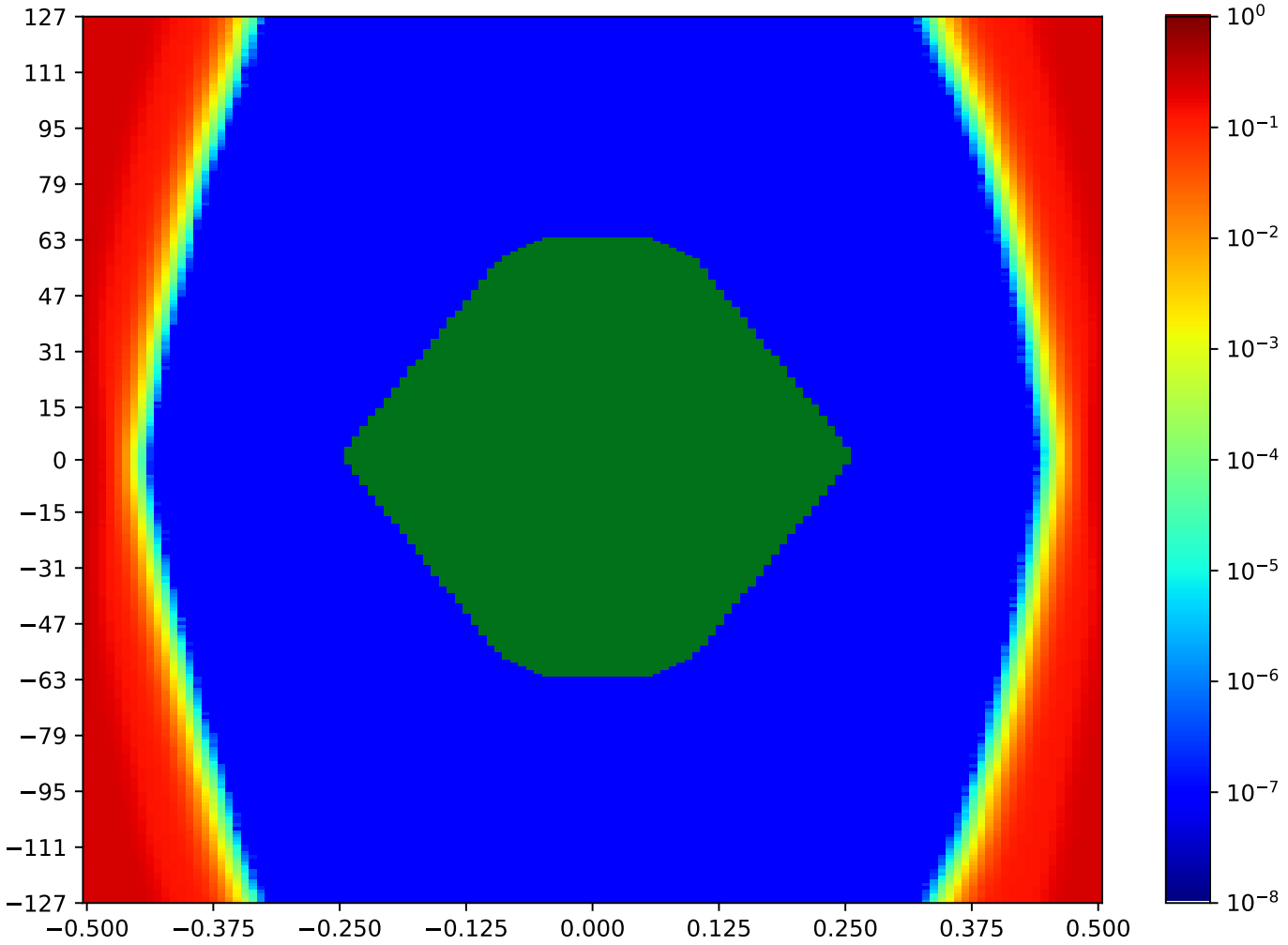


Figure 3.72: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.4 MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Table 3.65: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:59:49		2018-Sep-26 18:01:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24909	106	82.17%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

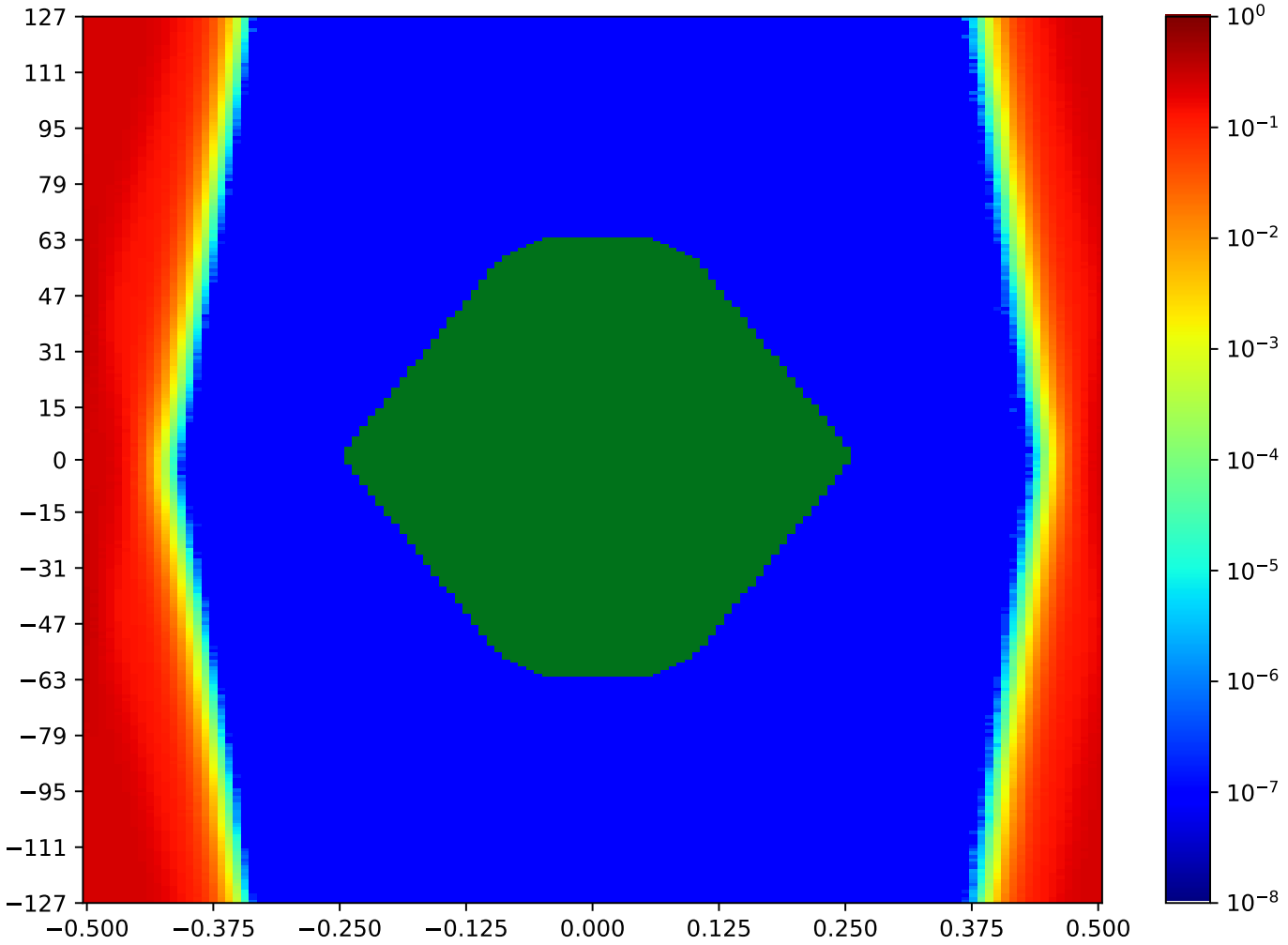


Figure 3.73: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.5 MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Table 3.66: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:01:02		2018-Sep-26 18:02:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25324	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

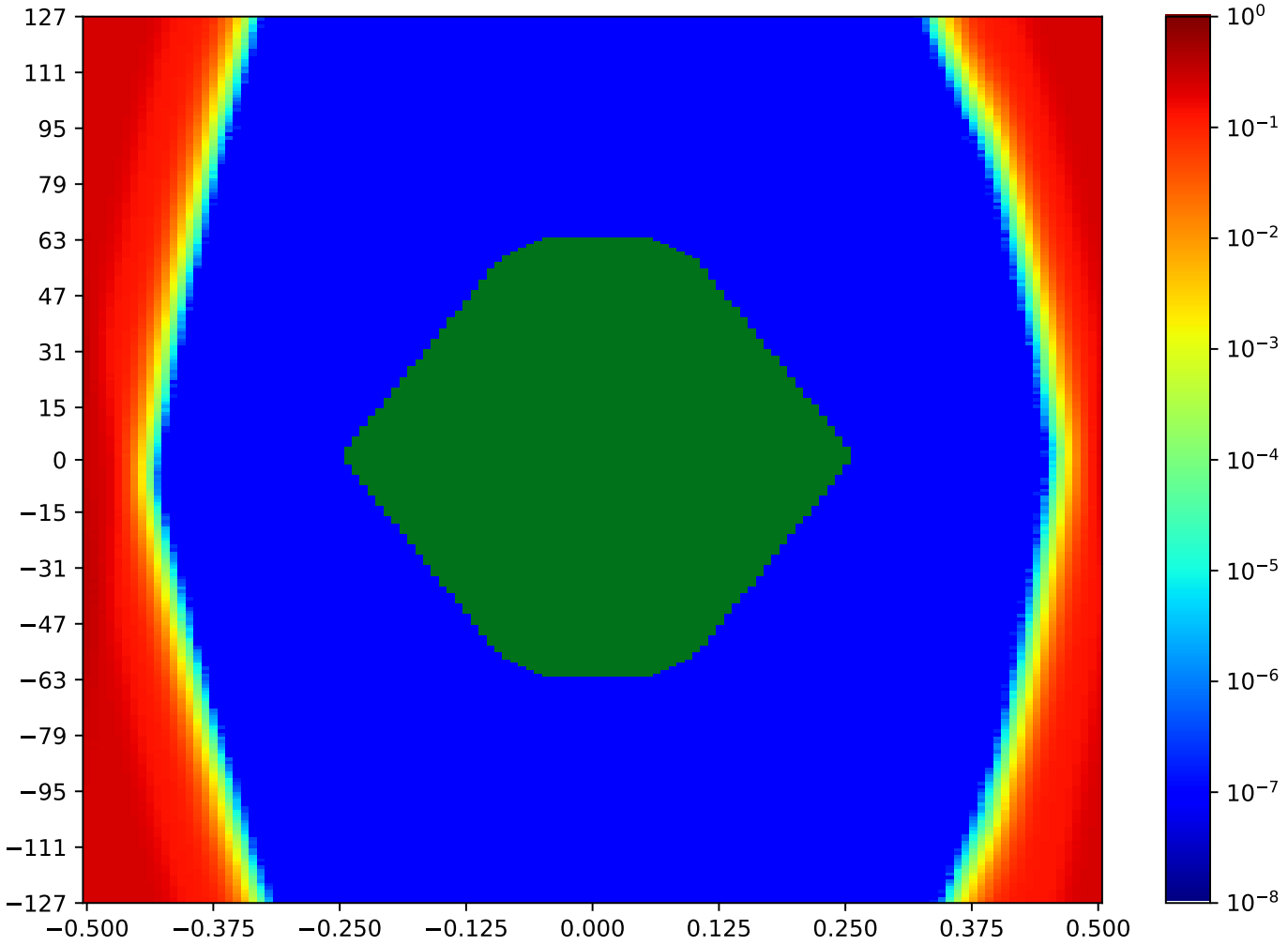


Figure 3.74: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.6 MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Table 3.67: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:02:15		2018-Sep-26 18:03:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25263	109	84.50%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

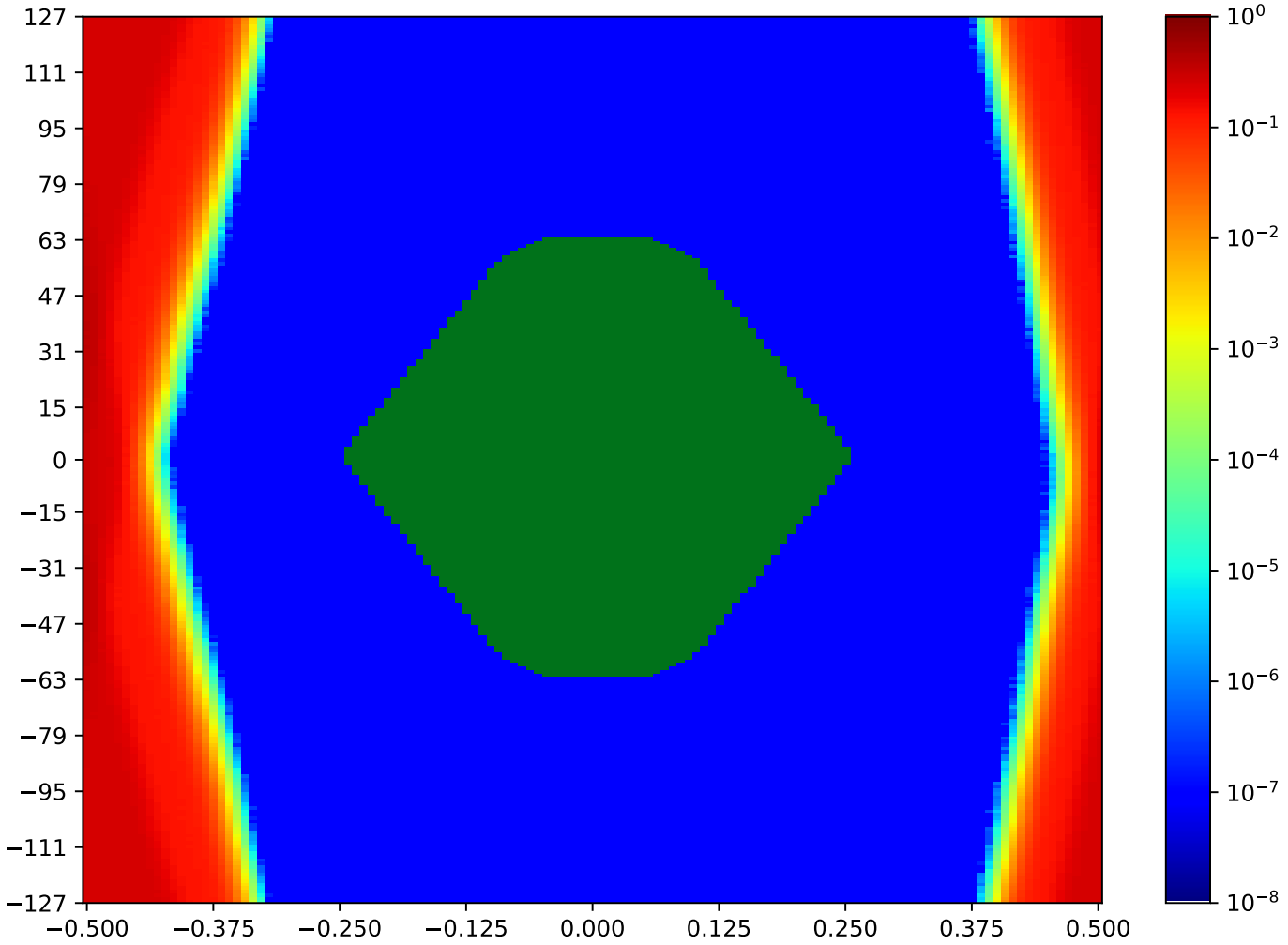


Figure 3.75: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.7 MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Table 3.68: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:03:27		2018-Sep-26 18:04:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24060	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

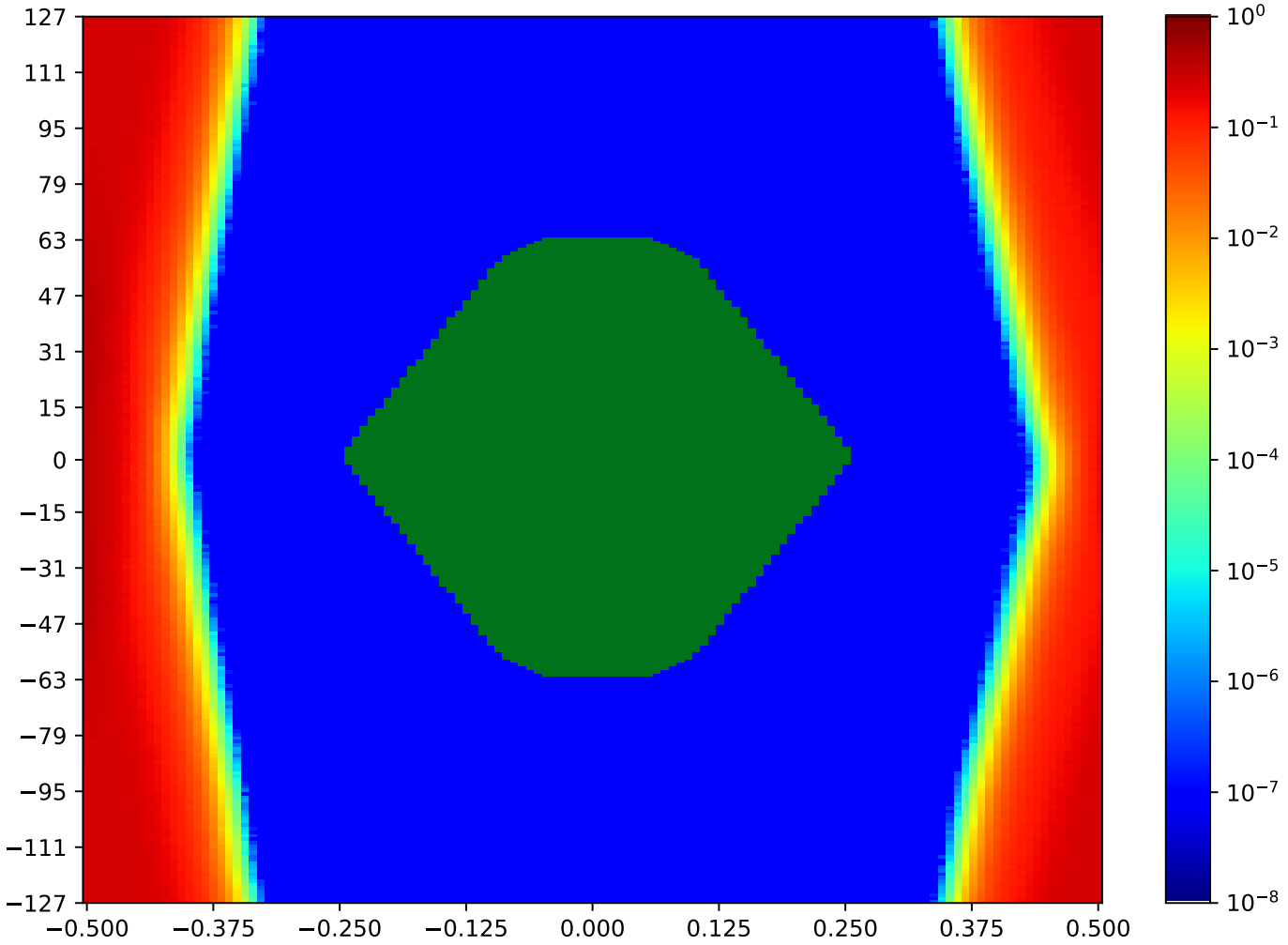


Figure 3.76: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.8 MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Table 3.69: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:04:38		2018-Sep-26 18:05:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25403	109	84.50%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

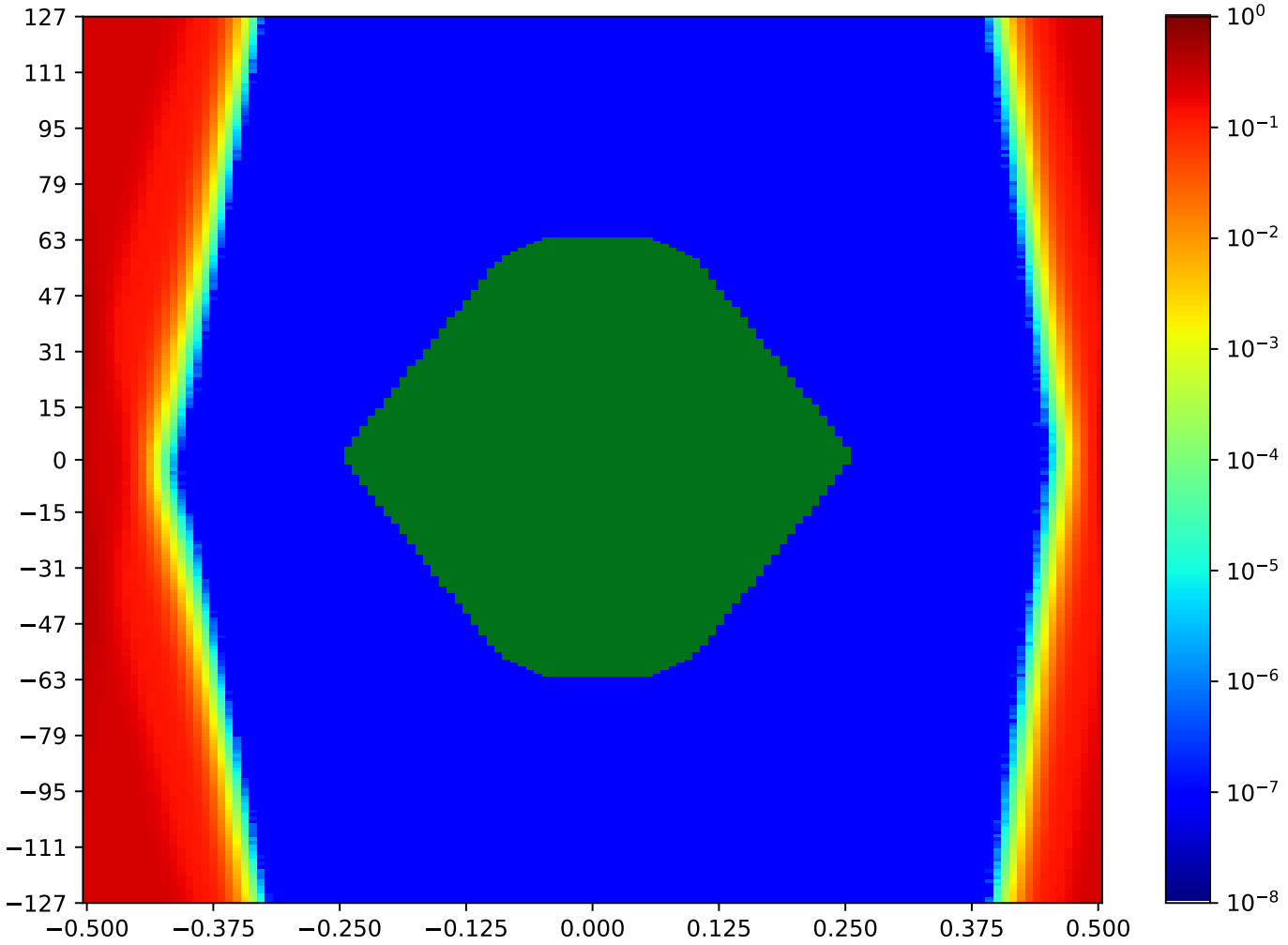


Figure 3.77: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.9 MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Table 3.70: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:05:51		2018-Sep-26 18:07:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25194	111	85.27%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

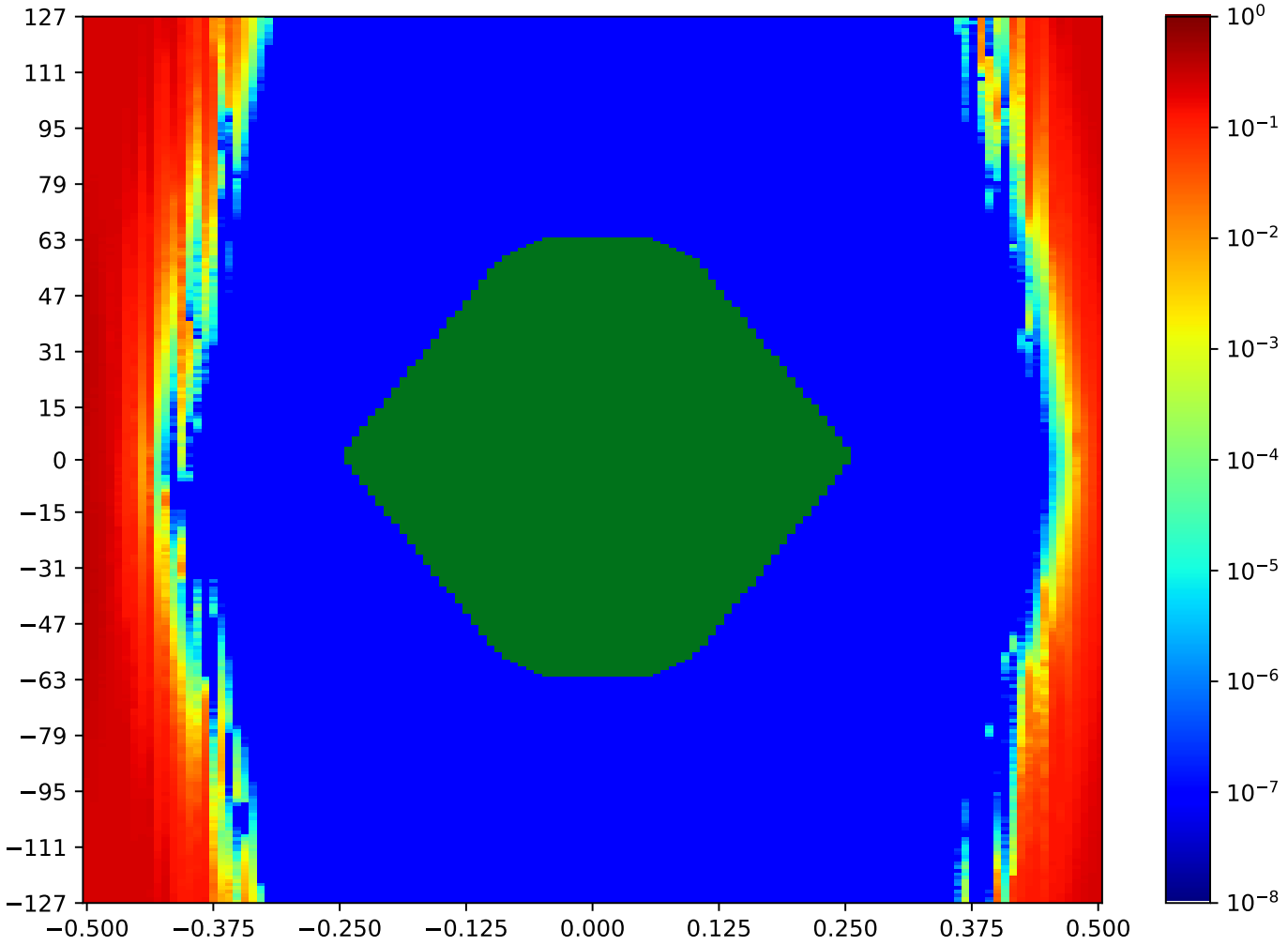


Figure 3.78: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.10 MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Table 3.71: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:07:04		2018-Sep-26 18:08:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25468	110	84.50%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

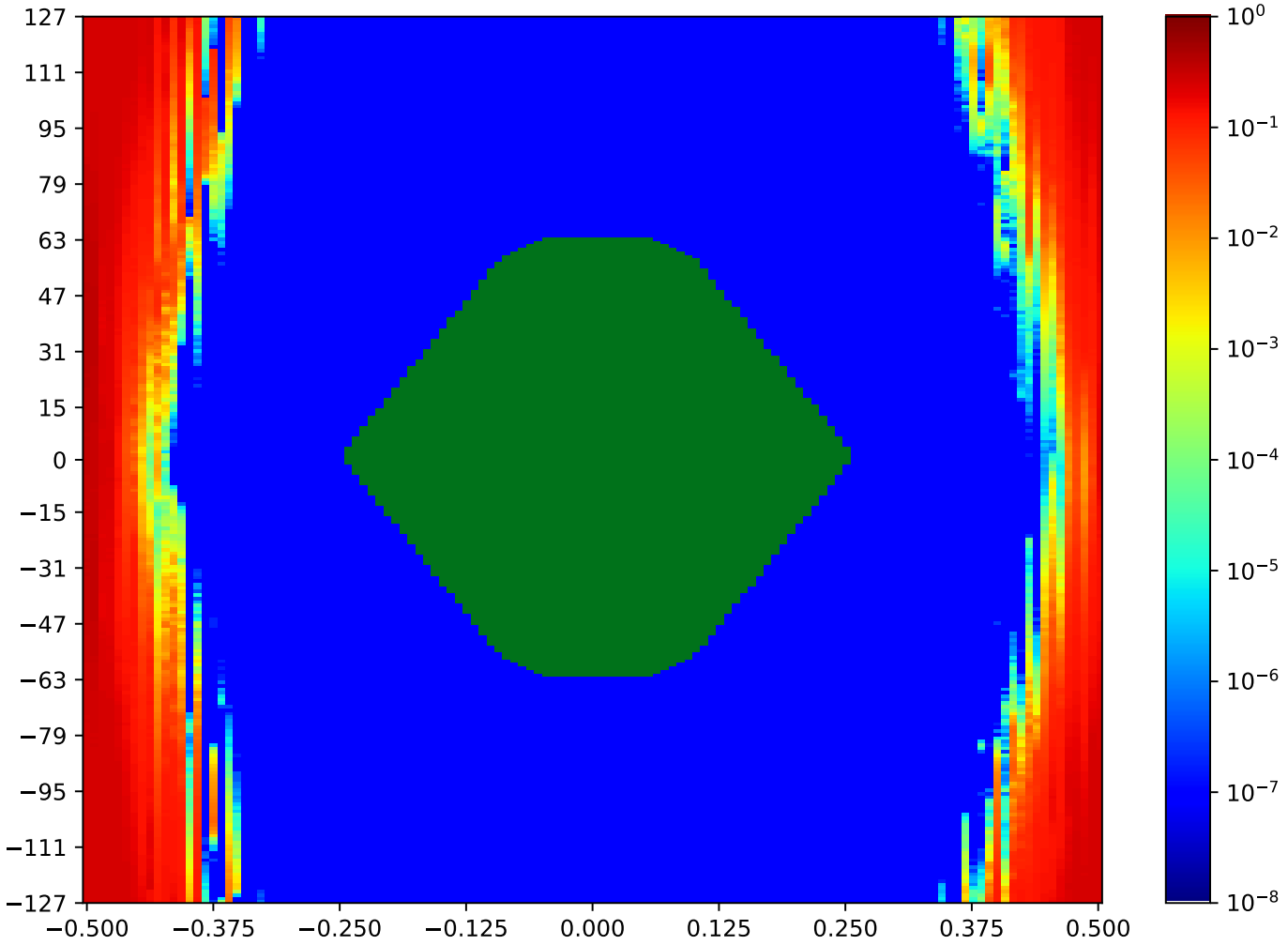


Figure 3.79: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.11 MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Table 3.72: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:08:16		2018-Sep-26 18:09:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25142	108	83.72%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

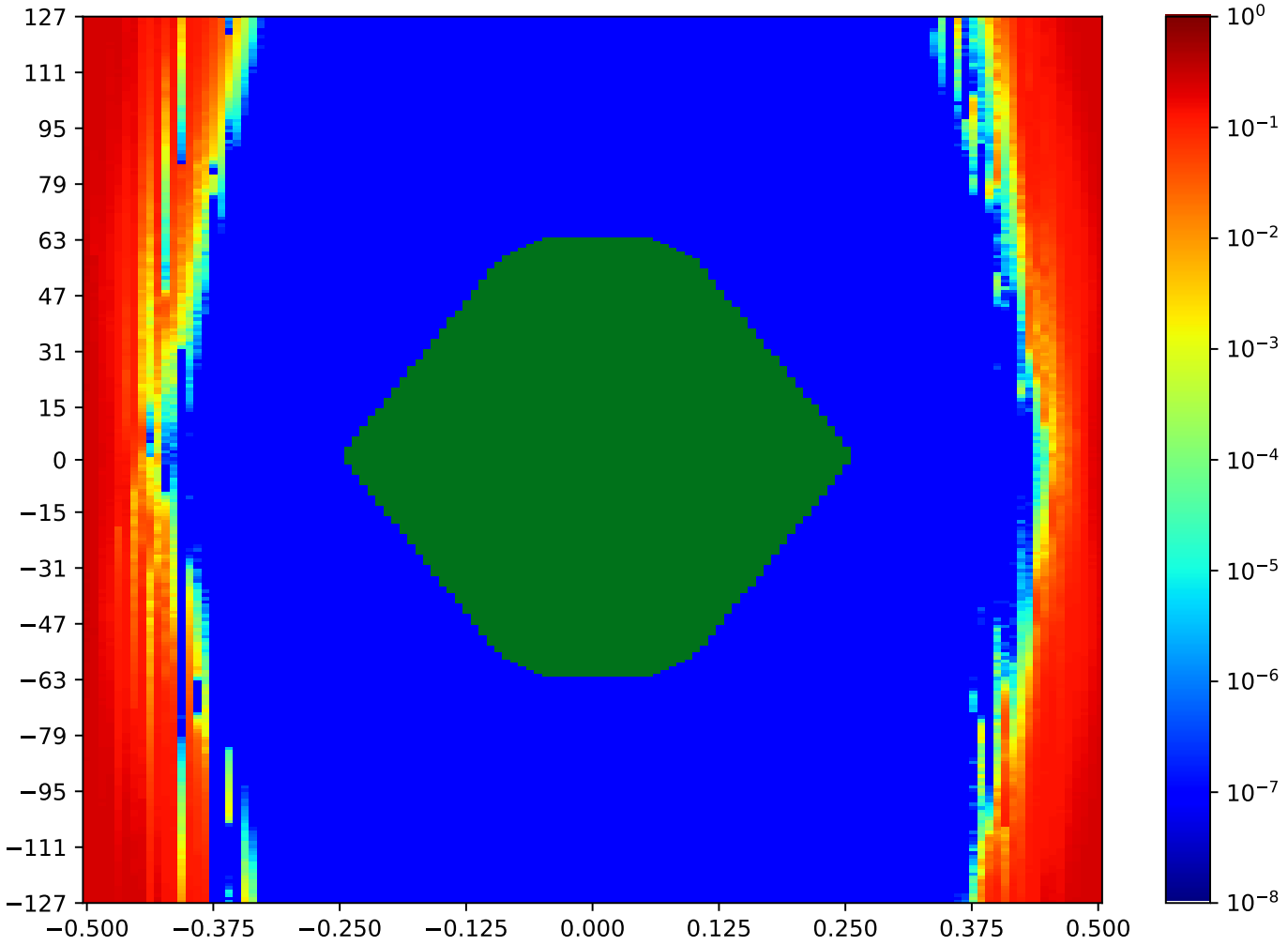


Figure 3.80: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.12 MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Table 3.73: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:09:28		2018-Sep-26 18:10:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25176	107	82.95%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

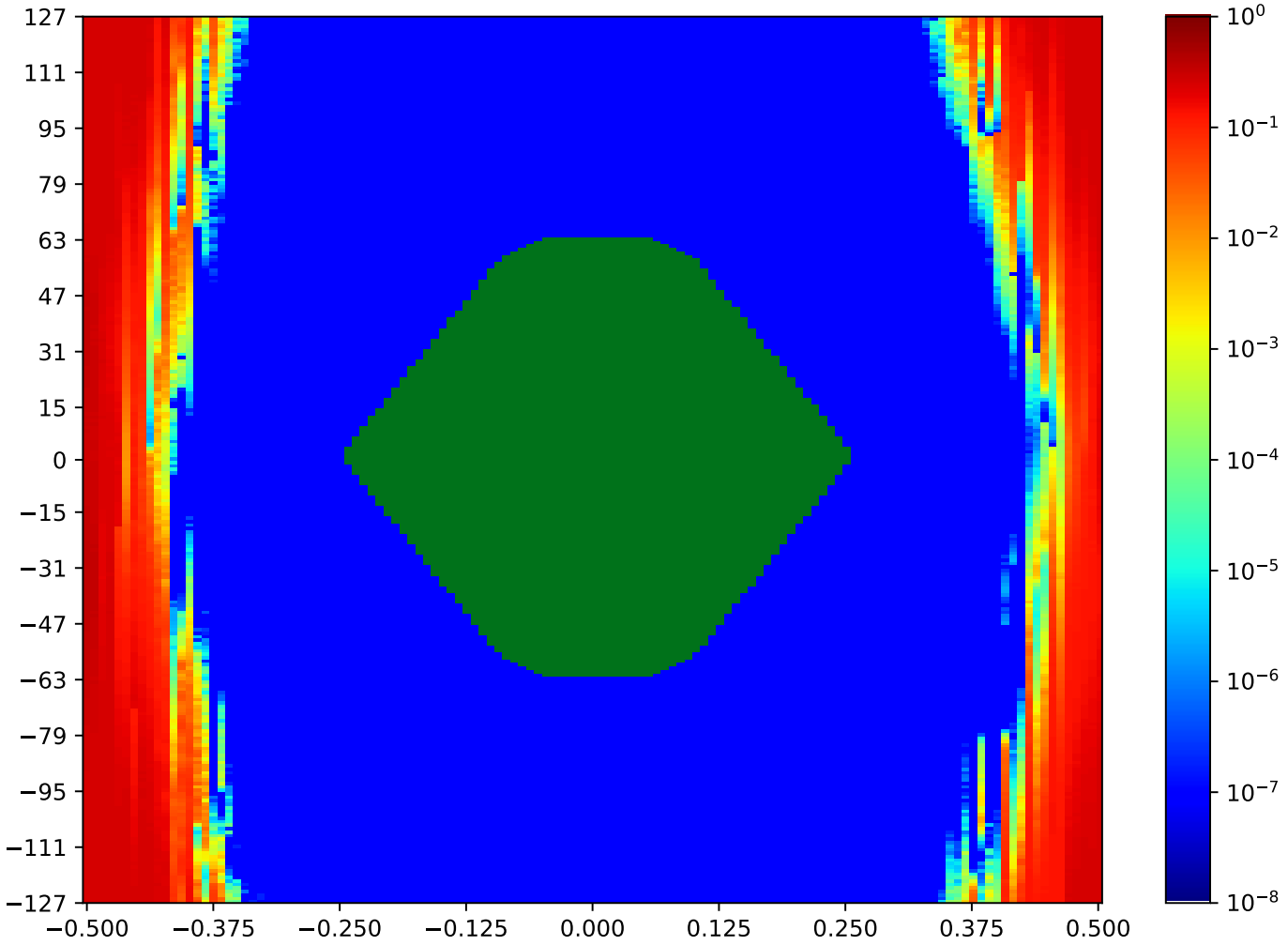


Figure 3.81: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.13 MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Table 3.74: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:10:41		2018-Sep-26 18:11:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24242	108	83.72%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

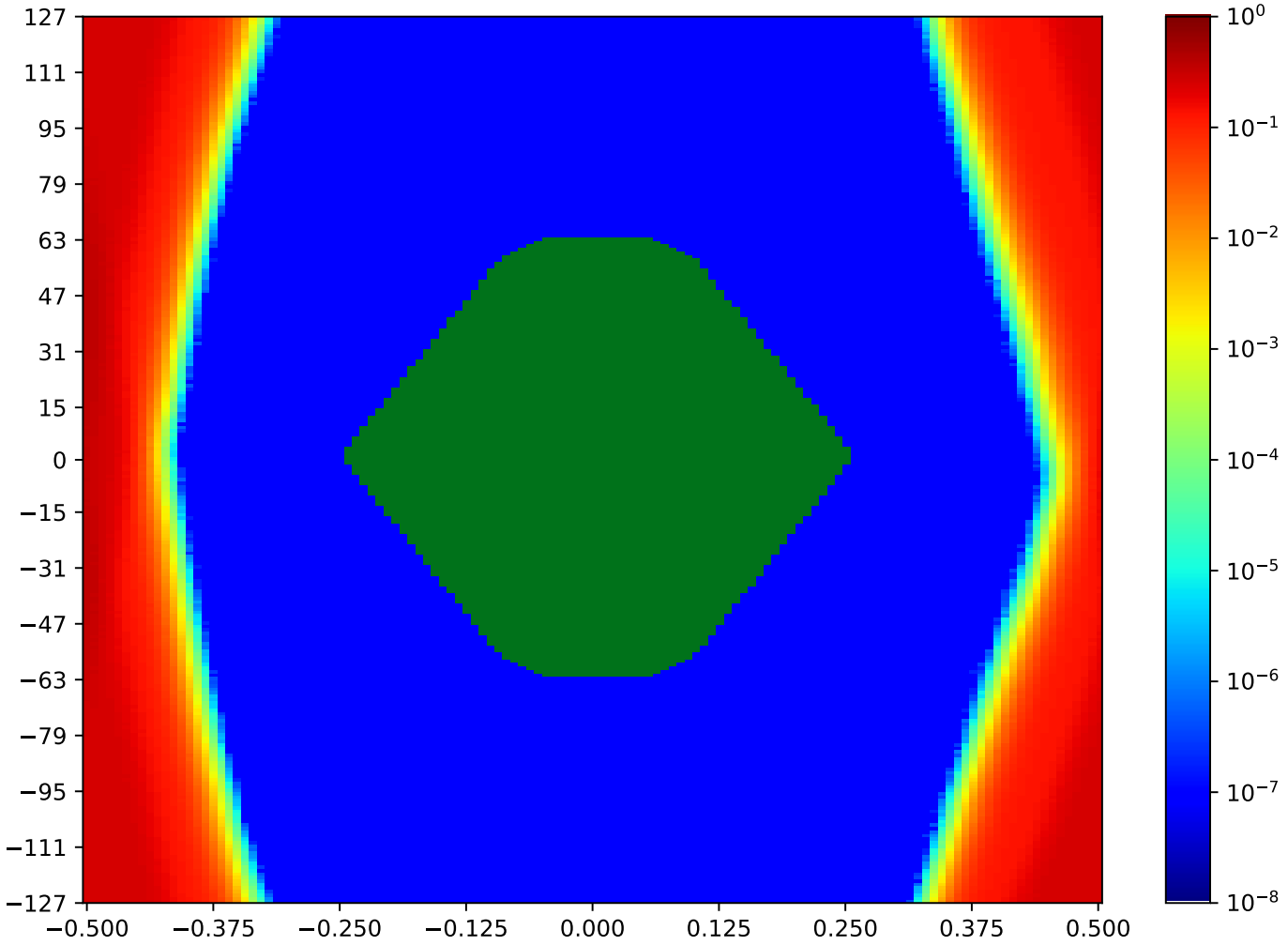


Figure 3.82: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.14 MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Table 3.75: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:11:53		2018-Sep-26 18:13:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26331	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

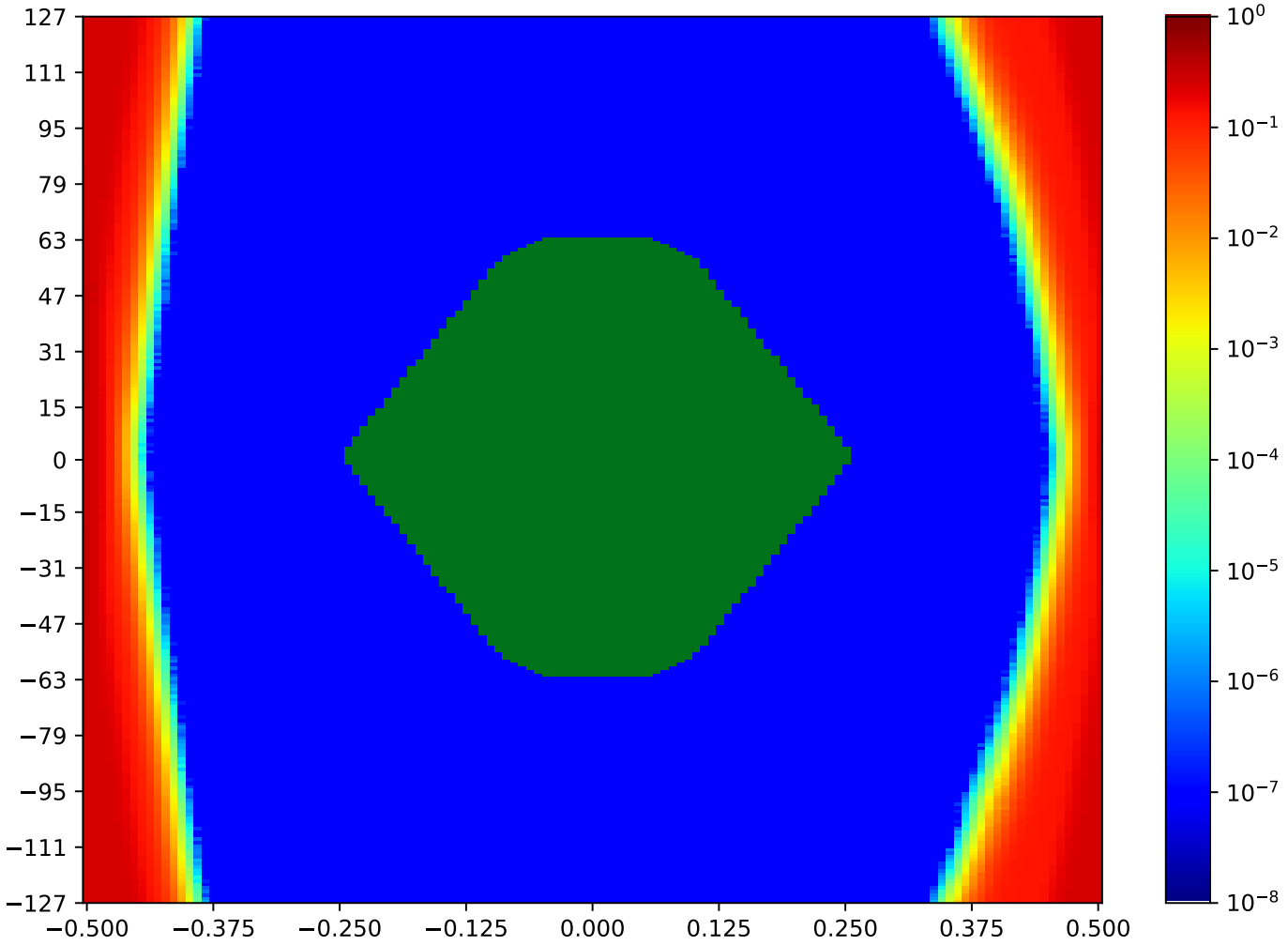


Figure 3.83: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.15 MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Table 3.76: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:13:06		2018-Sep-26 18:14:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23881	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

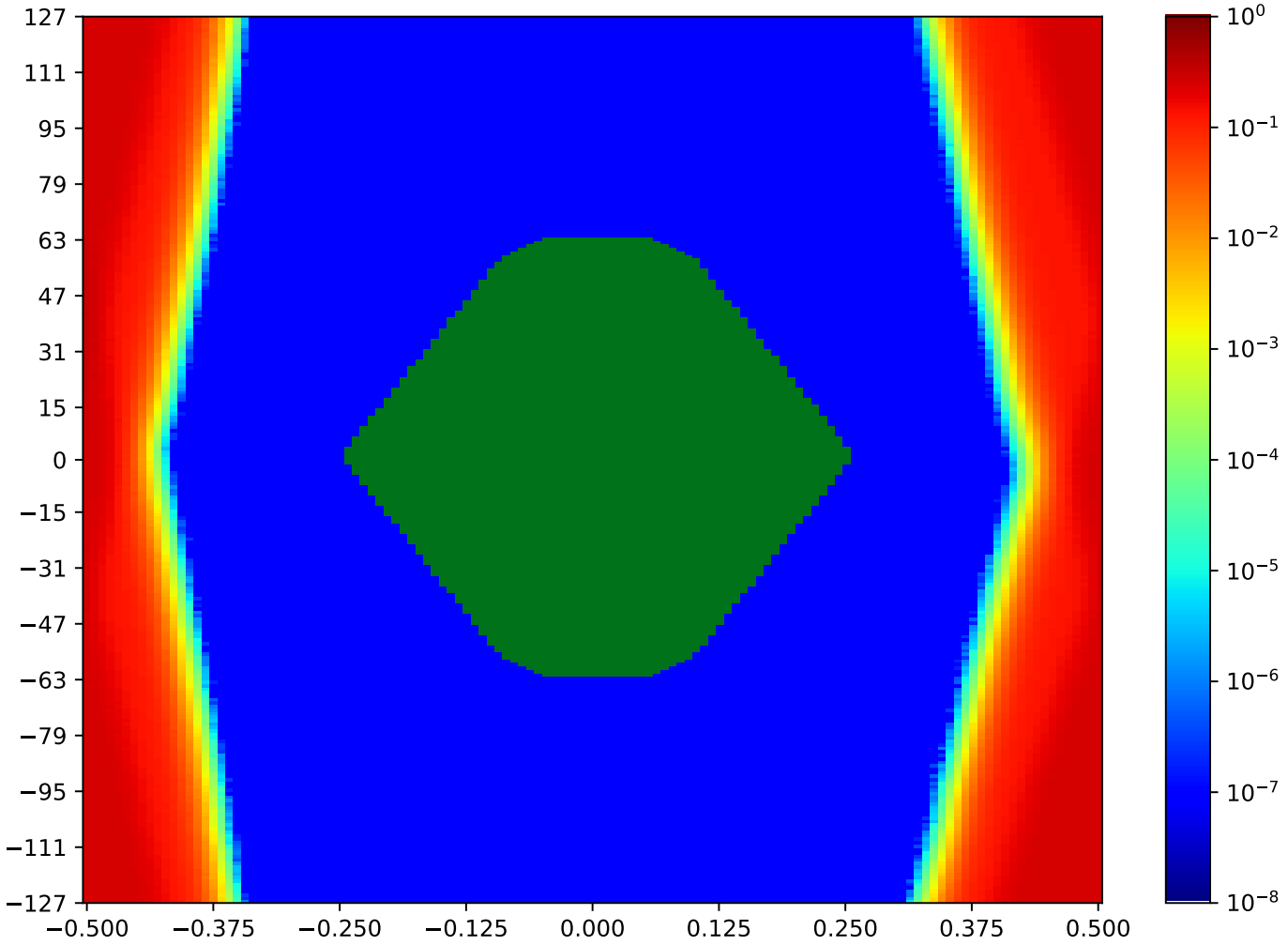


Figure 3.84: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.16 MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Table 3.77: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:14:17		2018-Sep-26 18:15:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25577	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

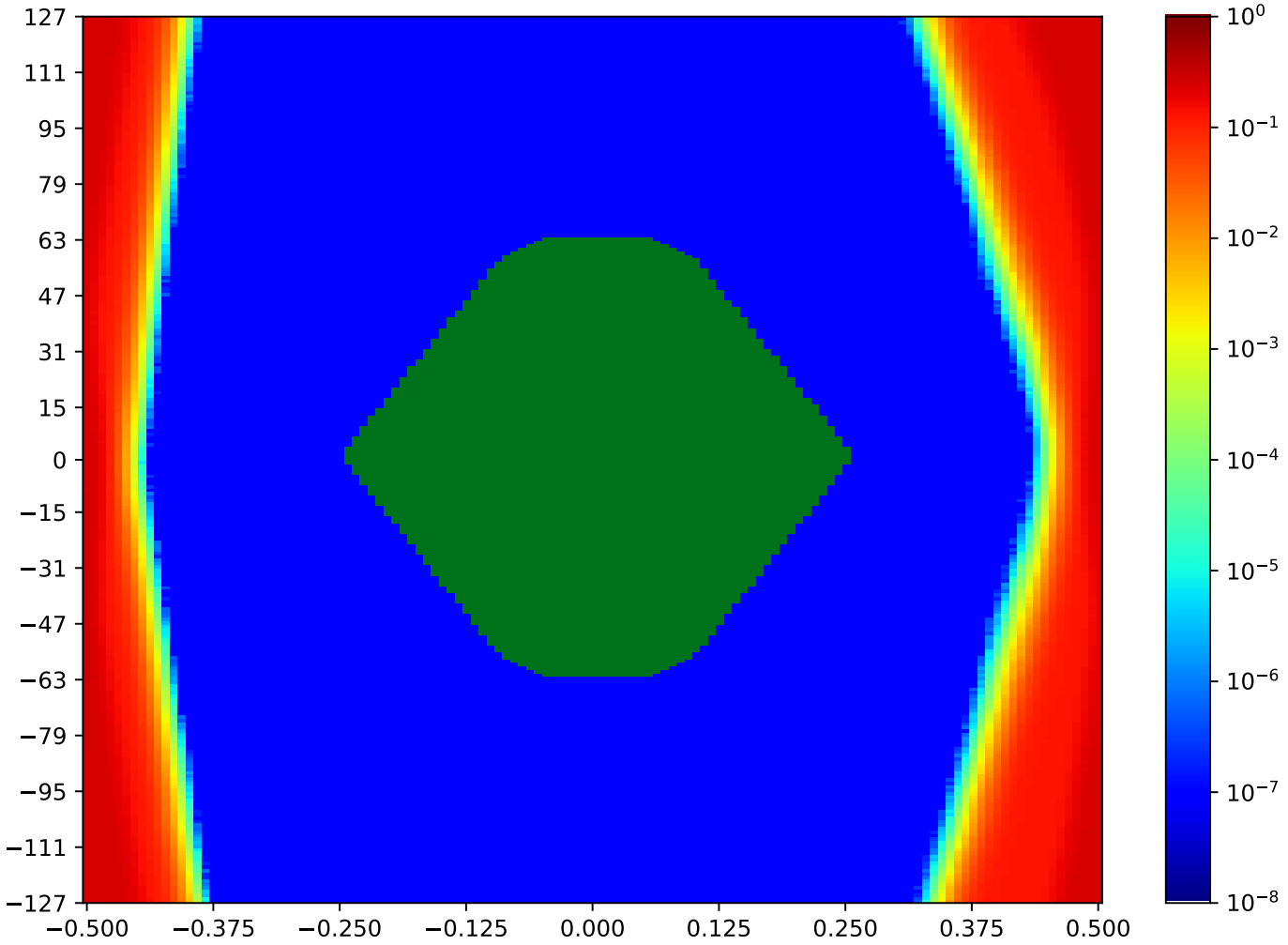


Figure 3.85: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.17 MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Table 3.78: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:15:30		2018-Sep-26 18:16:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25259	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

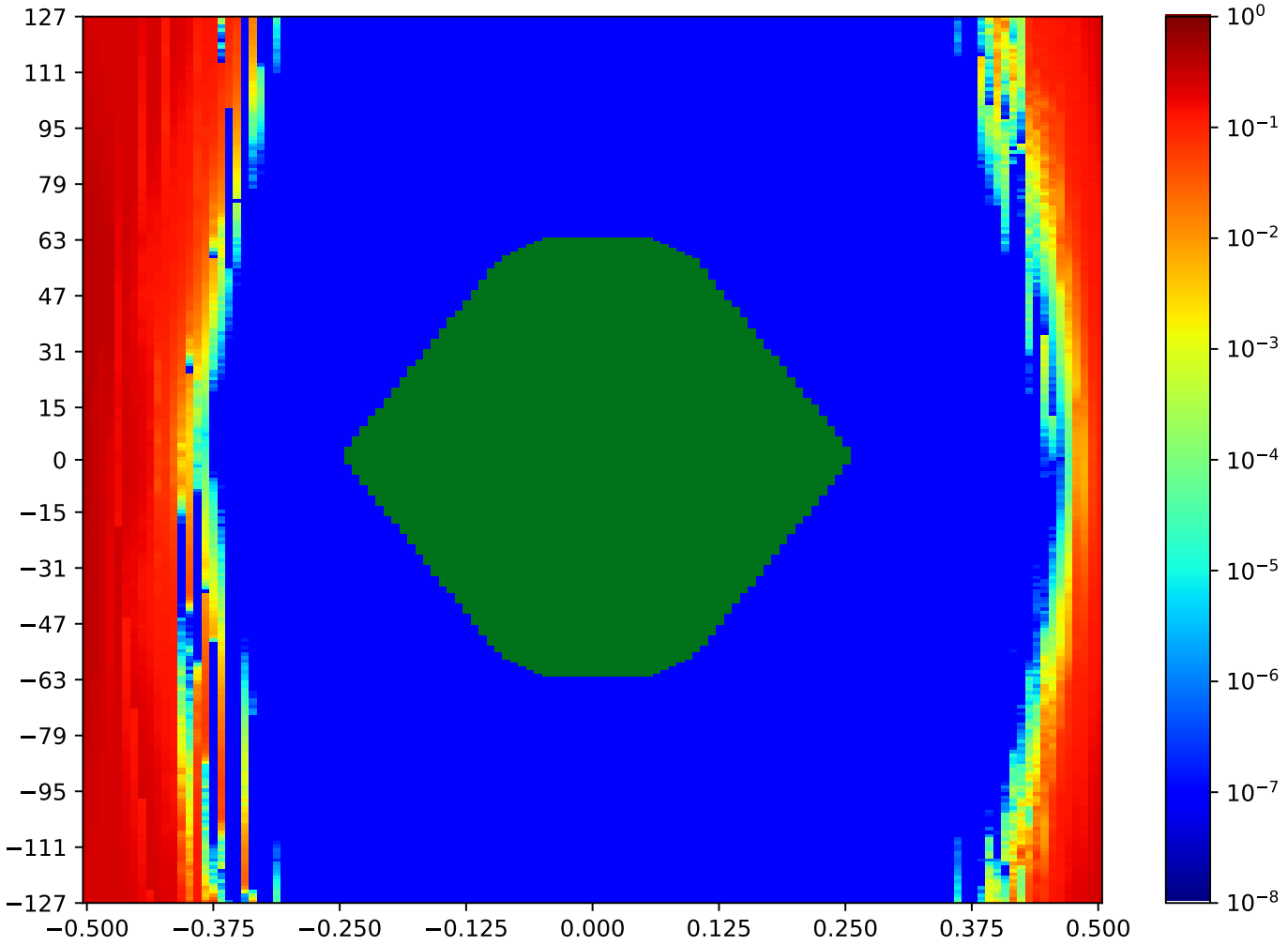


Figure 3.86: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.18 MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Table 3.79: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:16:43		2018-Sep-26 18:17:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23968	106	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

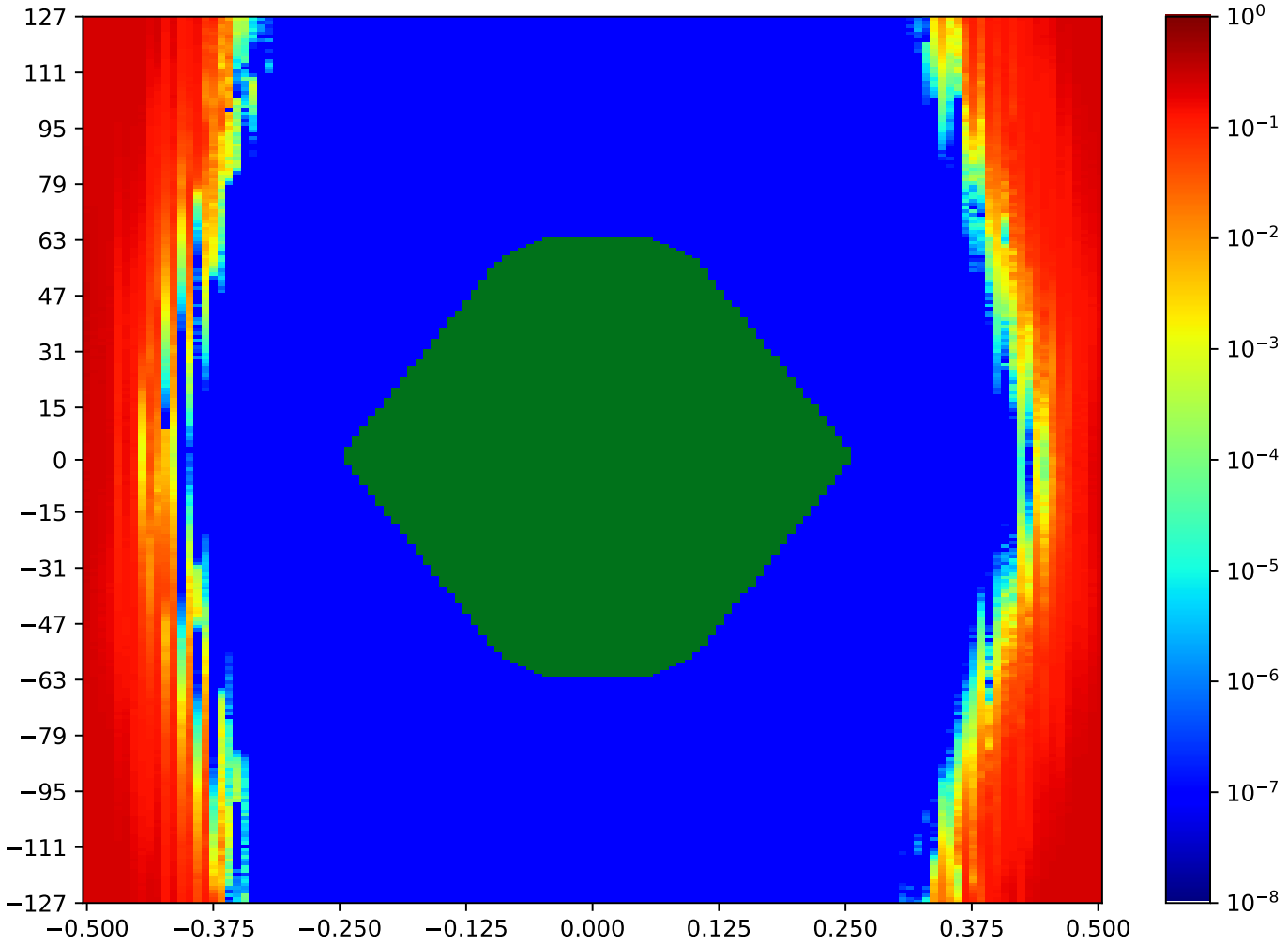


Figure 3.87: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.19 MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Table 3.80: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:17:54		2018-Sep-26 18:19:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26039	111	84.50%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

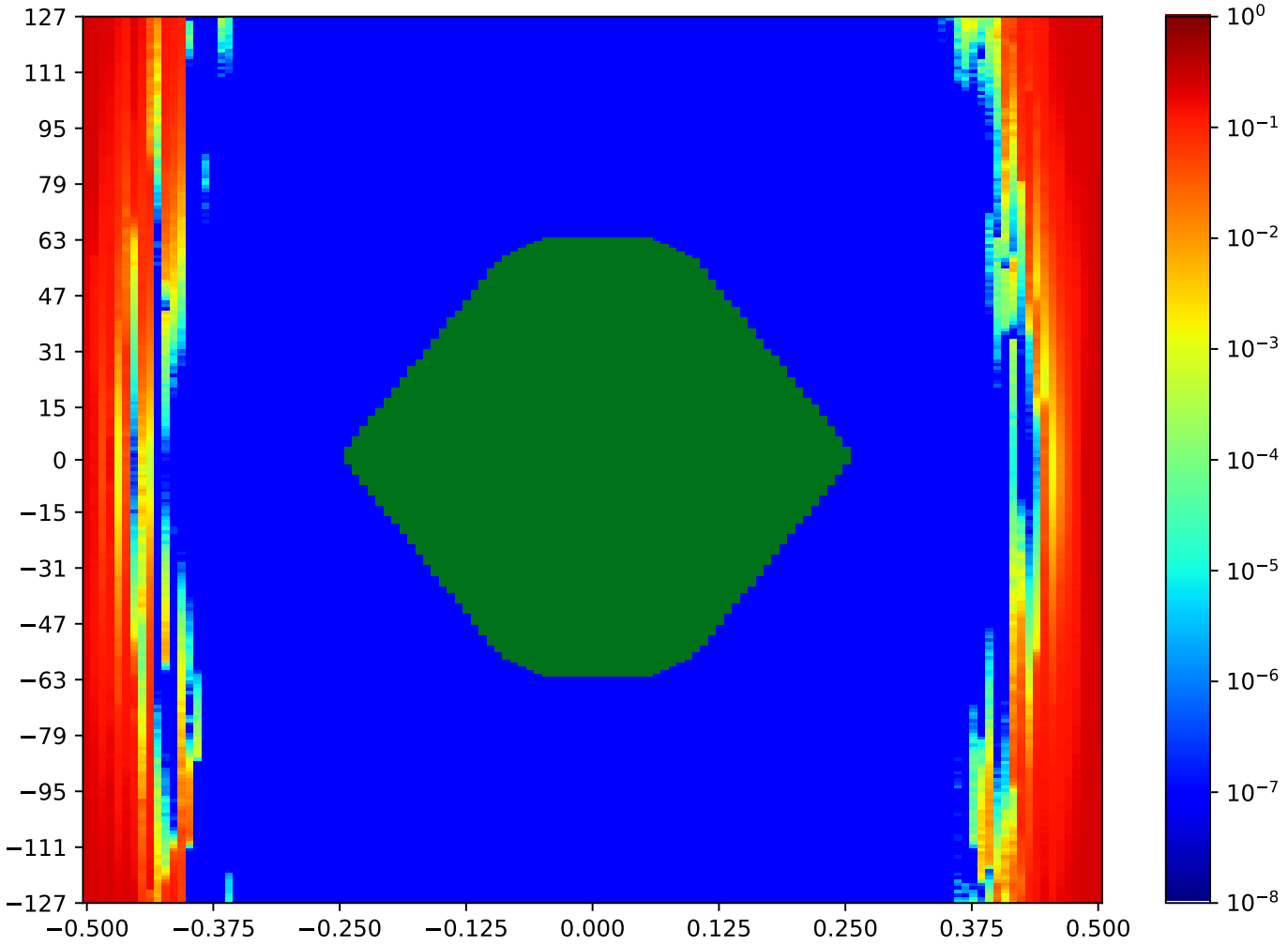


Figure 3.88: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.20 MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Table 3.81: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:19:08		2018-Sep-26 18:20:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25028	108	83.72%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

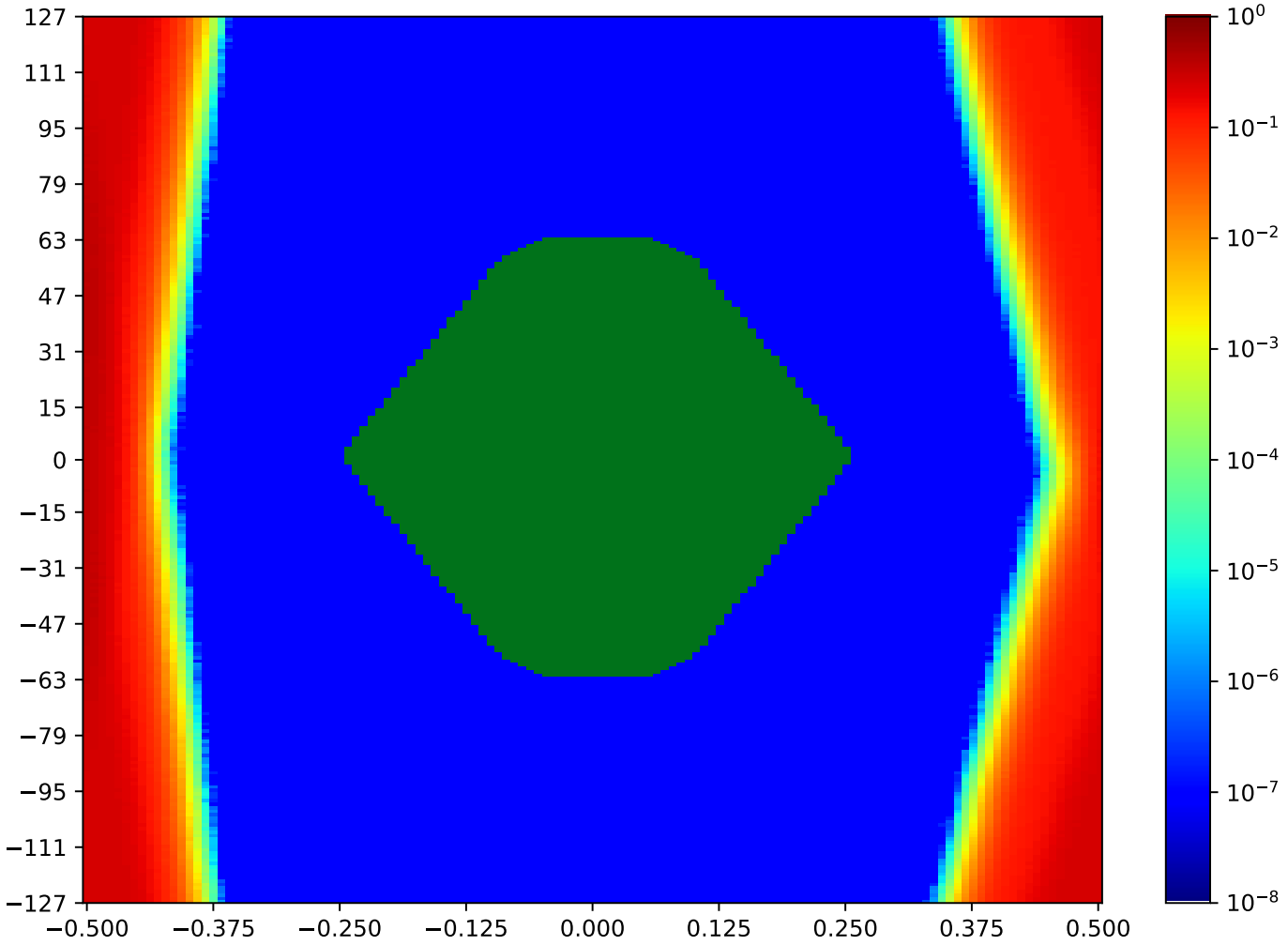


Figure 3.89: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.21 MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Table 3.82: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:20:21		2018-Sep-26 18:21:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24922	106	82.17%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

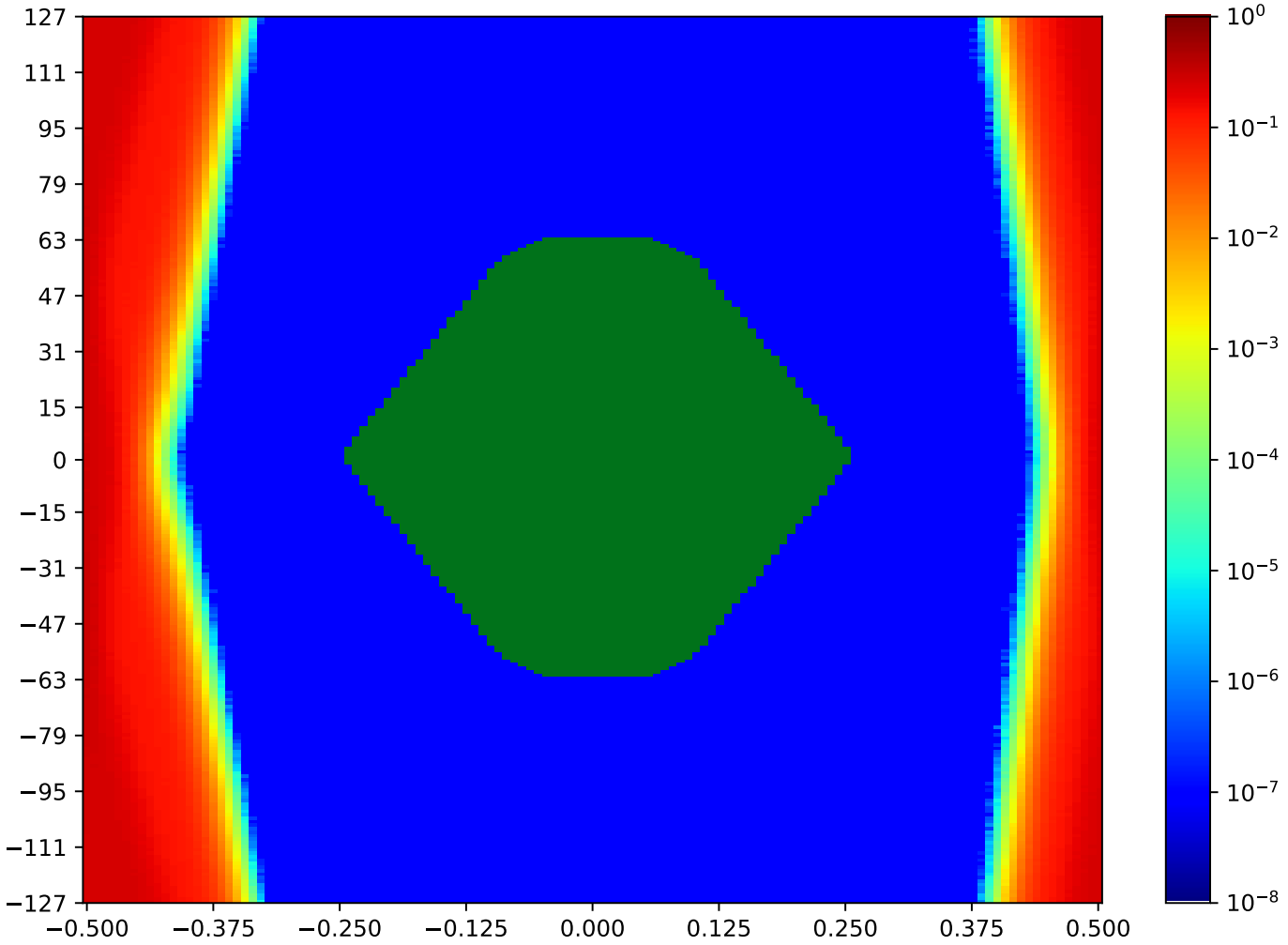


Figure 3.90: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.22 MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Table 3.83: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:21:33		2018-Sep-26 18:22:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24925	109	82.95%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

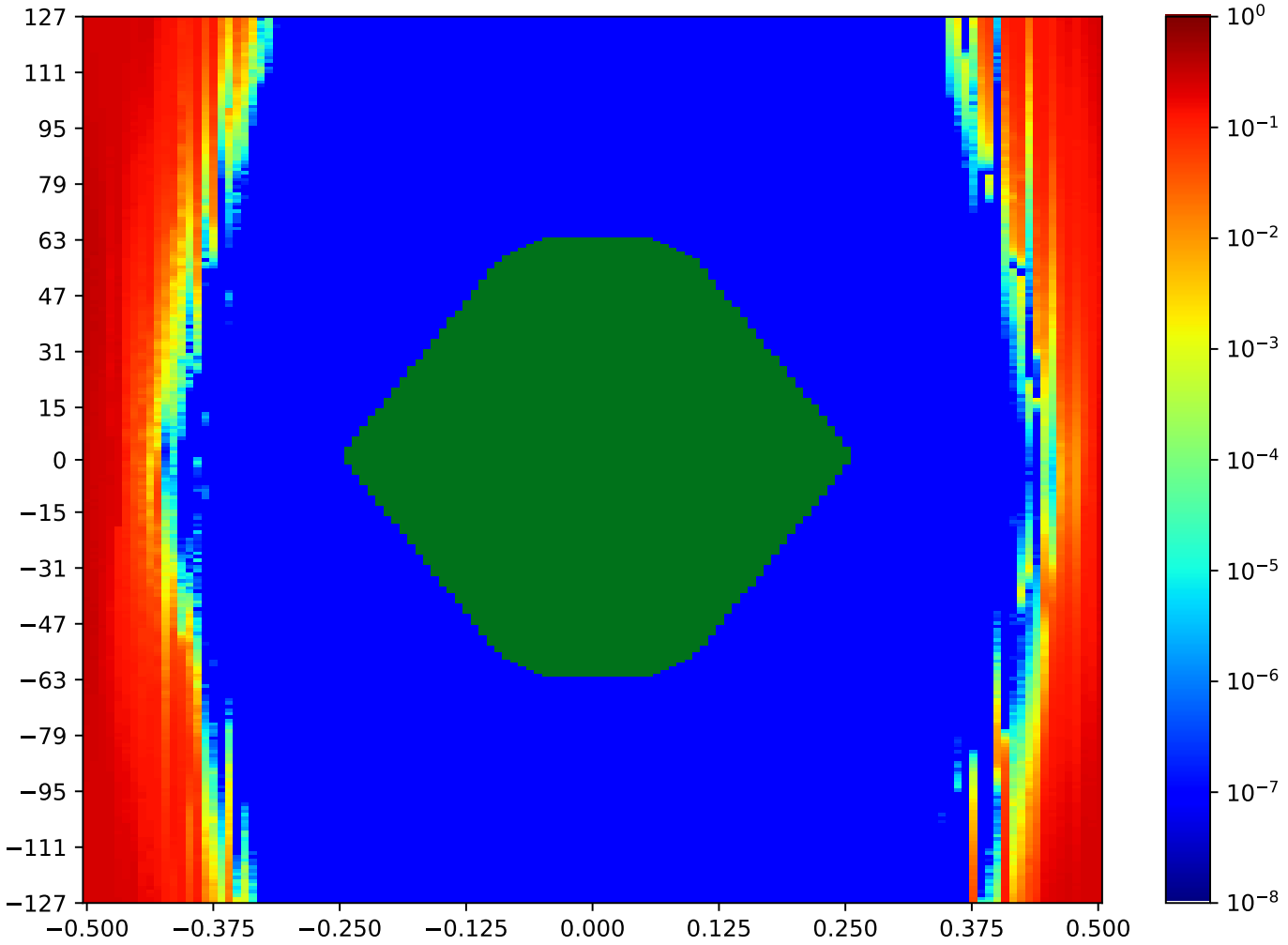


Figure 3.91: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.23 MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Table 3.84: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:22:45		2018-Sep-26 18:23:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23346	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

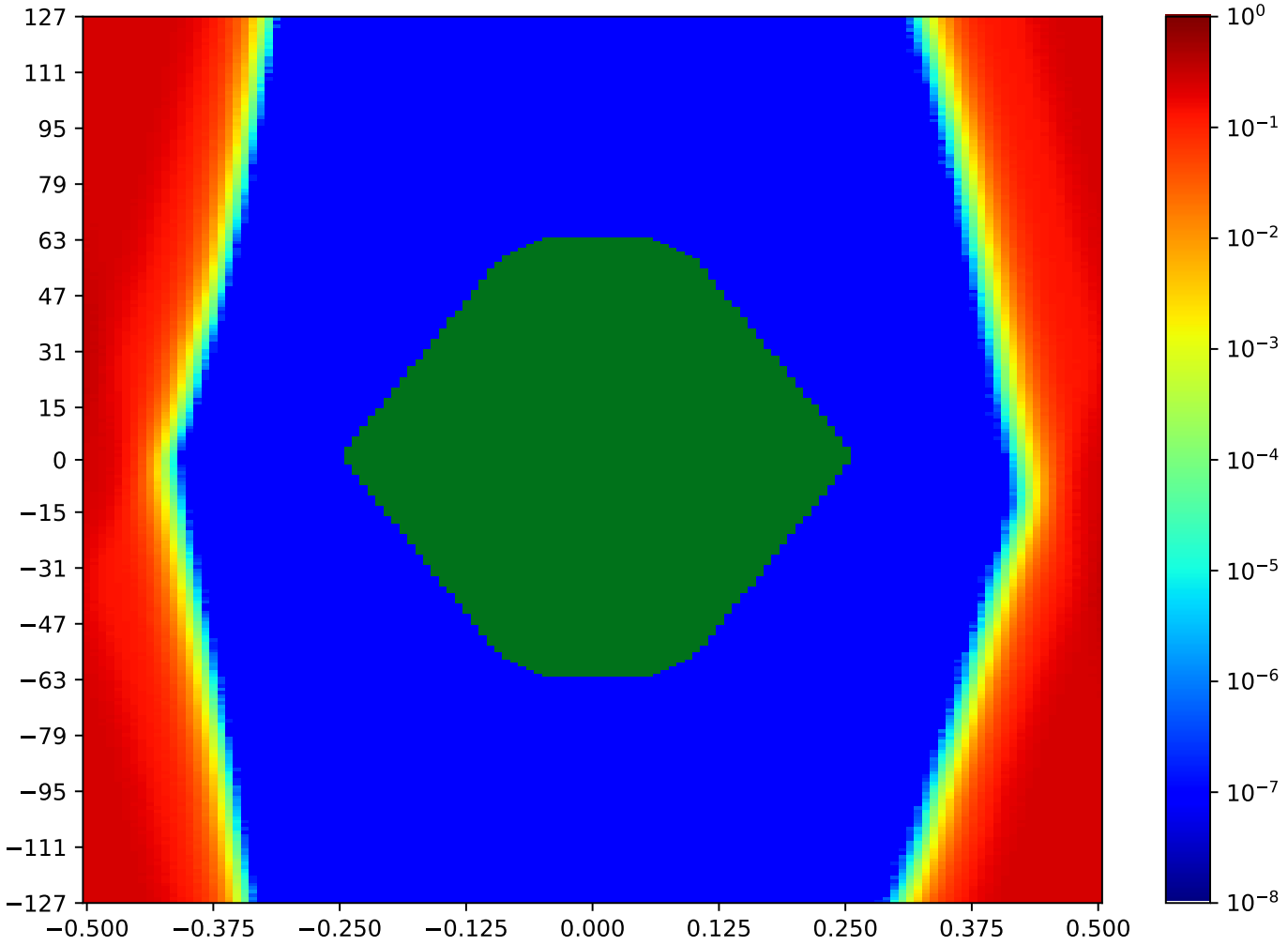


Figure 3.92: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.24 MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Table 3.85: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:23:55		2018-Sep-26 18:25:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24495	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

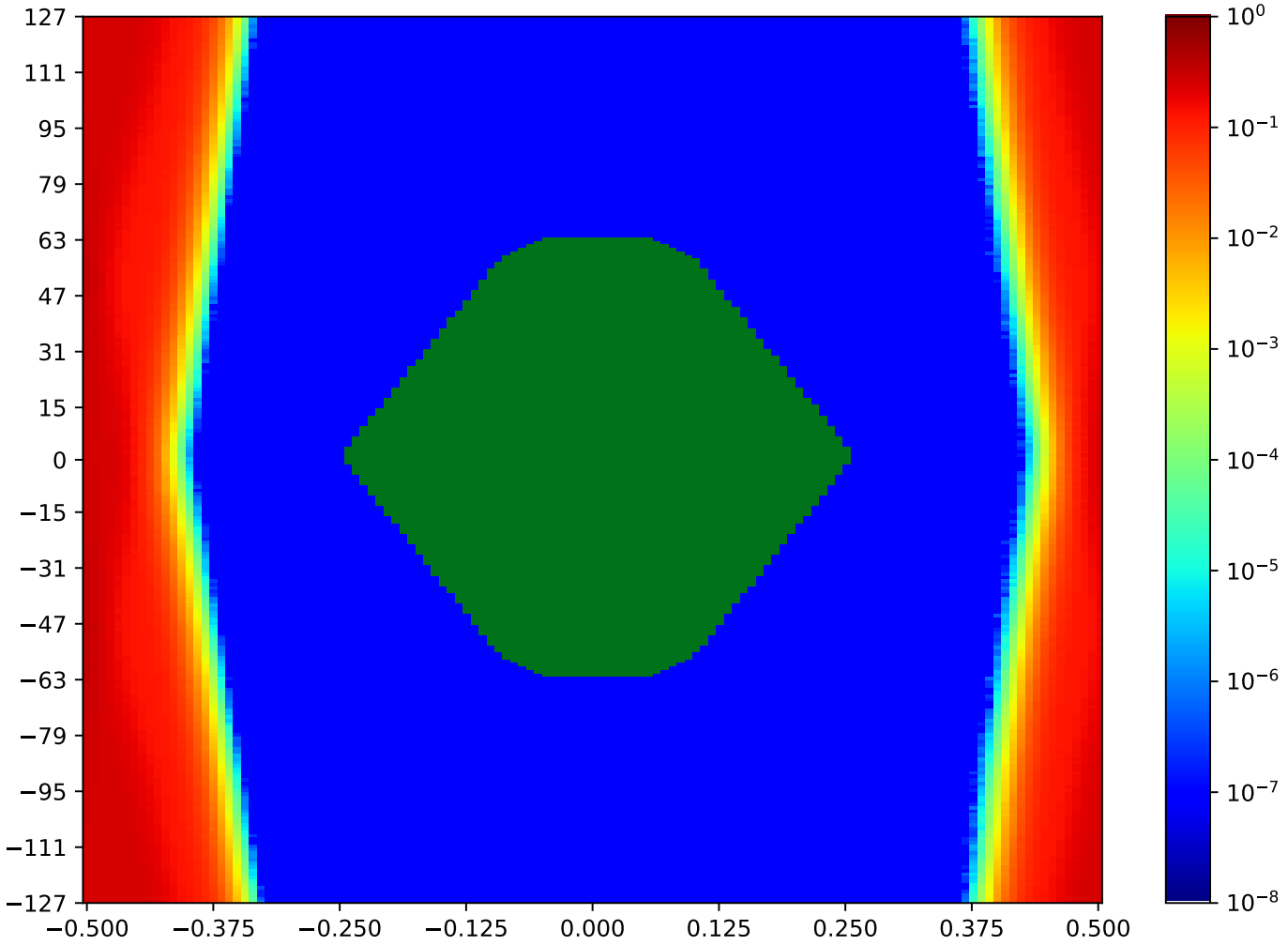


Figure 3.93: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.25 MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Table 3.86: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:25:07		2018-Sep-26 18:26:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25186	109	84.50%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

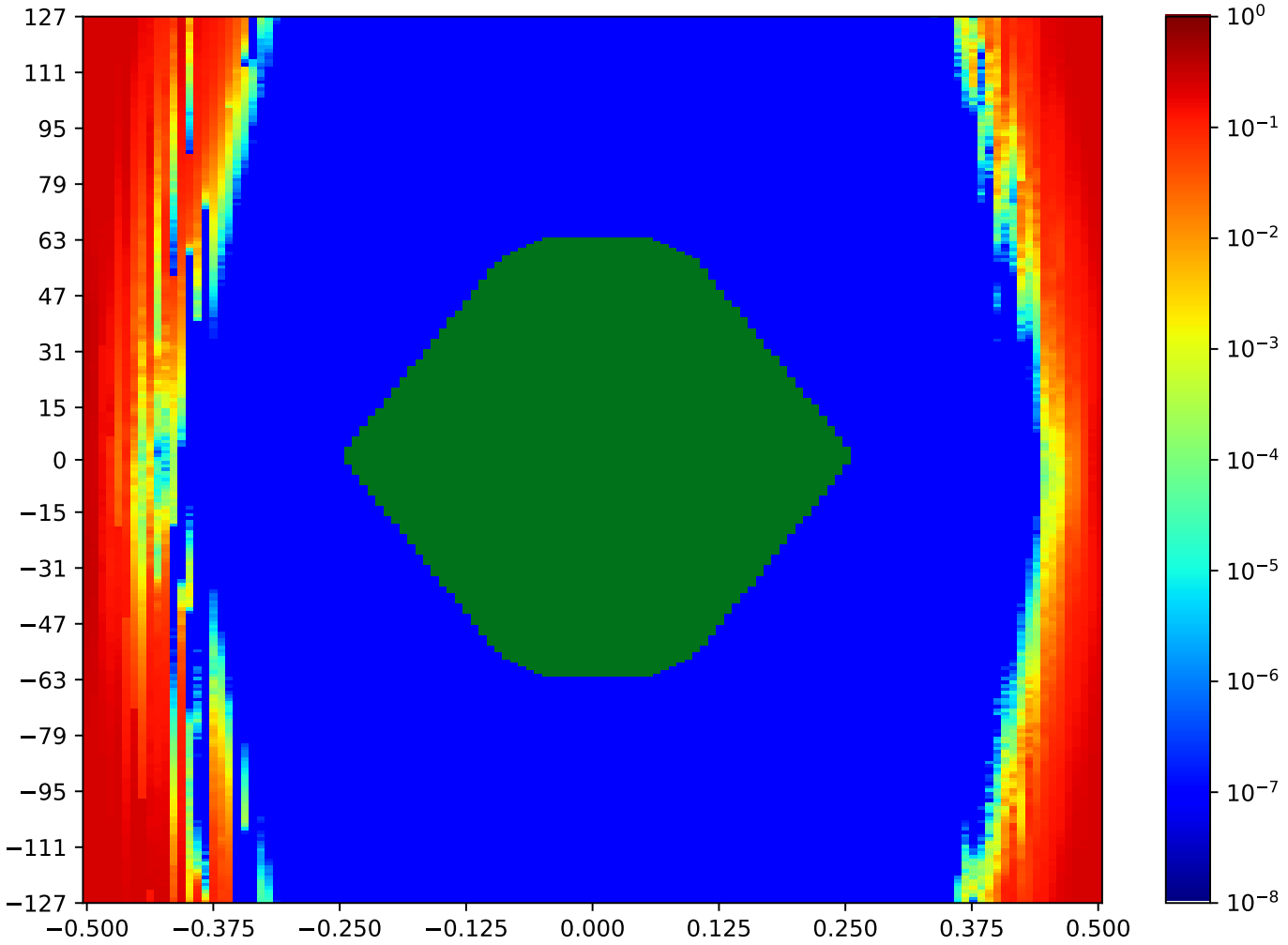


Figure 3.94: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.26 MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Table 3.87: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:26:19		2018-Sep-26 18:27:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25548	111	86.05%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

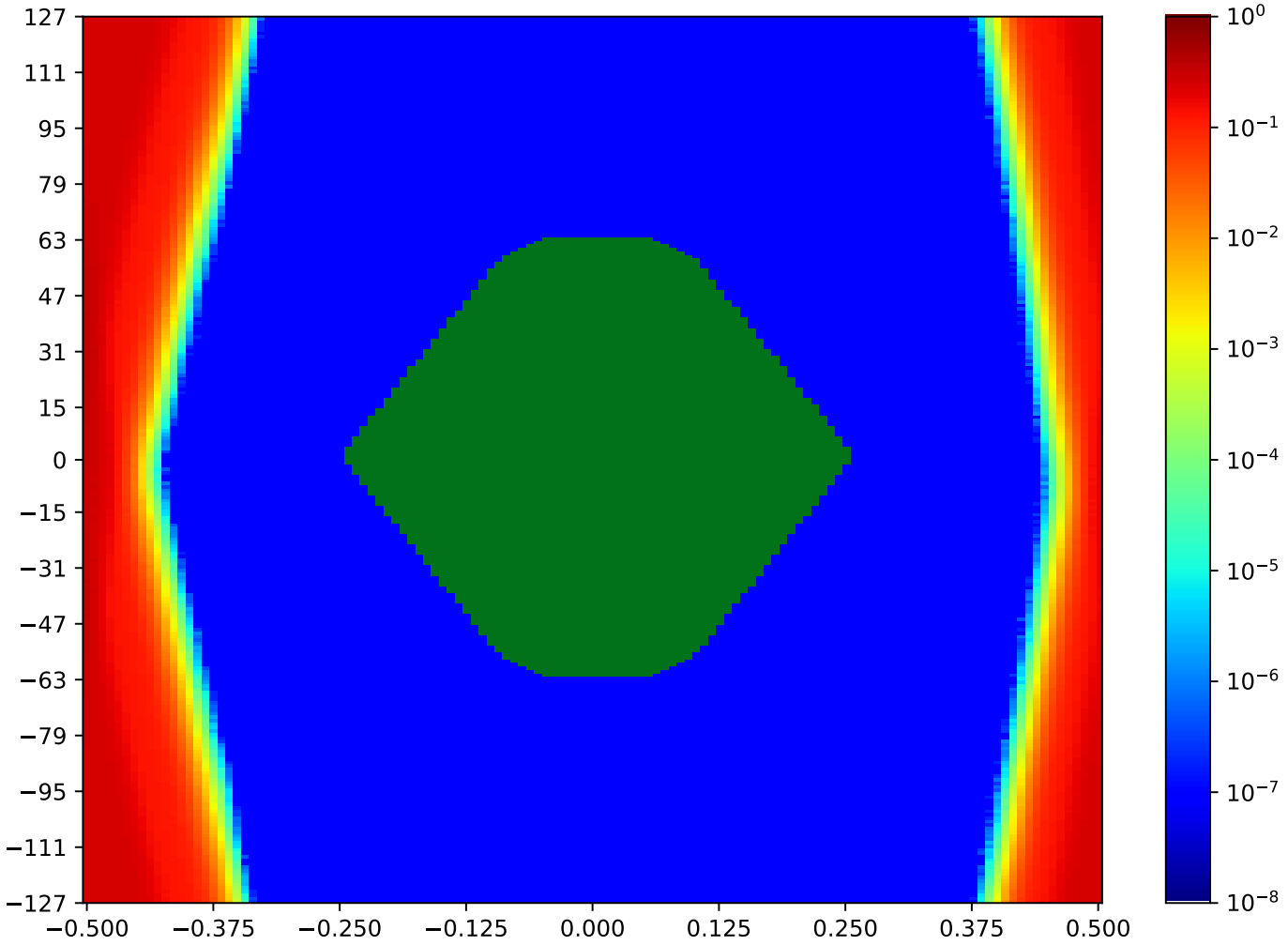


Figure 3.95: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.27 MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Table 3.88: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:27:33		2018-Sep-26 18:28:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24290	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

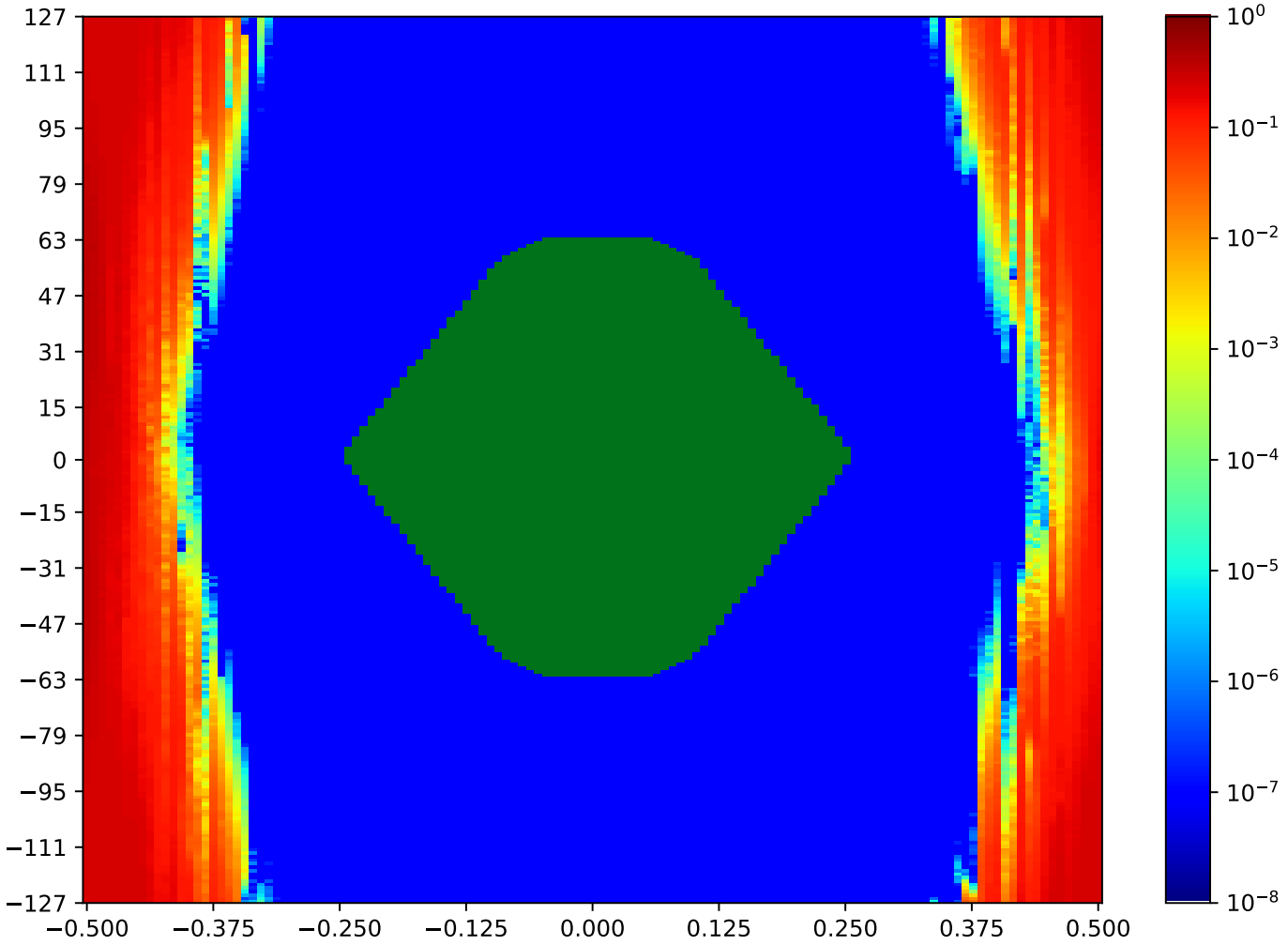


Figure 3.96: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.8.28 MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Table 3.89: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:28:44		2018-Sep-26 18:29:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25253	111	86.05%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

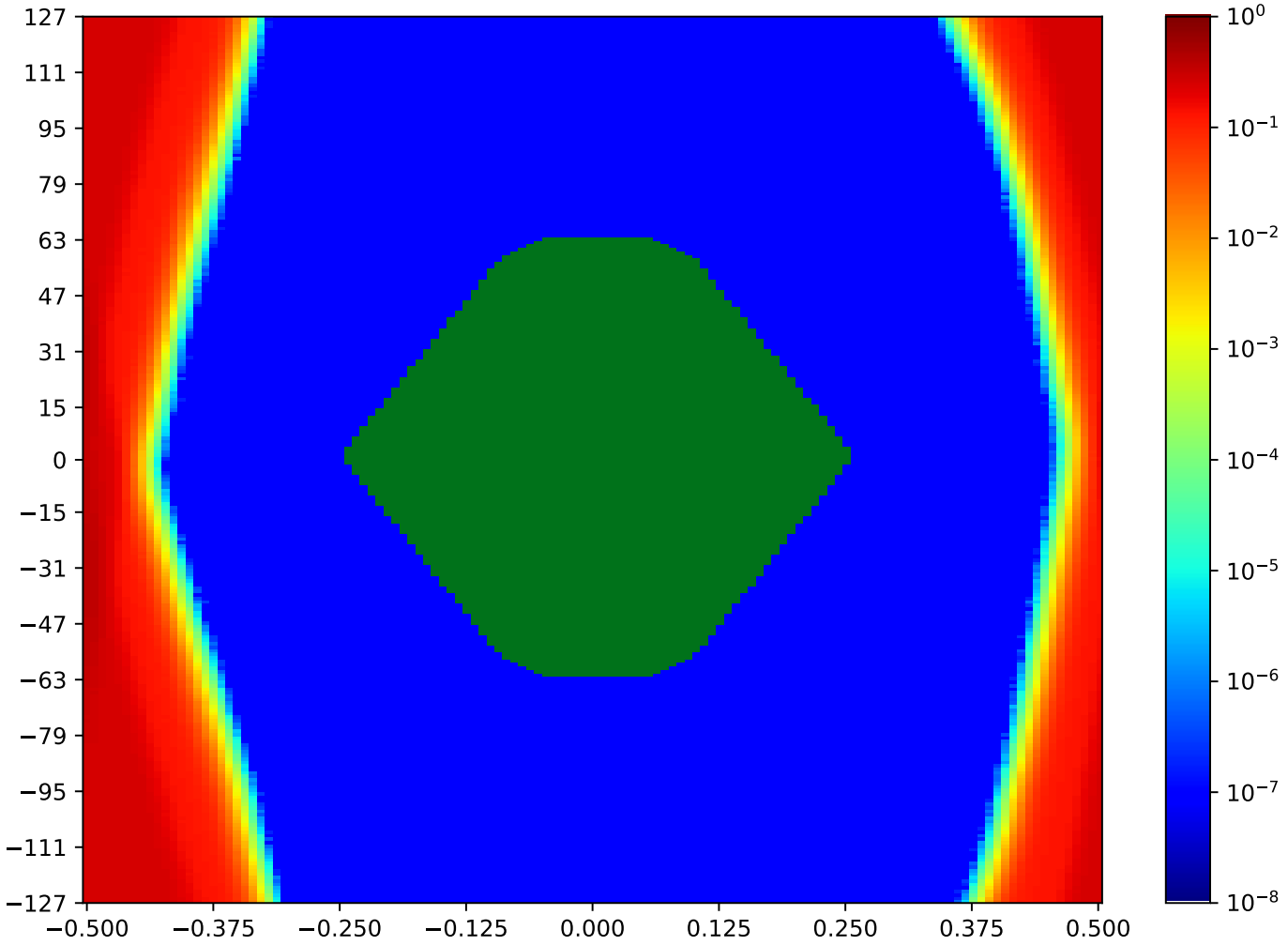


Figure 3.97: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9 MSP_C TRP On board links

A cross-reference to Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.127.

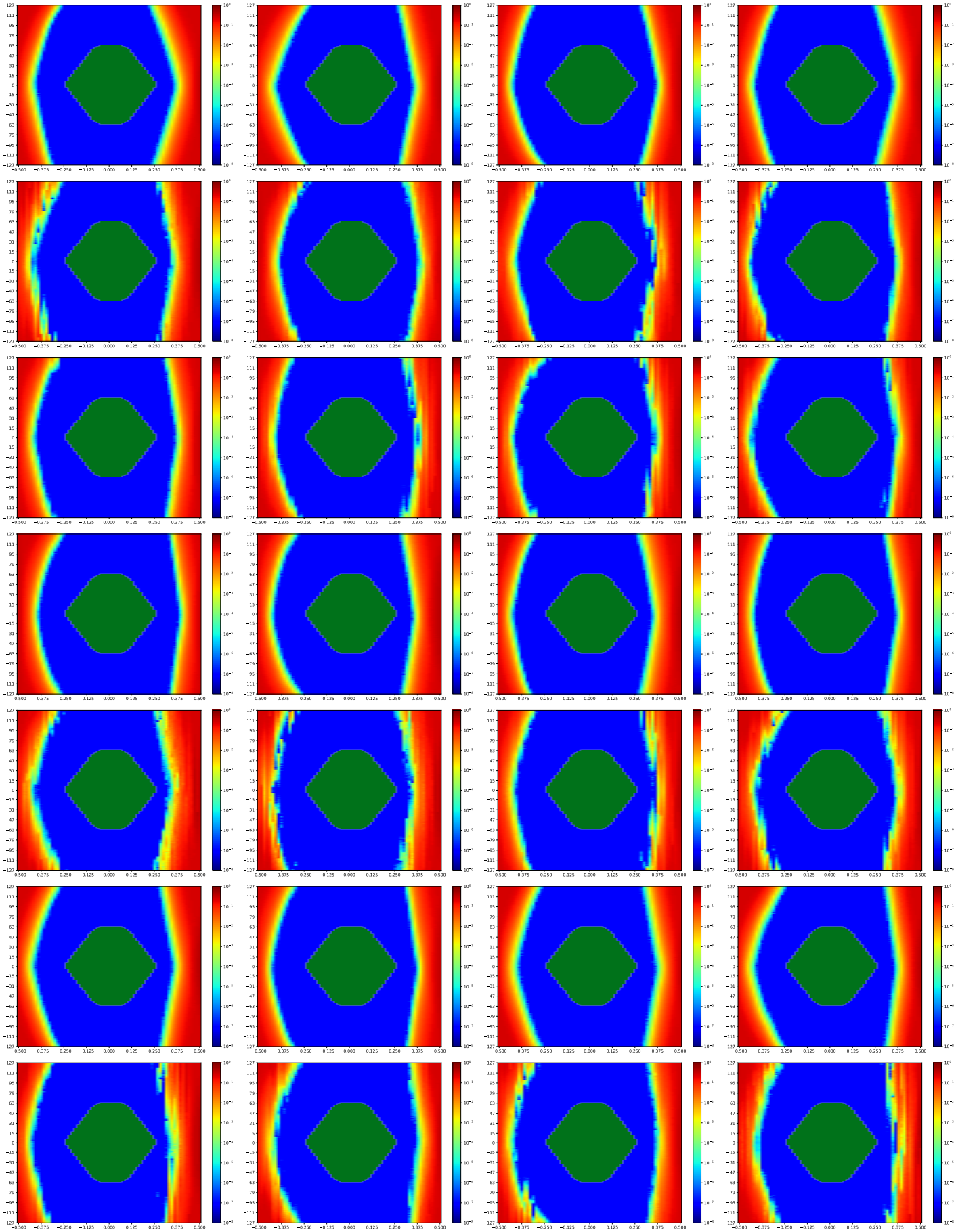


Figure 3.98: MSP_C TRP On board links

3.9.1 MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Table 3.90: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:29:56		2018-Sep-26 18:30:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10292	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

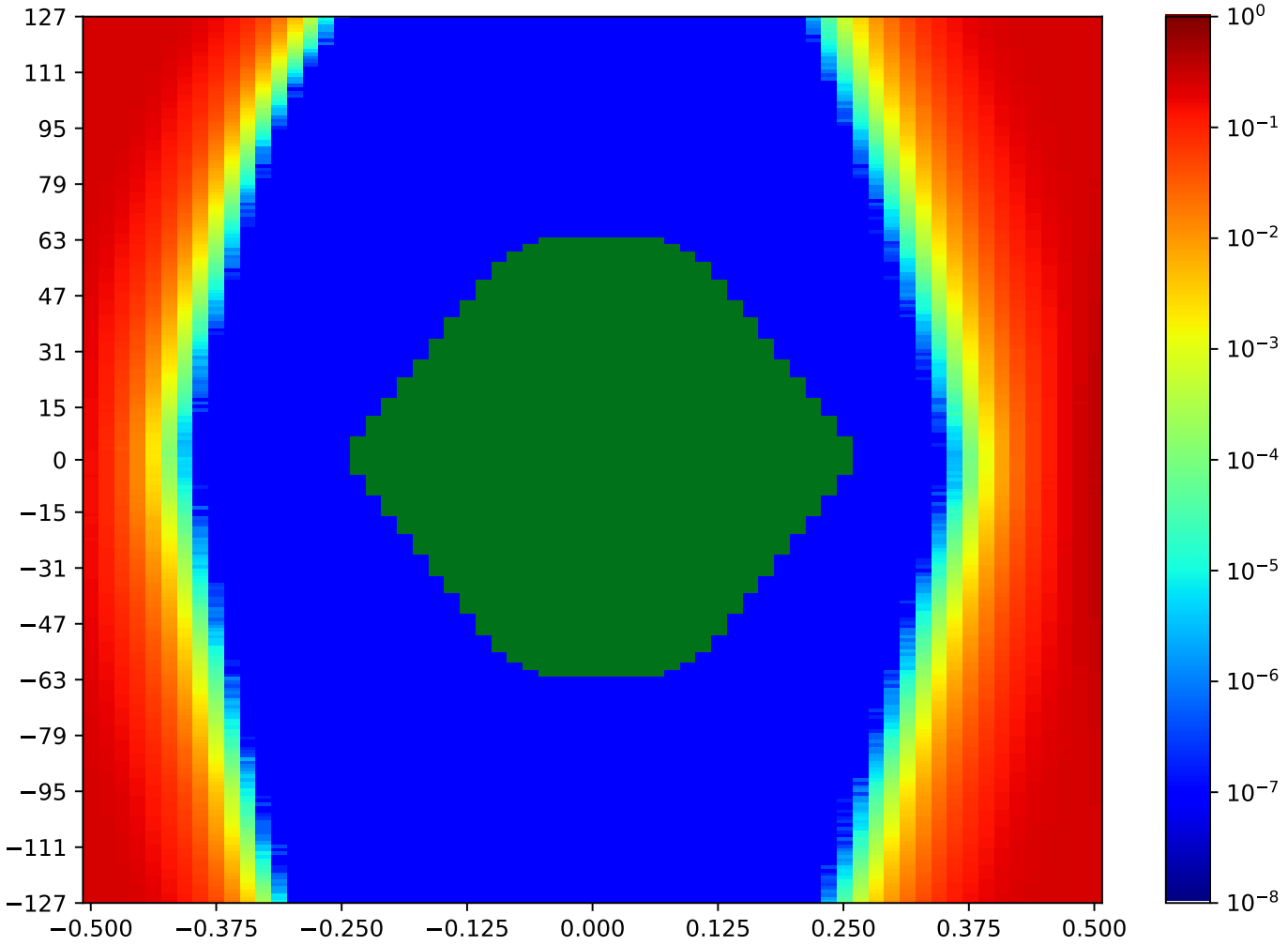


Figure 3.99: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.2 MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Table 3.91: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:30:34		2018-Sep-26 18:31:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10005	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

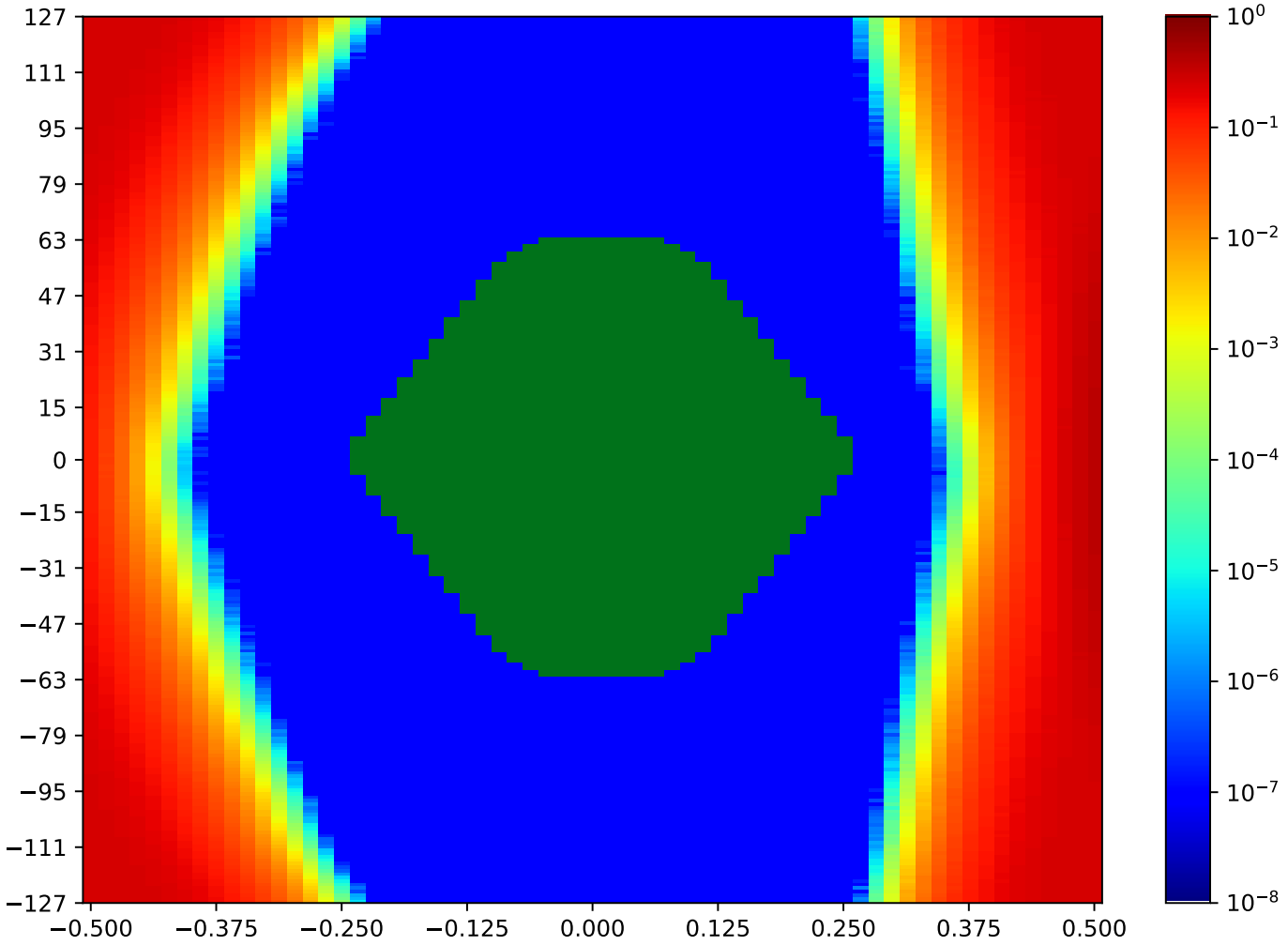


Figure 3.100: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.3 MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Table 3.92: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:31:10		2018-Sep-26 18:31:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10876	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

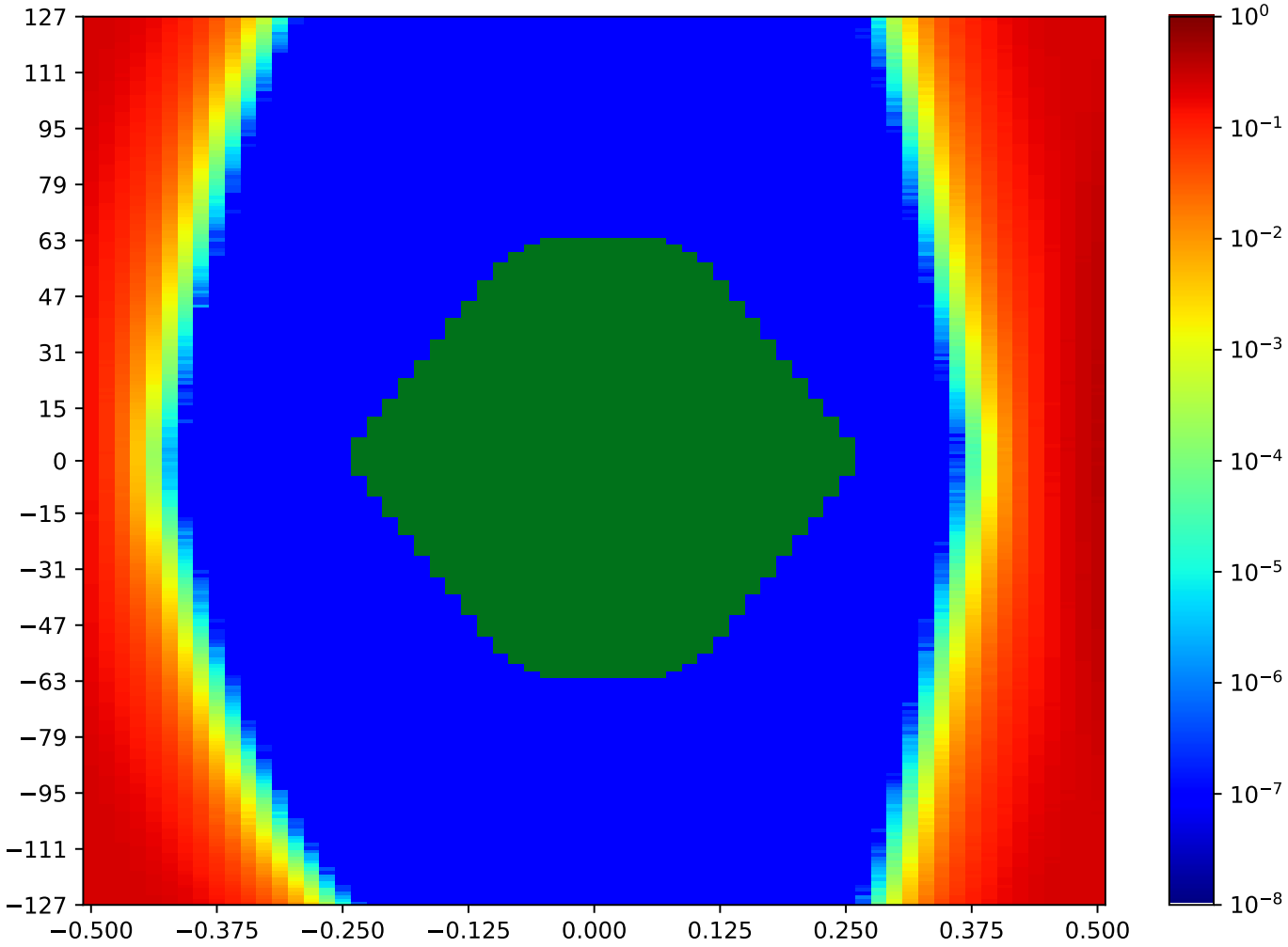


Figure 3.101: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.4 MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Table 3.93: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:31:47		2018-Sep-26 18:32:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10389	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

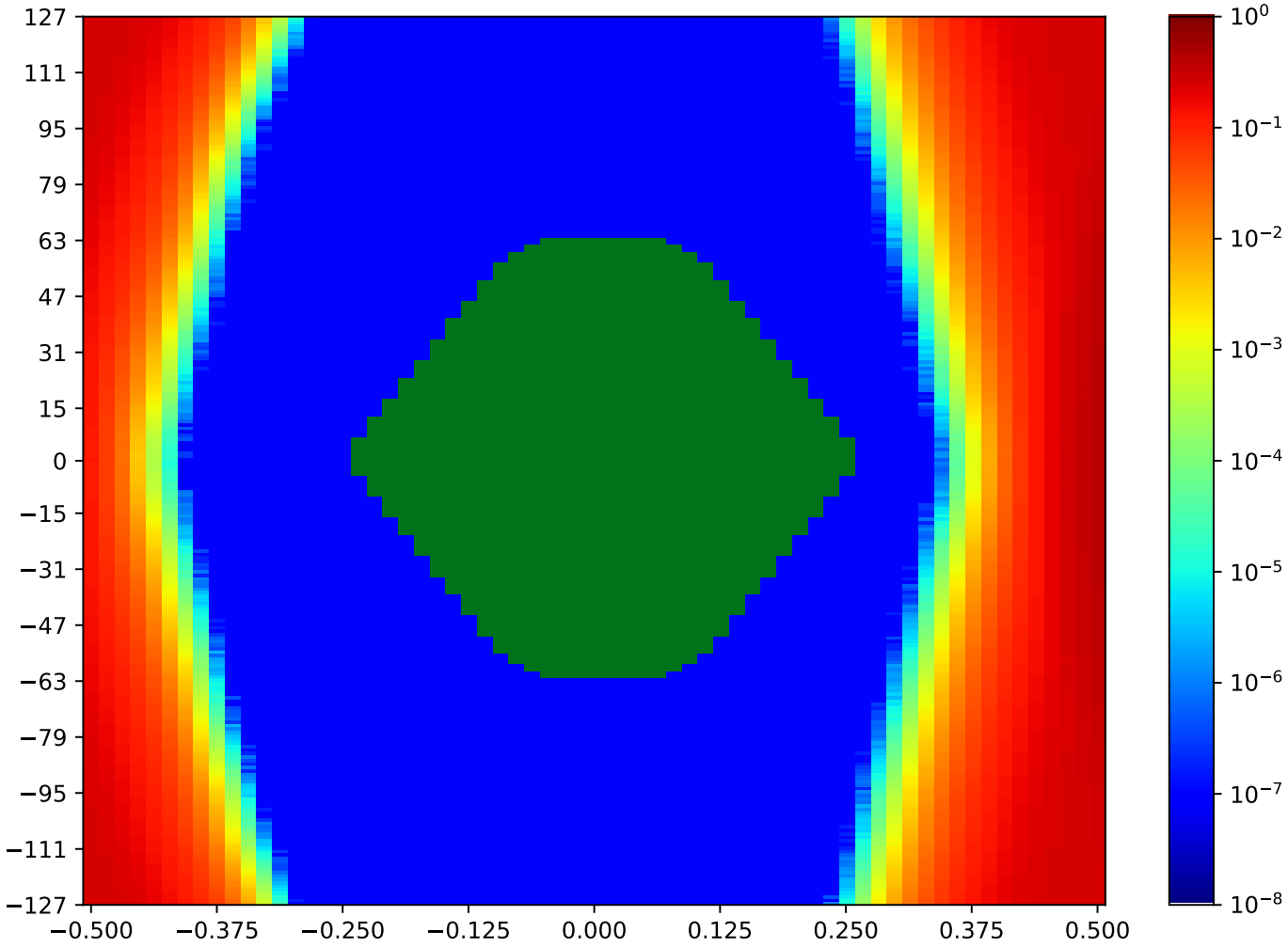


Figure 3.102: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.5 MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Table 3.94: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:32:25		2018-Sep-26 18:33:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10376	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

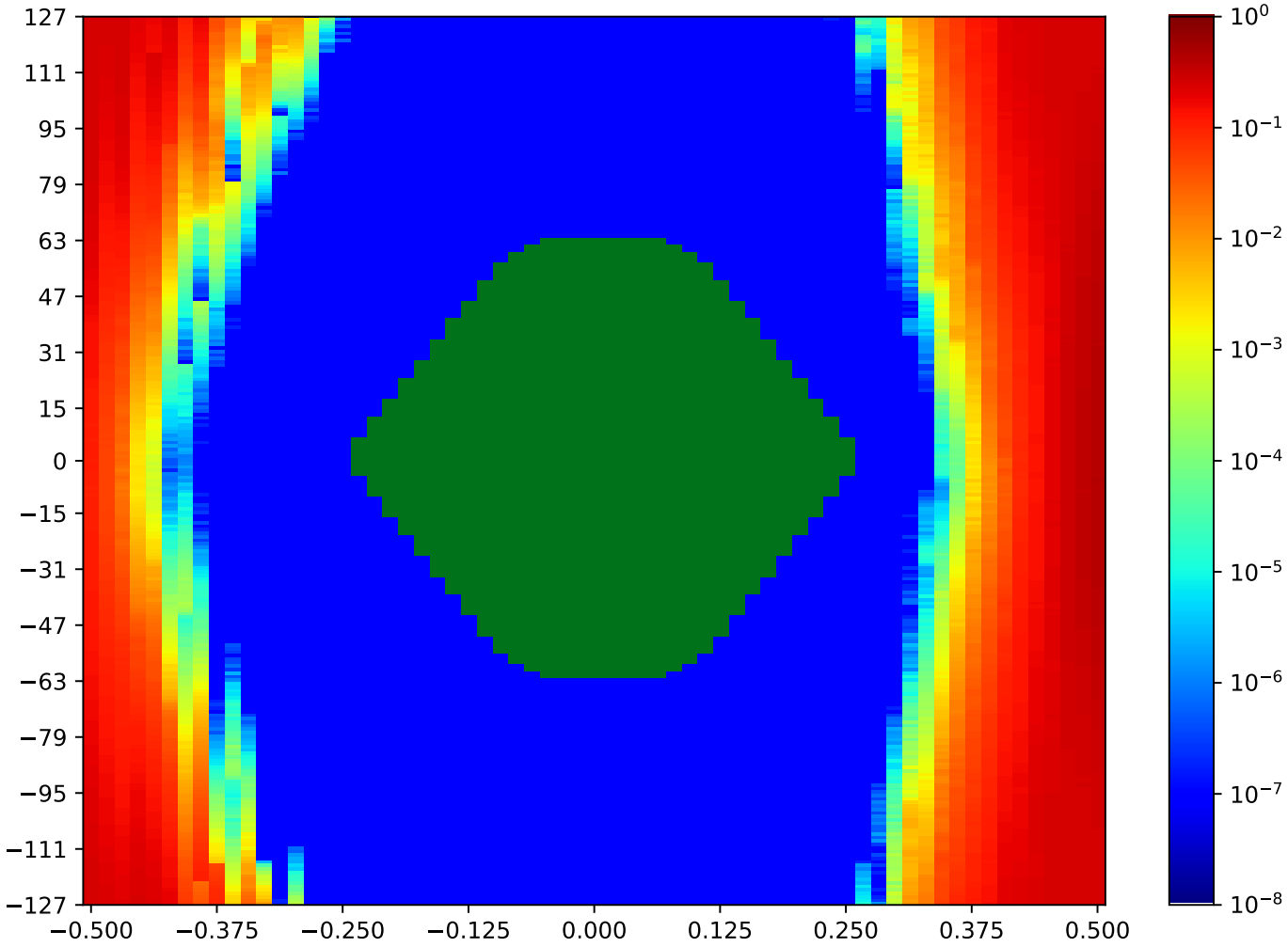


Figure 3.103: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.6 MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Table 3.95: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:33:02		2018-Sep-26 18:33:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10708	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

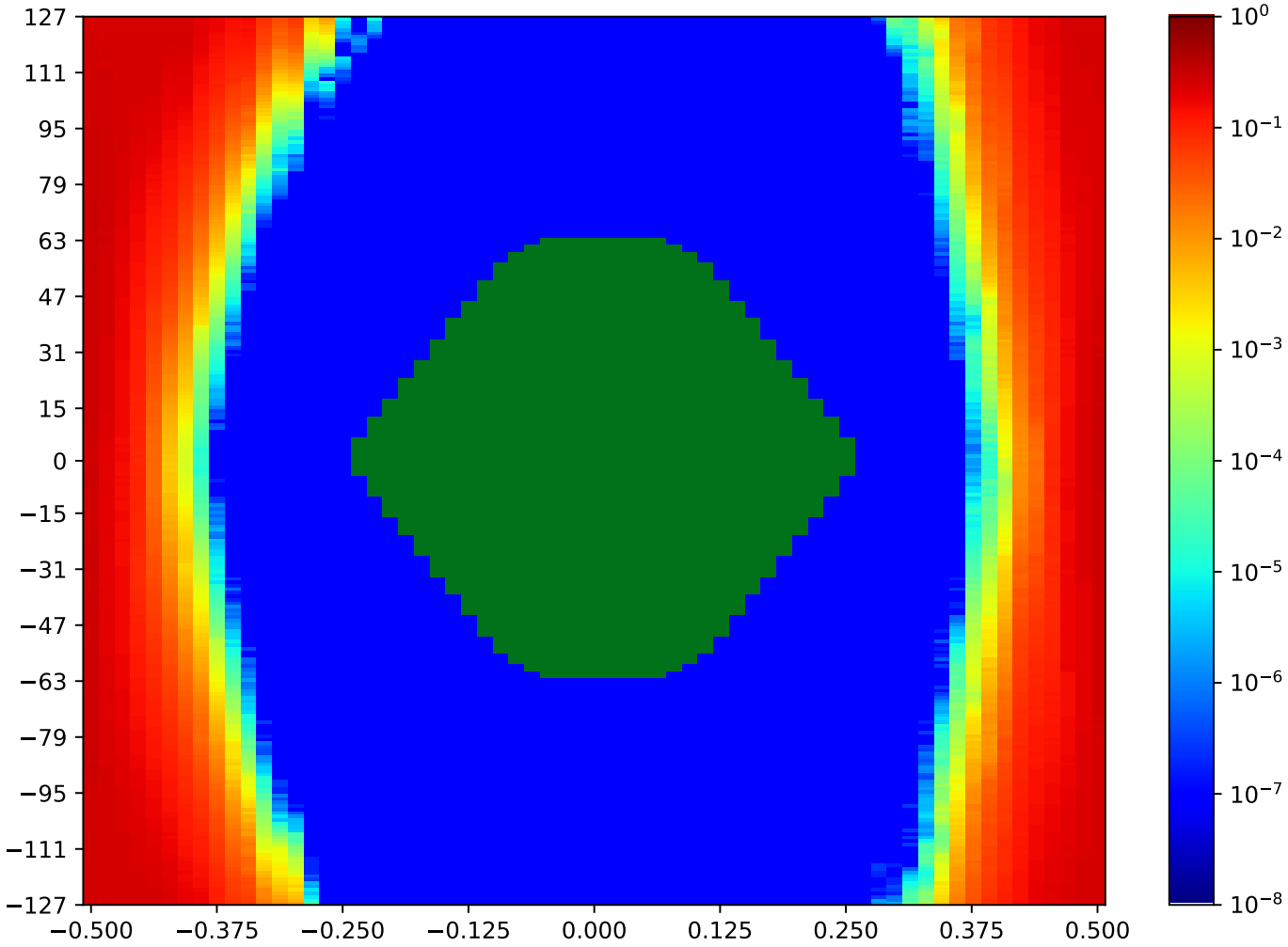


Figure 3.104: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.7 MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Table 3.96: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:33:40		2018-Sep-26 18:34:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10391	48	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

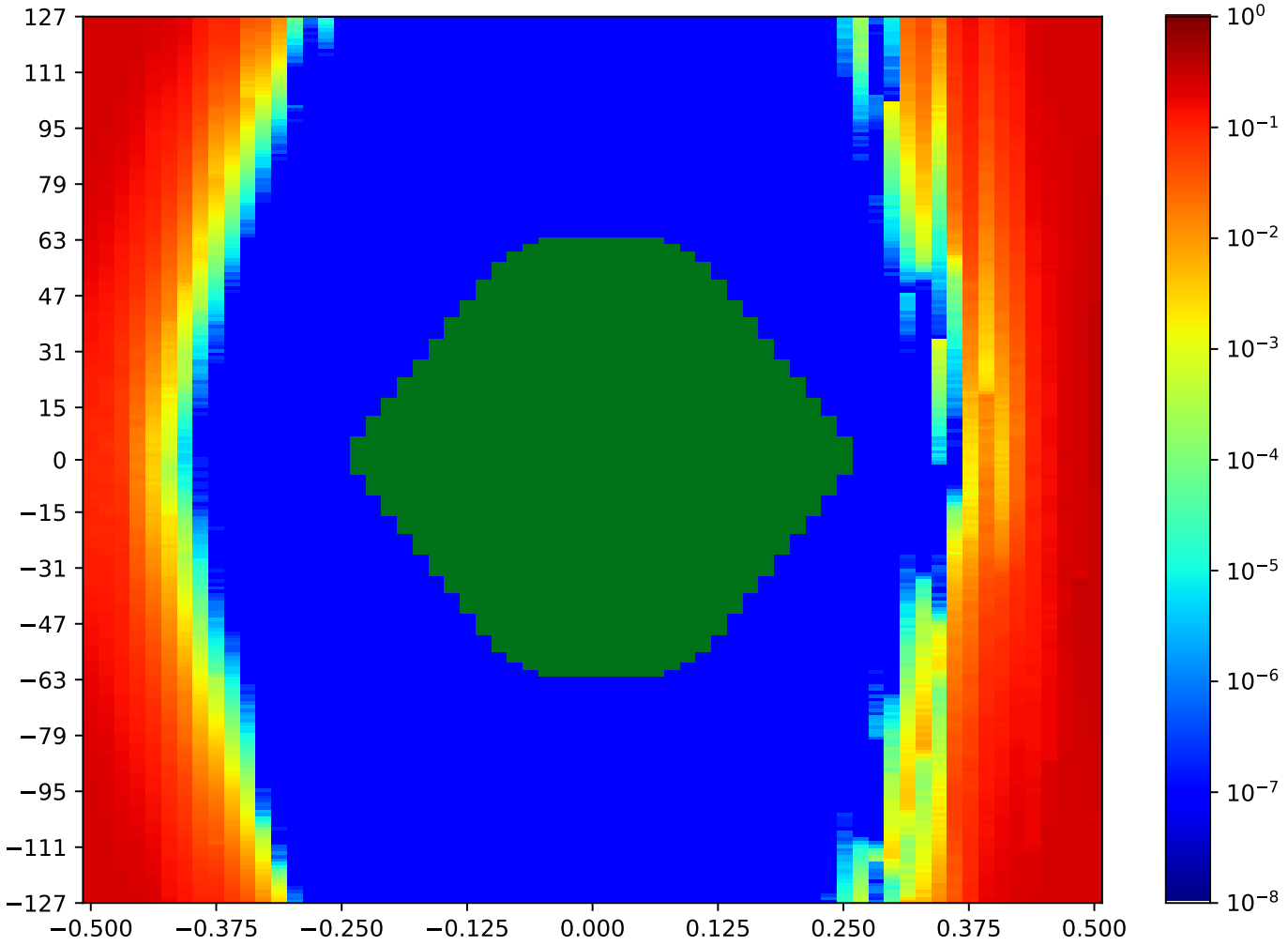


Figure 3.105: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.8 MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Table 3.97: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:34:17		2018-Sep-26 18:34:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11218	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

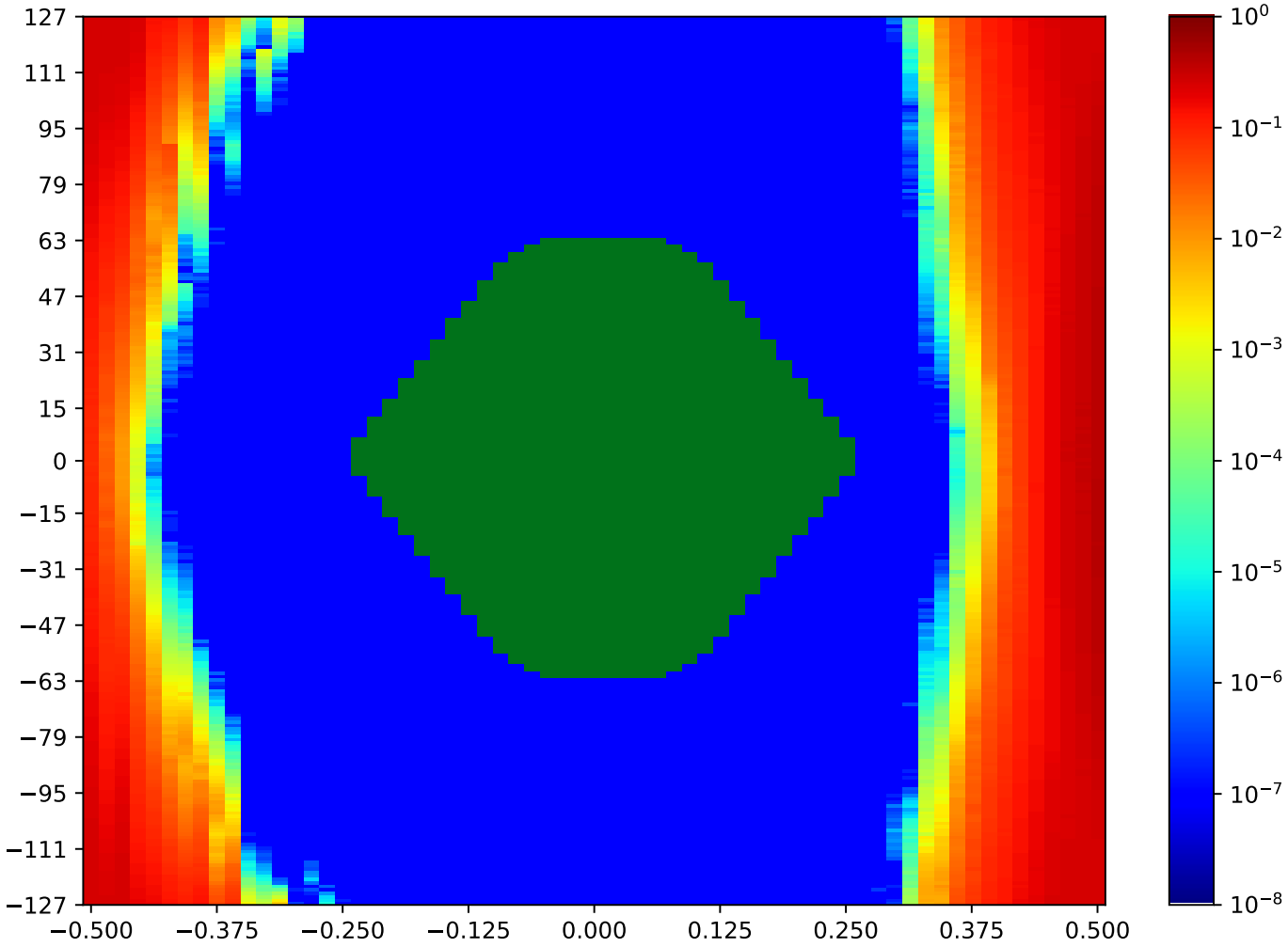


Figure 3.106: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.9 MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Table 3.98: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:34:54		2018-Sep-26 18:35:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10998	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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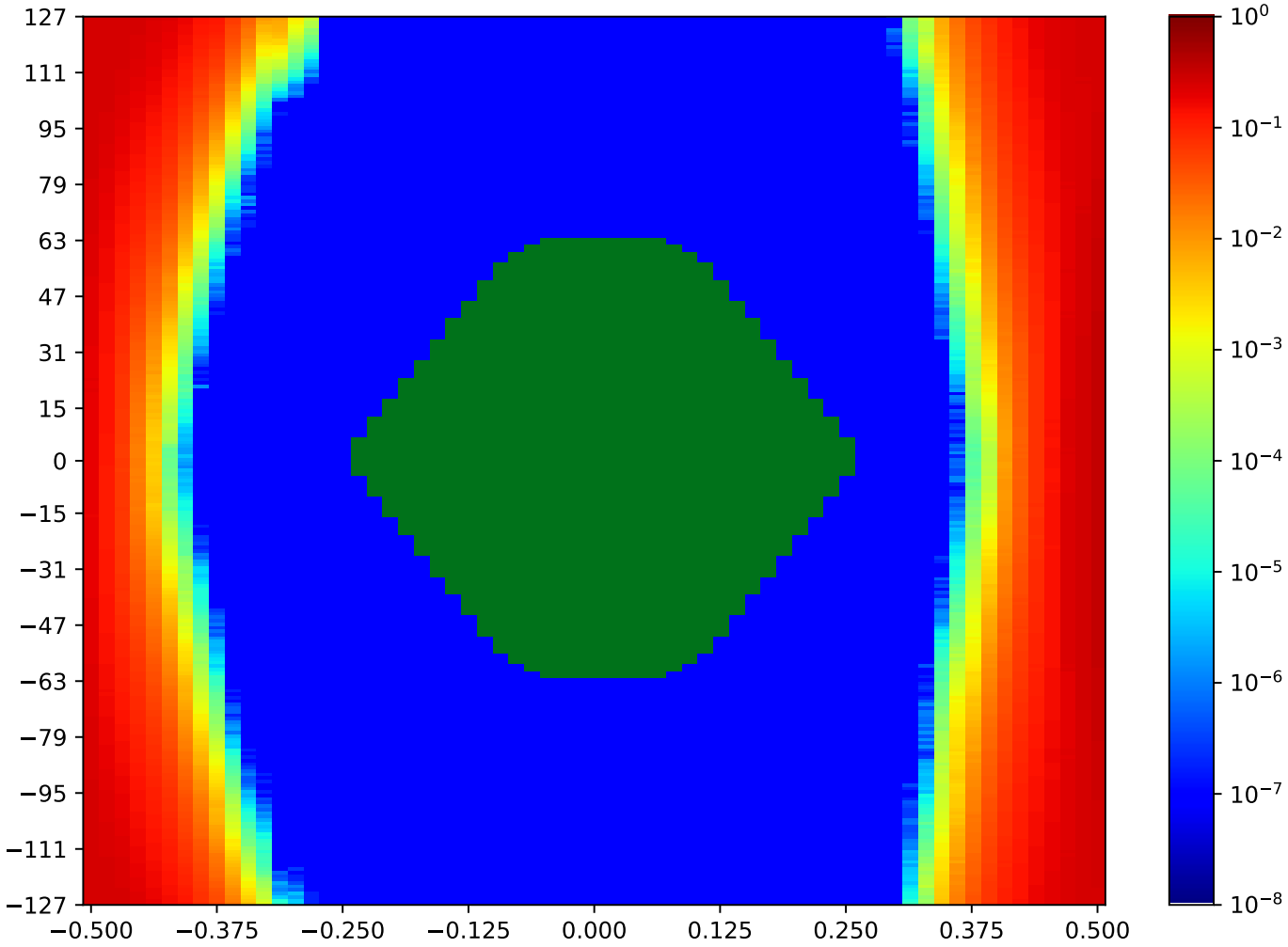


Figure 3.107: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.10 MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Table 3.99: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:35:32		2018-Sep-26 18:36:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10978	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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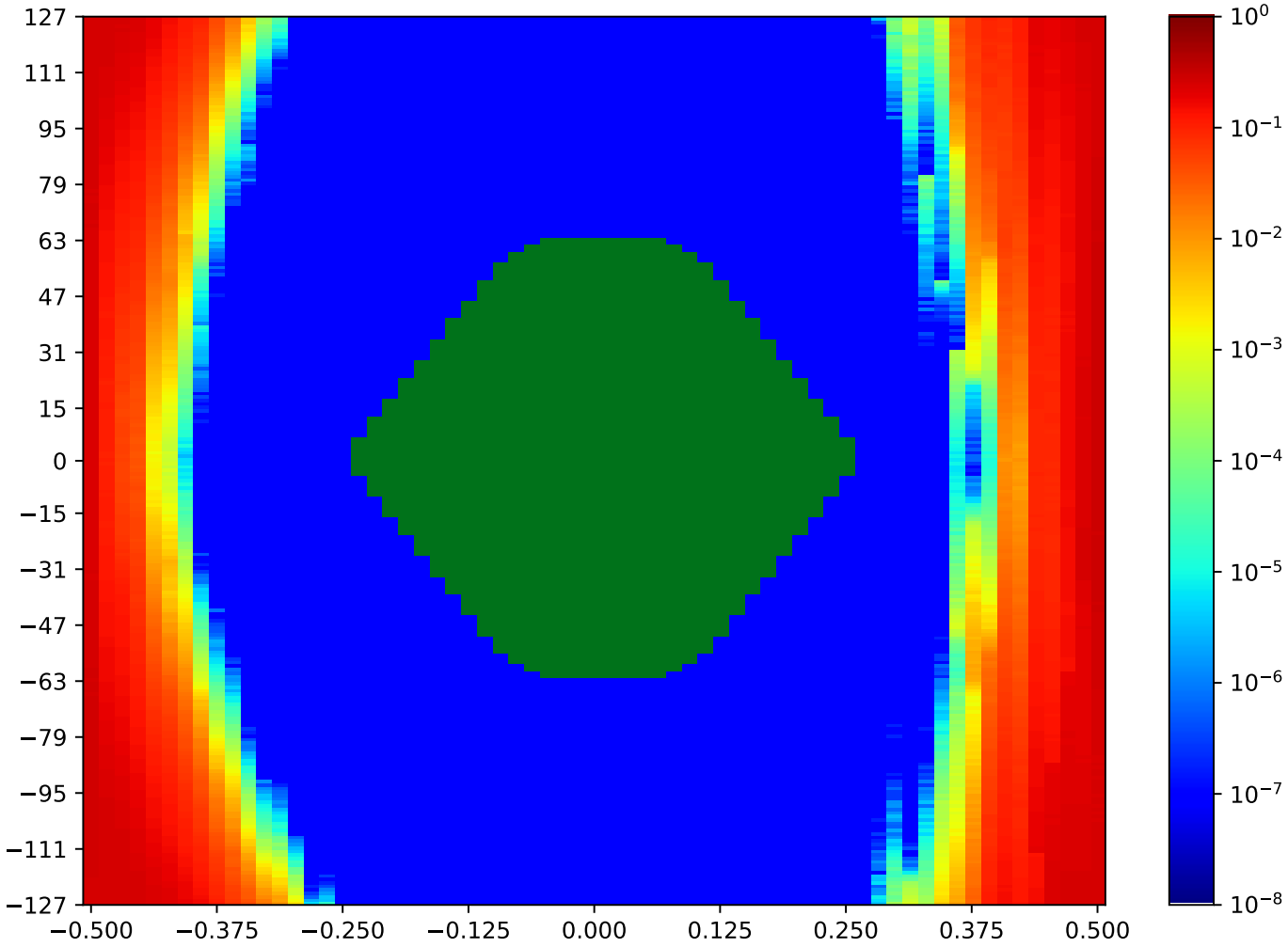


Figure 3.108: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.11 MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Table 3.100: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:36:09		2018-Sep-26 18:36:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10700	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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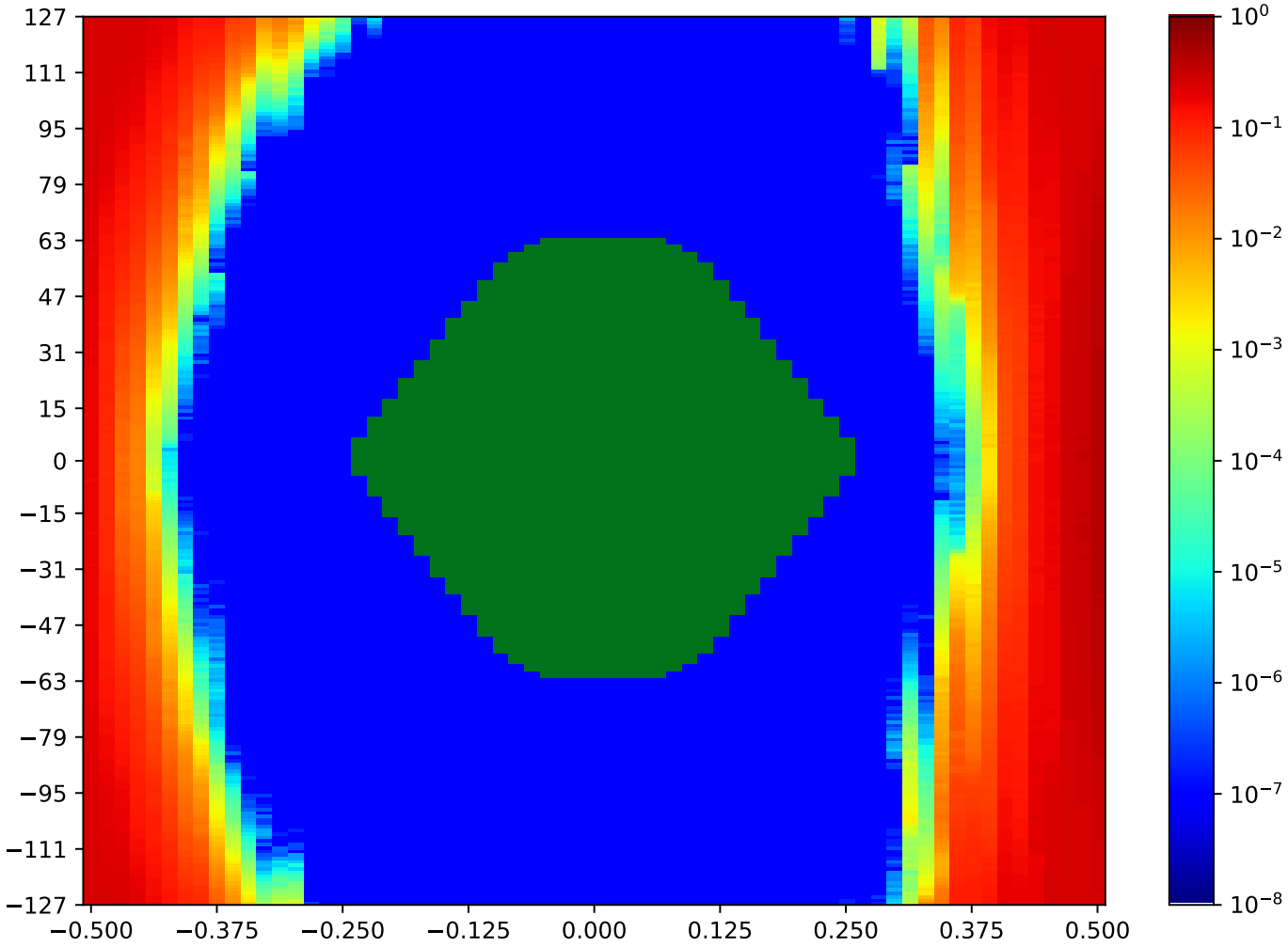


Figure 3.109: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.12 MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Table 3.101: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:36:47		2018-Sep-26 18:37:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11002	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

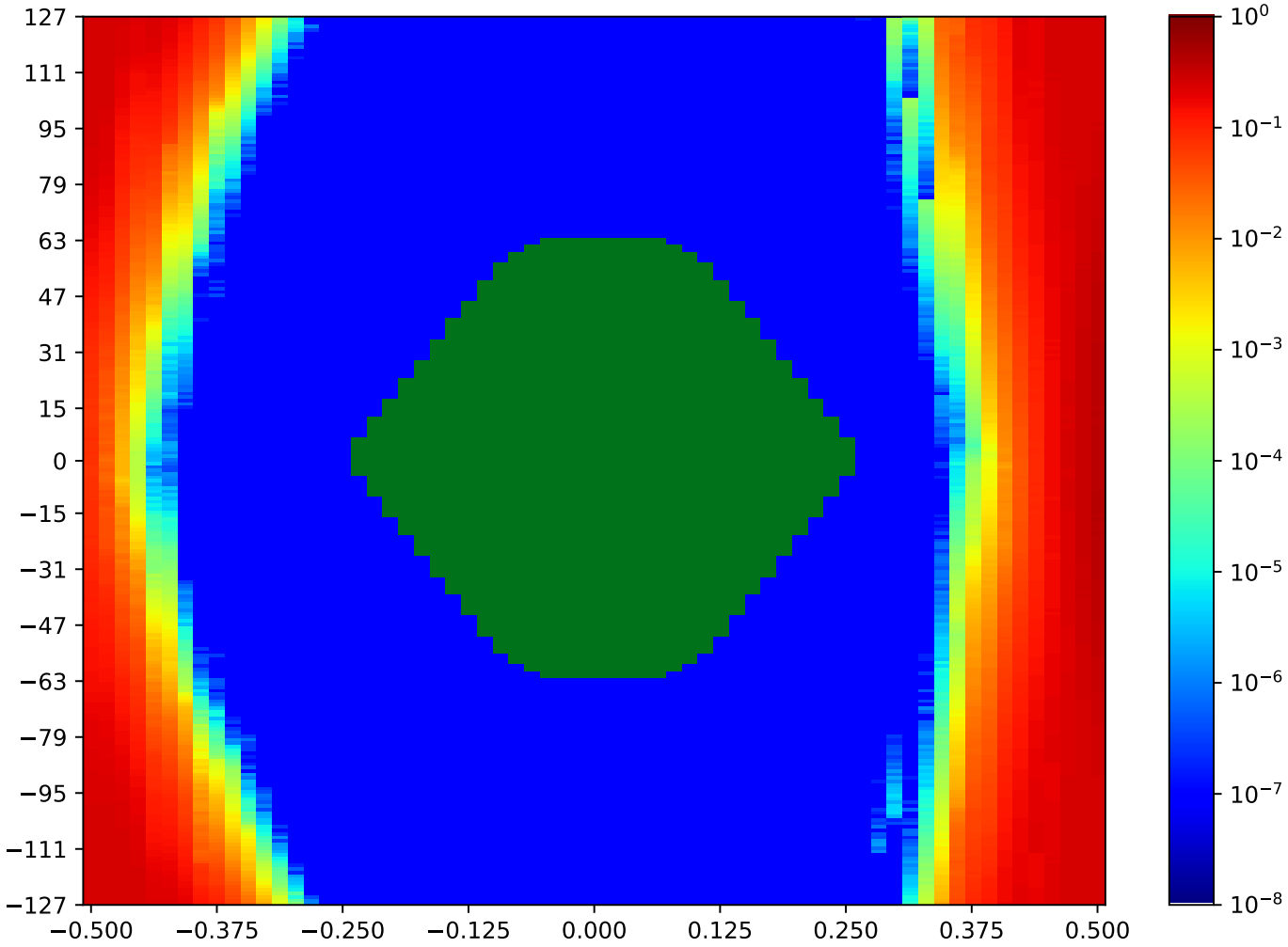


Figure 3.110: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.13 MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Table 3.102: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:37:24		2018-Sep-26 18:38:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11112	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

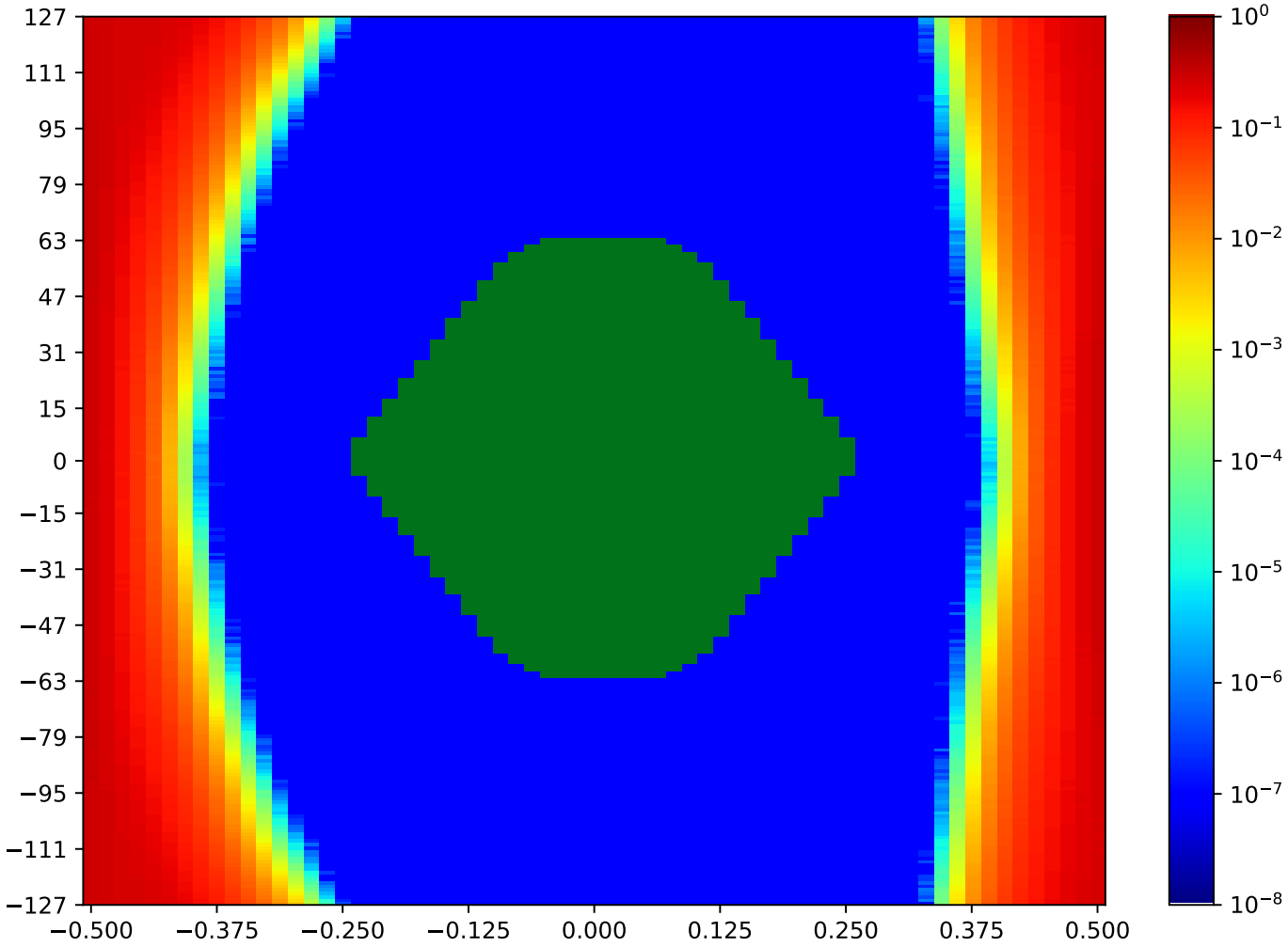


Figure 3.111: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.14 MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Table 3.103: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:38:01		2018-Sep-26 18:38:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10808	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

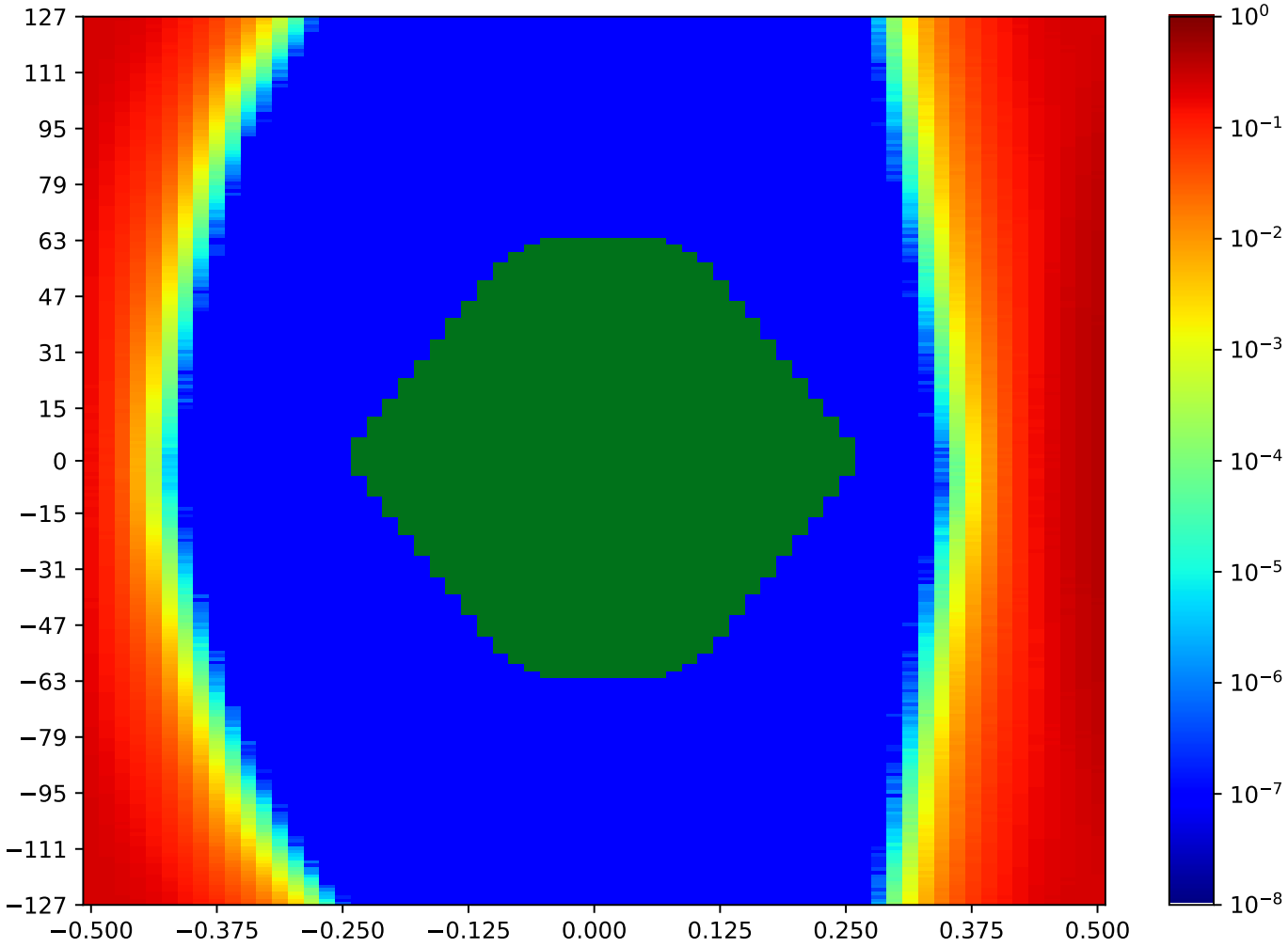


Figure 3.112: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.15 MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Table 3.104: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:38:39		2018-Sep-26 18:39:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10801	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

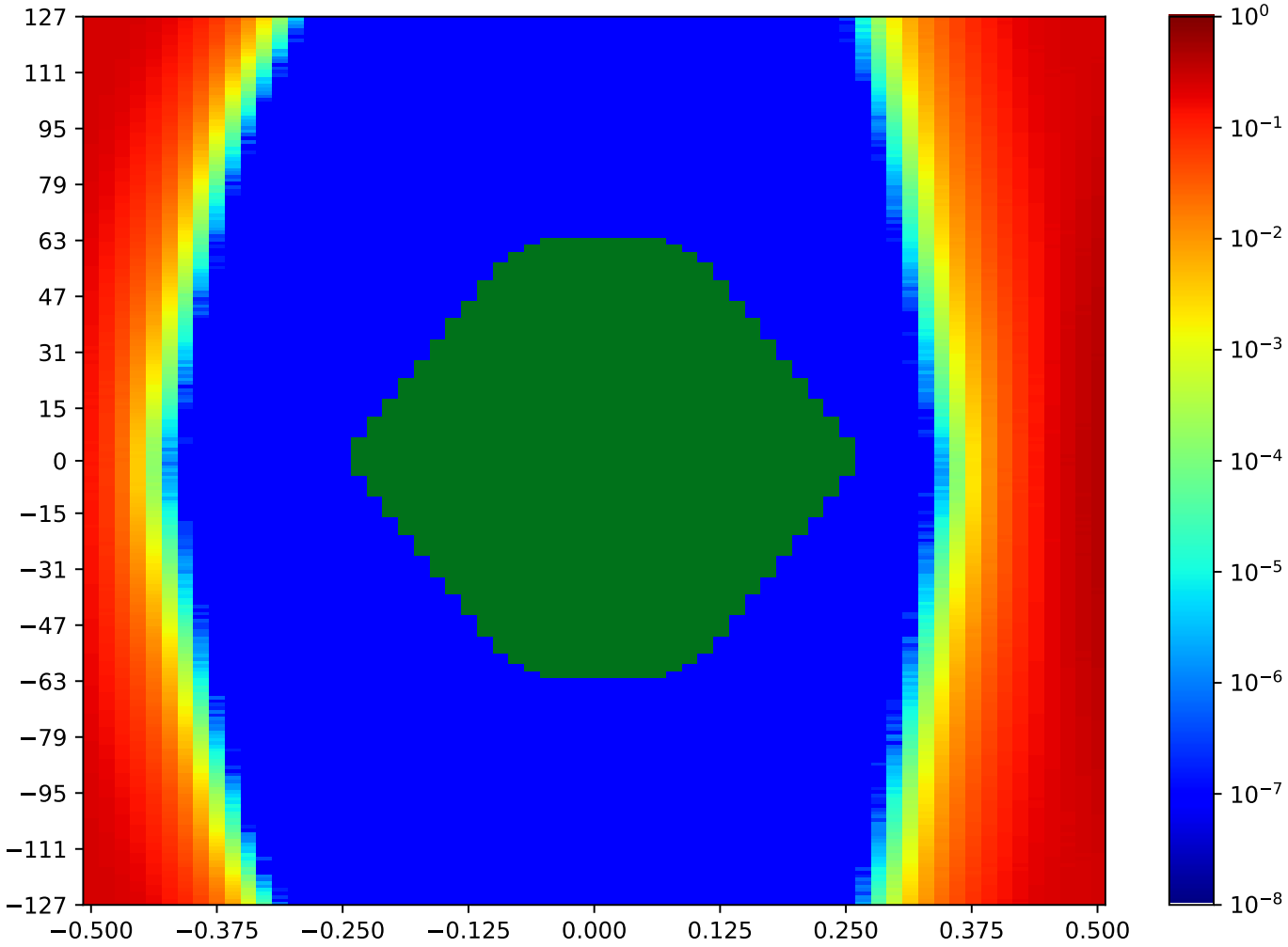


Figure 3.113: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.16 MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Table 3.105: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:39:16		2018-Sep-26 18:39:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11215	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

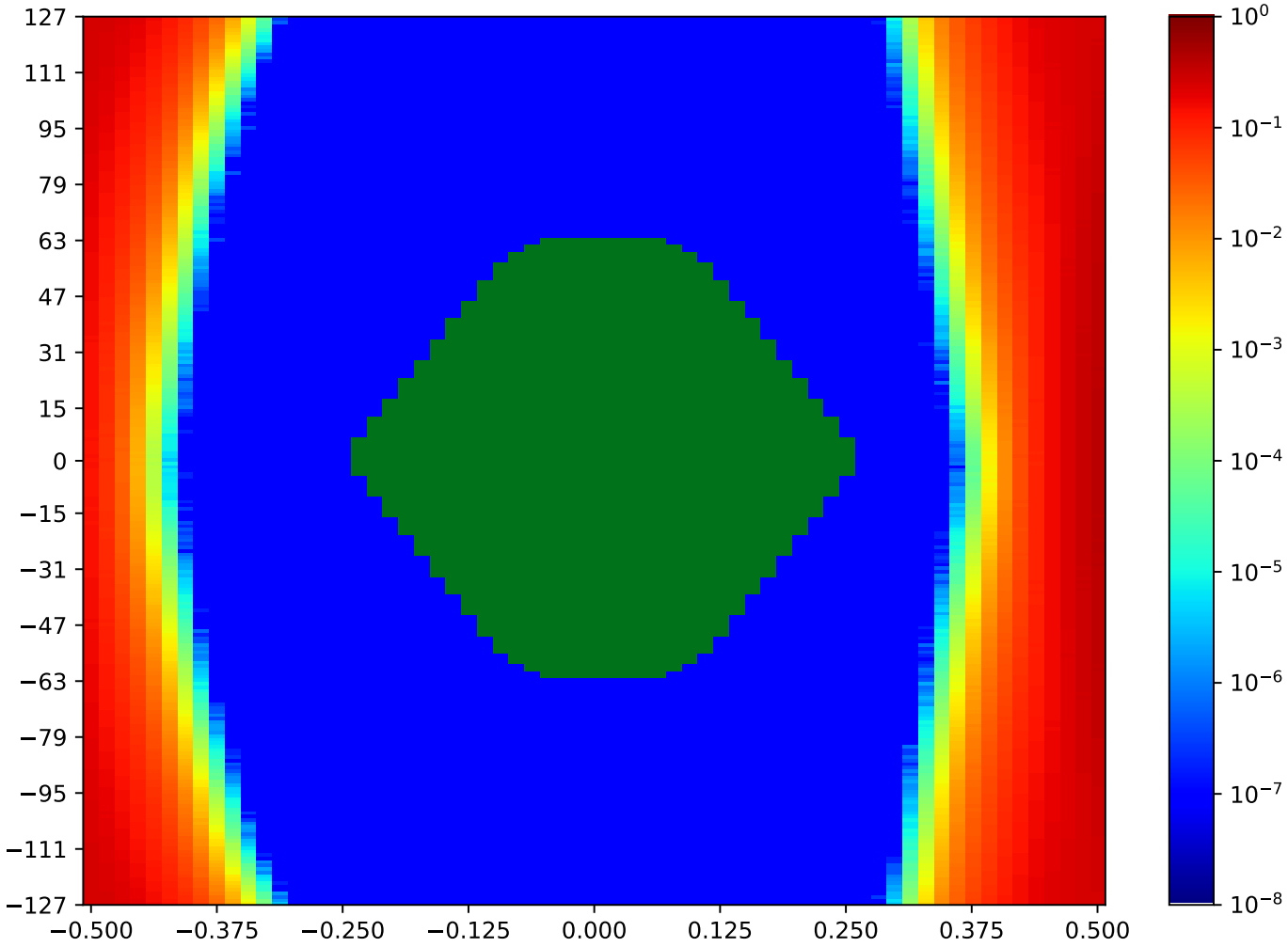


Figure 3.114: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.17 MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Table 3.106: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:39:54		2018-Sep-26 18:40:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9975	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

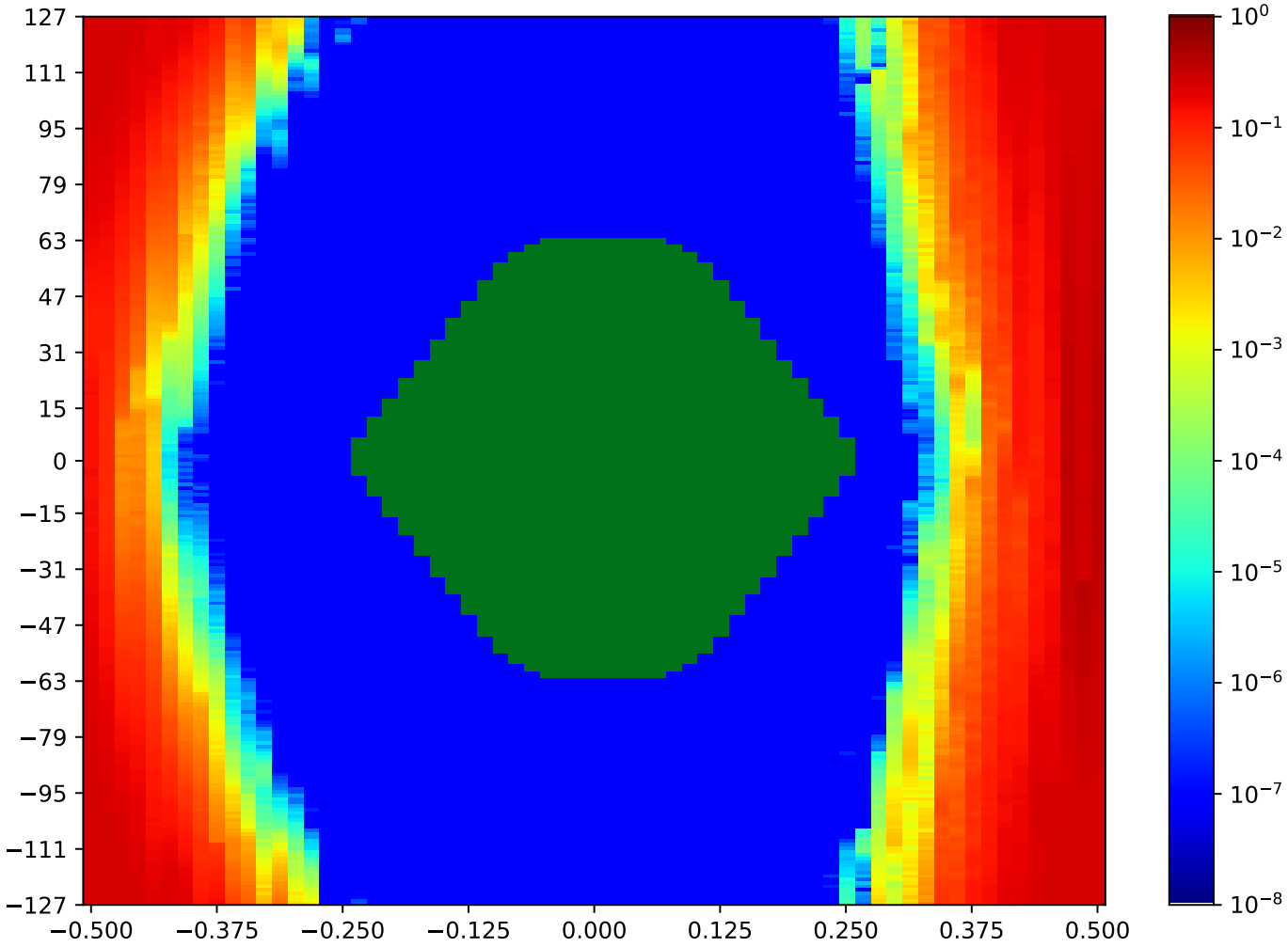


Figure 3.115: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.18 MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Table 3.107: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:40:30		2018-Sep-26 18:41:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10660	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

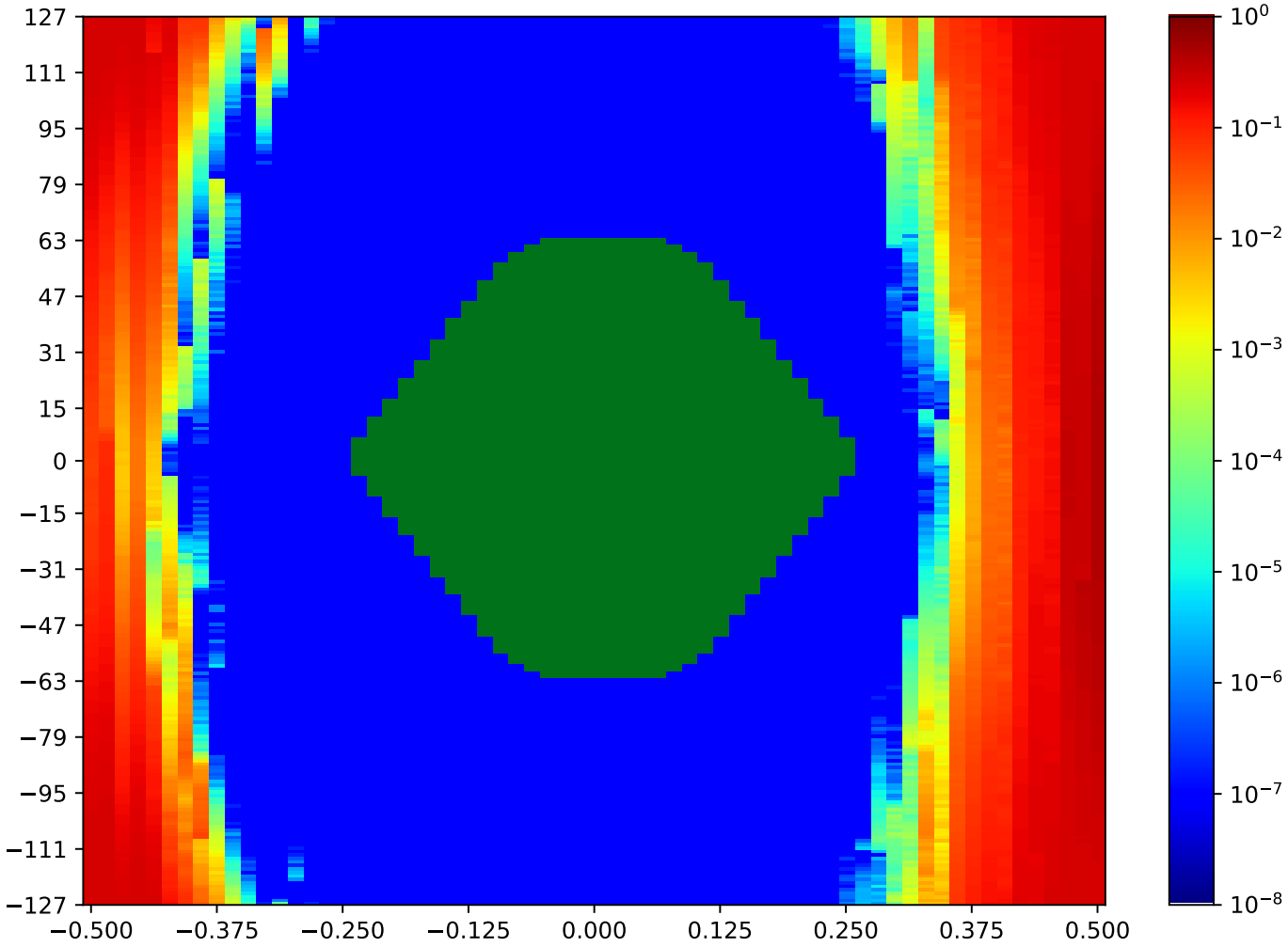


Figure 3.116: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.19 MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Table 3.108: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:41:08		2018-Sep-26 18:41:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10995	49	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

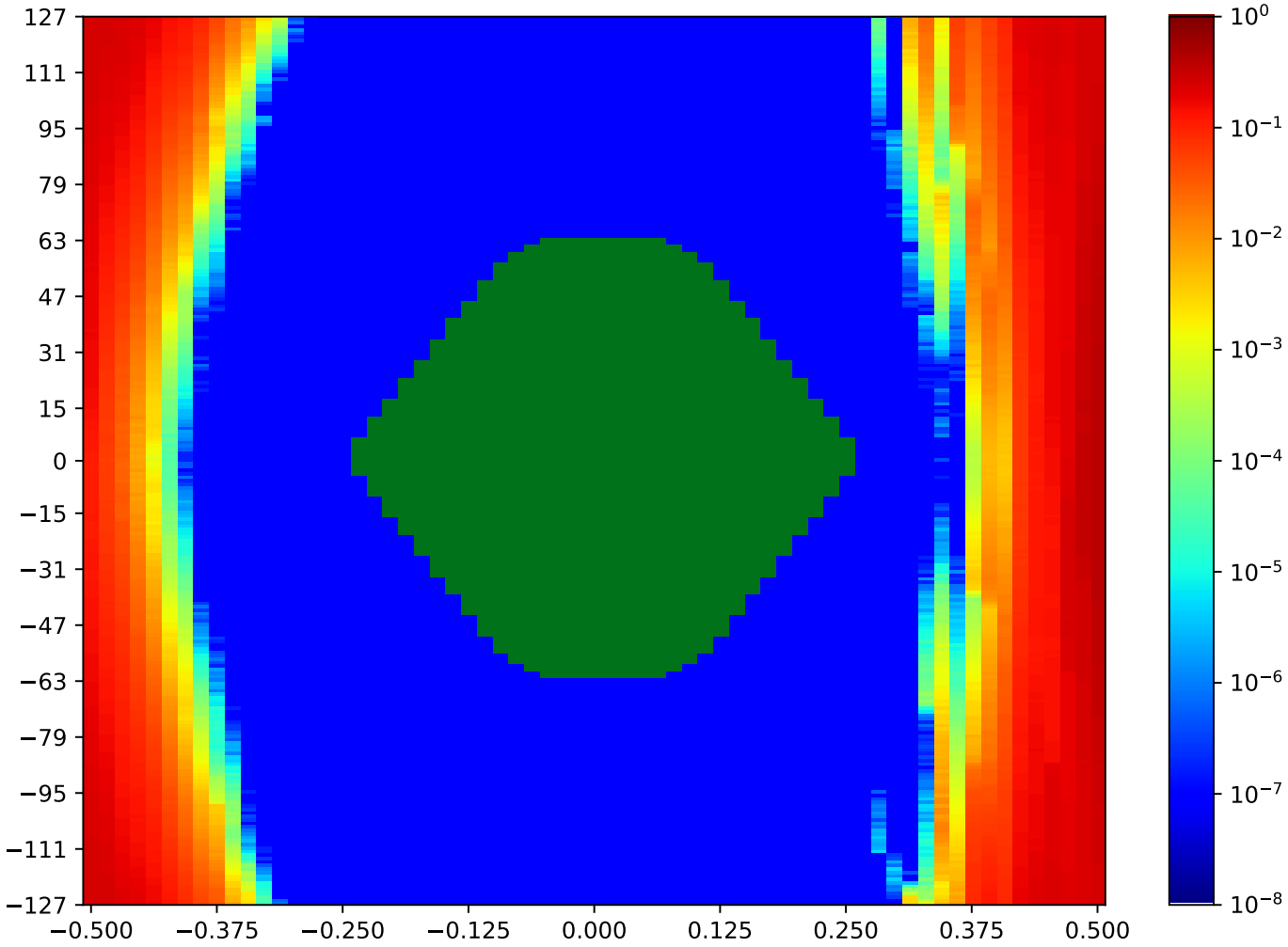


Figure 3.117: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.20 MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Table 3.109: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:41:45		2018-Sep-26 18:42:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10488	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

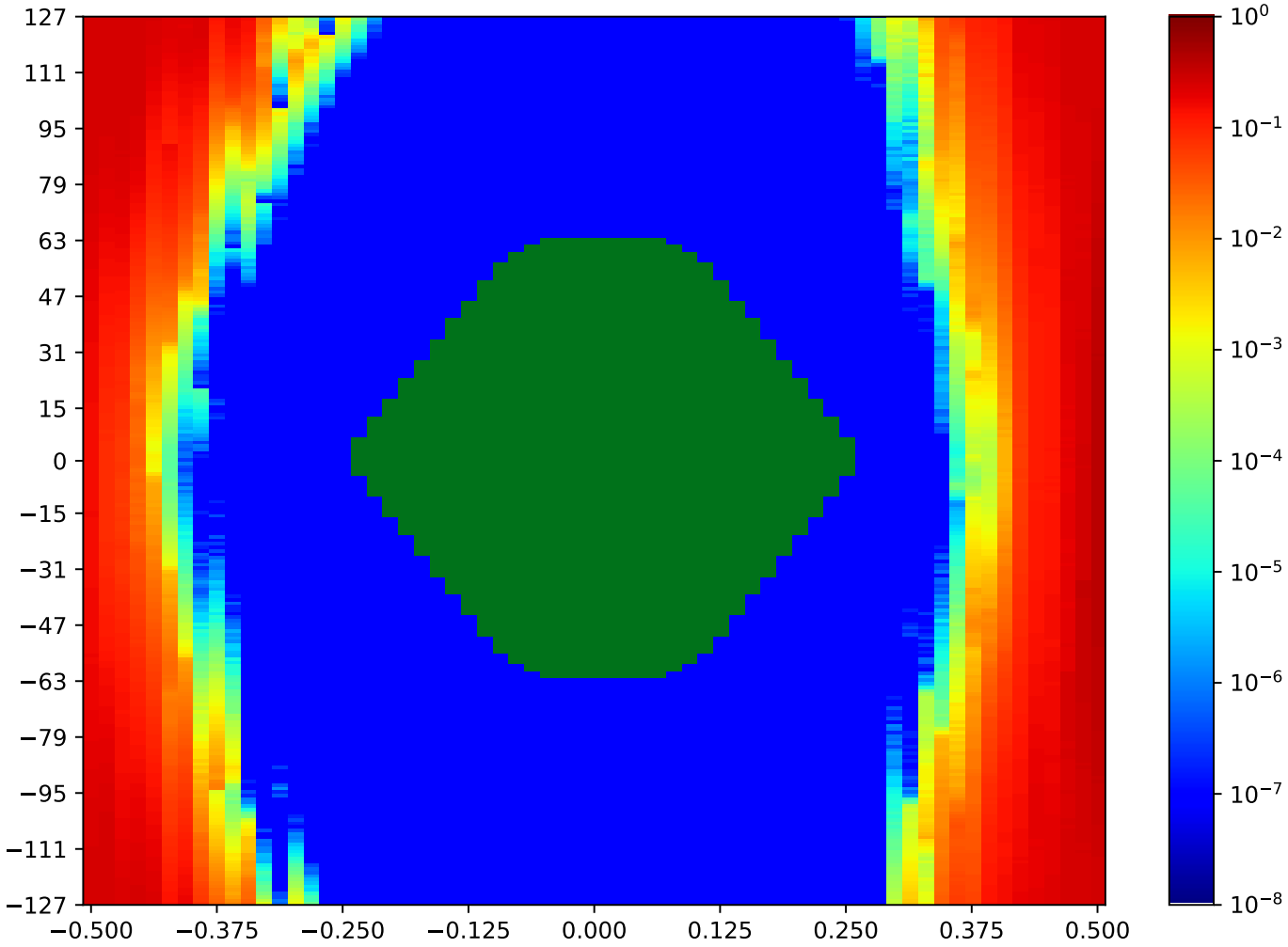


Figure 3.118: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.21 MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Table 3.110: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:42:23		2018-Sep-26 18:43:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10524	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

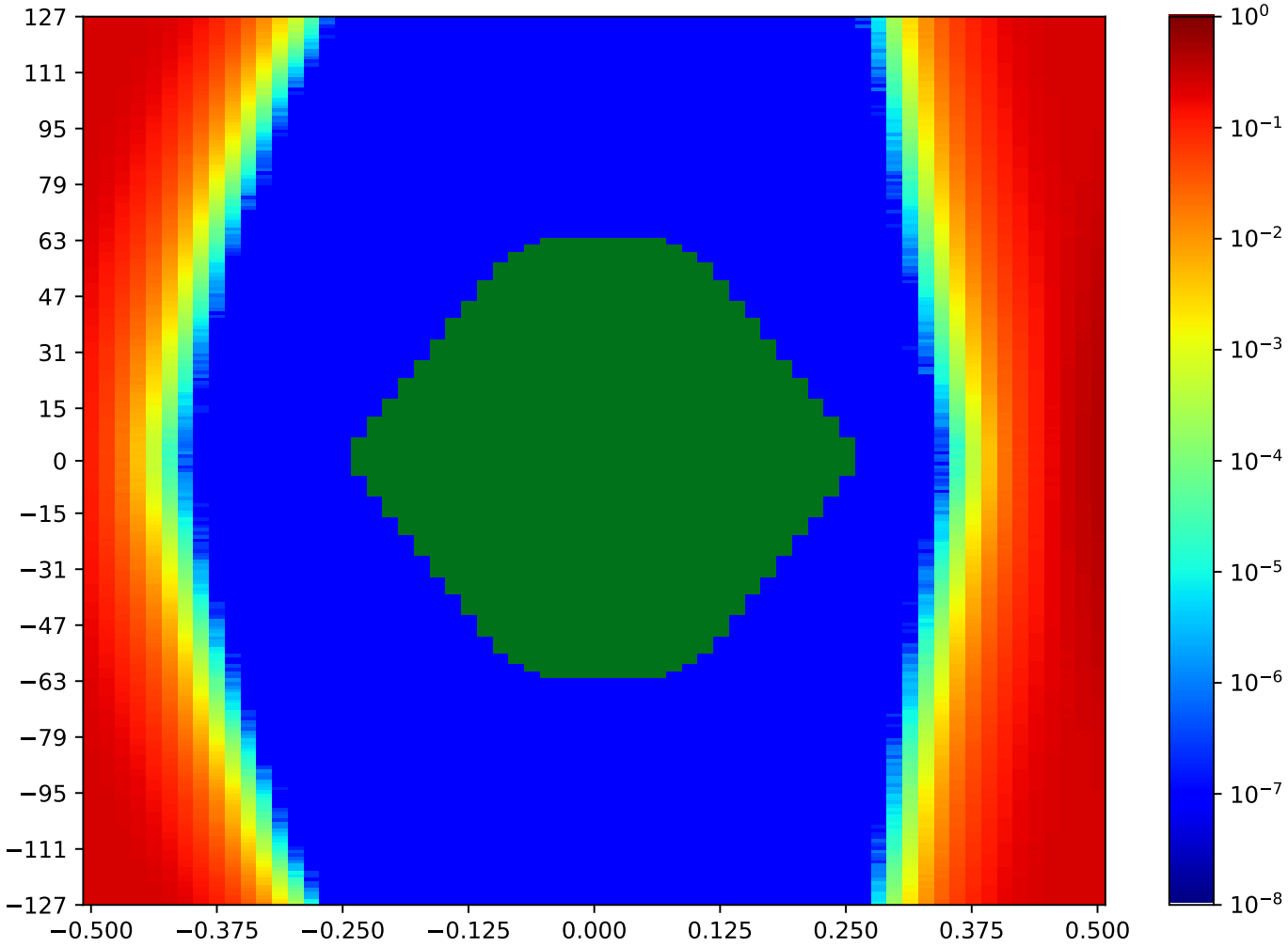


Figure 3.119: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.22 MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Table 3.111: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:43:00		2018-Sep-26 18:43:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11315	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

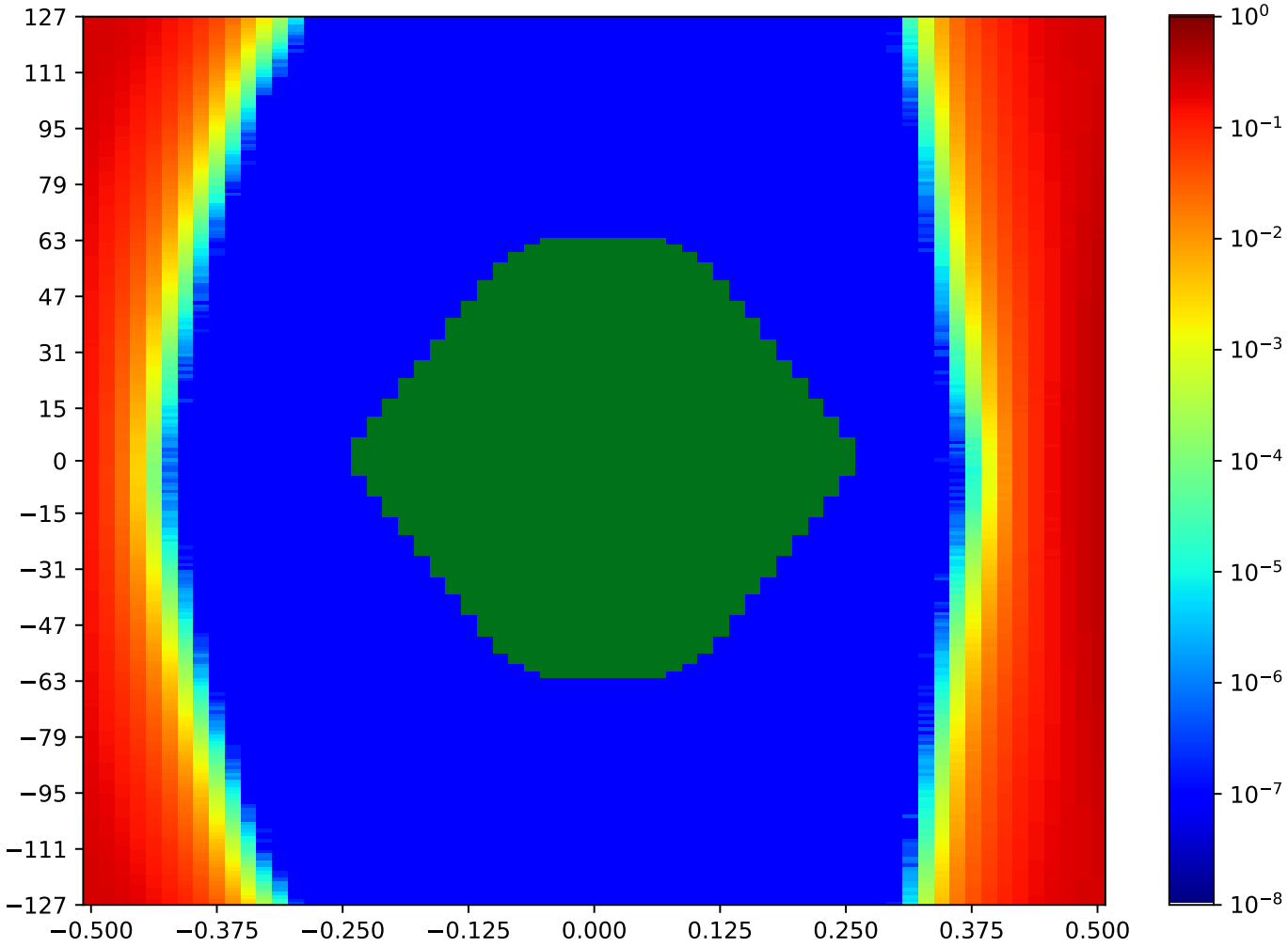


Figure 3.120: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.23 MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Table 3.112: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:43:38		2018-Sep-26 18:44:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10523	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

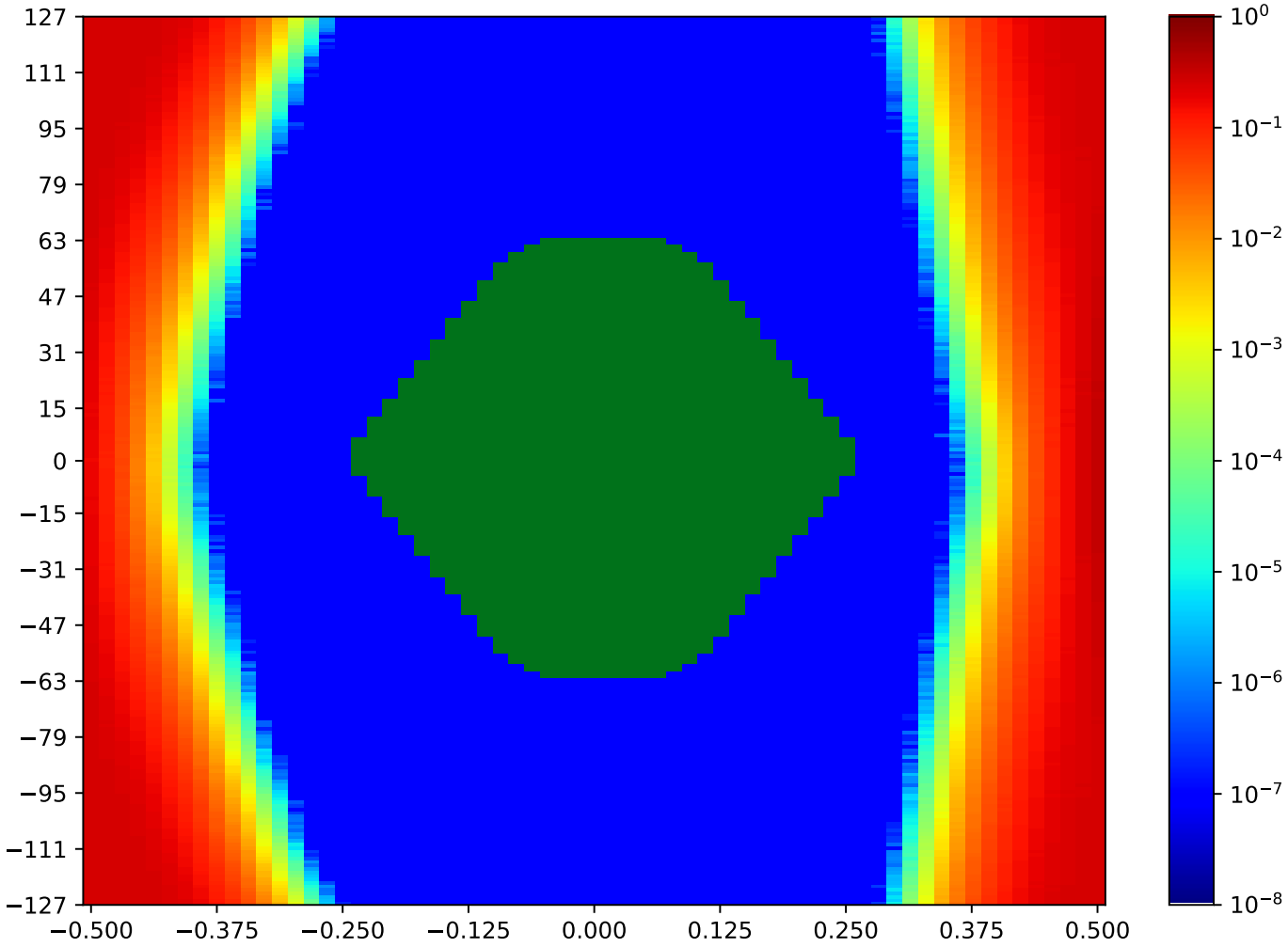


Figure 3.121: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.24 MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Table 3.113: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:44:15		2018-Sep-26 18:44:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10607	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

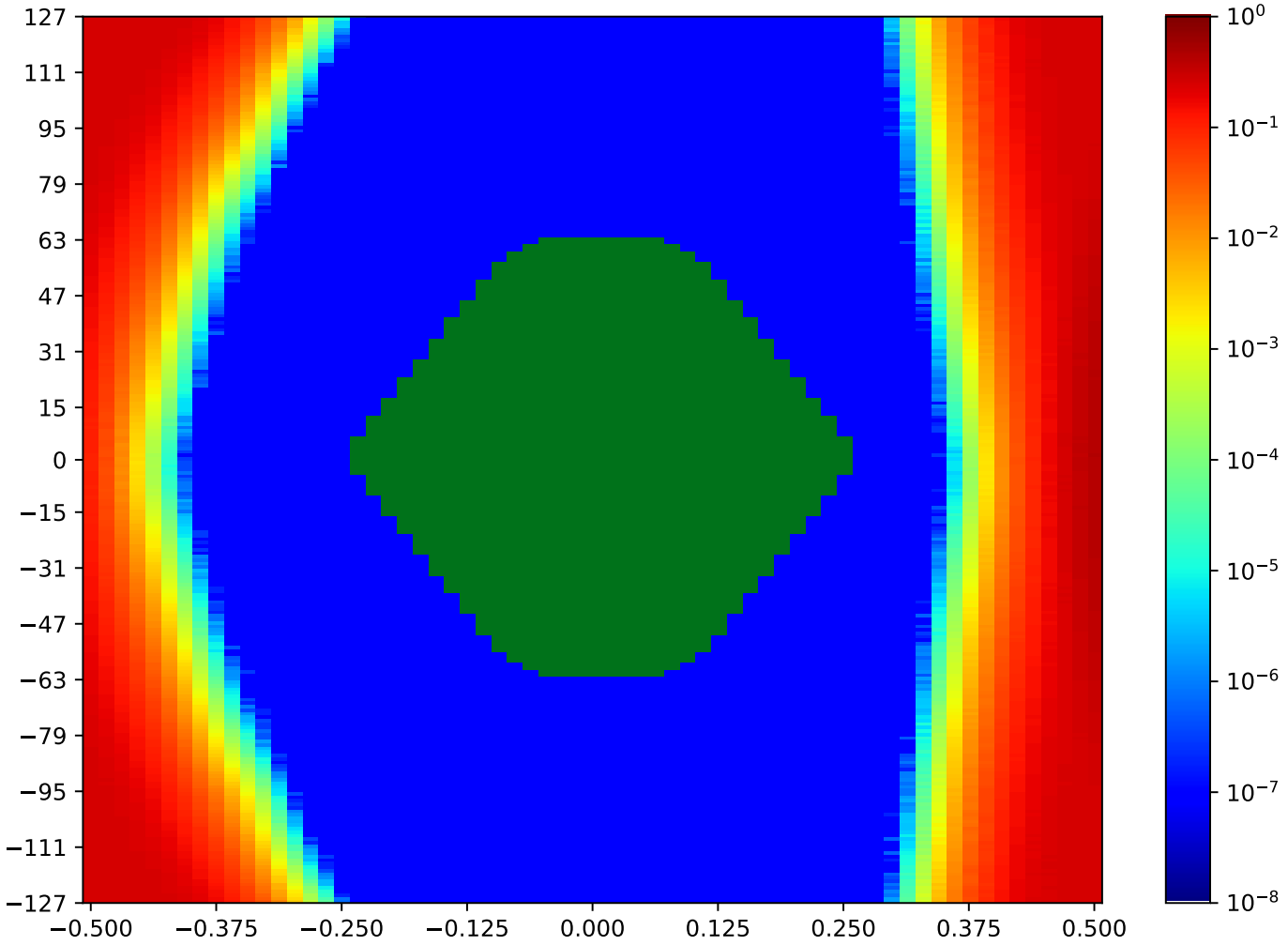


Figure 3.122: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.25 MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Table 3.114: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:44:53		2018-Sep-26 18:45:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10903	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

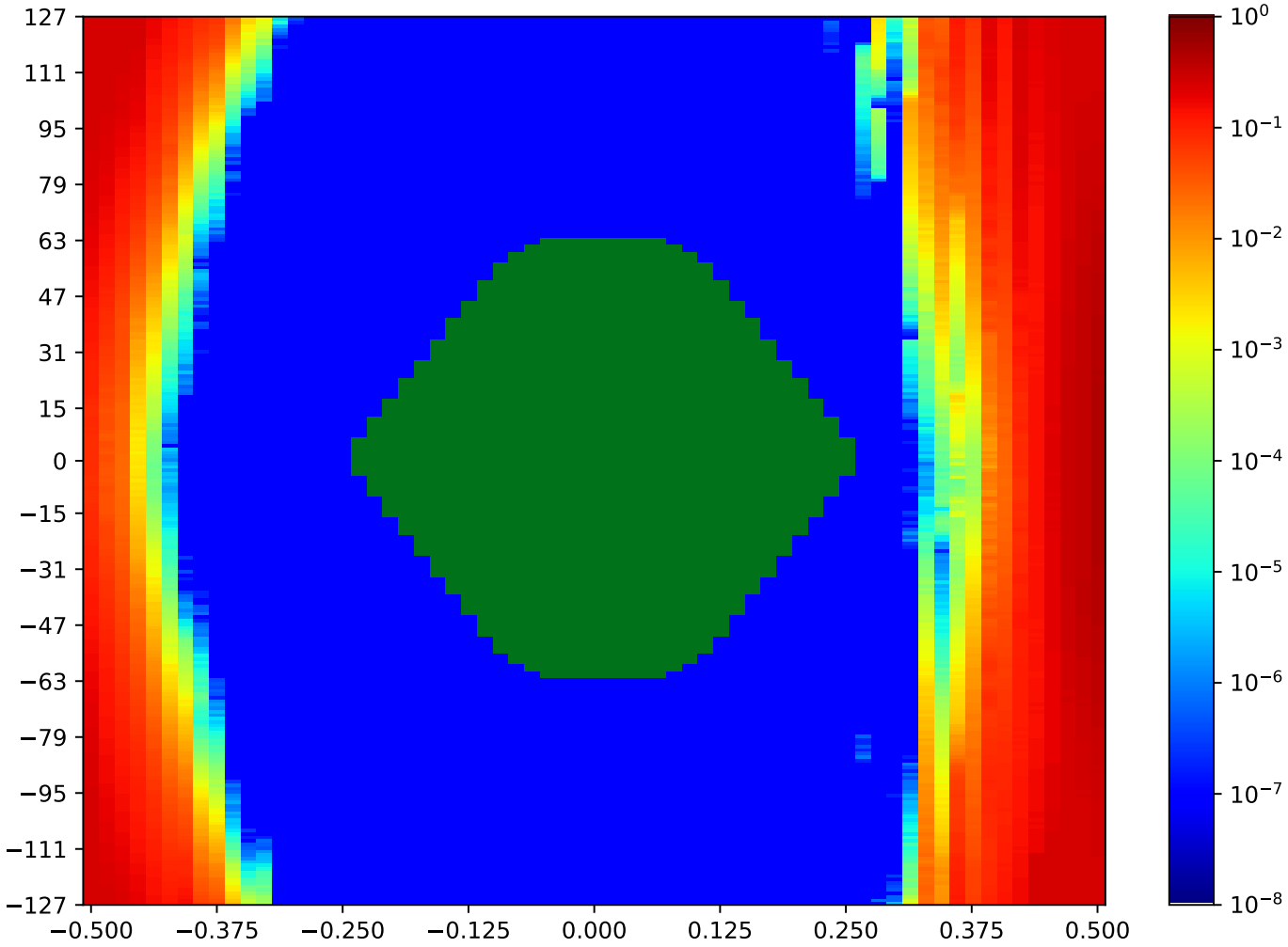


Figure 3.123: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.26 MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Table 3.115: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:45:30		2018-Sep-26 18:46:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11082	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

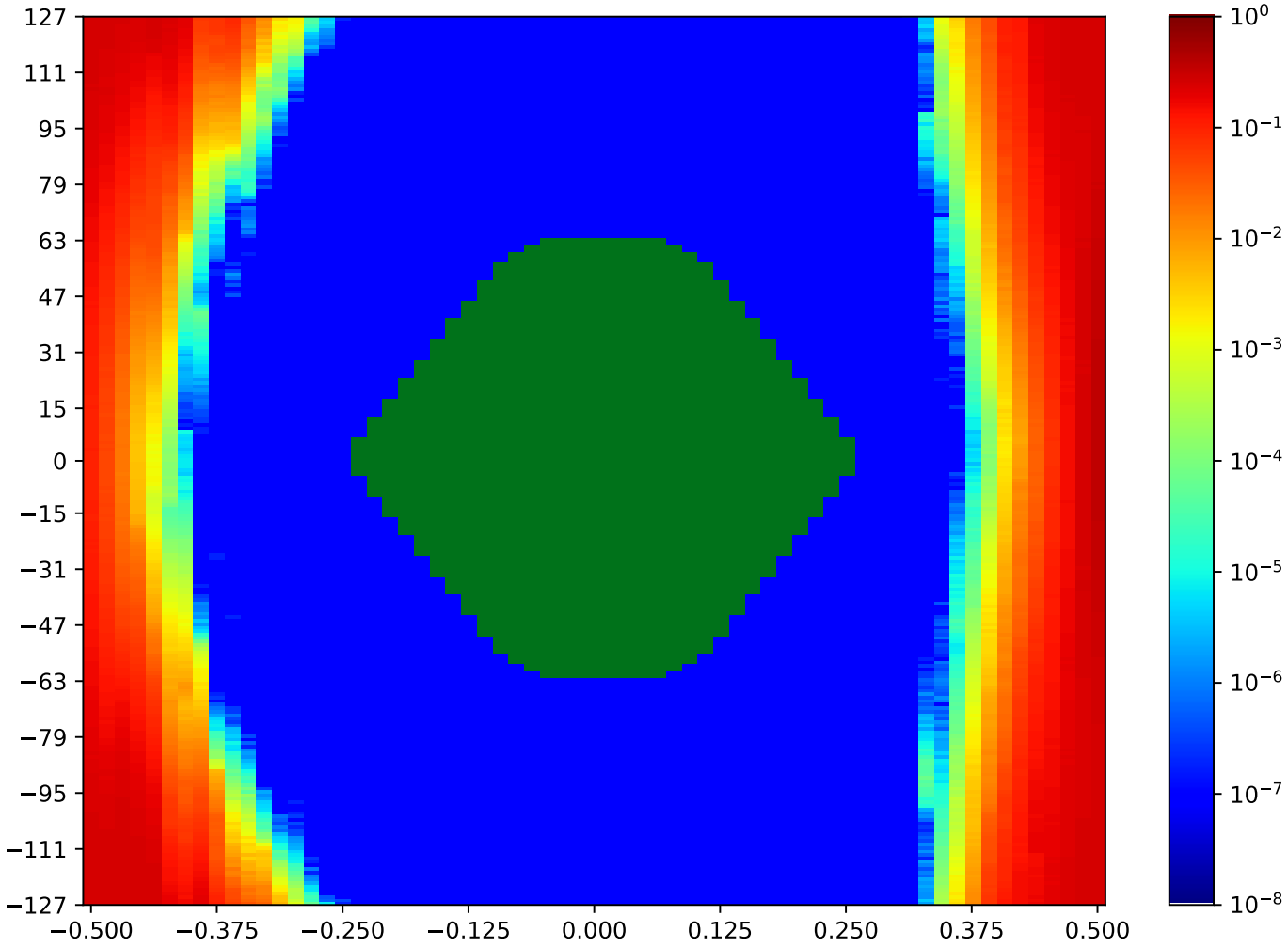


Figure 3.124: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.27 MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Table 3.116: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:46:08		2018-Sep-26 18:46:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11147	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

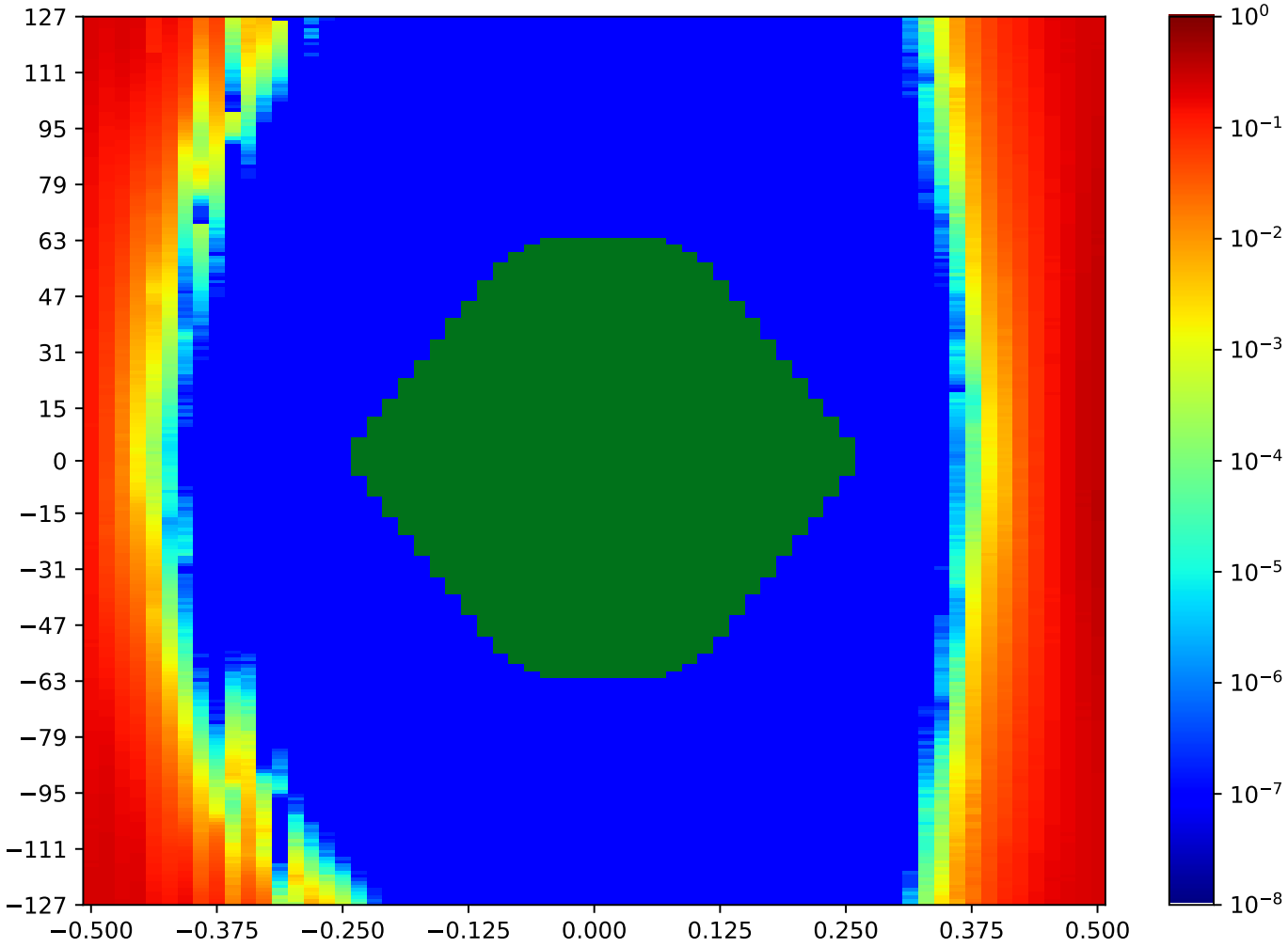


Figure 3.125: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.9.28 MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Table 3.117: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:46:45		2018-Sep-26 18:47:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10693	48	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

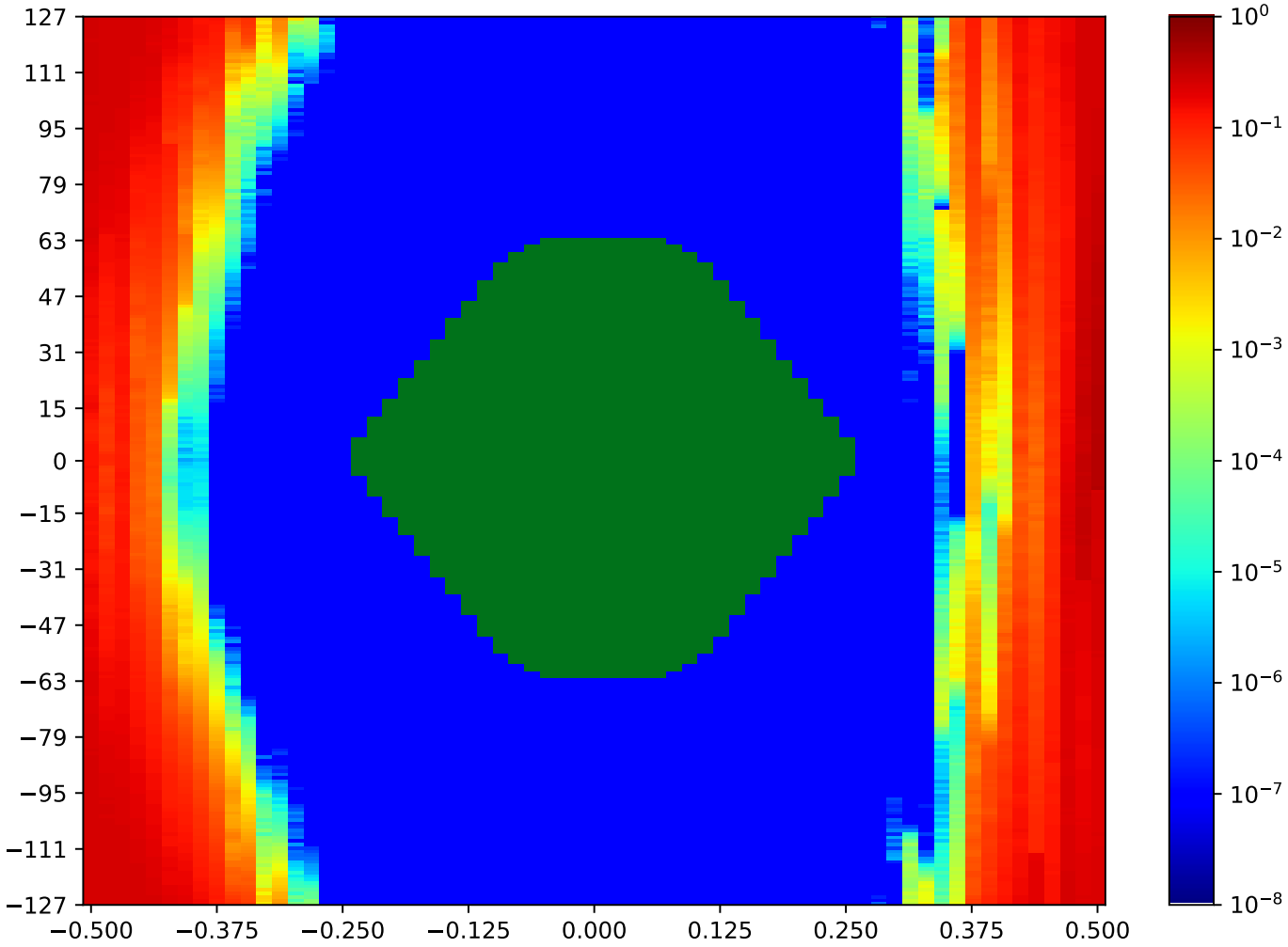


Figure 3.126: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10 MSP_A TX1 MSP_C RX17 Minipod Loopback

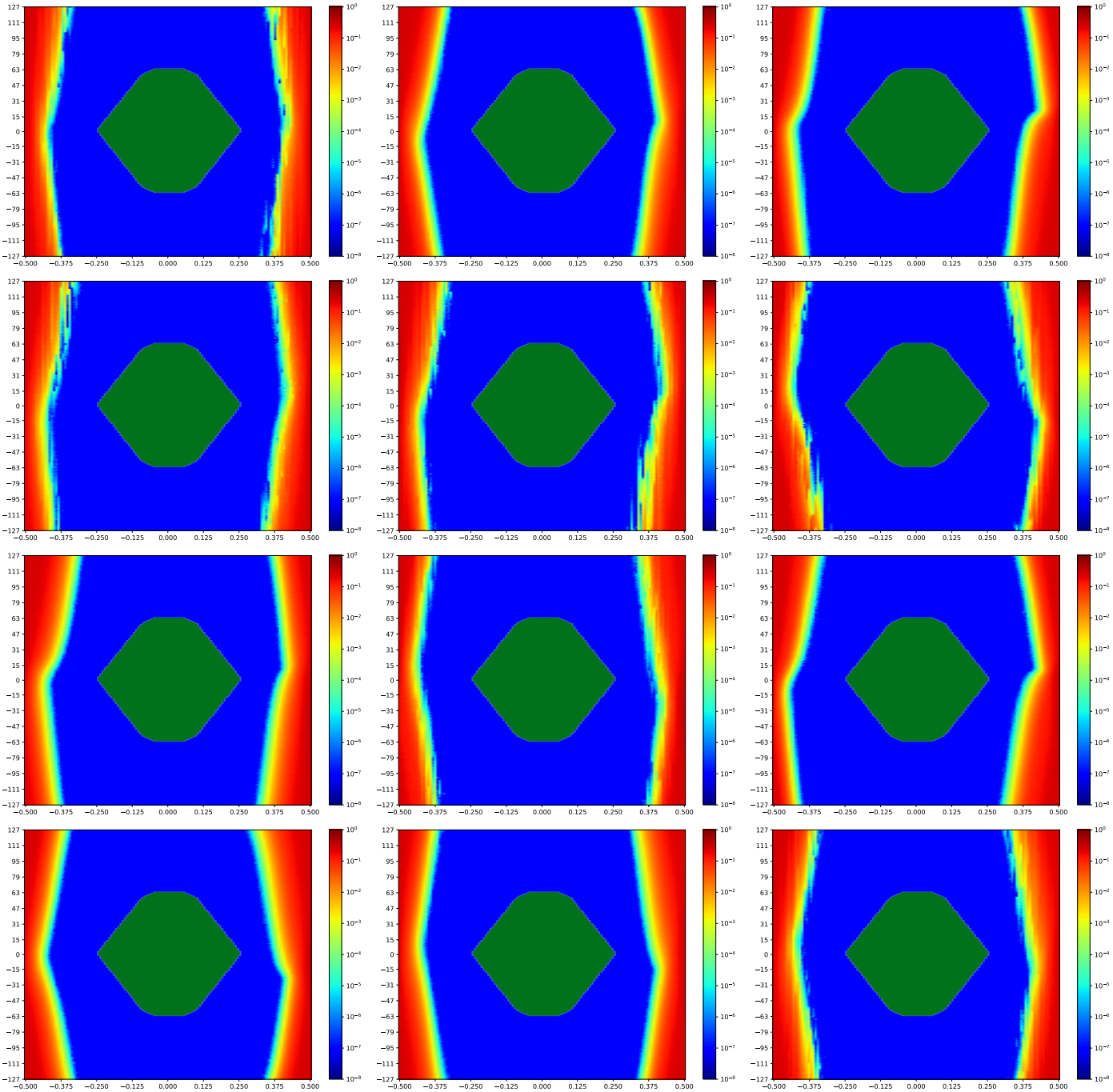


Figure 3.127: MSP_A TX1 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.140.

3.10.1 MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Table 3.118: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:55:55		2018-Sep-26 18:57:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24022	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

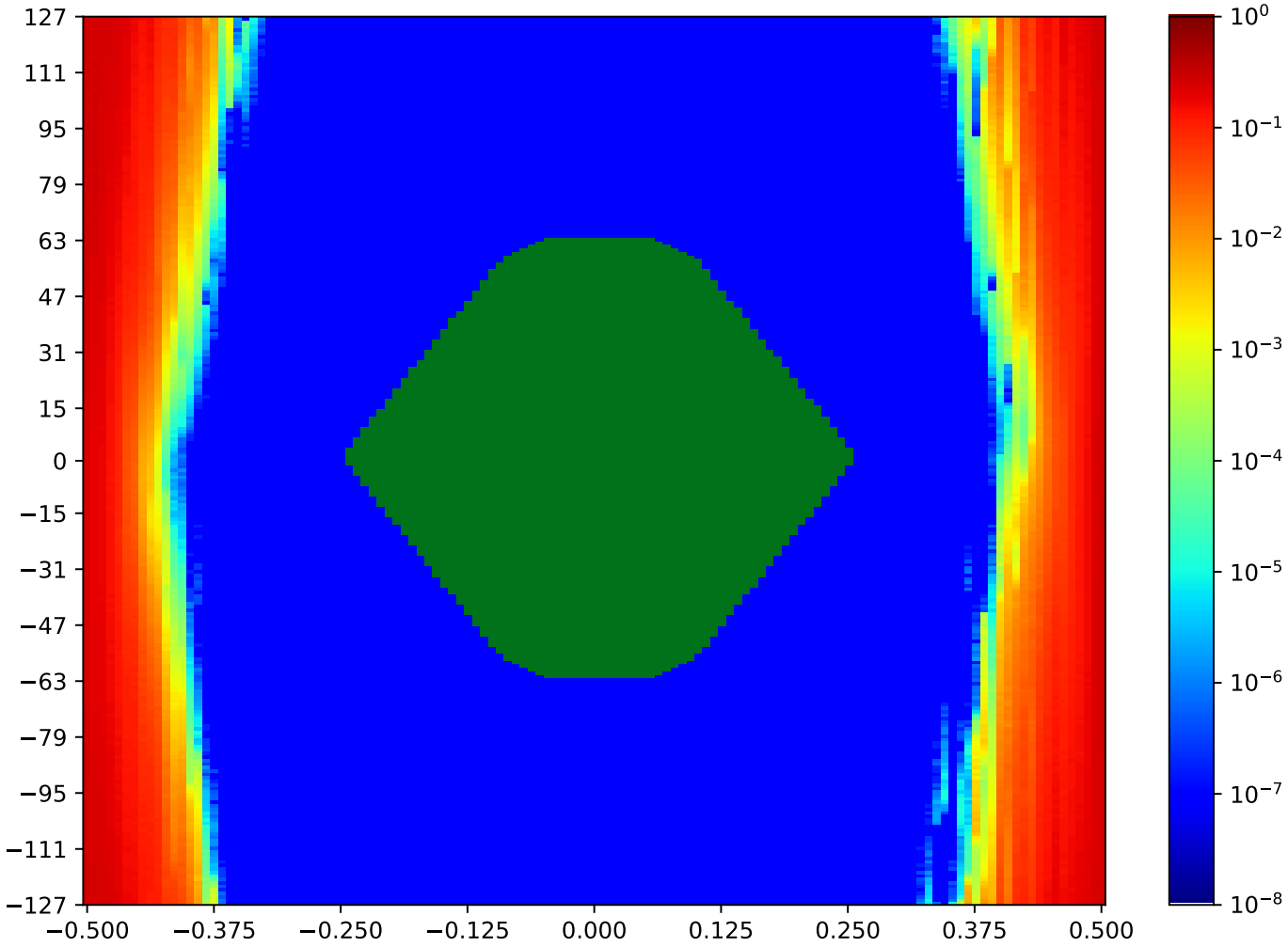


Figure 3.128: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.2 MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Table 3.119: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:58:21		2018-Sep-26 18:59:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23067	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

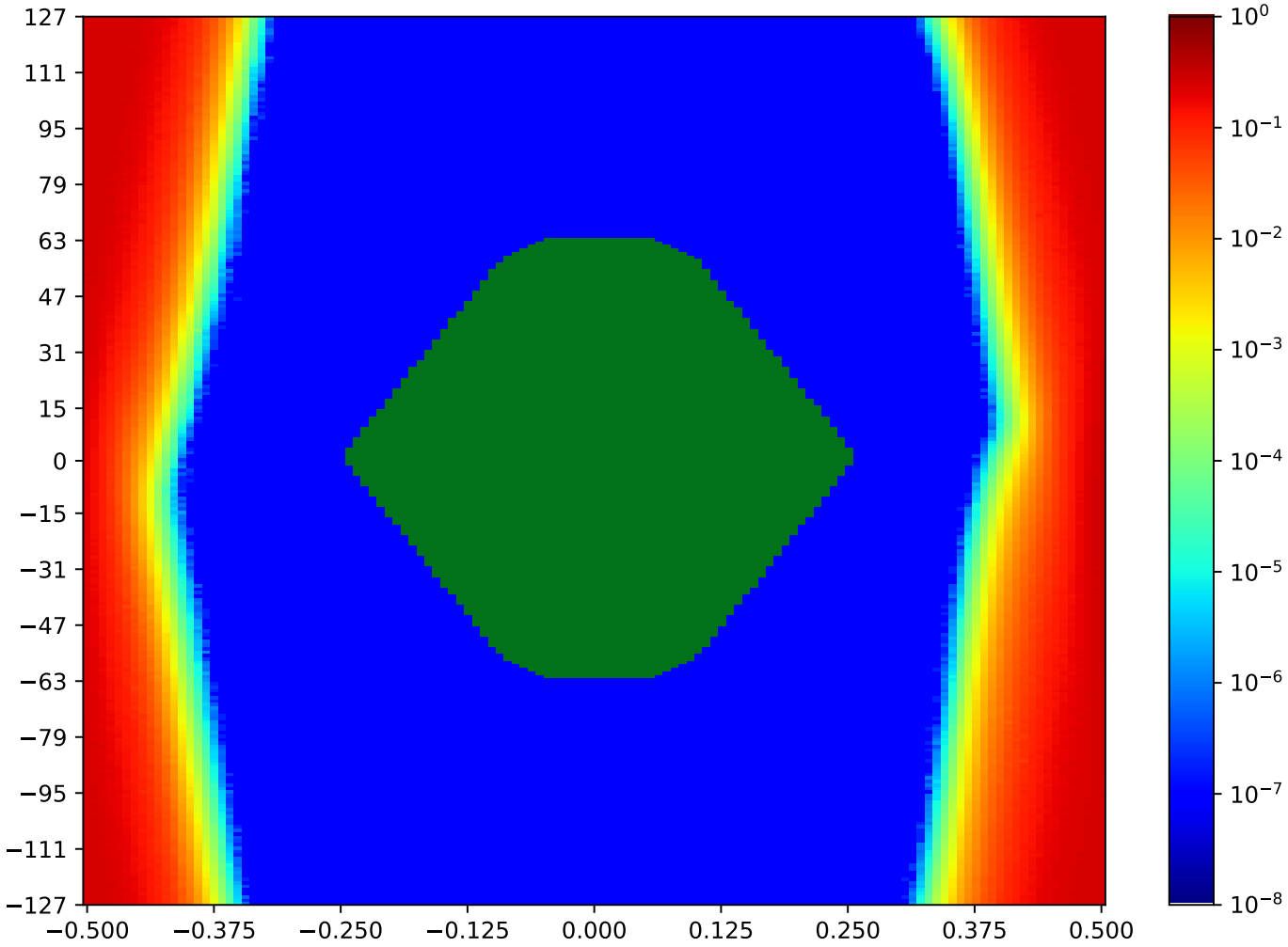


Figure 3.129: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.3 MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Table 3.120: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:59:34		2018-Sep-26 19:00:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23497	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

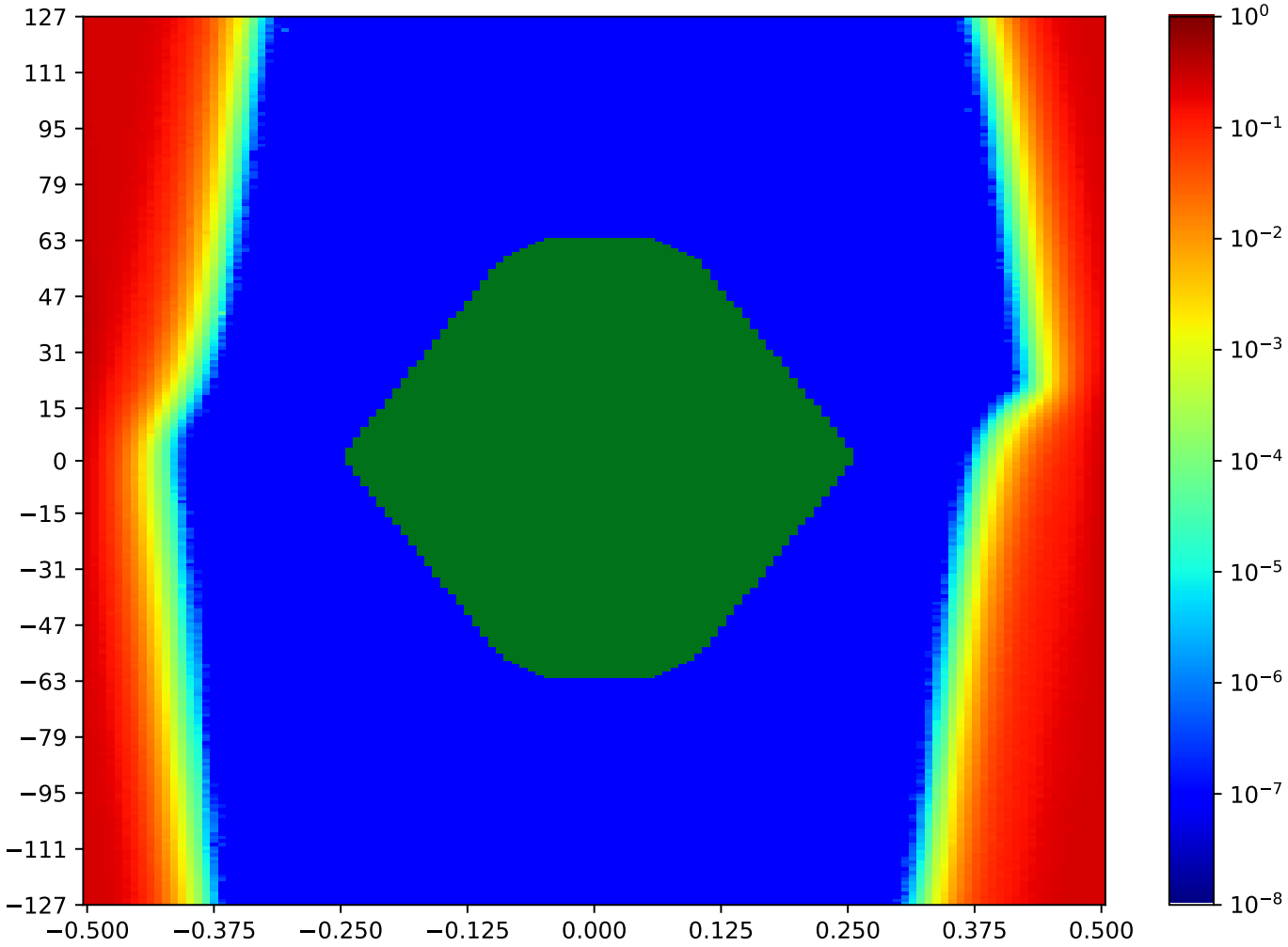


Figure 3.130: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.4 MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Table 3.121: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:53:28		2018-Sep-26 18:54:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23609	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

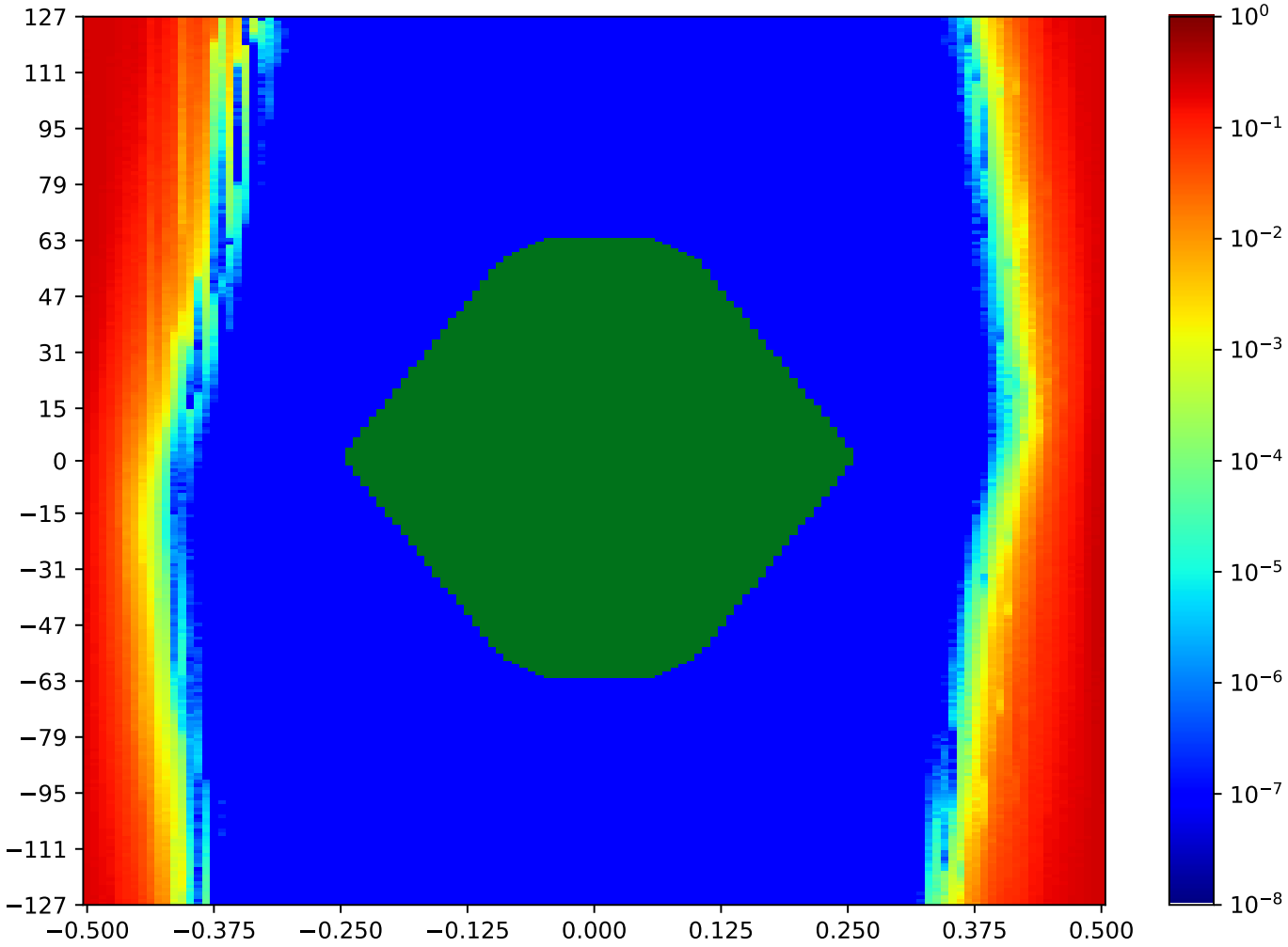


Figure 3.131: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.5 MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Table 3.122: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:03:14		2018-Sep-26 19:04:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23832	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

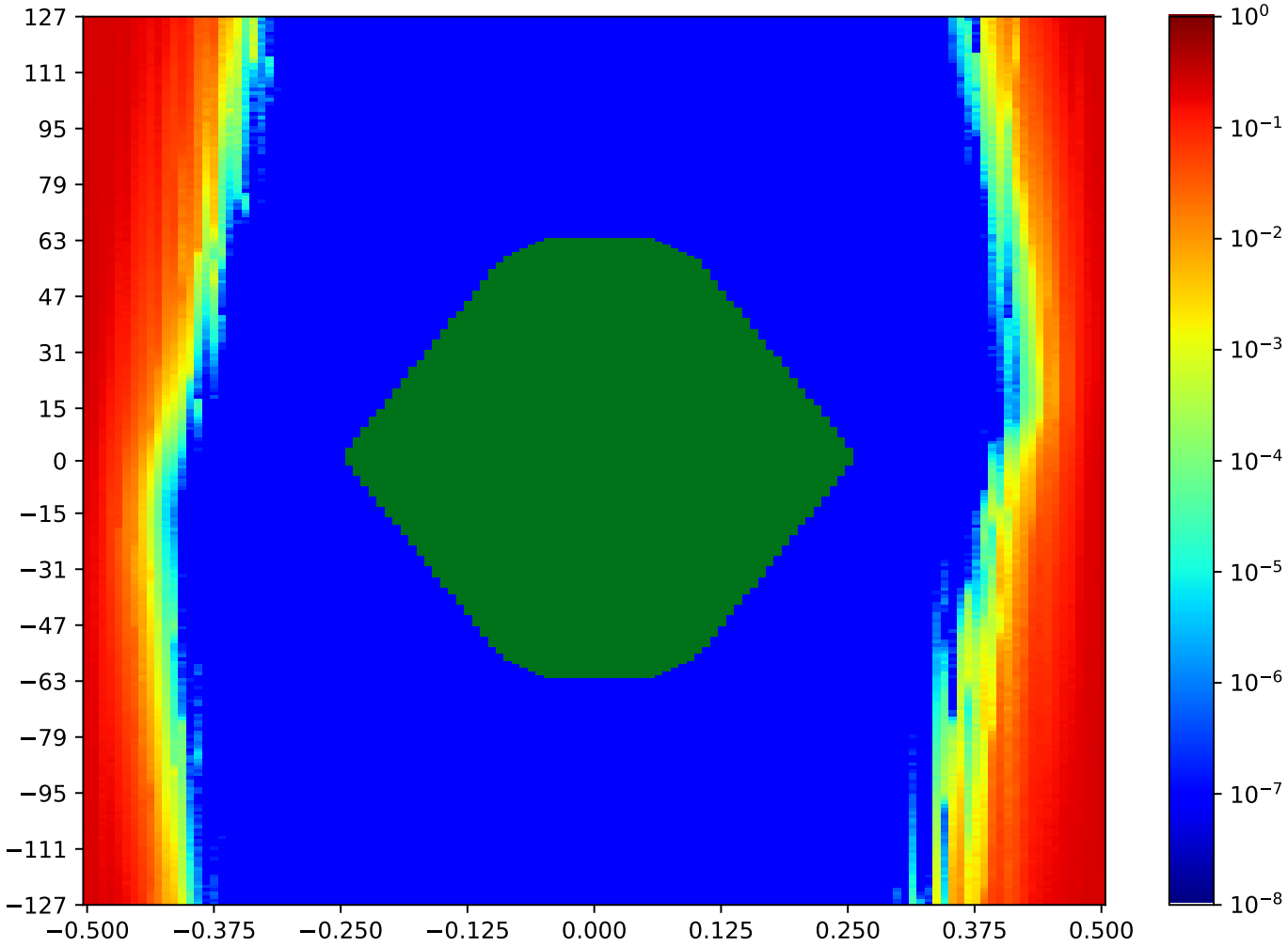


Figure 3.132: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.6 MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Table 3.123: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:52:15		2018-Sep-26 18:53:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23817	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

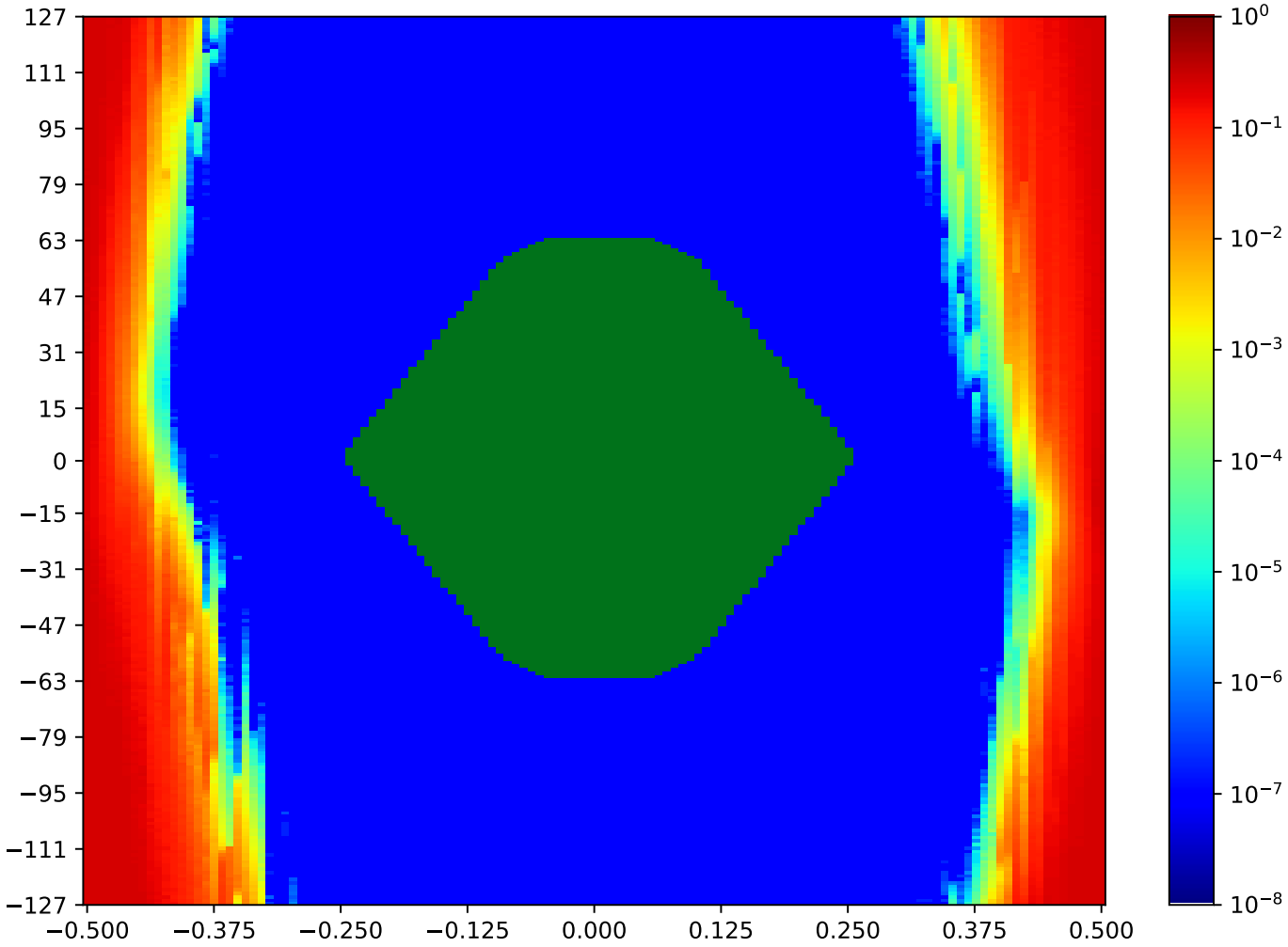


Figure 3.133: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.7 MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Table 3.124: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:05:43		2018-Sep-26 19:06:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22950	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

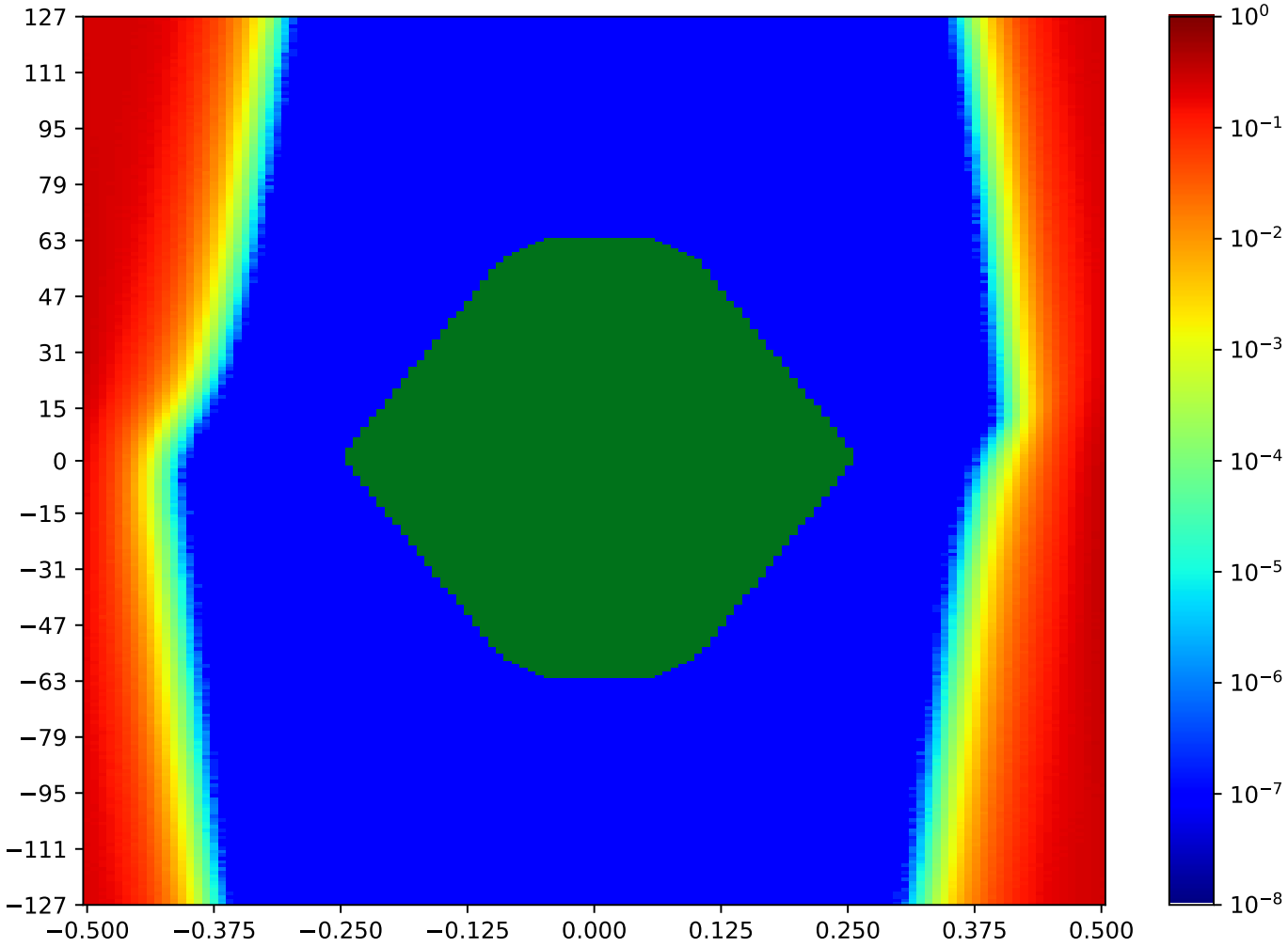


Figure 3.134: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.8 MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Table 3.125: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:54:42		2018-Sep-26 18:55:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24254	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

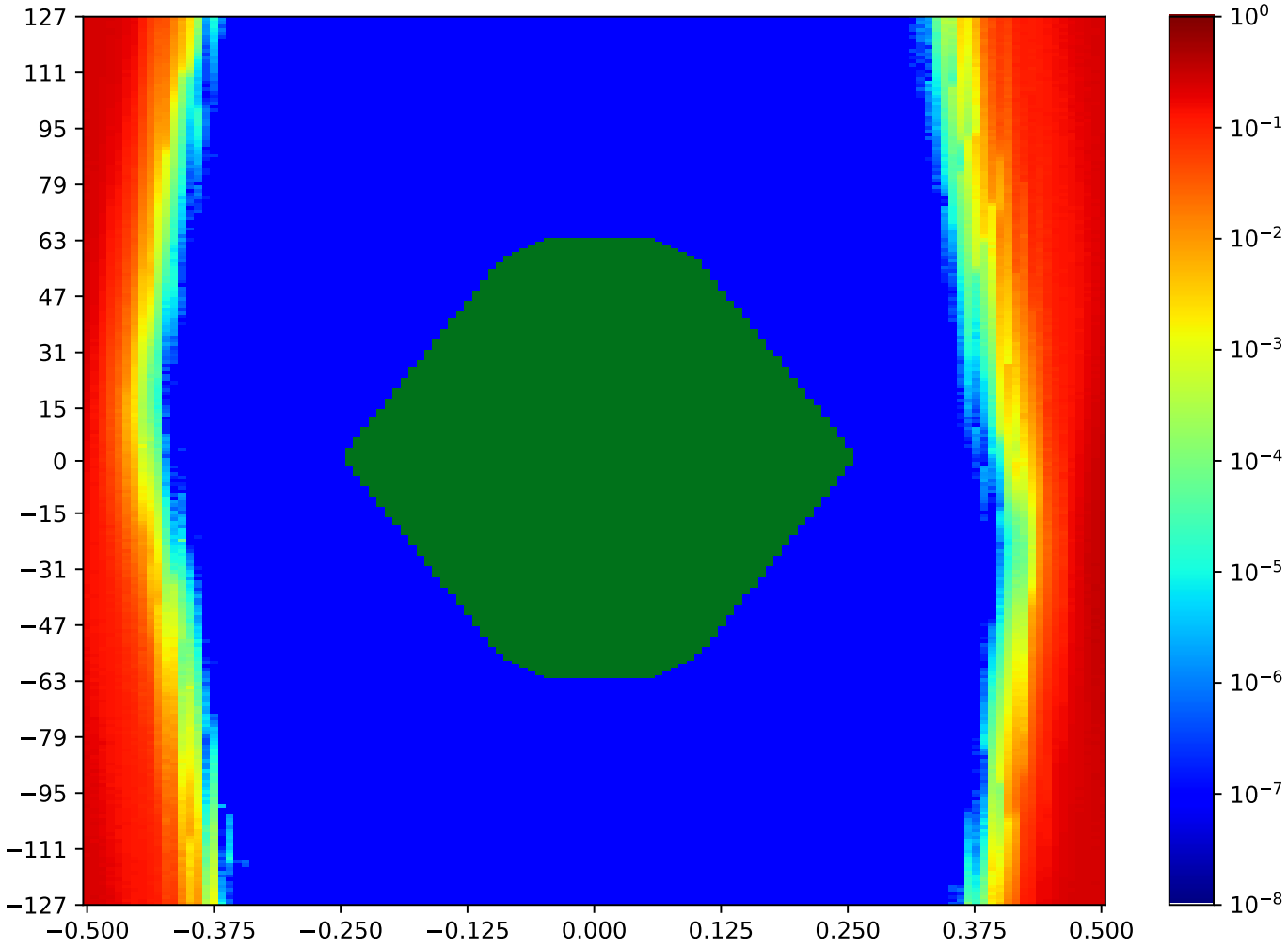


Figure 3.135: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.9 MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Table 3.126: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:04:28		2018-Sep-26 19:05:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23733	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

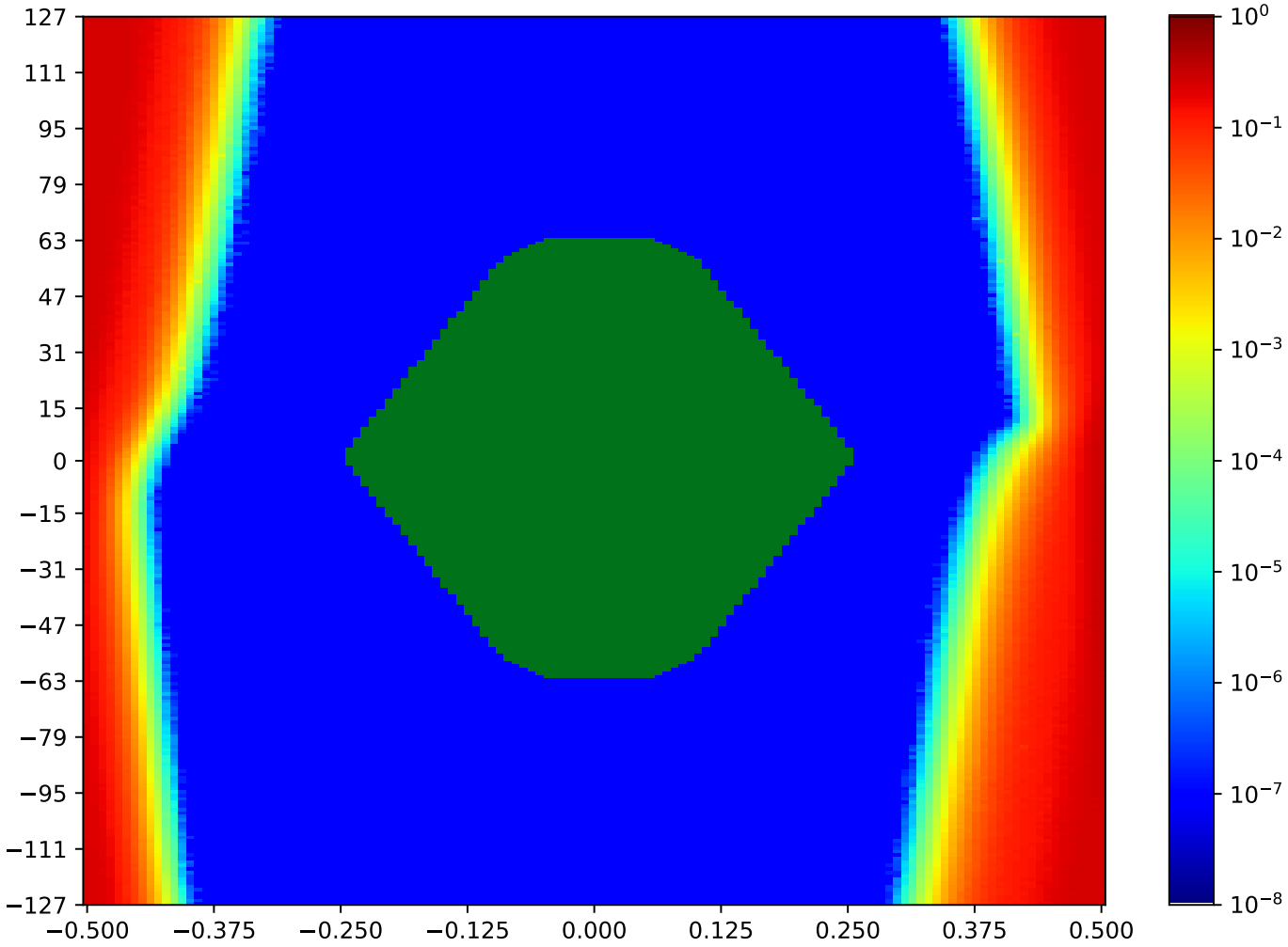


Figure 3.136: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.10 MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Table 3.127: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:57:09		2018-Sep-26 18:58:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22984	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

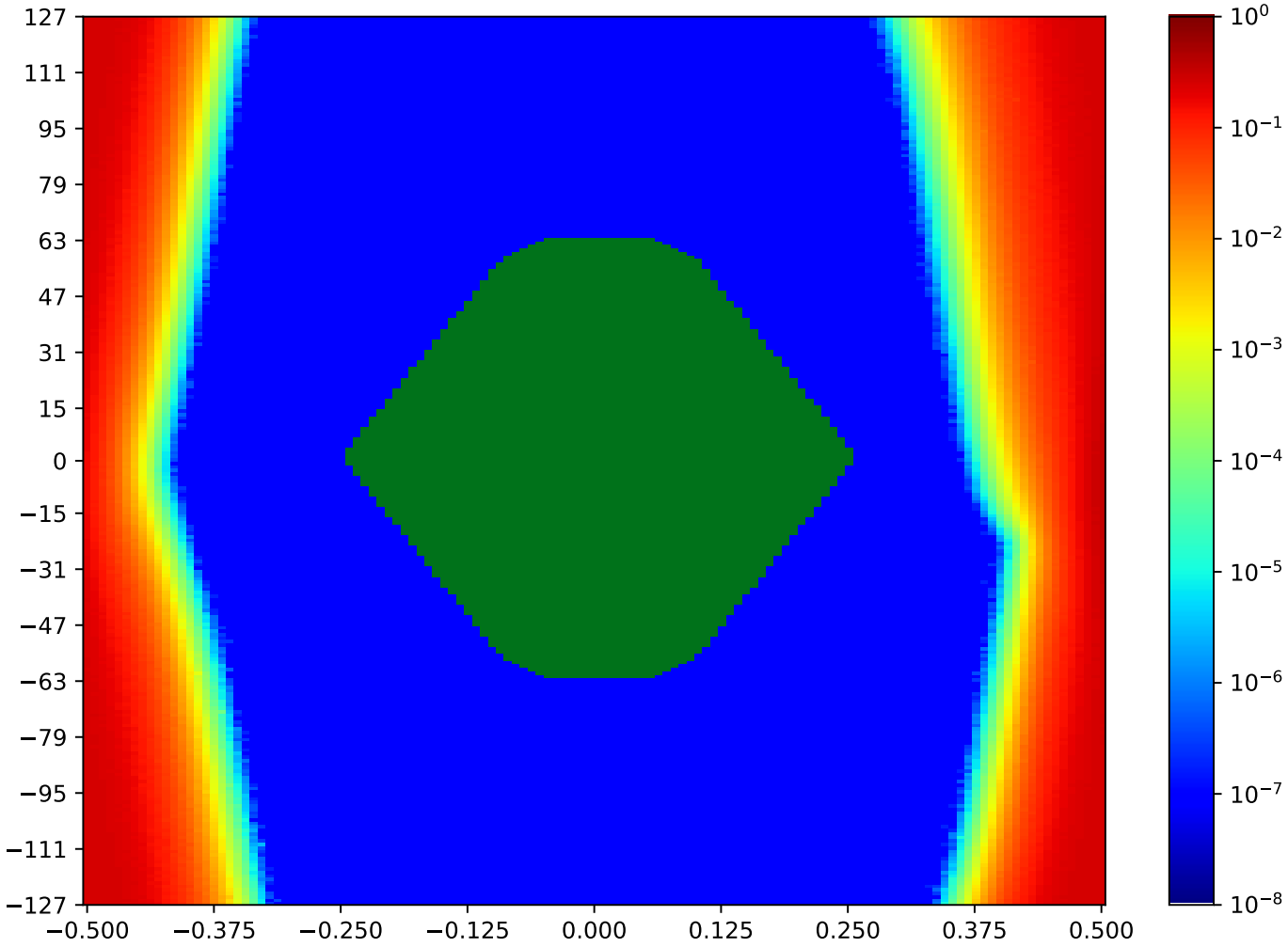


Figure 3.137: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.11 MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Table 3.128: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:02:00		2018-Sep-26 19:03:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23256	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

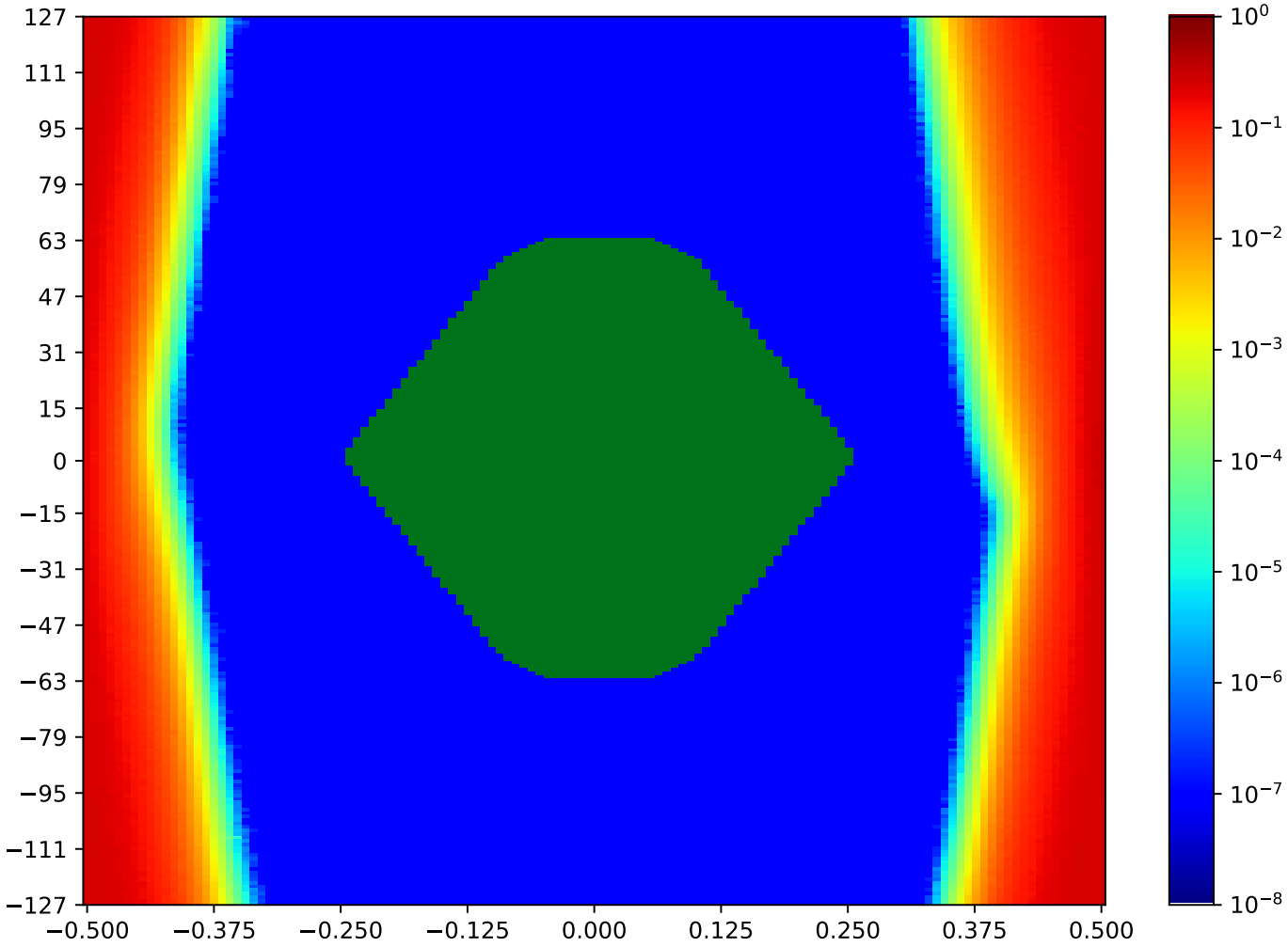


Figure 3.138: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.10.12 MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Table 3.129: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:00:47		2018-Sep-26 19:02:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23183	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

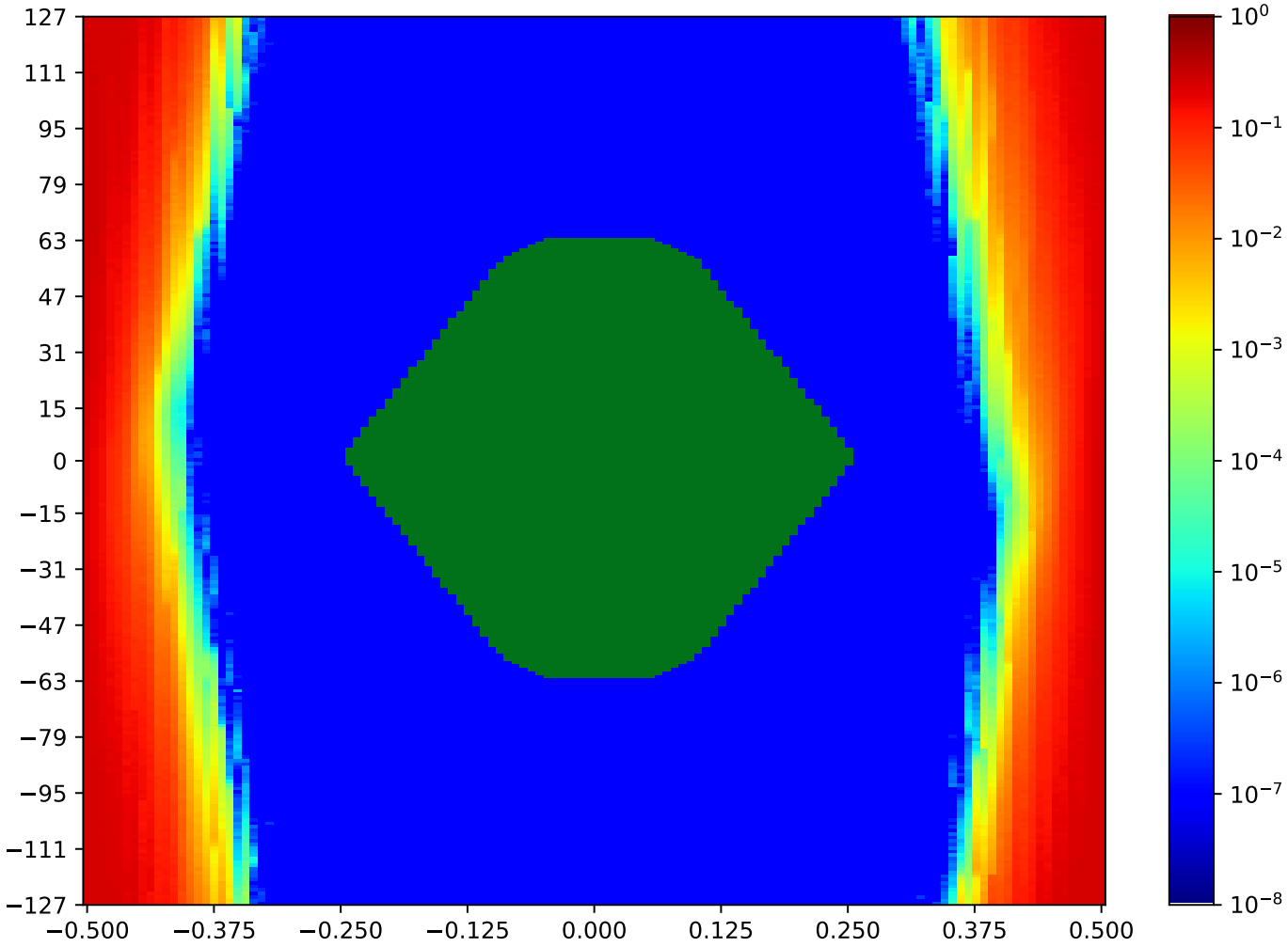


Figure 3.139: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11 MSP_A TX2 MSP_C RX18 Minipod Loopback

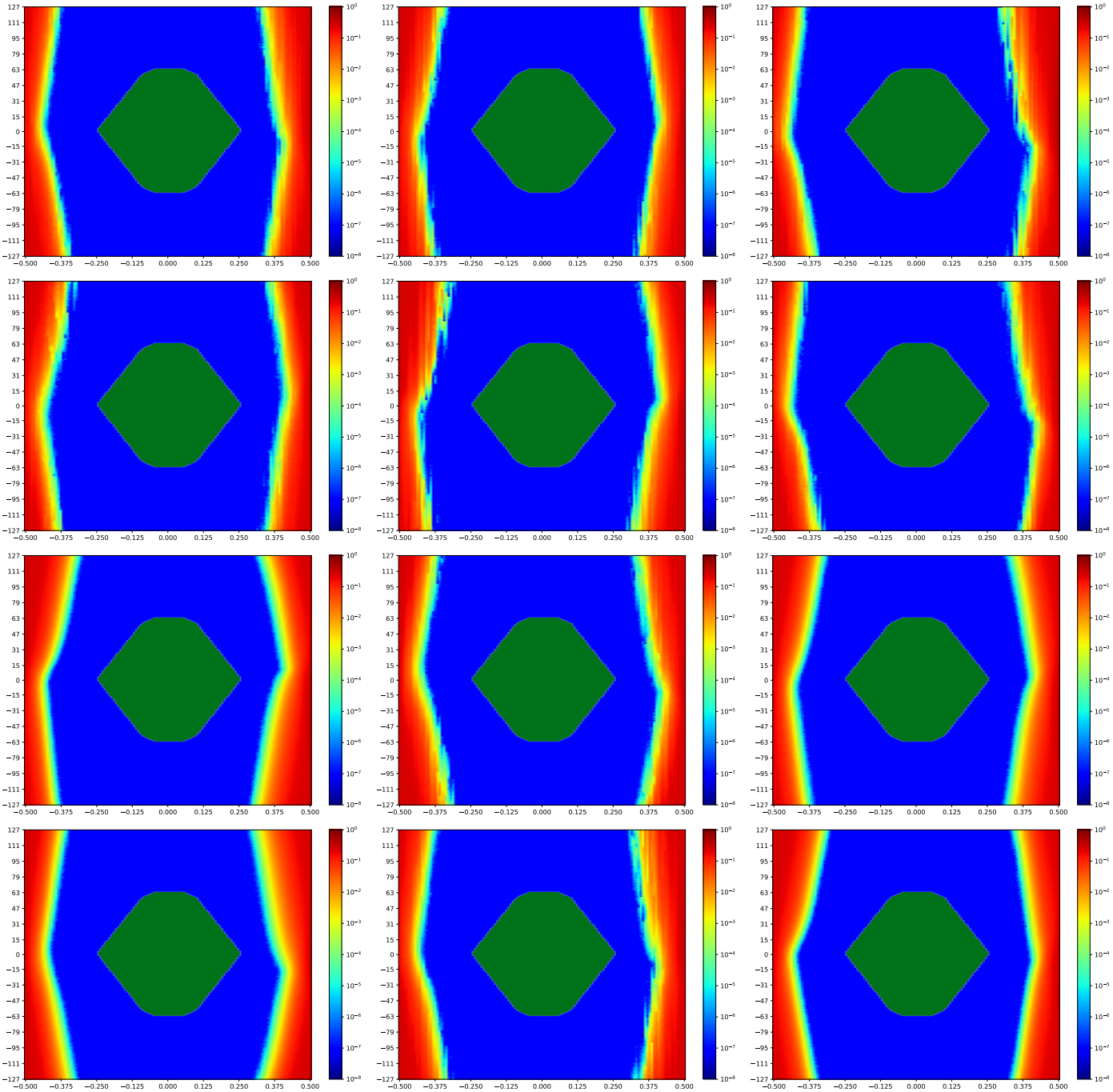


Figure 3.140: MSP_A TX2 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.153.

3.11.1 MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Table 3.130: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:10:37		2018-Sep-26 19:11:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23565	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

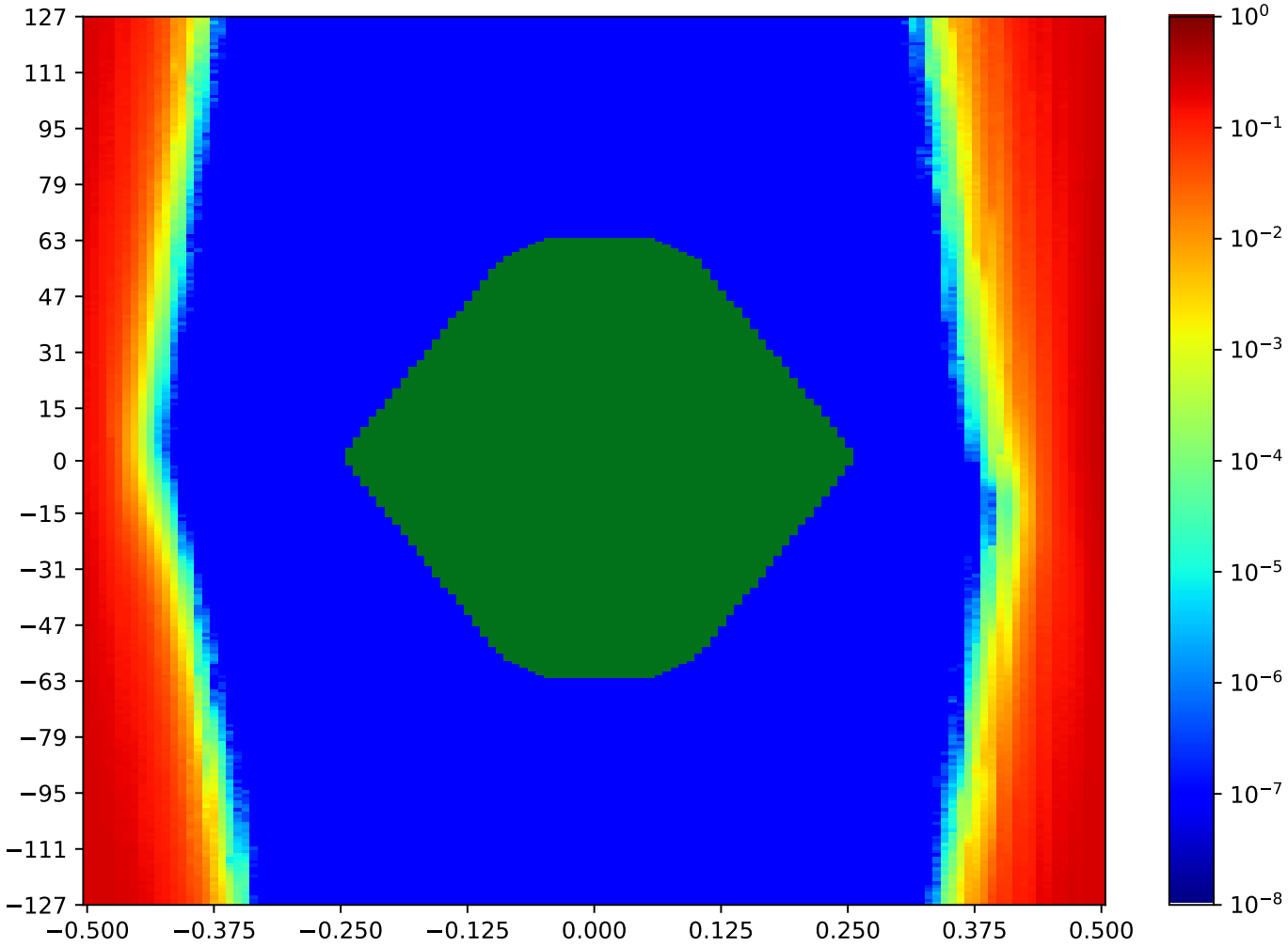


Figure 3.141: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.2 MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Table 3.131: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:08:10		2018-Sep-26 19:09:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23712	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

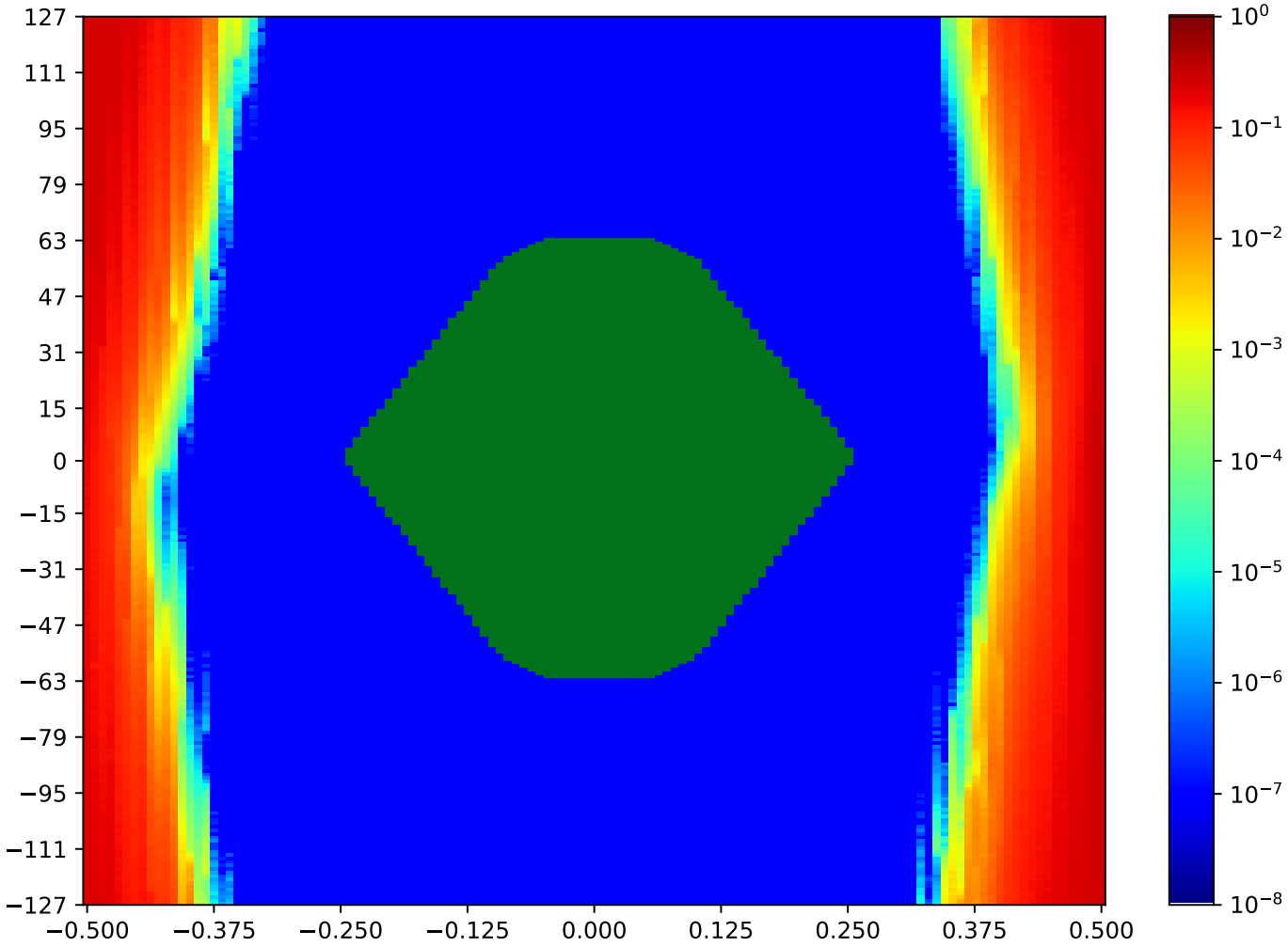


Figure 3.142: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.3 MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Table 3.132: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:14:17		2018-Sep-26 19:15:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23326	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

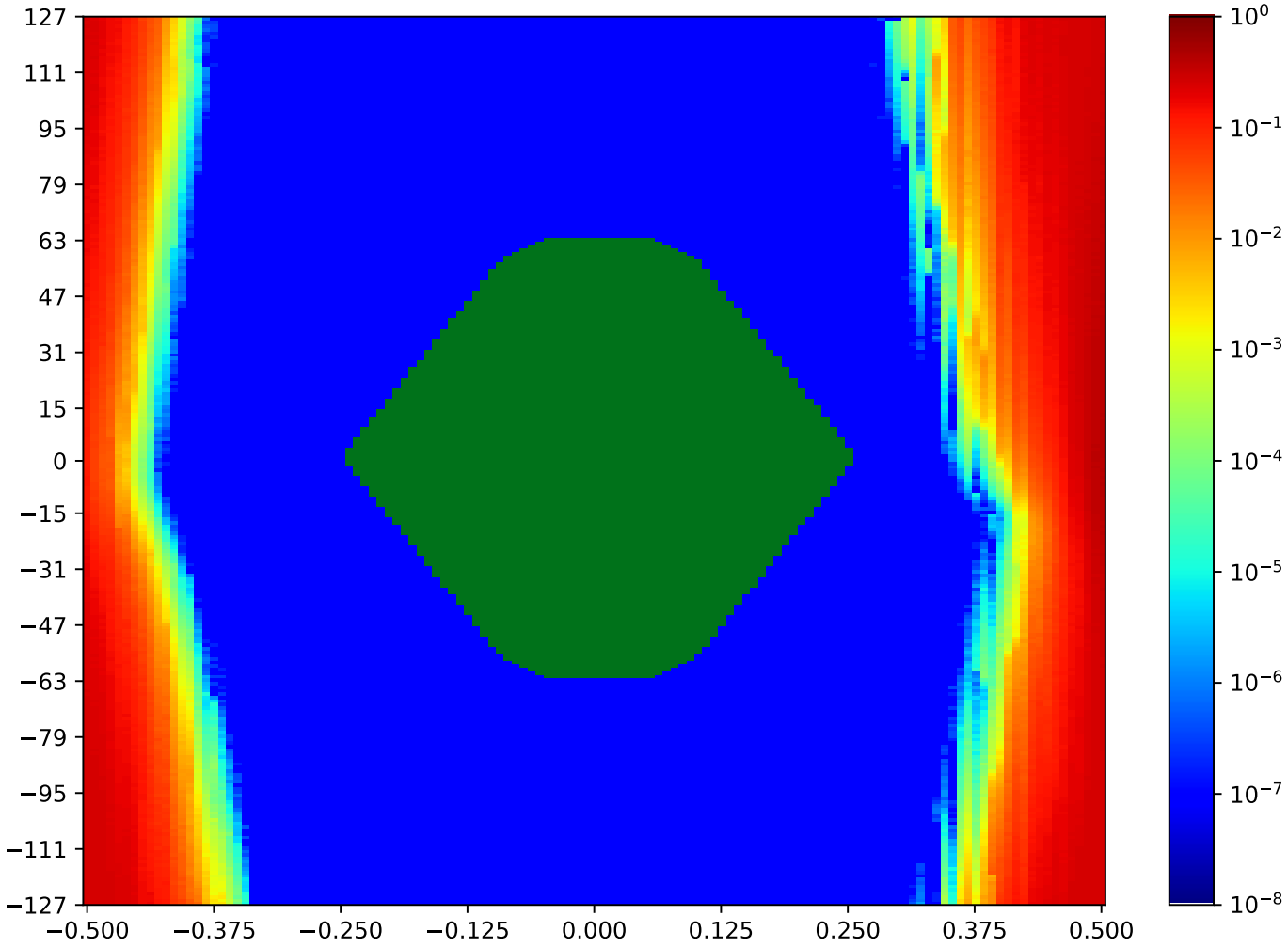


Figure 3.143: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.4 MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Table 3.133: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:06:56		2018-Sep-26 19:08:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23679	102	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

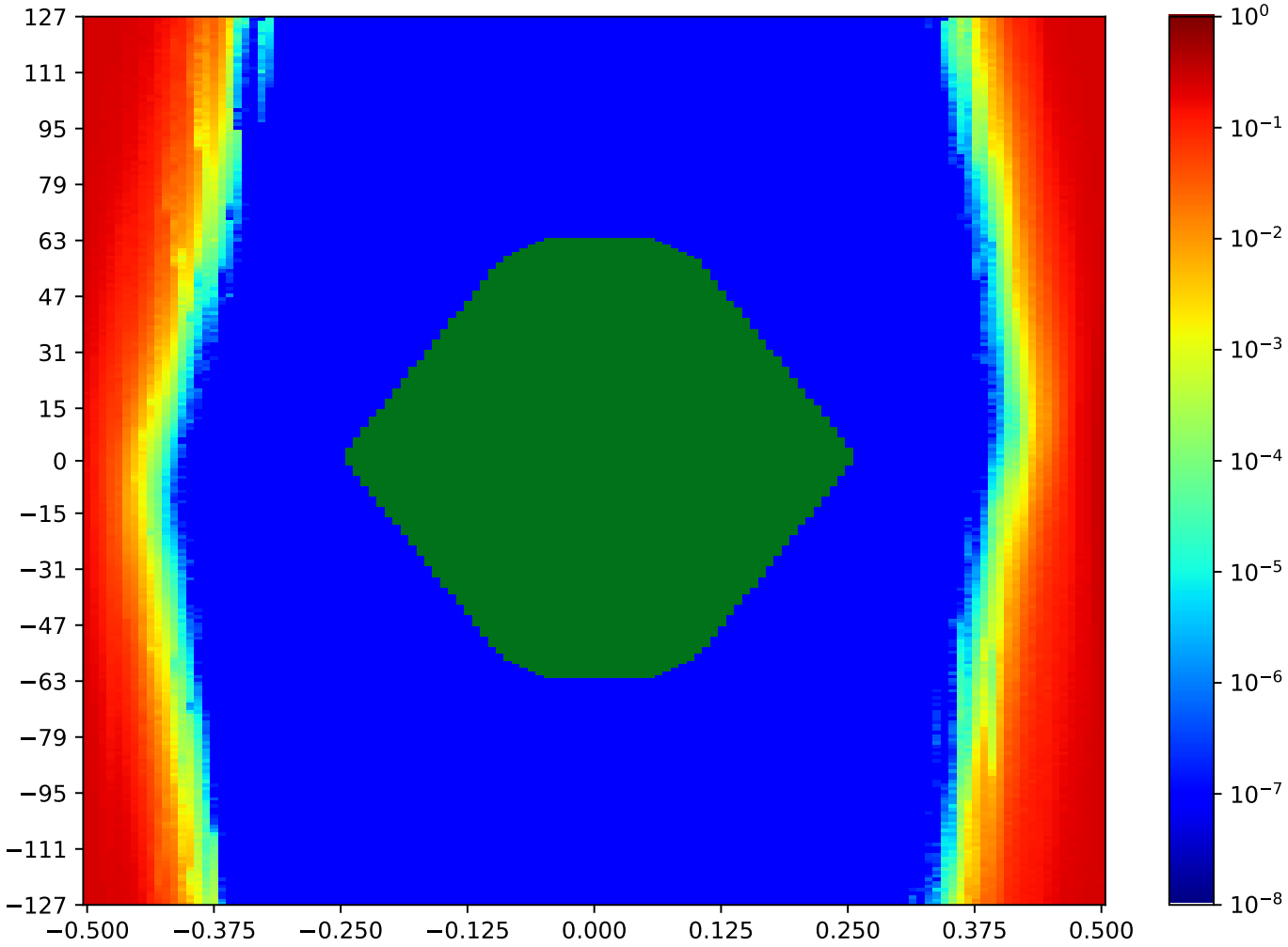


Figure 3.144: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.5 MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Table 3.134: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:17:58		2018-Sep-26 19:19:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23262	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

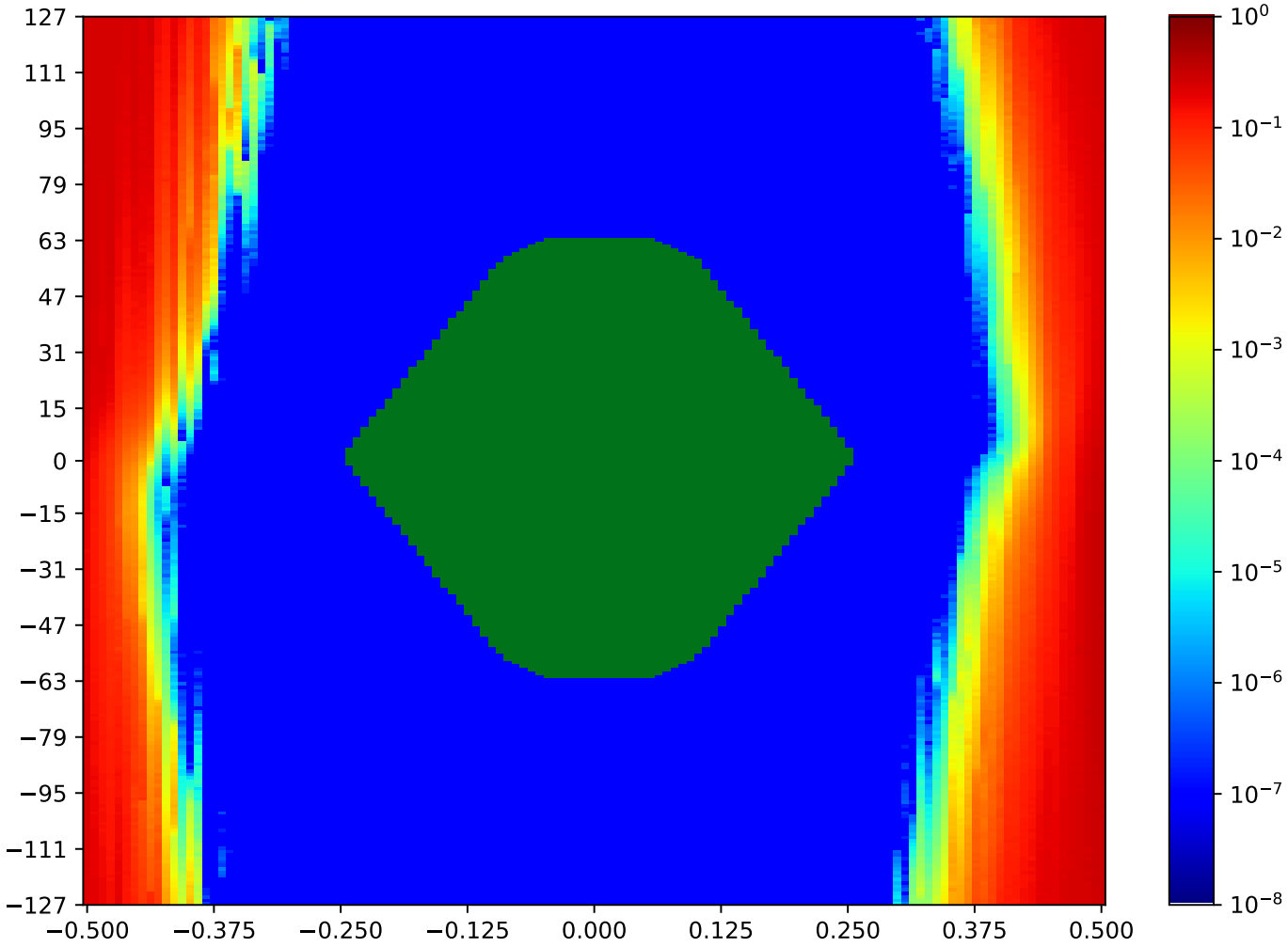


Figure 3.145: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.6 MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Table 3.135: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:09:23		2018-Sep-26 19:10:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23670	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

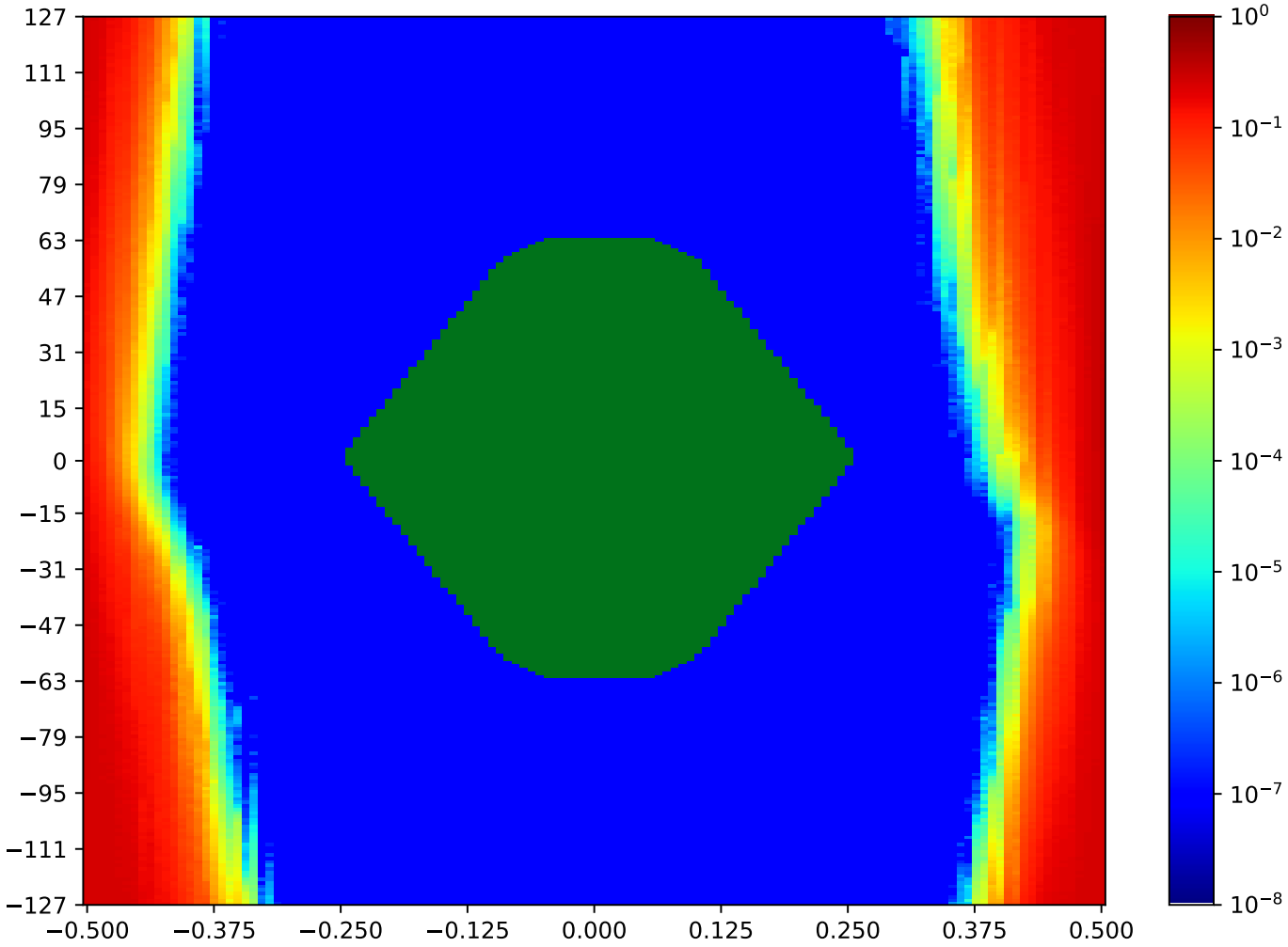


Figure 3.146: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.7 MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Table 3.136: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:20:24		2018-Sep-26 19:21:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22712	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

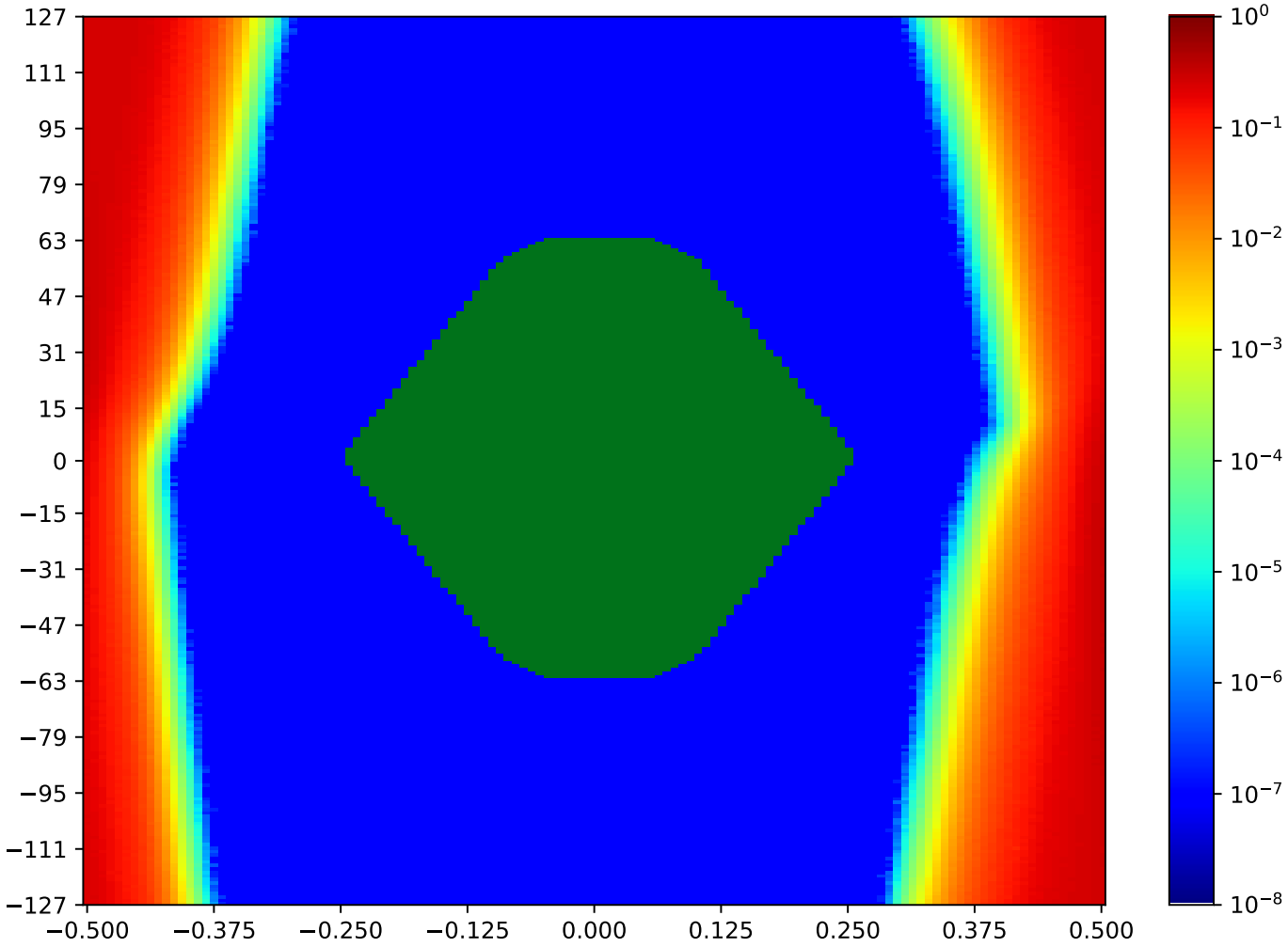


Figure 3.147: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.8 MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Table 3.137: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:11:50		2018-Sep-26 19:13:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23048	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

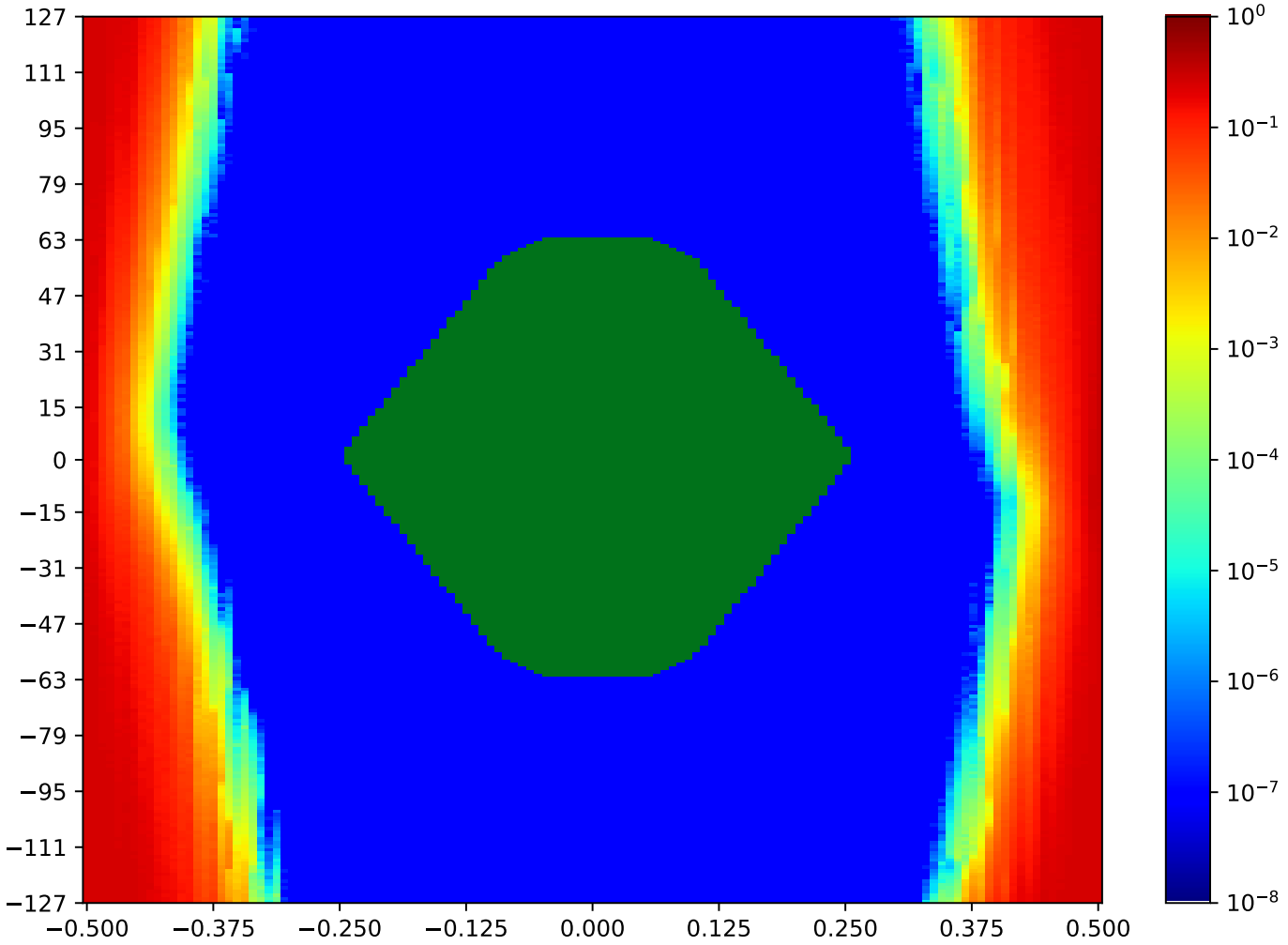


Figure 3.148: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.9 MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Table 3.138: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:19:11		2018-Sep-26 19:20:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22838	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

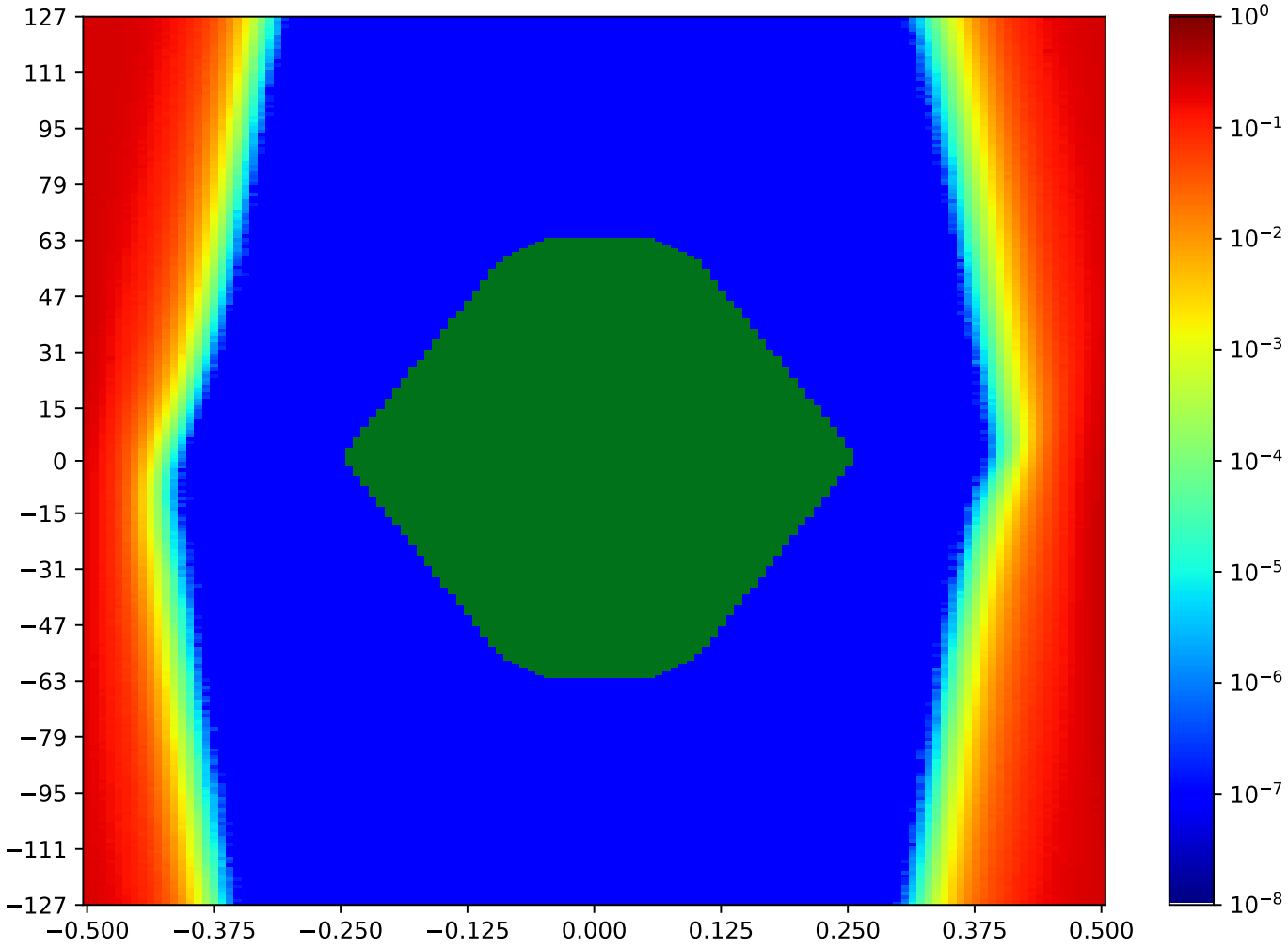


Figure 3.149: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.10 MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Table 3.139: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:13:04		2018-Sep-26 19:14:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22490	95	73.64%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

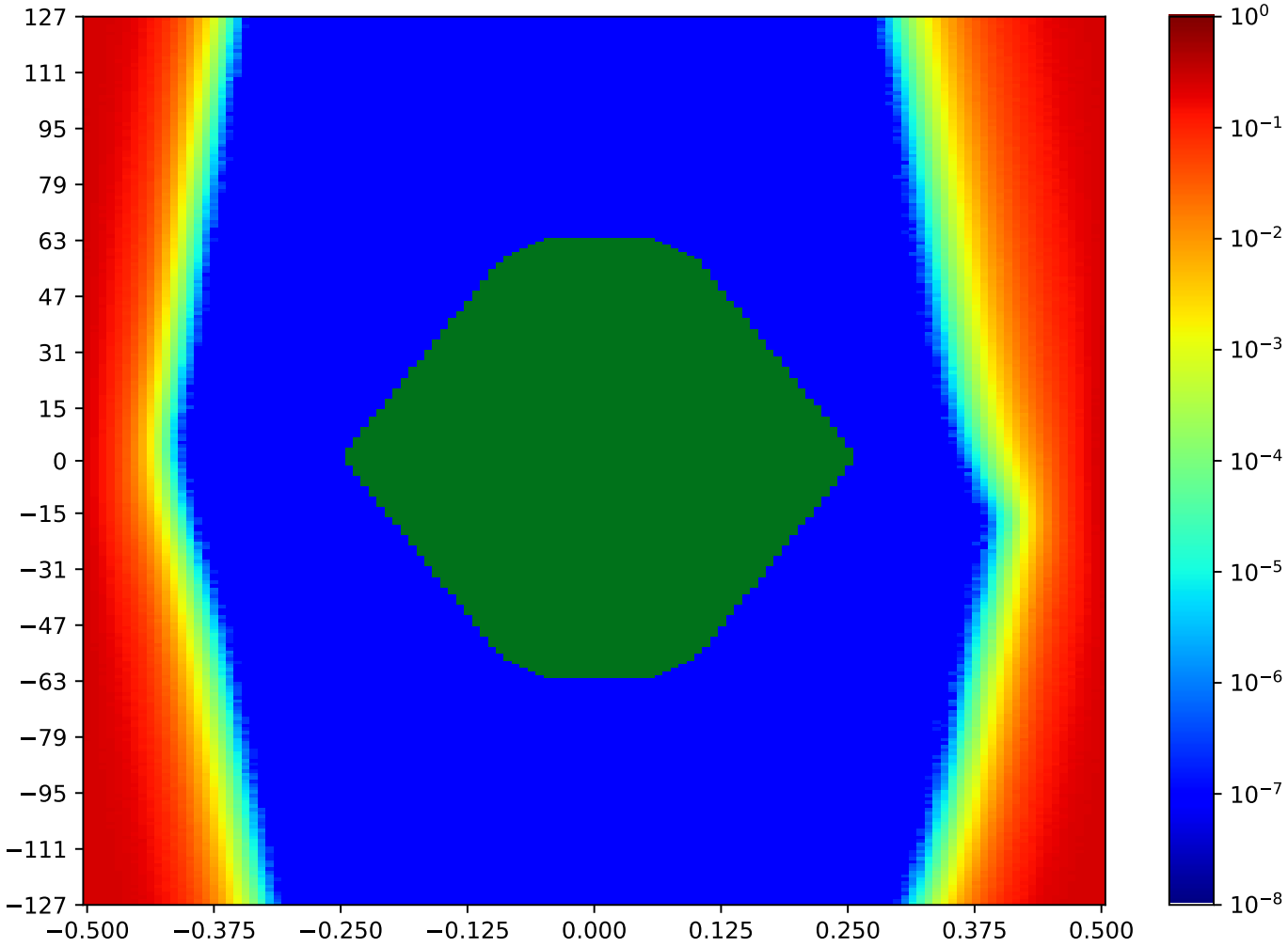


Figure 3.150: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.11 MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Table 3.140: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:16:44		2018-Sep-26 19:17:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23129	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

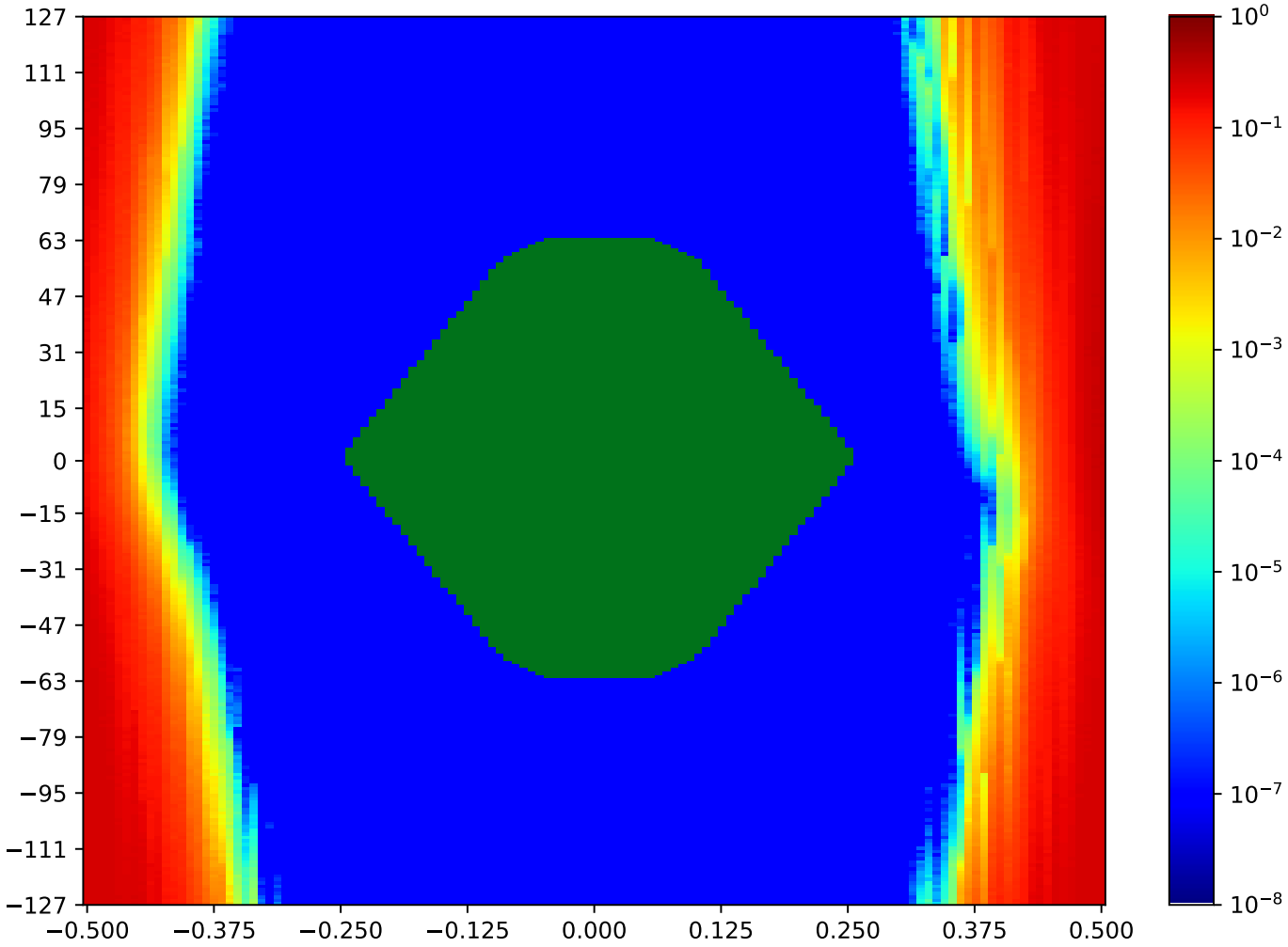


Figure 3.151: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.11.12 MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Table 3.141: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:15:31		2018-Sep-26 19:16:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23312	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

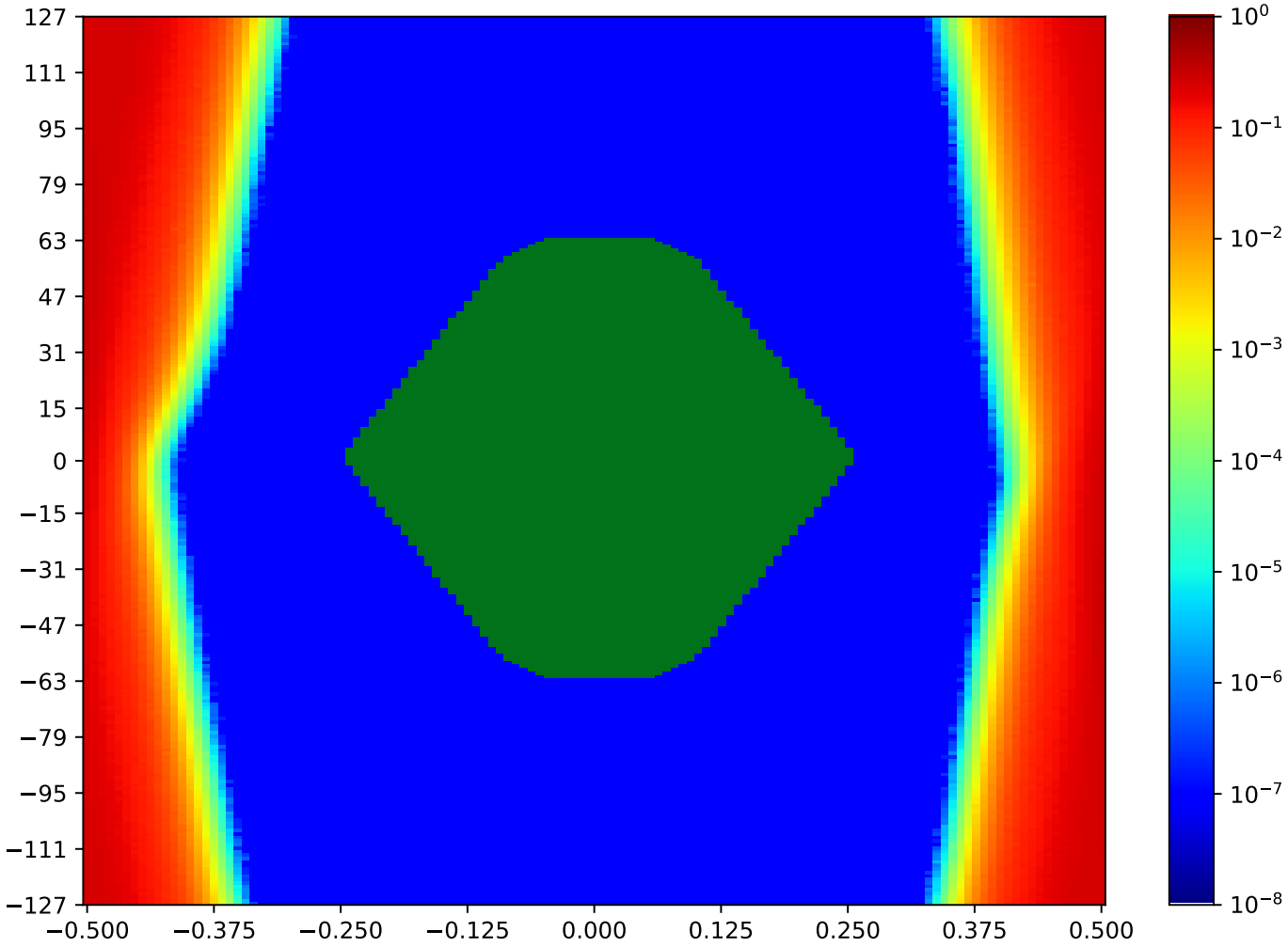


Figure 3.152: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12 MSP_C TX3 MSP_A RX8 Minipod Loopback

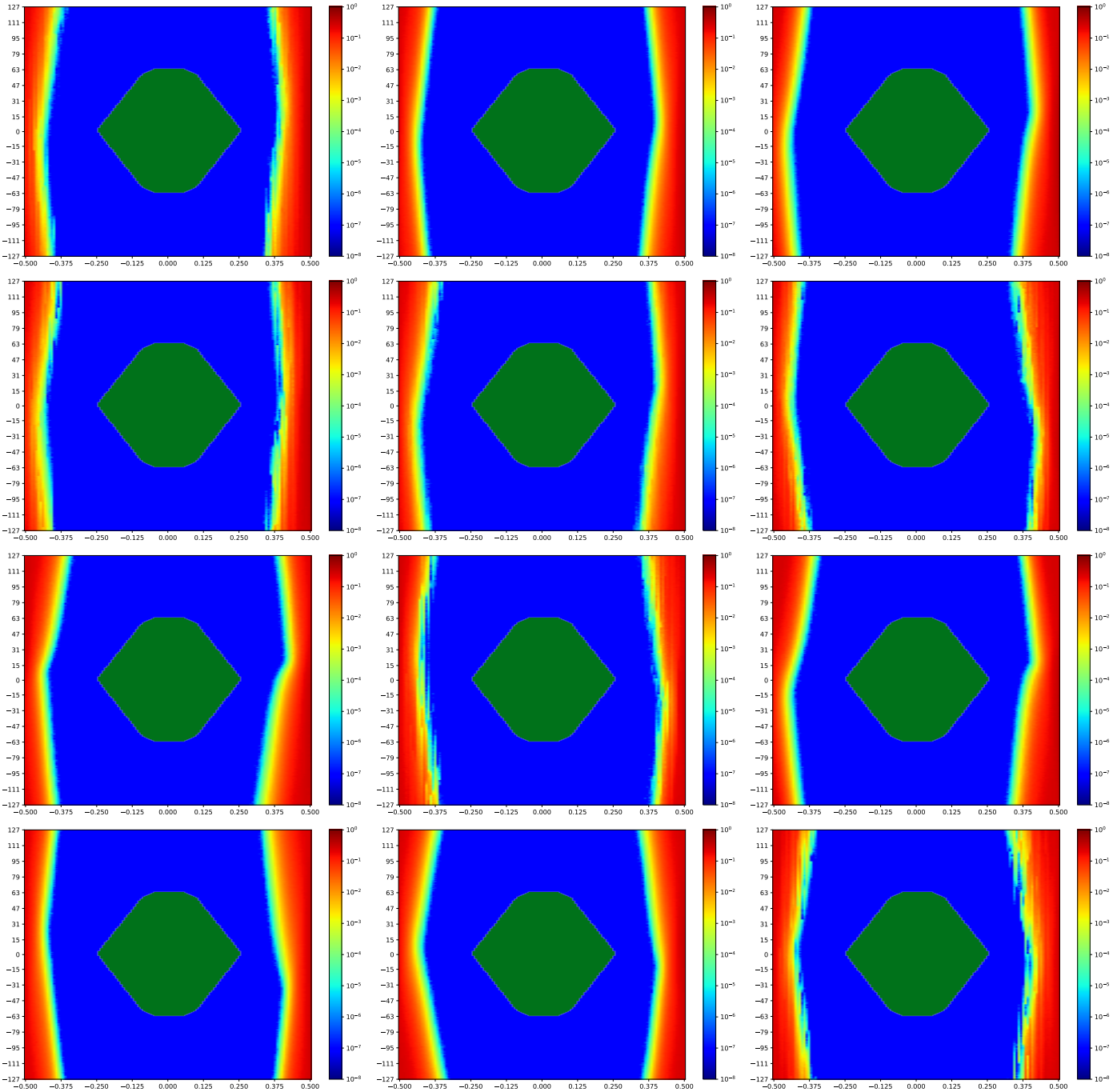


Figure 3.153: MSP_C TX3 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.166.

3.12.1 MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Table 3.142: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:25:23		2018-Sep-26 19:26:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24408	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

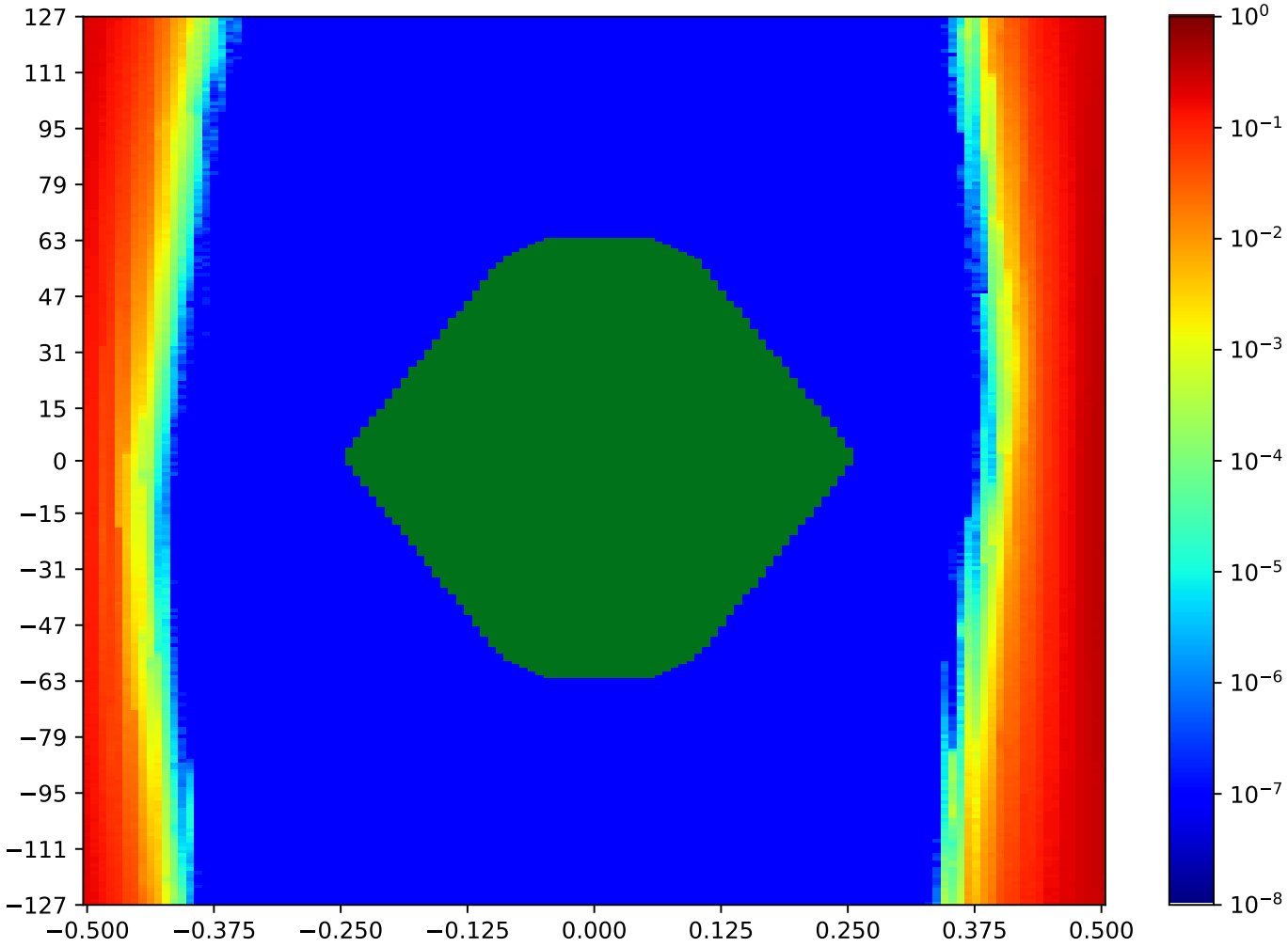


Figure 3.154: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.2 MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Table 3.143: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:27:53		2018-Sep-26 19:29:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24641	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

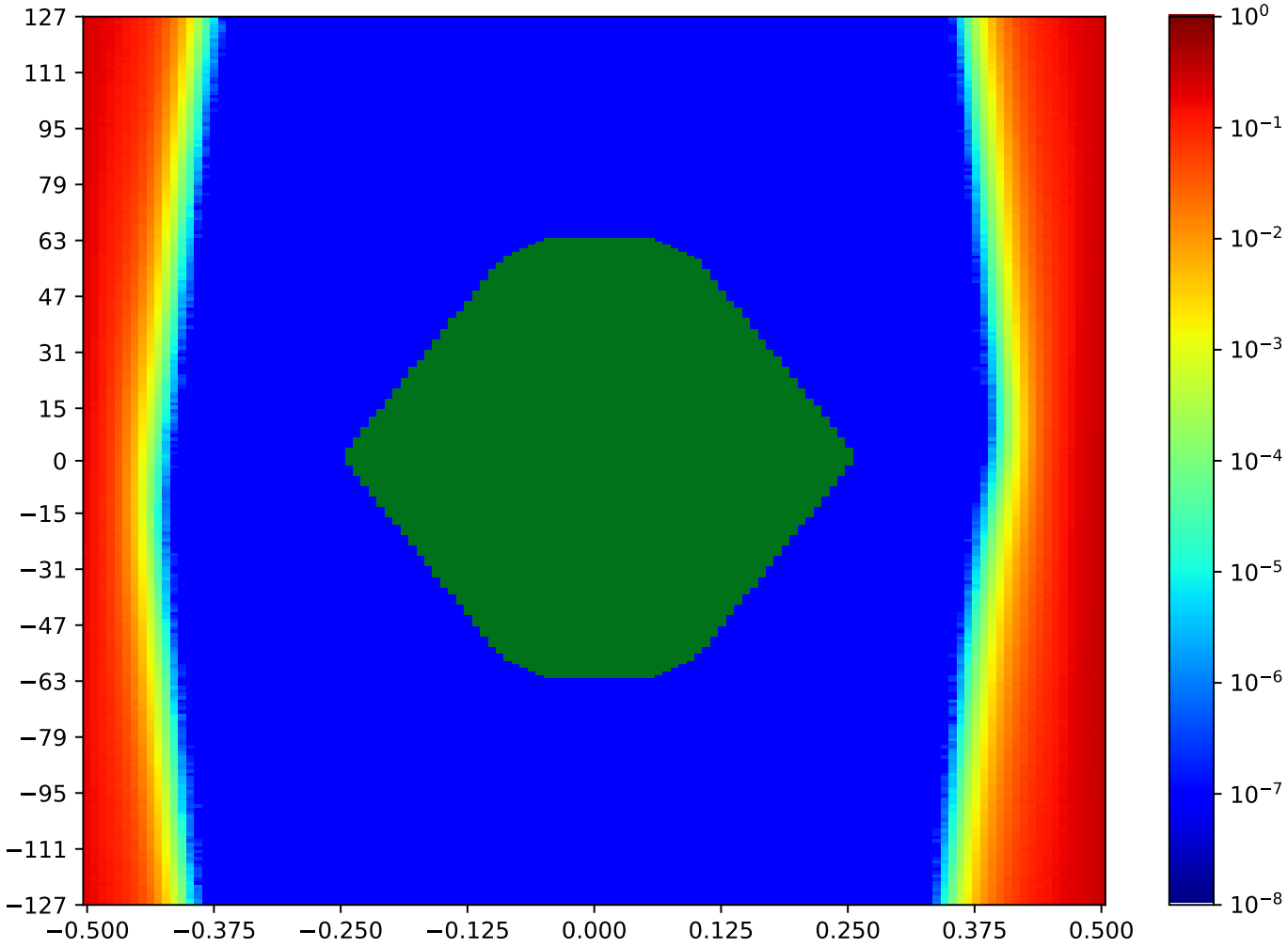


Figure 3.155: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.3 MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Table 3.144: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:29:08		2018-Sep-26 19:30:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24652	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

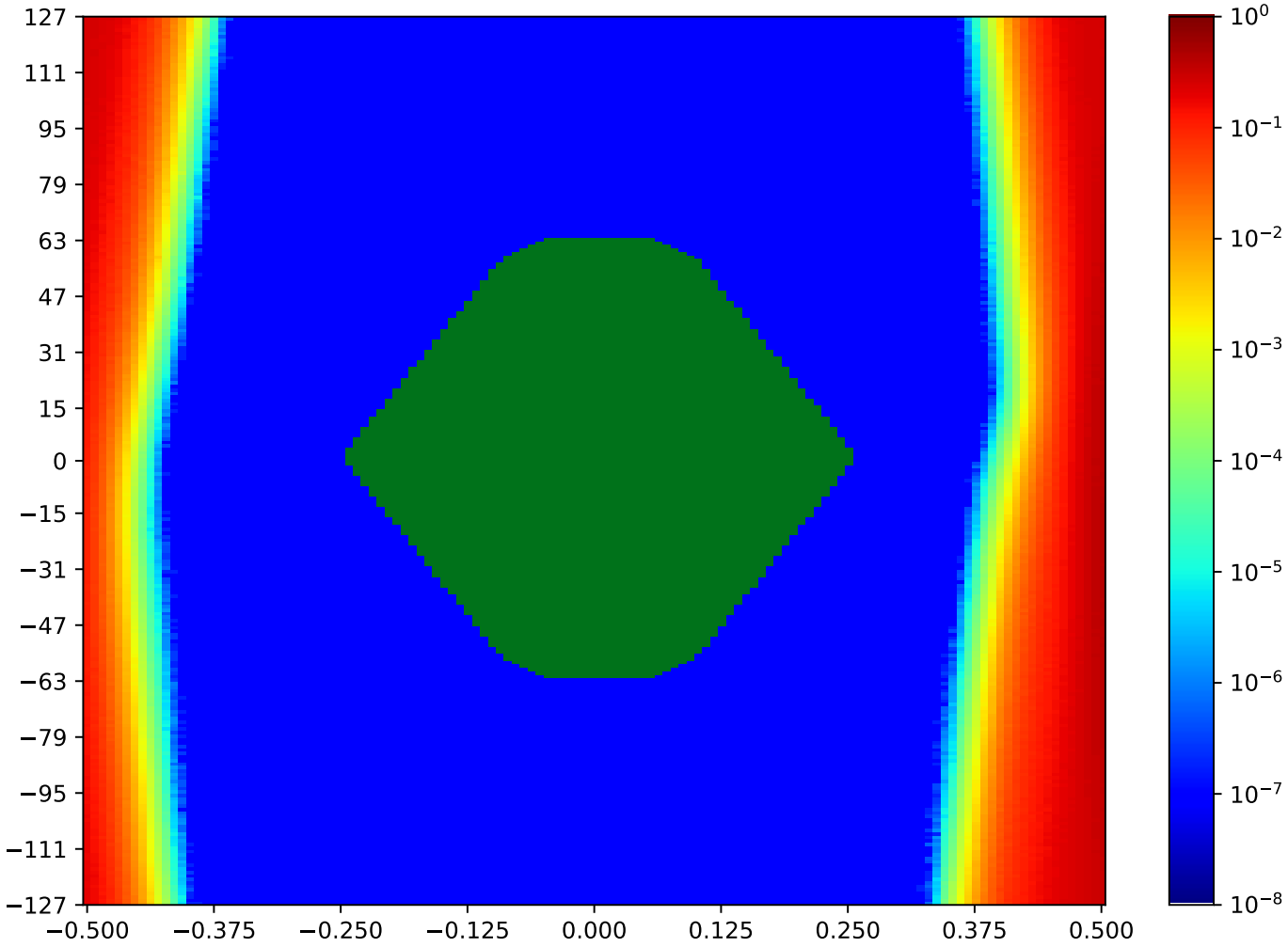


Figure 3.156: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.4 MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Table 3.145: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:22:53		2018-Sep-26 19:24:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24709	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

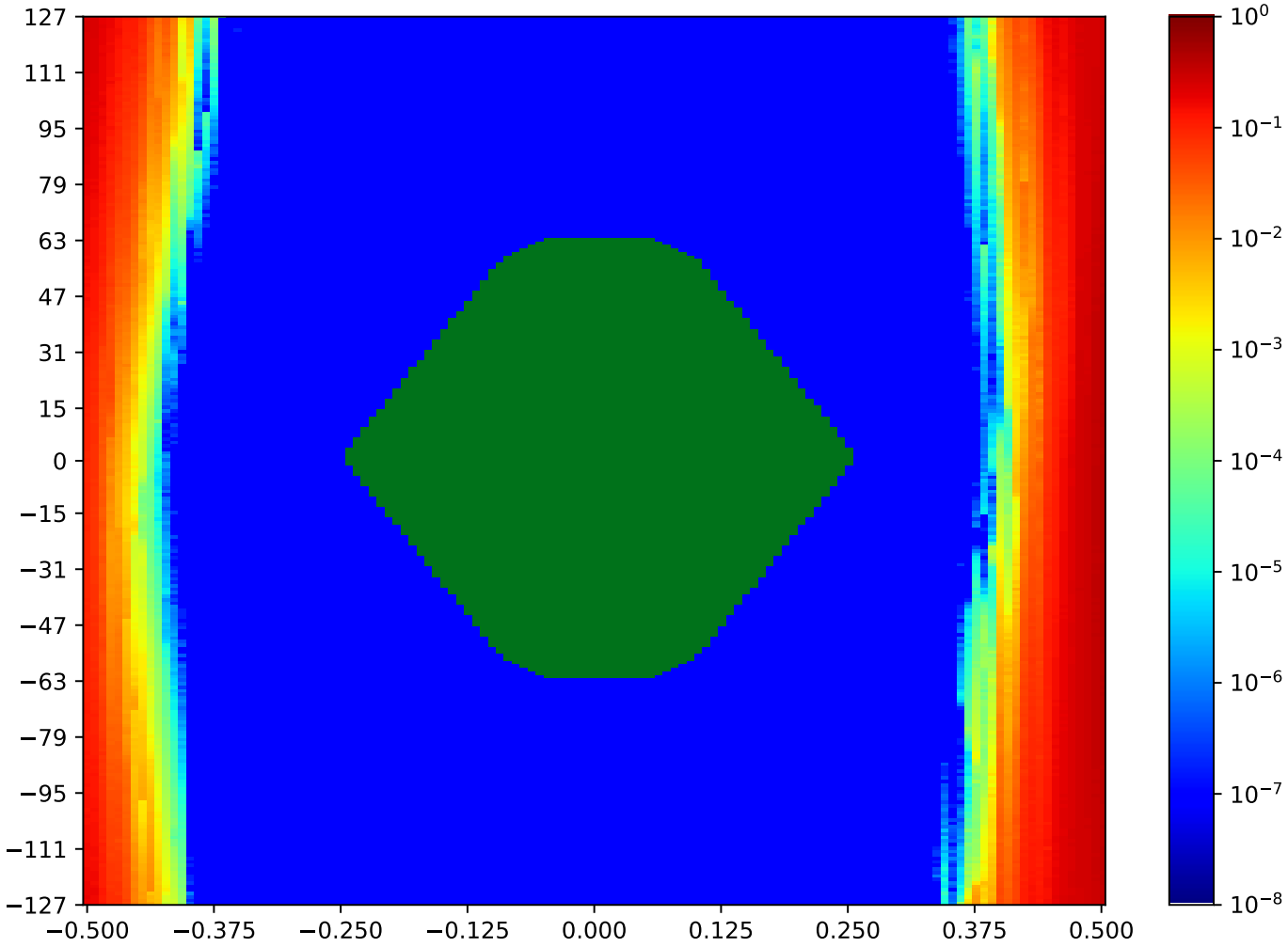


Figure 3.157: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.5 MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Table 3.146: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:32:51		2018-Sep-26 19:34:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24249	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

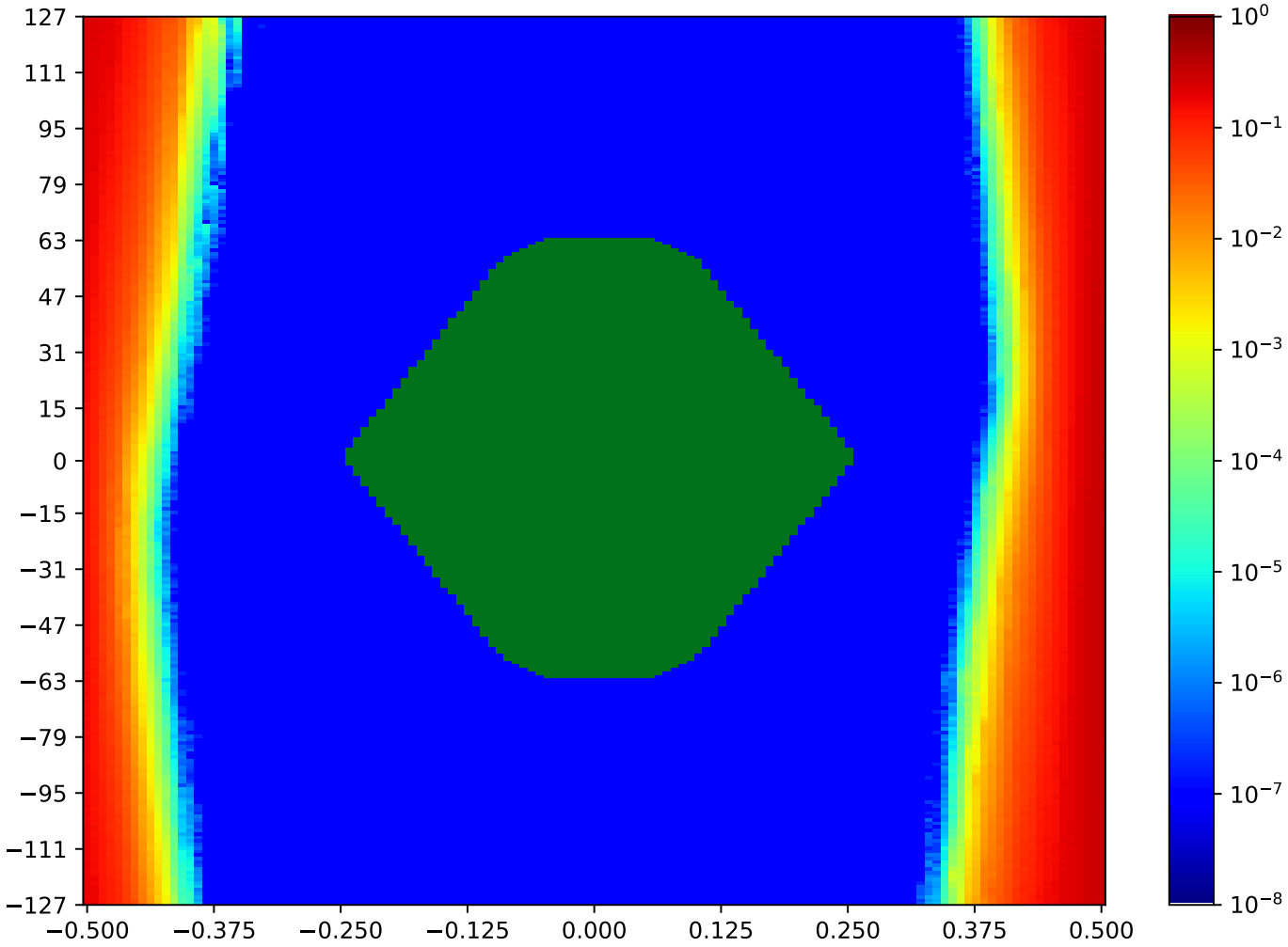


Figure 3.158: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.6 MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Table 3.147: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:21:37		2018-Sep-26 19:22:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24870	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

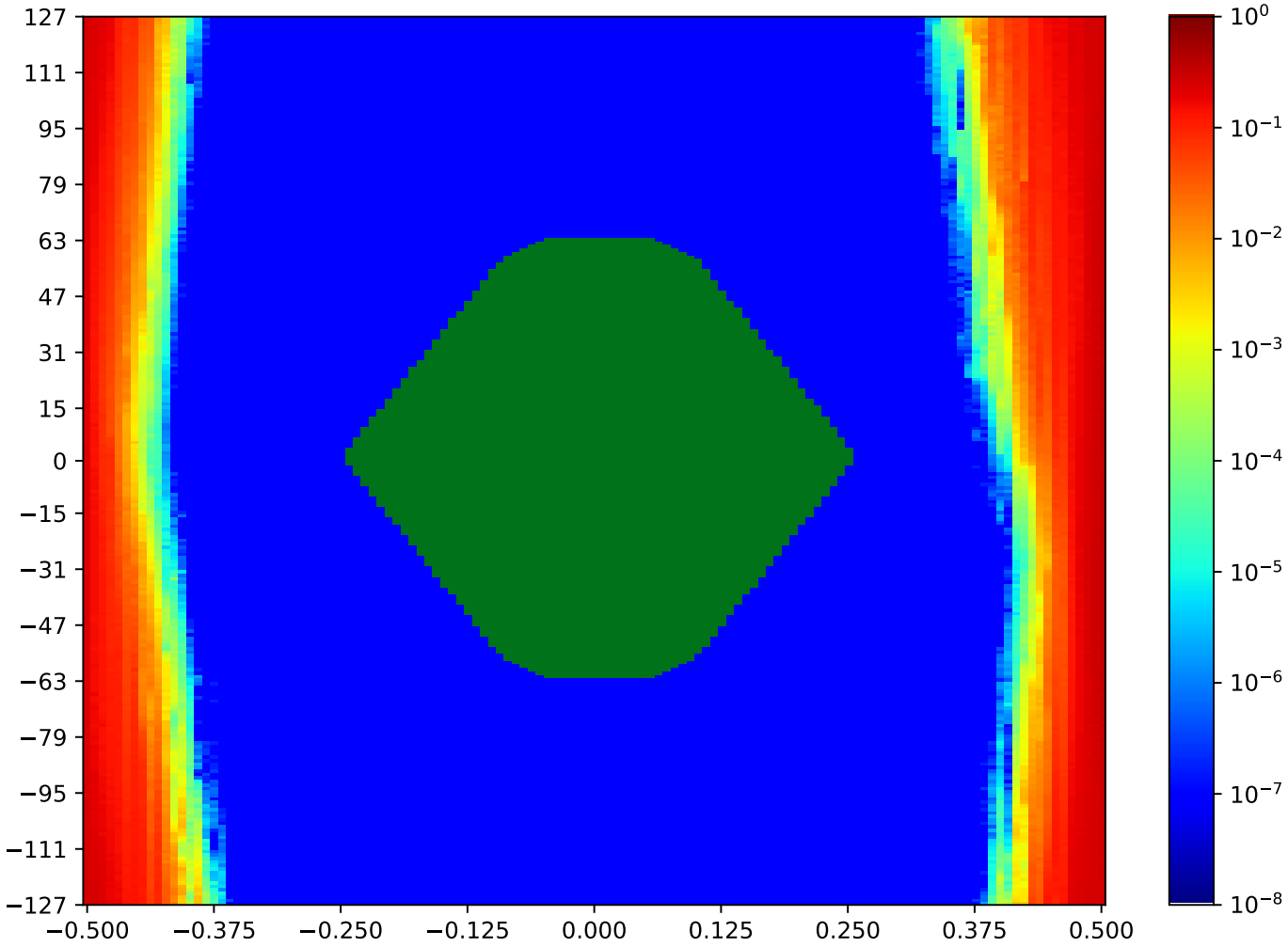


Figure 3.159: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.7 MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Table 3.148: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:35:20		2018-Sep-26 19:36:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23838	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

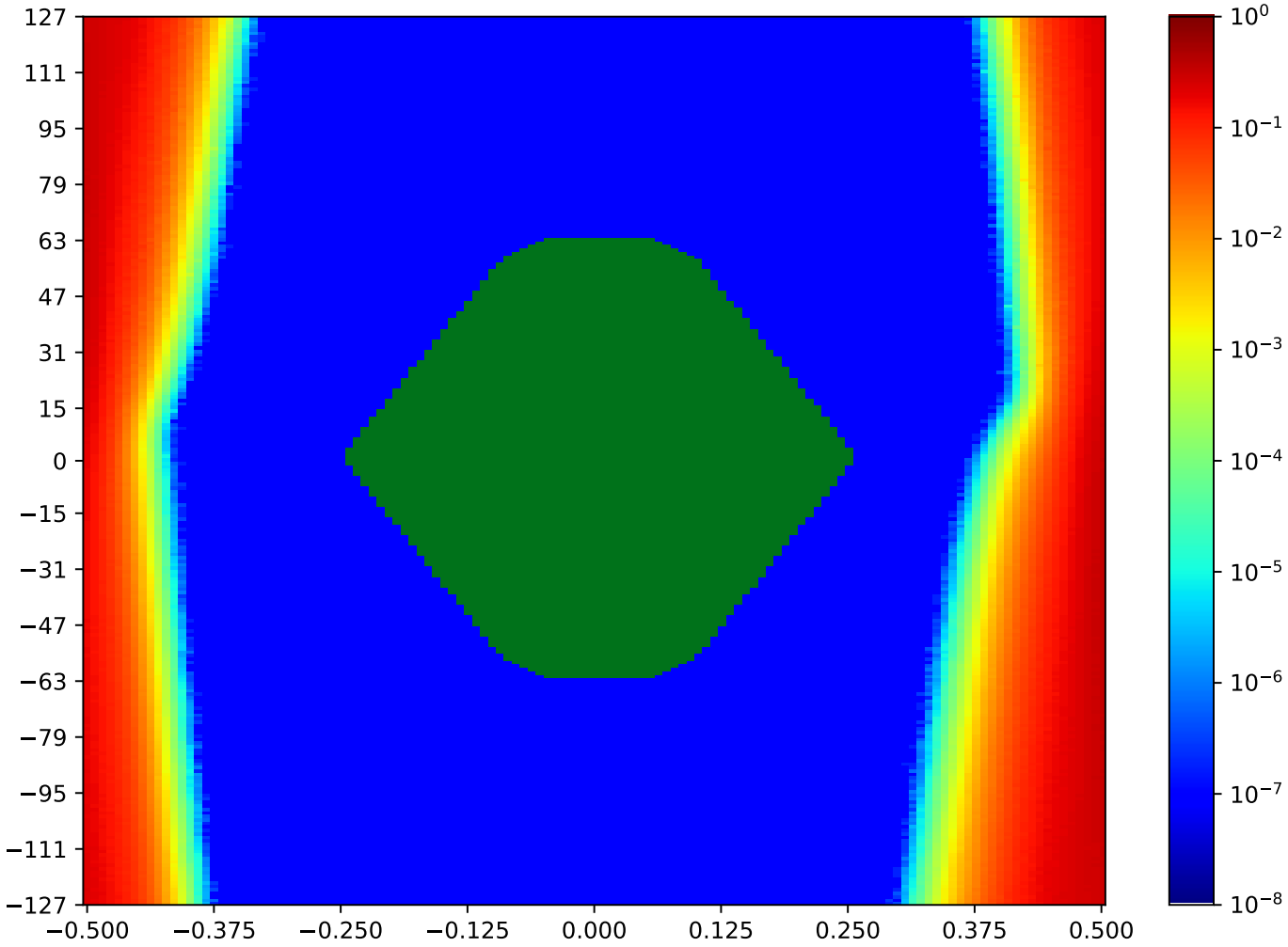


Figure 3.160: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.8 MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Table 3.149: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:24:08		2018-Sep-26 19:25:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24542	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

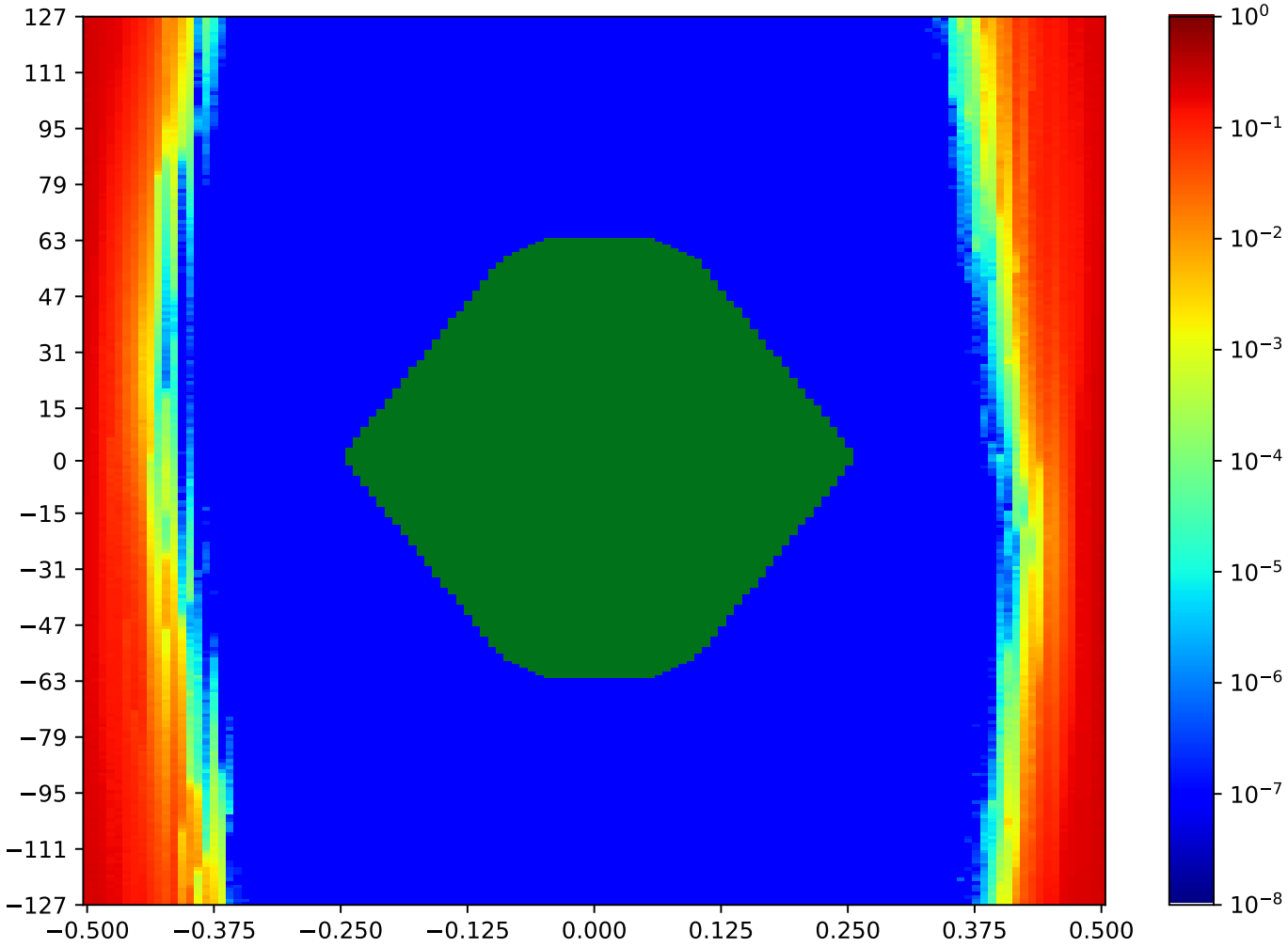


Figure 3.161: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.9 MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Table 3.150: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:34:06		2018-Sep-26 19:35:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23939	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

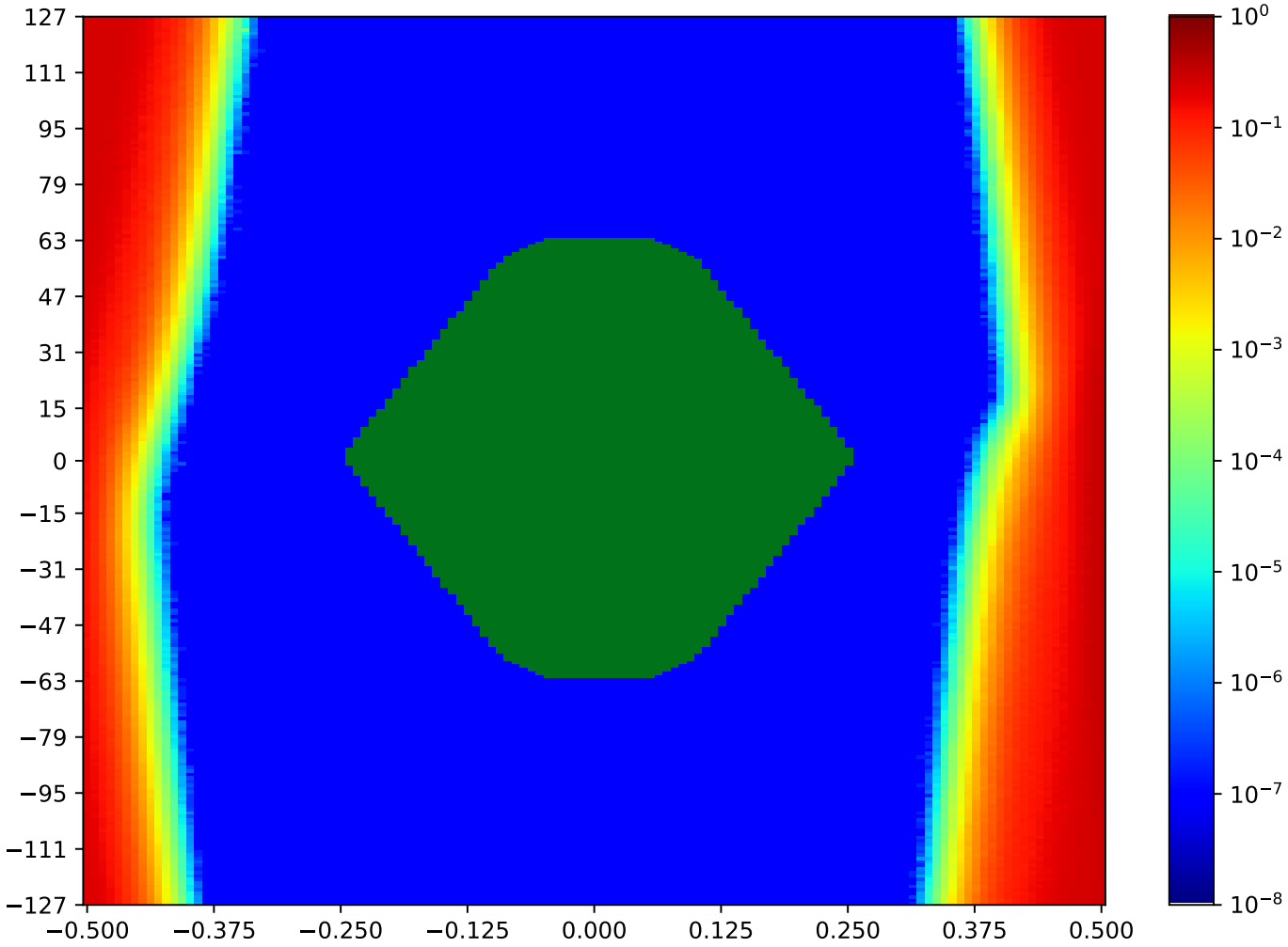


Figure 3.162: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.10 MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Table 3.151: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:26:39		2018-Sep-26 19:27:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24312	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

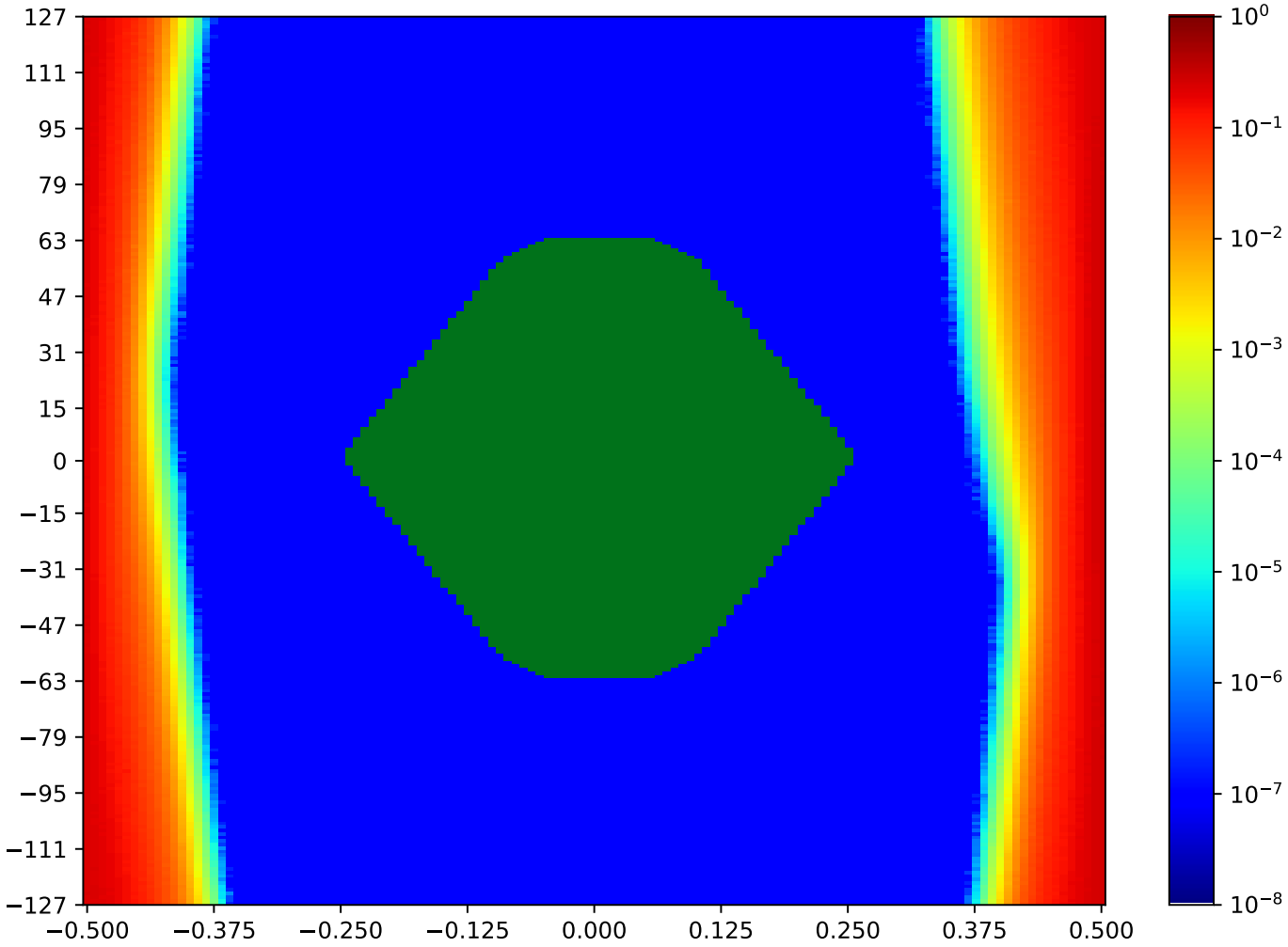


Figure 3.163: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.11 MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Table 3.152: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:31:37		2018-Sep-26 19:32:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23773	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

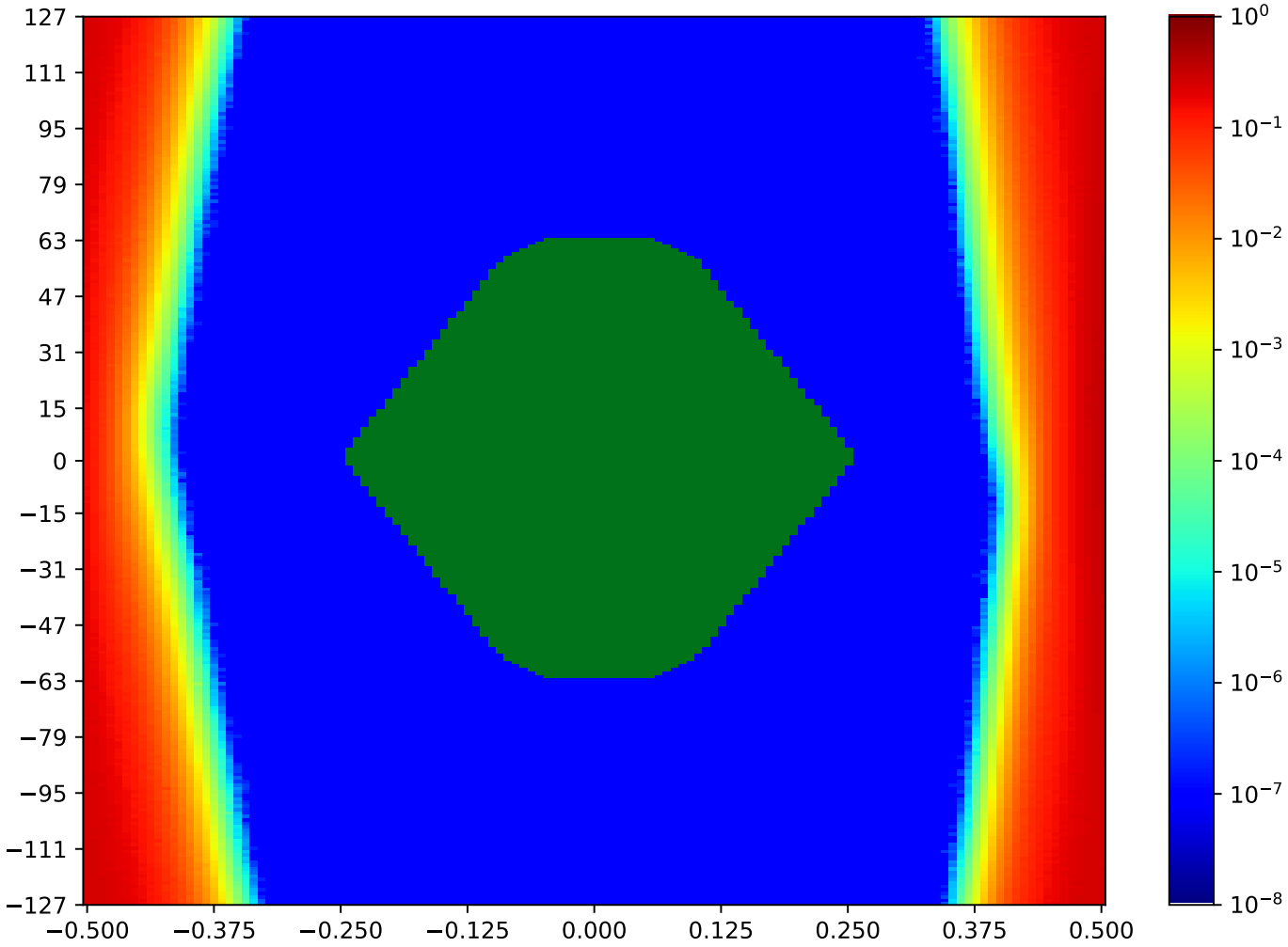


Figure 3.164: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.12.12 MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Table 3.153: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:30:23		2018-Sep-26 19:31:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23812	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

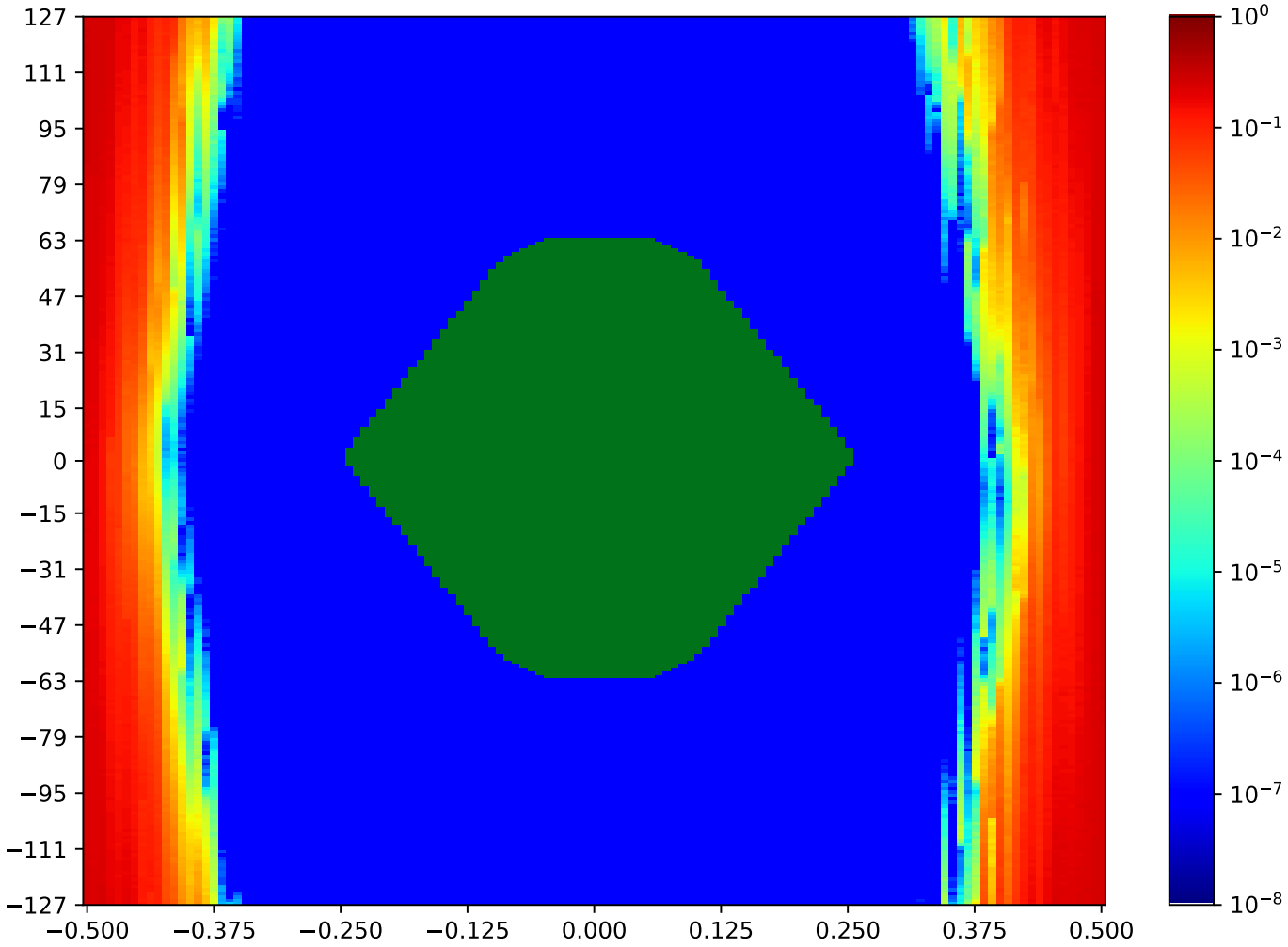


Figure 3.165: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13 MSP_C TX4 MSP_A RX9 Minipod Loopback

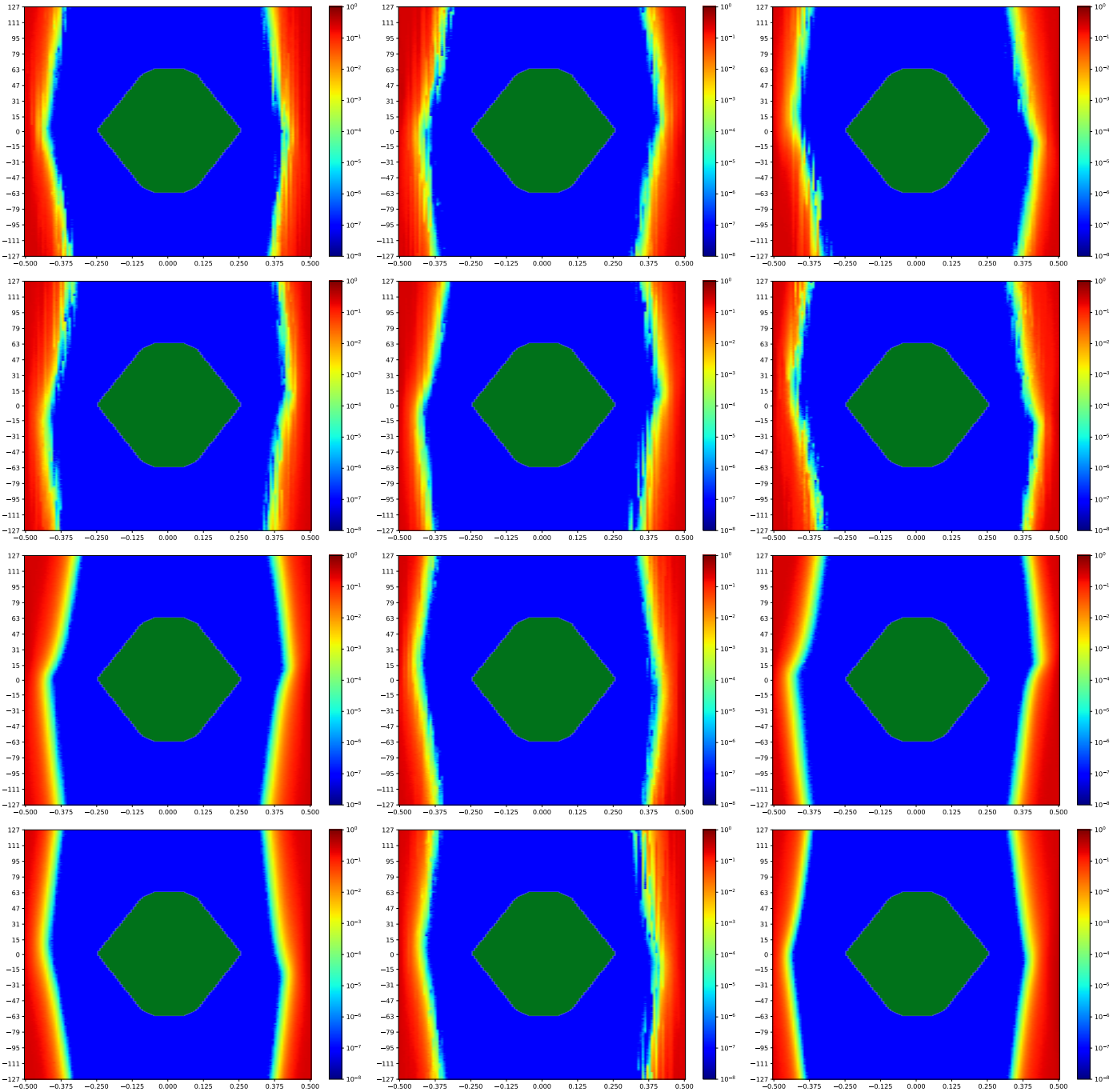


Figure 3.166: MSP_C TX4 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.179.

3.13.1 MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Table 3.154: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:40:17		2018-Sep-26 19:41:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23864	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

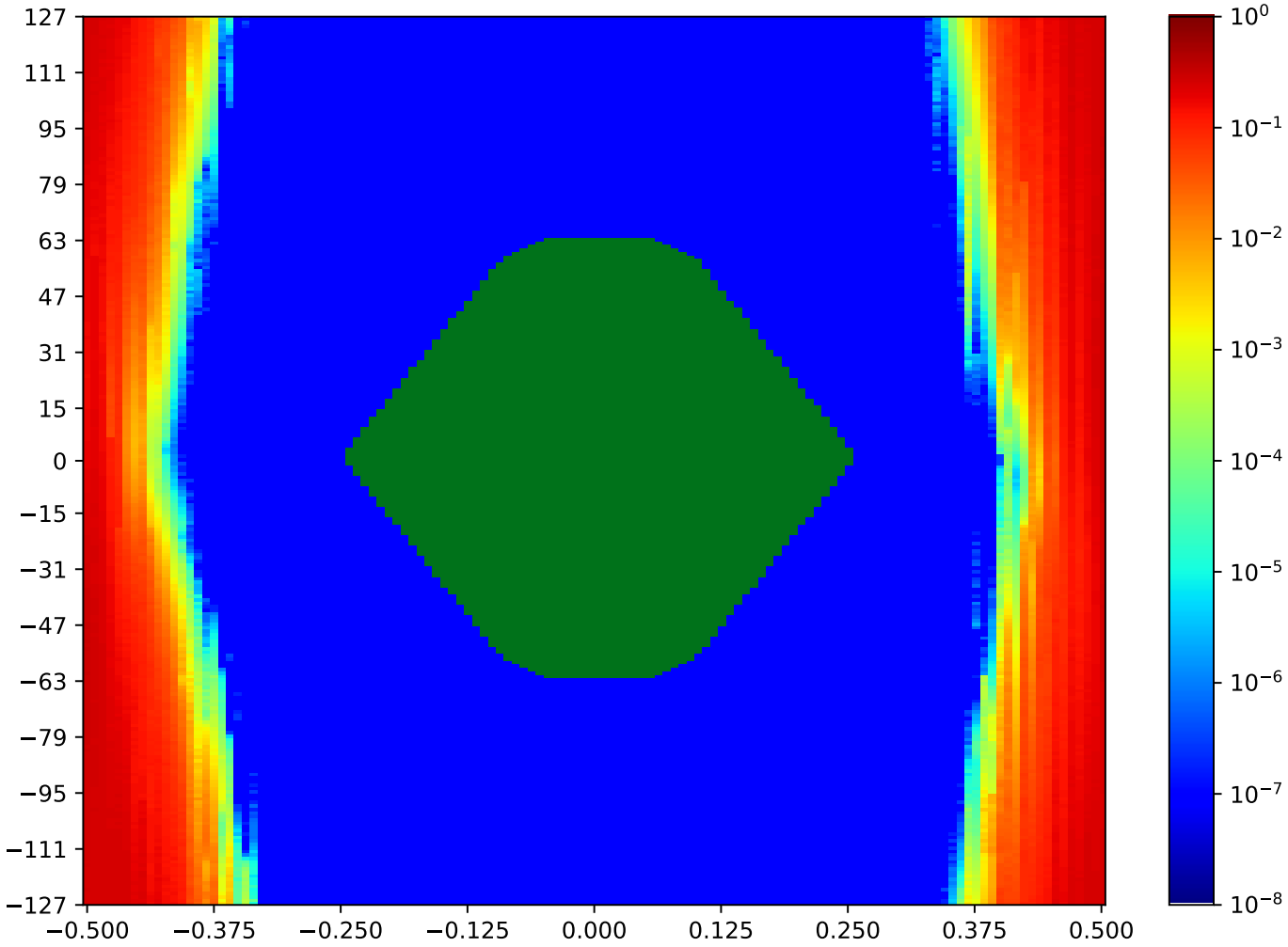


Figure 3.167: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.2 MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Table 3.155: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:37:50		2018-Sep-26 19:39:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23327	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

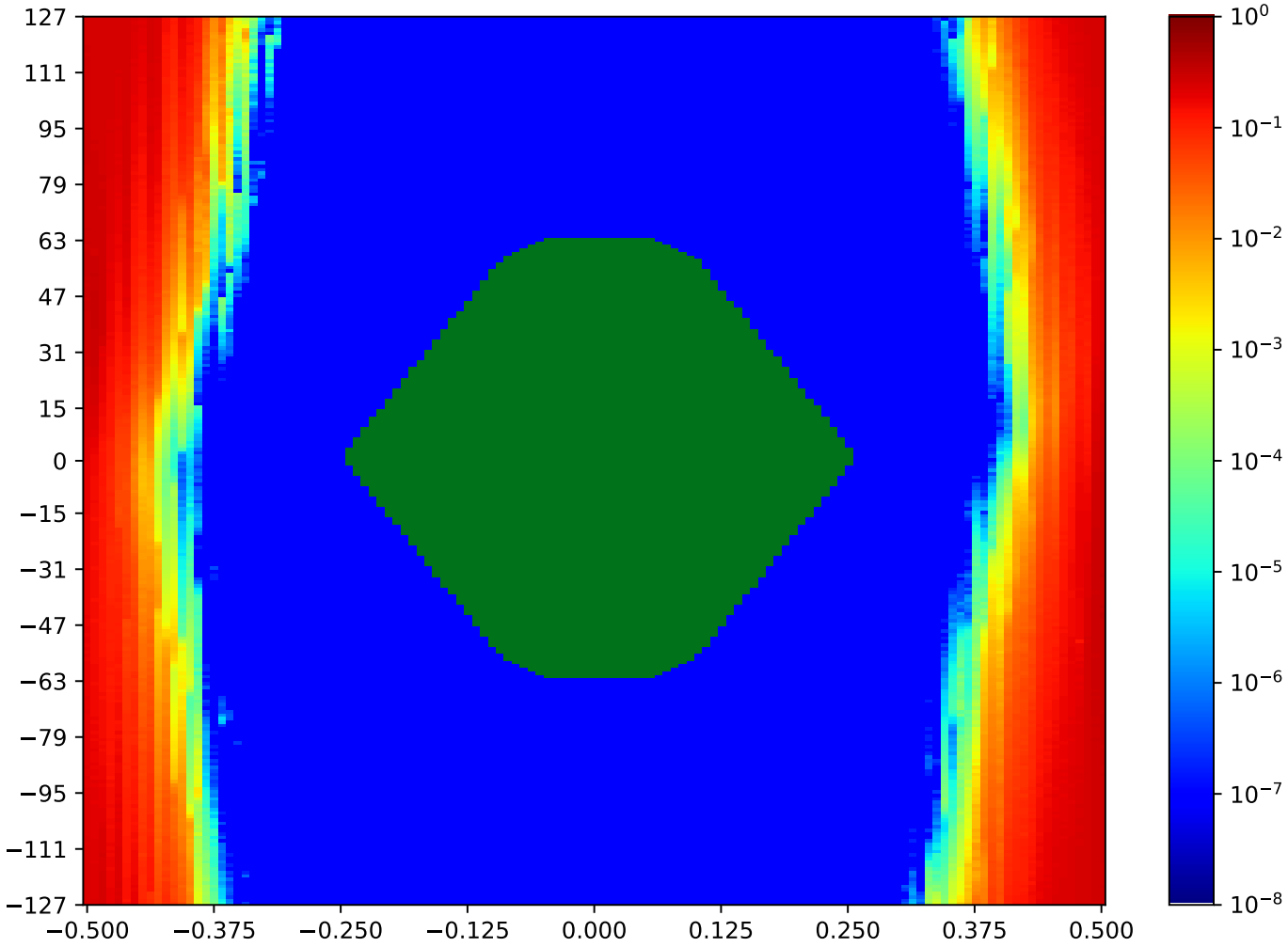


Figure 3.168: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.3 MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Table 3.156: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:44:00		2018-Sep-26 19:45:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23292	101	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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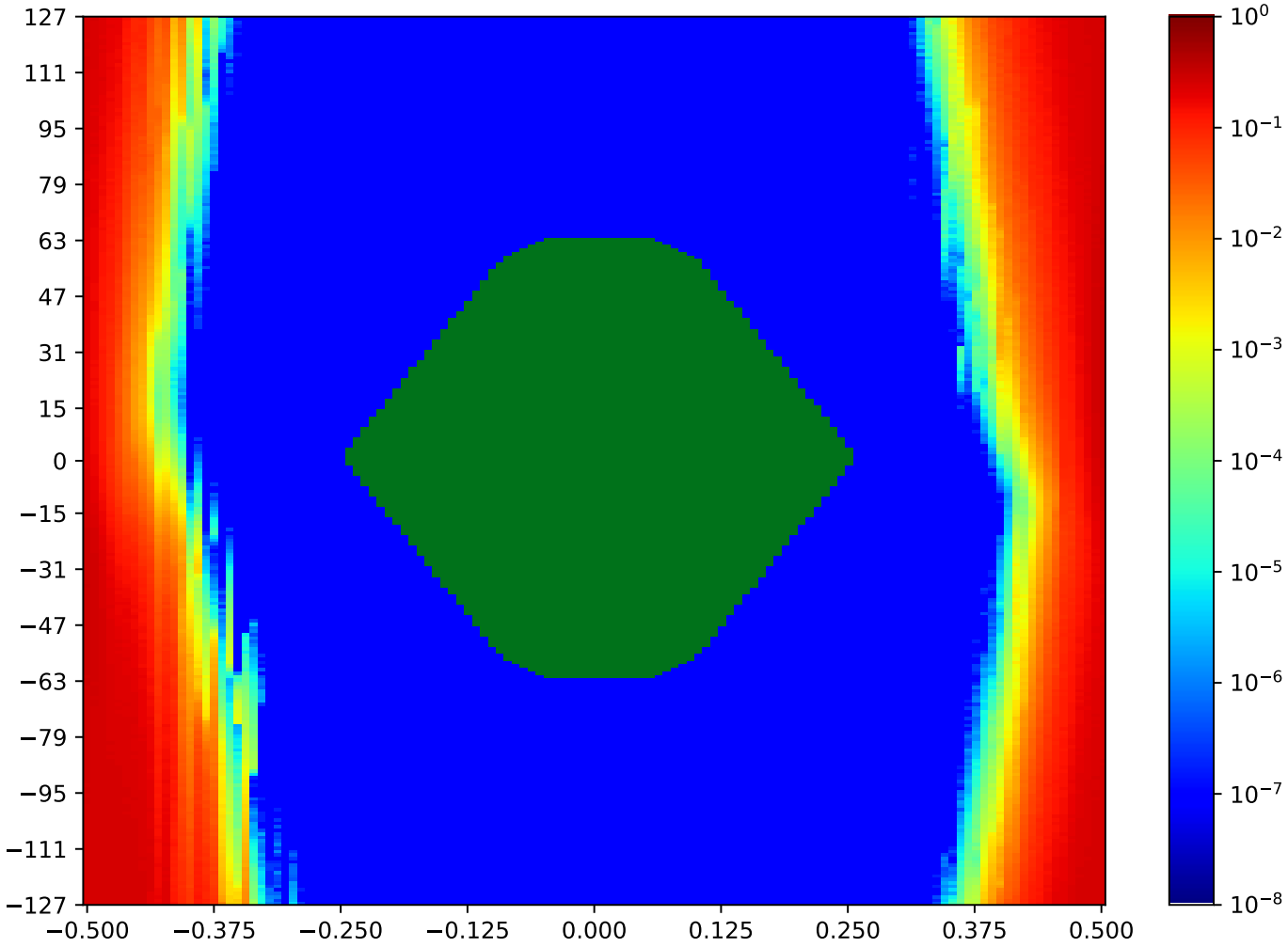


Figure 3.169: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.4 MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Table 3.157: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:36:35		2018-Sep-26 19:37:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23795	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

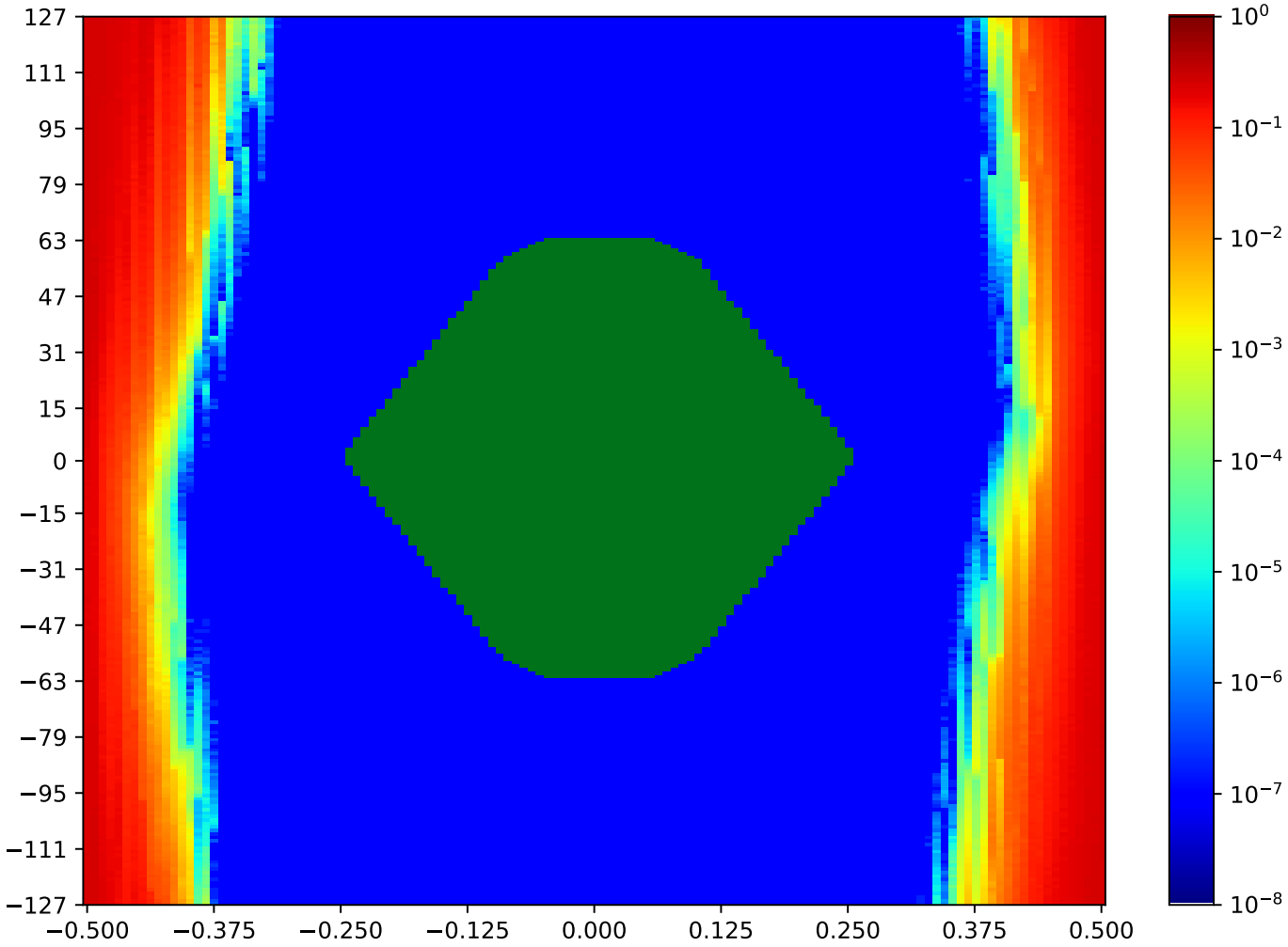


Figure 3.170: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.5 MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Table 3.158: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:47:41		2018-Sep-26 19:48:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23410	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

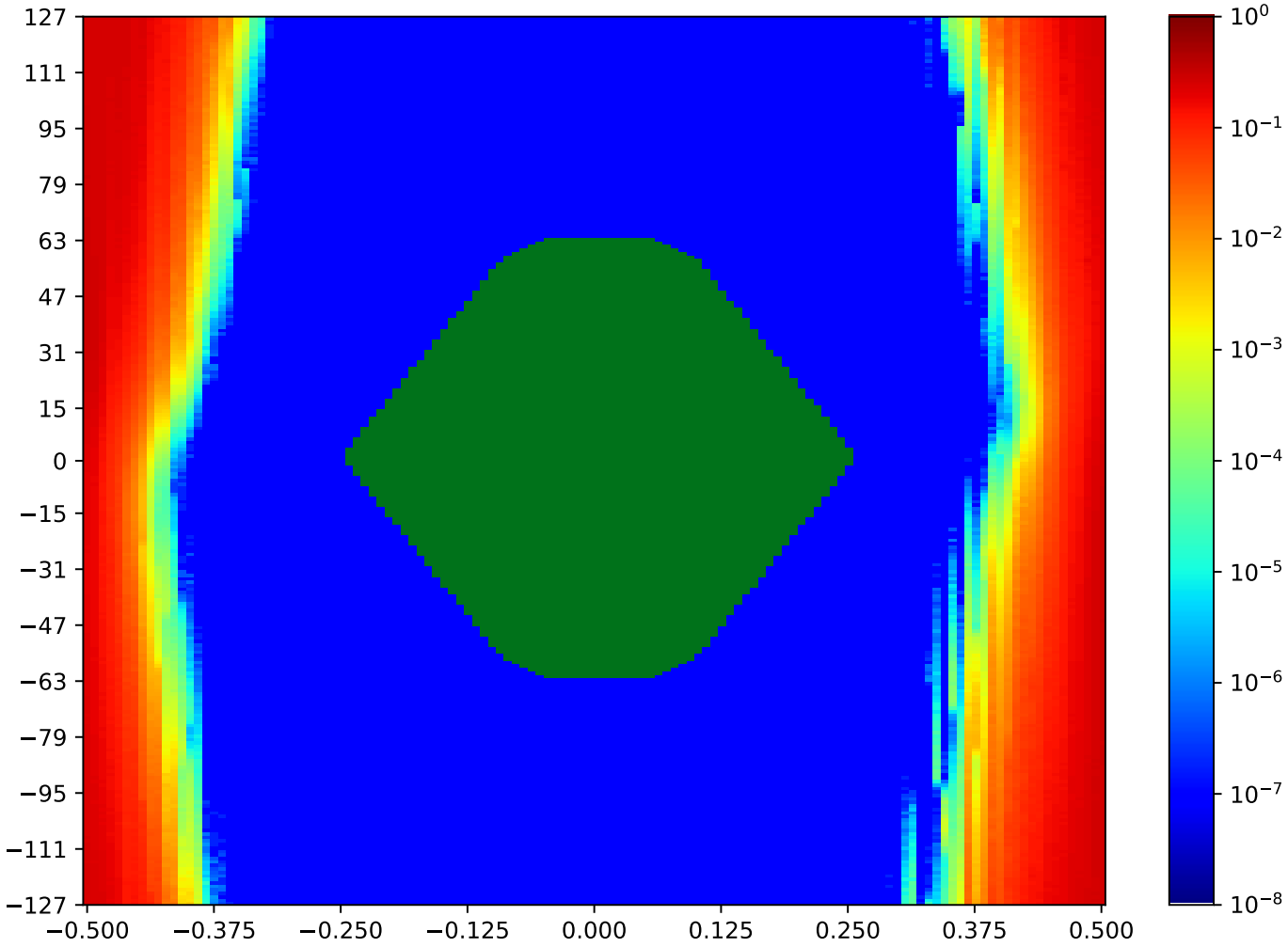


Figure 3.171: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.6 MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Table 3.159: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:39:03		2018-Sep-26 19:40:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23629	100	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

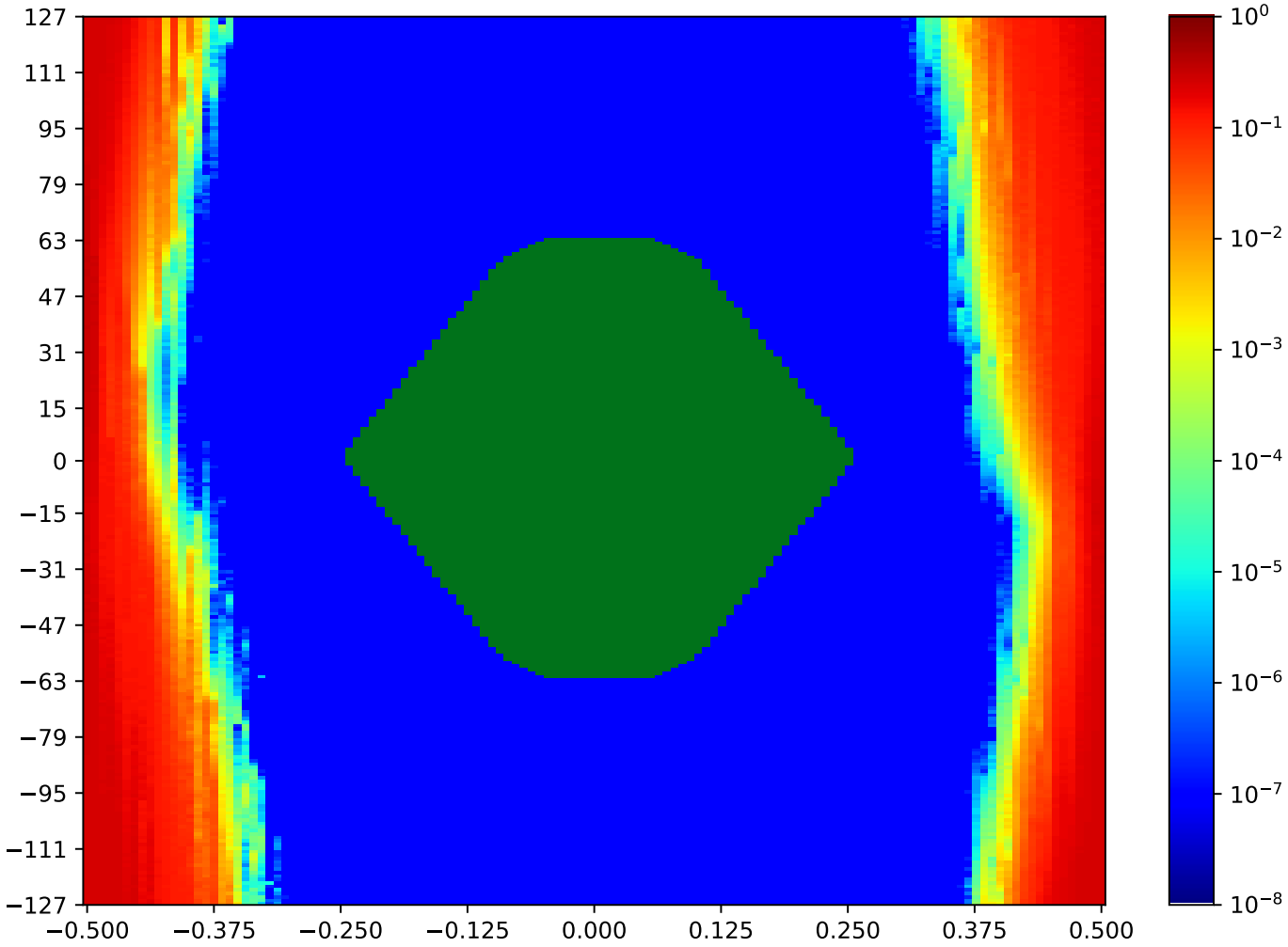


Figure 3.172: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.7 MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Table 3.160: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:50:08		2018-Sep-26 19:51:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23291	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

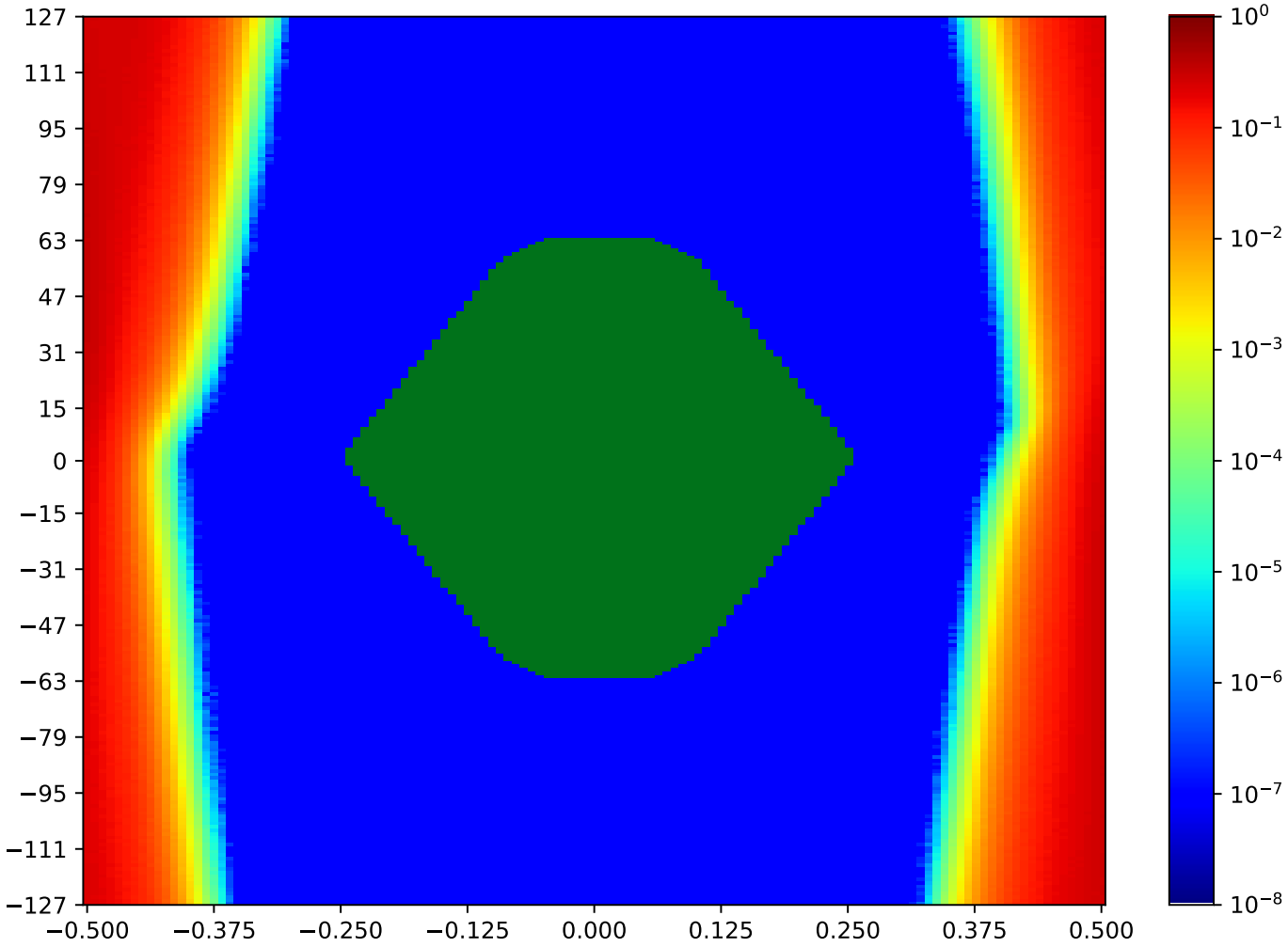


Figure 3.173: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.8 MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Table 3.161: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:41:31		2018-Sep-26 19:42:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24013	100	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

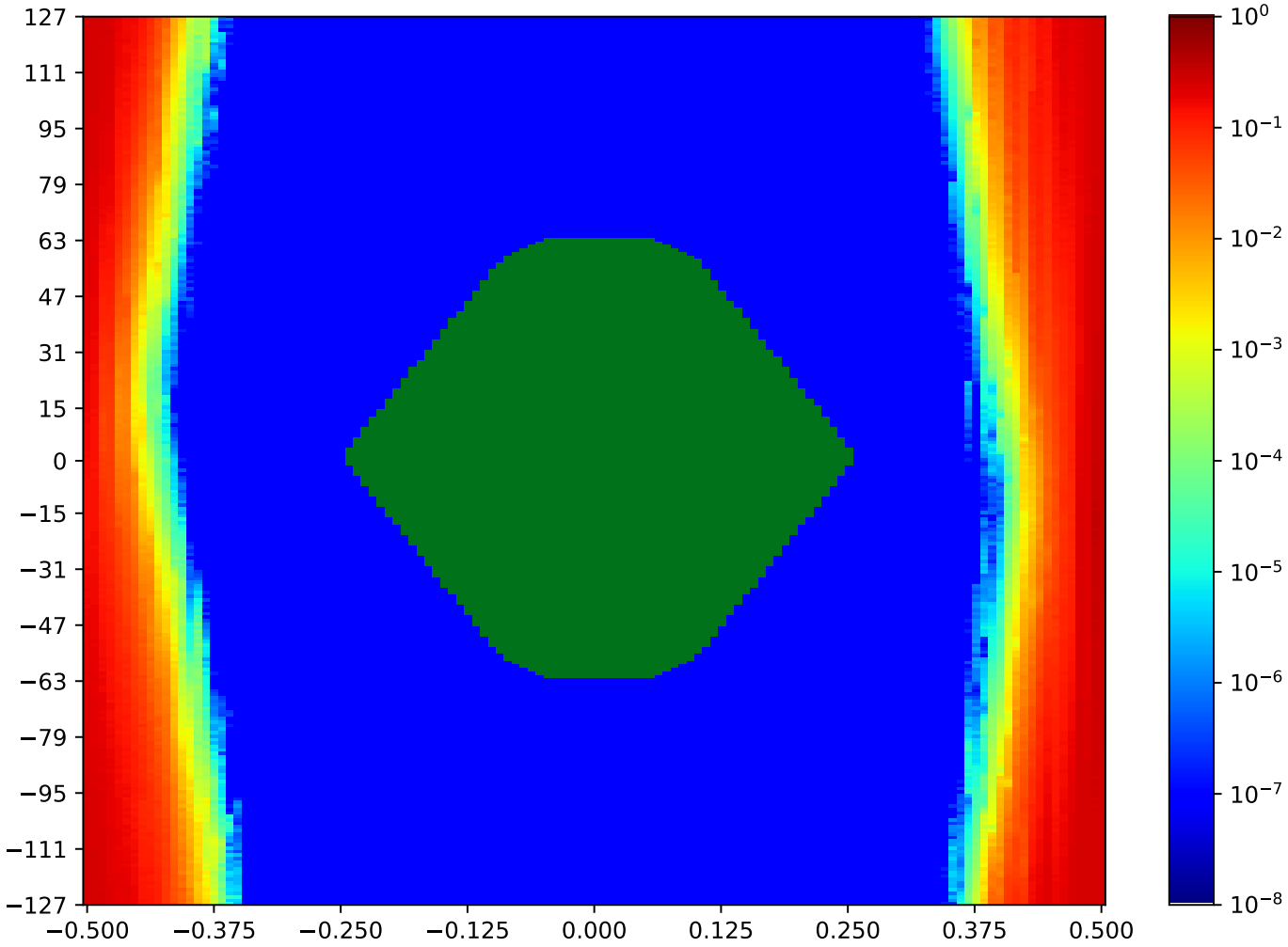


Figure 3.174: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.9 MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Table 3.162: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:48:54		2018-Sep-26 19:50:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23585	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

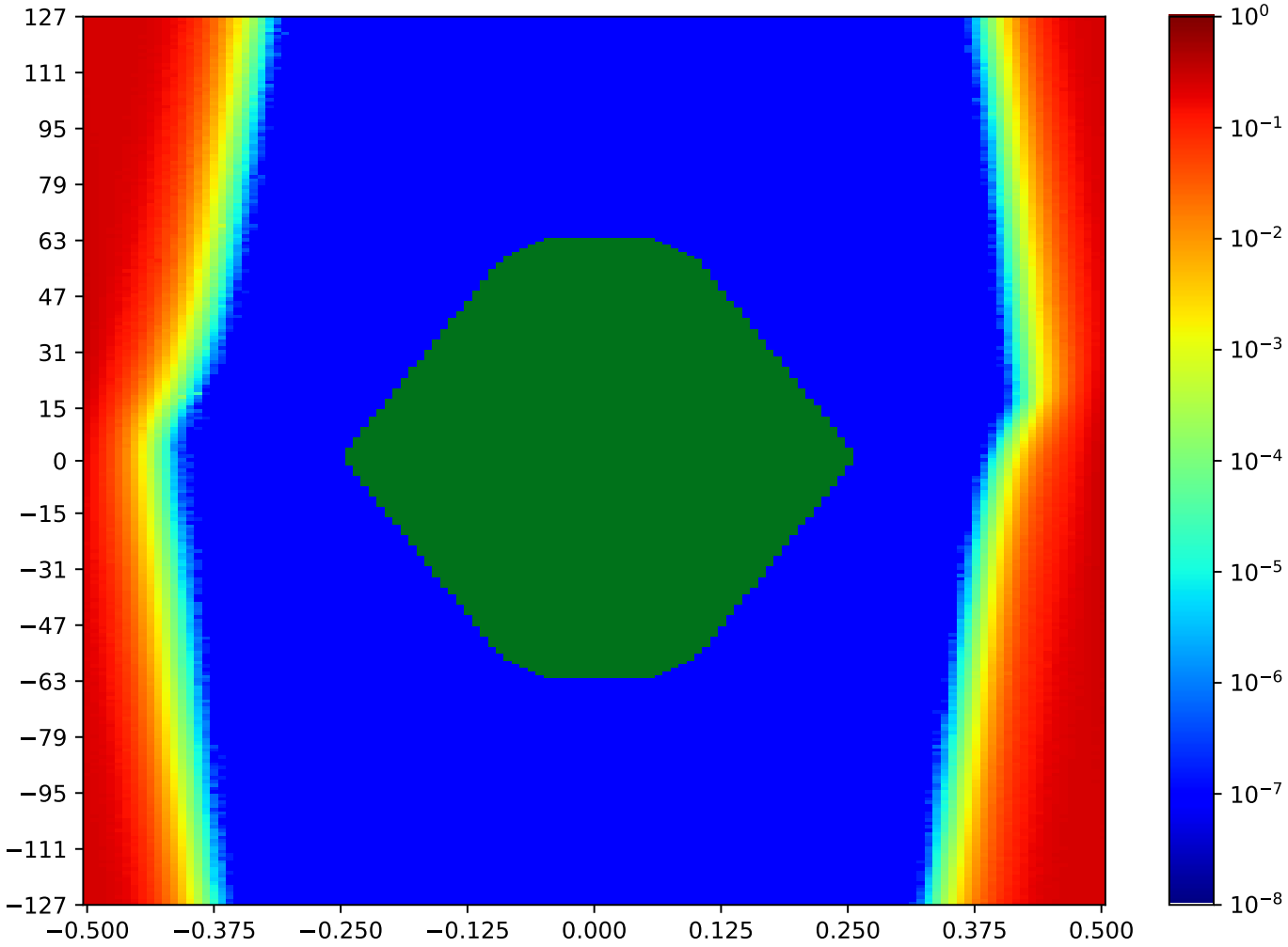


Figure 3.175: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.10 MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Table 3.163: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:42:46		2018-Sep-26 19:44:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23722	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

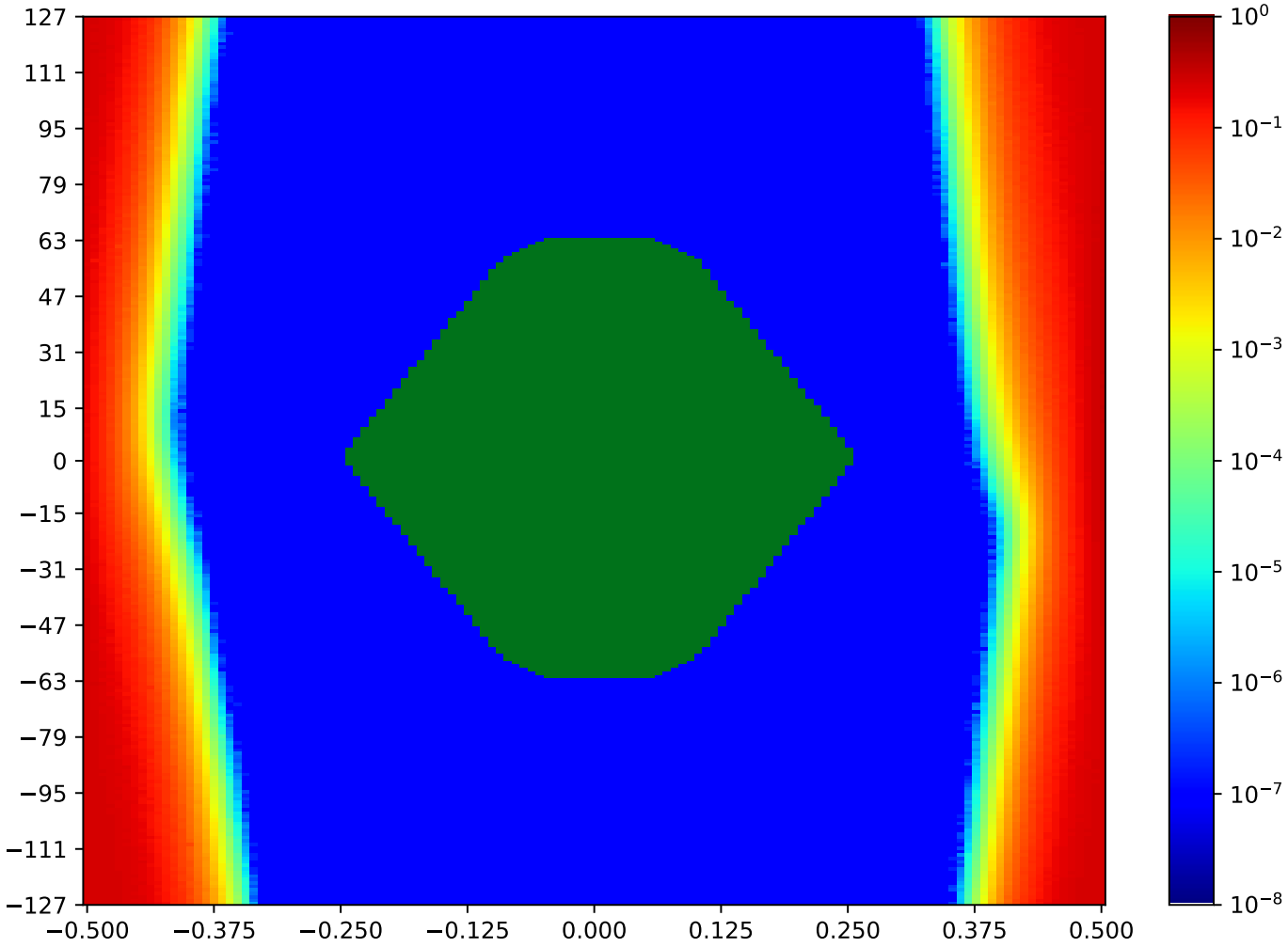


Figure 3.176: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.11 MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Table 3.164: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:46:28		2018-Sep-26 19:47:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23438	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

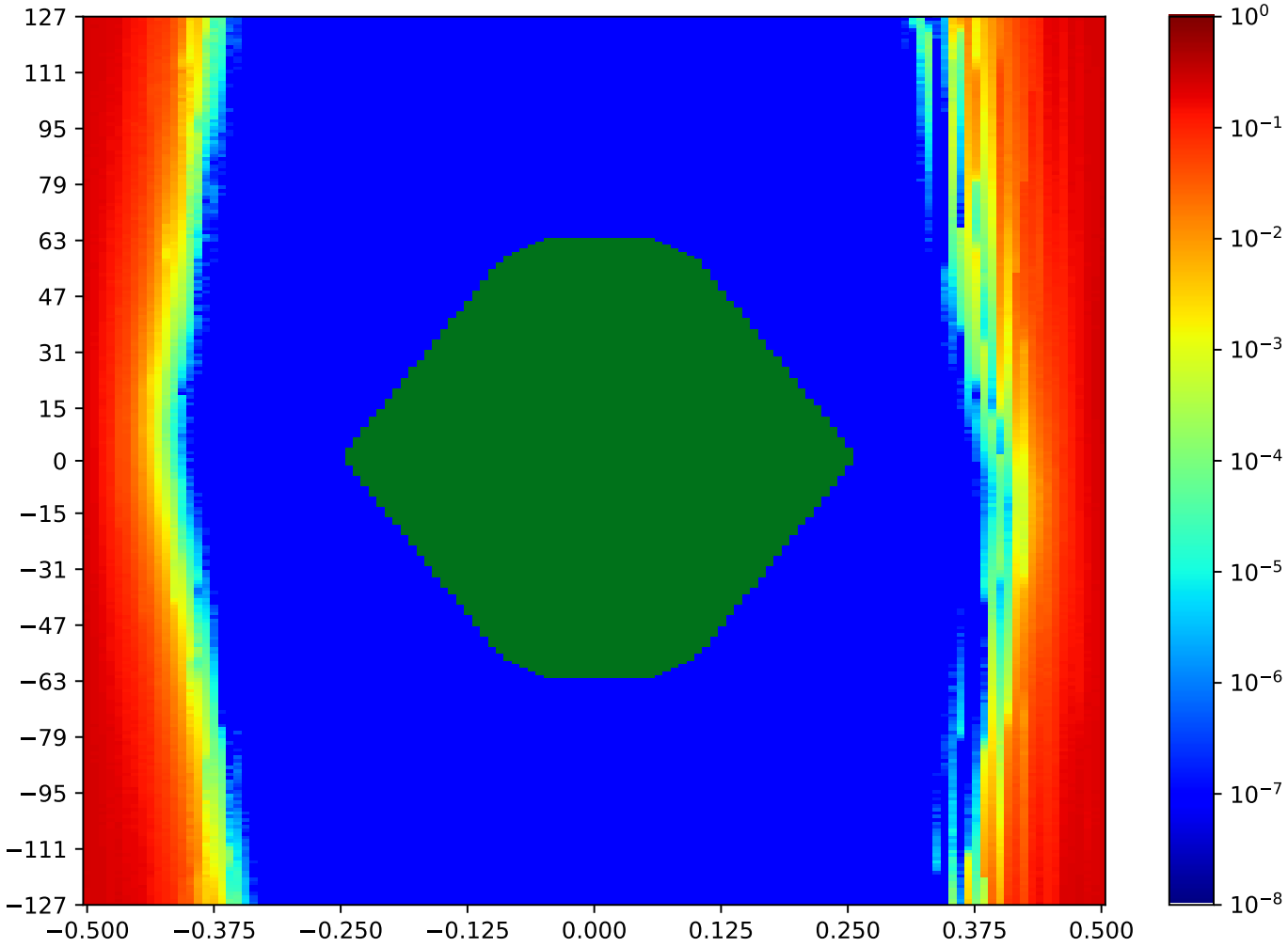


Figure 3.177: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.13.12 MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Table 3.165: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:45:14		2018-Sep-26 19:46:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24102	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

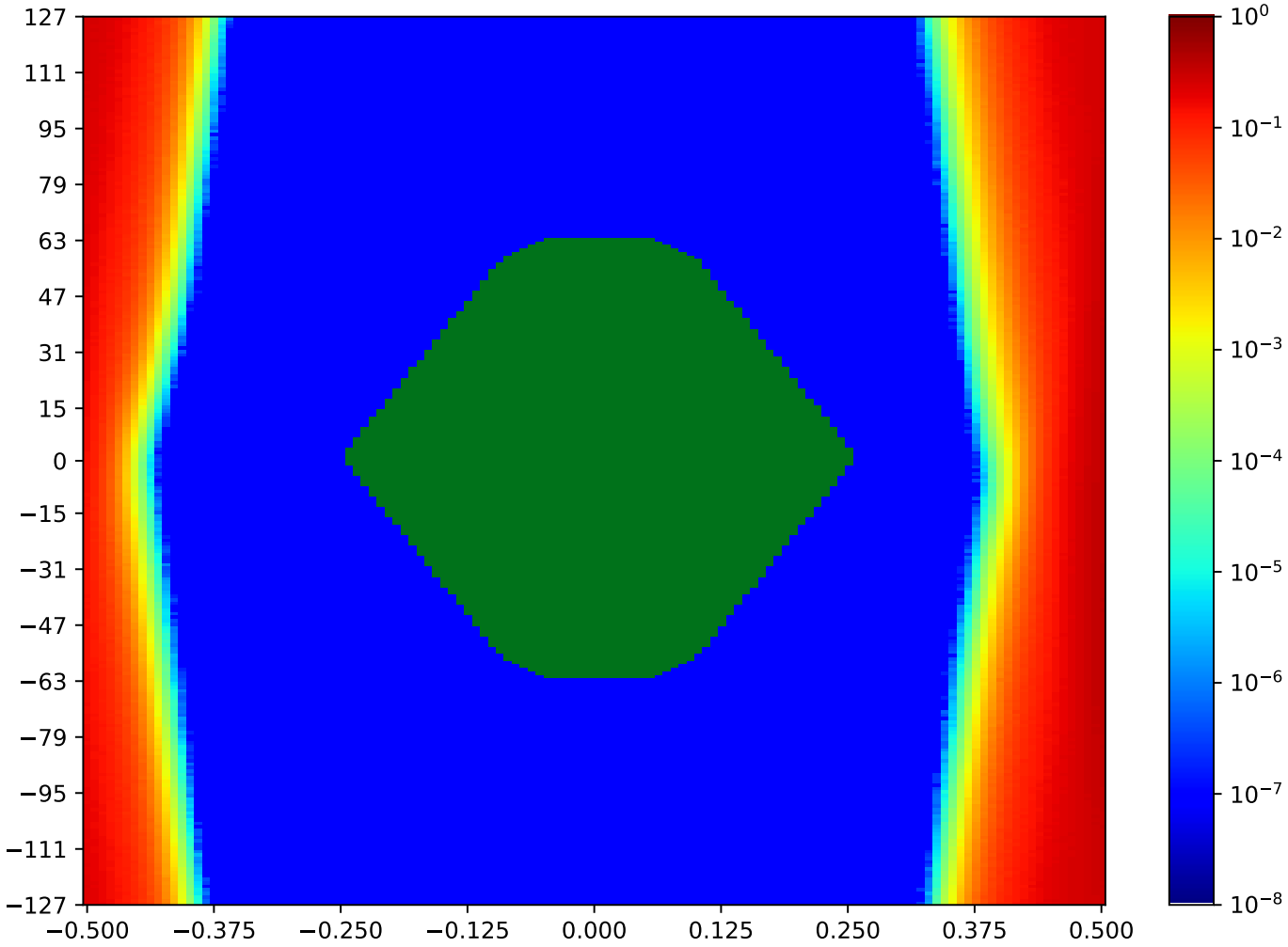


Figure 3.178: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.188.

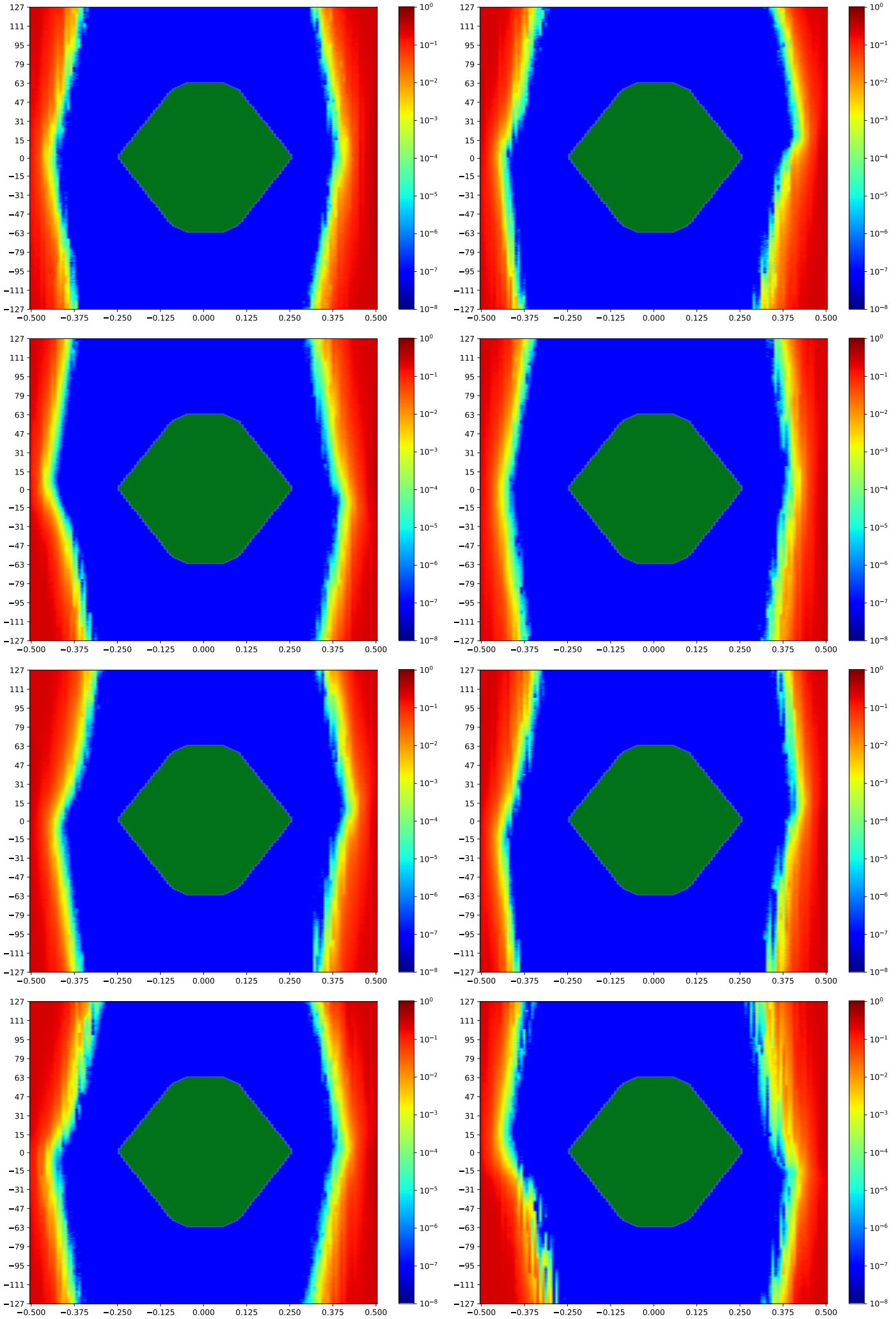


Figure 3.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback

3.14.1 TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Table 3.166: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:55:02		2018-Sep-26 19:56:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23282	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

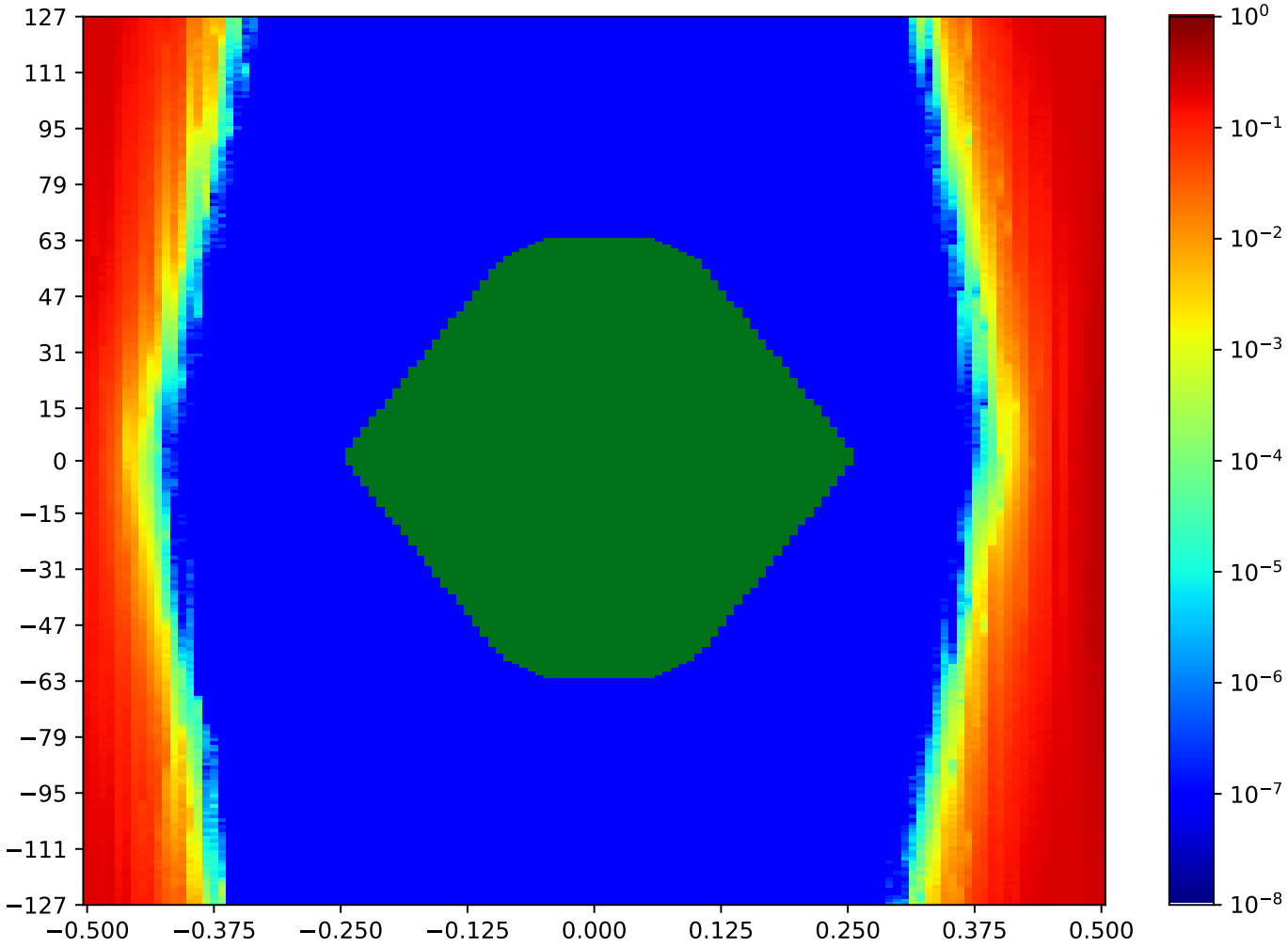


Figure 3.180: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.2 TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Table 3.167: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:52:35		2018-Sep-26 19:53:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23337	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

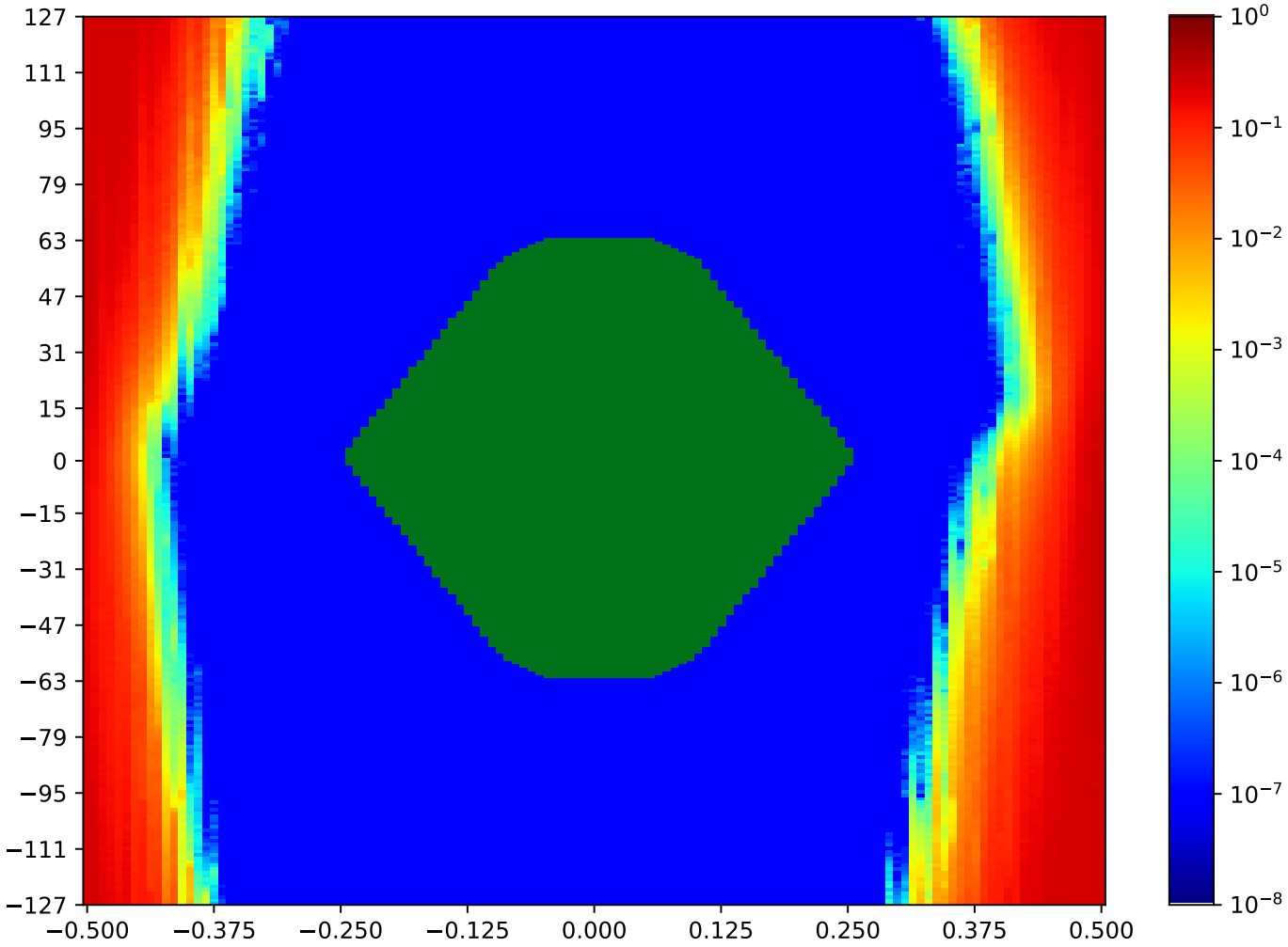


Figure 3.181: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.3 TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Table 3.168: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:57:29		2018-Sep-26 19:58:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23164	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

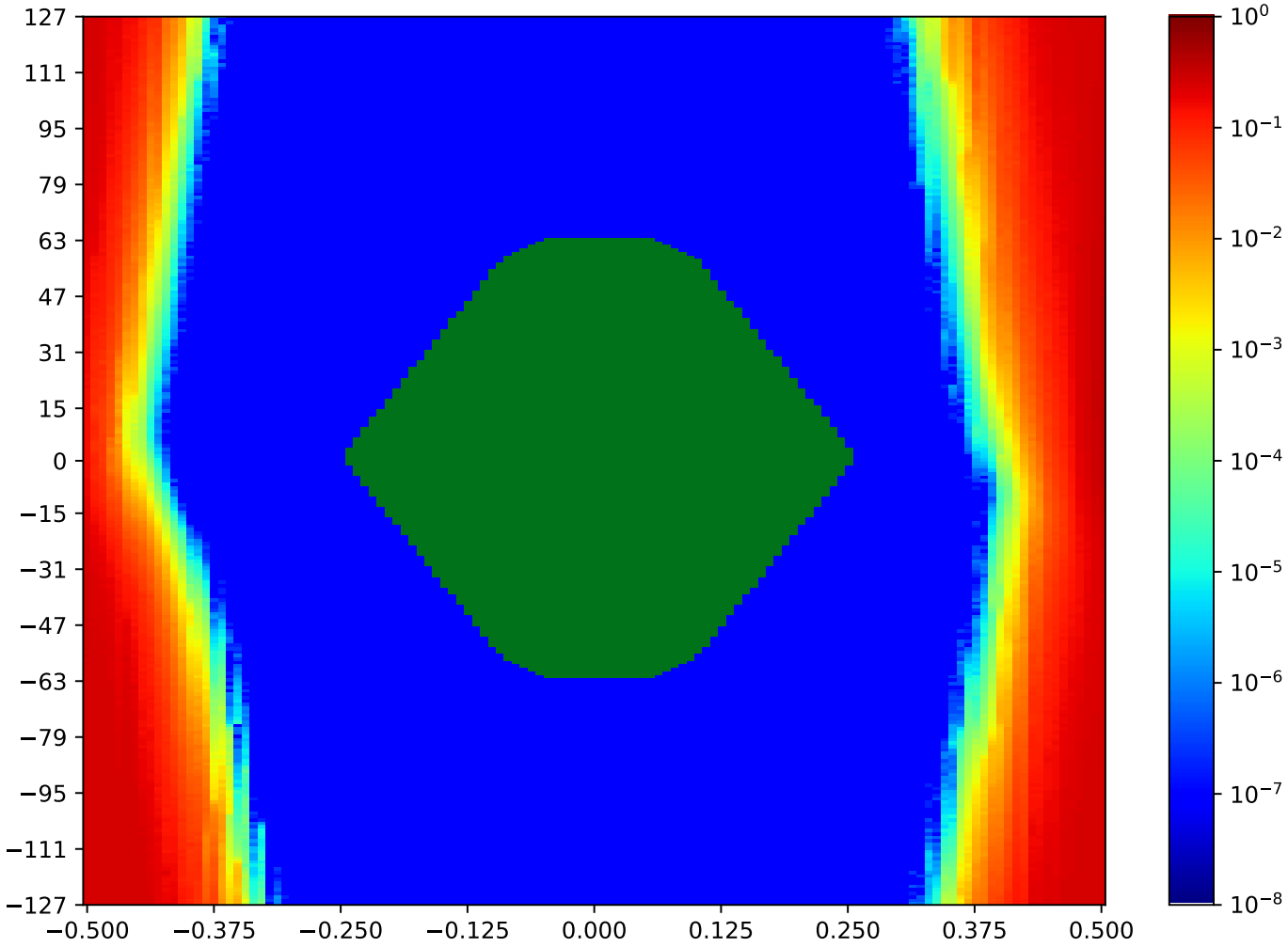


Figure 3.182: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.4 TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Table 3.169: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:53:49		2018-Sep-26 19:55:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23523	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

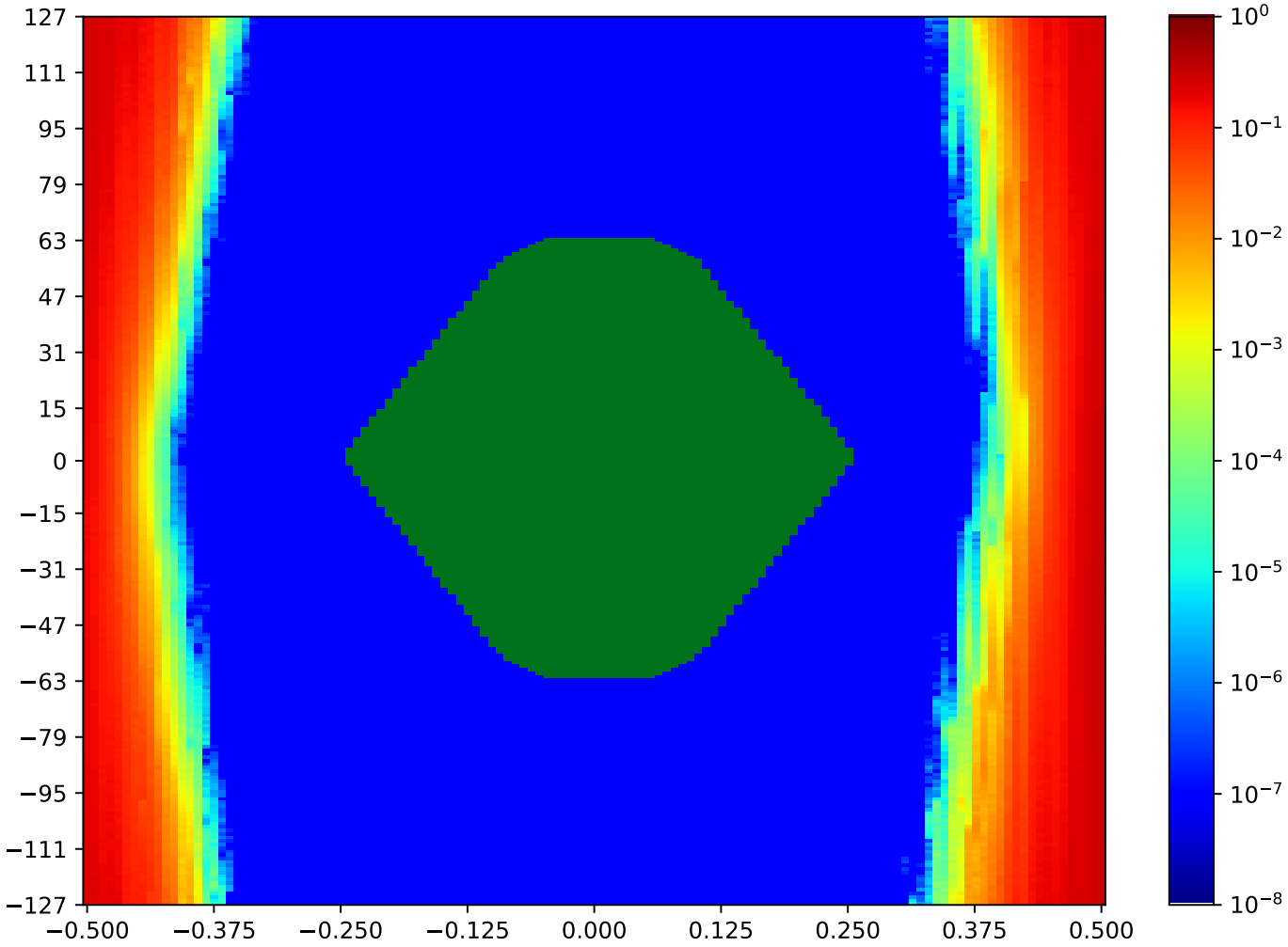


Figure 3.183: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.5 TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Table 3.170: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:59:56		2018-Sep-26 20:01:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22896	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

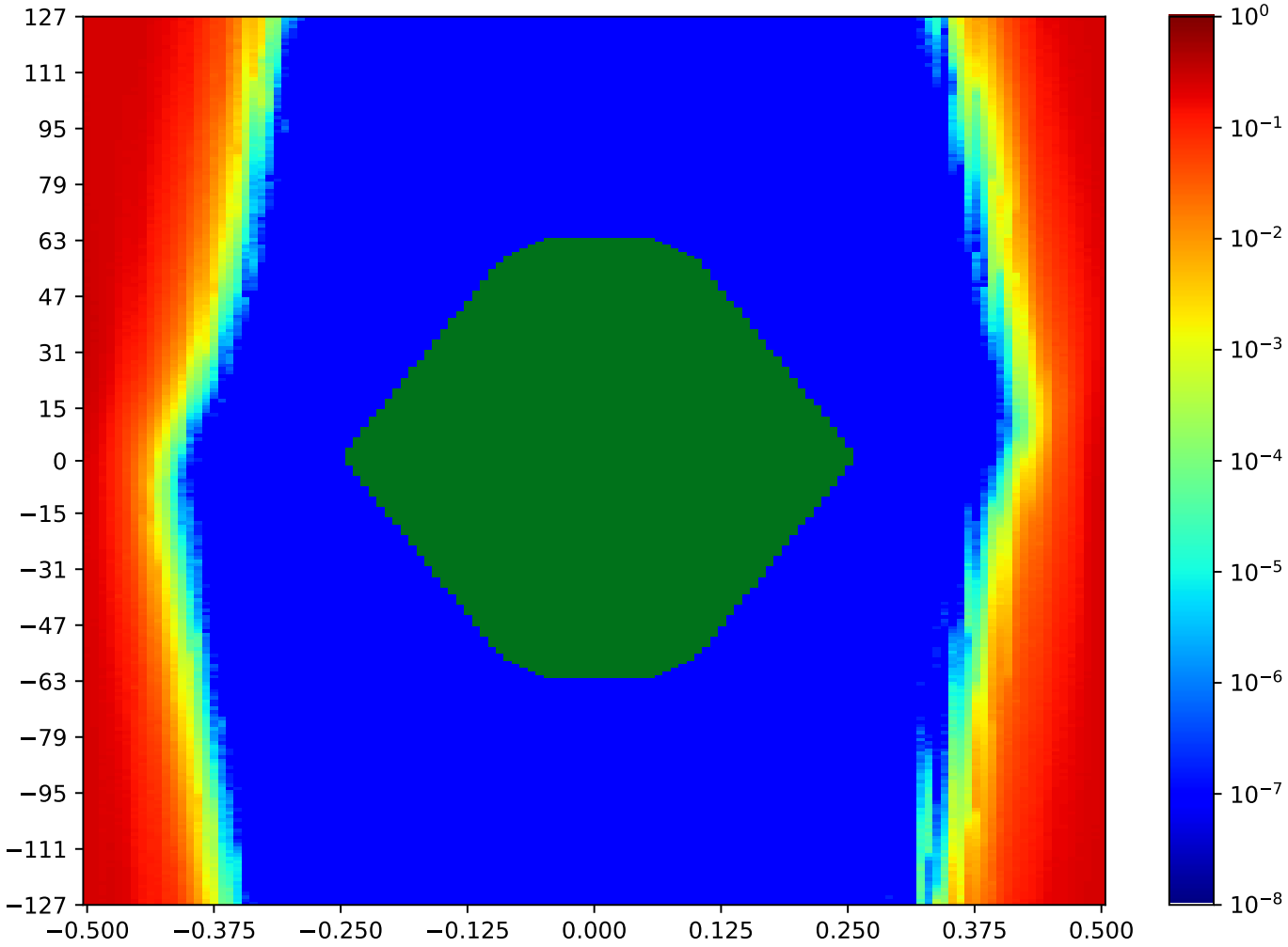


Figure 3.184: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.6 TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Table 3.171: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:51:21		2018-Sep-26 19:52:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23857	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

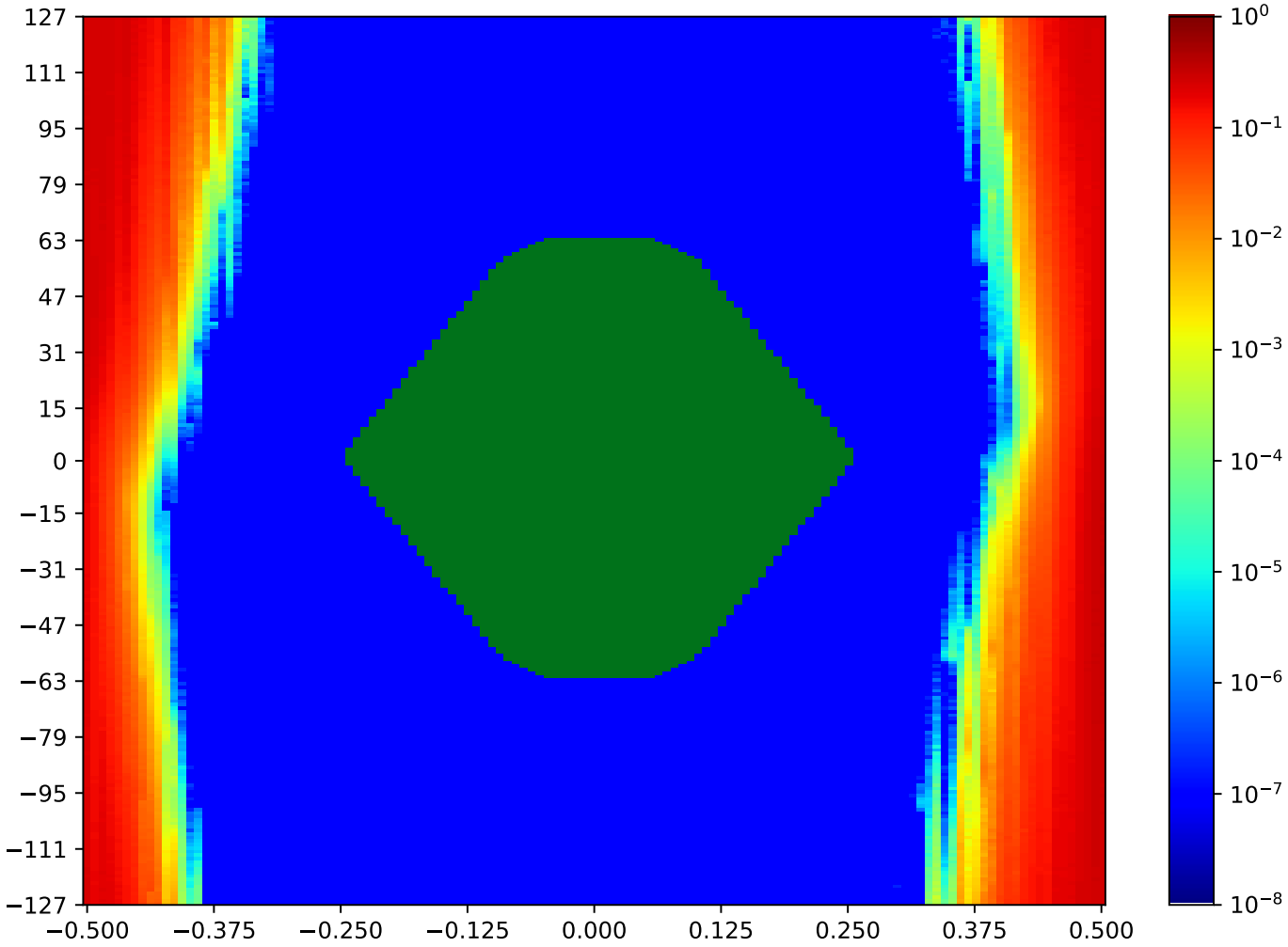


Figure 3.185: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.7 TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Table 3.172: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:56:15		2018-Sep-26 19:57:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22360	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

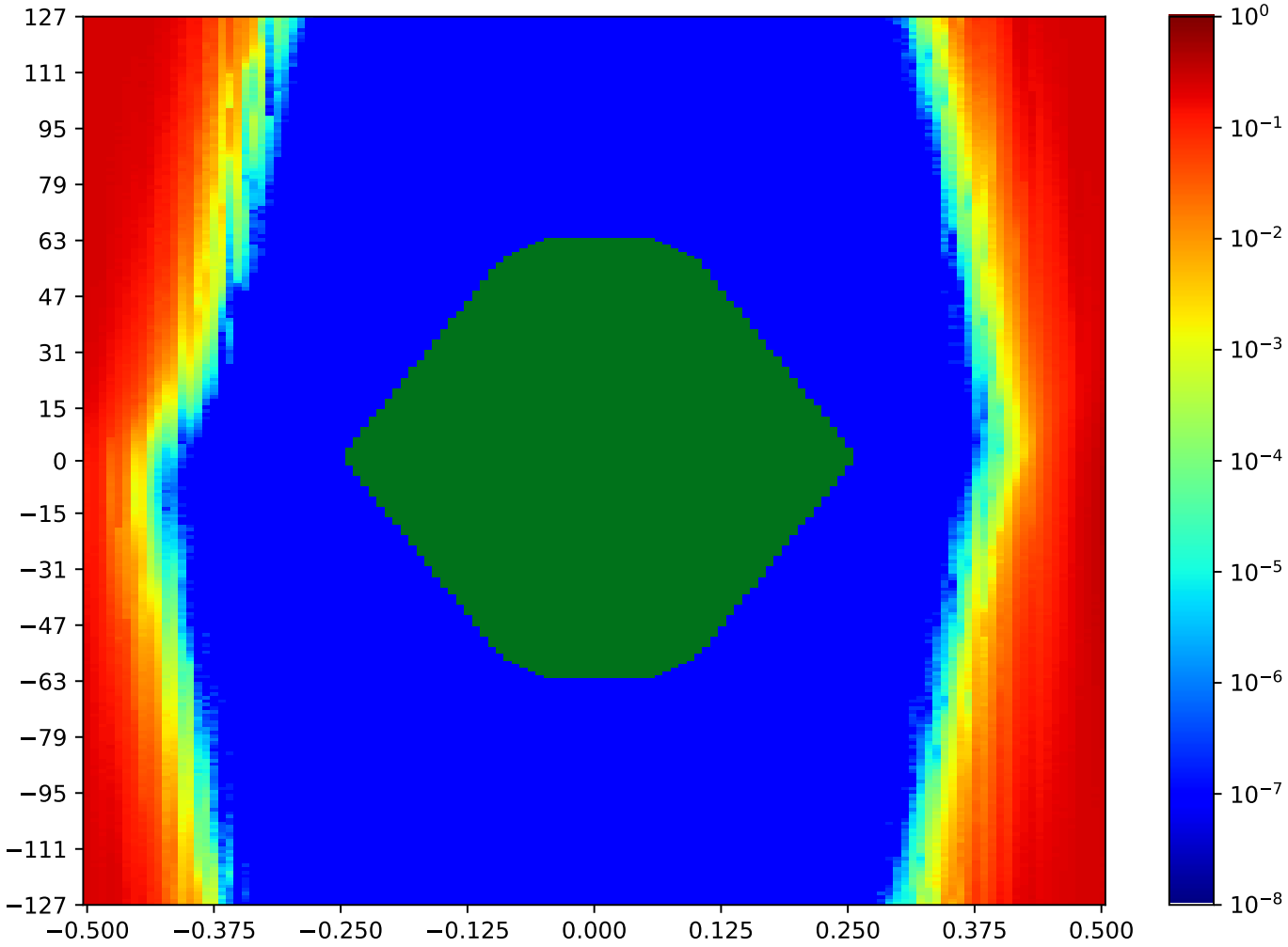


Figure 3.186: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.14.8 TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Table 3.173: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:58:43		2018-Sep-26 19:59:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21932	93	71.32%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

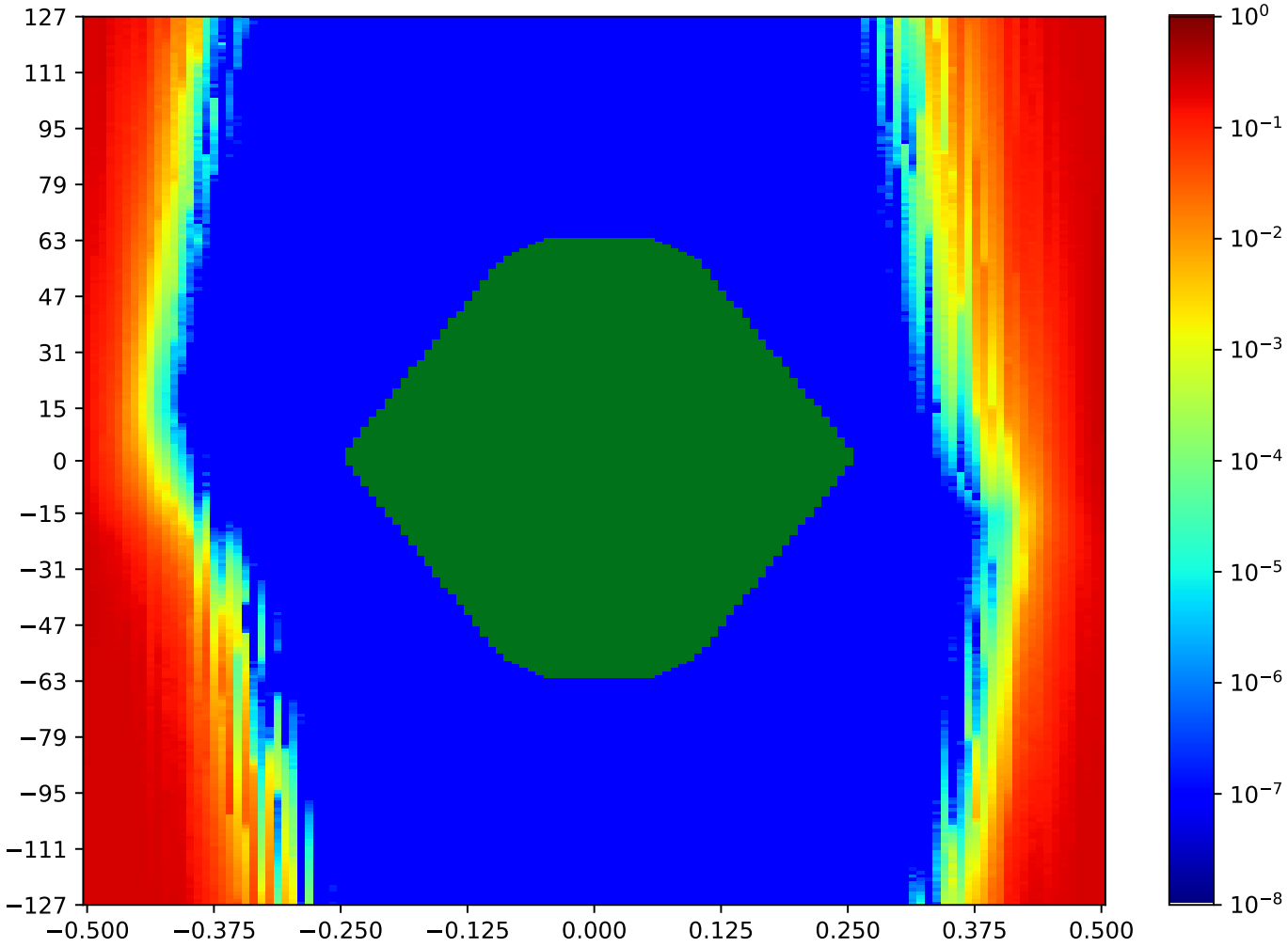


Figure 3.187: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15 MSP_A TX1 MSP_C RX10 Minipod Loopback

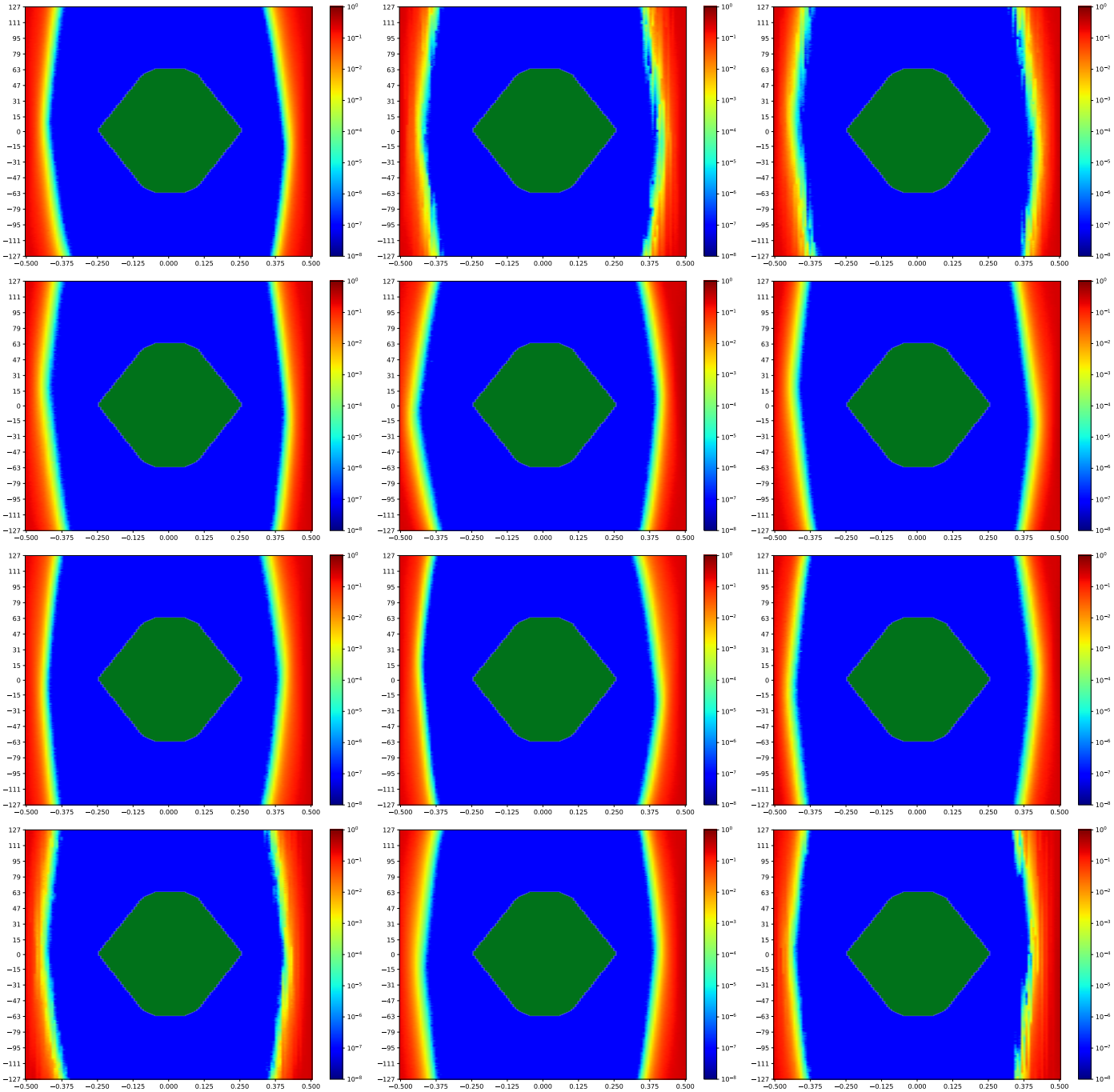


Figure 3.188: MSP_A TX1 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.201.

3.15.1 MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Table 3.174: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:53:09		2018-Sep-28 09:54:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24571	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

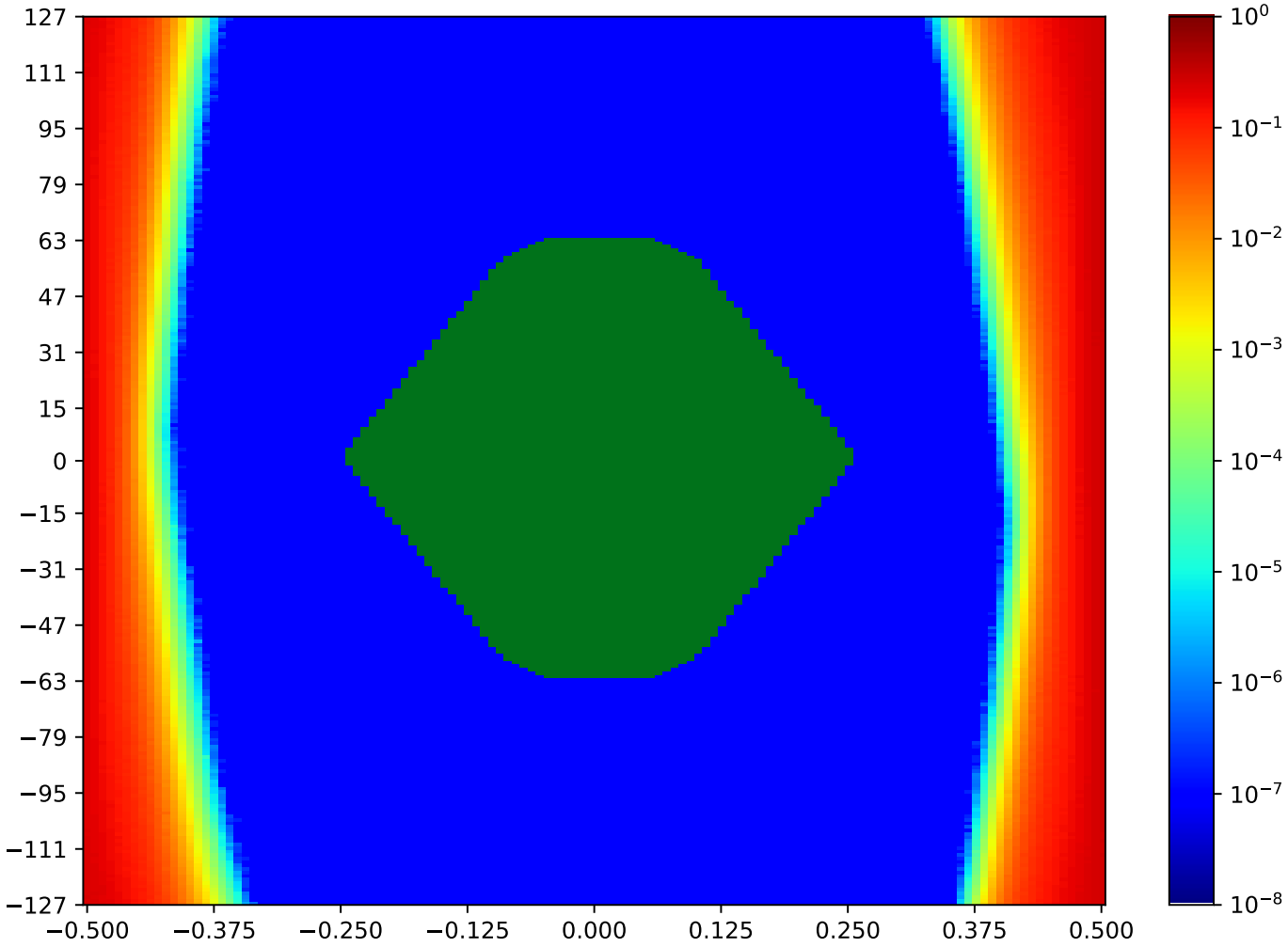


Figure 3.189: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.2 MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Table 3.175: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:55:38		2018-Sep-28 09:56:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24264	103	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

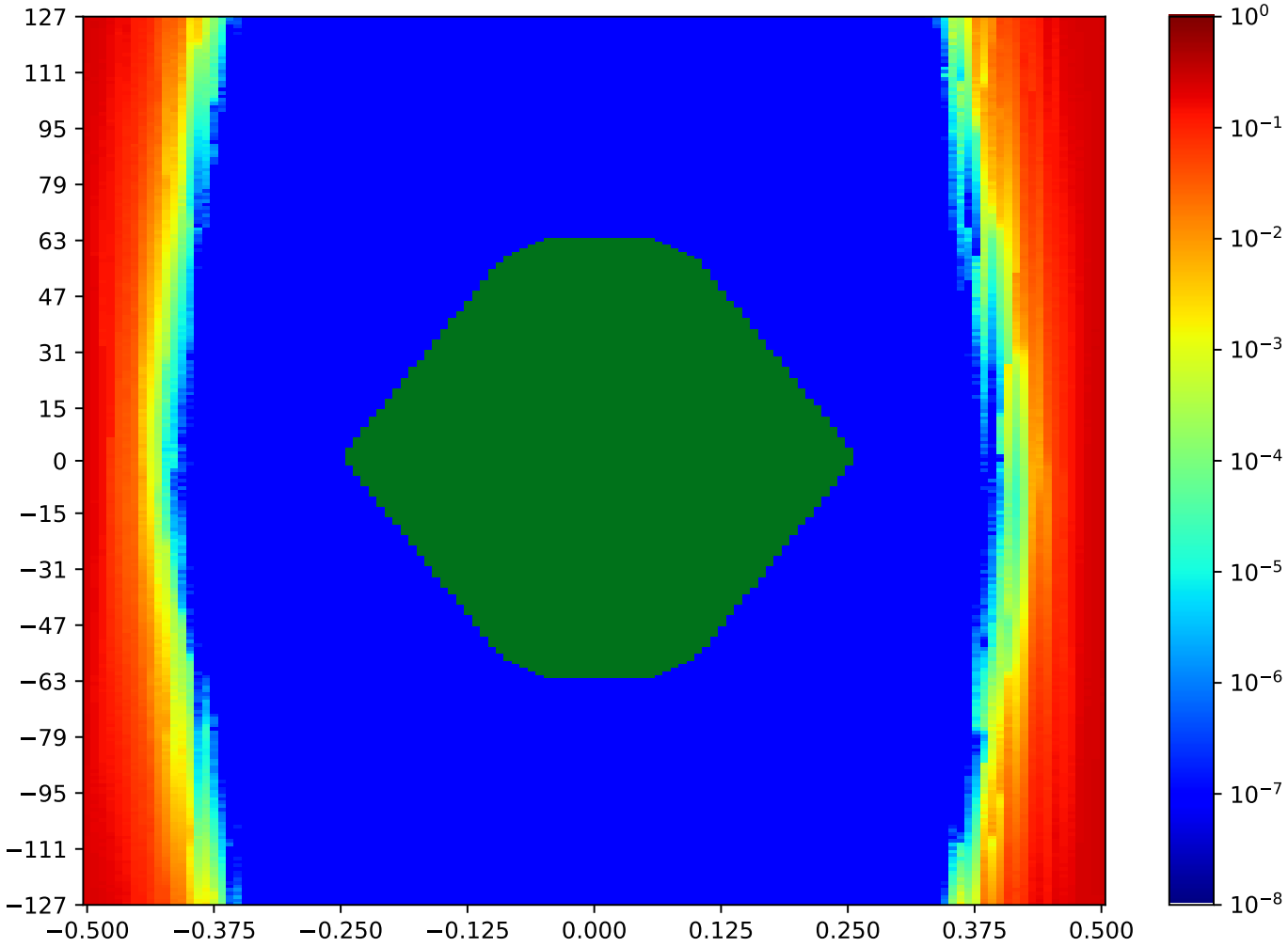


Figure 3.190: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.3 MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Table 3.176: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:56:53		2018-Sep-28 09:58:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24252	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

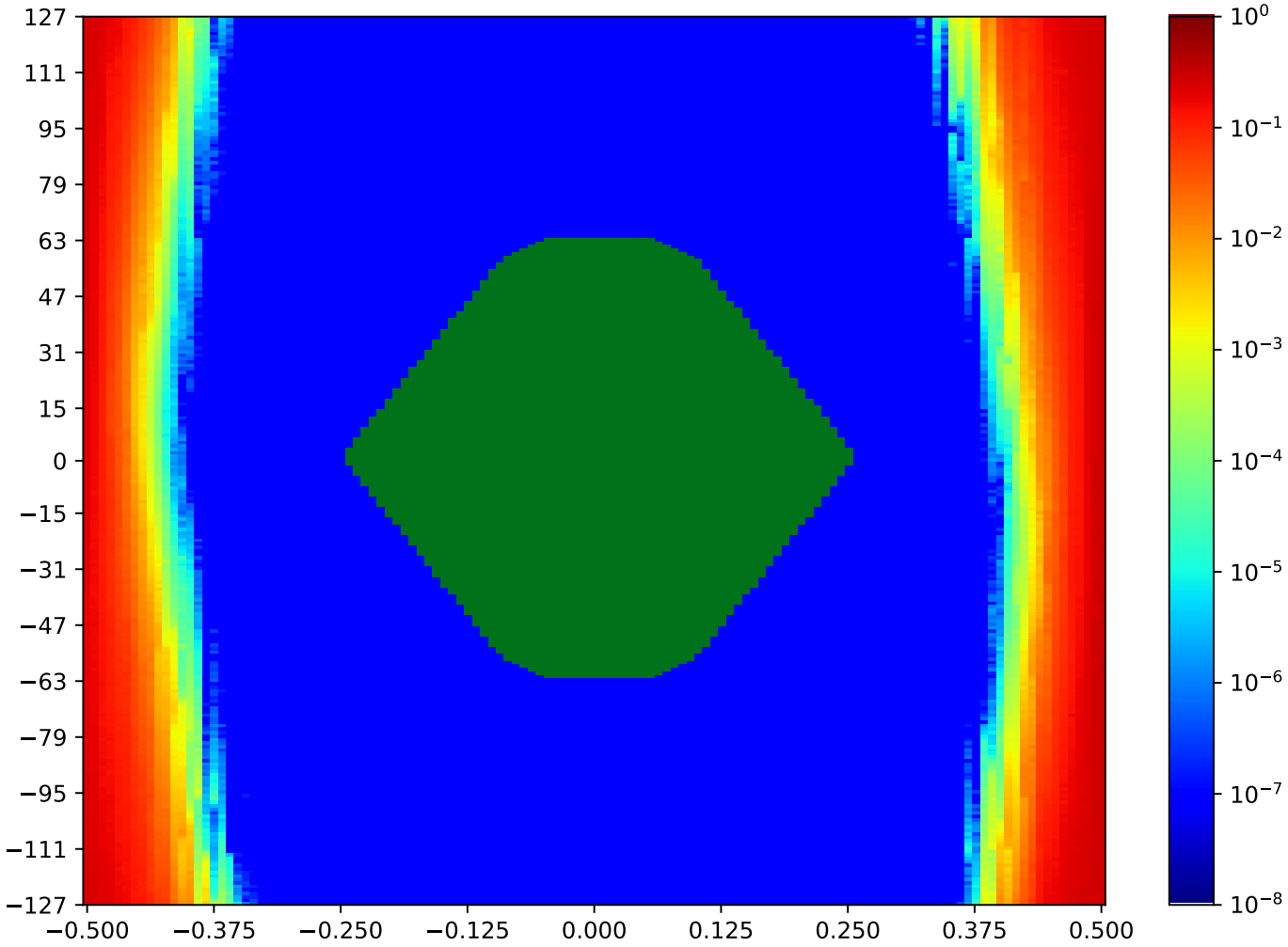


Figure 3.191: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.4 MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Table 3.177: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:50:41		2018-Sep-28 09:51:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24549	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

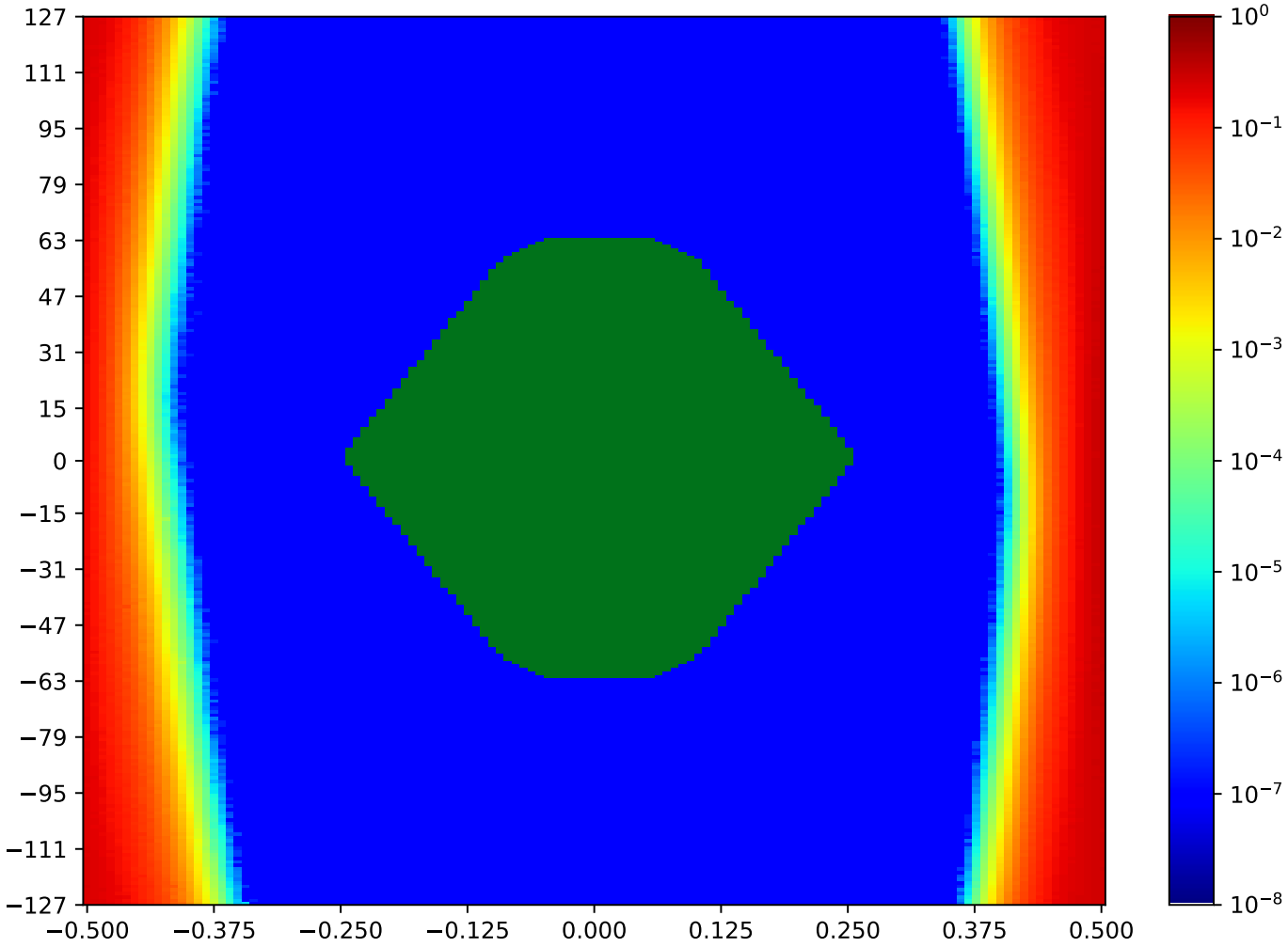


Figure 3.192: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.5 MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Table 3.178: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:00:37		2018-Sep-28 10:01:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24479	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

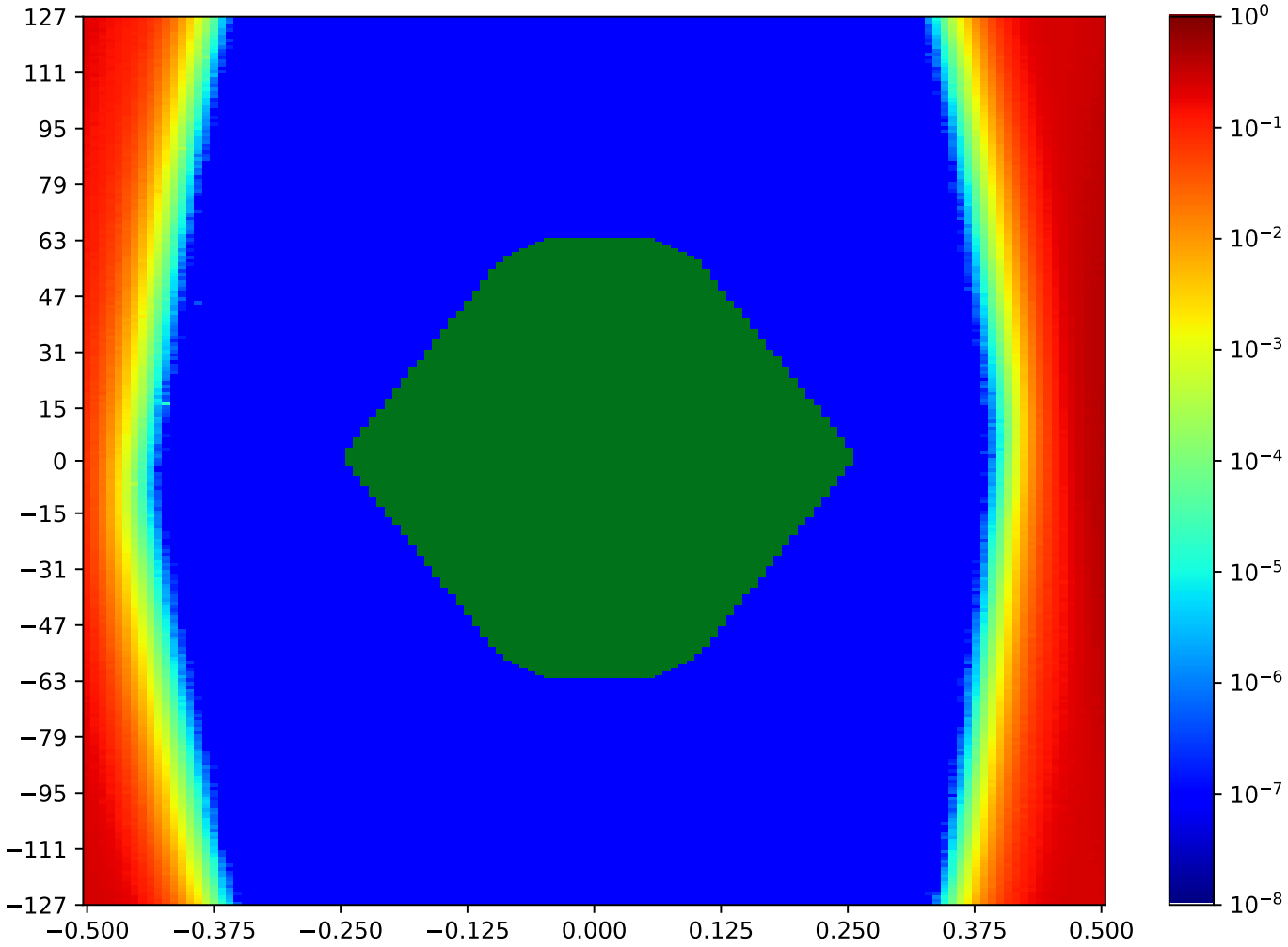


Figure 3.193: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.6 MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Table 3.179: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:49:26		2018-Sep-28 09:50:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24131	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

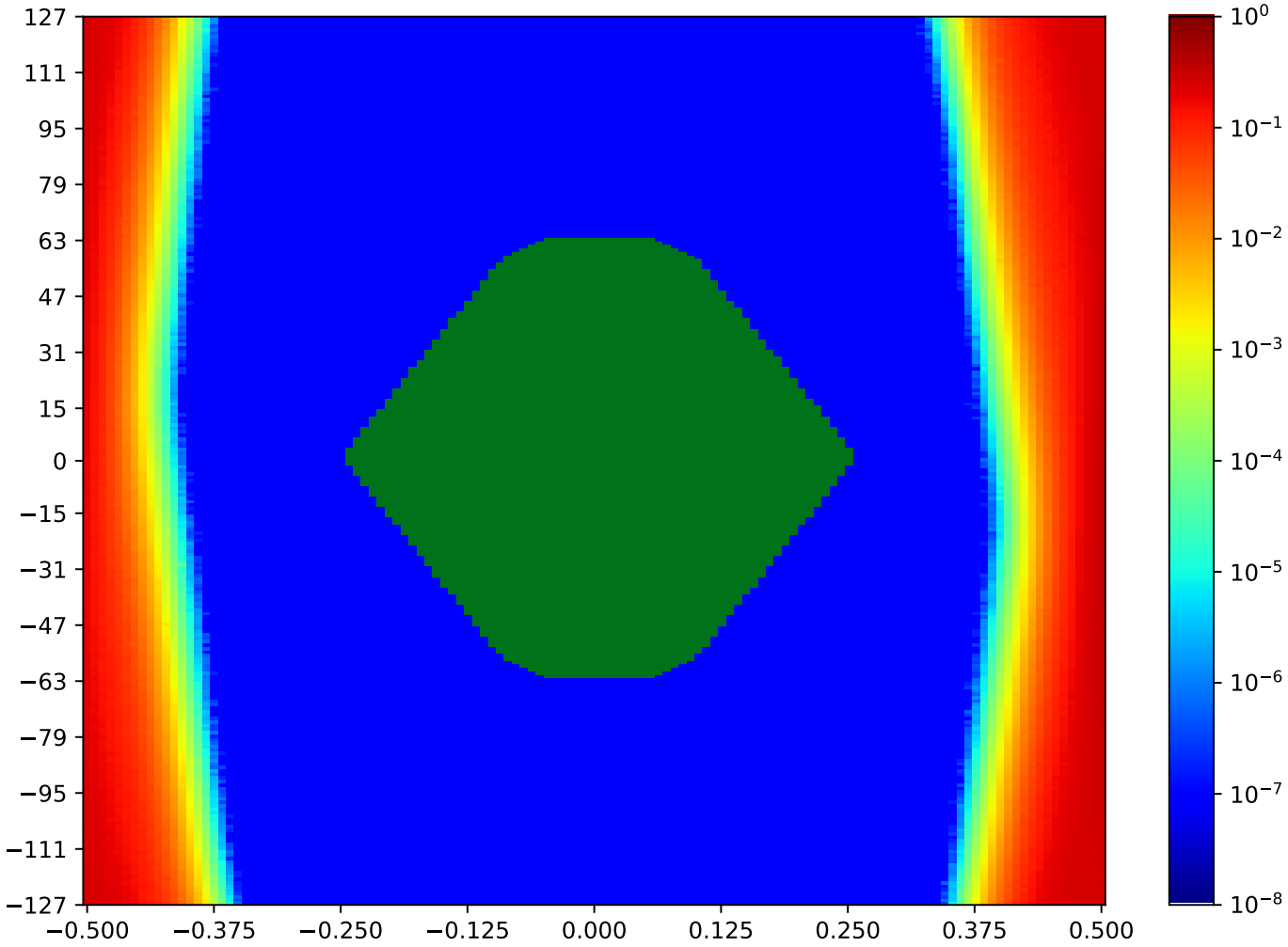


Figure 3.194: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.7 MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Table 3.180: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:03:07		2018-Sep-28 10:04:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24232	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

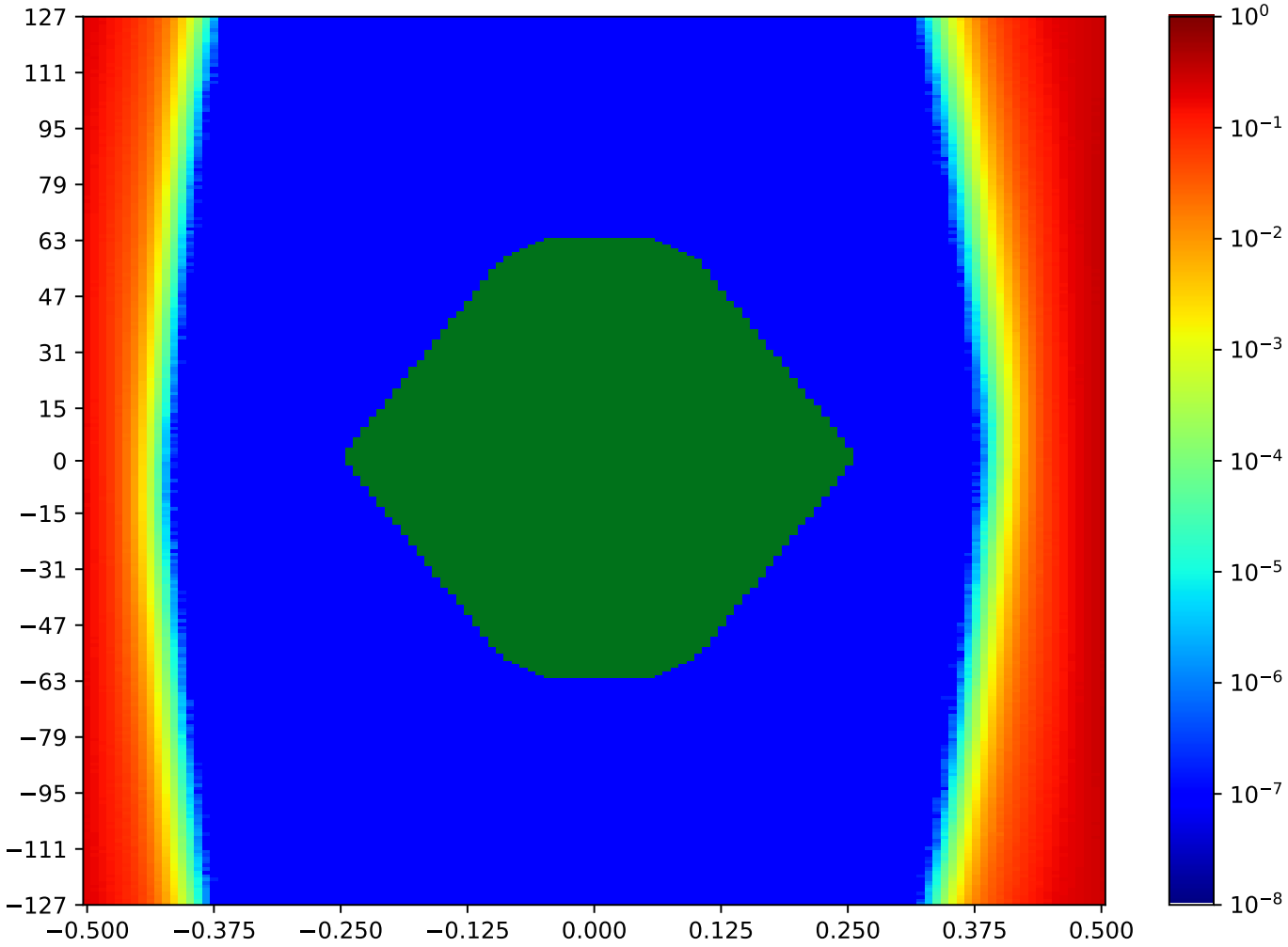


Figure 3.195: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.8 MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Table 3.181: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:51:55		2018-Sep-28 09:53:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24365	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

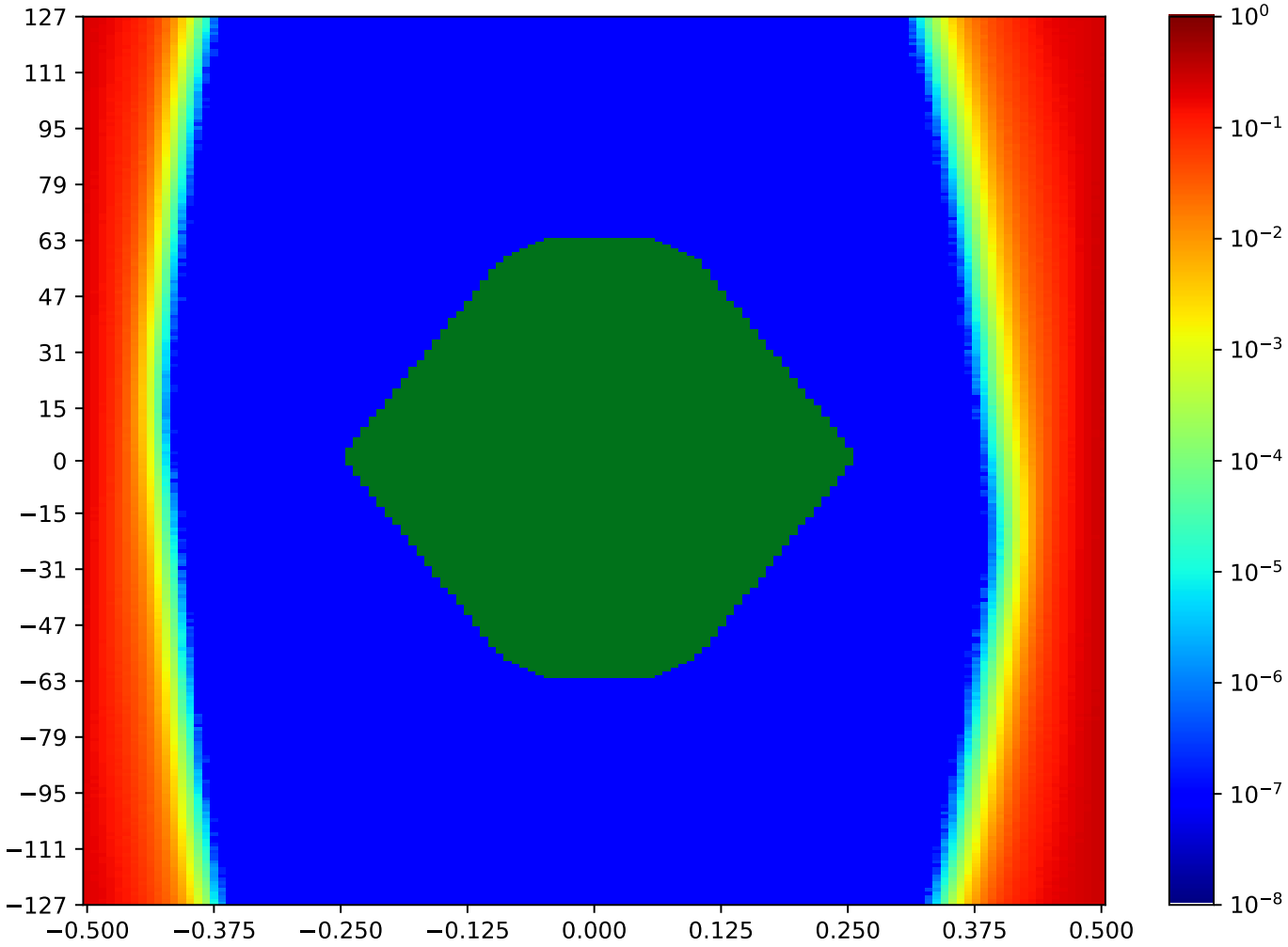


Figure 3.196: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.9 MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Table 3.182: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:01:52		2018-Sep-28 10:03:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24655	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

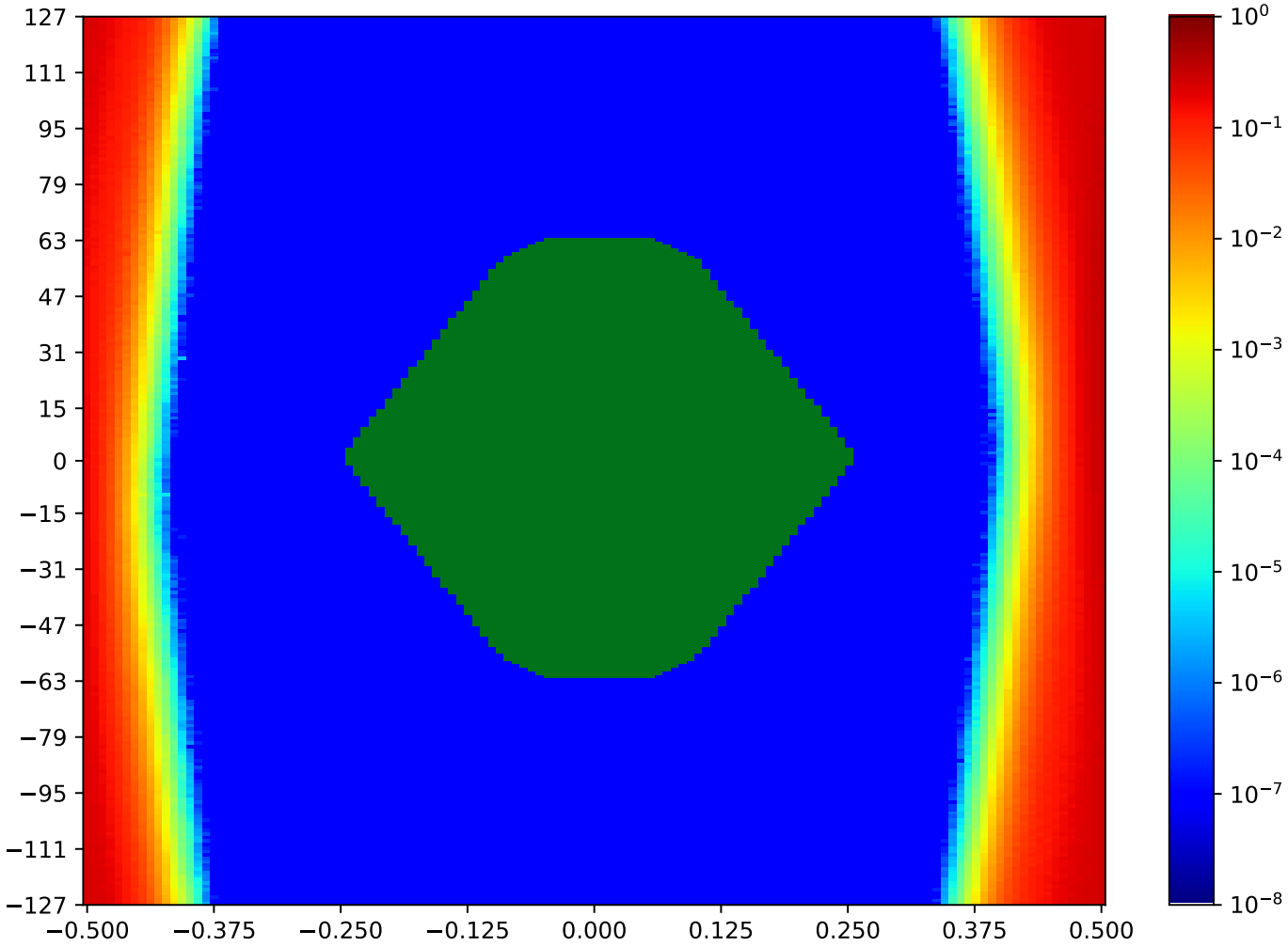


Figure 3.197: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.10 MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Table 3.183: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:54:23		2018-Sep-28 09:55:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24738	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

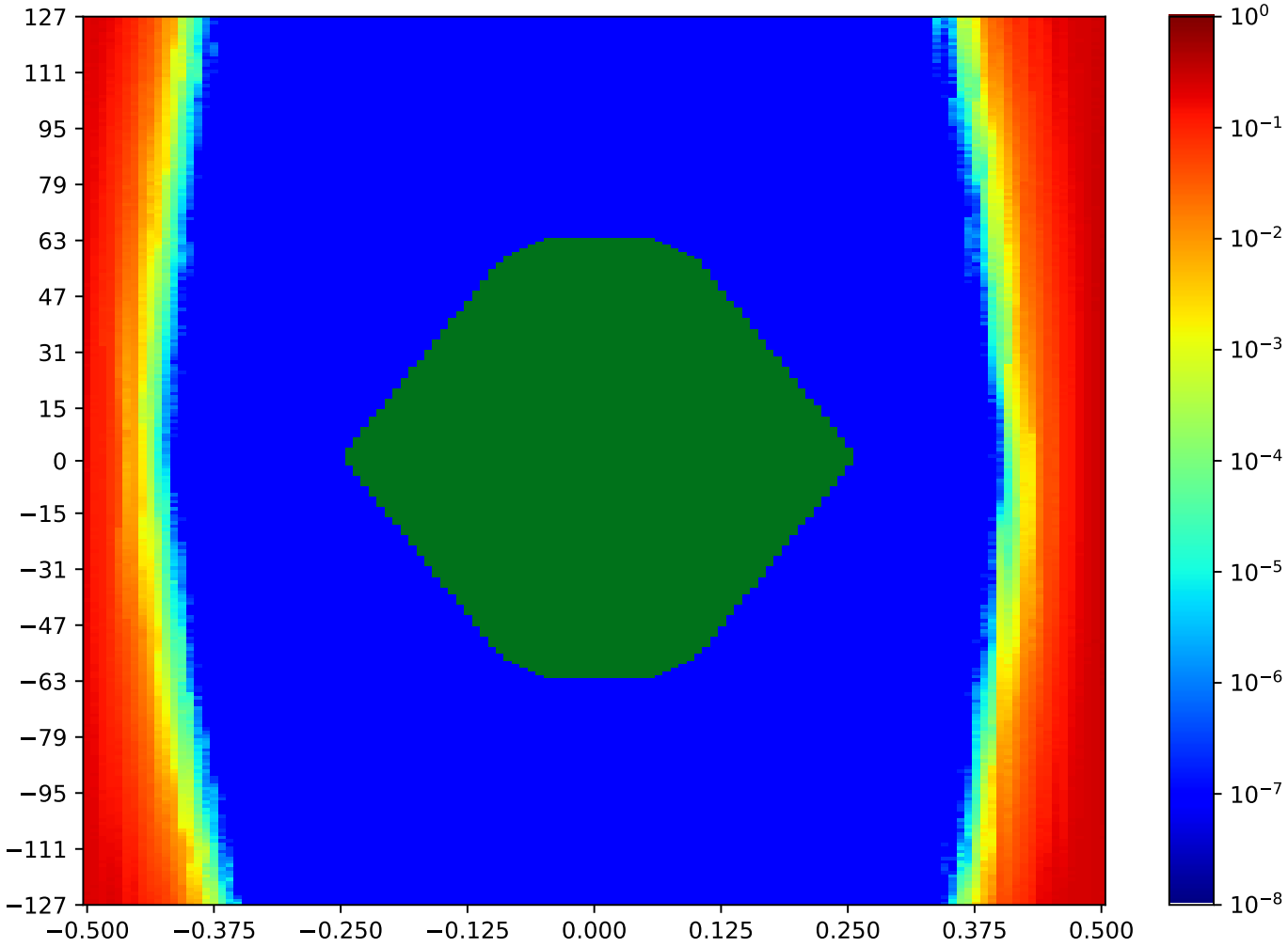


Figure 3.198: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.11 MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Table 3.184: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:59:23		2018-Sep-28 10:00:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24015	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

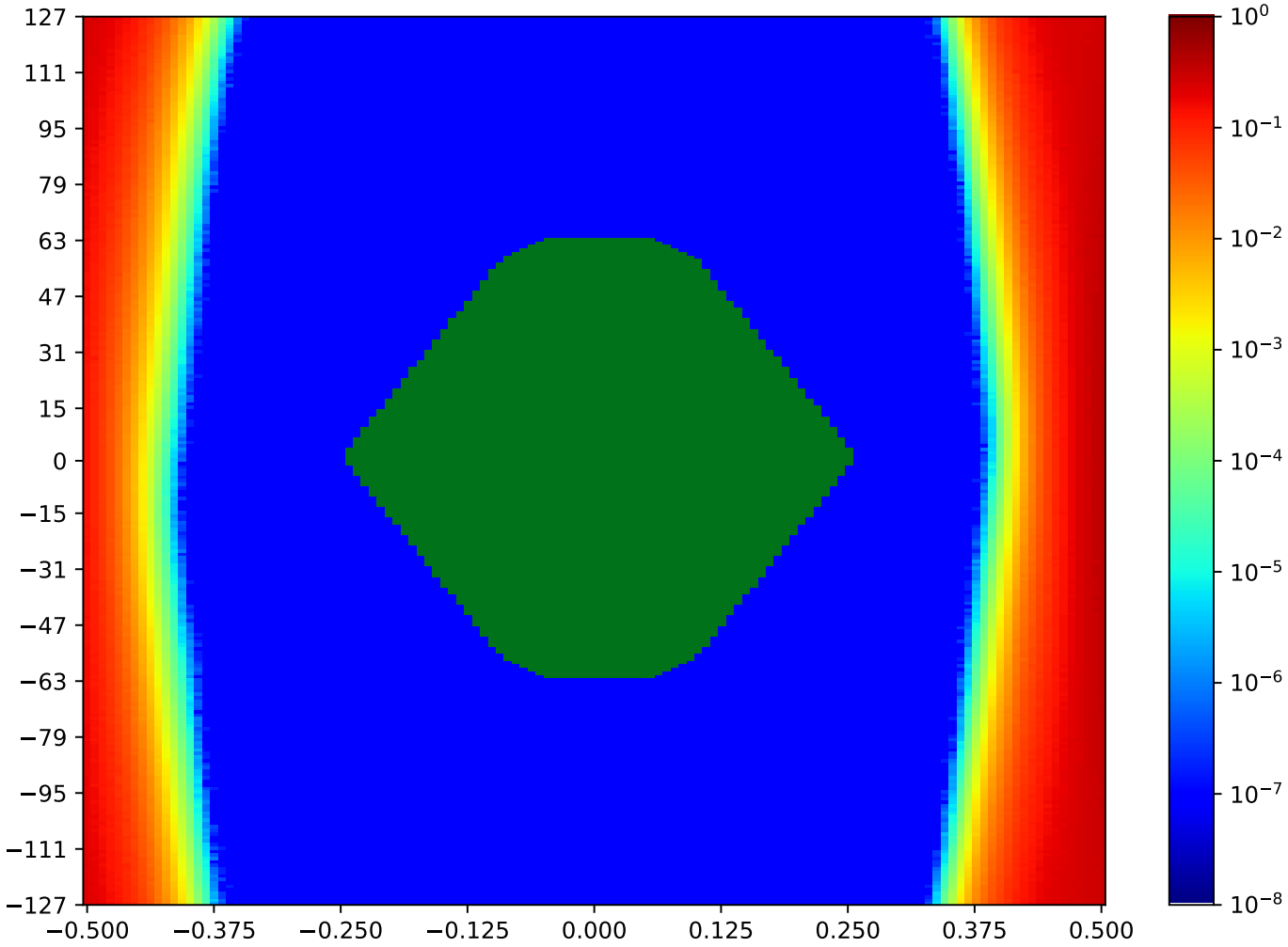


Figure 3.199: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.15.12 MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Table 3.185: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:58:08		2018-Sep-28 09:59:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24716	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

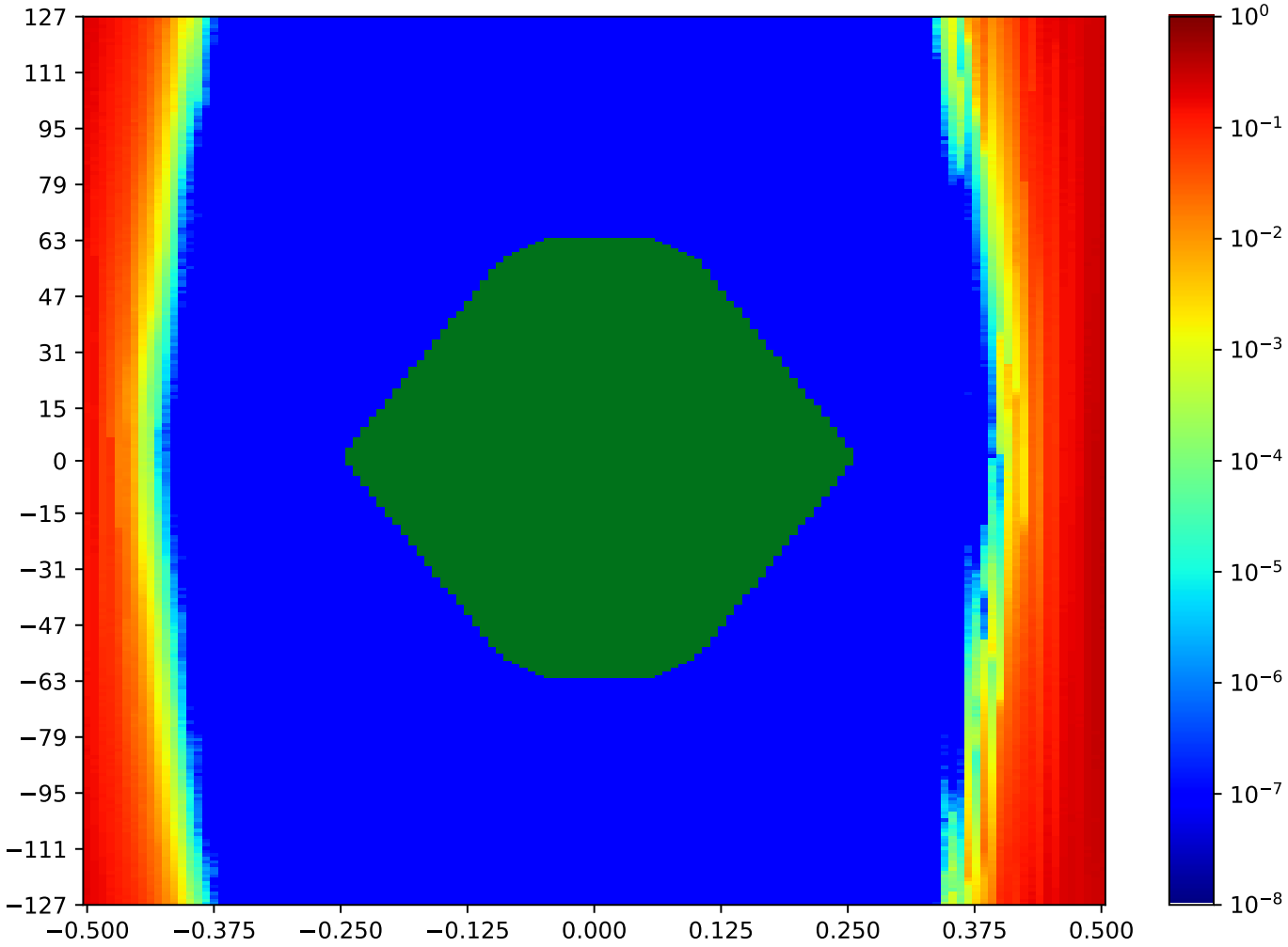


Figure 3.200: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16 MSP_A TX2 MSP_C RX11 Minipod Loopback

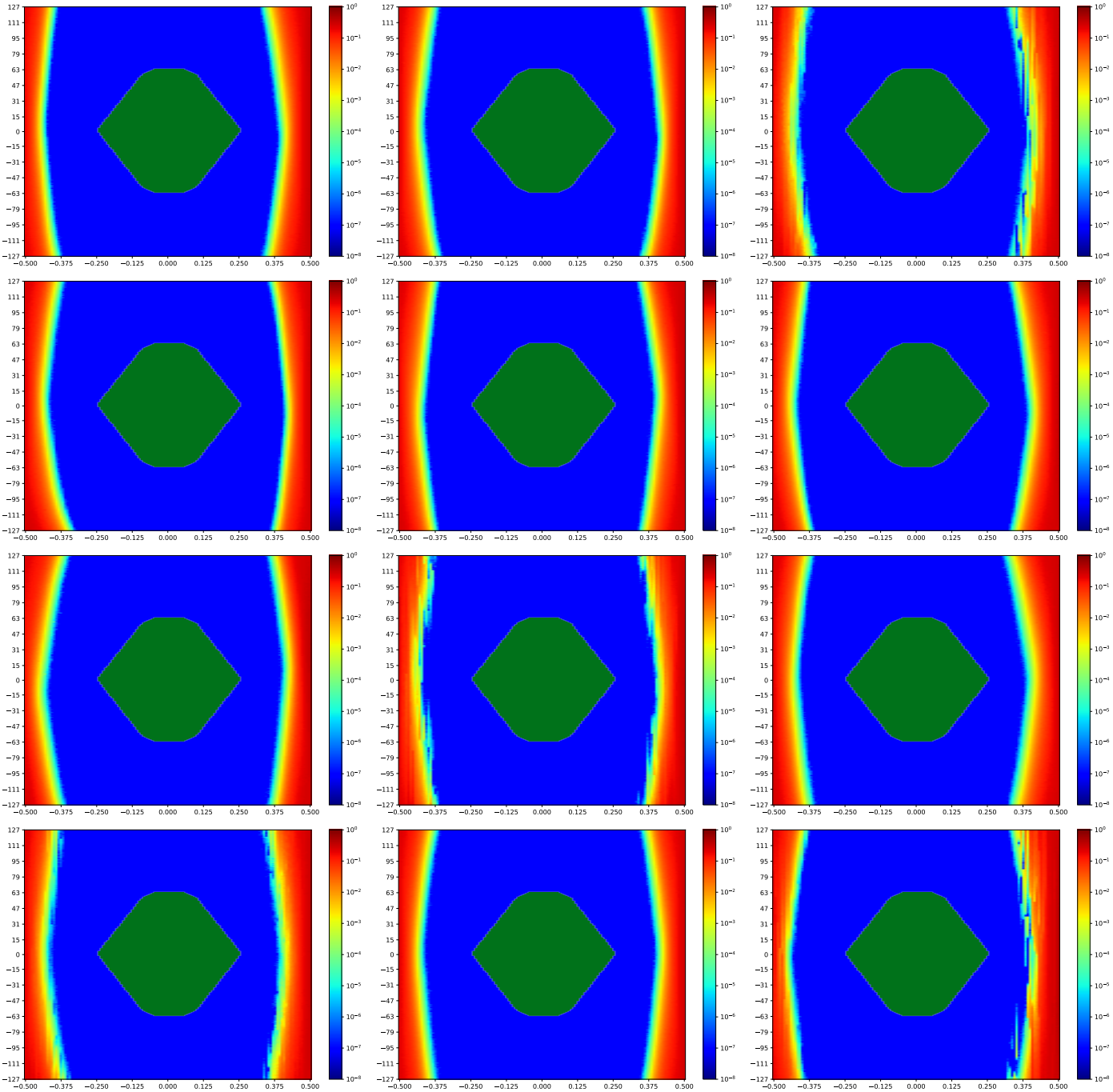


Figure 3.201: MSP_A TX2 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.214.

3.16.1 MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Table 3.186: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:08:07		2018-Sep-28 10:09:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24614	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

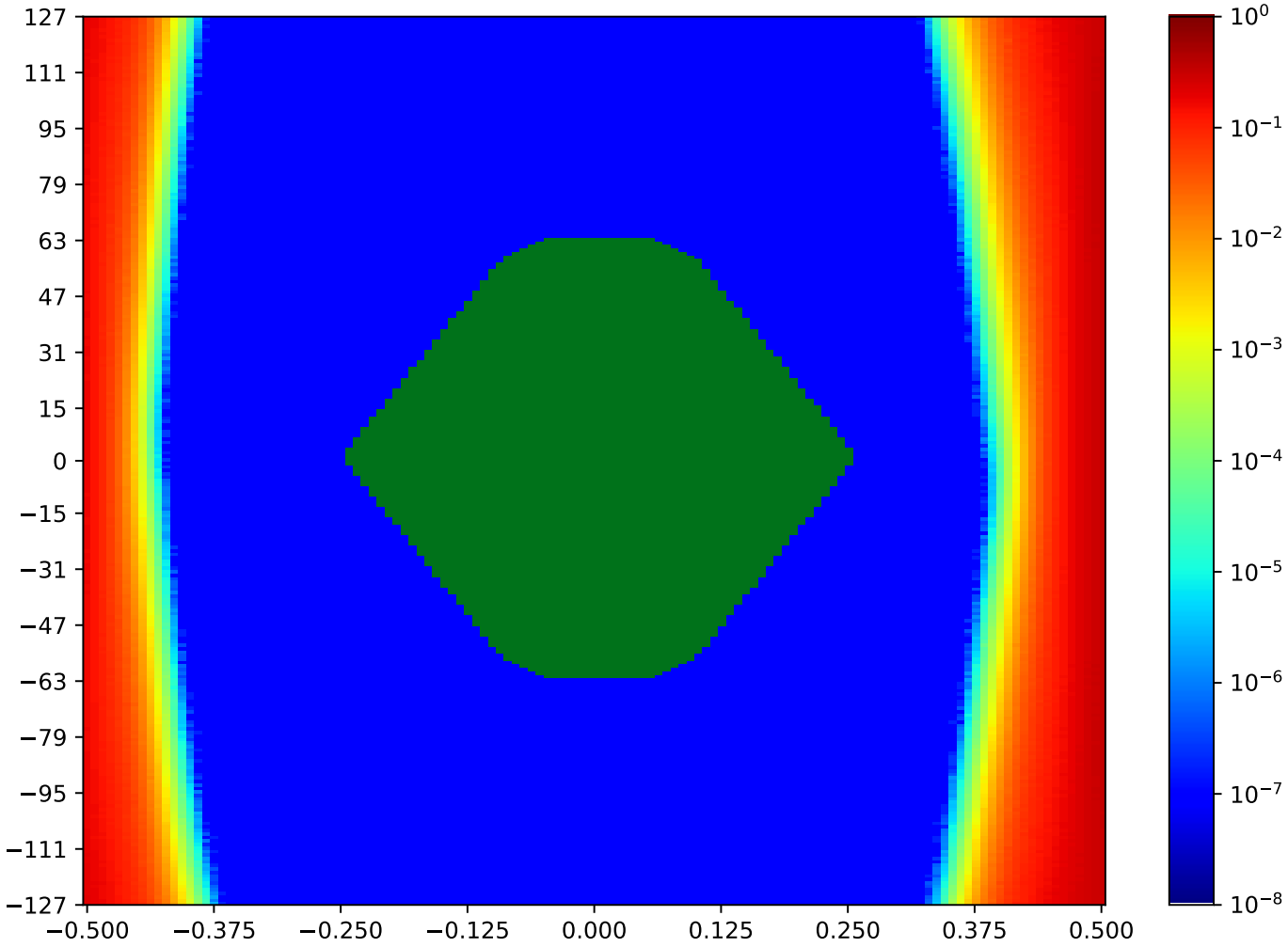


Figure 3.202: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.2 MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Table 3.187: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:05:37		2018-Sep-28 10:06:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24513	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

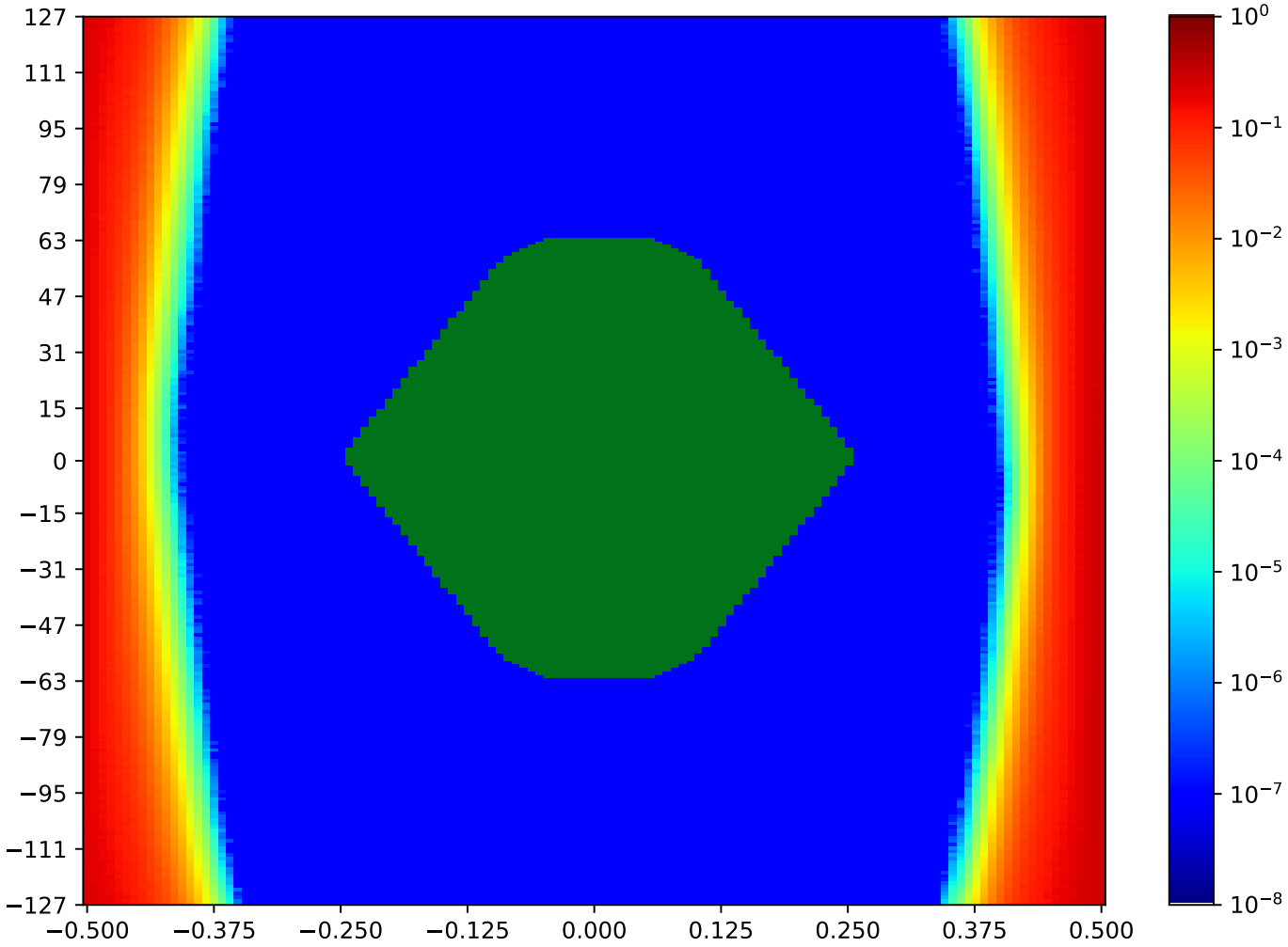


Figure 3.203: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.3 MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Table 3.188: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:11:53		2018-Sep-28 10:13:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23833	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

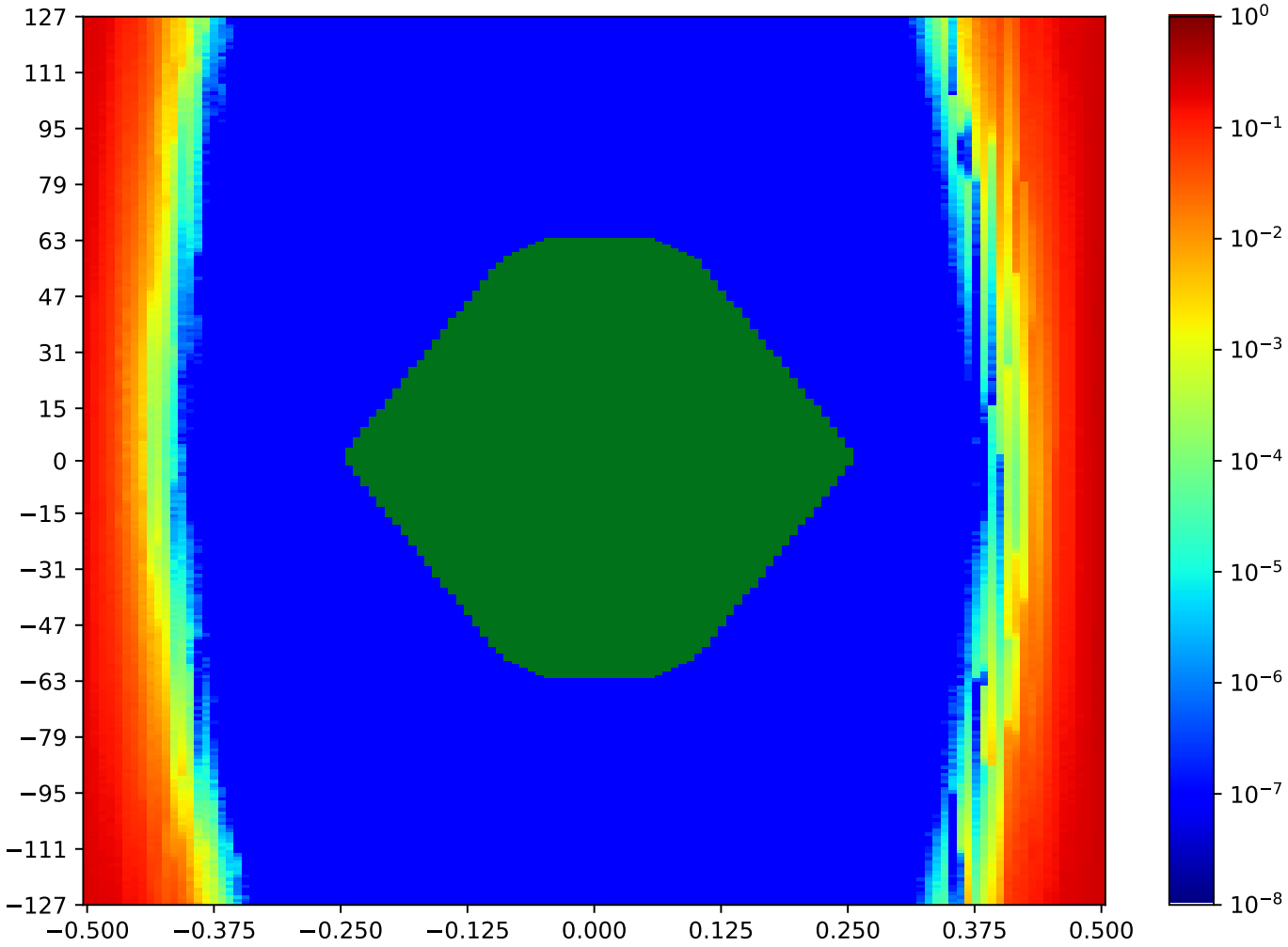


Figure 3.204: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.4 MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Table 3.189: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:04:22		2018-Sep-28 10:05:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24778	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

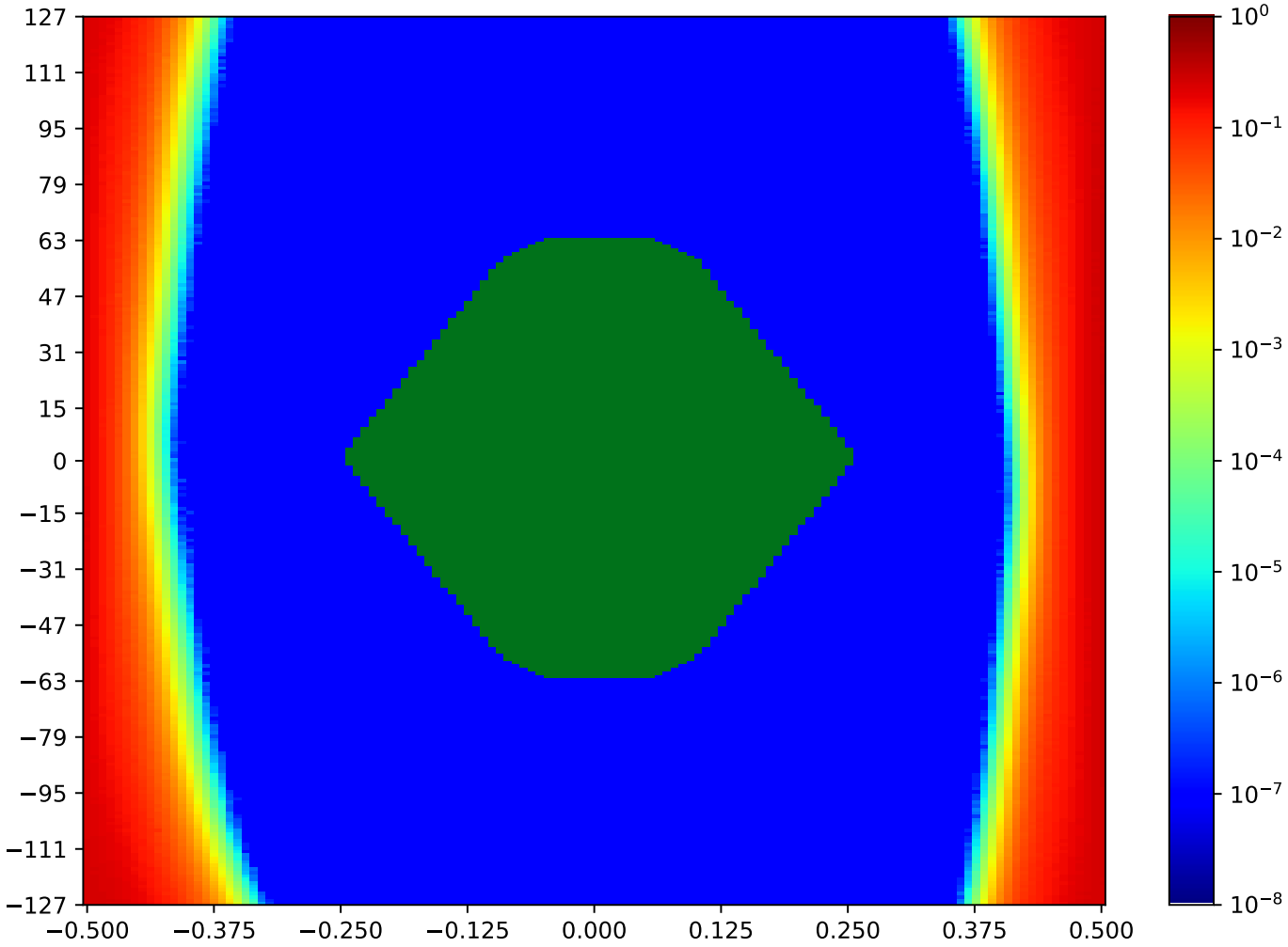


Figure 3.205: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.5 MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Table 3.190: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:15:40		2018-Sep-28 10:16:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24188	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

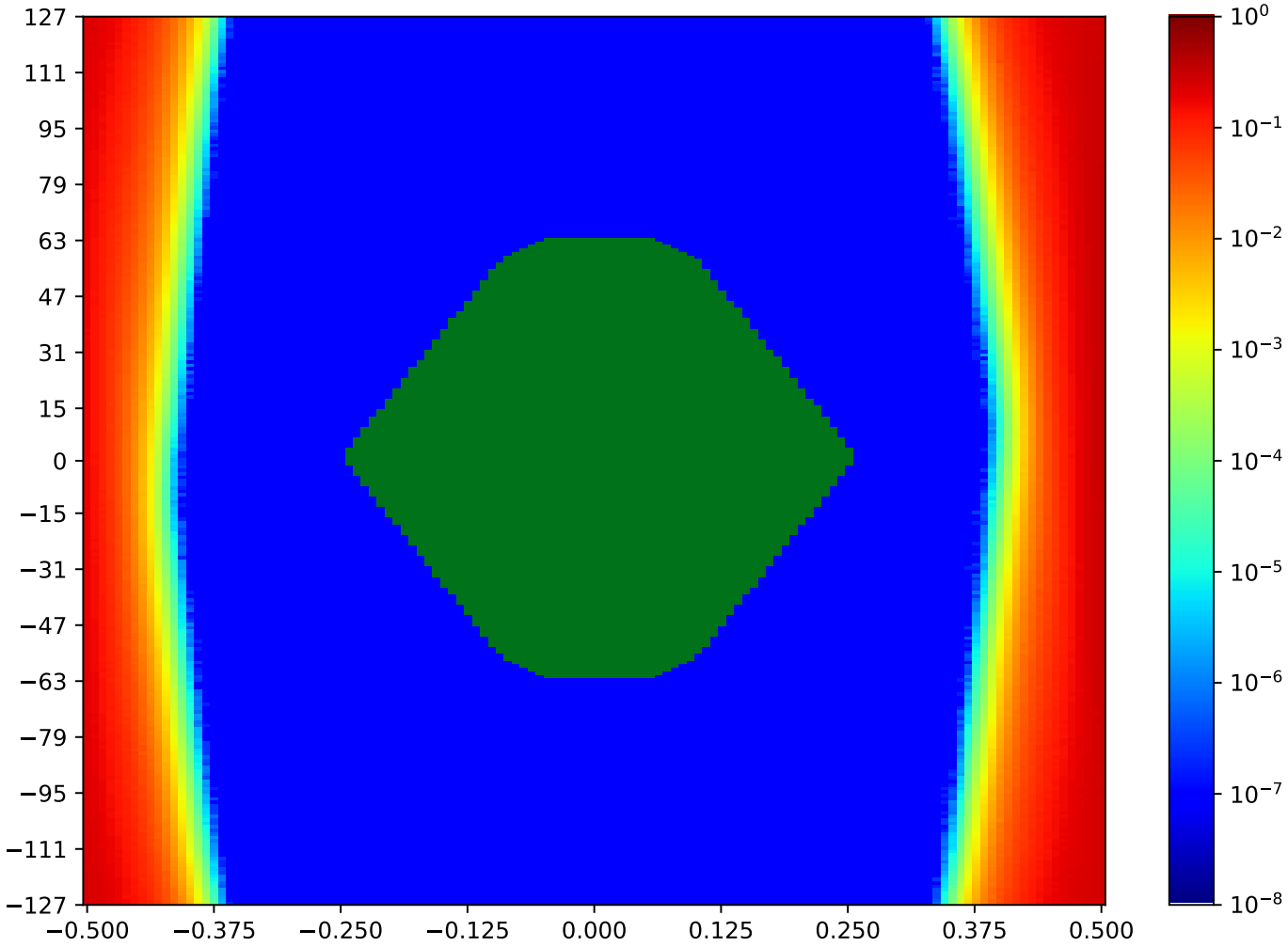


Figure 3.206: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.6 MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Table 3.191: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:06:52		2018-Sep-28 10:08:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24180	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

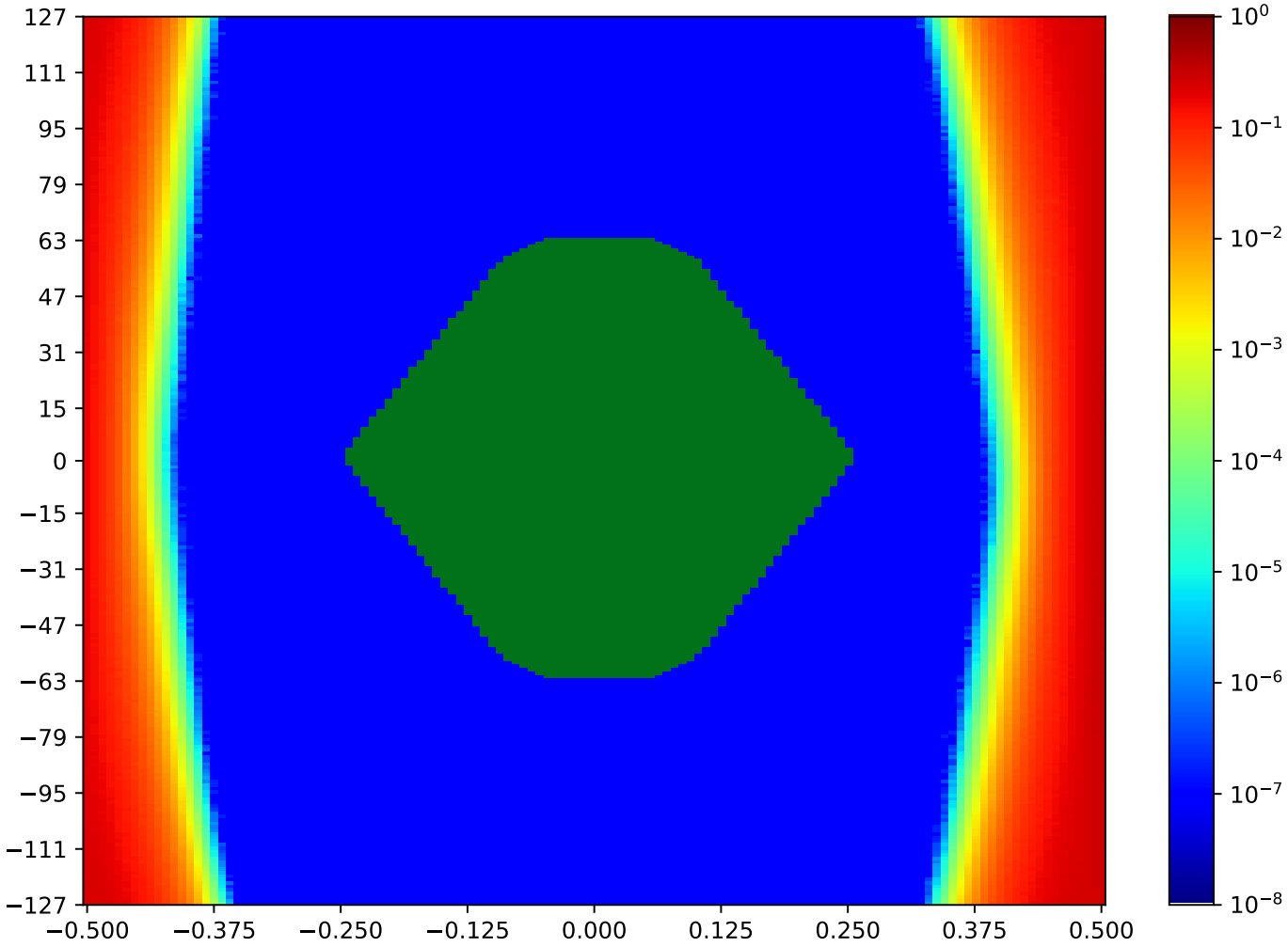


Figure 3.207: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.7 MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Table 3.192: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:18:11		2018-Sep-28 10:19:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24557	104	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

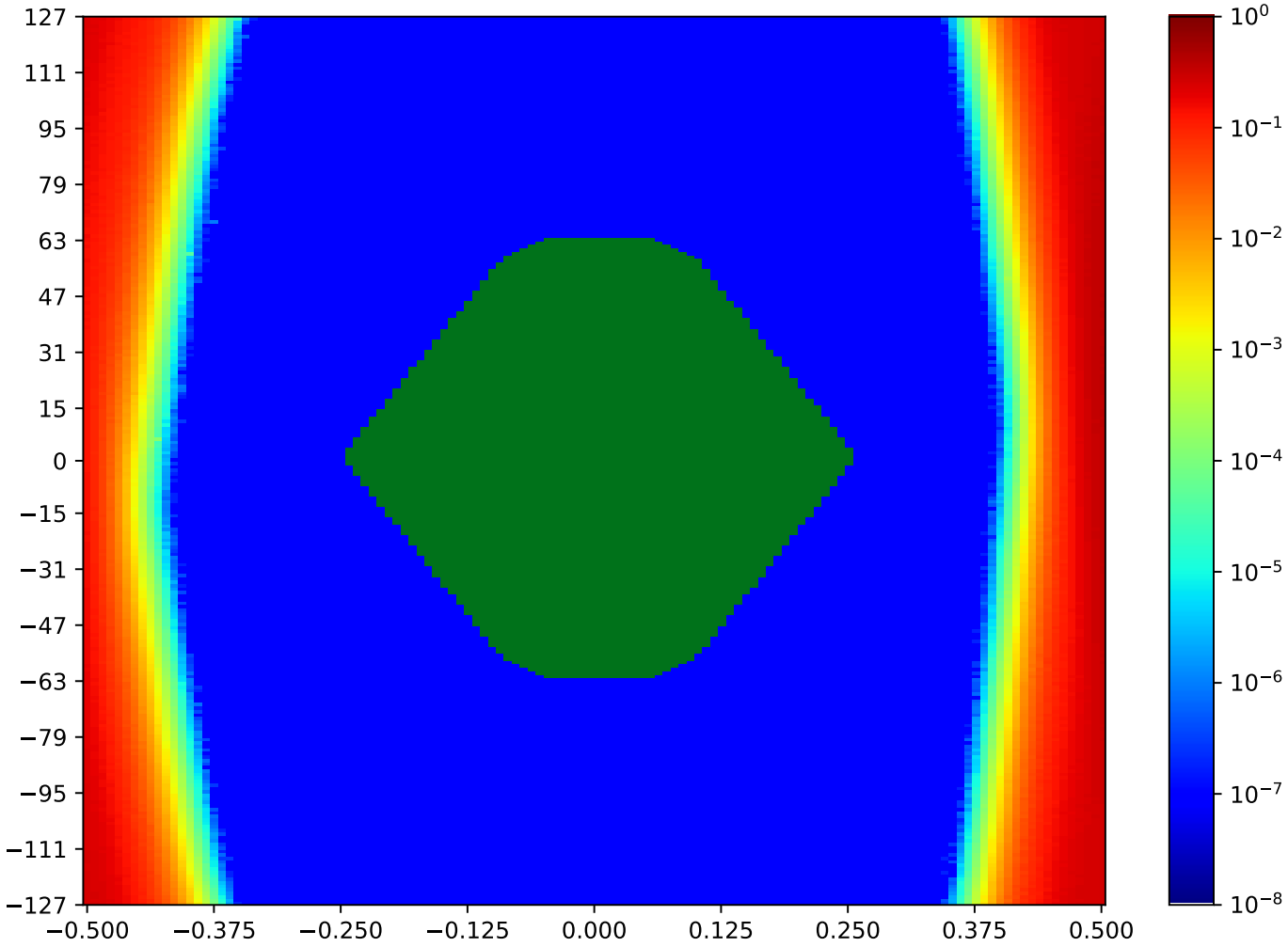


Figure 3.208: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.8 MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Table 3.193: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:09:22		2018-Sep-28 10:10:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24604	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

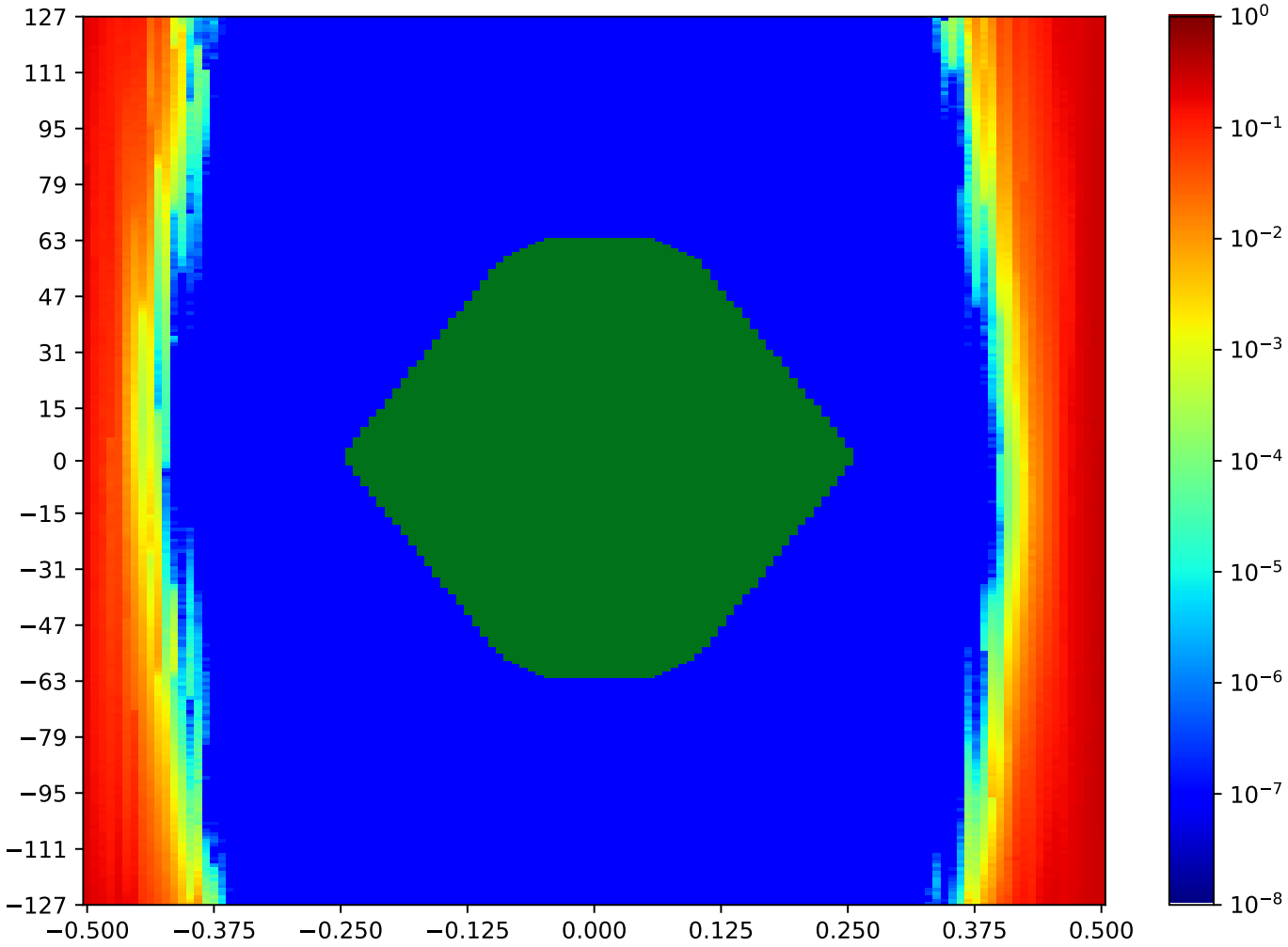


Figure 3.209: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.9 MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Table 3.194: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:16:55		2018-Sep-28 10:18:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23572	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

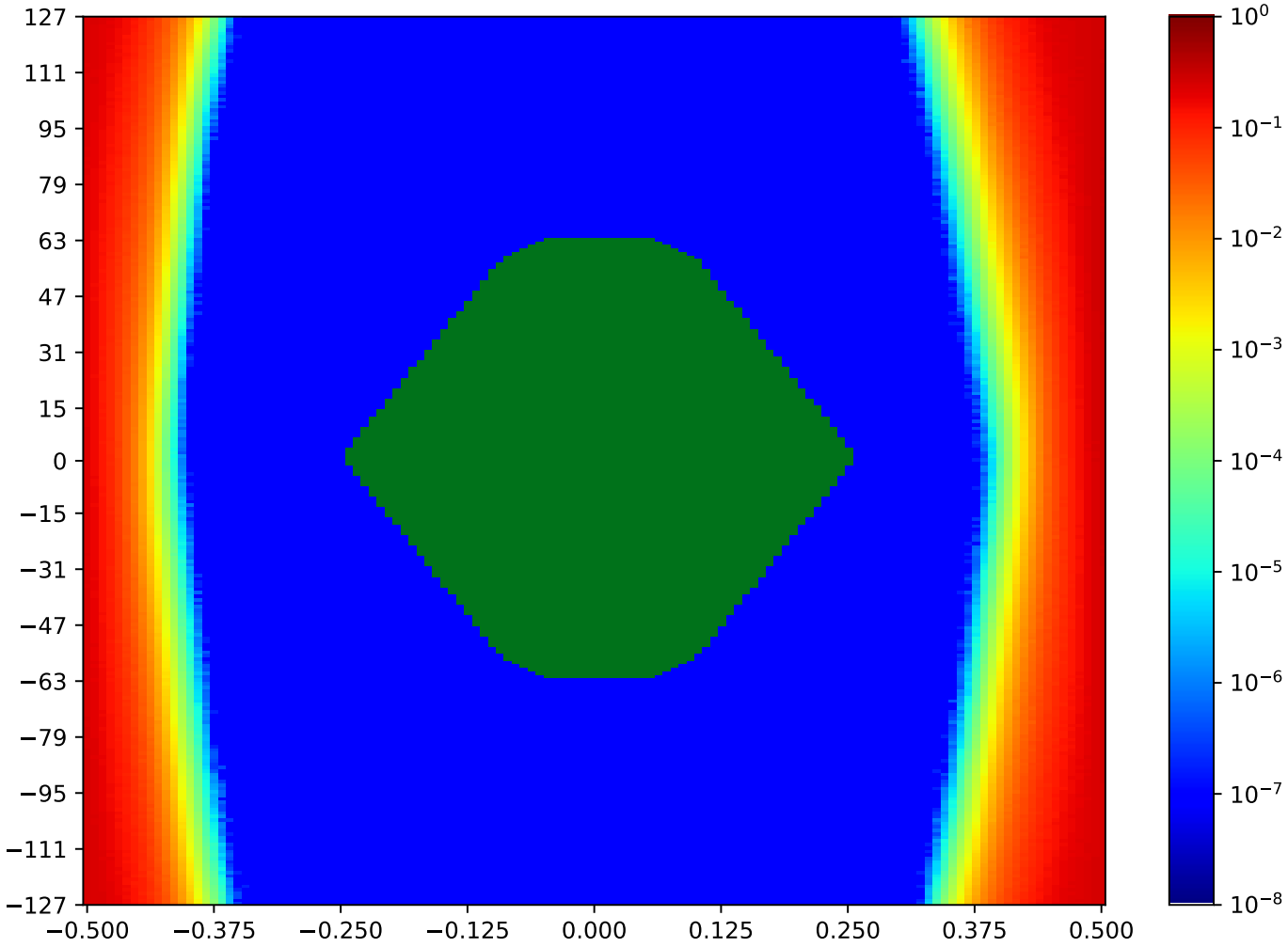


Figure 3.210: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.10 MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Table 3.195: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:10:38		2018-Sep-28 10:11:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24031	101	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

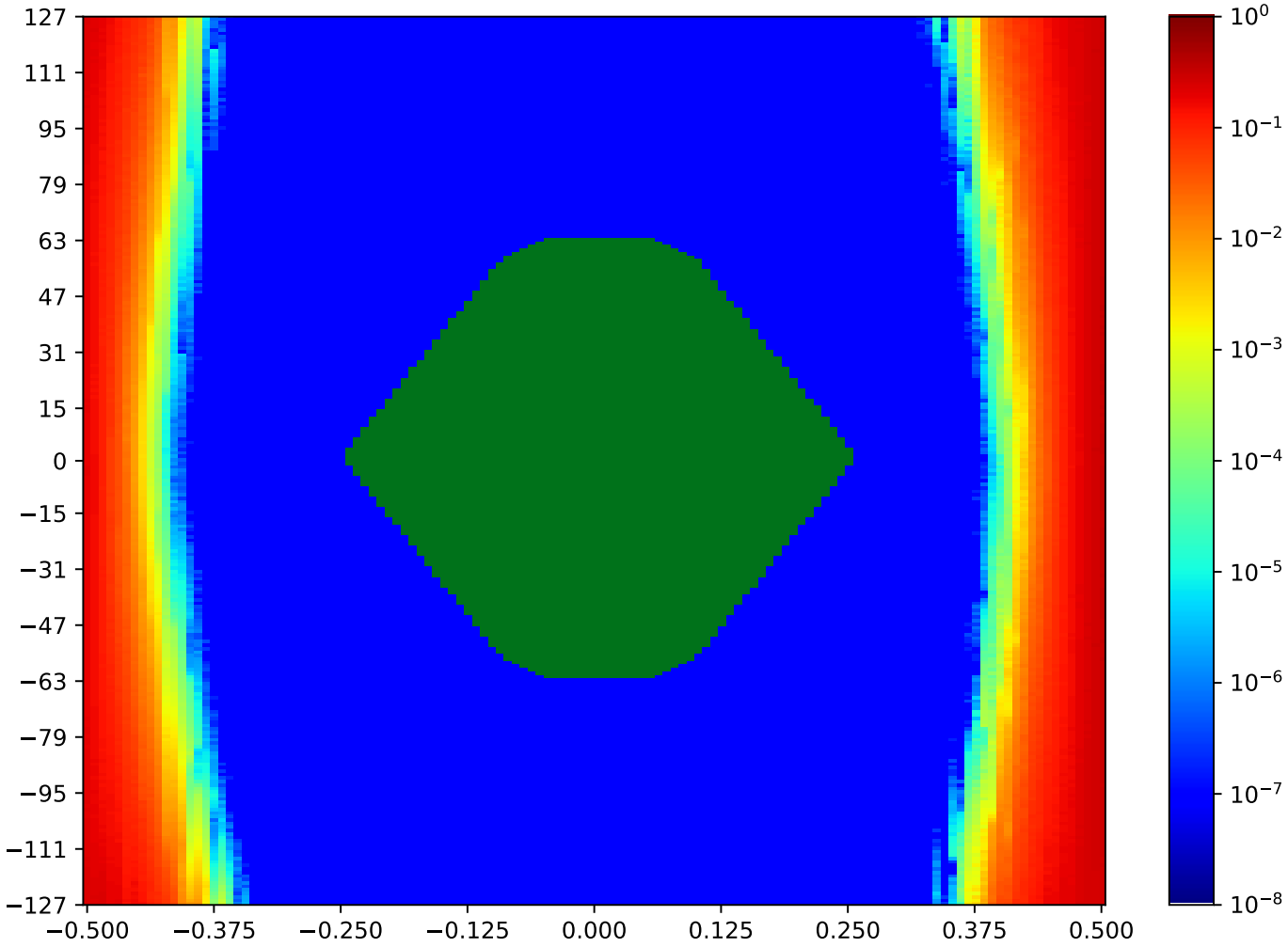


Figure 3.211: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.11 MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Table 3.196: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:14:24		2018-Sep-28 10:15:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24495	103	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

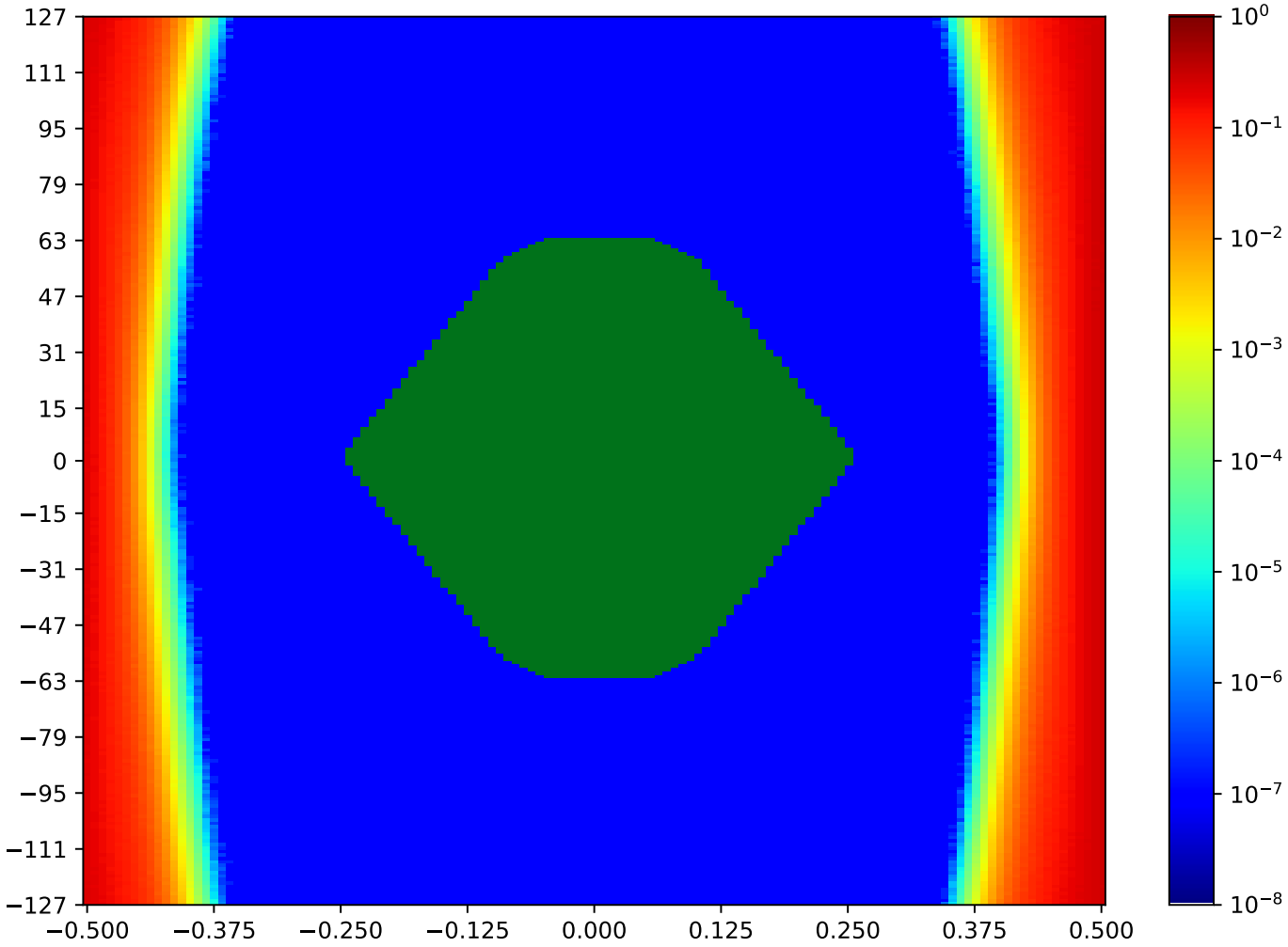


Figure 3.212: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.16.12 MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Table 3.197: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:13:09		2018-Sep-28 10:14:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24908	105	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

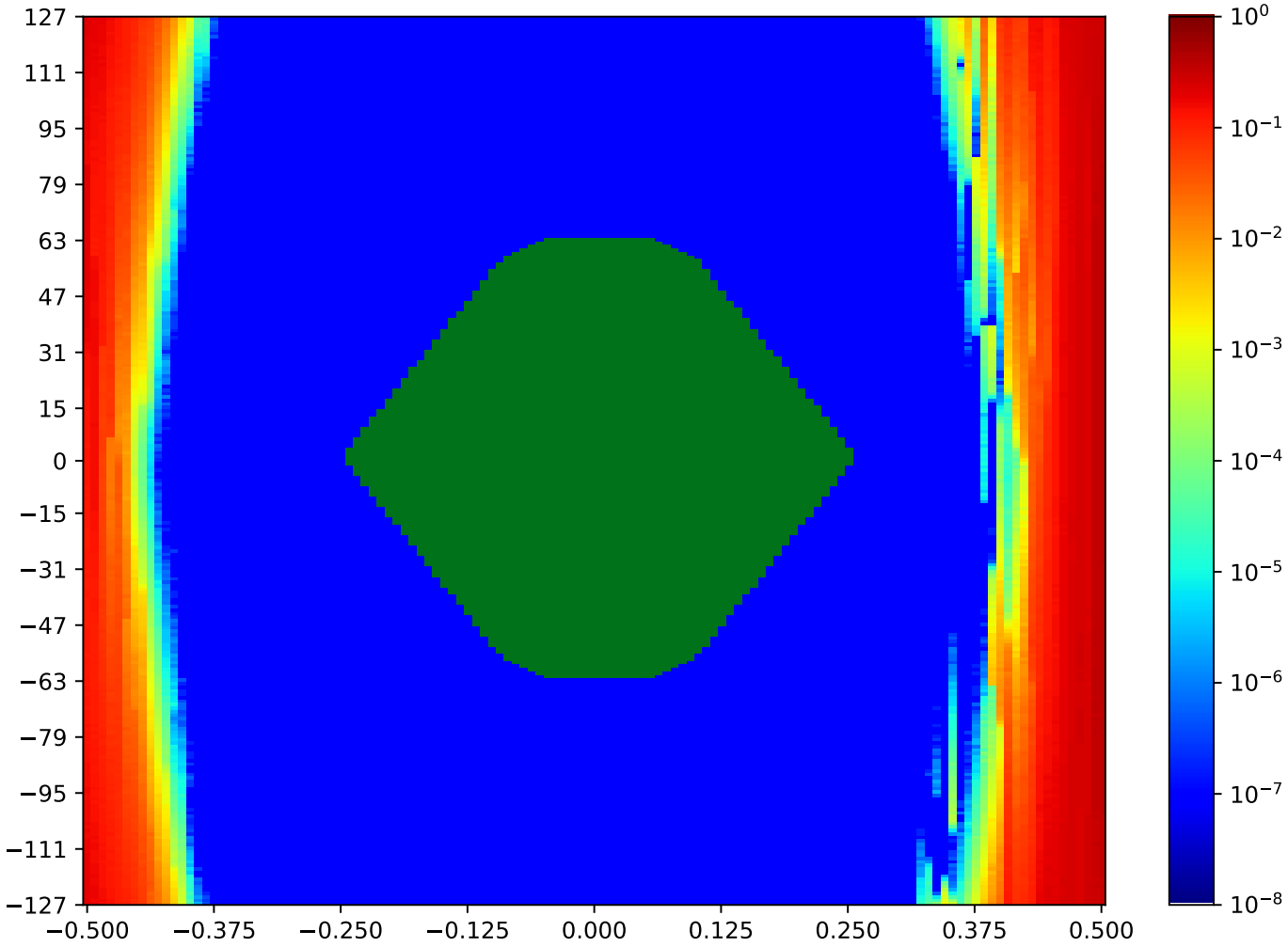


Figure 3.213: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17 MSP_C TX3 MSP_A RX1 Minipod Loopback

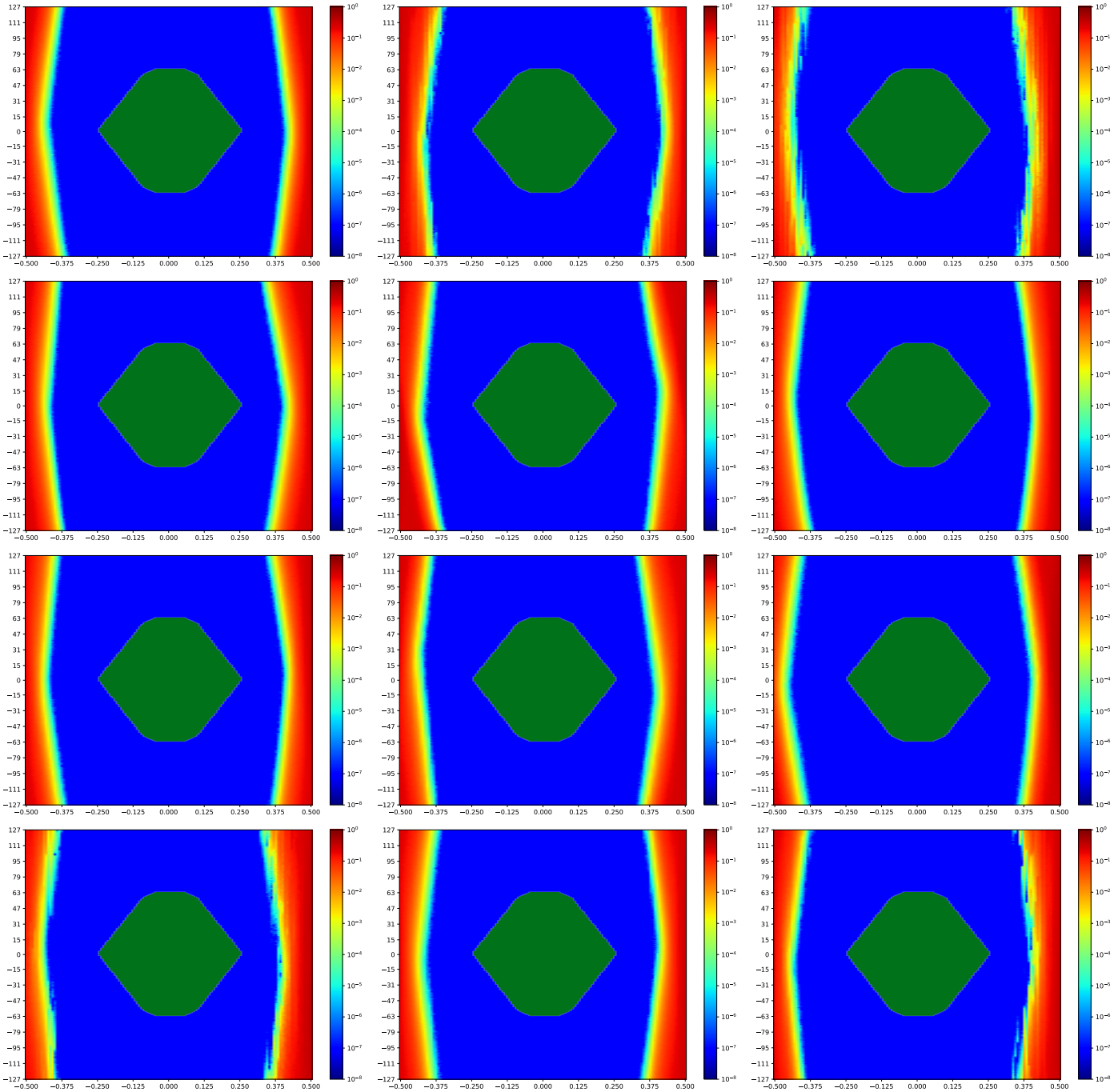


Figure 3.214: MSP_C TX3 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.227.

3.17.1 MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Table 3.198: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:23:13		2018-Sep-28 10:24:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24574	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

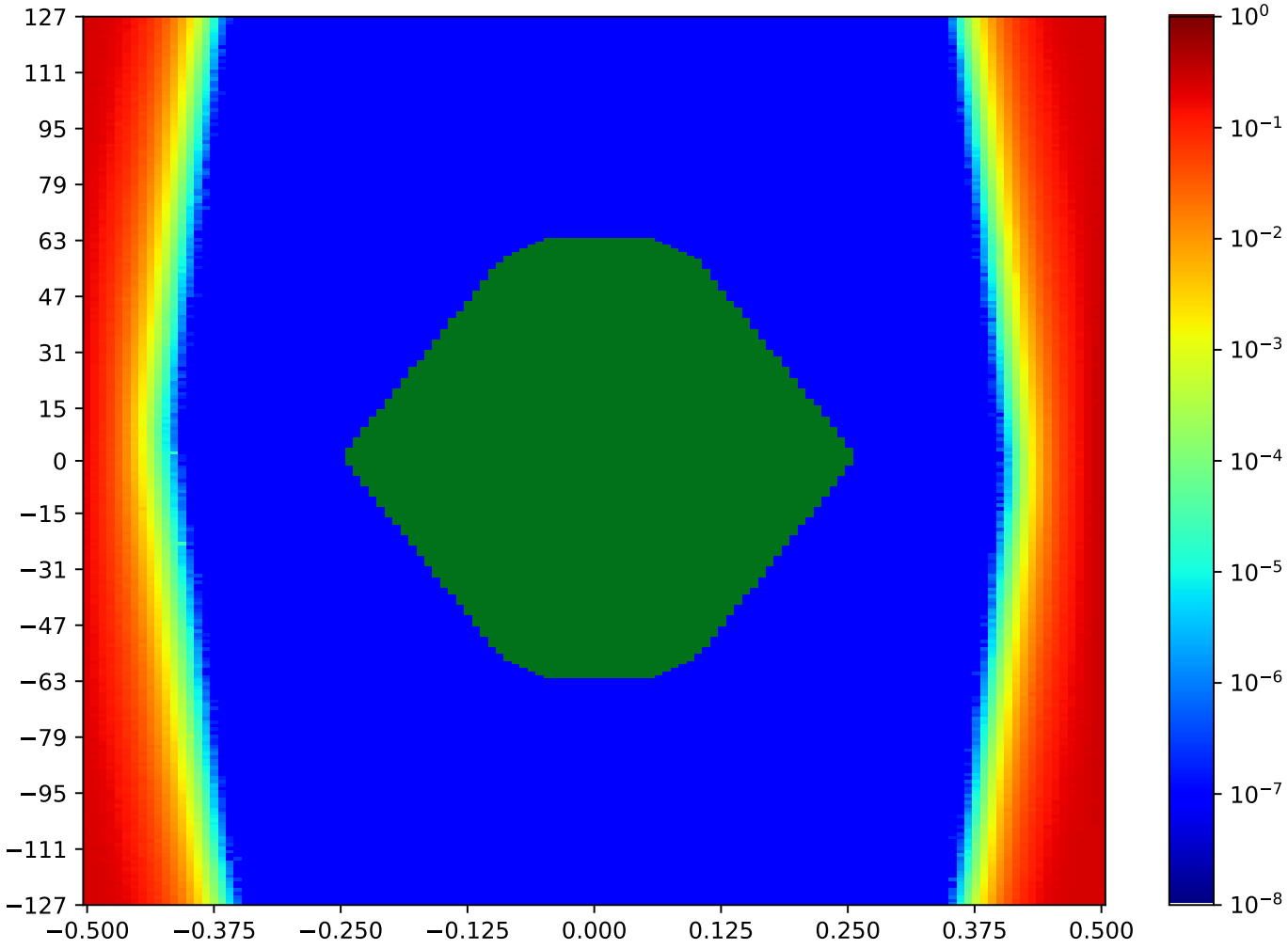


Figure 3.215: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.2 MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Table 3.199: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:25:44		2018-Sep-28 10:26:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24529	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

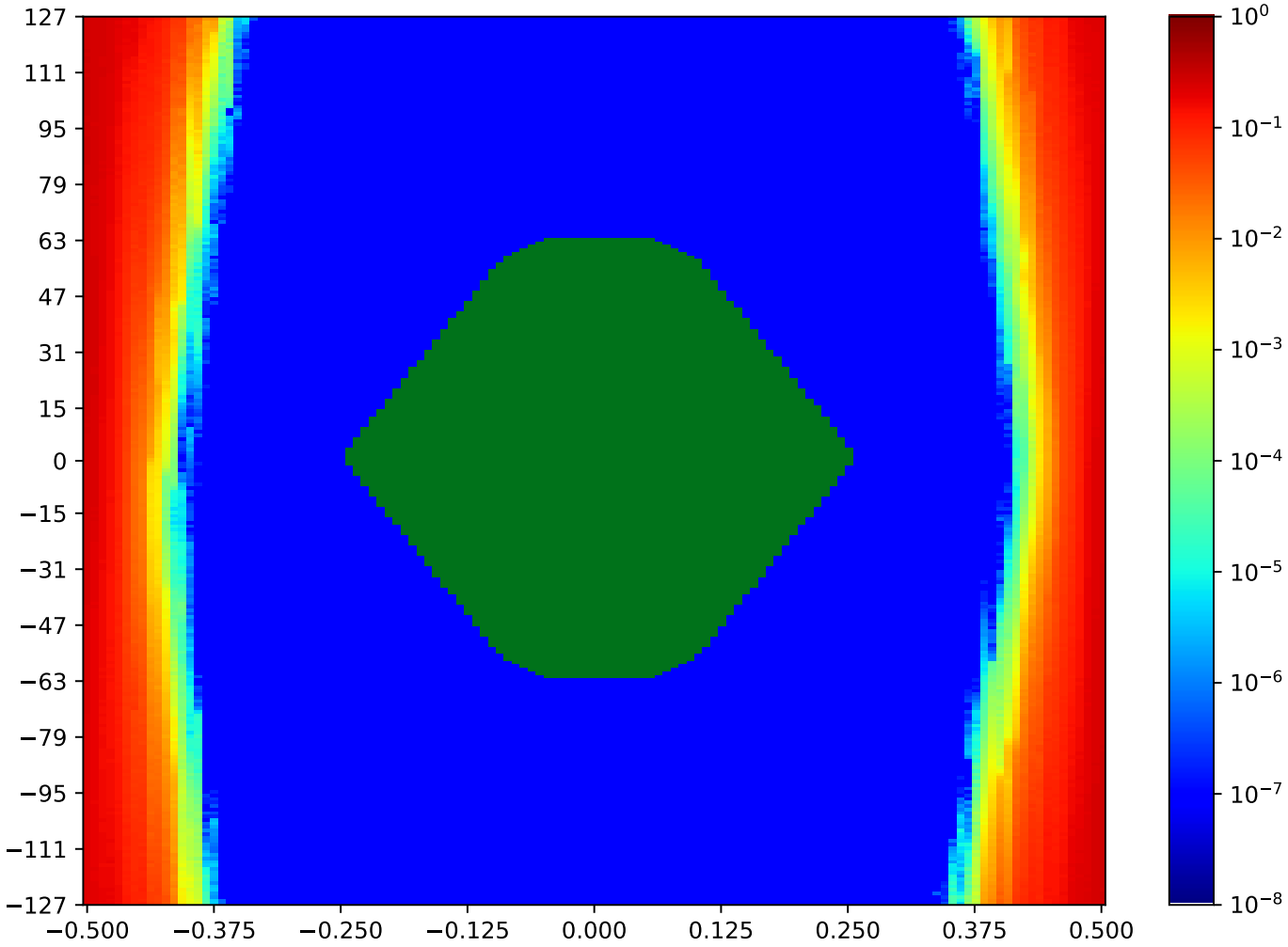


Figure 3.216: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.3 MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Table 3.200: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:26:59		2018-Sep-28 10:28:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24395	103	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

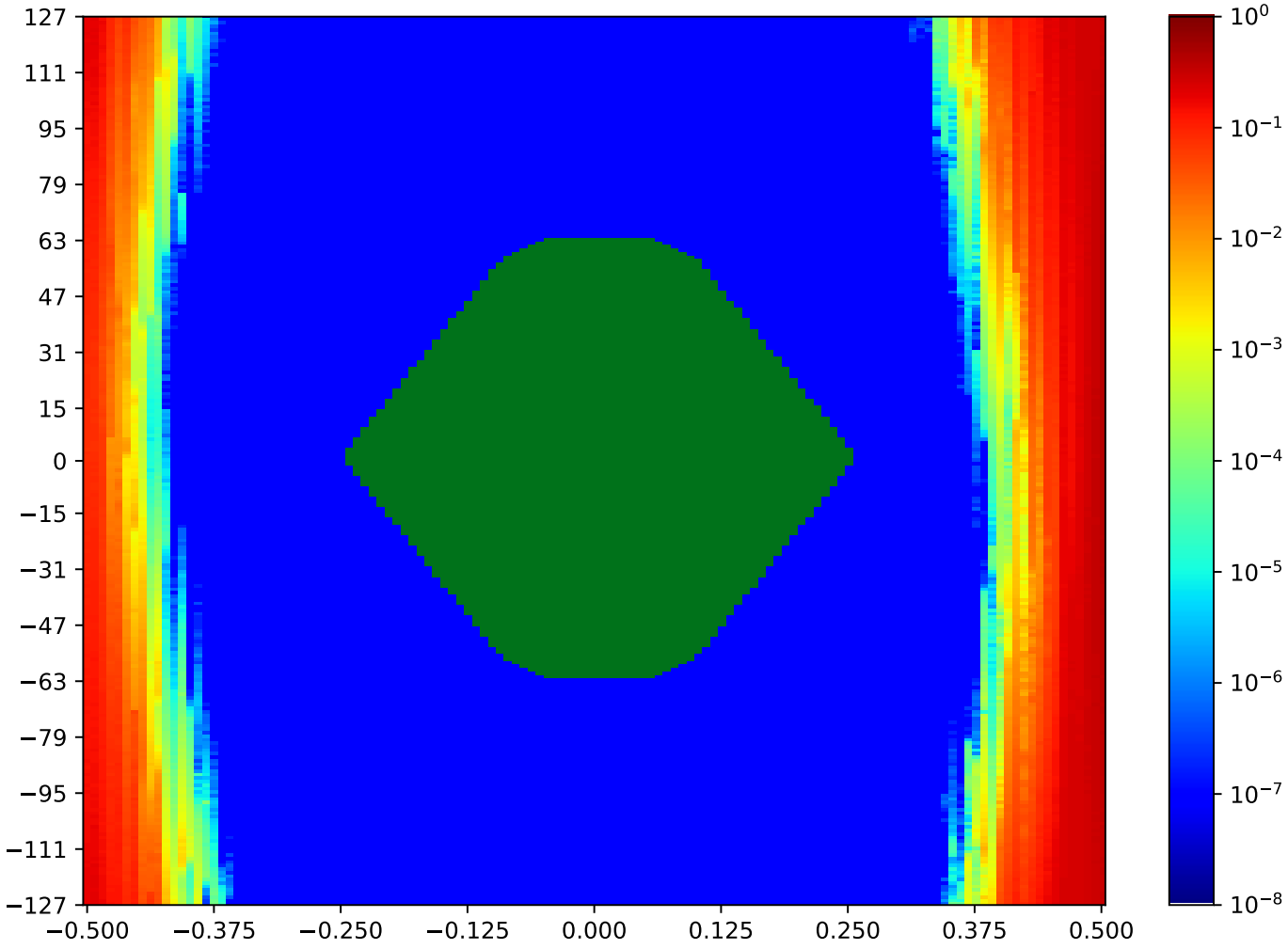


Figure 3.217: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.4 MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Table 3.201: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:20:42		2018-Sep-28 10:21:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24159	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

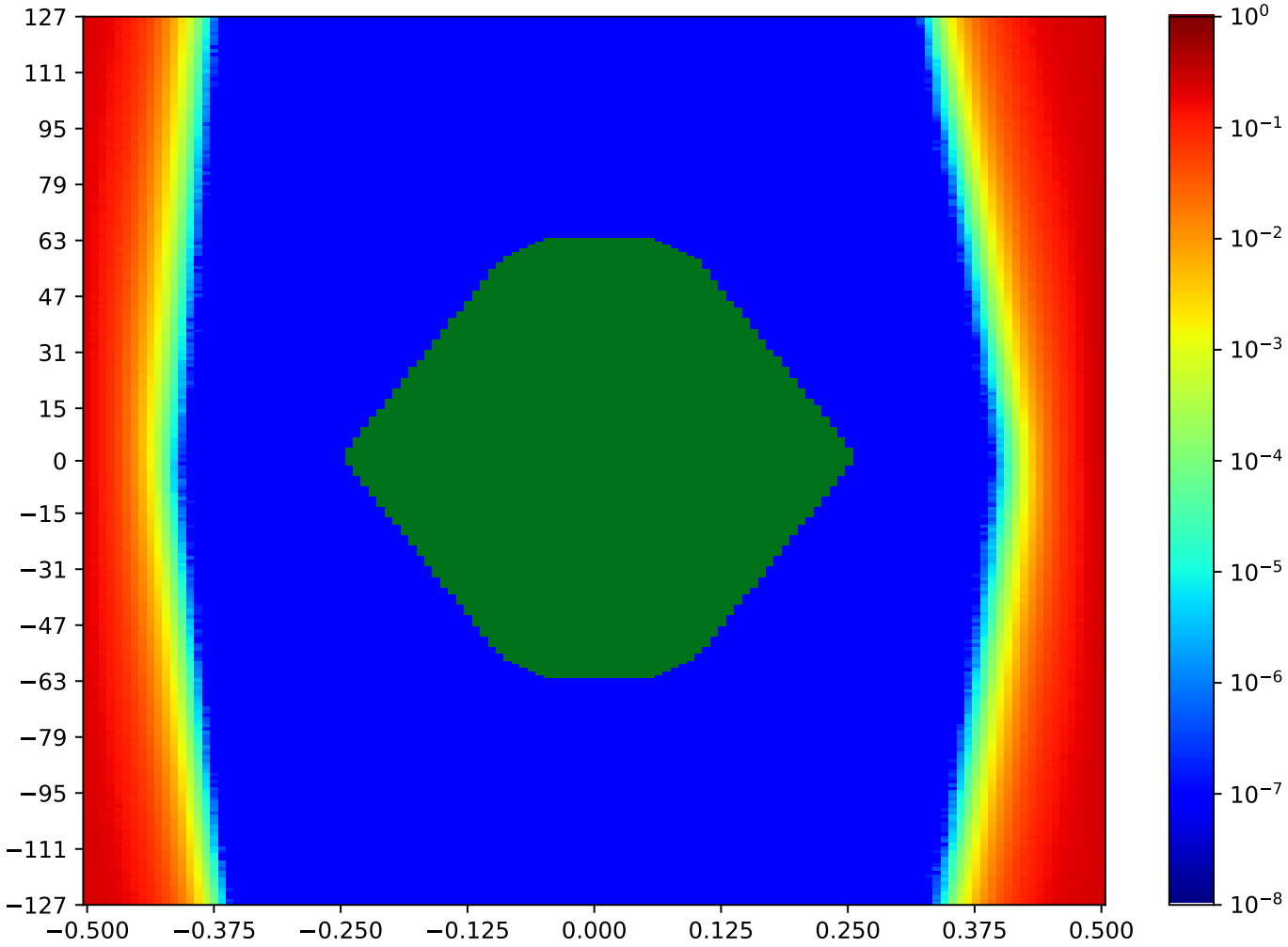


Figure 3.218: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.5 MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Table 3.202: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:30:46		2018-Sep-28 10:32:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24225	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

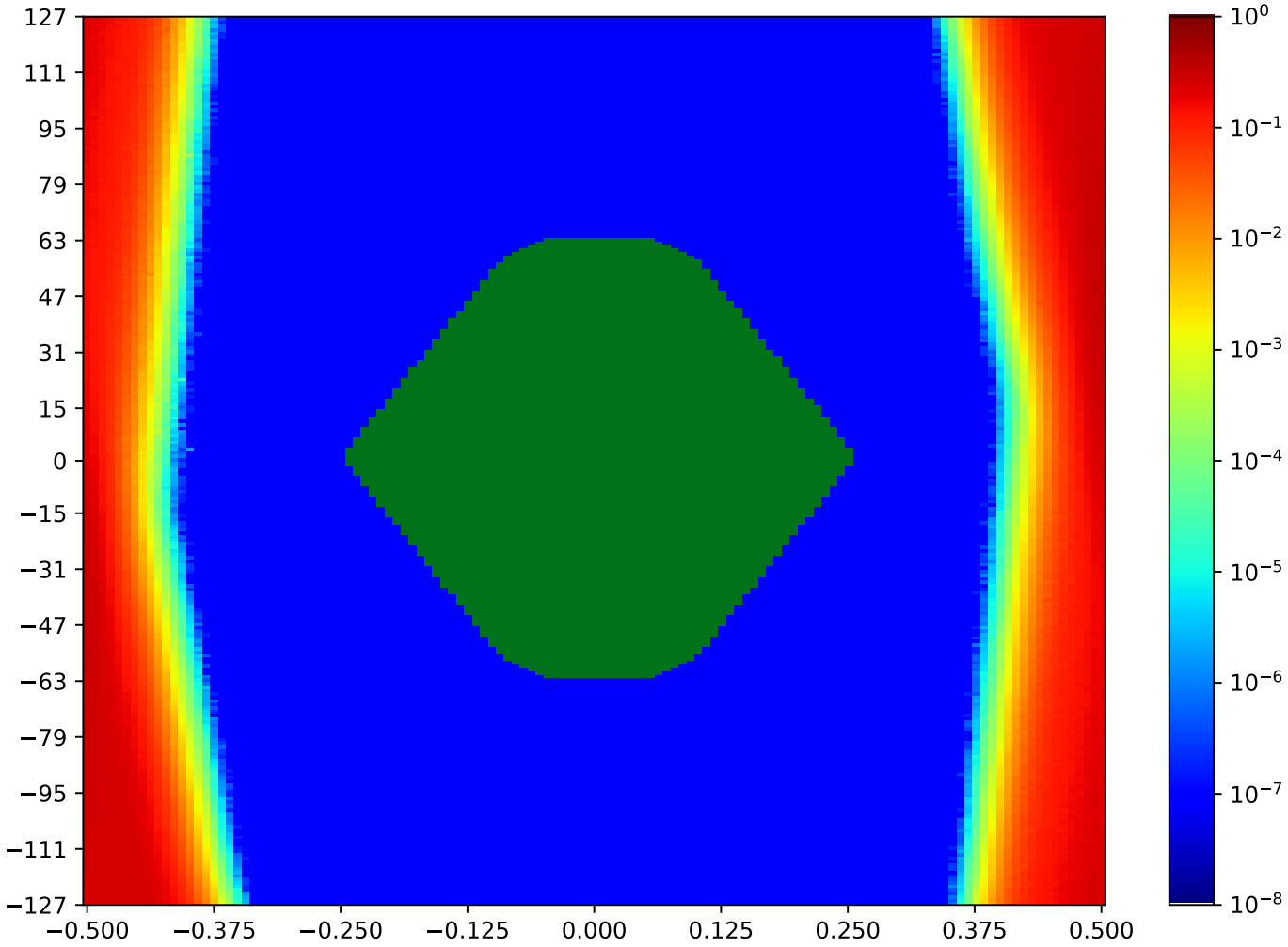


Figure 3.219: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.6 MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Table 3.203: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:19:27		2018-Sep-28 10:20:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24715	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

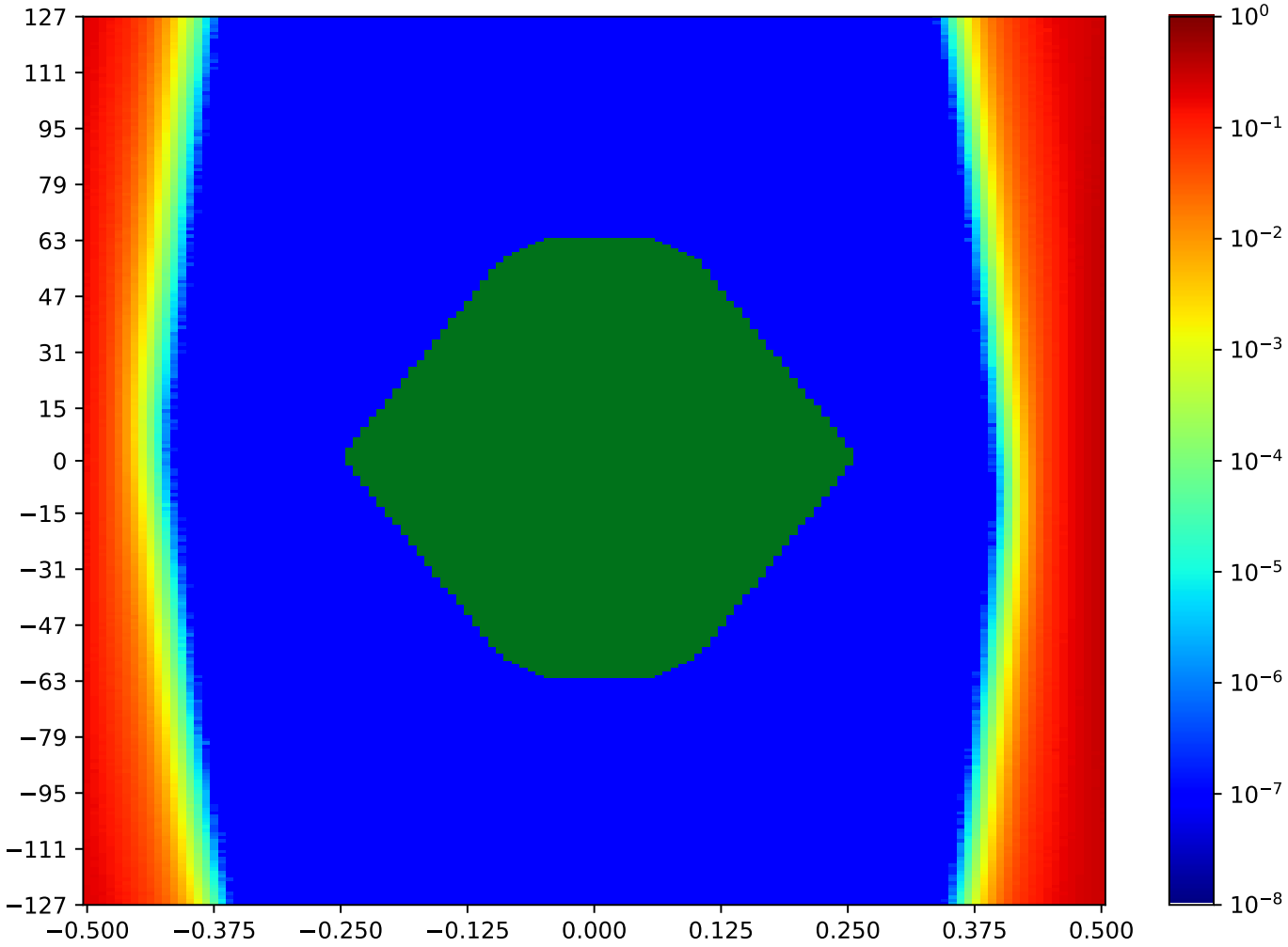


Figure 3.220: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.7 MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Table 3.204: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:33:17		2018-Sep-28 10:34:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24653	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

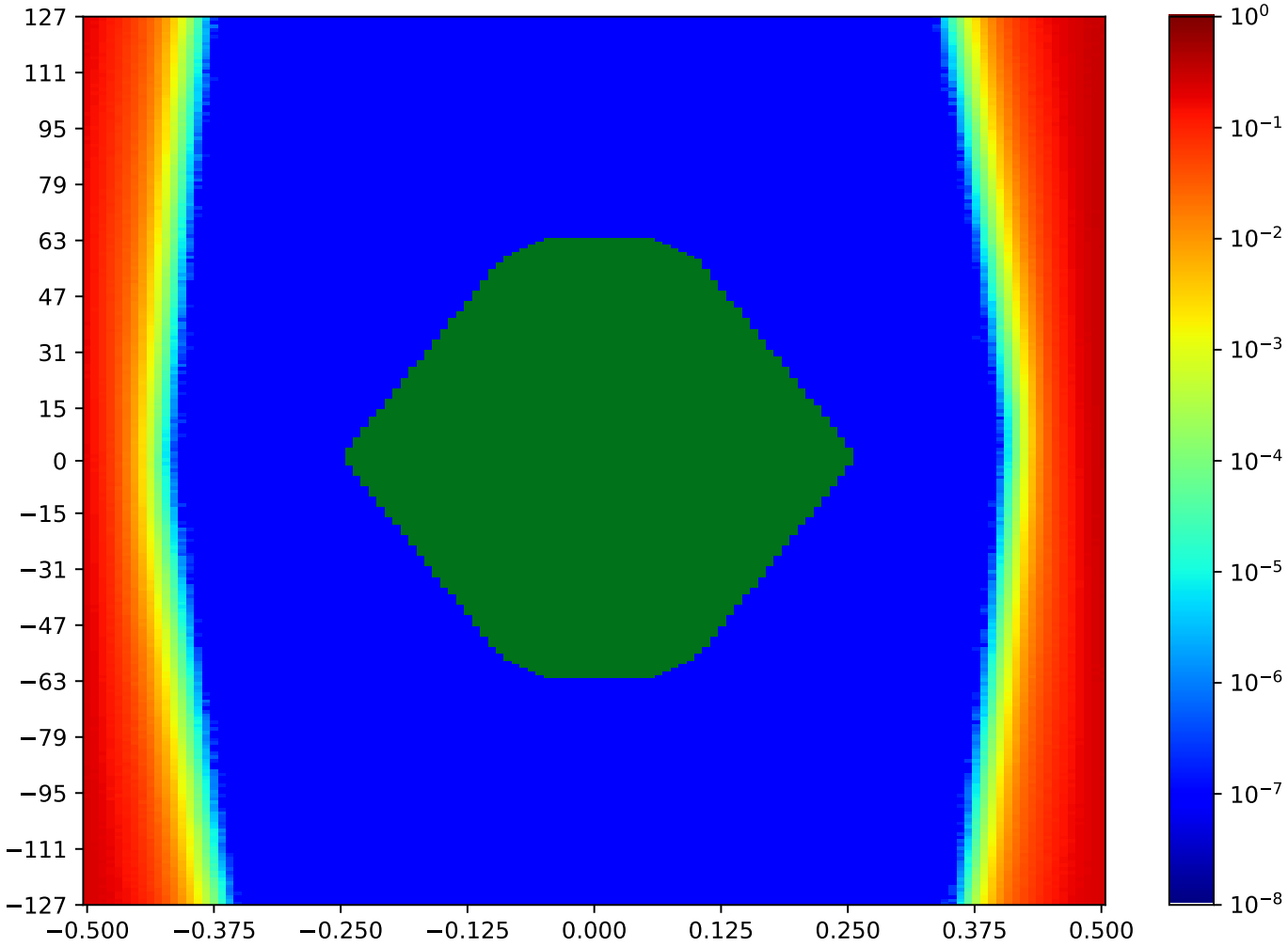


Figure 3.221: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.8 MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Table 3.205: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:21:58		2018-Sep-28 10:23:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24053	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

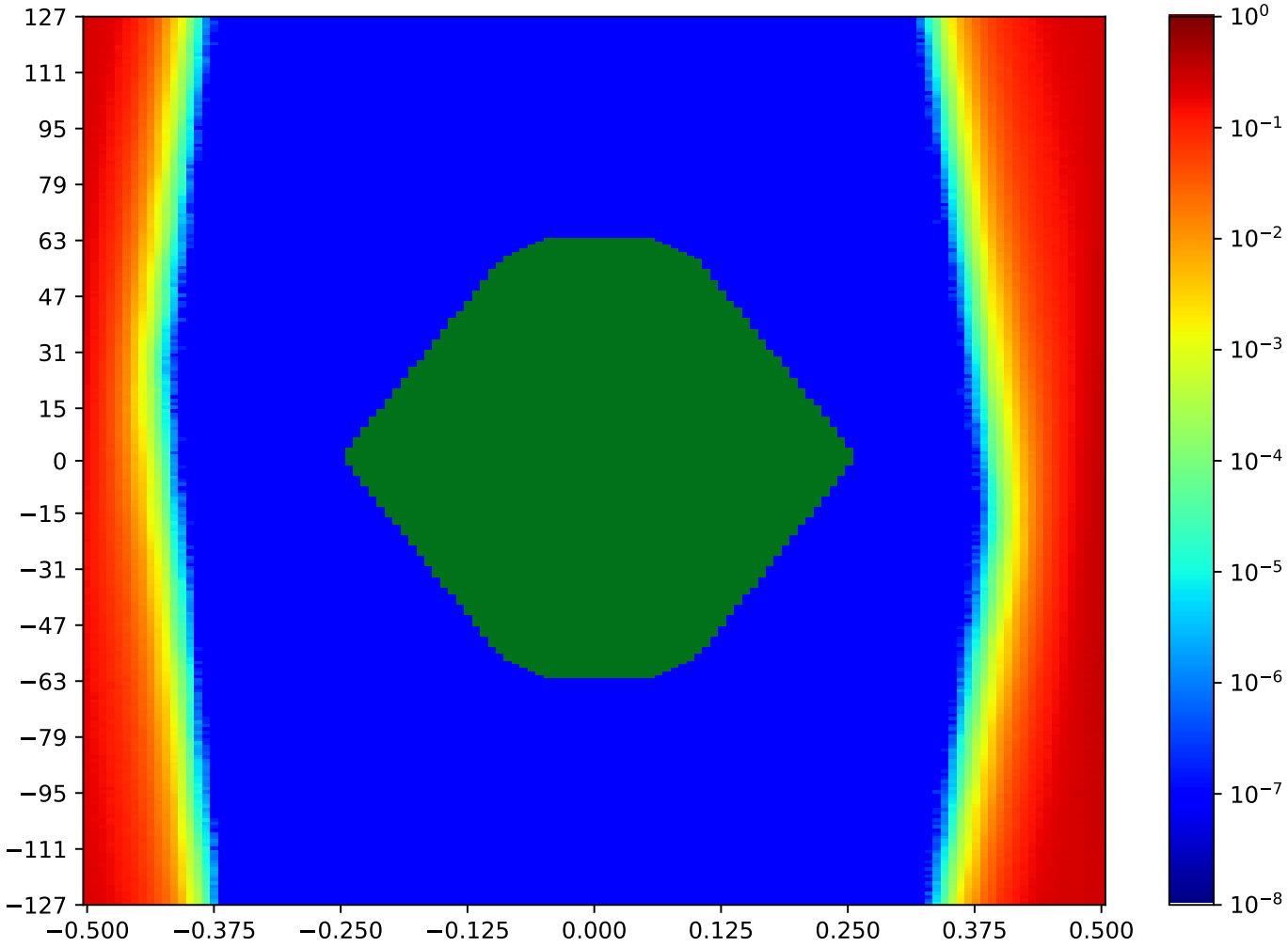


Figure 3.222: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.9 MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Table 3.206: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:32:01		2018-Sep-28 10:33:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25012	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

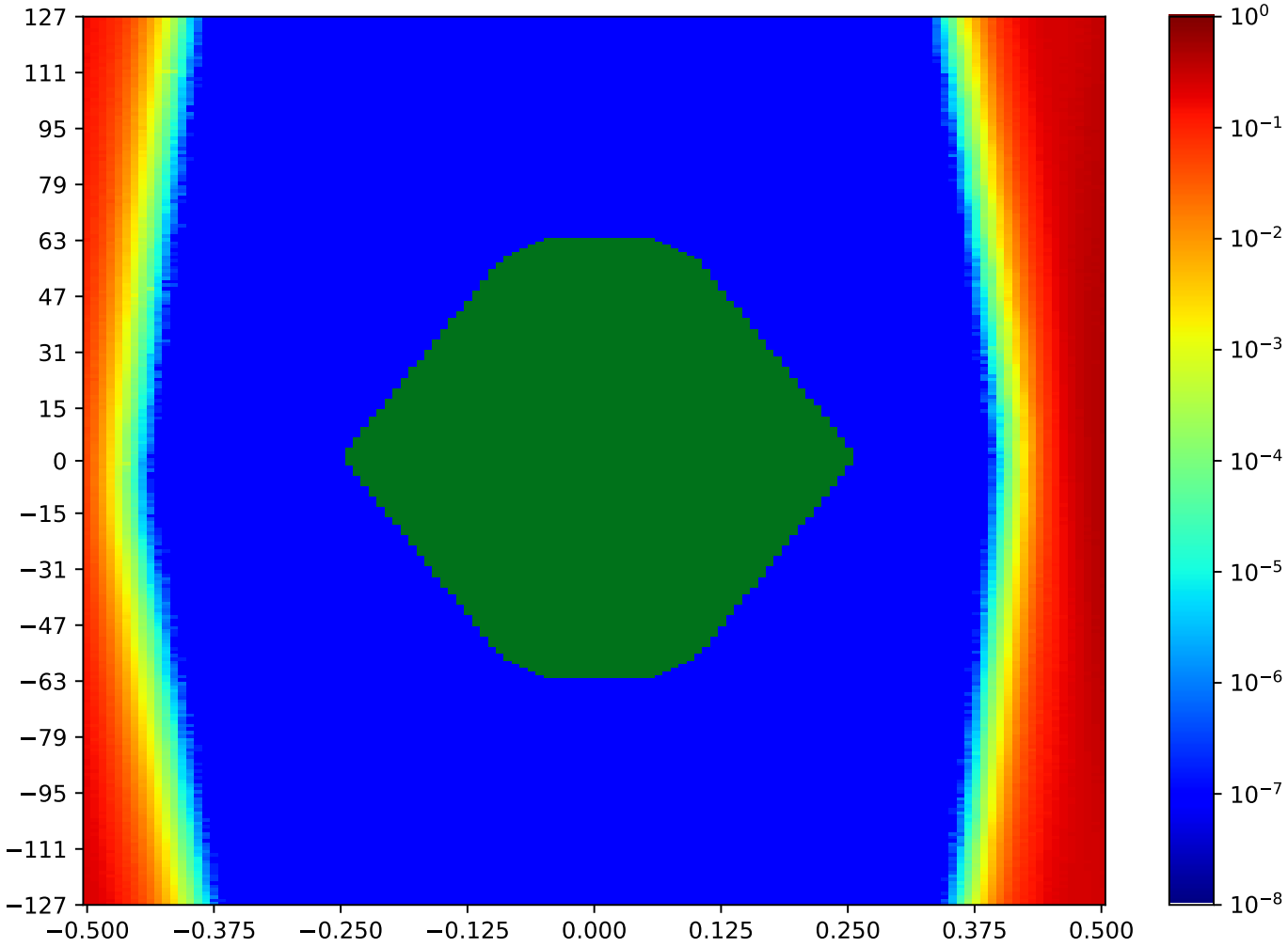


Figure 3.223: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.10 MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Table 3.207: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:24:29		2018-Sep-28 10:25:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24458	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

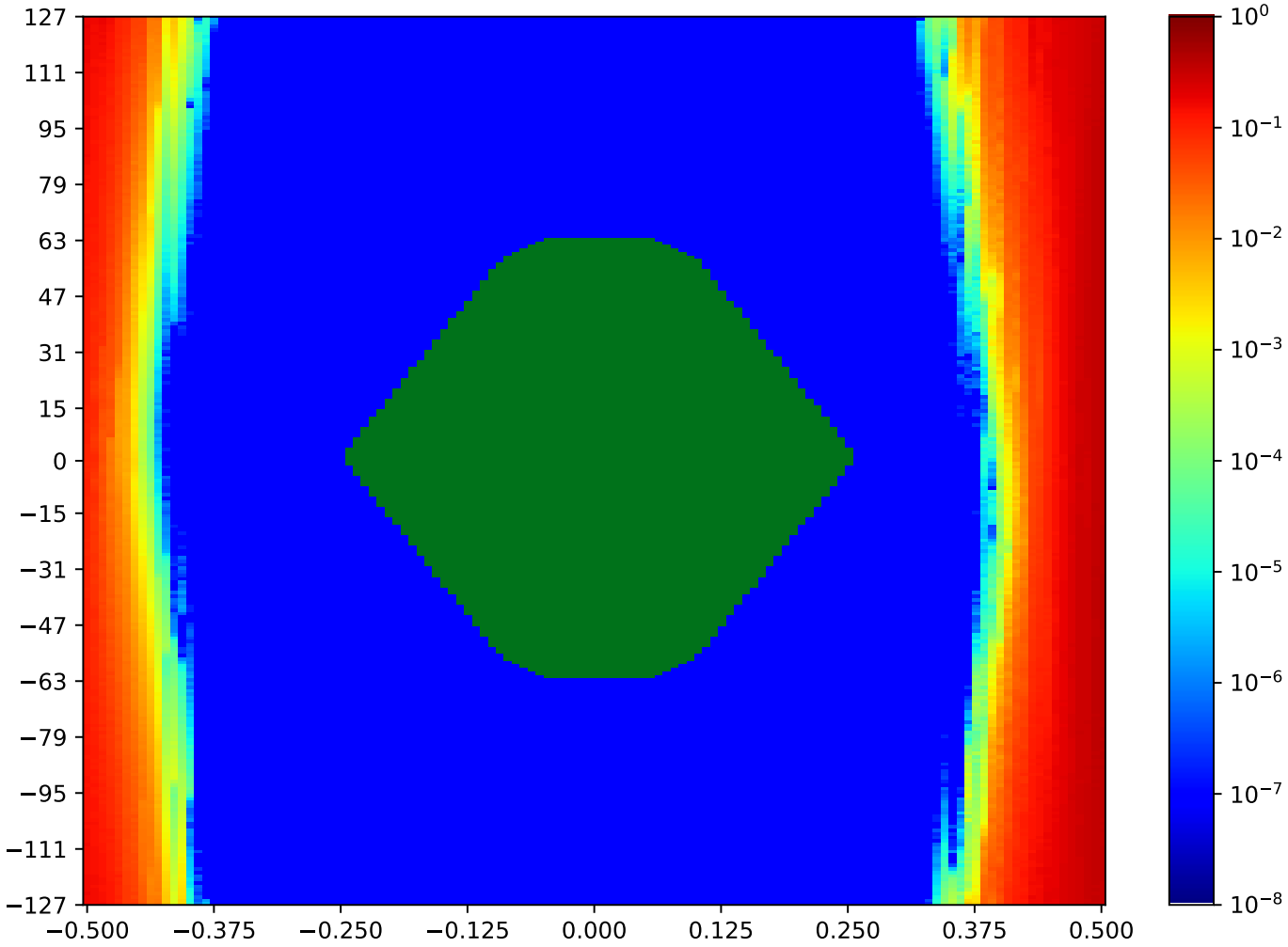


Figure 3.224: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.11 MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Table 3.208: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:29:31		2018-Sep-28 10:30:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24199	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

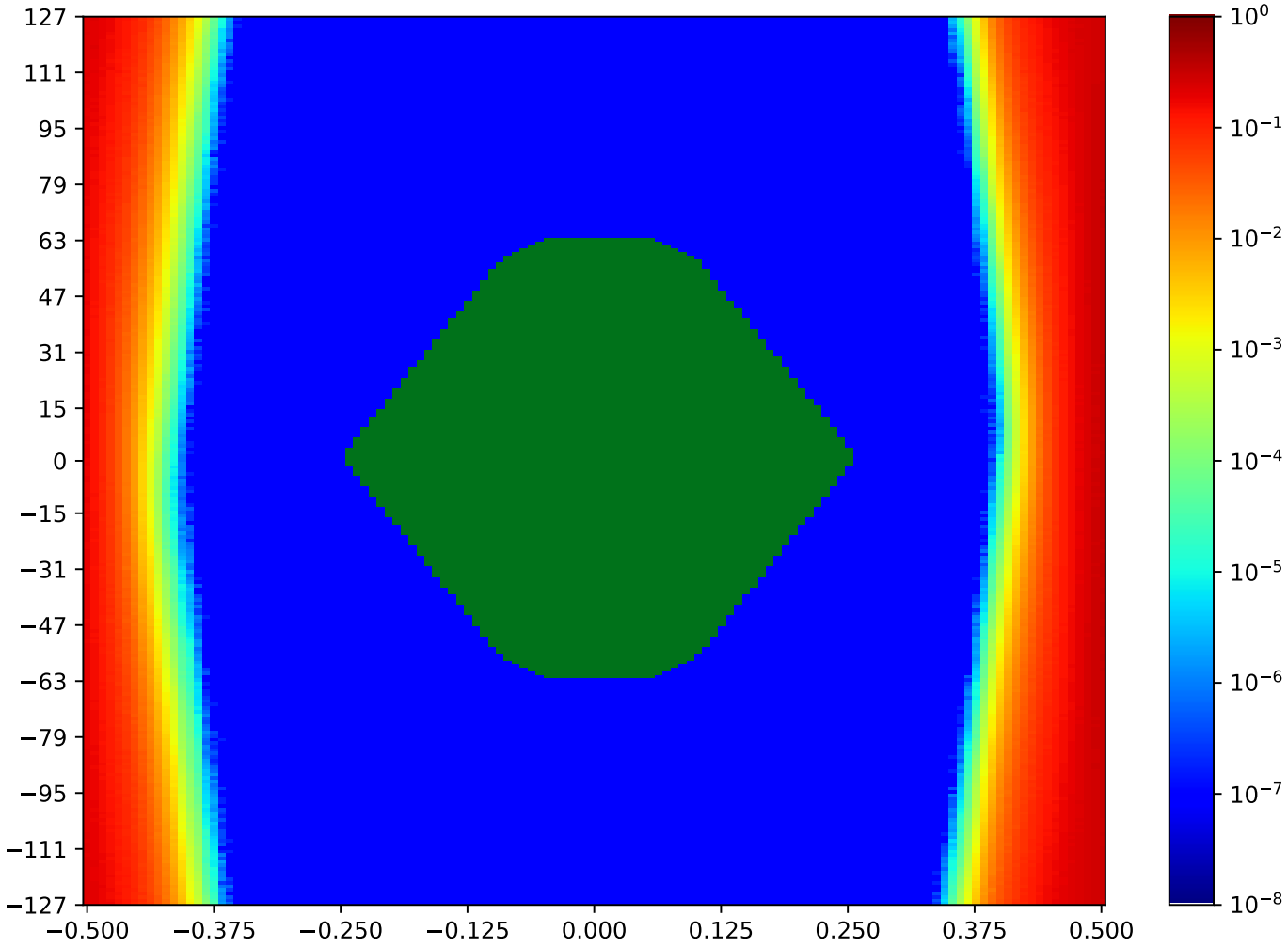


Figure 3.225: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.17.12 MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Table 3.209: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:28:15		2018-Sep-28 10:29:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24805	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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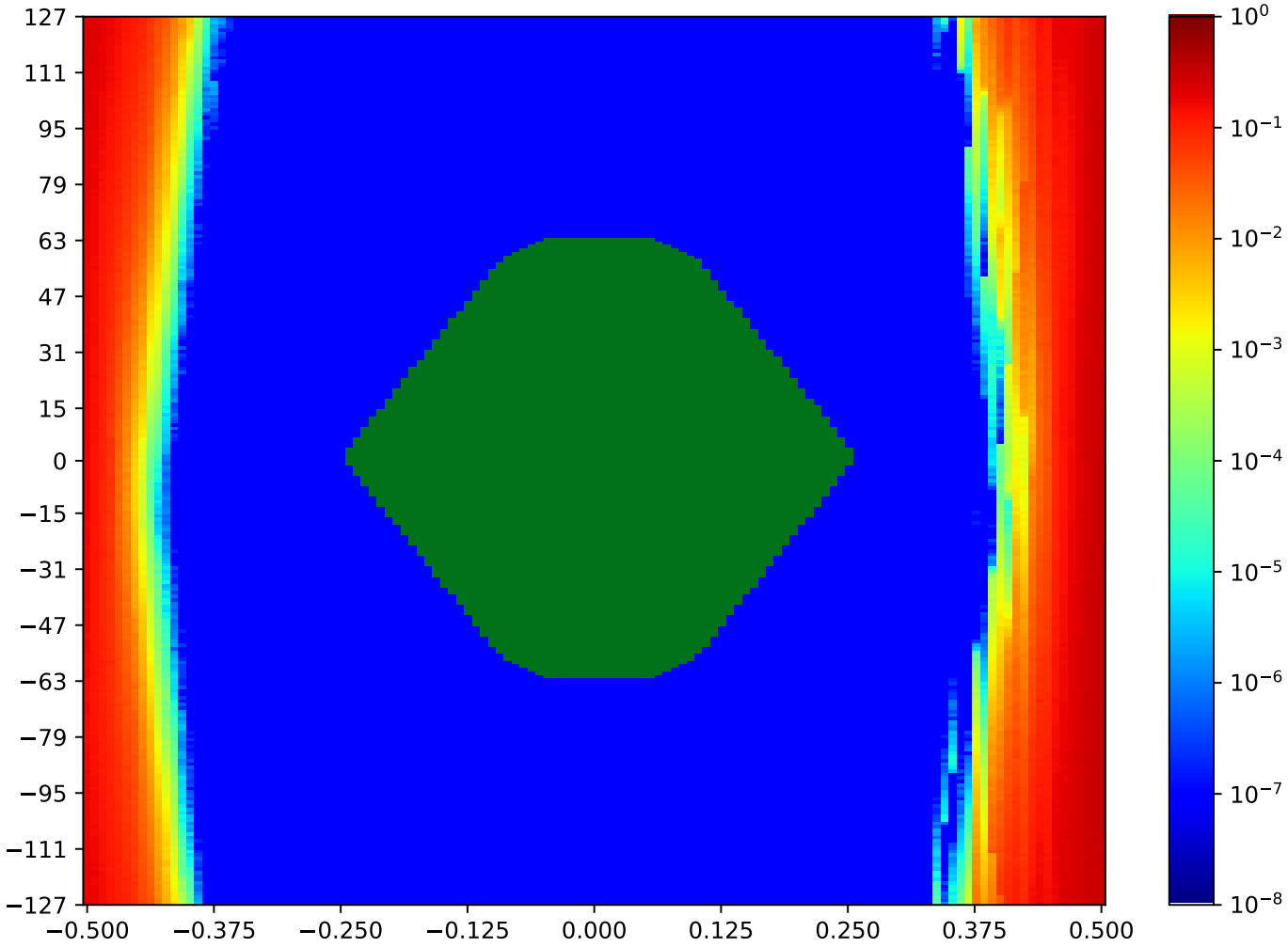


Figure 3.226: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18 MSP_C TX4 MSP_A RX2 Minipod Loopback

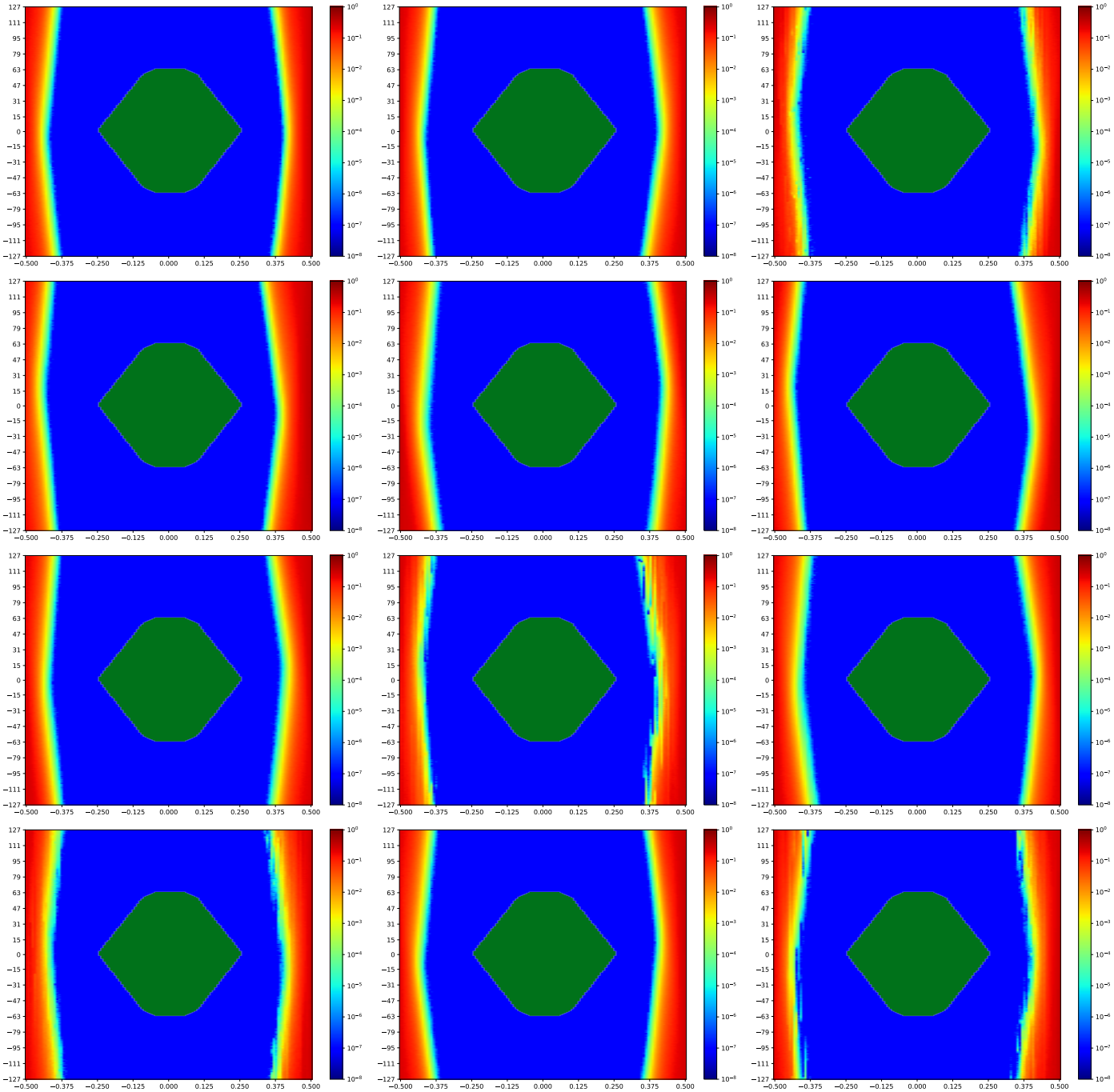


Figure 3.227: MSP_C TX4 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.240.

3.18.1 MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Table 3.210: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:38:19		2018-Sep-28 10:39:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24909	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

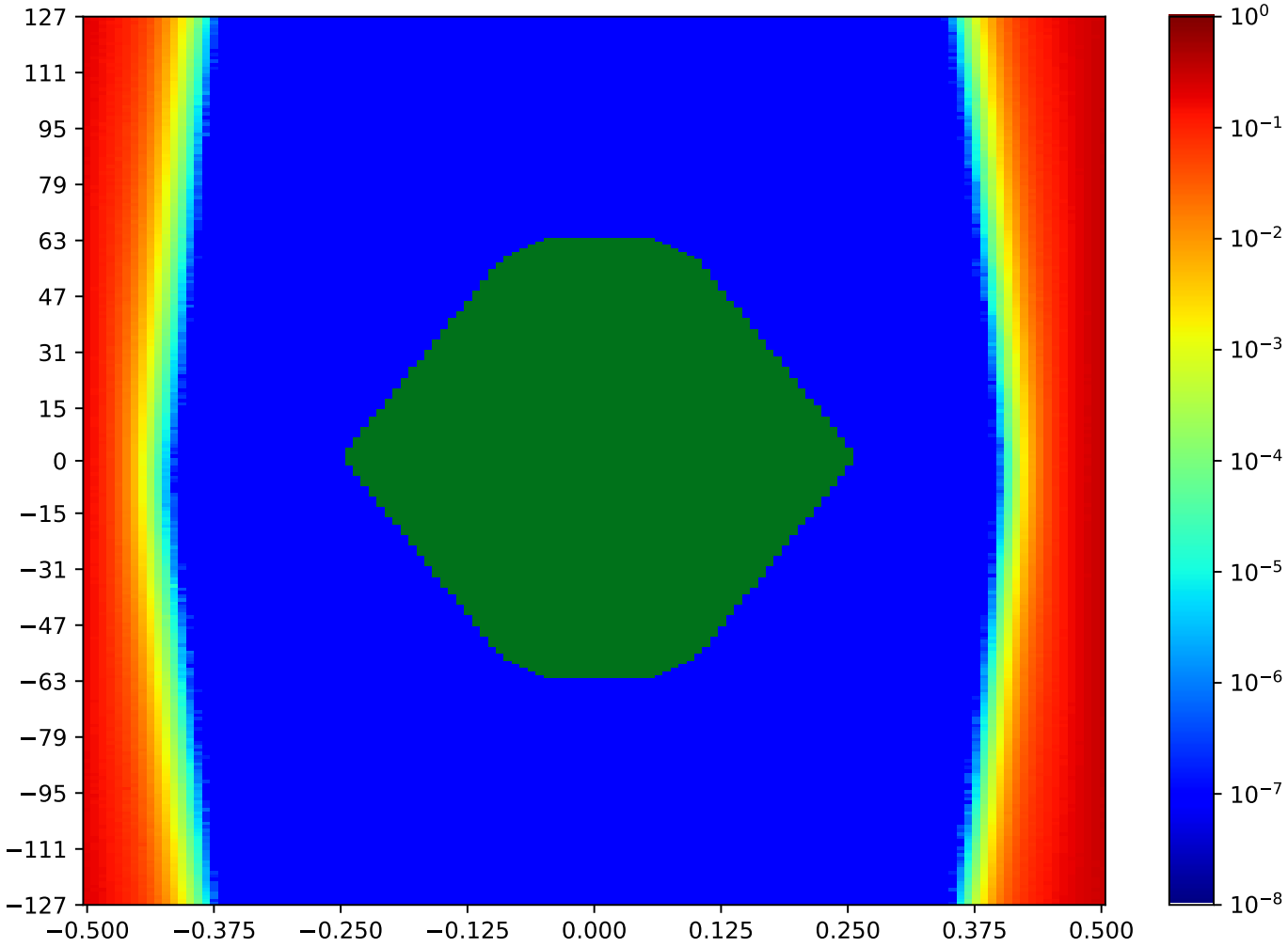


Figure 3.228: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.2 MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Table 3.211: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:35:48		2018-Sep-28 10:37:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24556	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

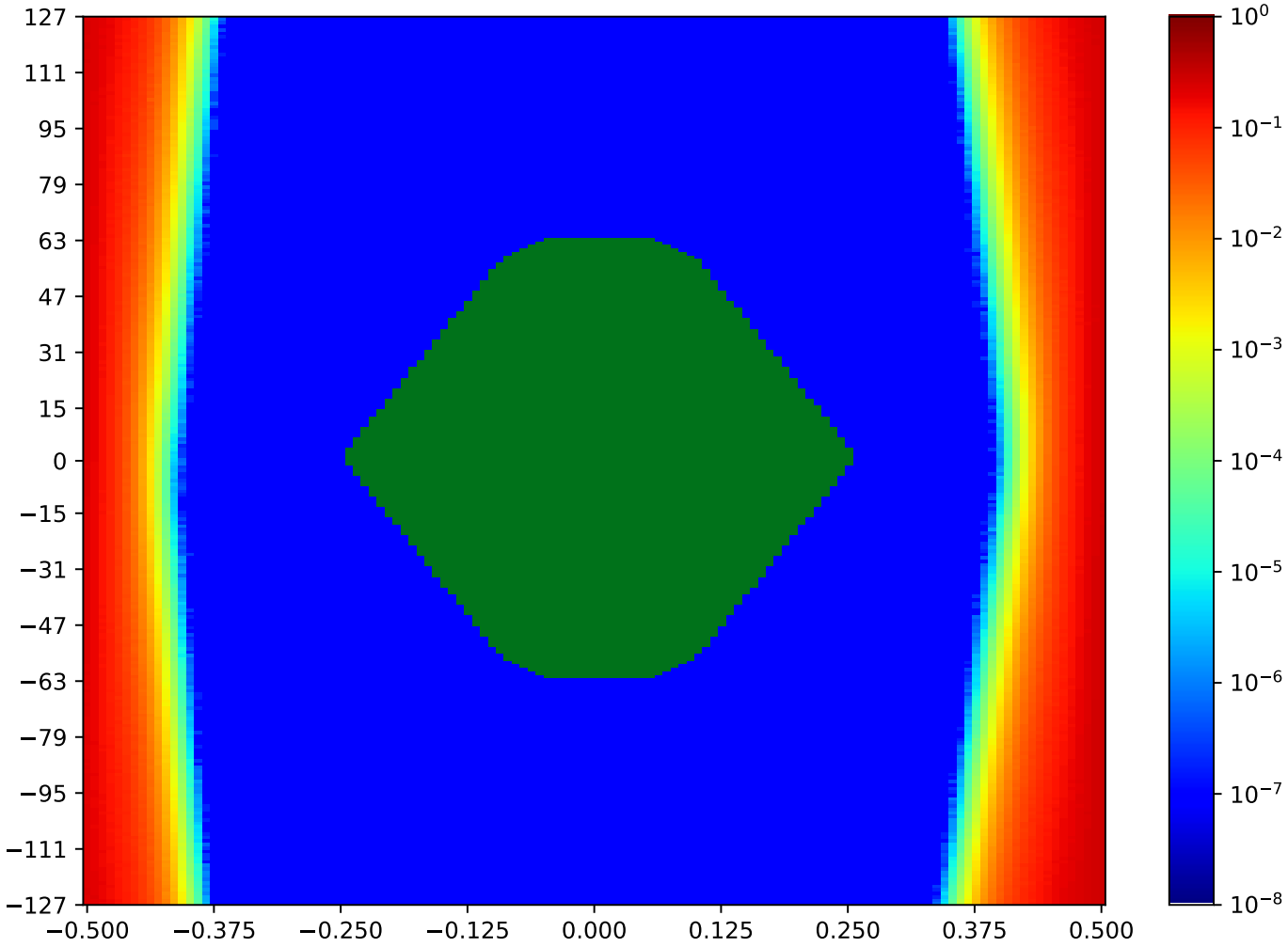


Figure 3.229: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.3 MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Table 3.212: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:42:06		2018-Sep-28 10:43:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24823	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

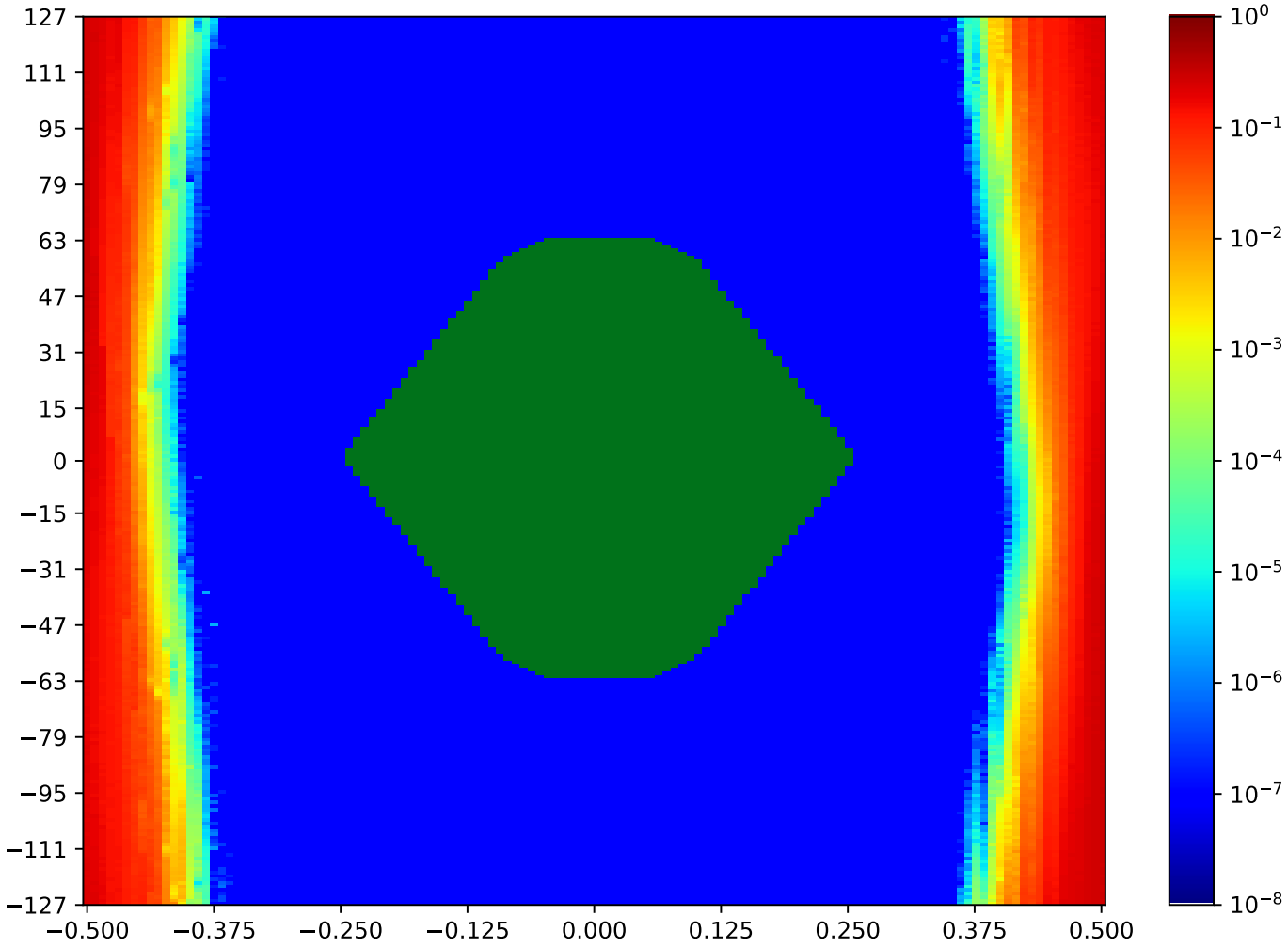


Figure 3.230: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.4 MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Table 3.213: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:34:33		2018-Sep-28 10:35:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24318	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

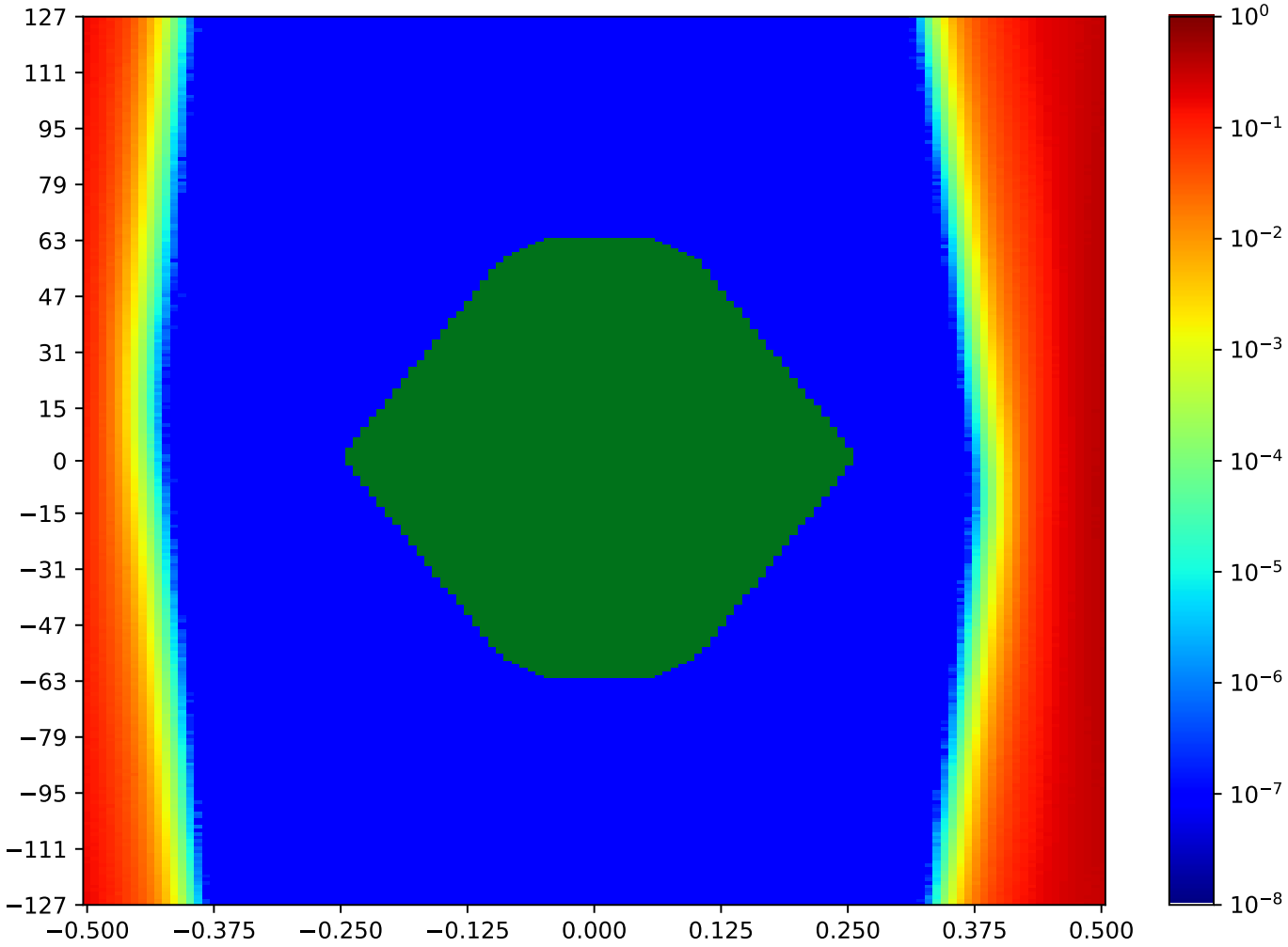


Figure 3.231: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.5 MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Table 3.214: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:45:52		2018-Sep-28 10:47:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24440	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

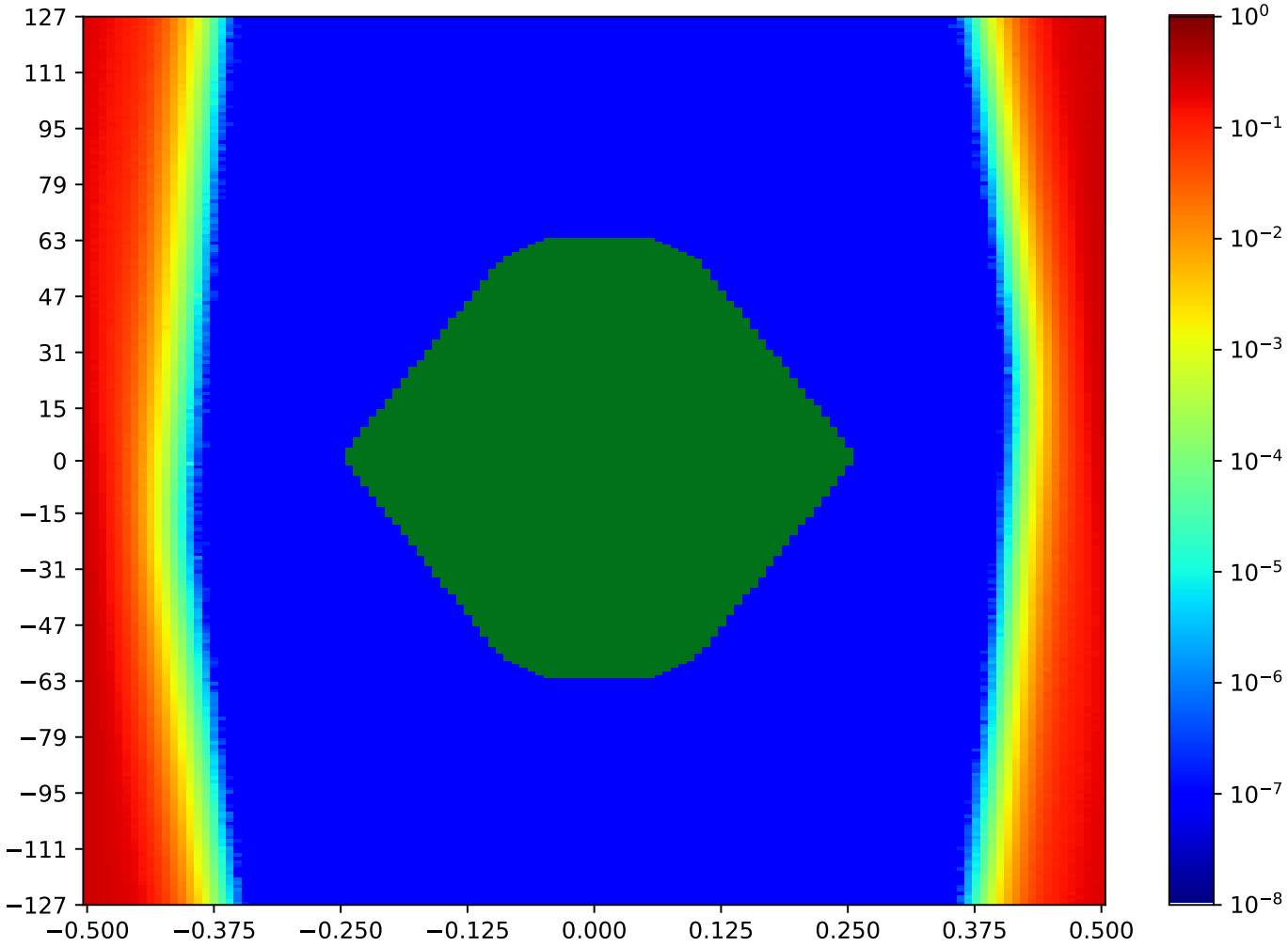


Figure 3.232: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.6 MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Table 3.215: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:37:03		2018-Sep-28 10:38:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24614	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

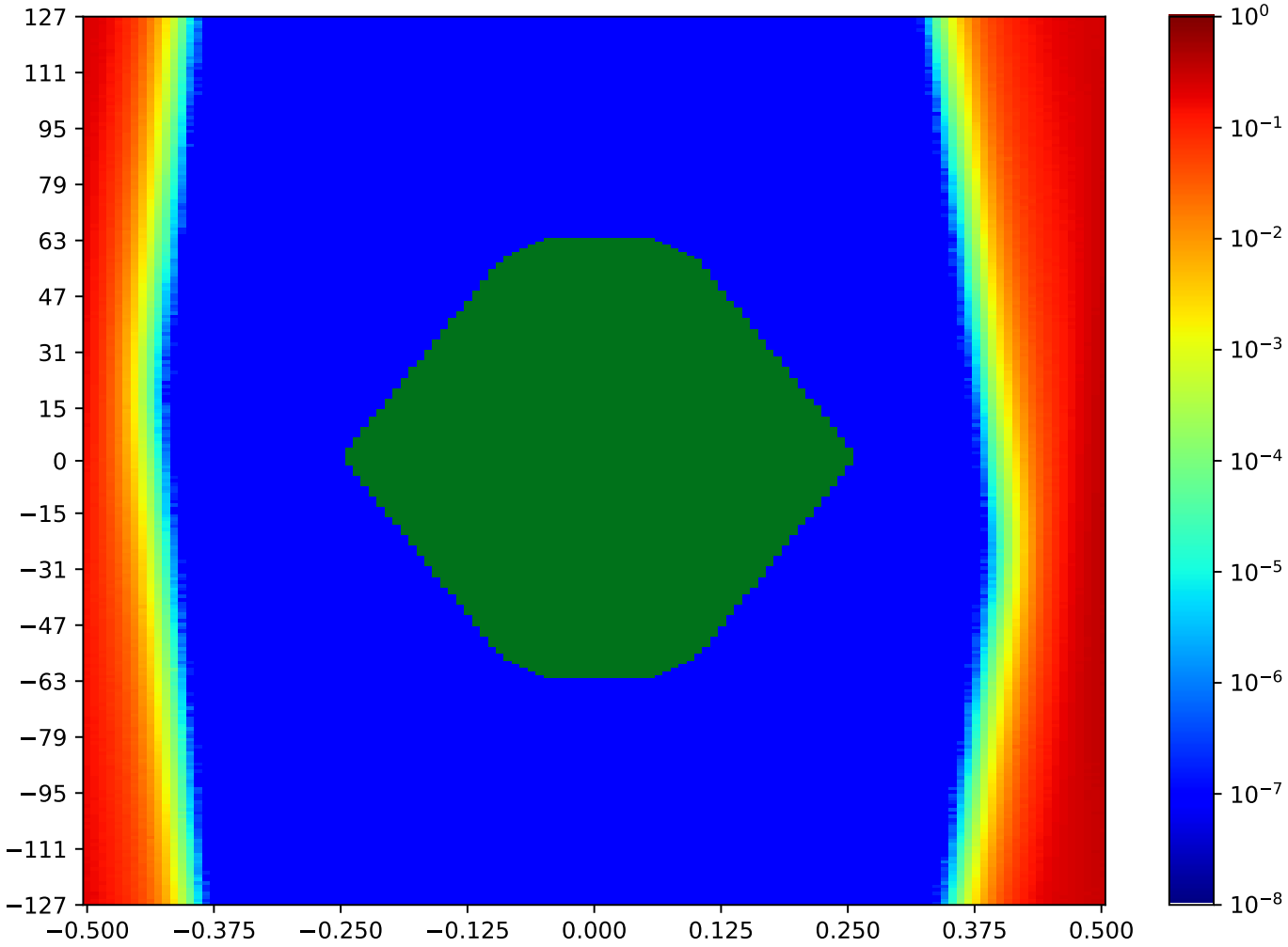


Figure 3.233: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.7 MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Table 3.216: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:48:23		2018-Sep-28 10:49:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24329	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

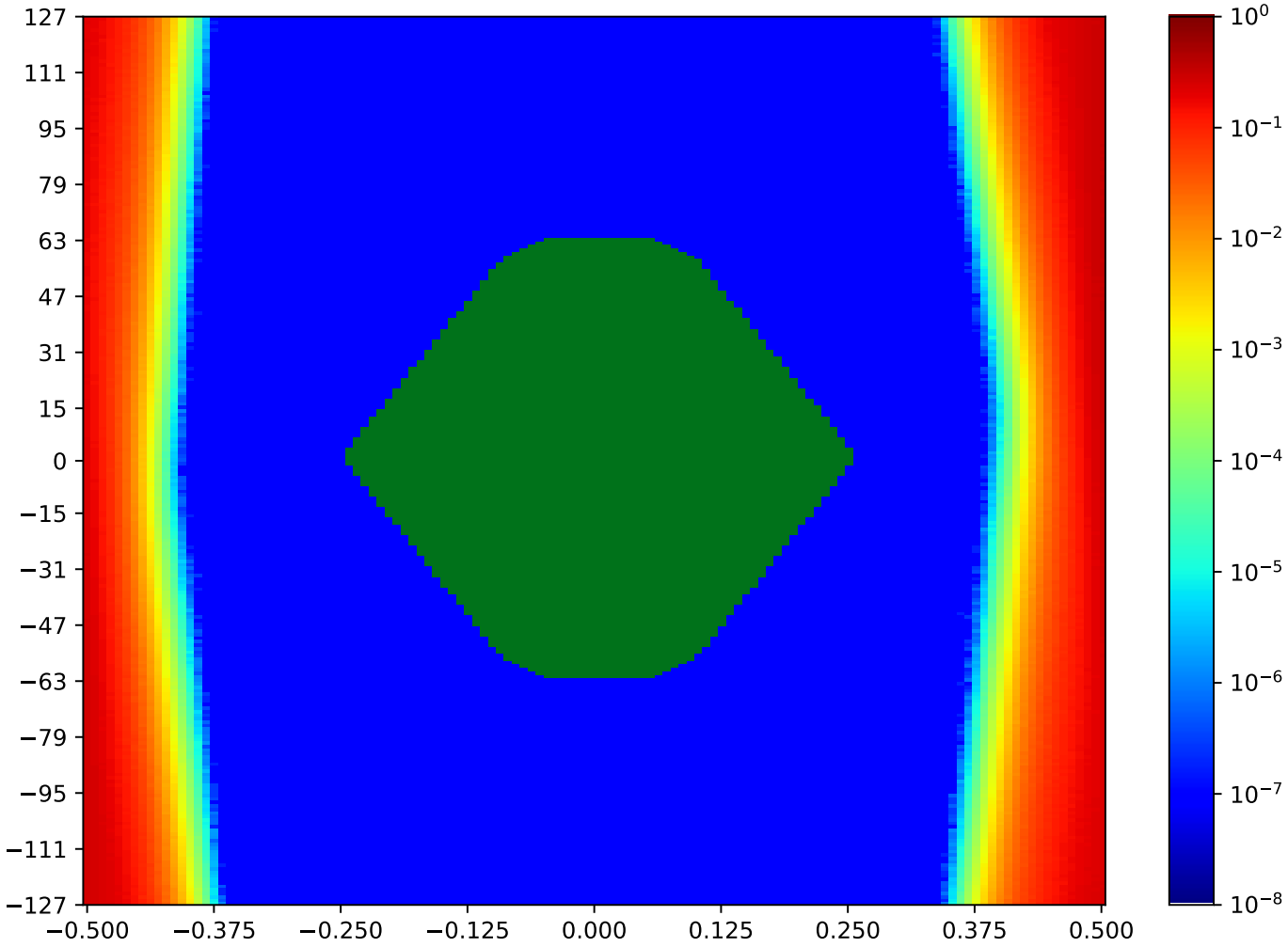


Figure 3.234: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.8 MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Table 3.217: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:39:35		2018-Sep-28 10:40:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24464	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

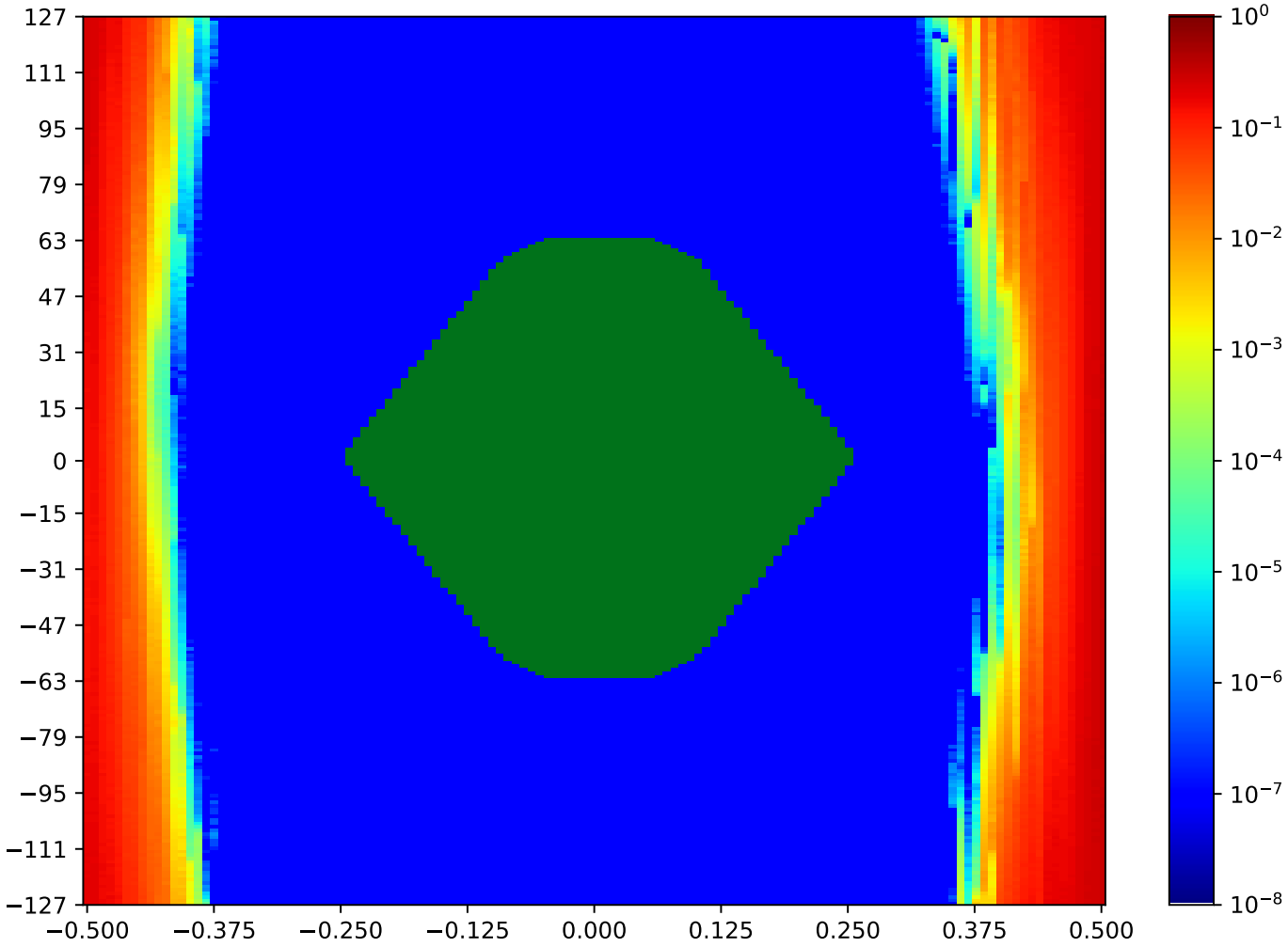


Figure 3.235: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.9 MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Table 3.218: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:47:07		2018-Sep-28 10:48:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23939	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

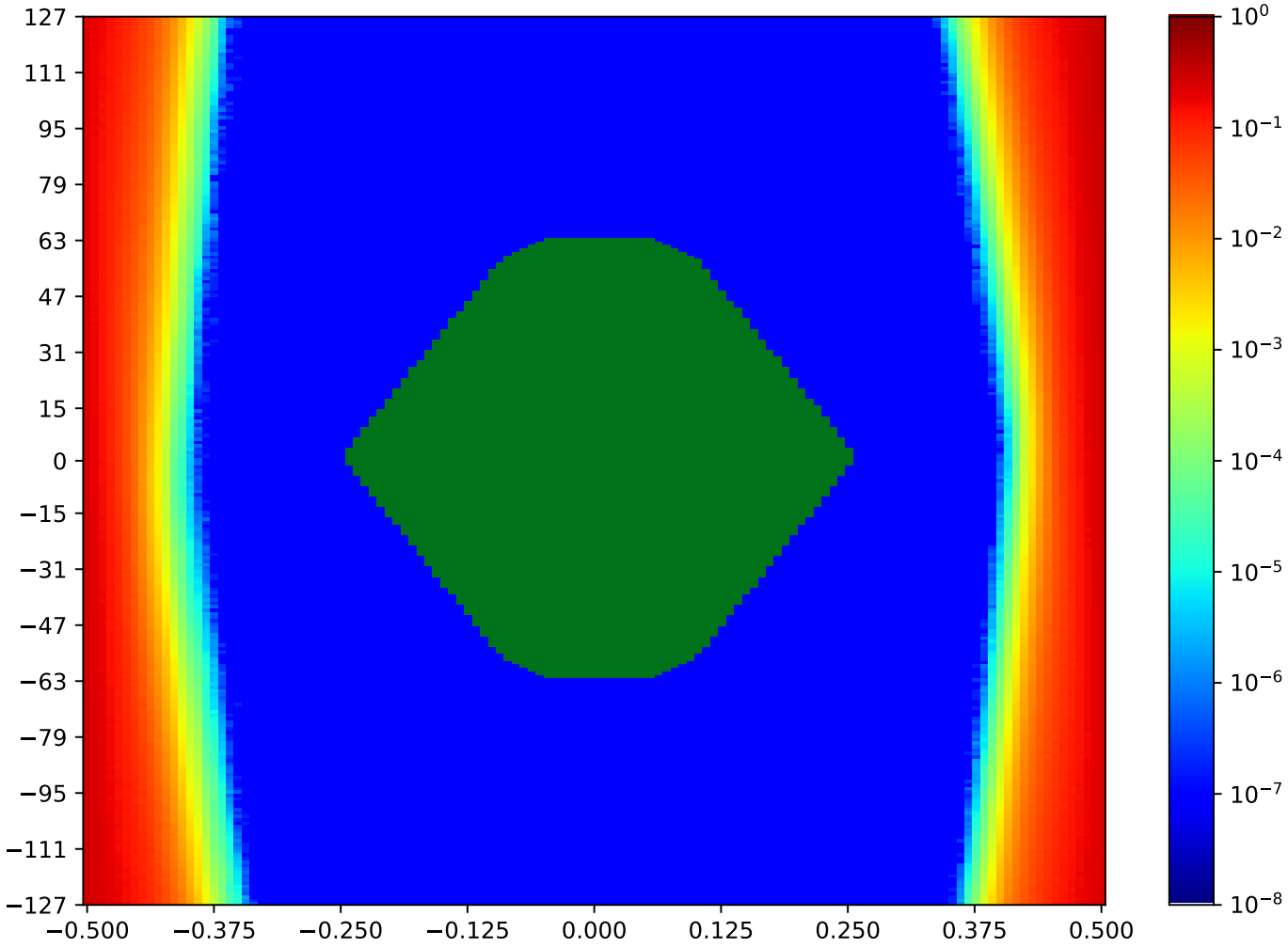


Figure 3.236: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.10 MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Table 3.219: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:40:50		2018-Sep-28 10:42:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24250	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

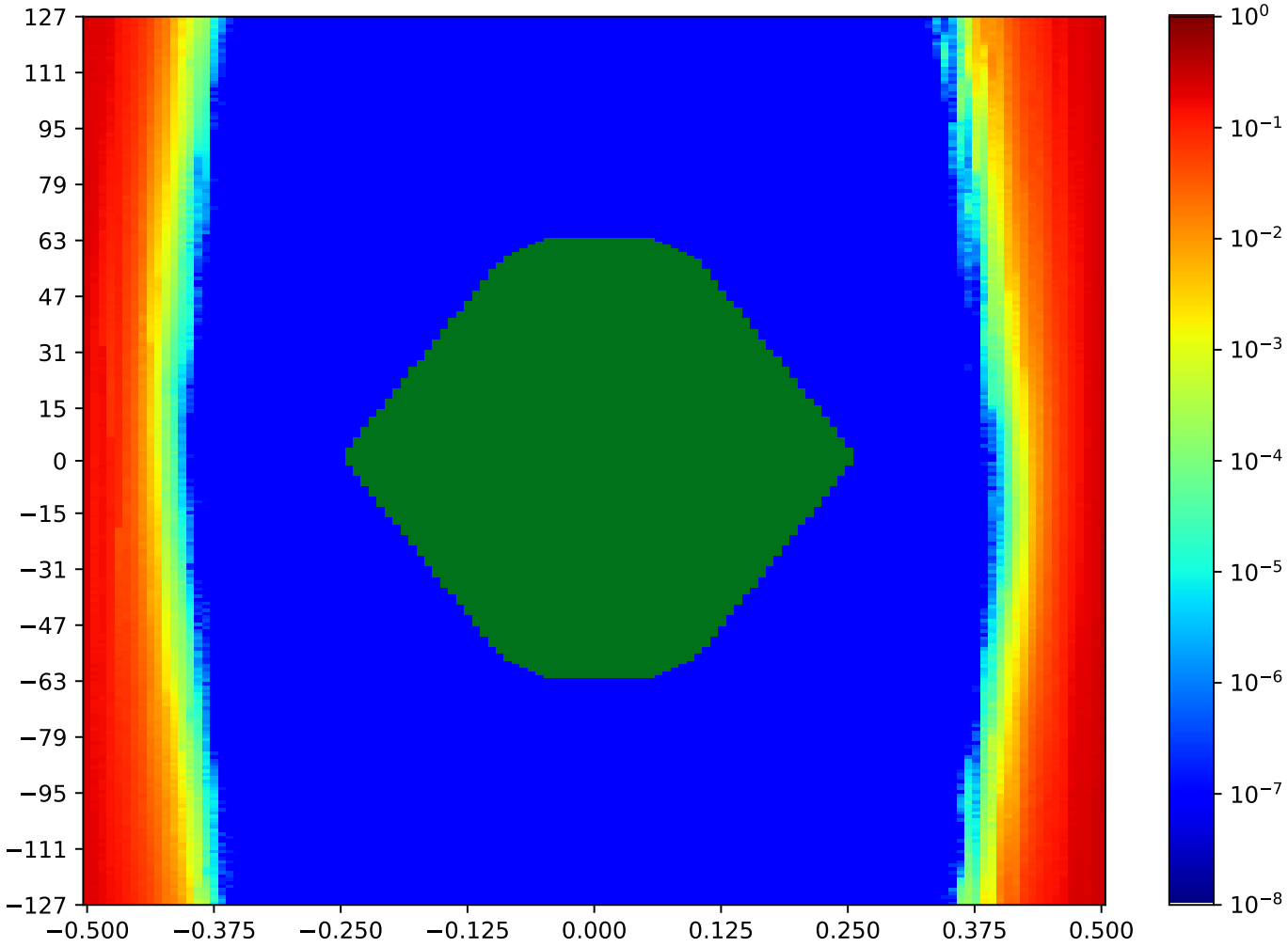


Figure 3.237: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.11 MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Table 3.220: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:44:37		2018-Sep-28 10:45:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24455	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

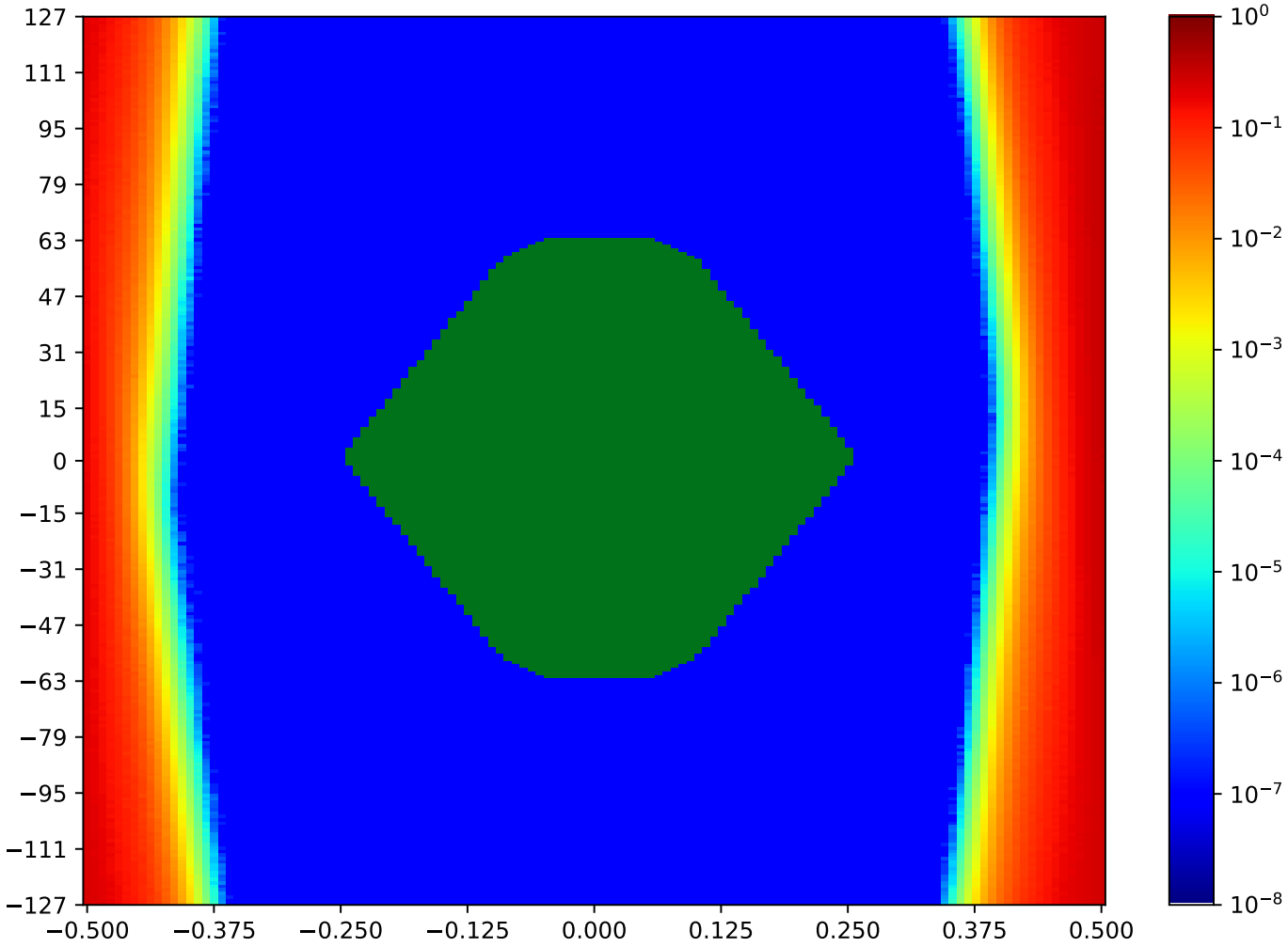


Figure 3.238: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.18.12 MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Table 3.221: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:43:22		2018-Sep-28 10:44:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24499	102	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

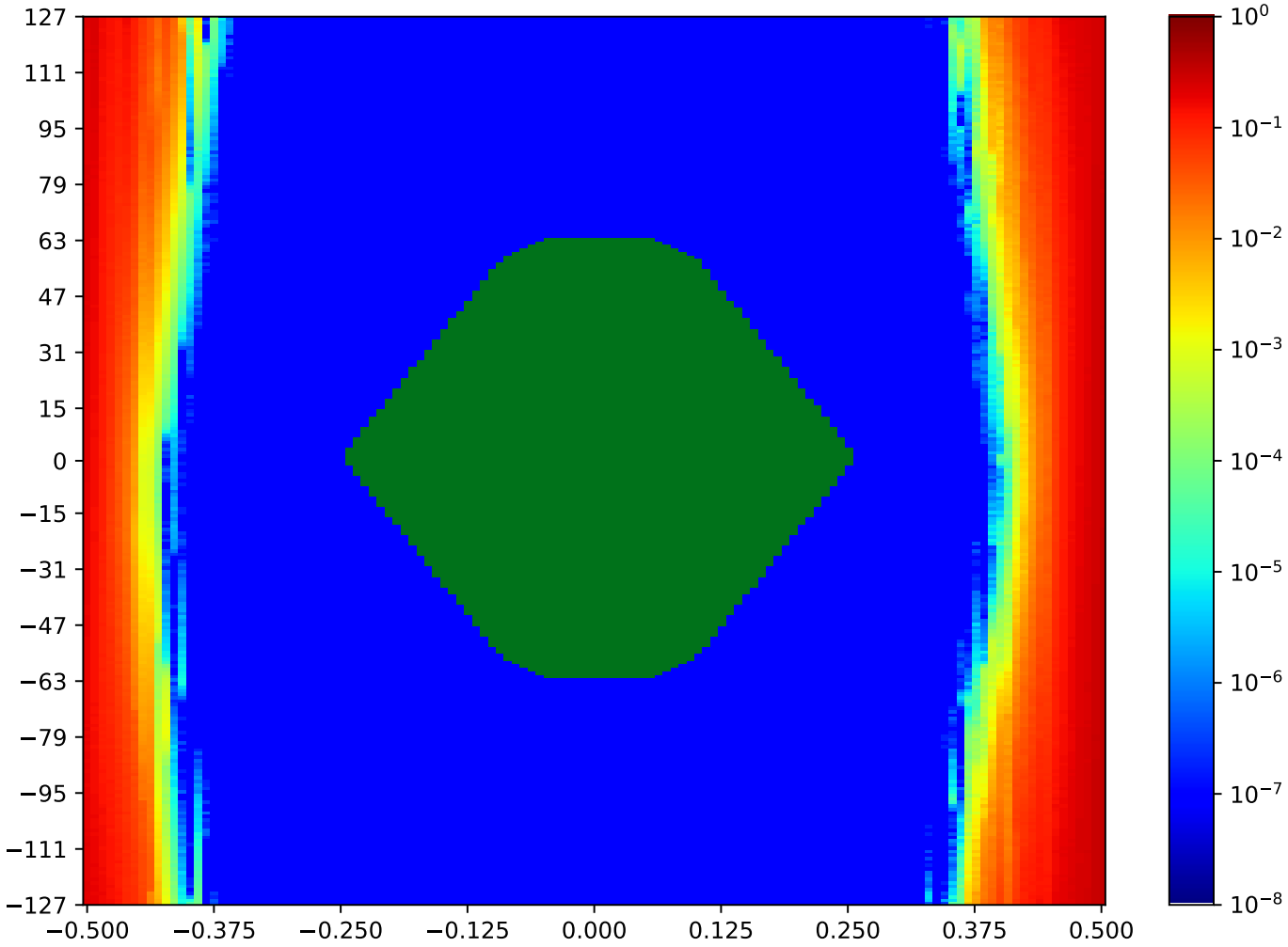


Figure 3.239: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19 MSP_A TX1 MSP_C RX12 Minipod Loopback

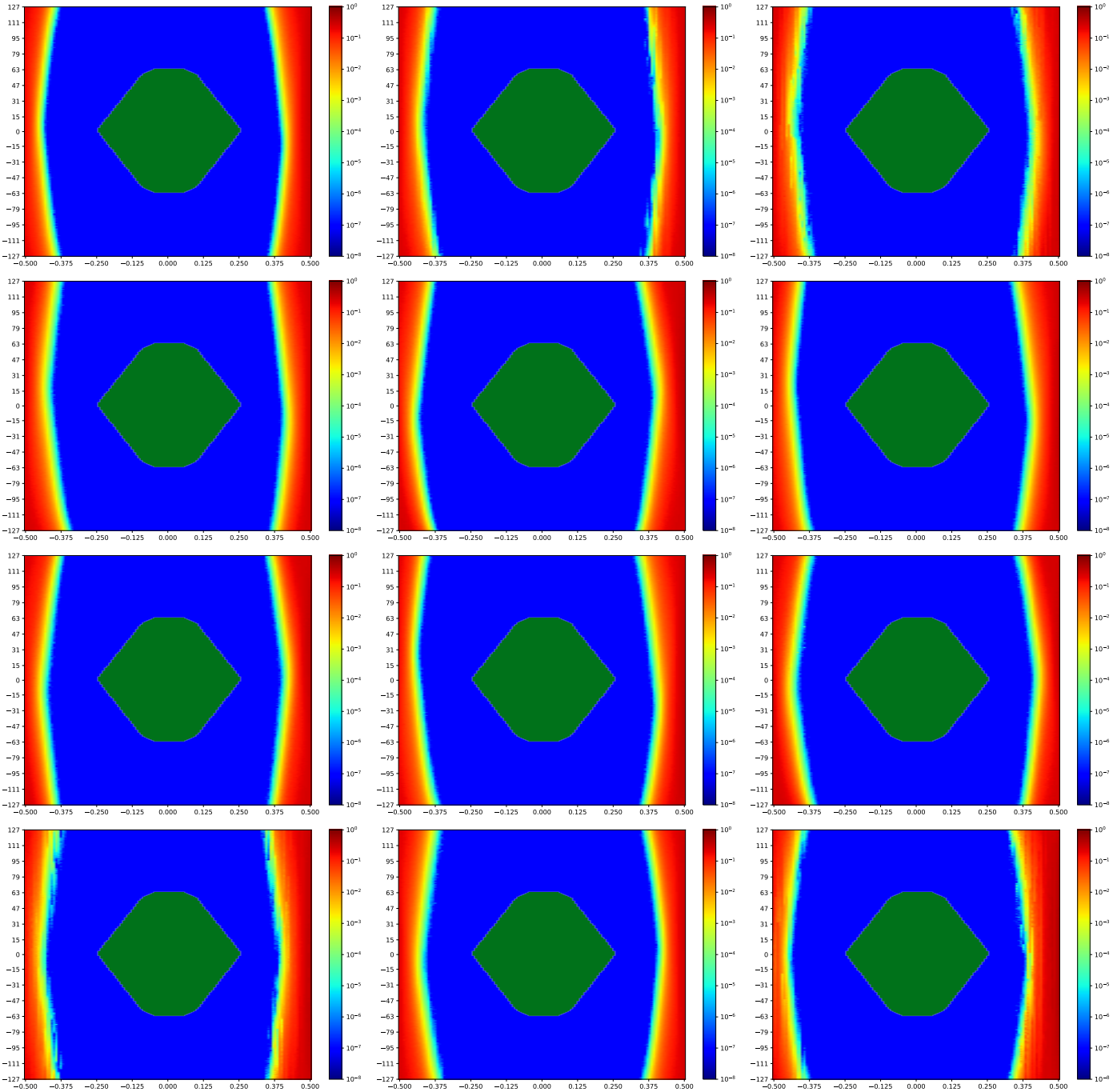


Figure 3.240: MSP_A TX1 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.253.

3.19.1 MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Table 3.222: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:13:00		2018-Sep-27 18:14:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25145	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

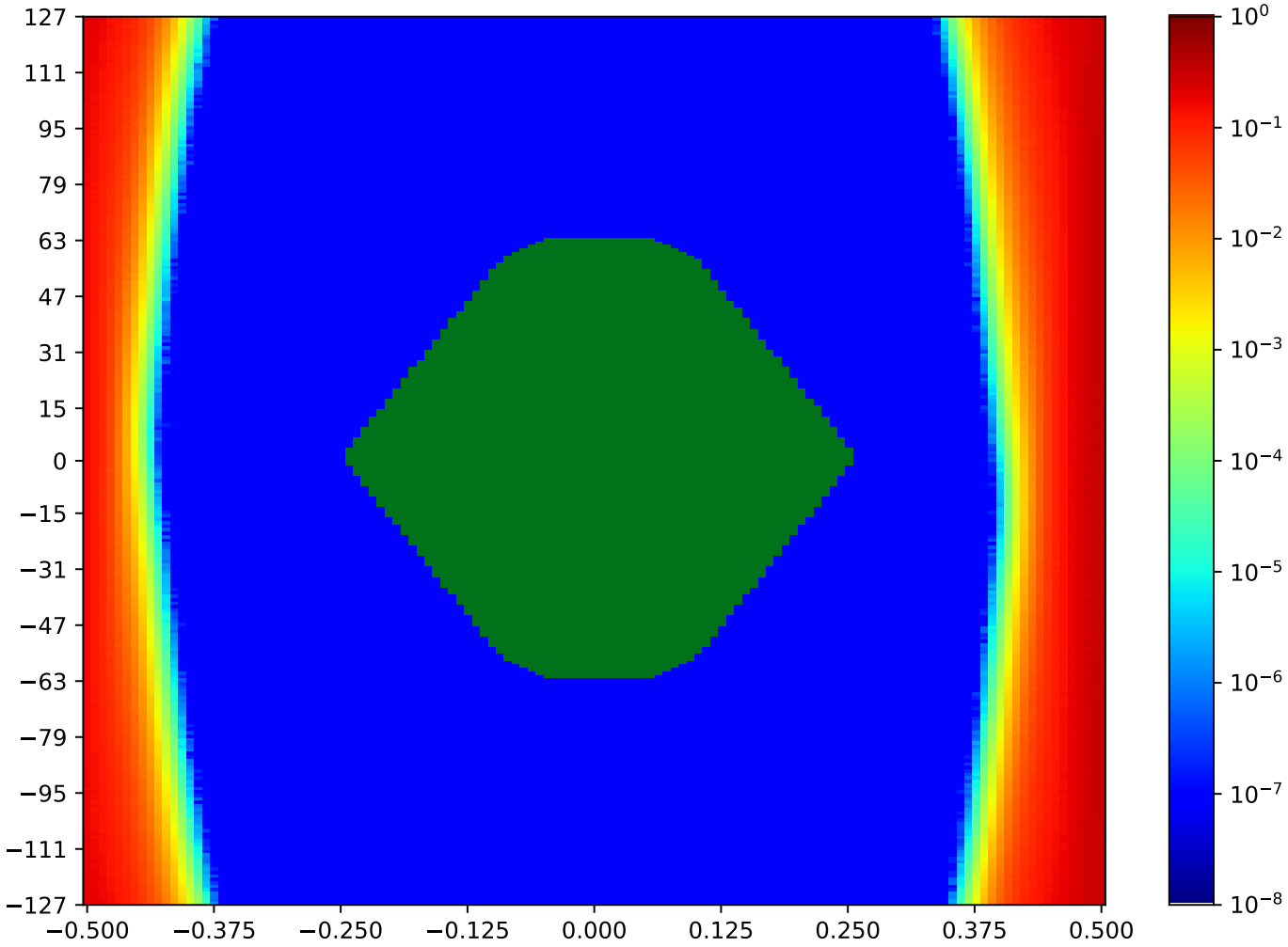


Figure 3.241: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.2 MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Table 3.223: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:15:28		2018-Sep-27 18:16:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24604	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

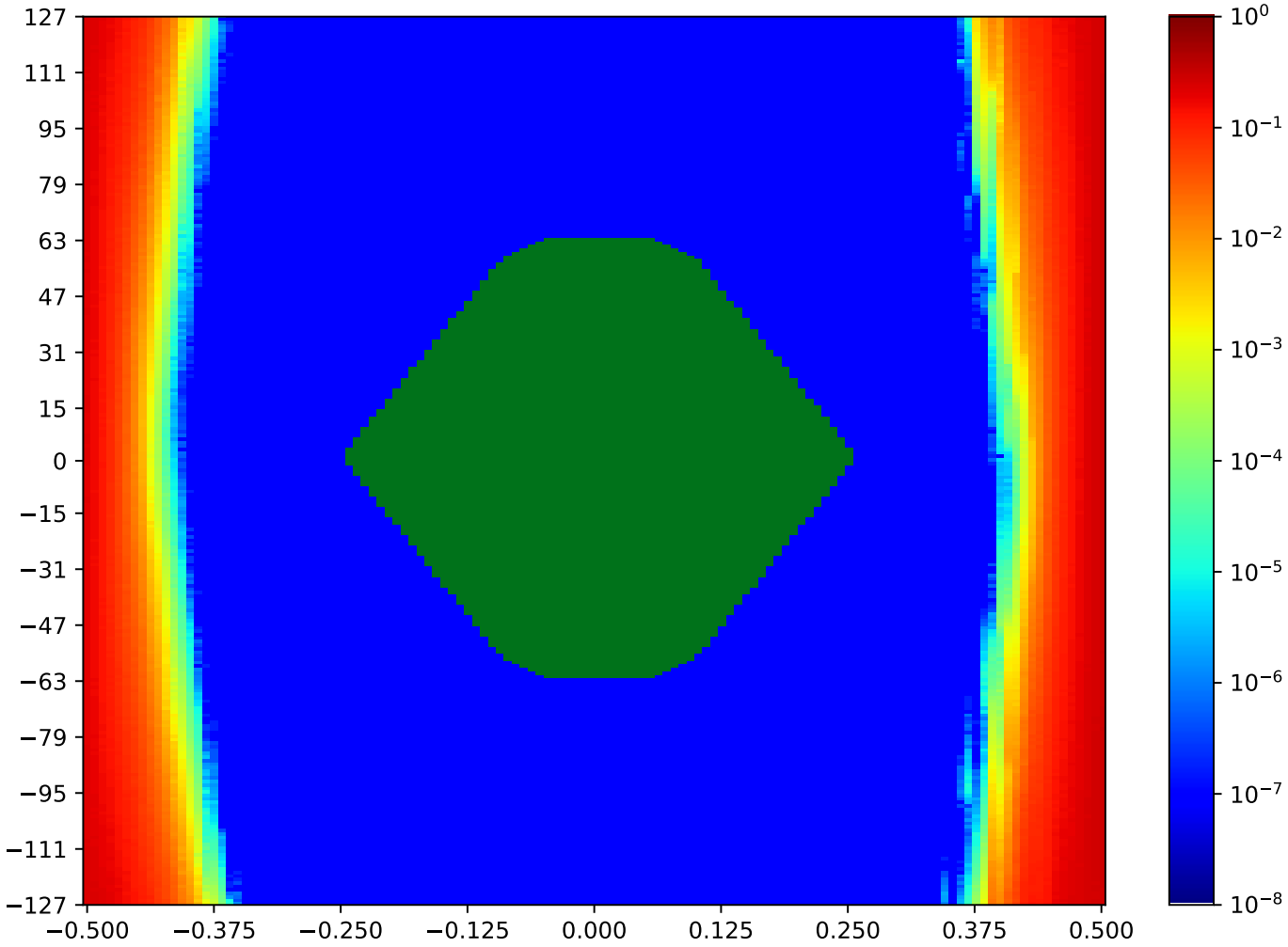


Figure 3.242: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.3 MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Table 3.224: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:16:42		2018-Sep-27 18:17:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24237	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

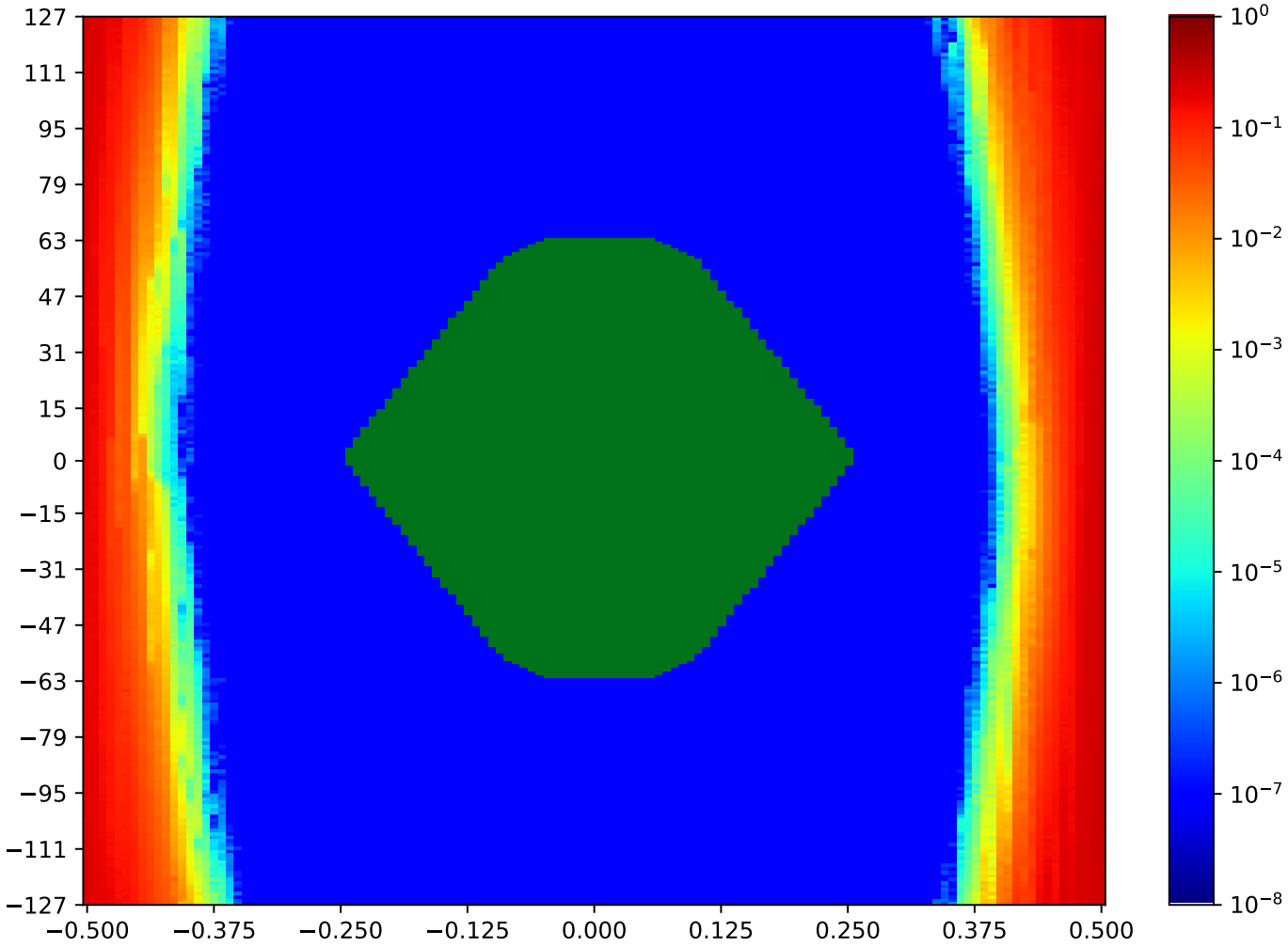


Figure 3.243: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.4 MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Table 3.225: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:10:30		2018-Sep-27 18:11:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24299	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

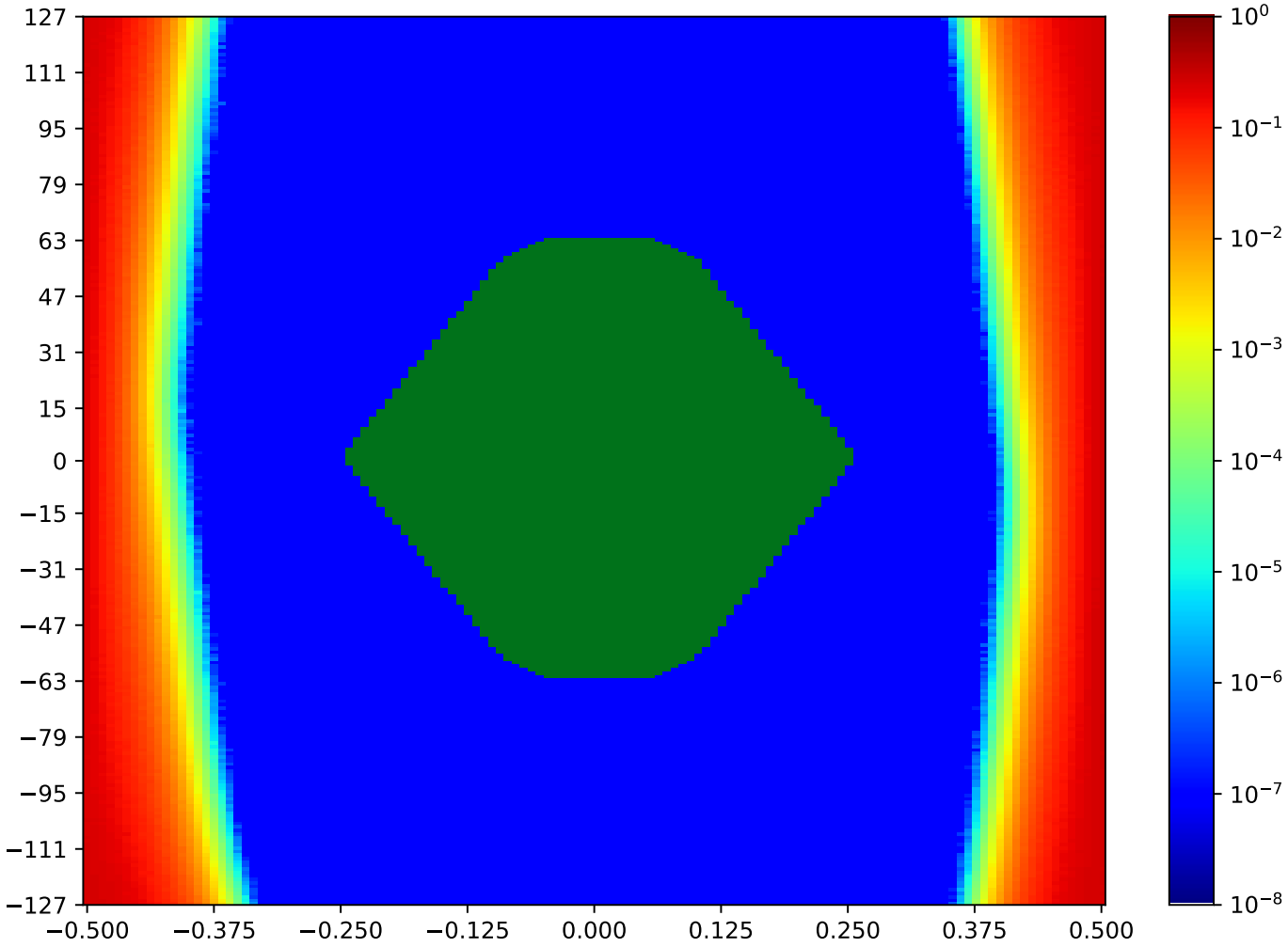


Figure 3.244: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.5 MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Table 3.226: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:20:26		2018-Sep-27 18:21:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24397	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

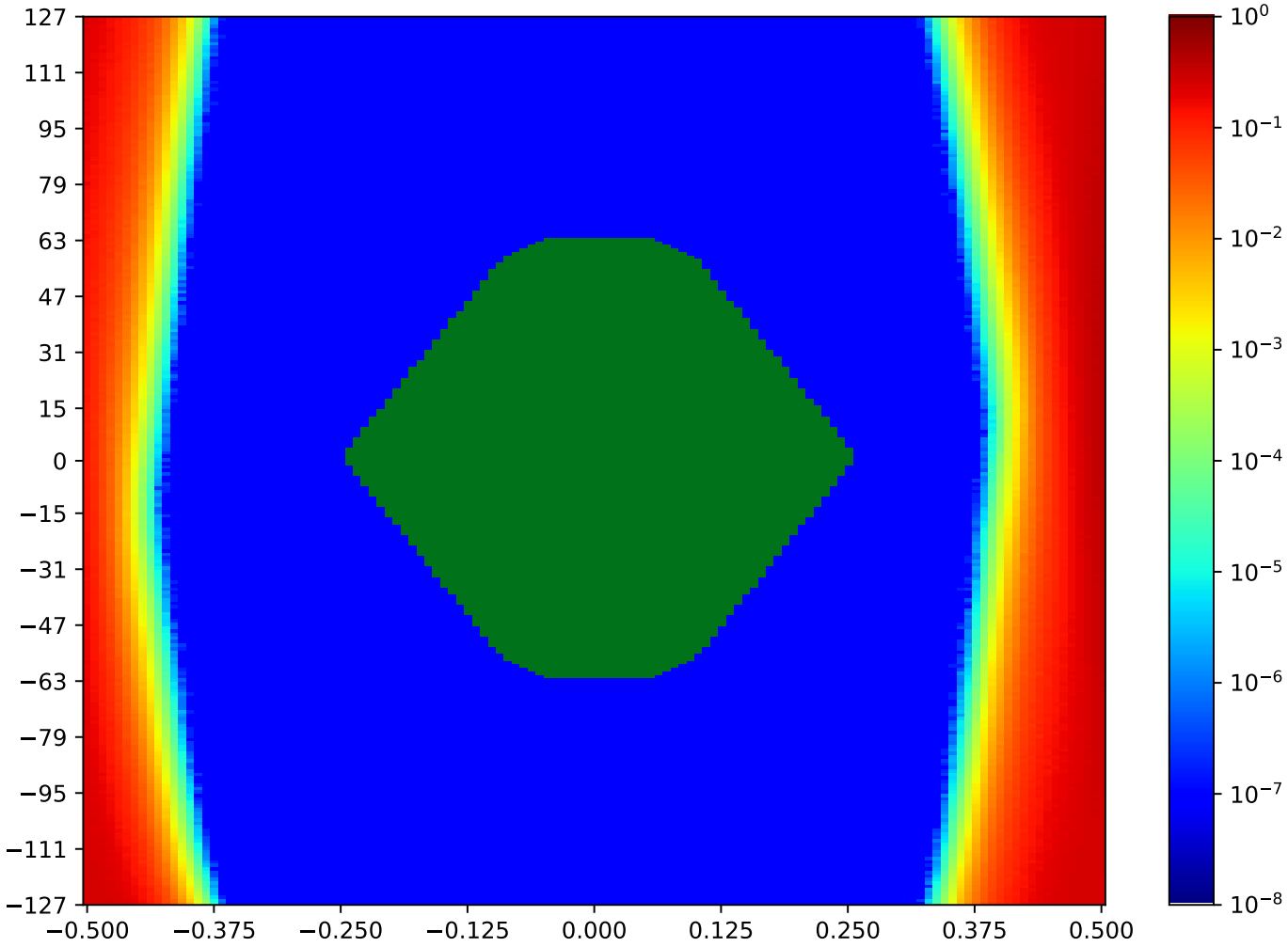


Figure 3.245: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.6 MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Table 3.227: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:09:16		2018-Sep-27 18:10:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24449	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

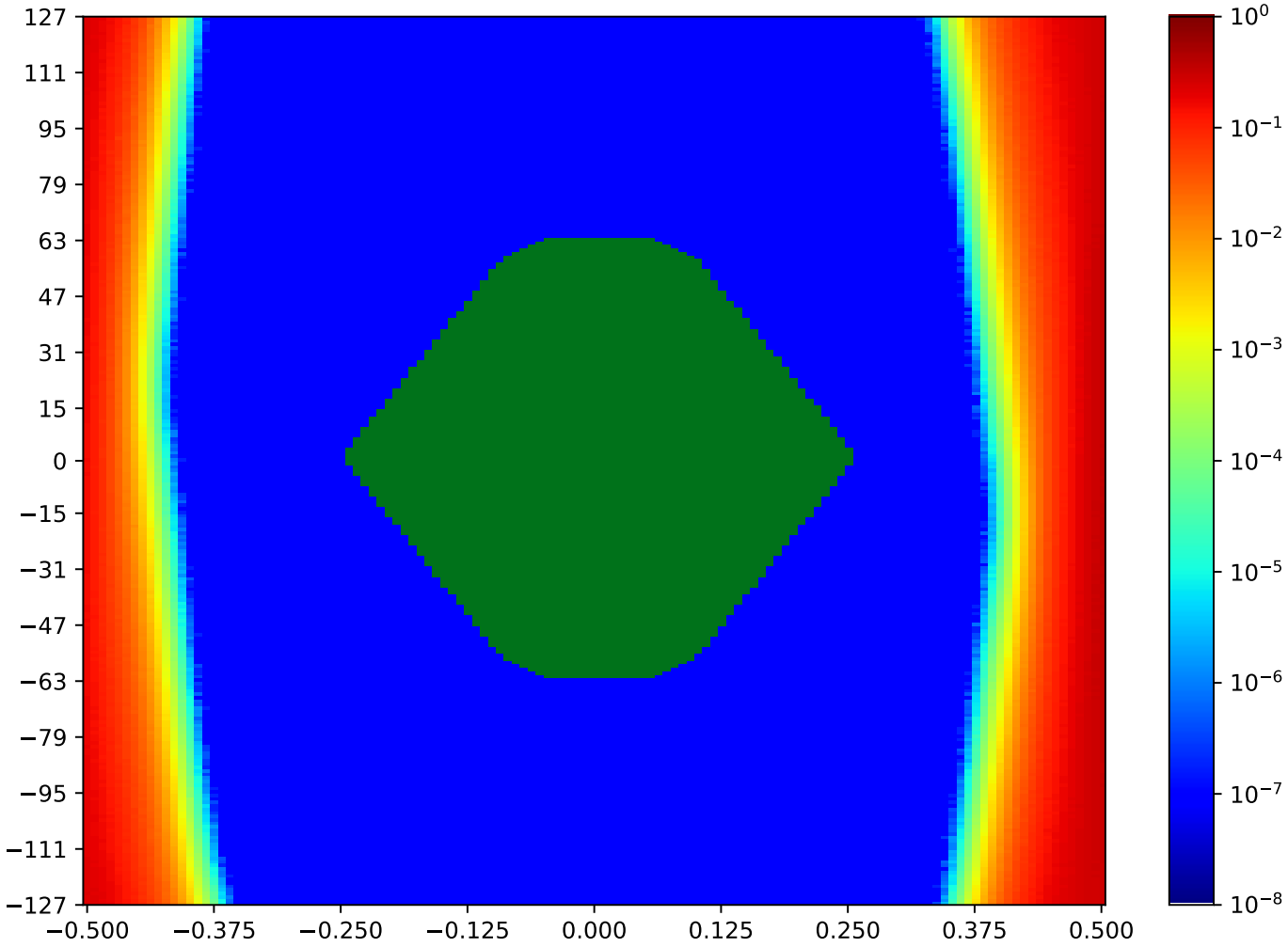


Figure 3.246: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.7 MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Table 3.228: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:22:54		2018-Sep-27 18:24:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24598	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

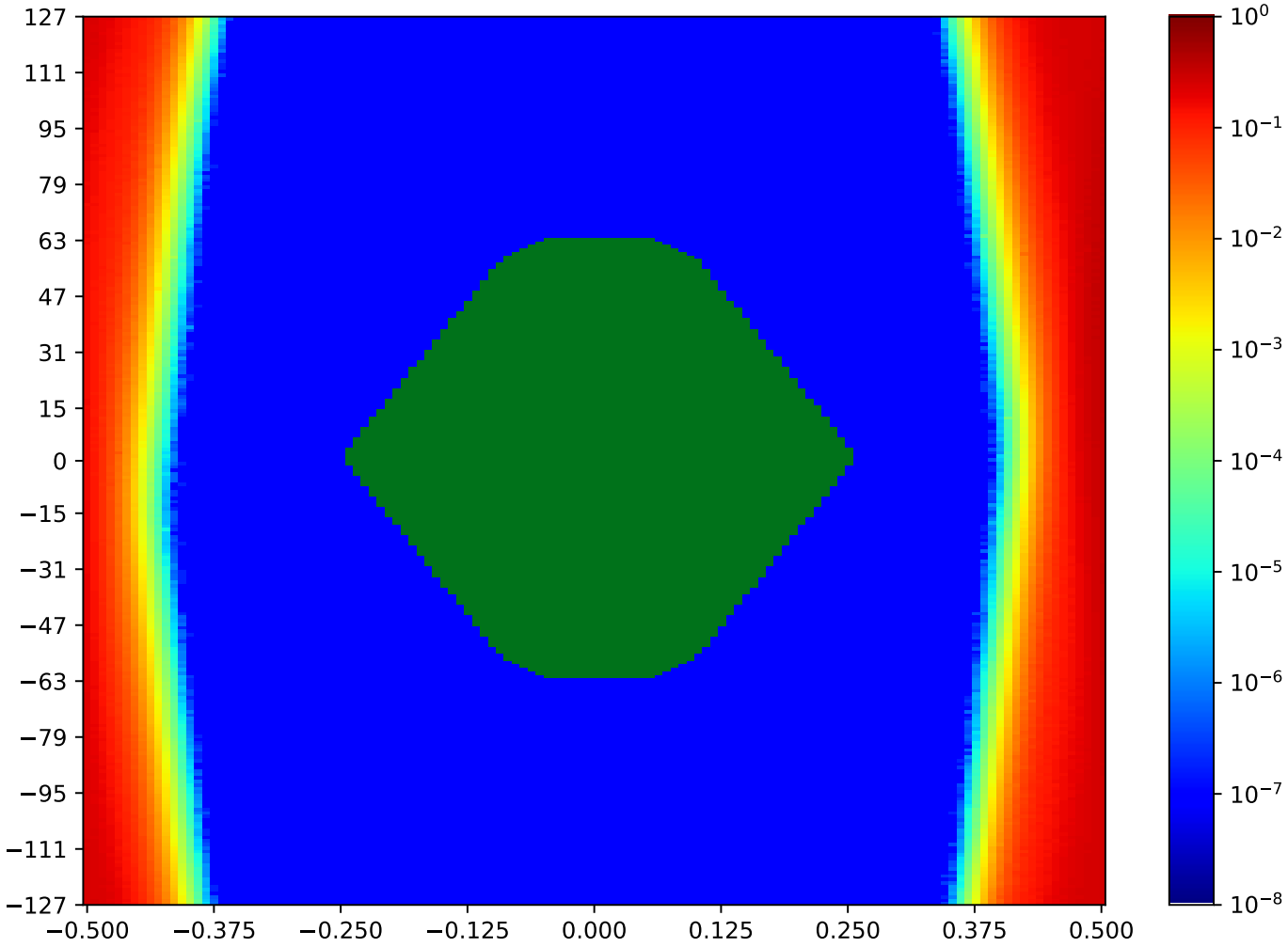


Figure 3.247: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.8 MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Table 3.229: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:11:45		2018-Sep-27 18:13:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24659	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

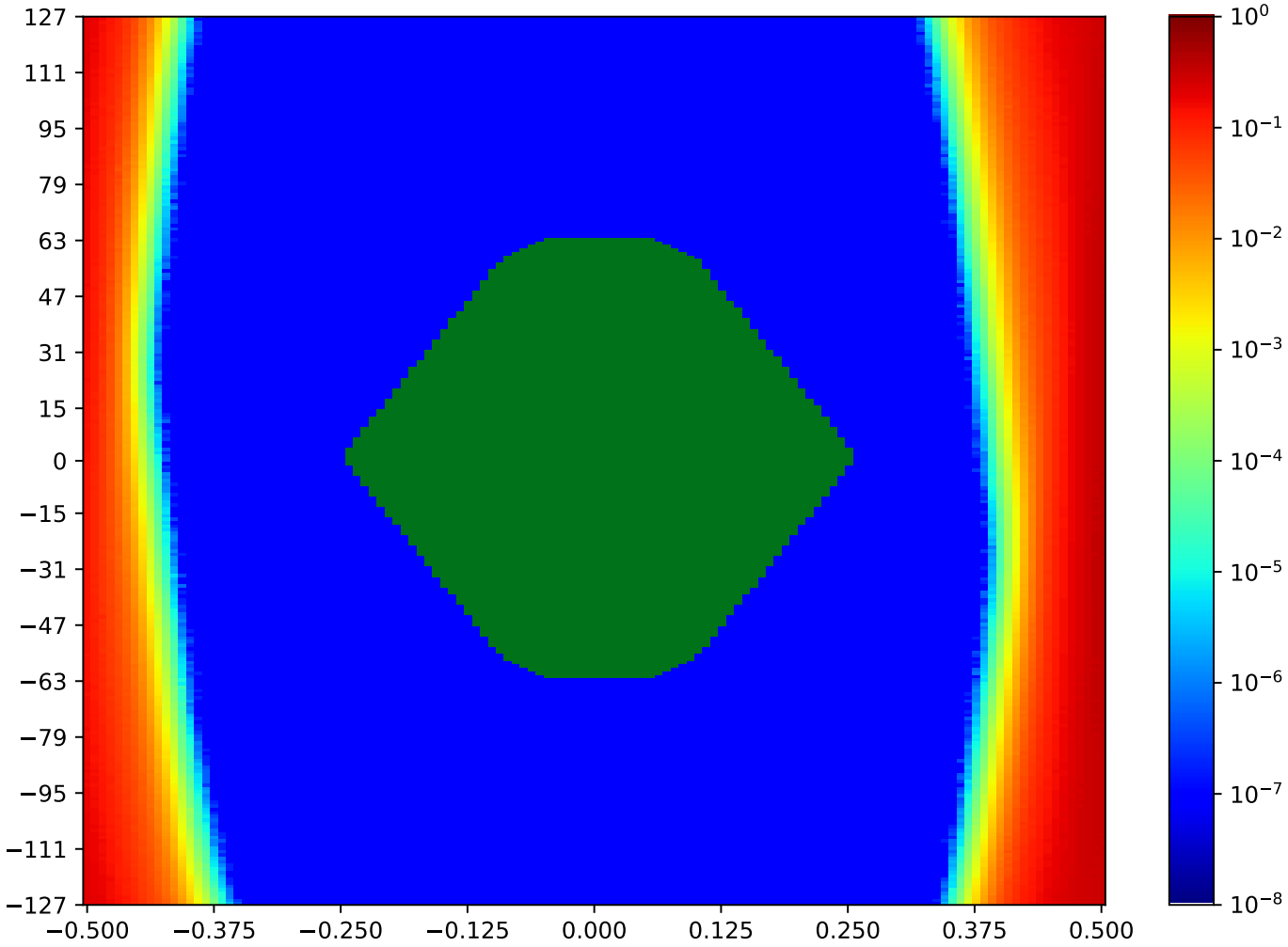


Figure 3.248: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.9 MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Table 3.230: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:21:40		2018-Sep-27 18:22:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24531	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

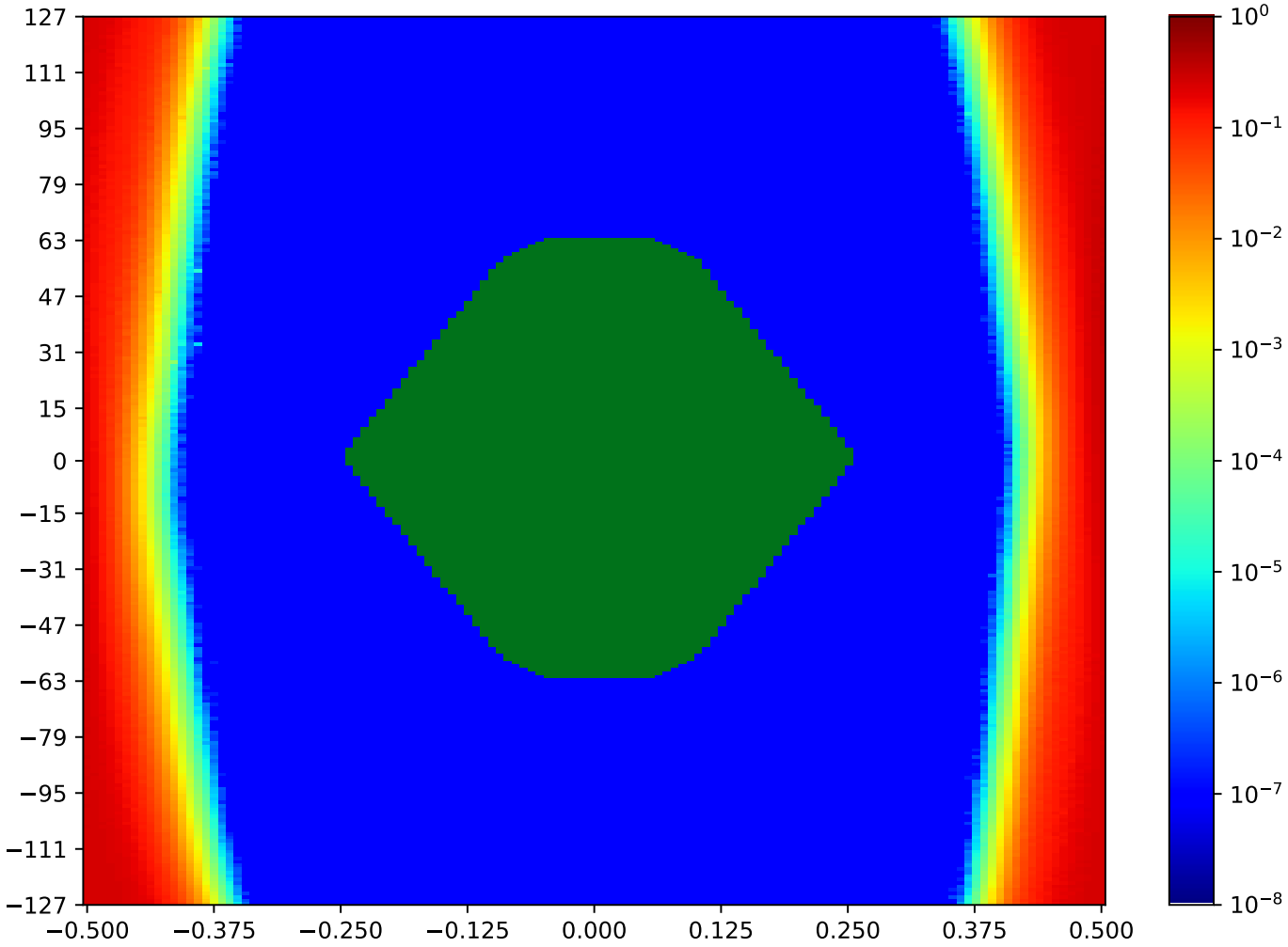


Figure 3.249: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.10 MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Table 3.231: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:14:14		2018-Sep-27 18:15:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24327	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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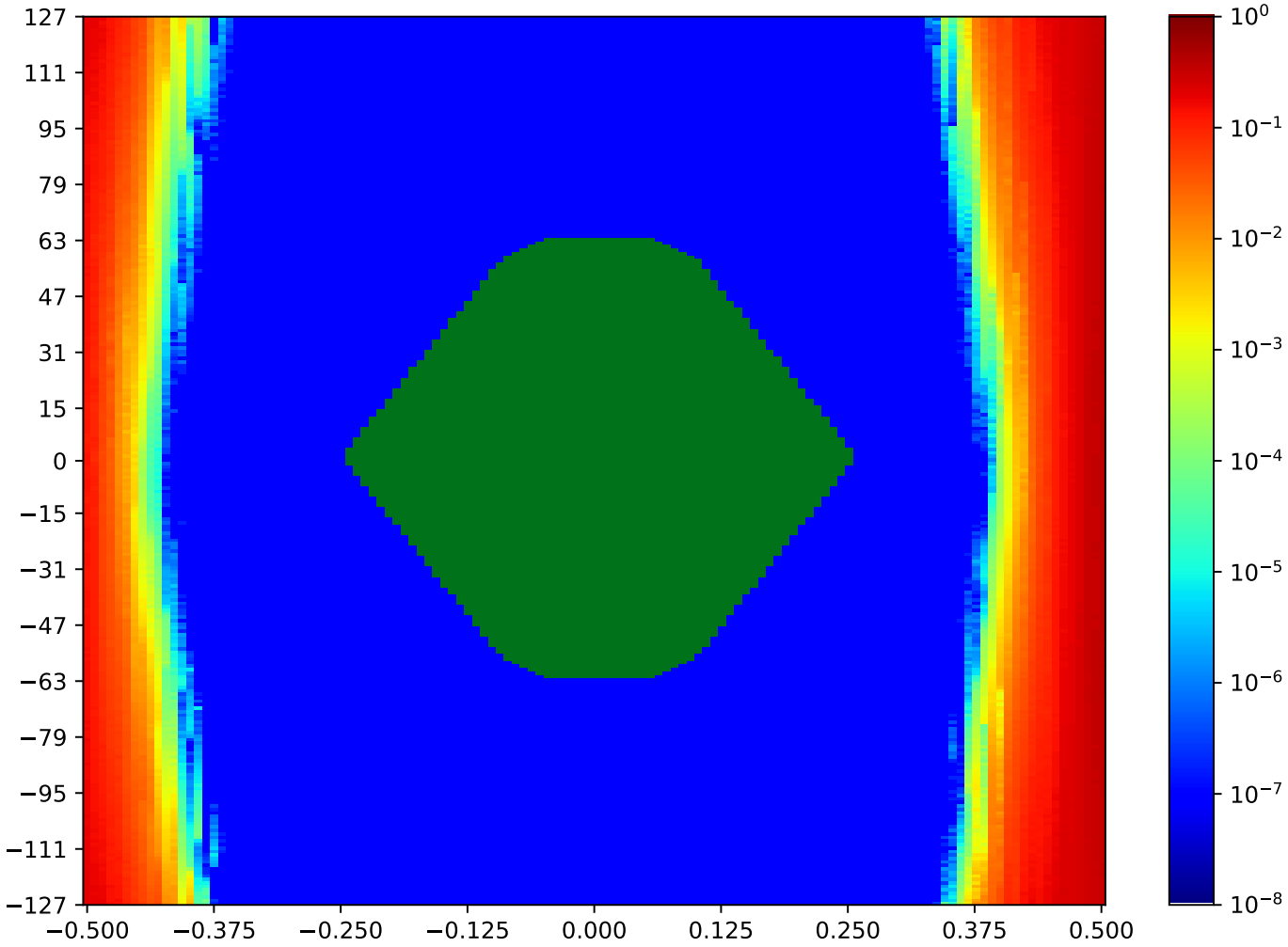


Figure 3.250: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.11 MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Table 3.232: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:19:12		2018-Sep-27 18:20:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24307	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

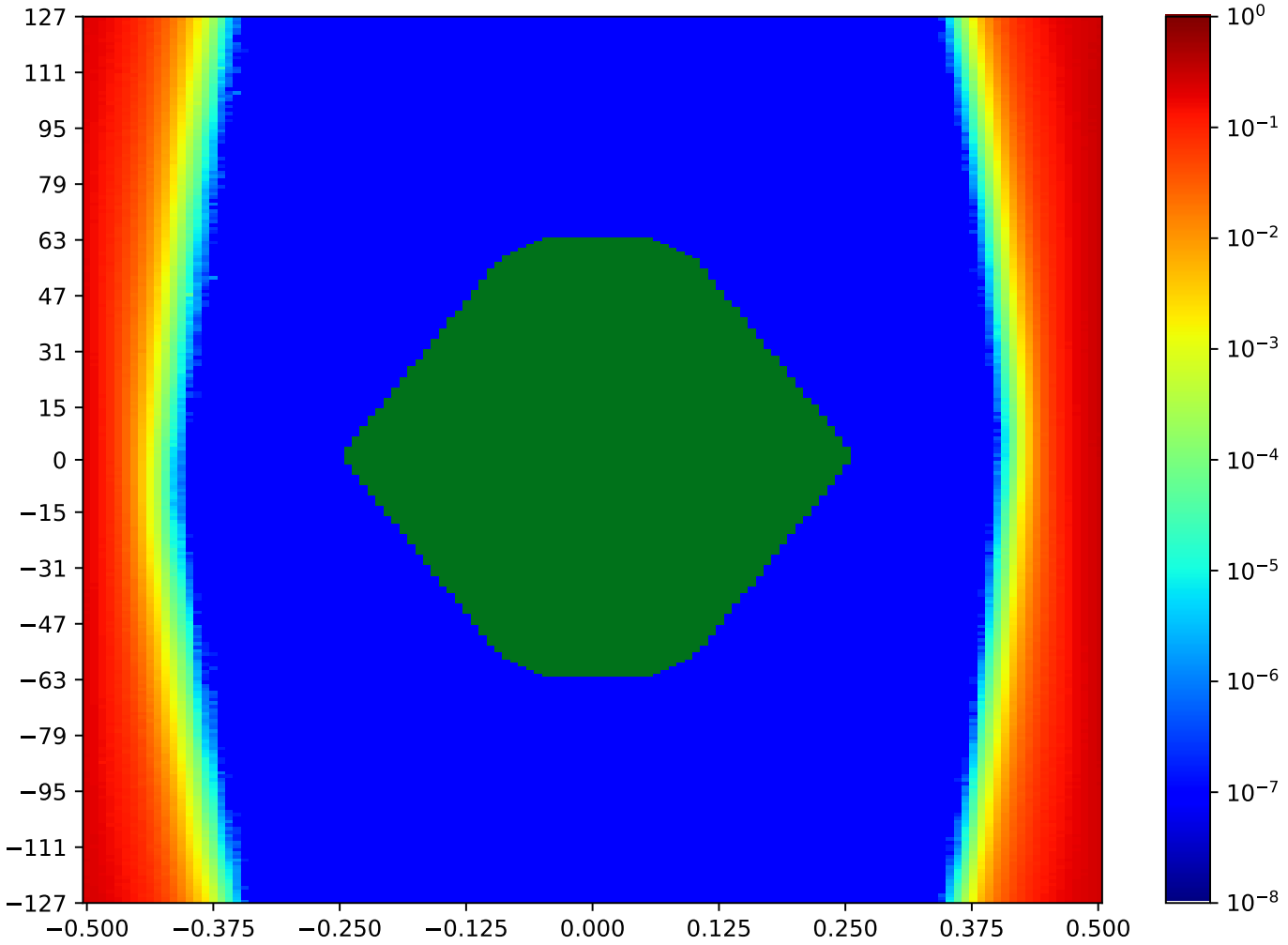


Figure 3.251: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.19.12 MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Table 3.233: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:17:57		2018-Sep-27 18:19:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24559	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

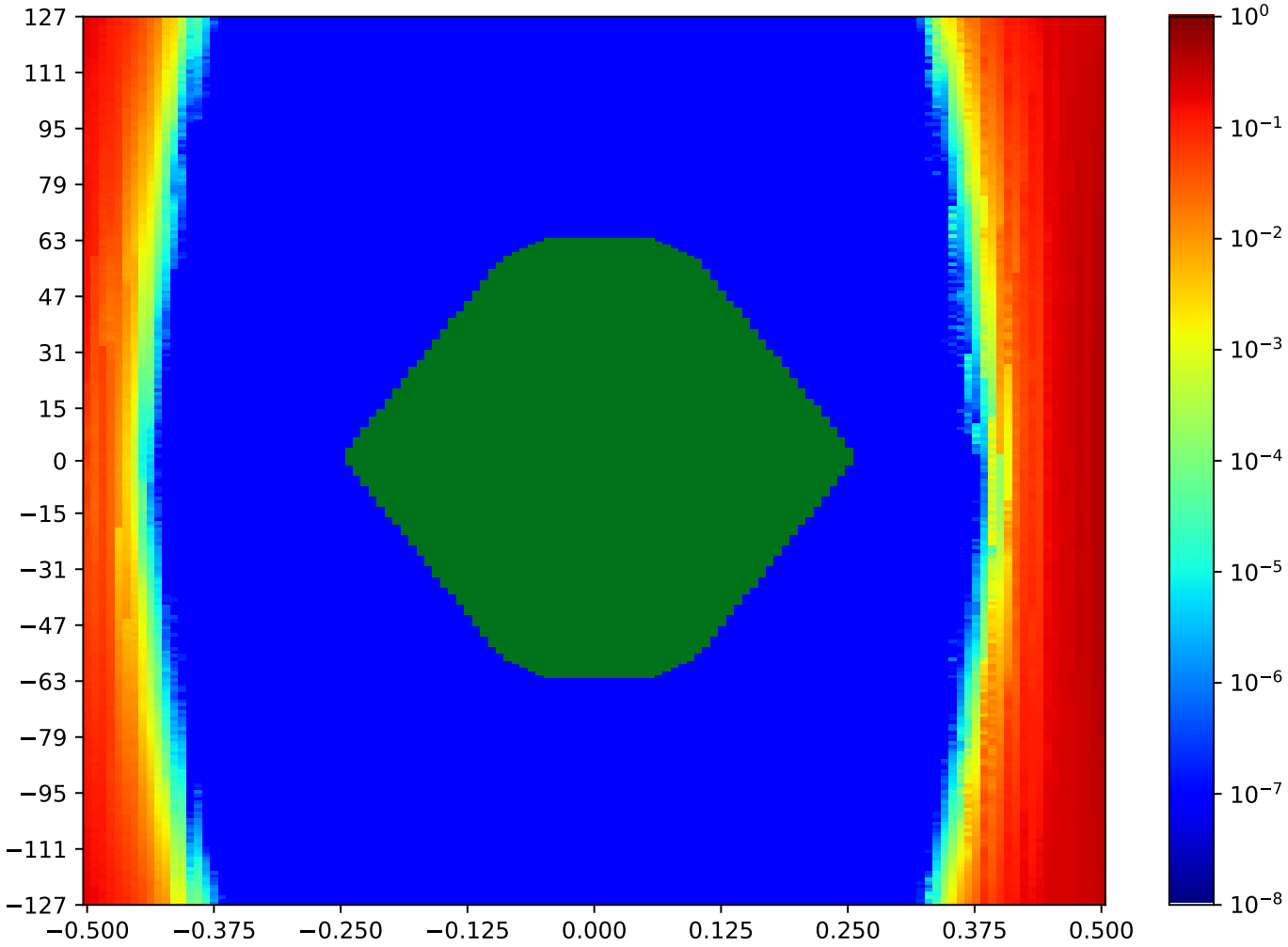


Figure 3.252: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20 MSP_A TX2 MSP_C RX13 Minipod Loopback

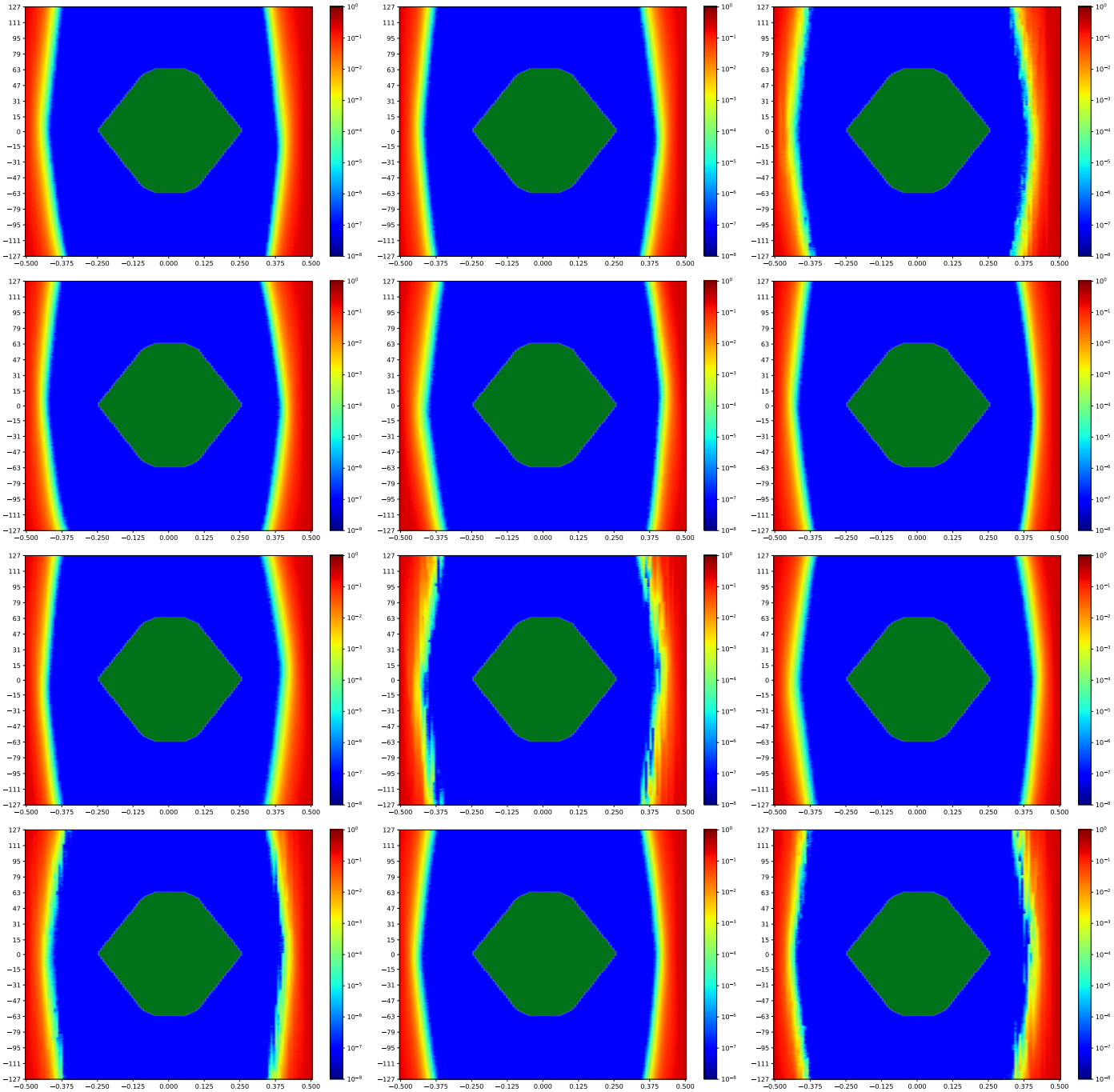


Figure 3.253: MSP_A TX2 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.266.

3.20.1 MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Table 3.234: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:27:52		2018-Sep-27 18:29:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24229	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

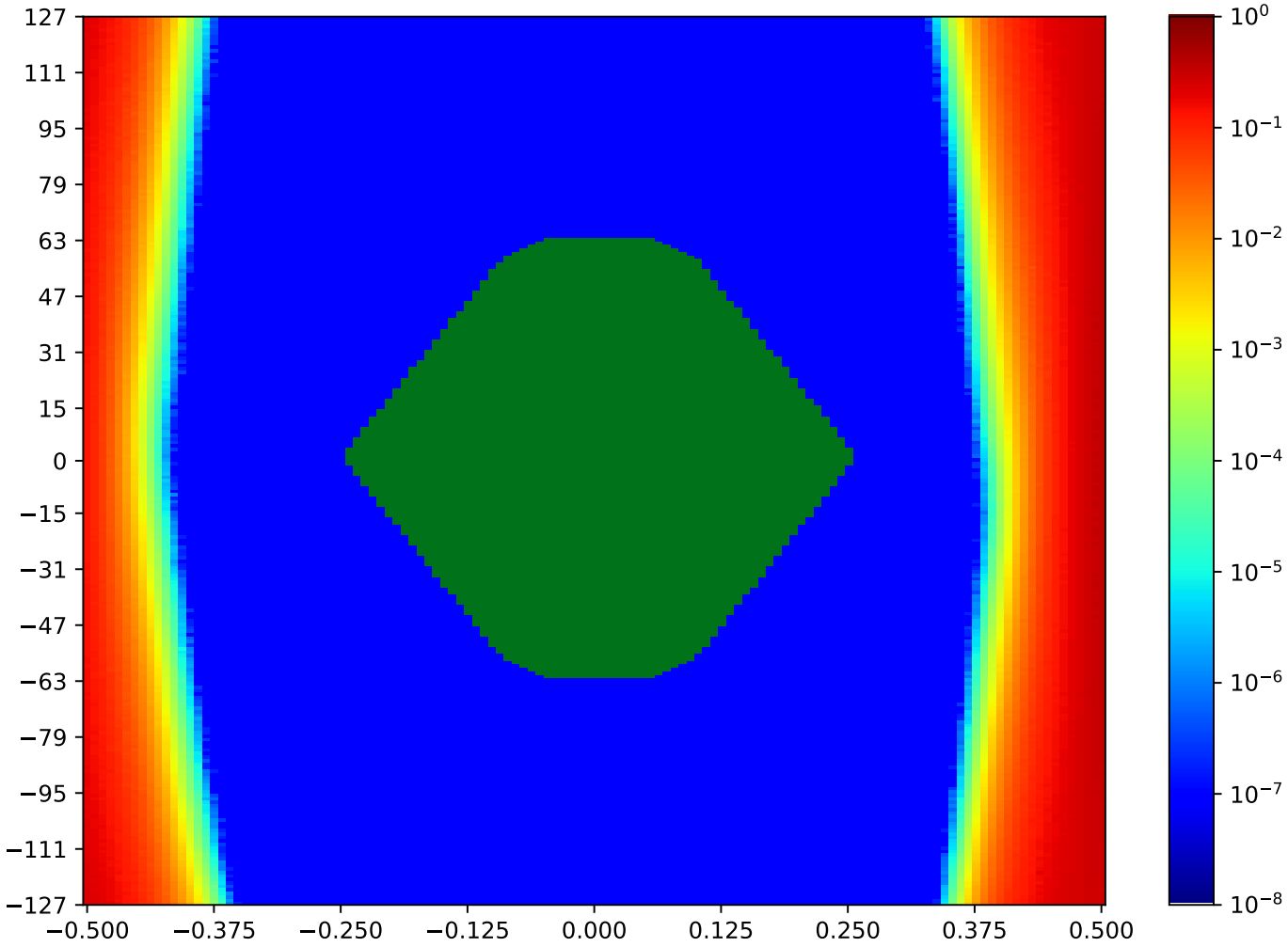


Figure 3.254: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.2 MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Table 3.235: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:25:23		2018-Sep-27 18:26:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24499	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

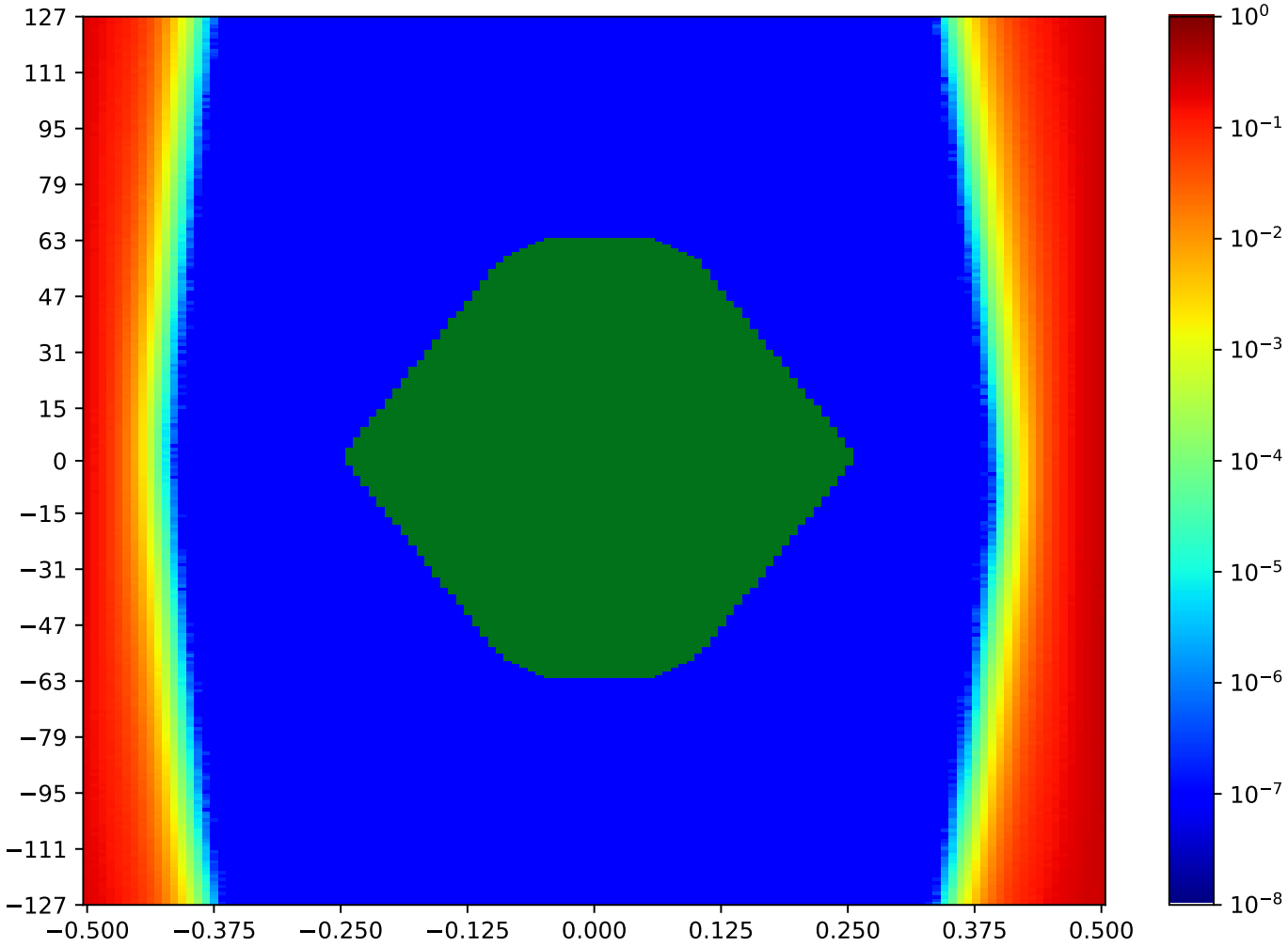


Figure 3.255: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.3 MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Table 3.236: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:31:36		2018-Sep-27 18:32:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24079	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

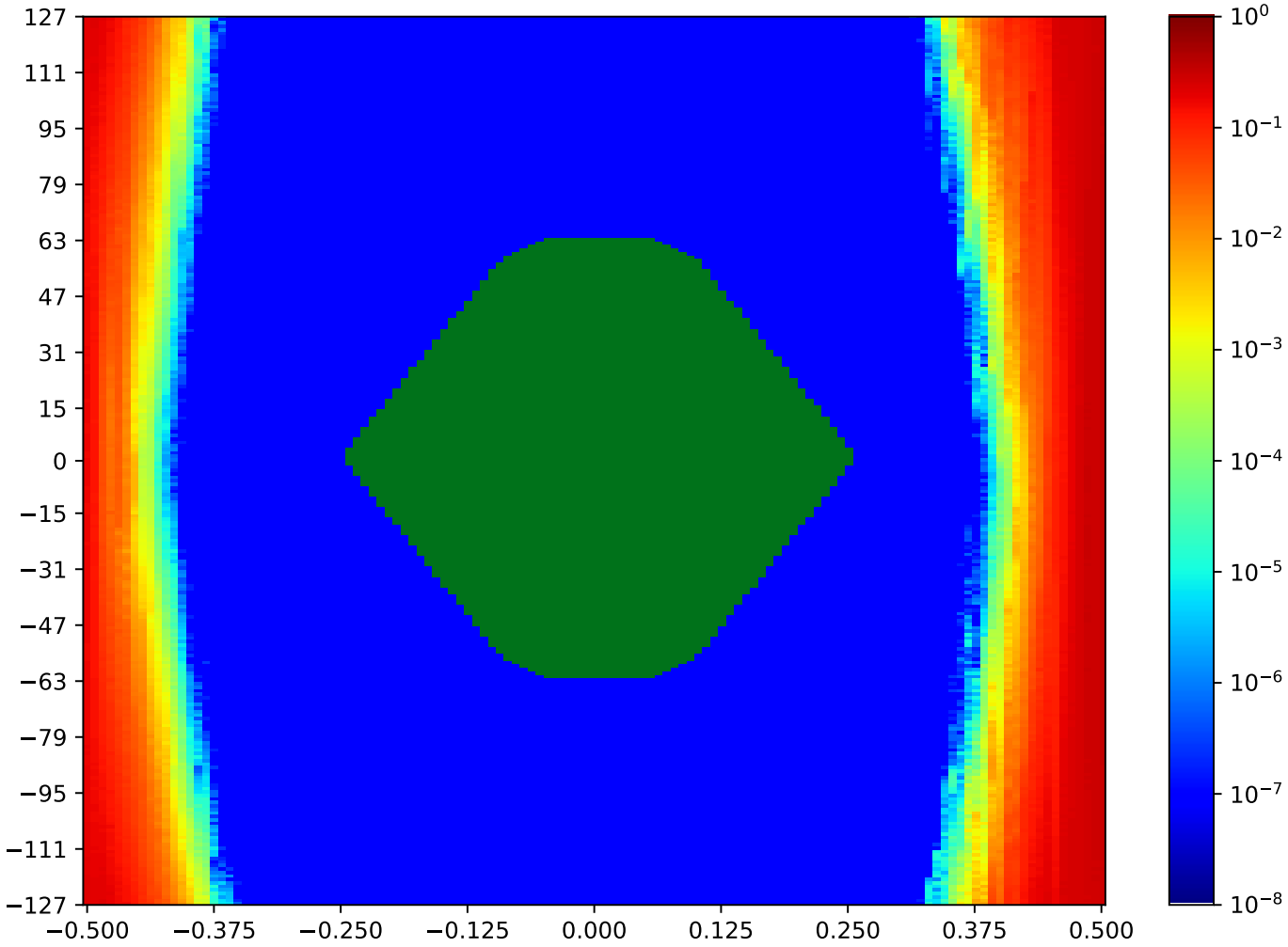


Figure 3.256: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.4 MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Table 3.237: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:24:09		2018-Sep-27 18:25:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24318	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

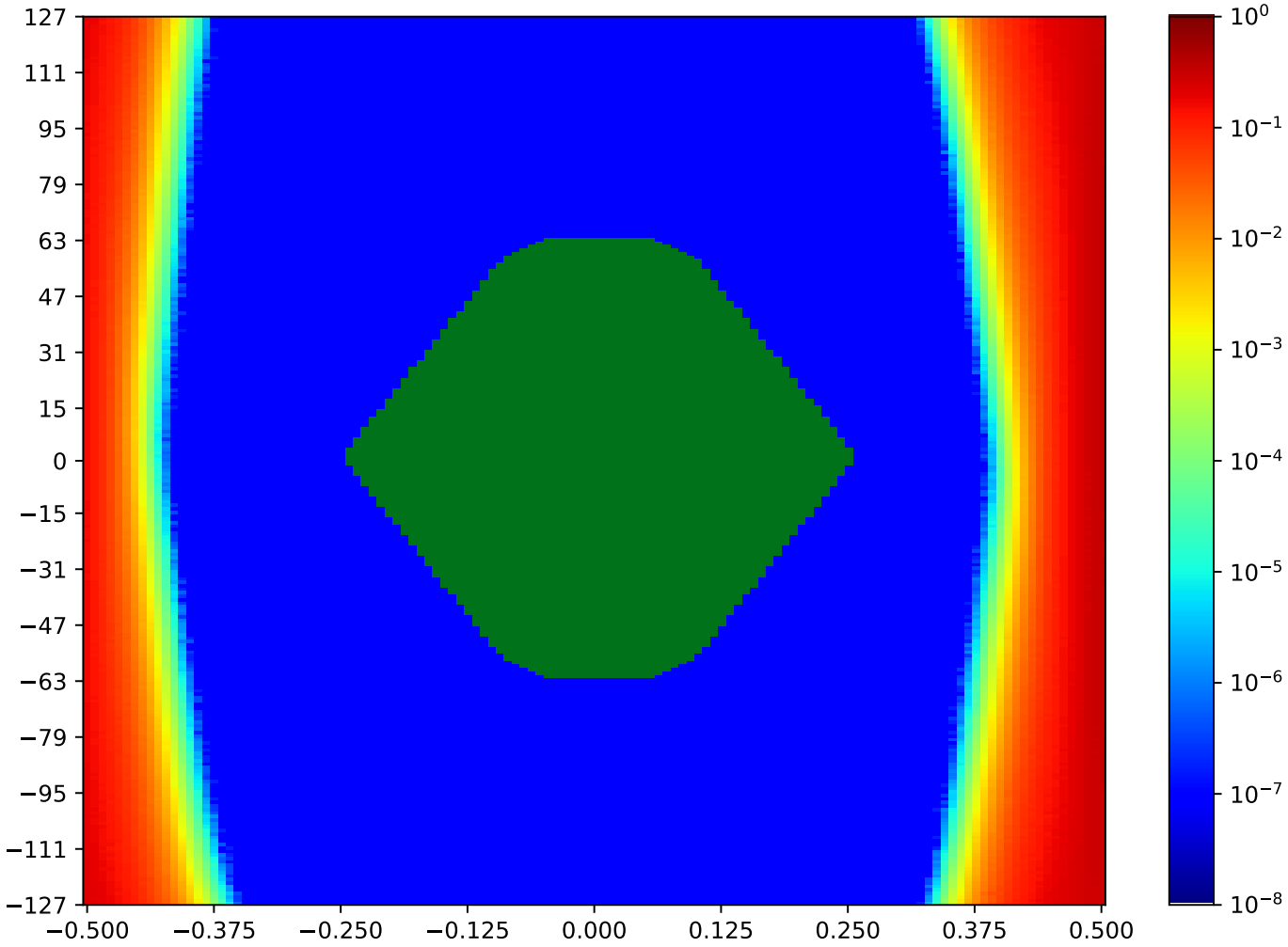


Figure 3.257: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.5 MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Table 3.238: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:35:22		2018-Sep-27 18:36:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24343	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

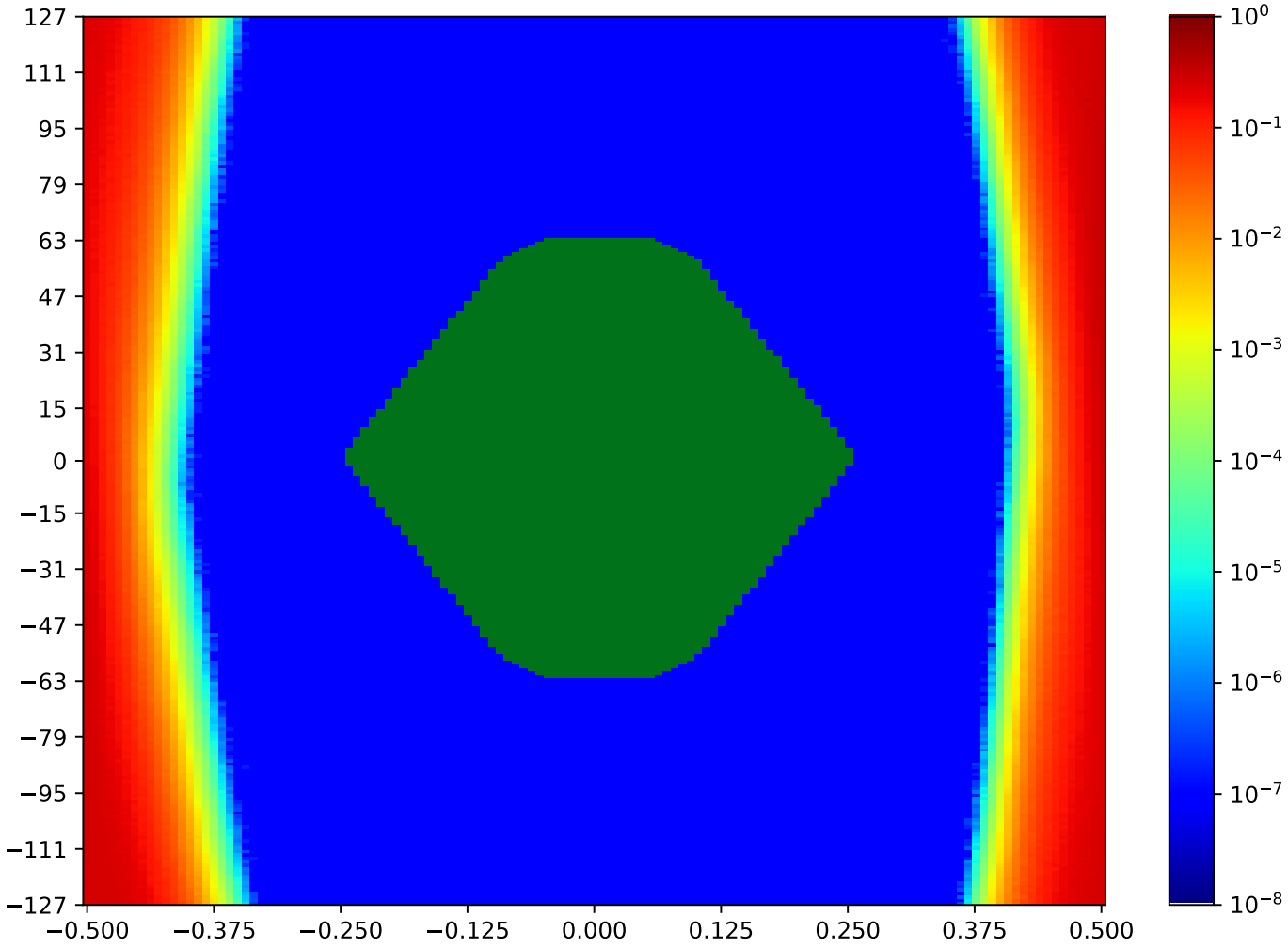


Figure 3.258: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.6 MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Table 3.239: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:26:37		2018-Sep-27 18:27:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24836	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

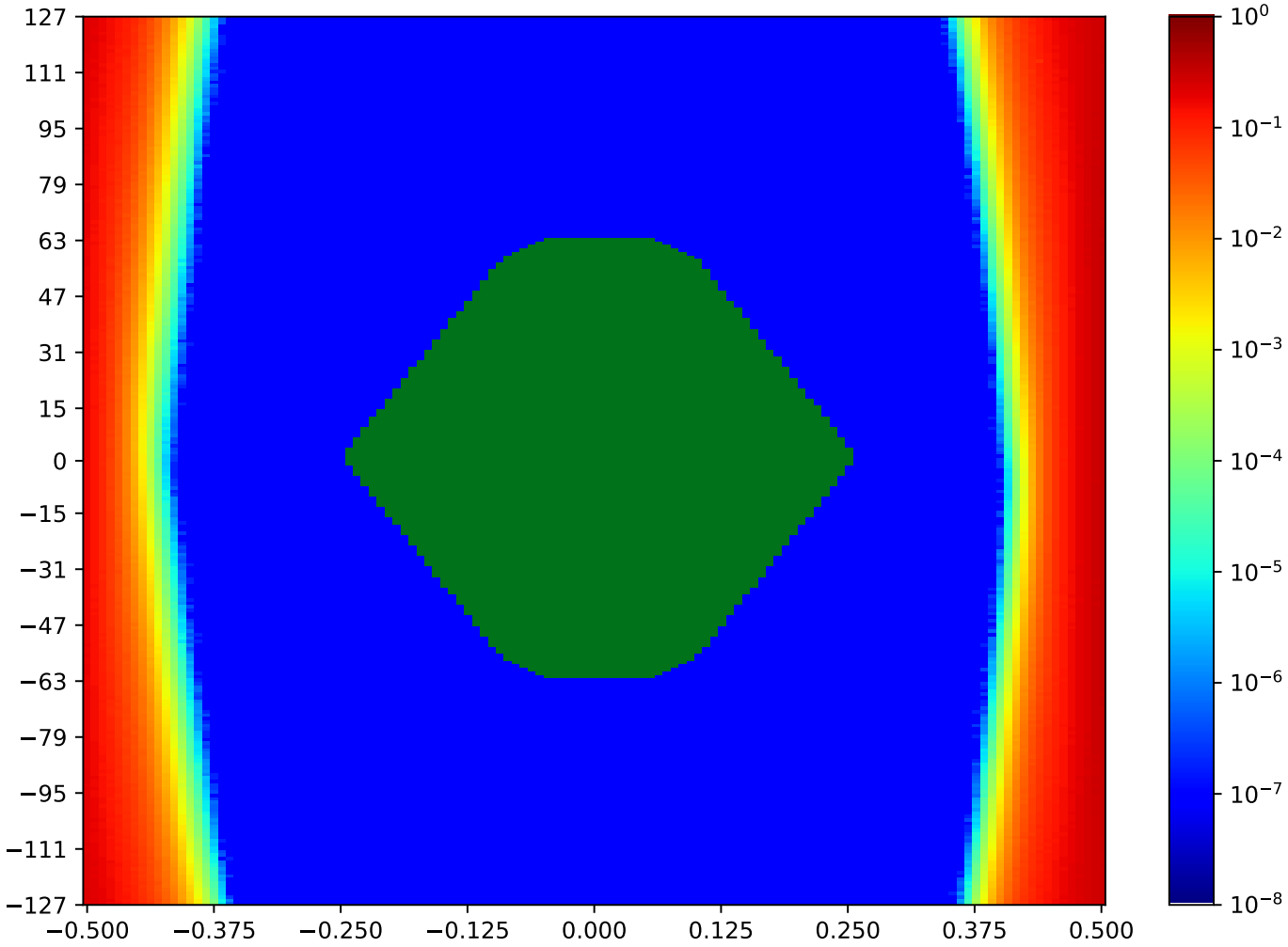


Figure 3.259: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.7 MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Table 3.240: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:37:54		2018-Sep-27 18:39:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24387	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

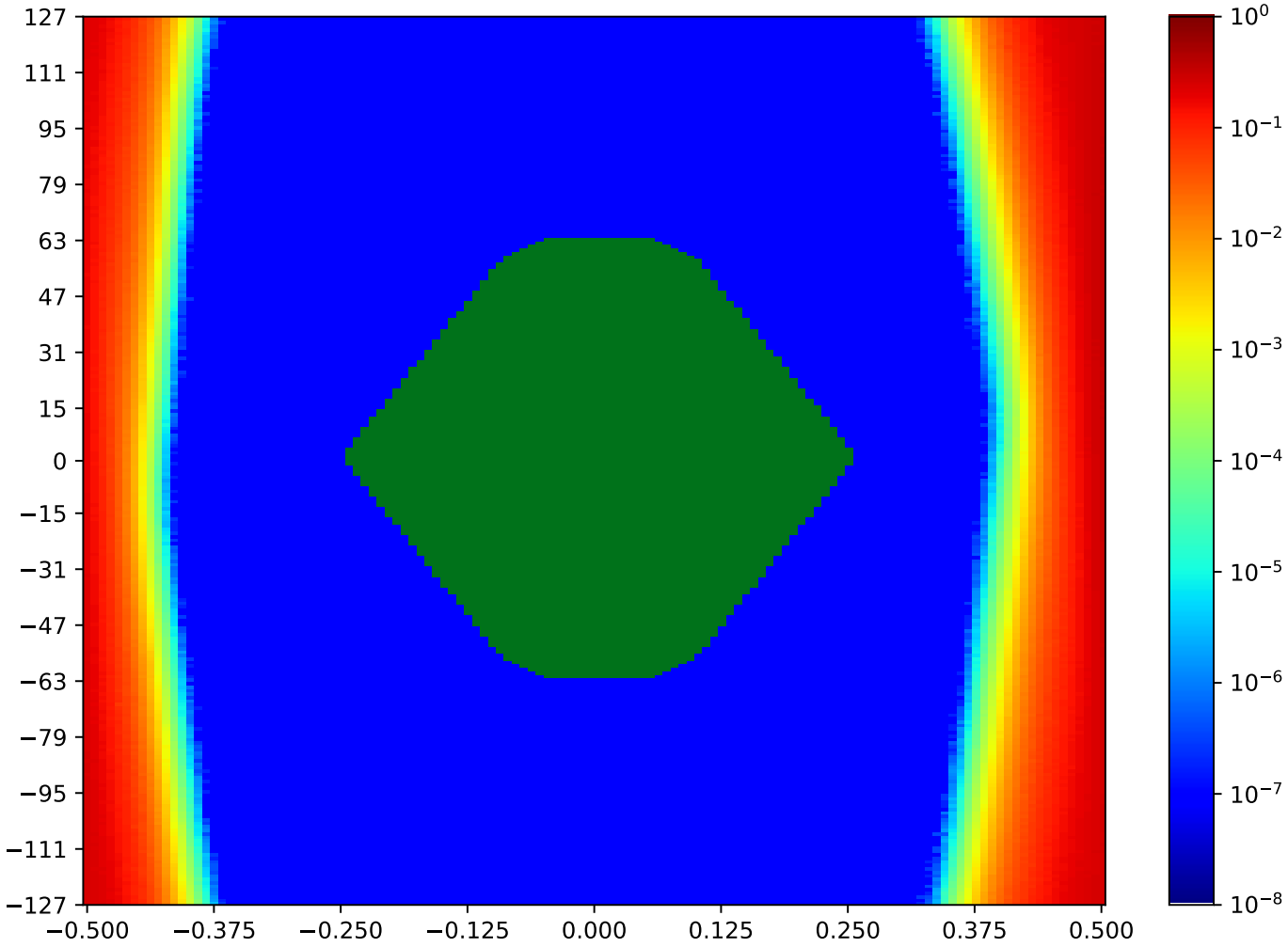


Figure 3.260: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.8 MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Table 3.241: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:29:06		2018-Sep-27 18:30:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24119	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

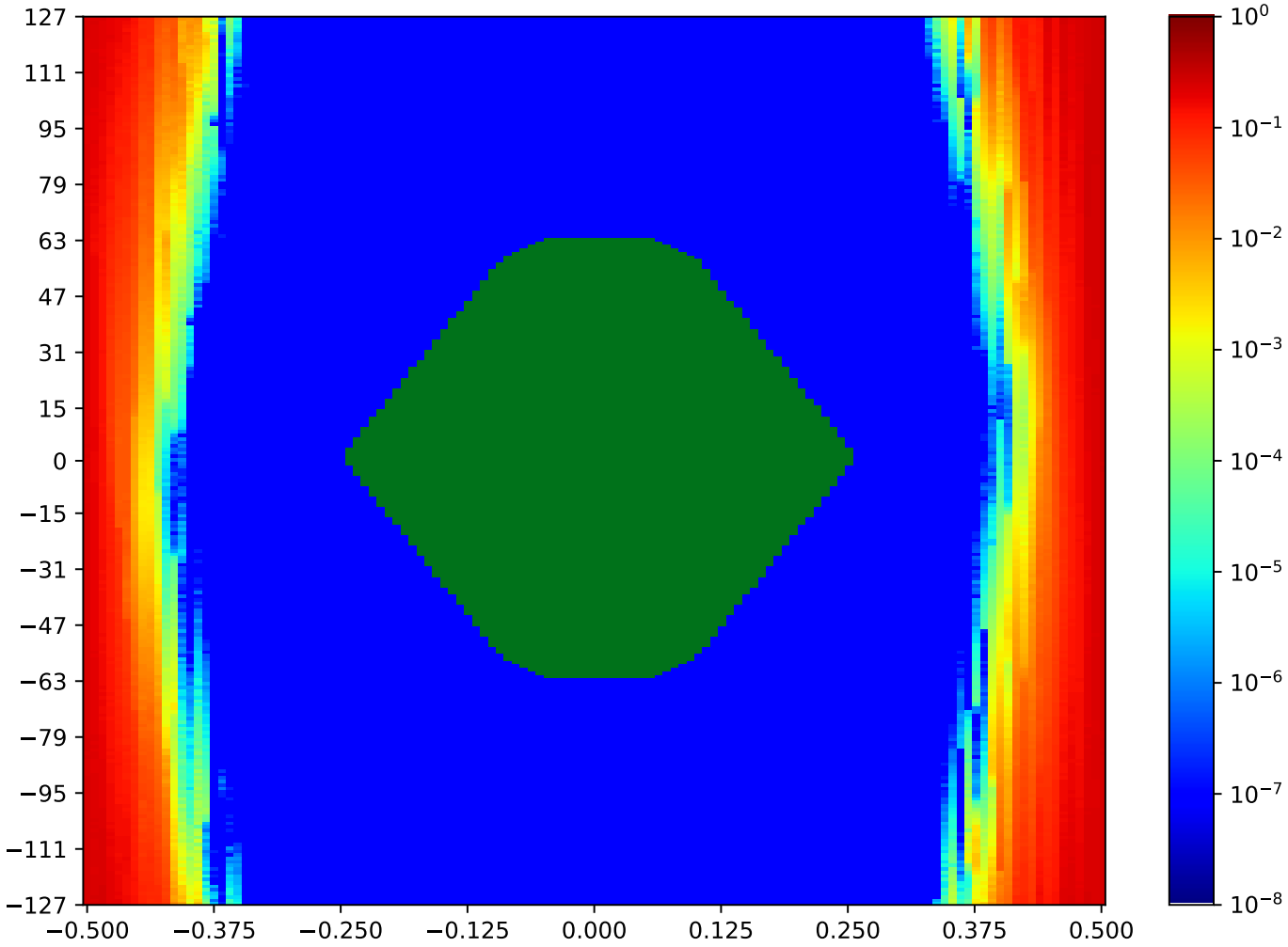


Figure 3.261: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.9 MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Table 3.242: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:36:38		2018-Sep-27 18:37:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24442	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

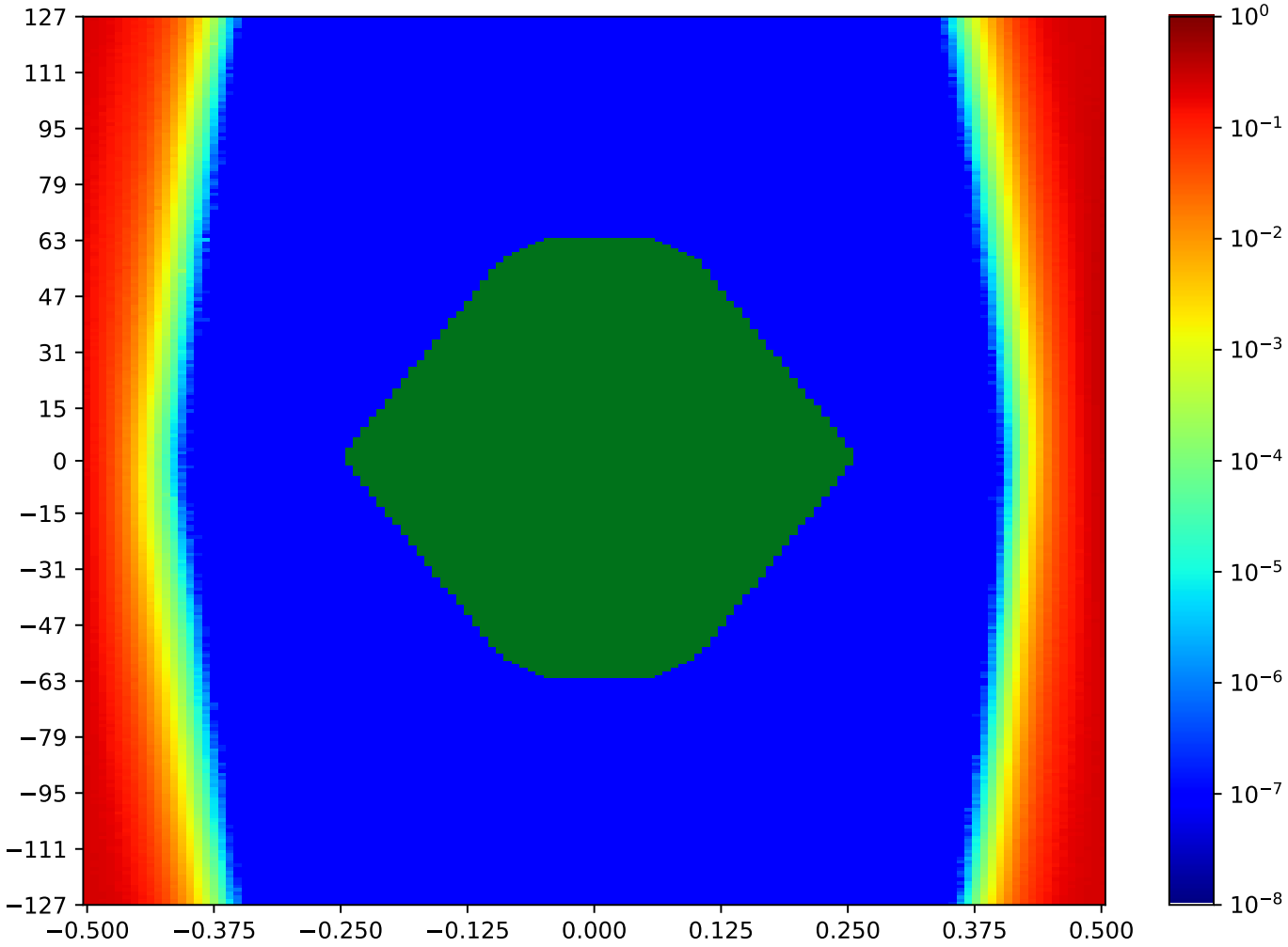


Figure 3.262: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.10 MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Table 3.243: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:30:21		2018-Sep-27 18:31:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24293	101	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

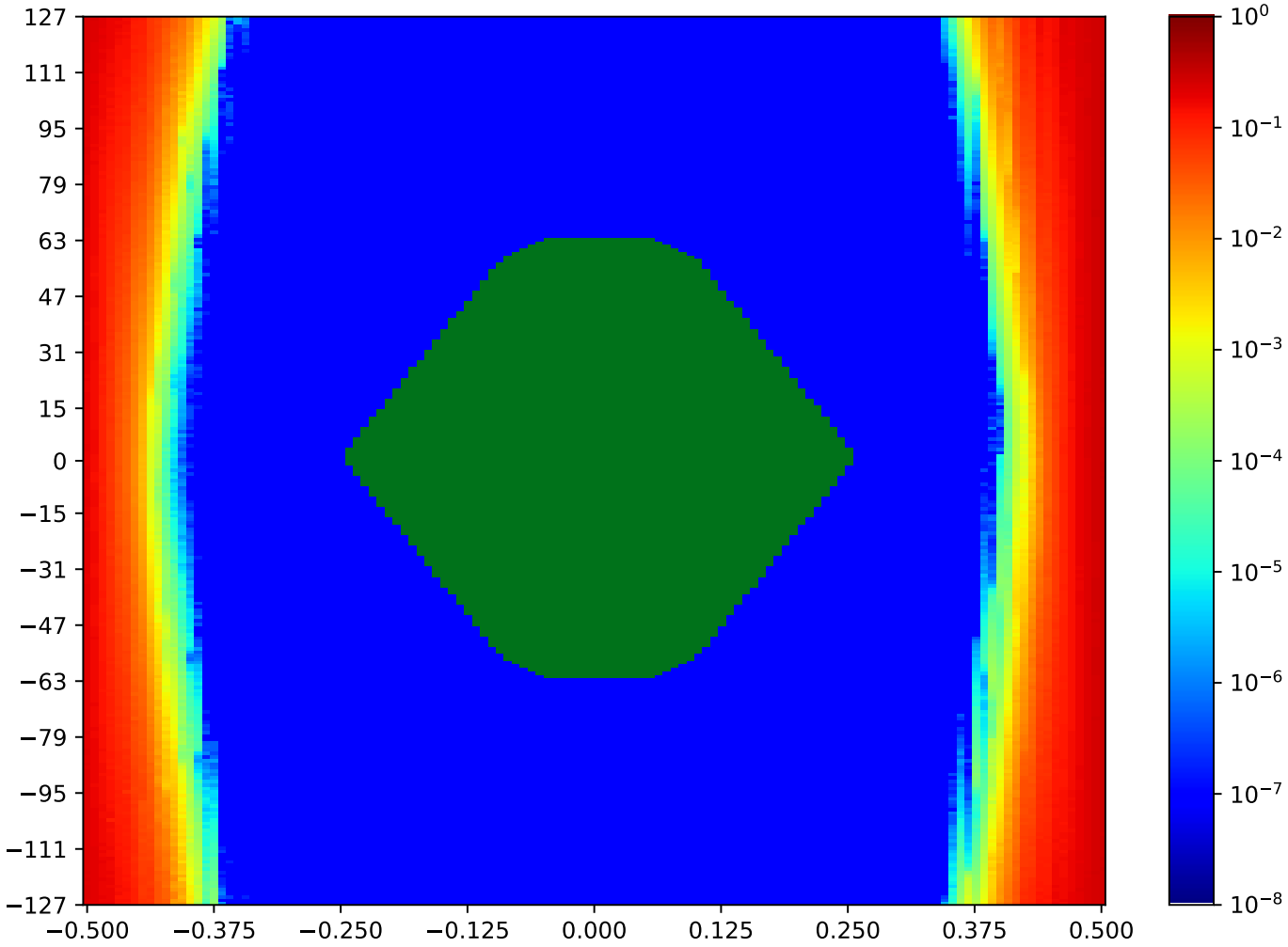


Figure 3.263: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.11 MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Table 3.244: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:34:07		2018-Sep-27 18:35:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24791	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

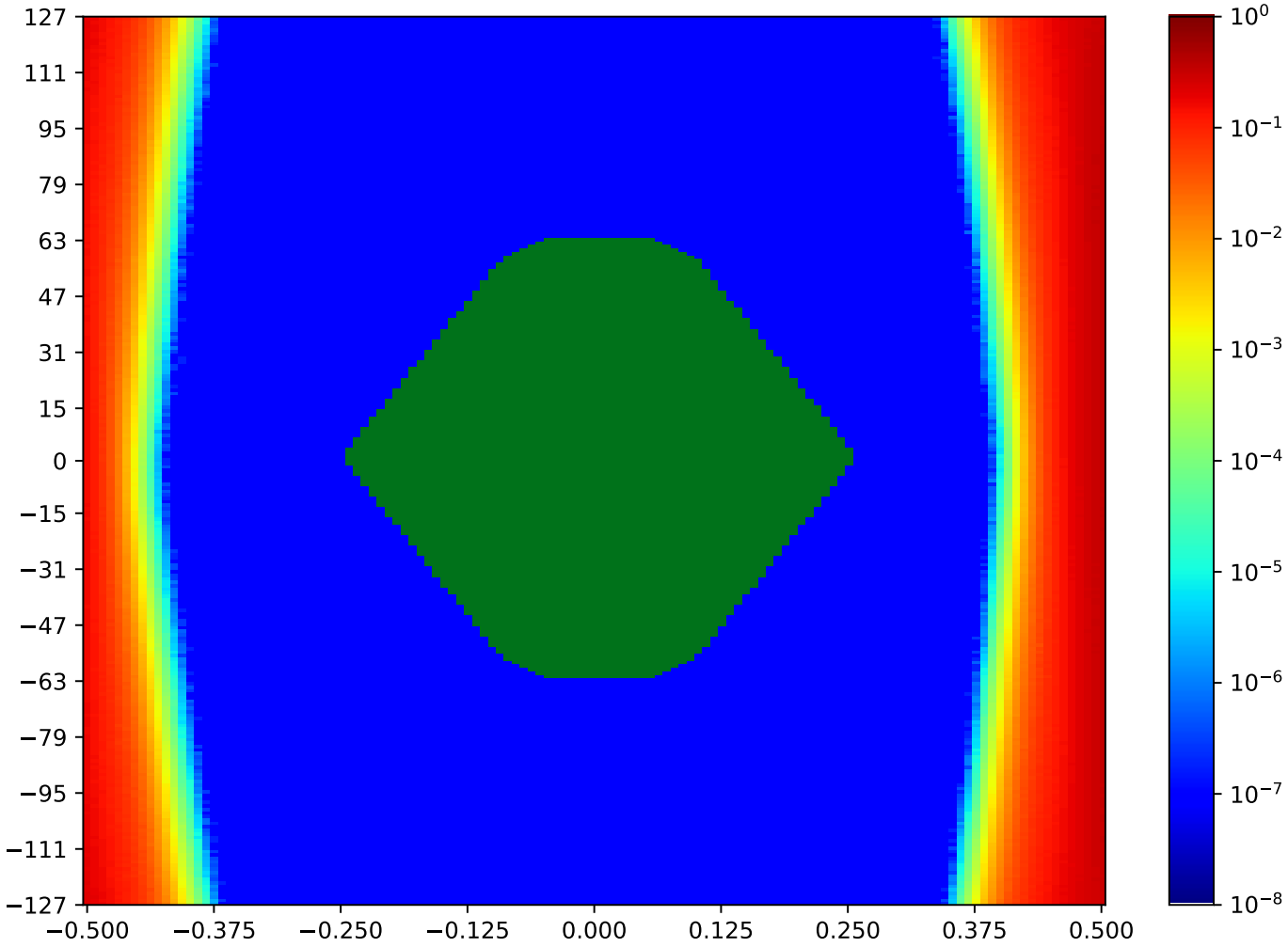


Figure 3.264: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.20.12 MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Table 3.245: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:32:51		2018-Sep-27 18:34:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24492	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

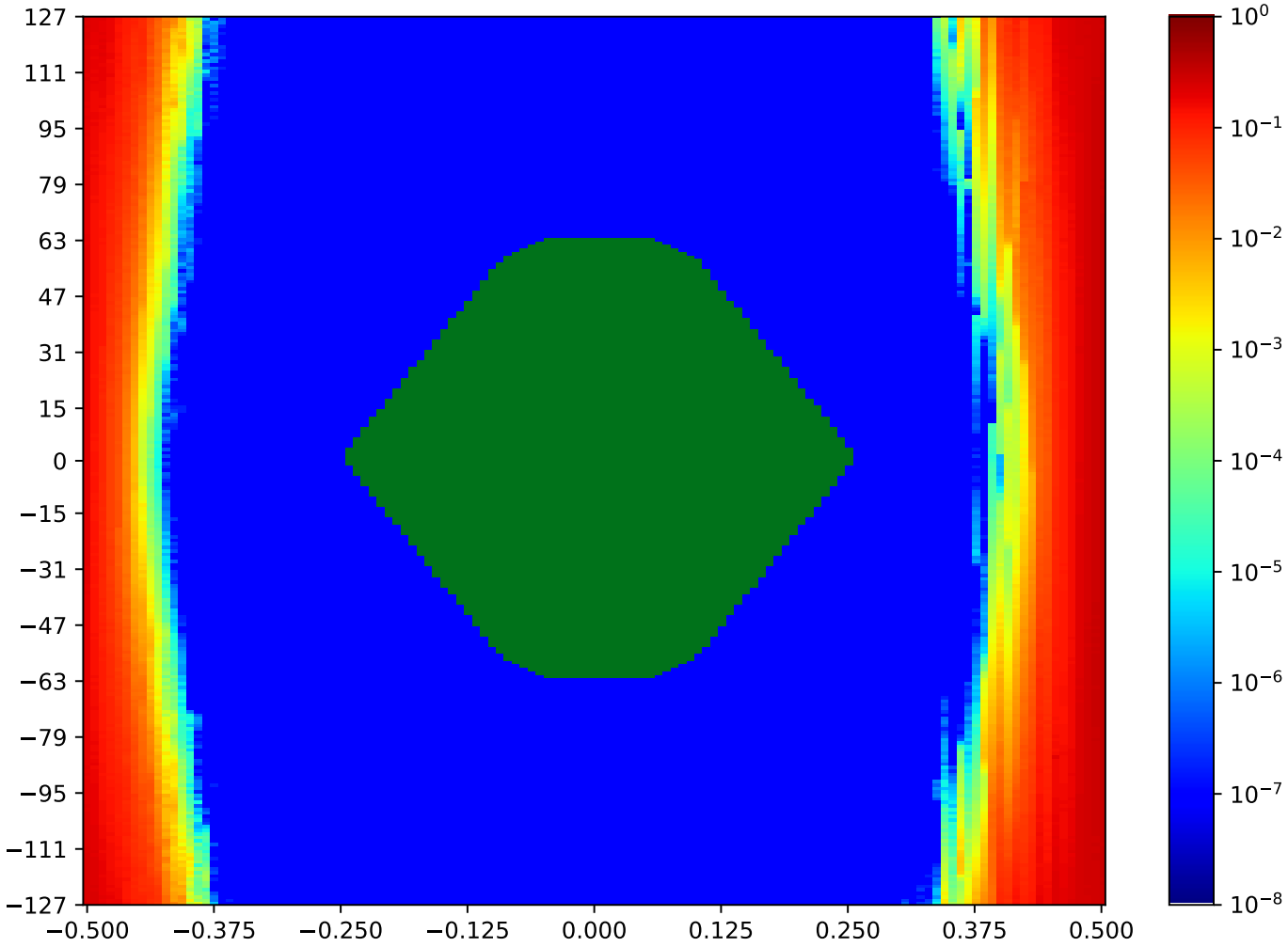


Figure 3.265: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21 MSP_C TX3 MSP_A RX3 Minipod Loopback

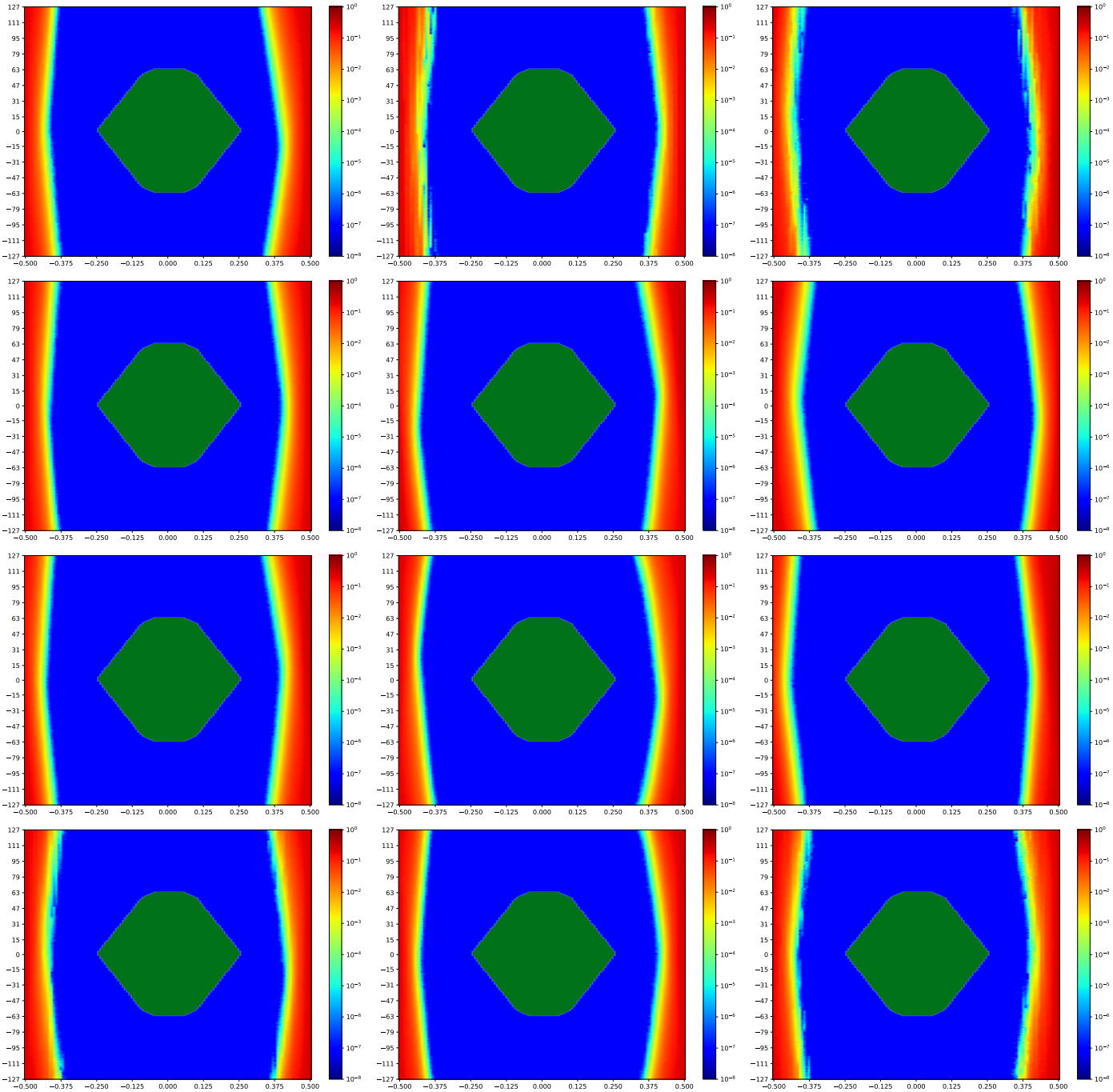


Figure 3.266: MSP_C TX3 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 3.279.

3.21.1 MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Table 3.246: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:42:57		2018-Sep-27 18:44:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24086	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

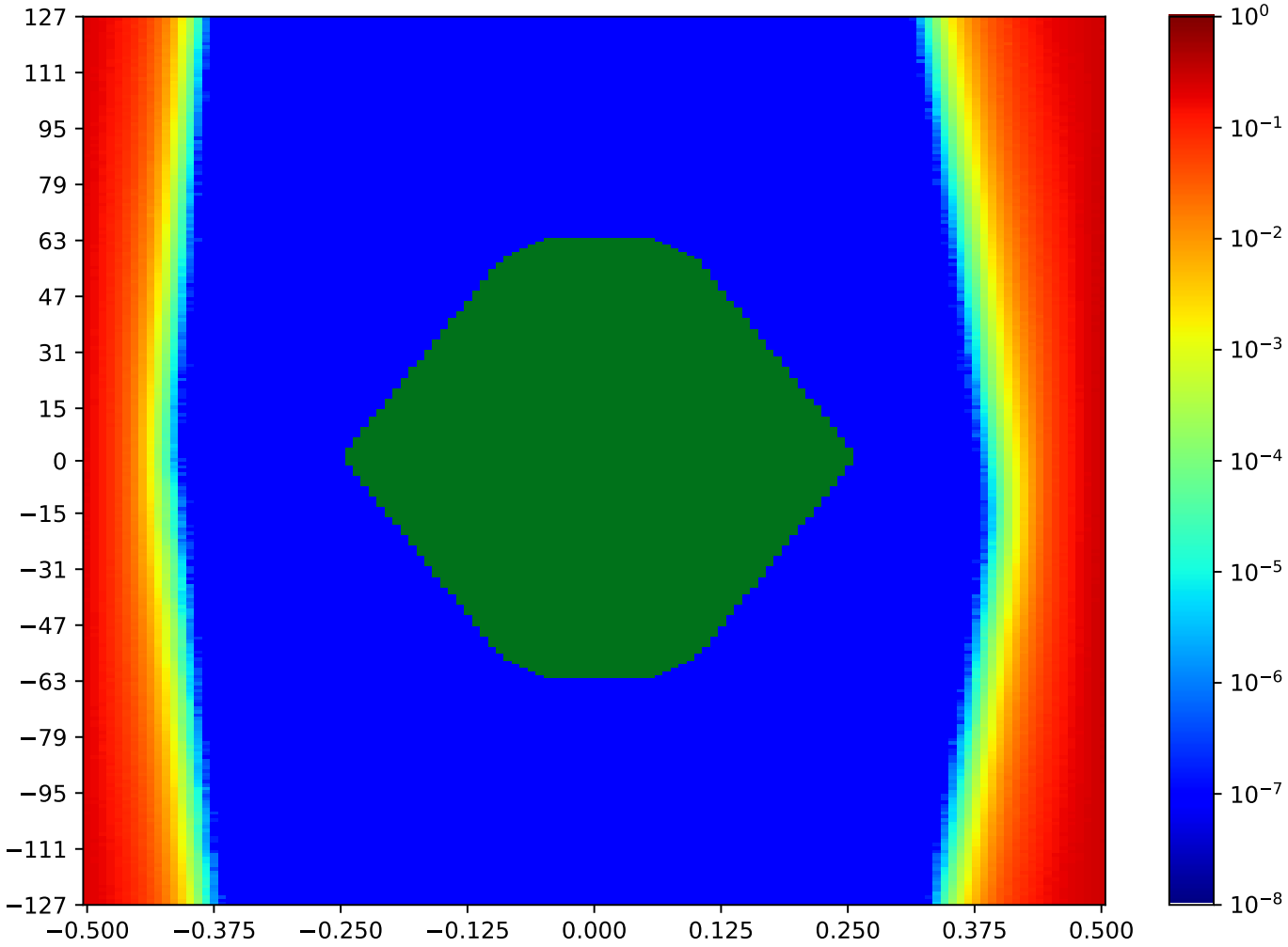


Figure 3.267: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.2 MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Table 3.247: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:45:28		2018-Sep-27 18:46:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24805	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

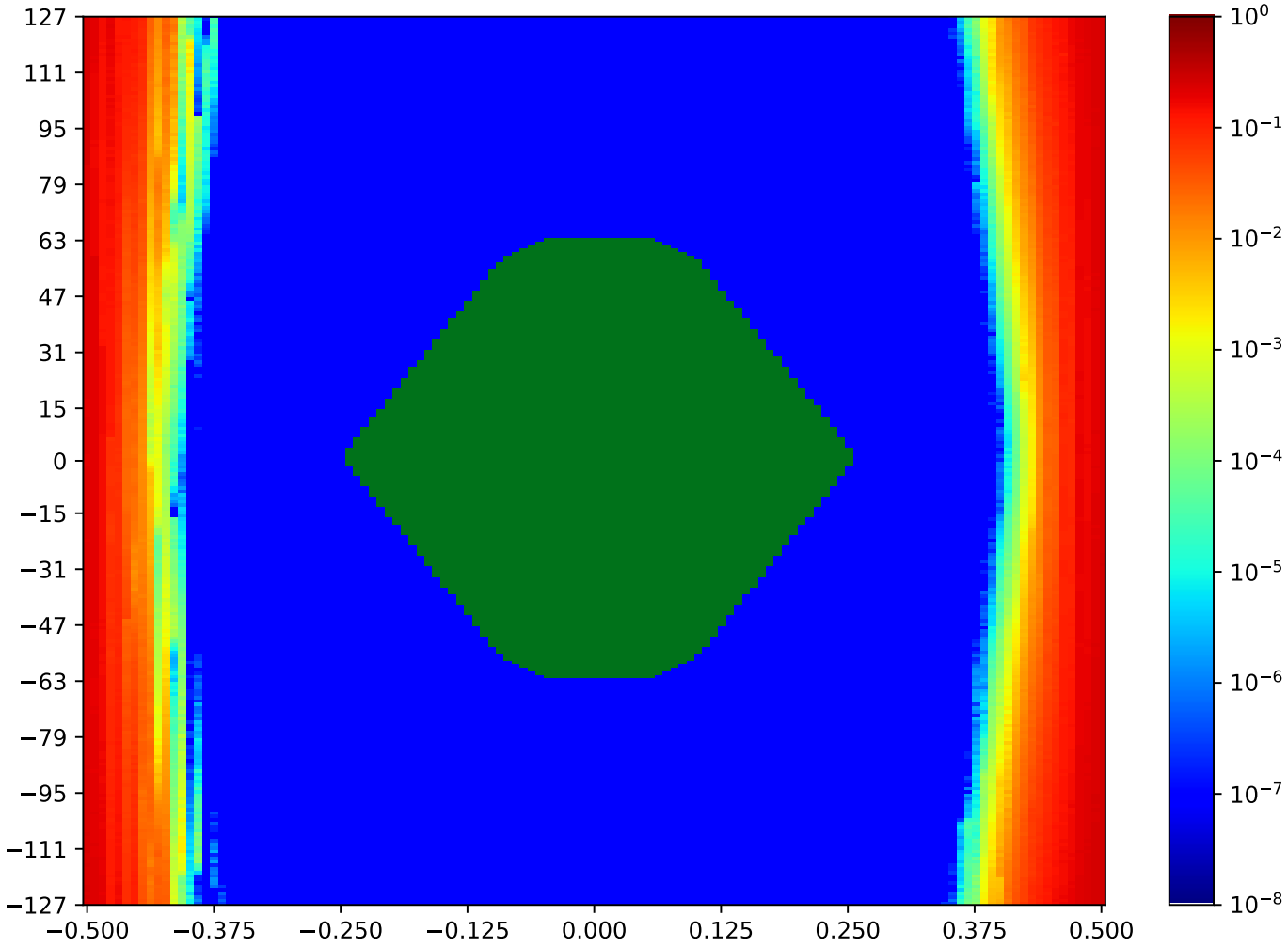


Figure 3.268: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.3 MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Table 3.248: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:46:44		2018-Sep-27 18:48:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24798	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

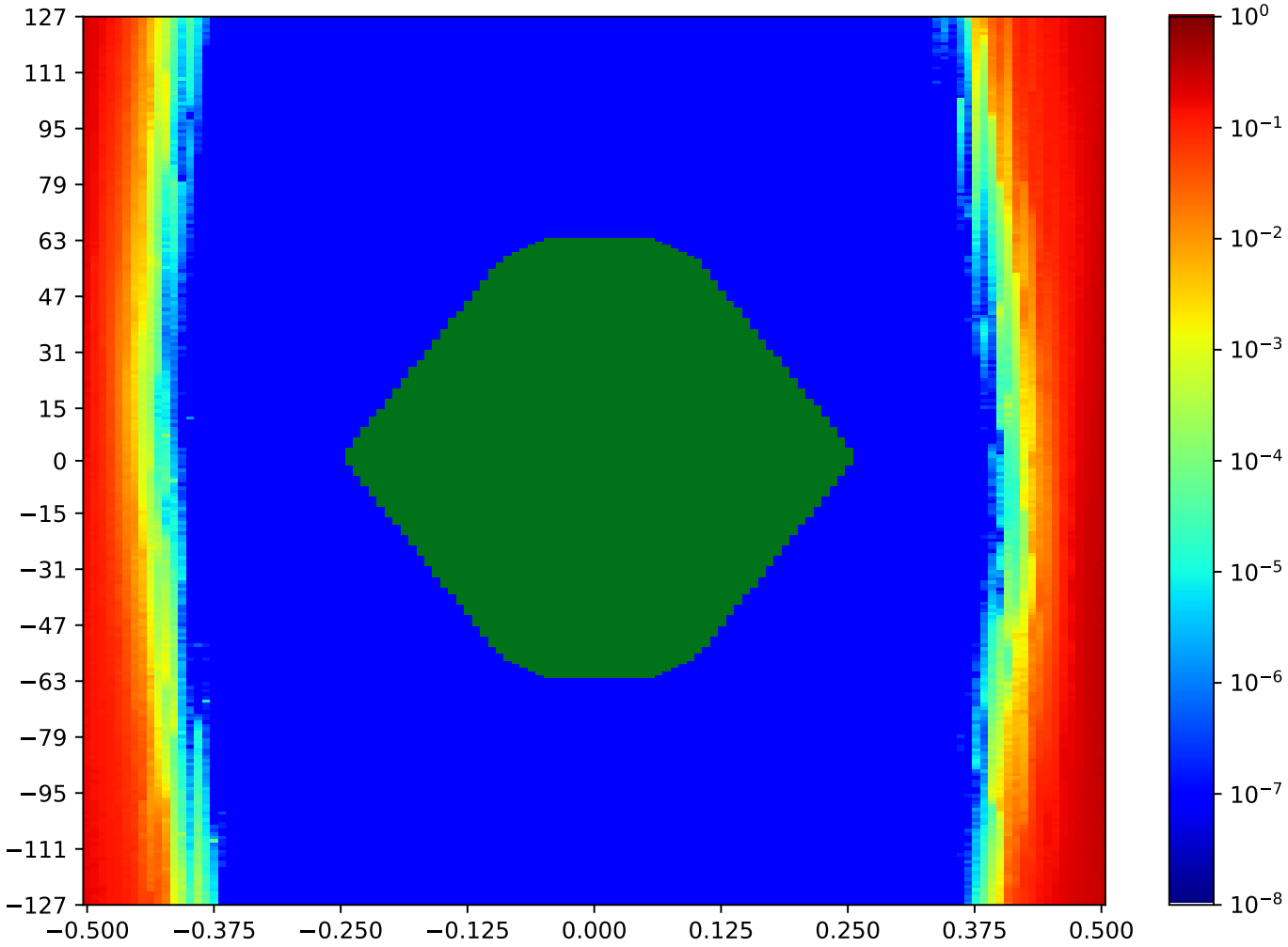


Figure 3.269: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.4 MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Table 3.249: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:40:26		2018-Sep-27 18:41:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24632	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

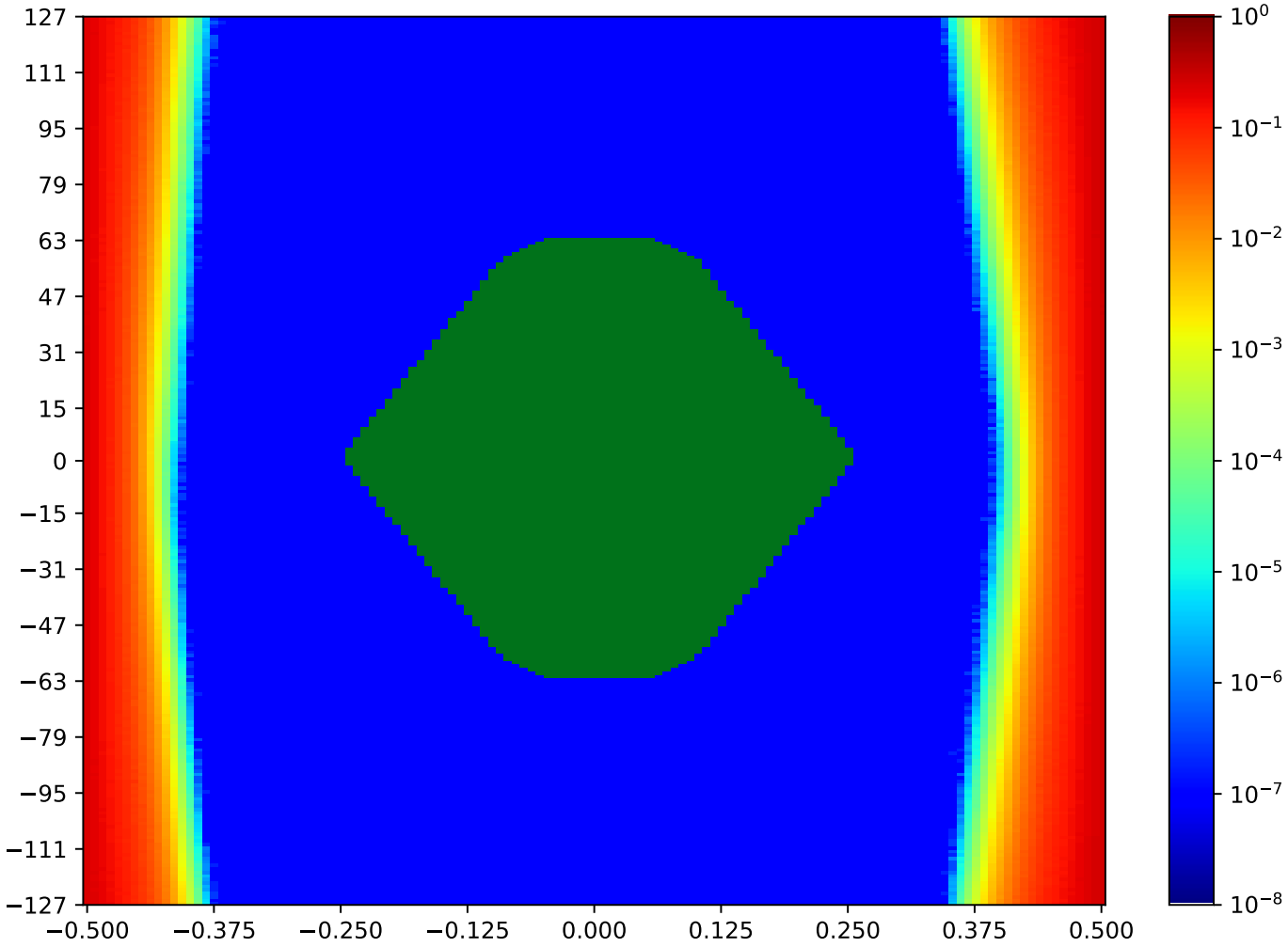


Figure 3.270: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.5 MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Table 3.250: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:50:31		2018-Sep-27 18:51:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24885	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

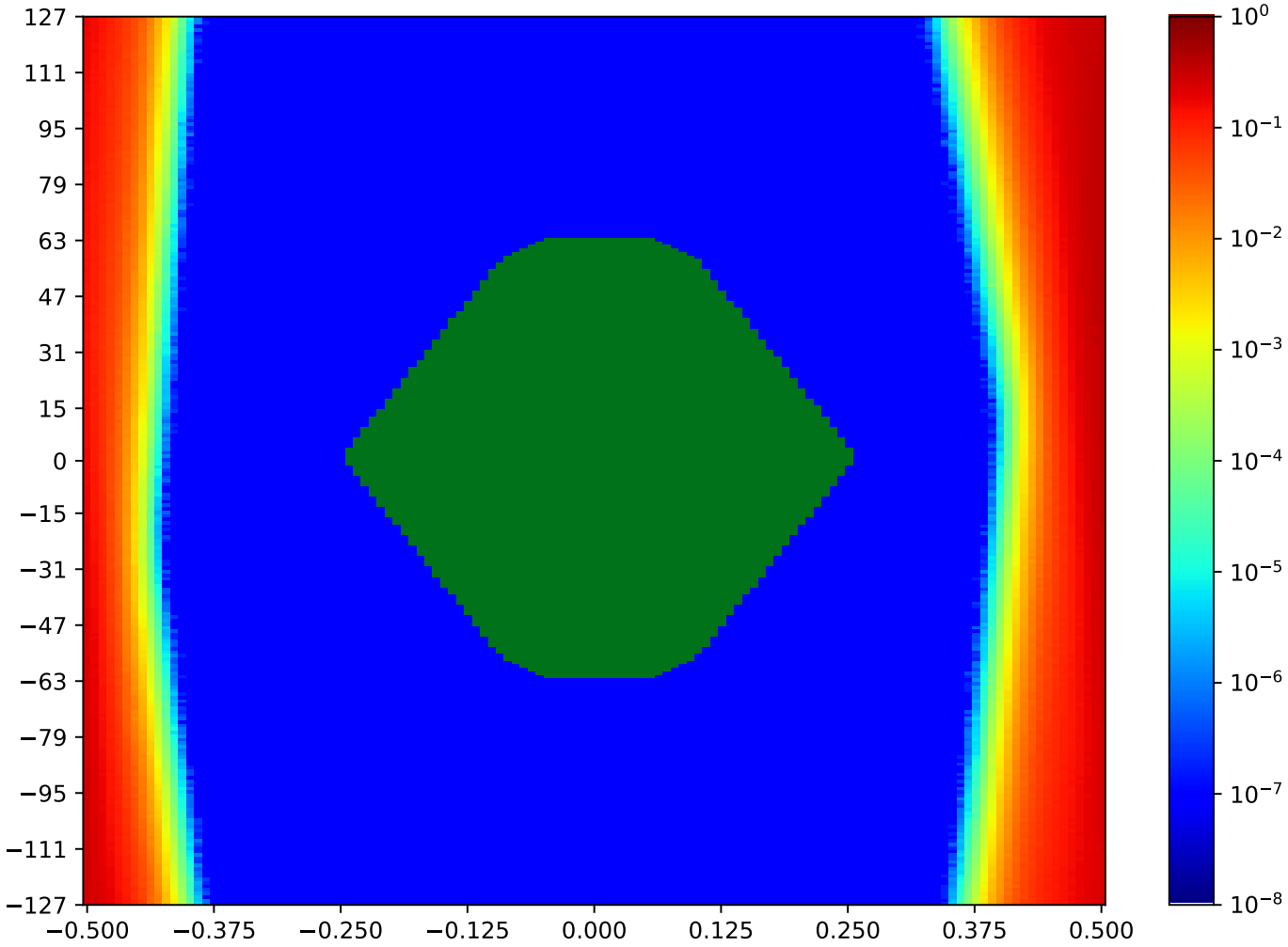


Figure 3.271: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.6 MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Table 3.251: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:39:10		2018-Sep-27 18:40:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24364	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

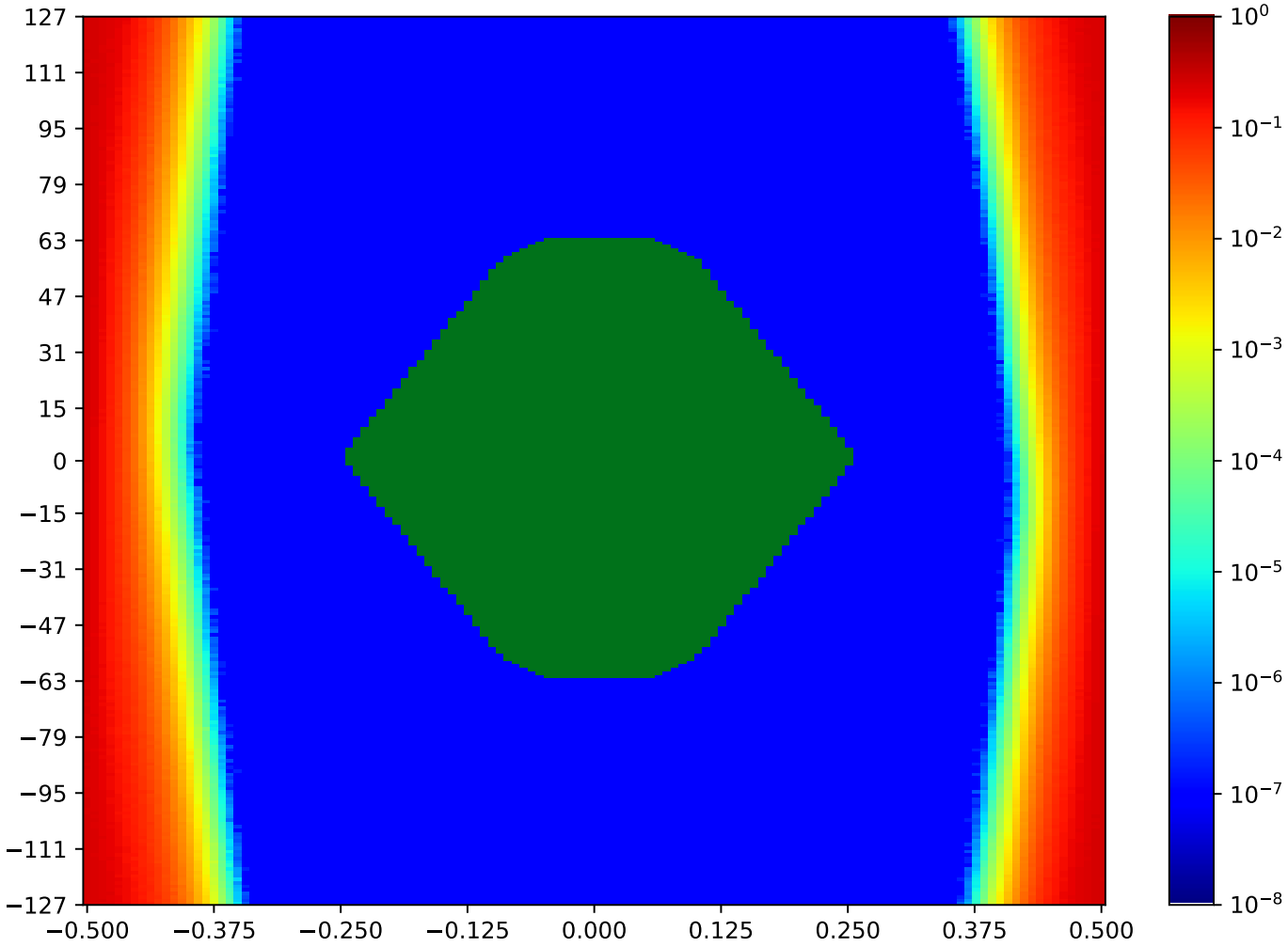


Figure 3.272: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.7 MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Table 3.252: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:53:03		2018-Sep-27 18:54:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24675	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

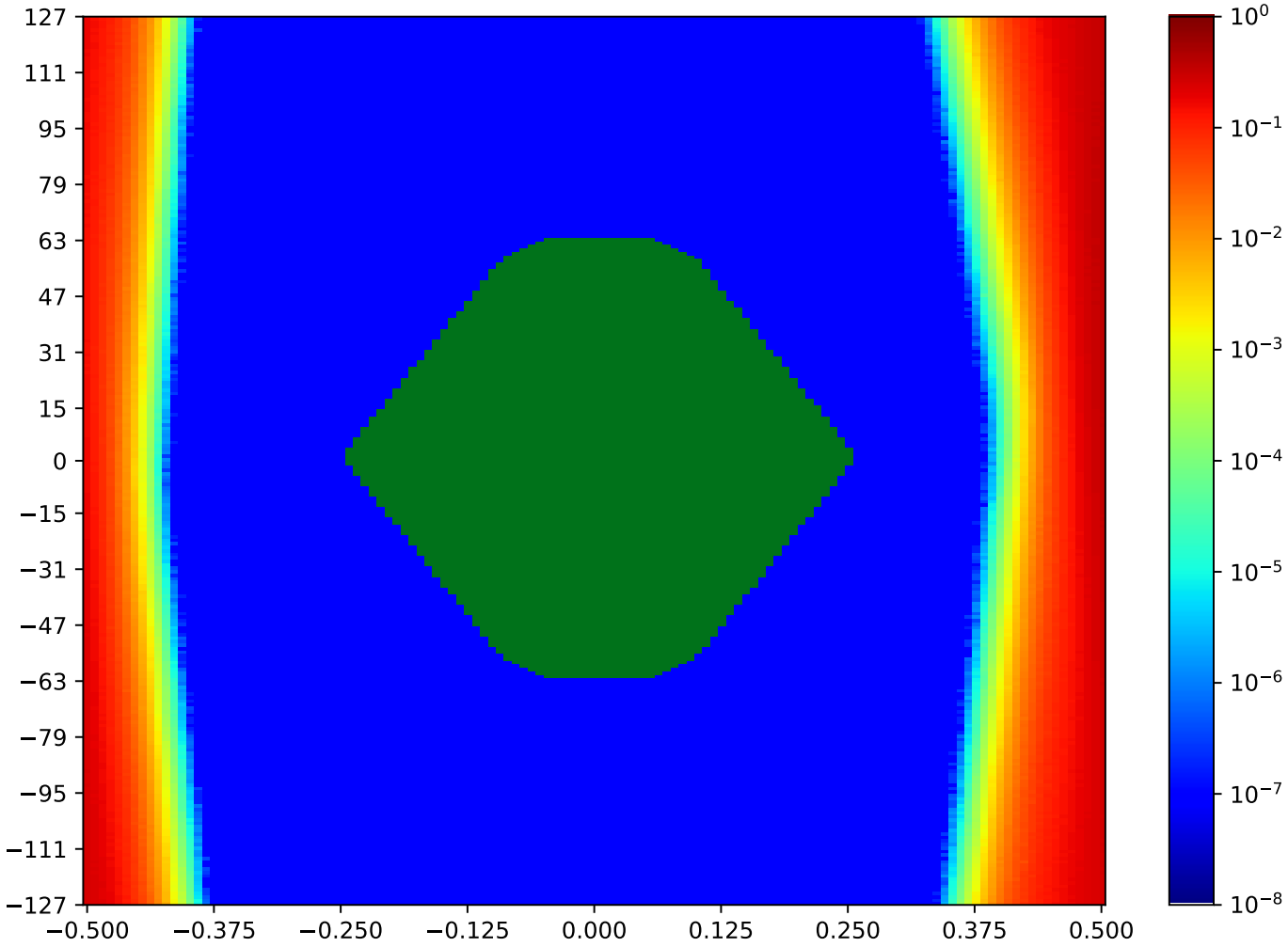


Figure 3.273: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.8 MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Table 3.253: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:41:41		2018-Sep-27 18:42:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24620	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

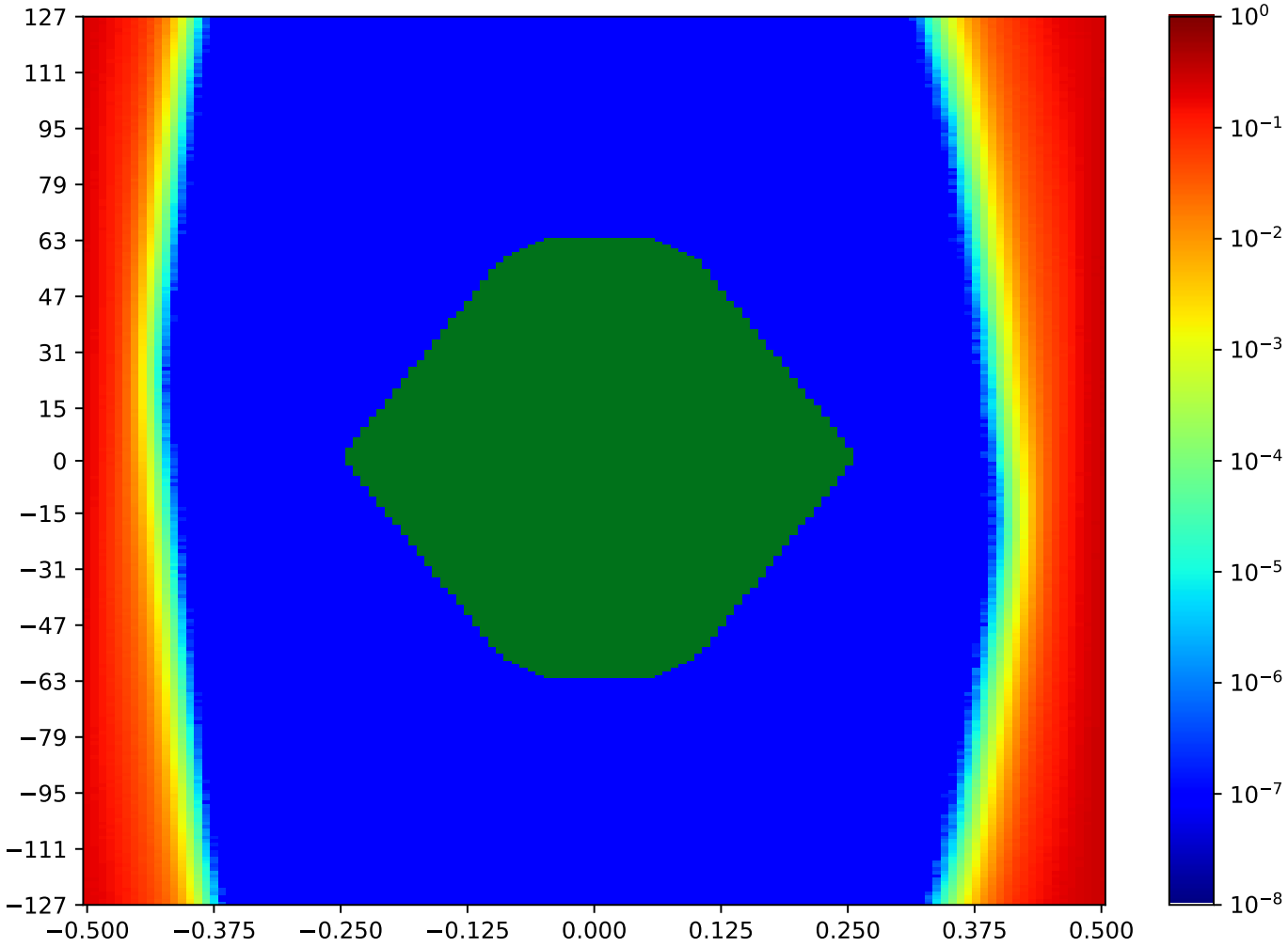


Figure 3.274: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.9 MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Table 3.254: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:51:47		2018-Sep-27 18:53:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25242	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

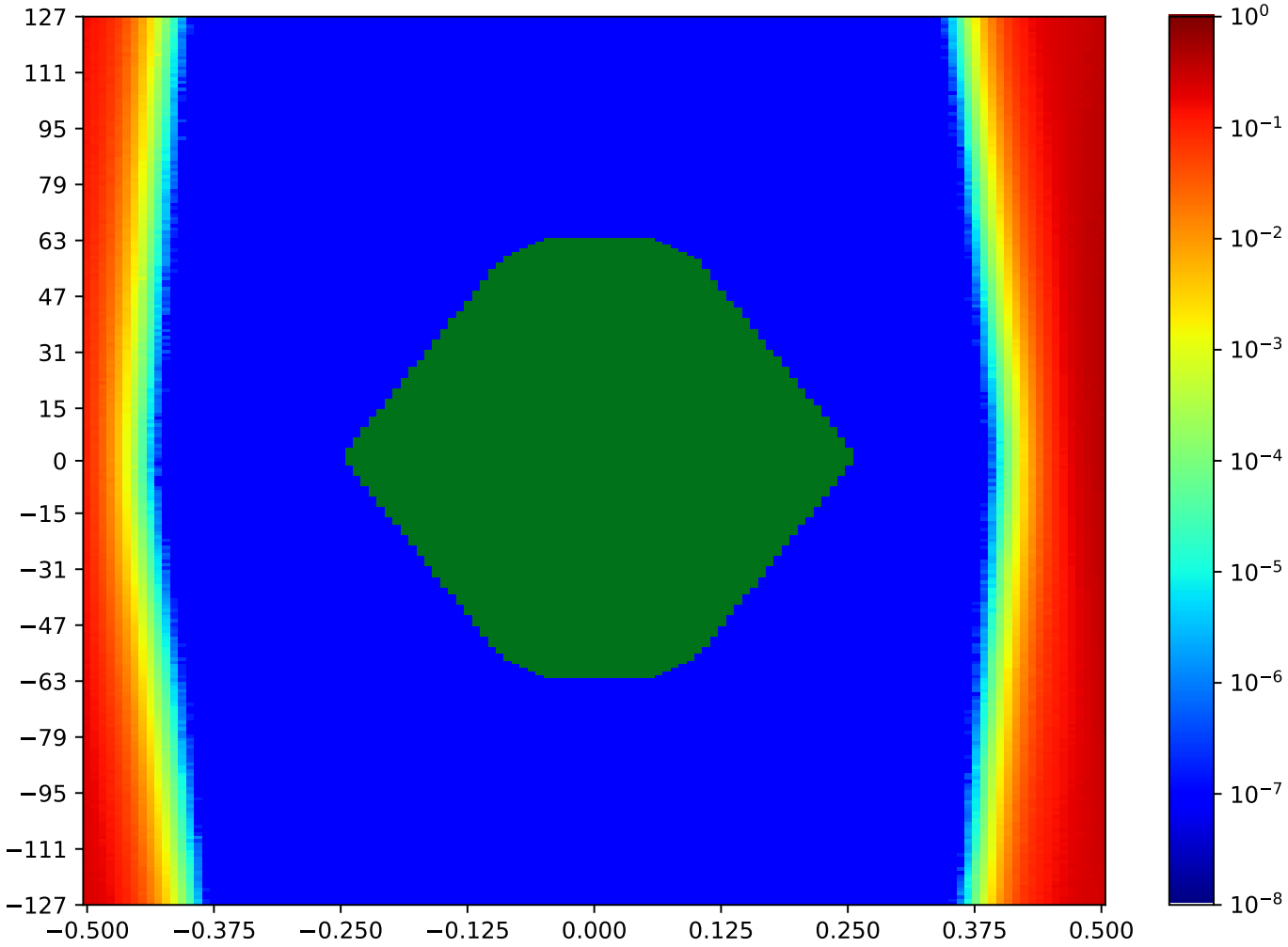


Figure 3.275: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.10 MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Table 3.255: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:44:12		2018-Sep-27 18:45:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24701	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

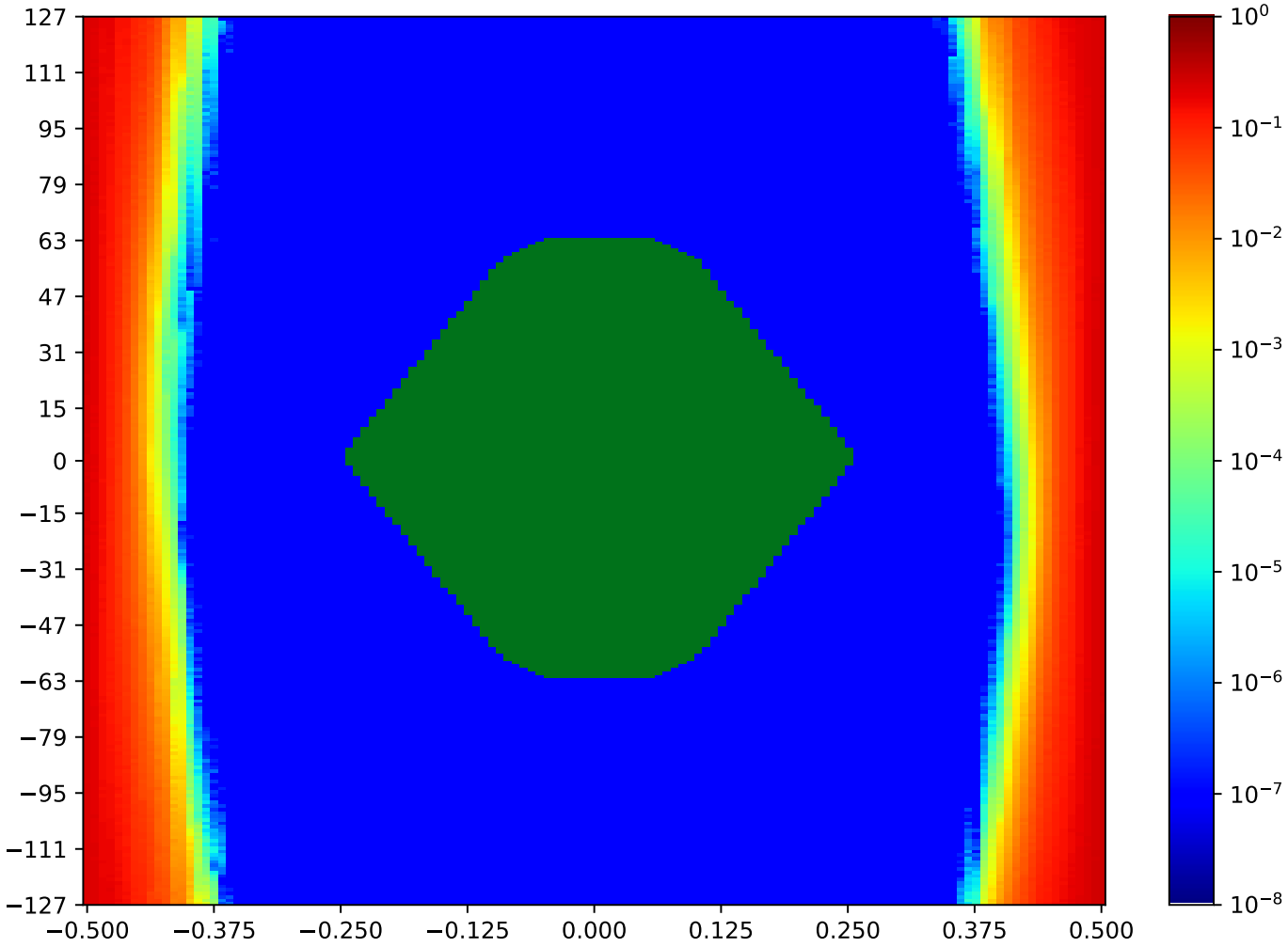


Figure 3.276: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.11 MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Table 3.256: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:49:15		2018-Sep-27 18:50:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25075	104	80.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

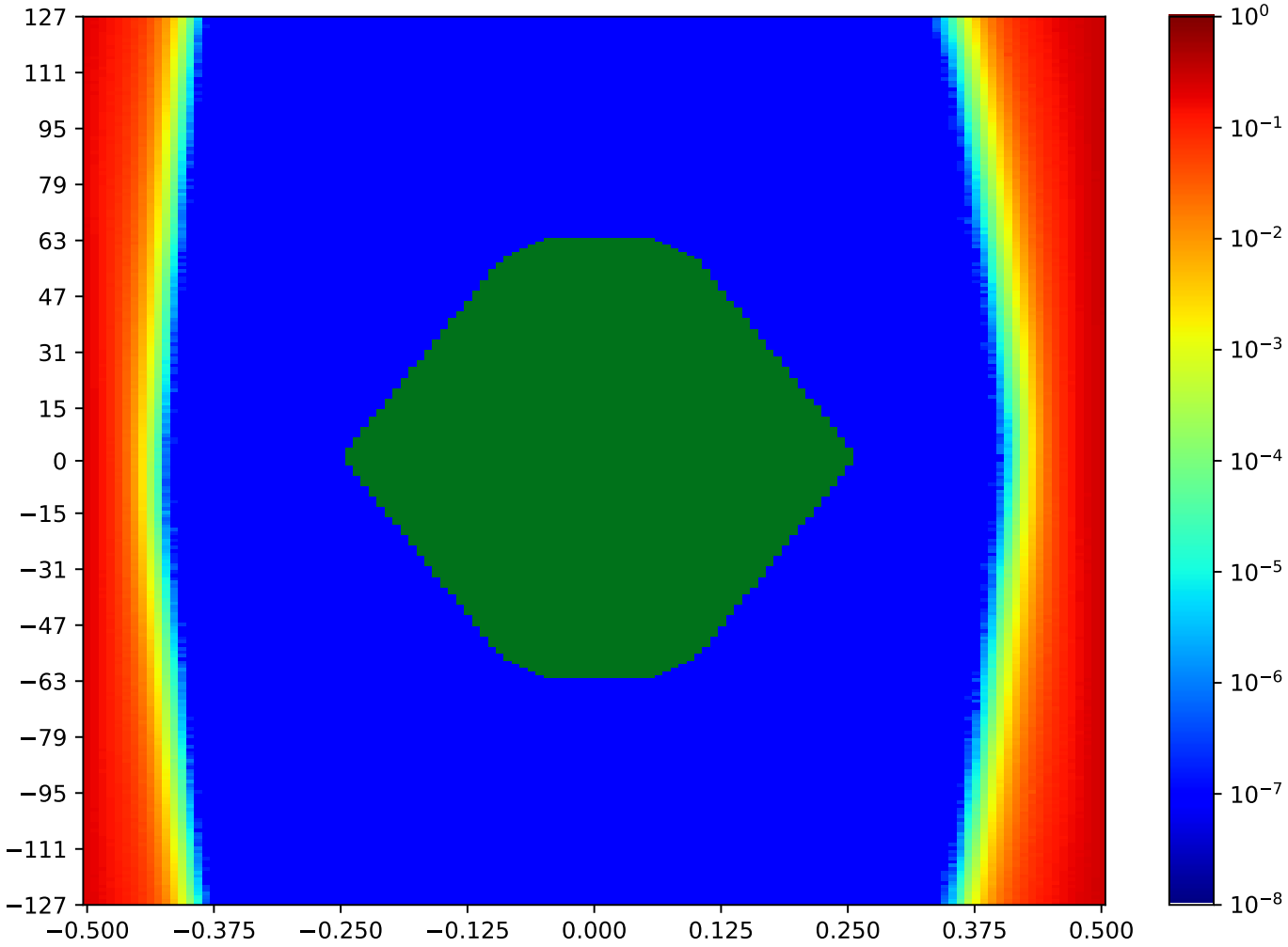


Figure 3.277: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.21.12 MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Table 3.257: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:48:00		2018-Sep-27 18:49:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24416	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

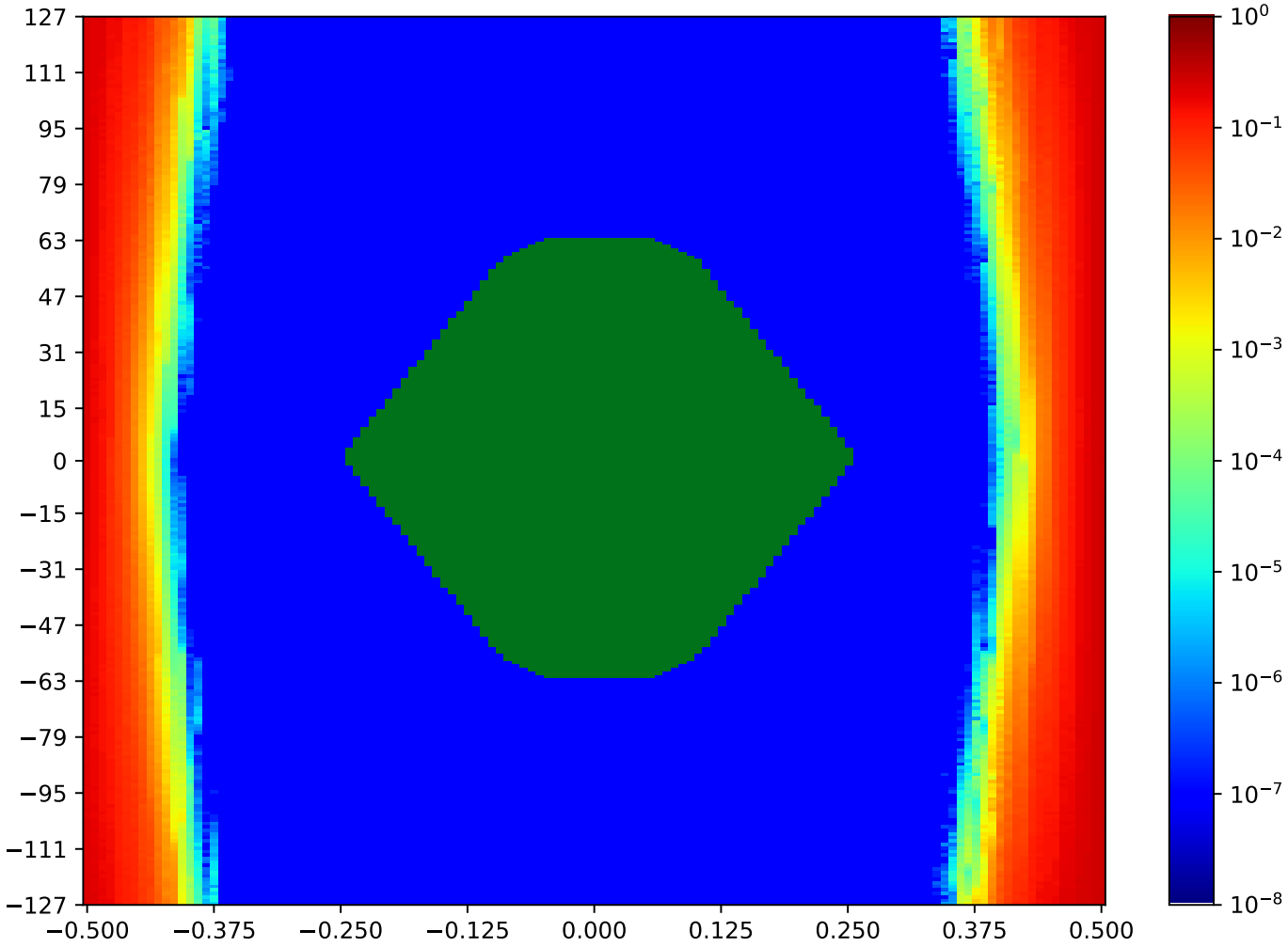


Figure 3.278: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22 MSP_C TX4 MSP_A RX4 Minipod Loopback

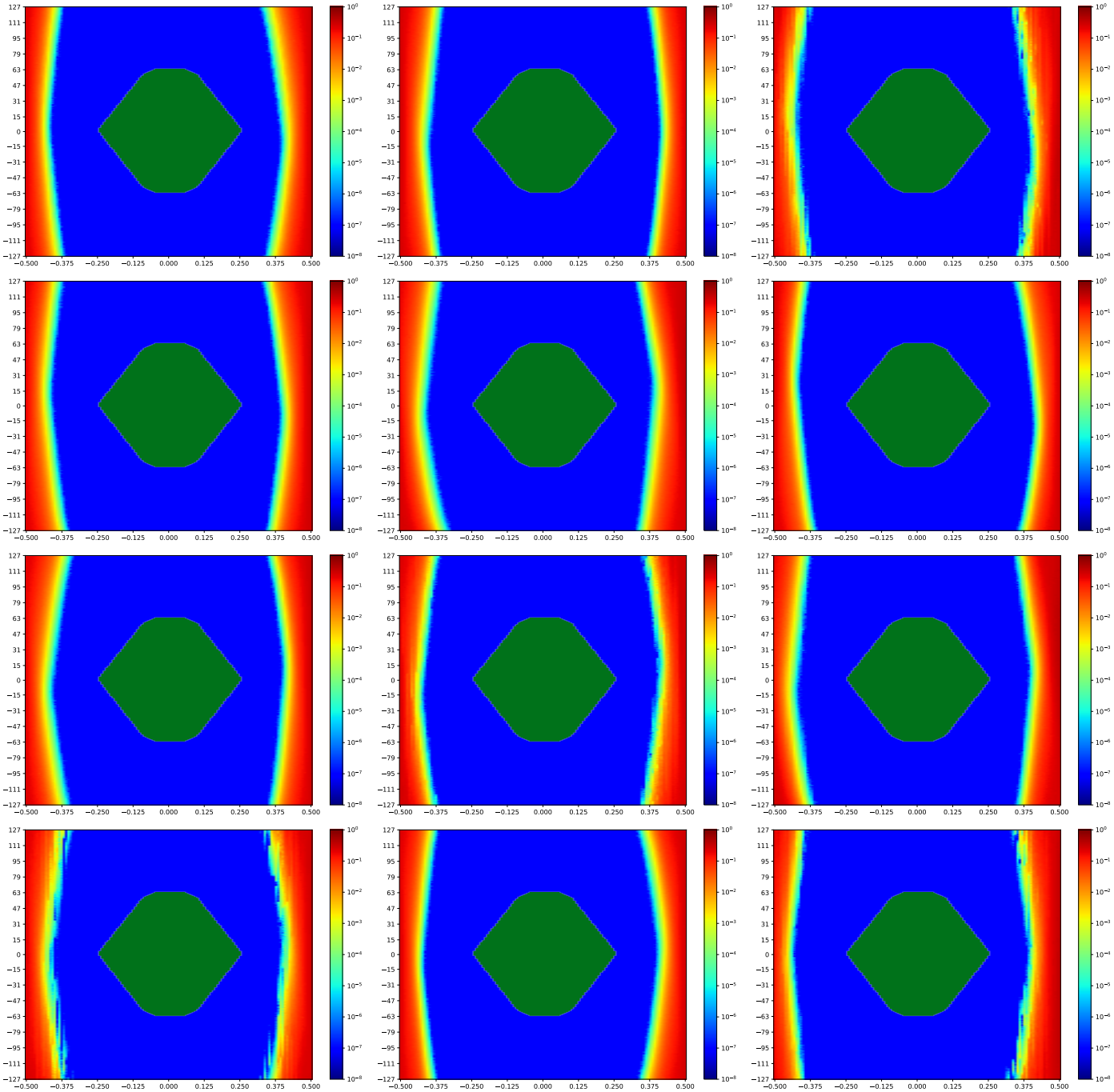


Figure 3.279: MSP_C TX4 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.
Next summary Figure 4.1.

3.22.1 MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Table 3.258: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:58:05		2018-Sep-27 18:59:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24288	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

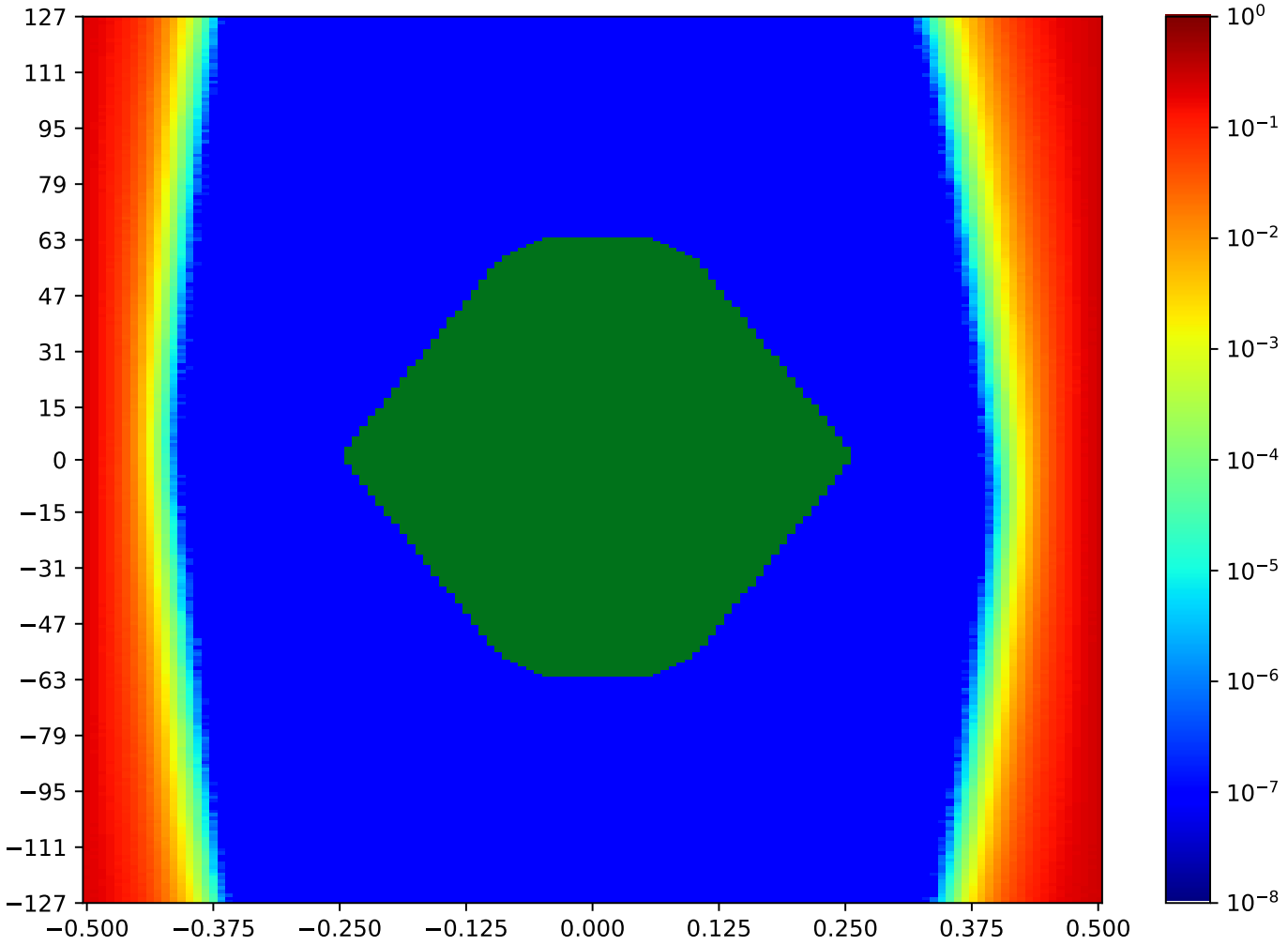


Figure 3.280: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.2 MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Table 3.259: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:55:34		2018-Sep-27 18:56:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24585	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

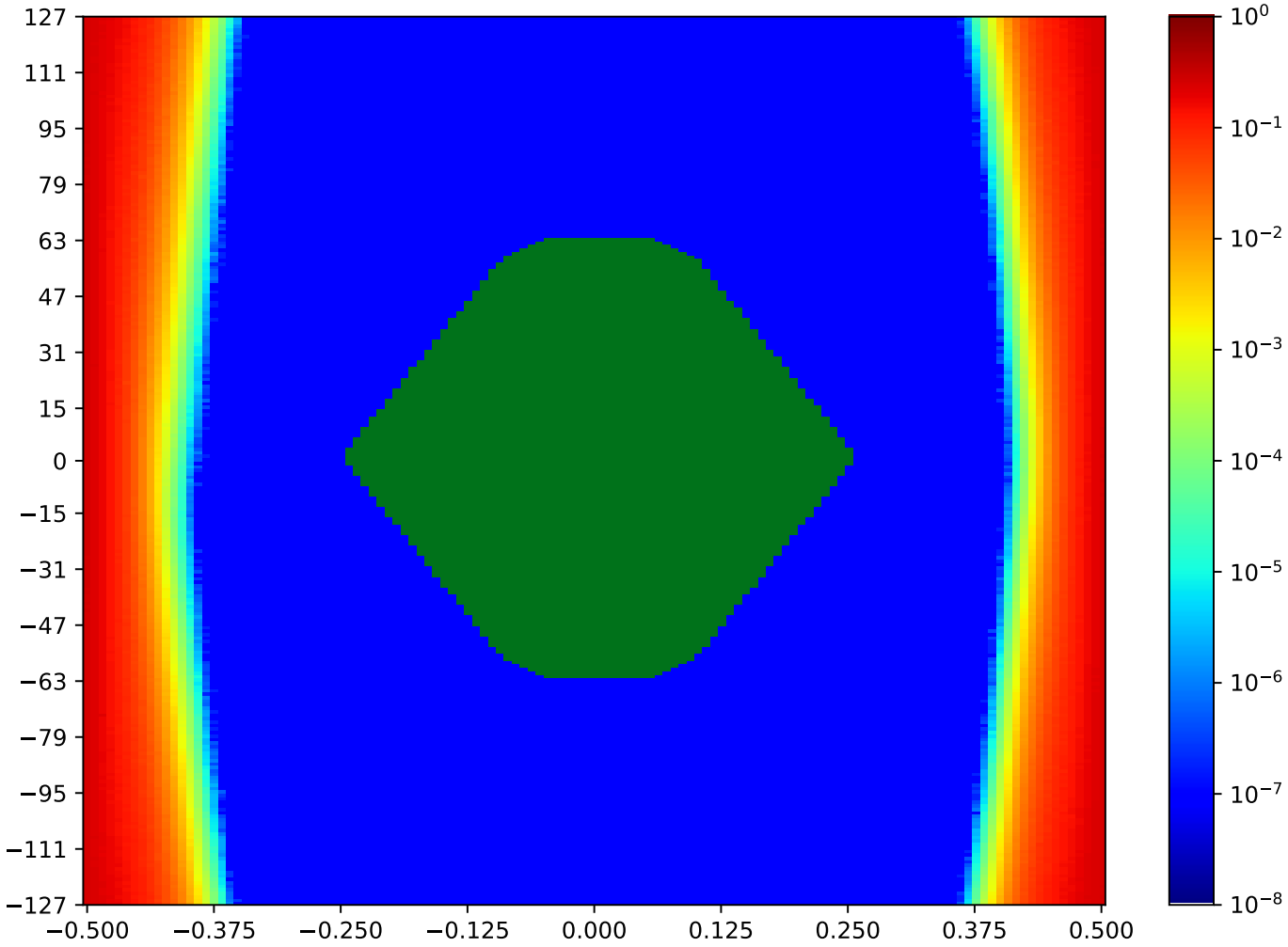


Figure 3.281: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.3 MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Table 3.260: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:01:51		2018-Sep-27 19:03:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24527	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

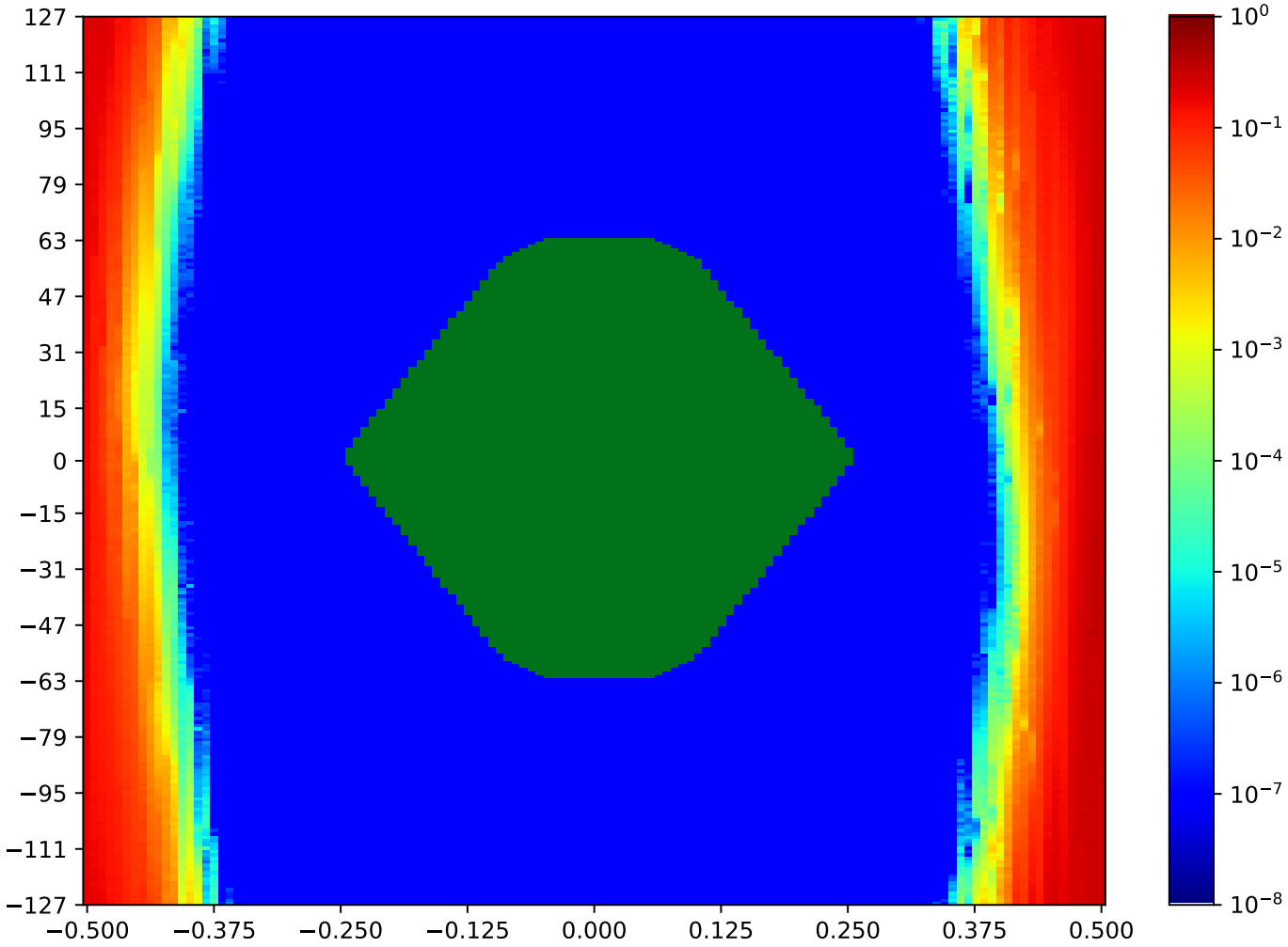


Figure 3.282: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.4 MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Table 3.261: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:54:18		2018-Sep-27 18:55:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24128	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

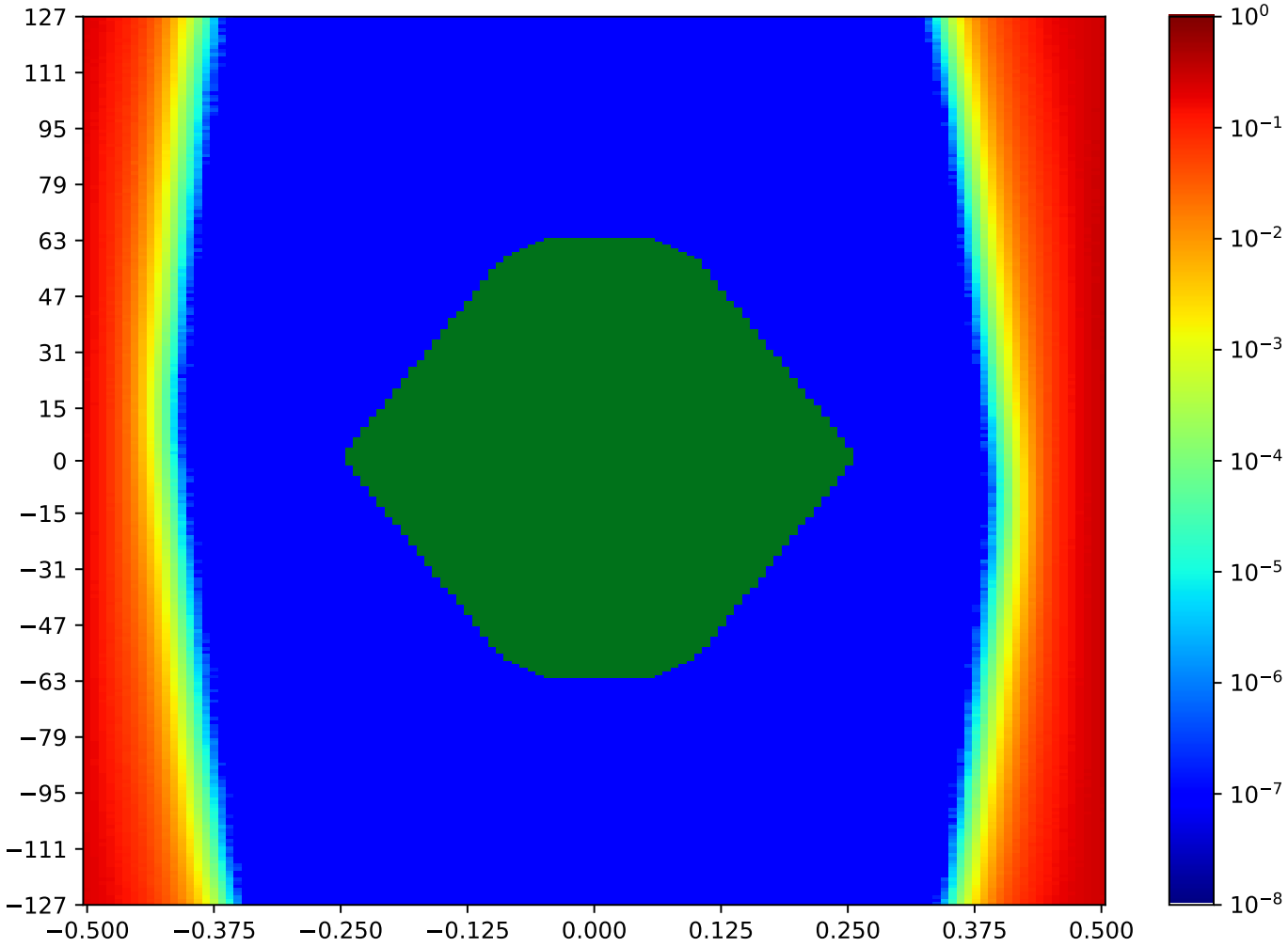


Figure 3.283: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.5 MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Table 3.262: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:05:38		2018-Sep-27 19:06:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23389	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

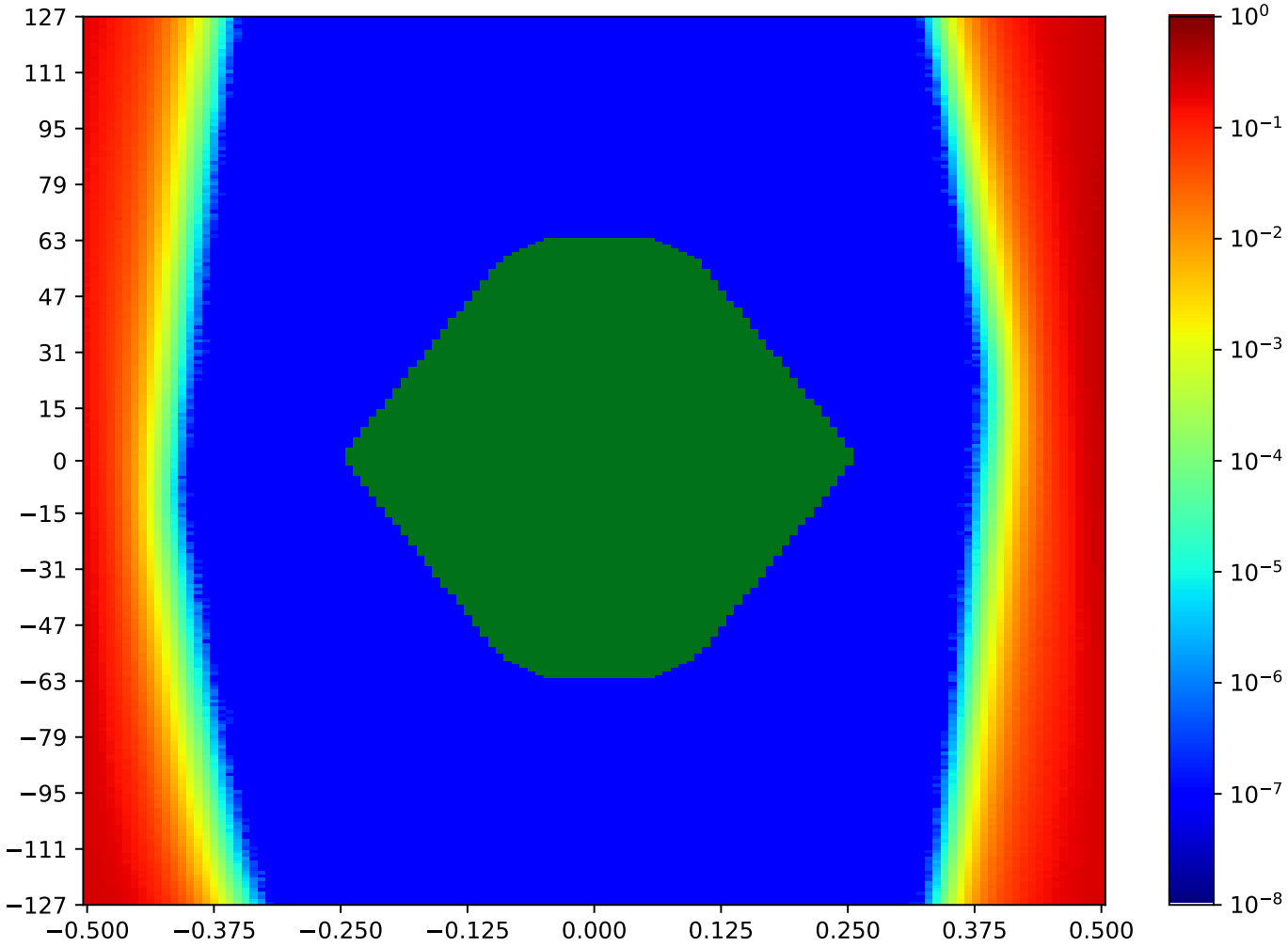


Figure 3.284: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.6 MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Table 3.263: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:56:49		2018-Sep-27 18:58:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24784	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

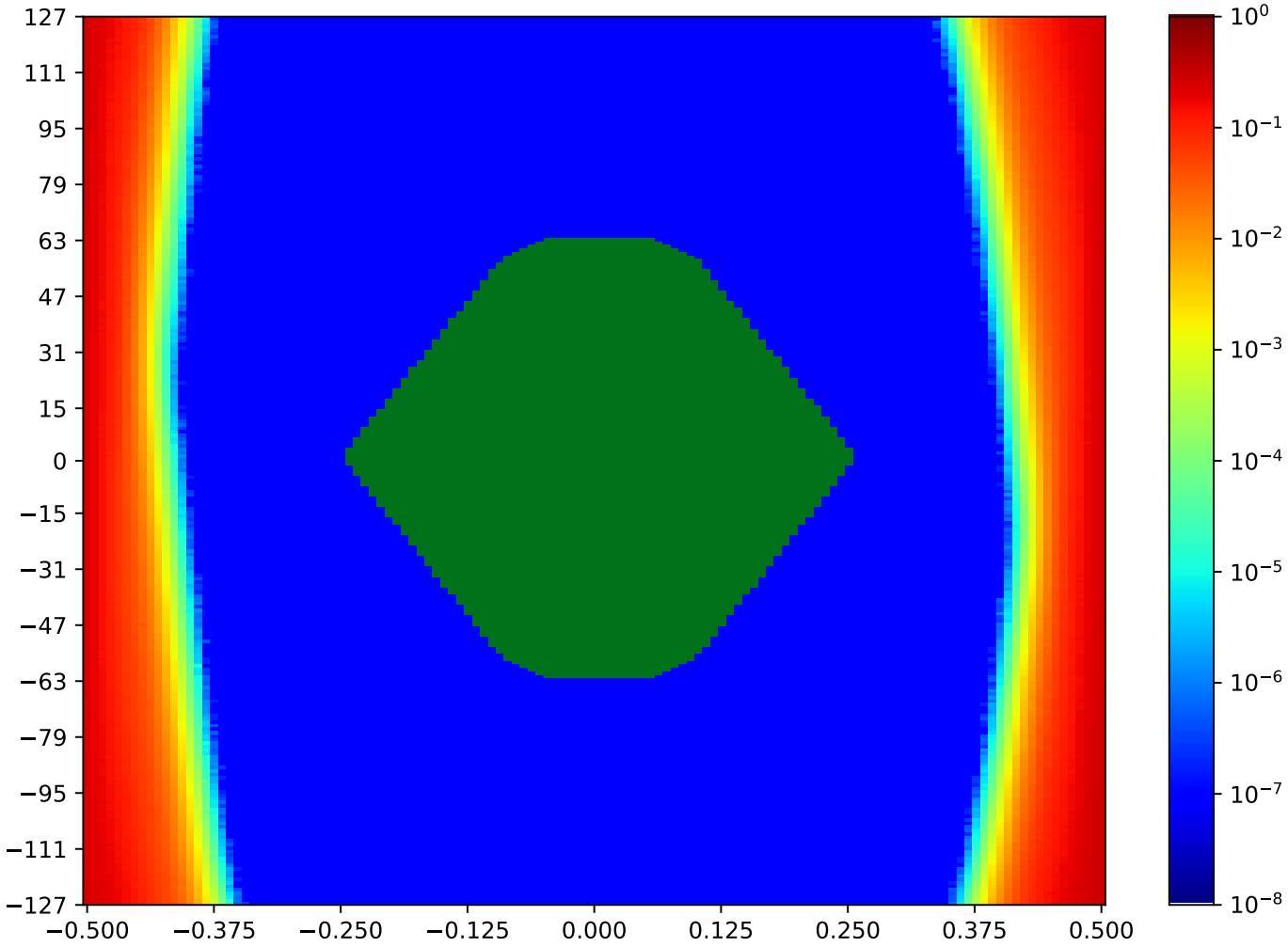


Figure 3.285: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.7 MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Table 3.264: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:08:08		2018-Sep-27 19:09:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24107	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

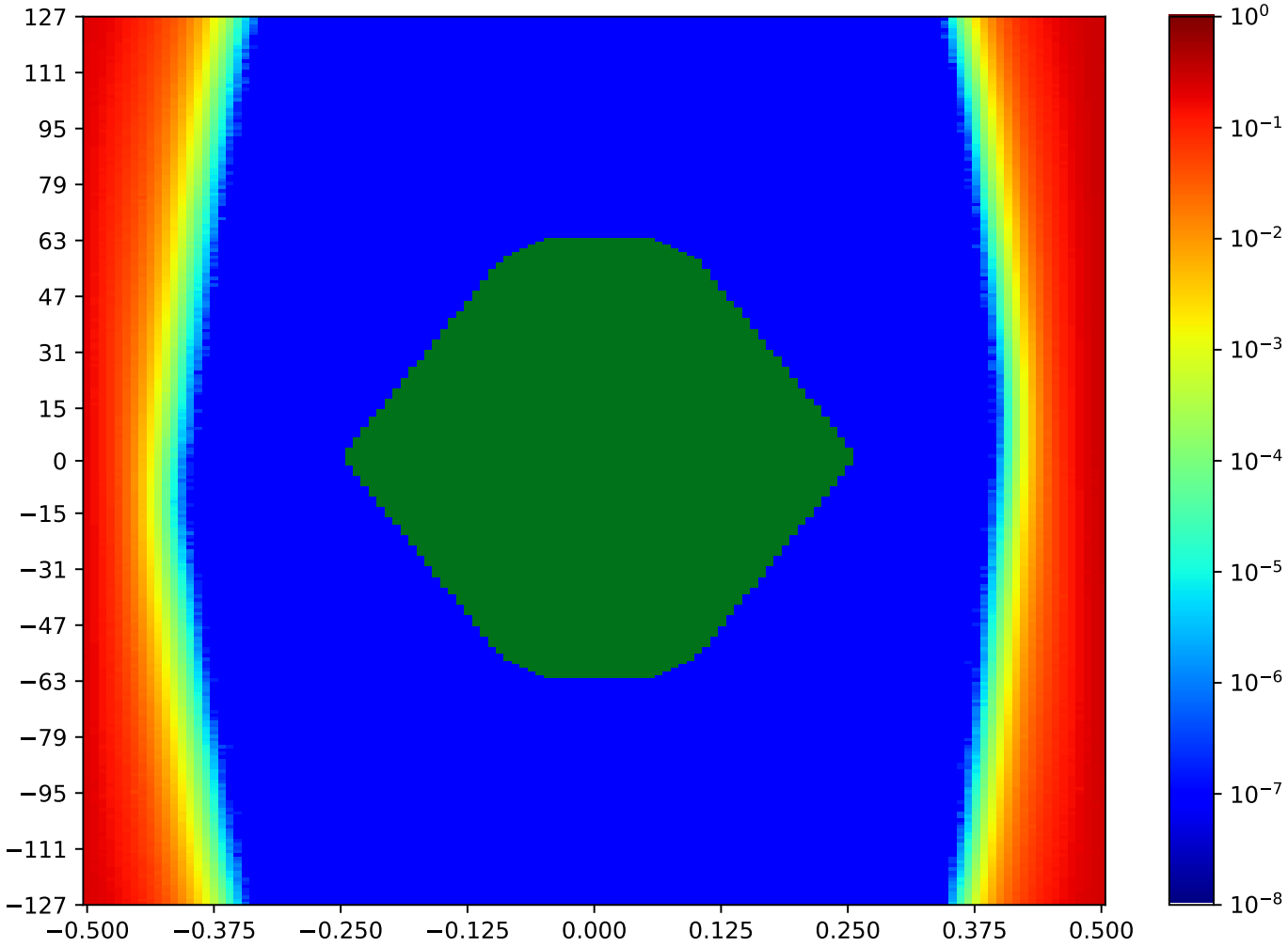


Figure 3.286: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.8 MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Table 3.265: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:59:21		2018-Sep-27 19:00:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24772	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

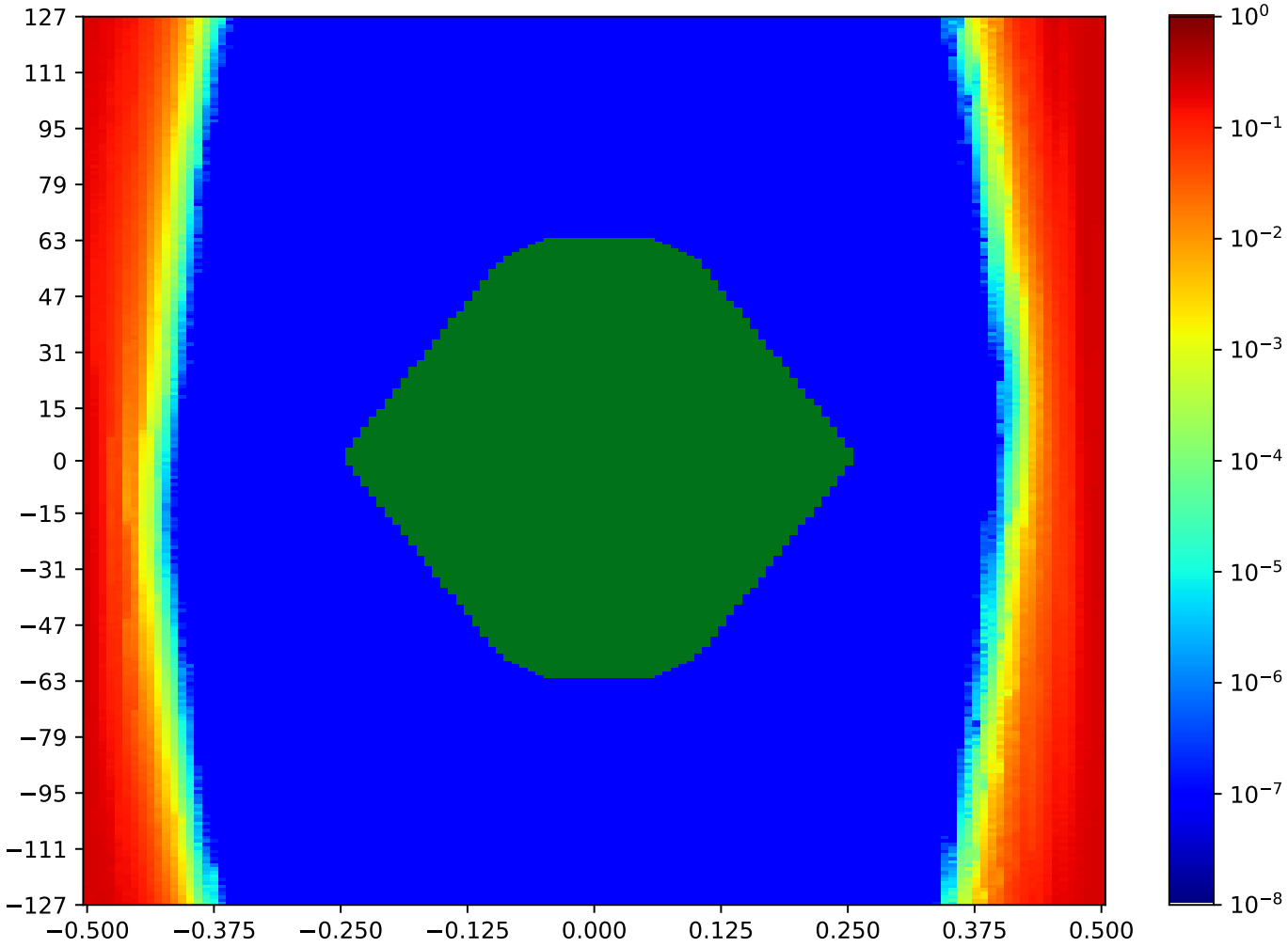


Figure 3.287: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.9 MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Table 3.266: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:06:53		2018-Sep-27 19:08:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24423	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

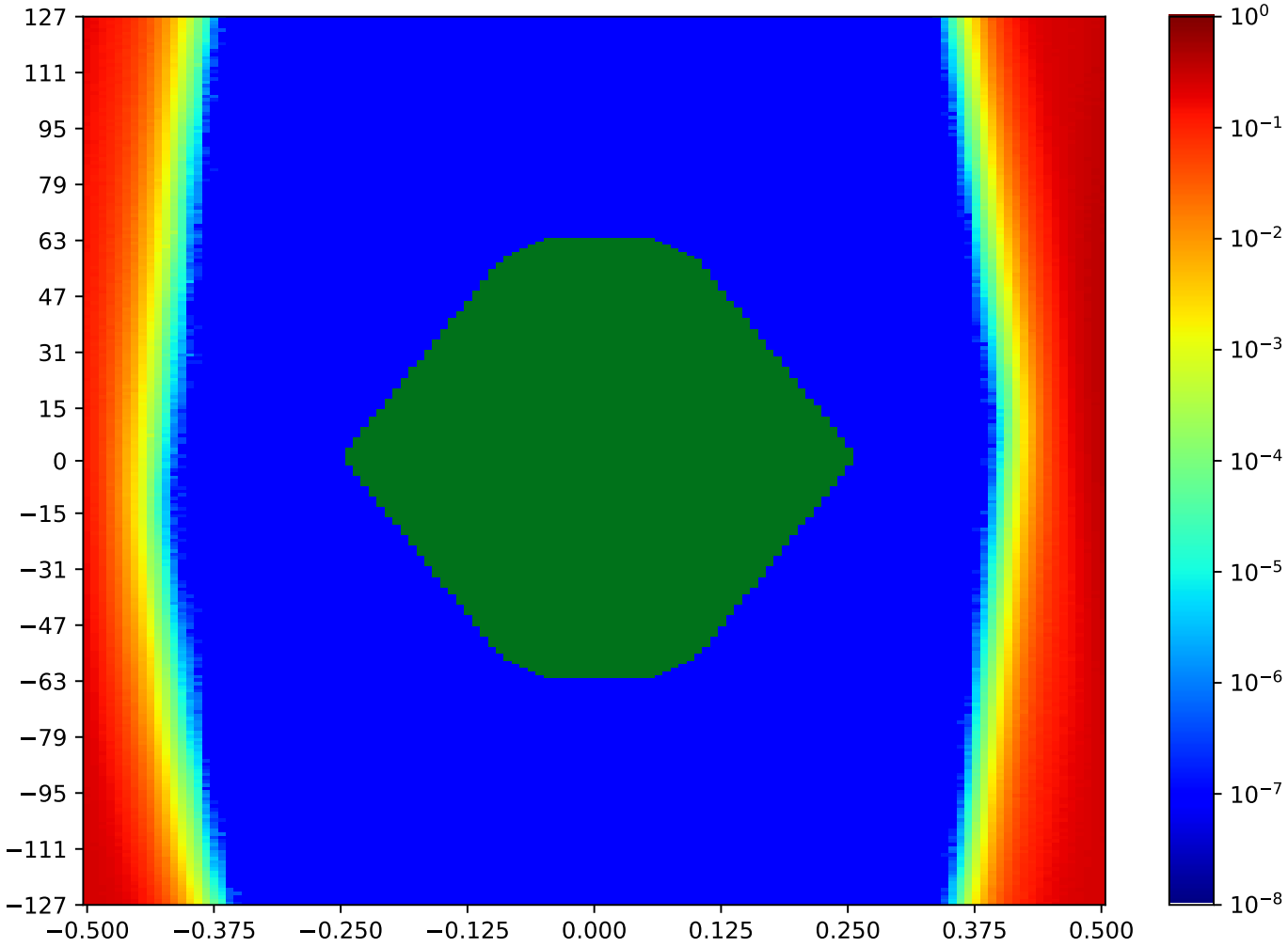


Figure 3.288: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.10 MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Table 3.267: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:00:37		2018-Sep-27 19:01:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23984	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

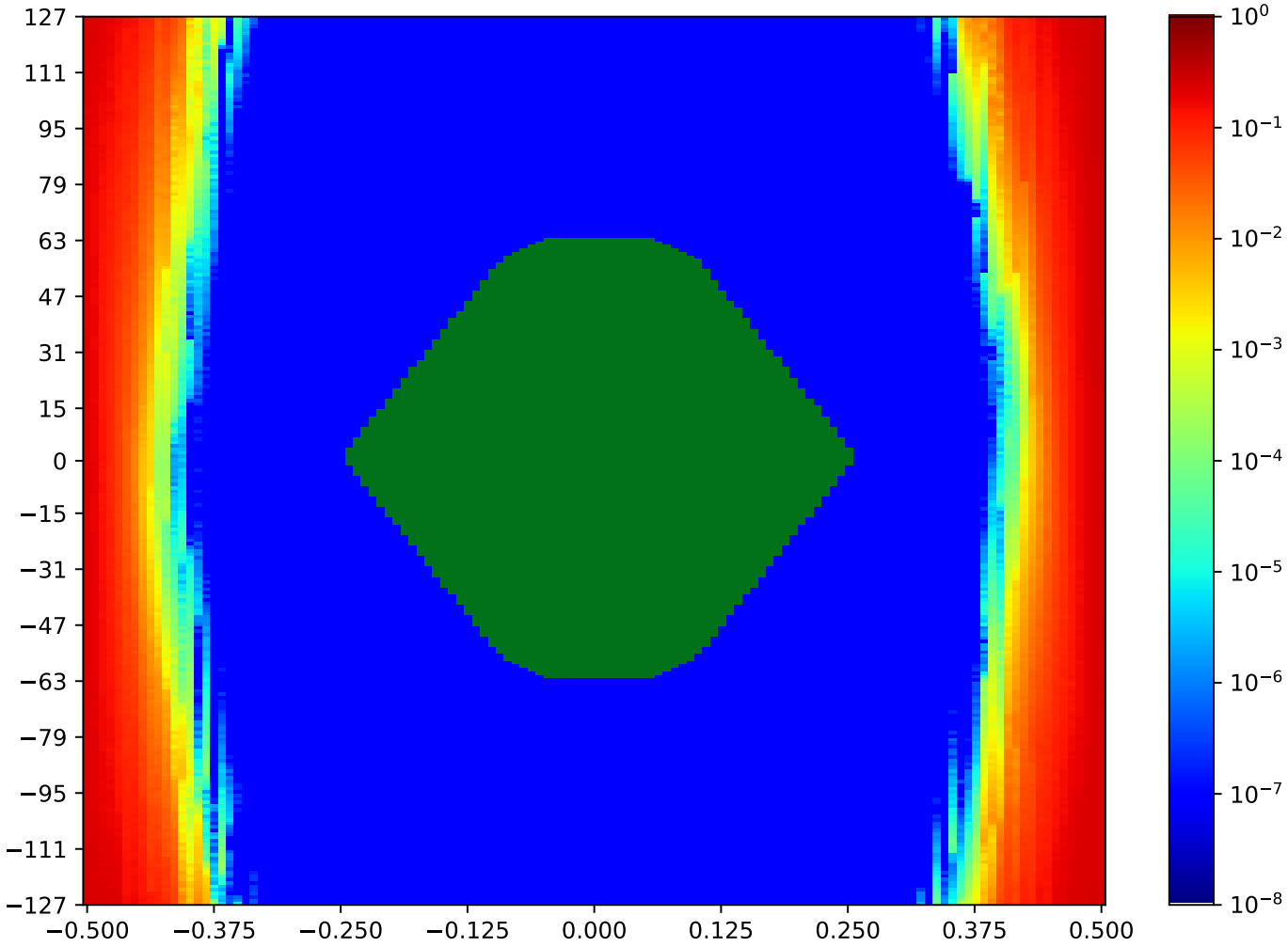


Figure 3.289: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.11 MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Table 3.268: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:04:22		2018-Sep-27 19:05:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24618	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

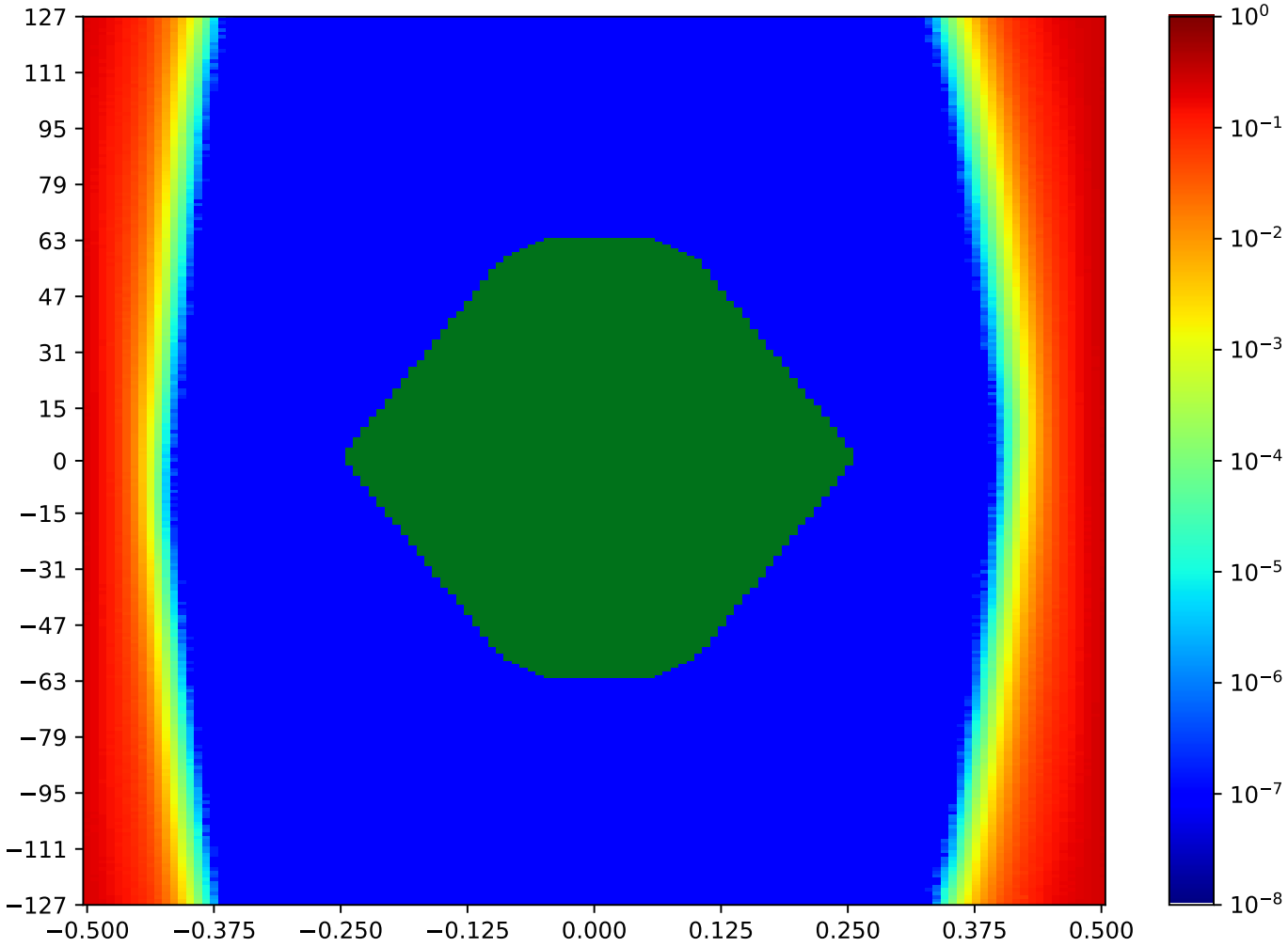


Figure 3.290: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

3.22.12 MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Table 3.269: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:03:07		2018-Sep-27 19:04:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24829	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

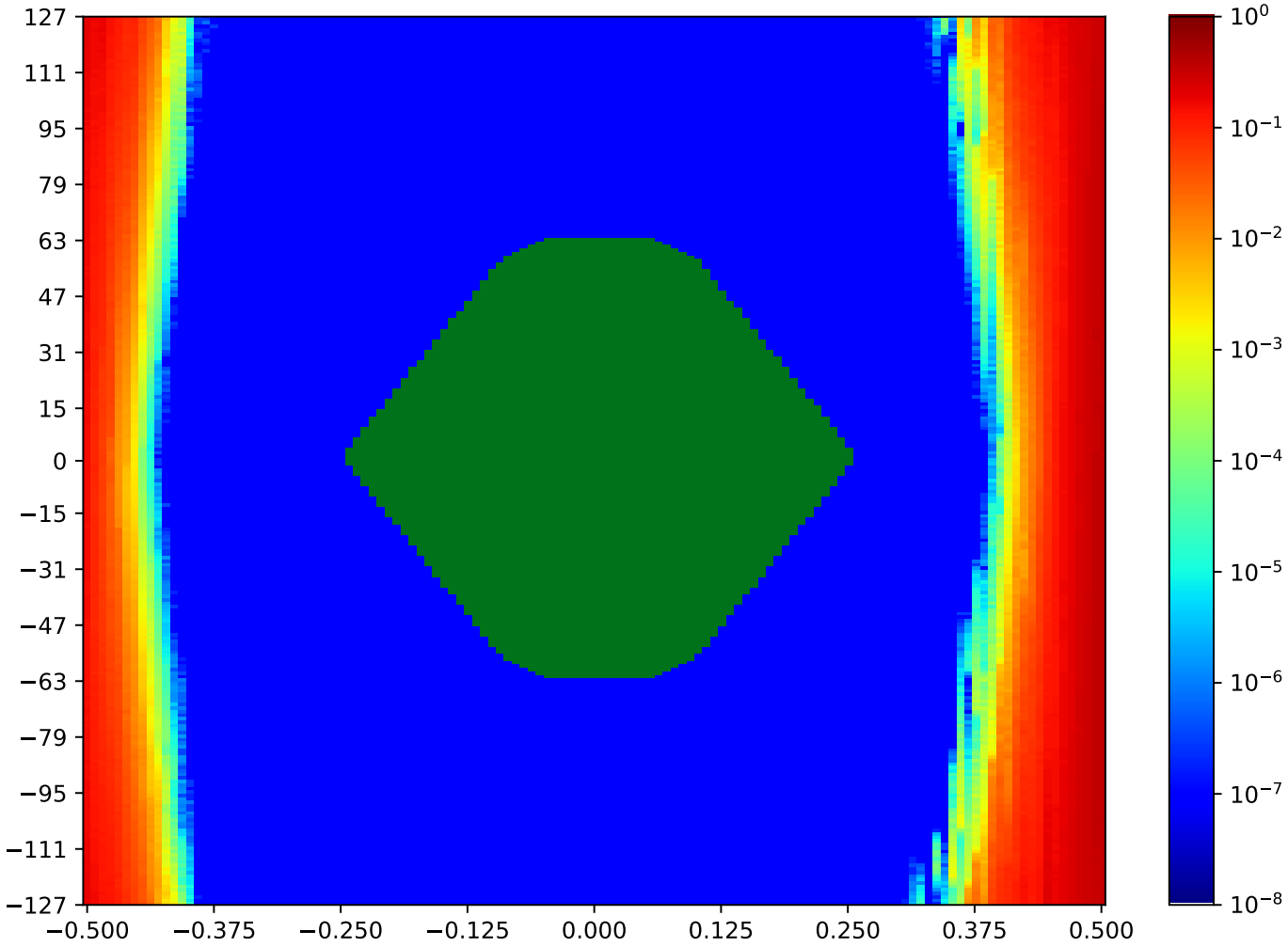


Figure 3.291: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V2-12.8, V3-6.4, V3-12.8.

Chapter 4

MUCTPI V2 12.8 Gbps

4.1 MSP_A TX1 MSP_C RX15 Minipod Loopback

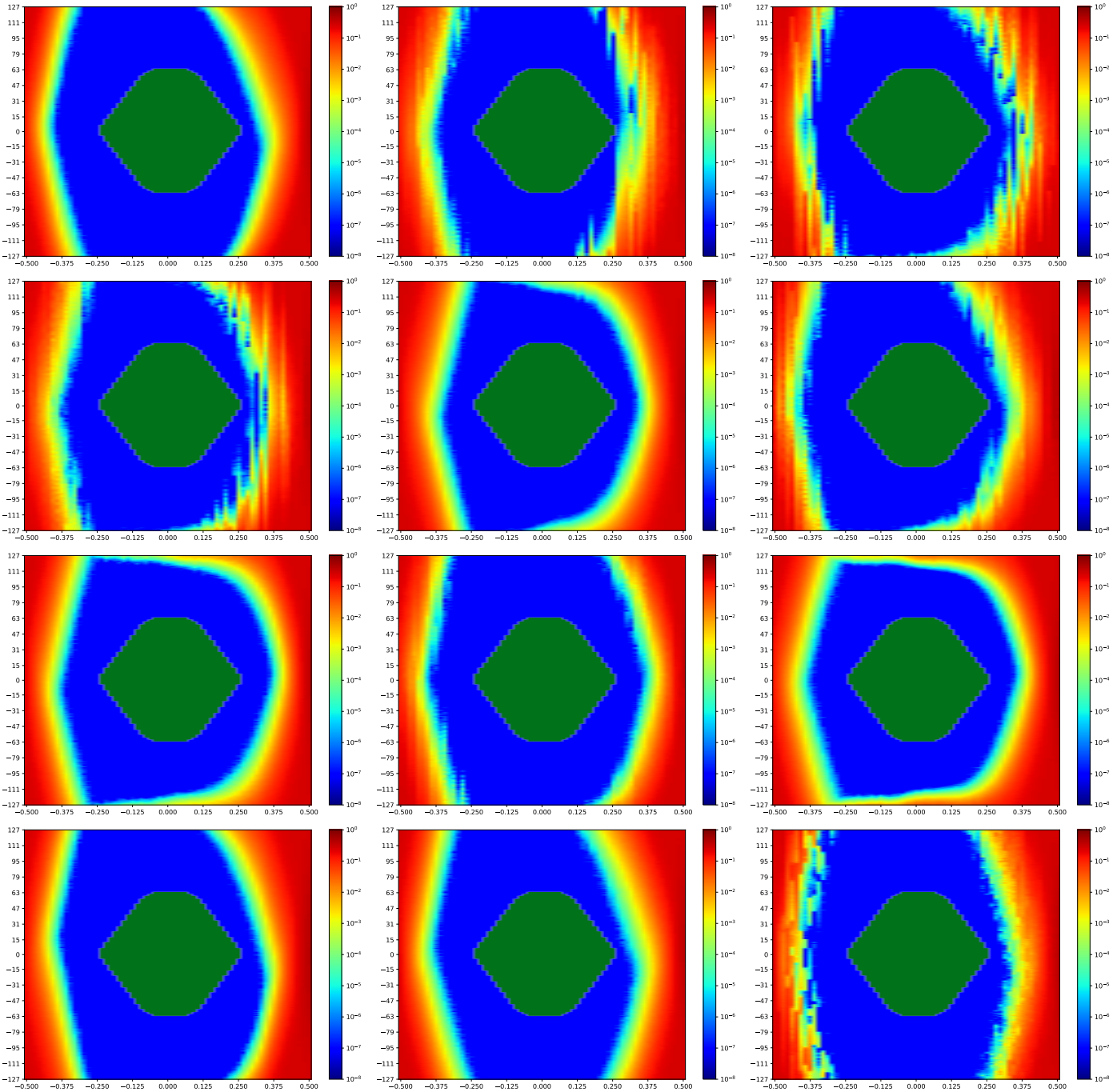


Figure 4.1: MSP_A TX1 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.14.

4.1.1 MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Table 4.1: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:45:40		2018-Sep-27 16:46:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9522	44	67.69%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

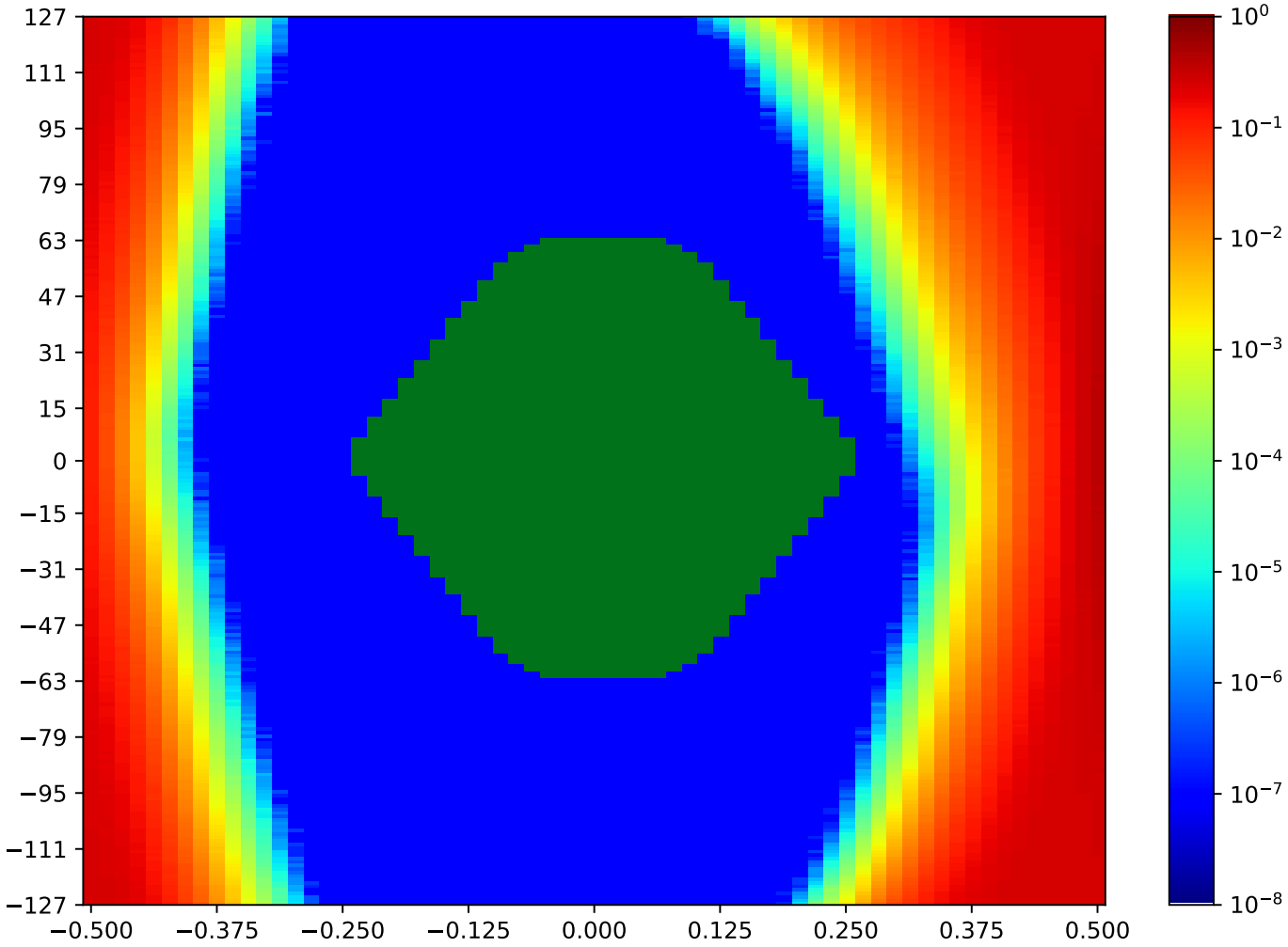


Figure 4.2: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.2 MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Table 4.2: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:46:21		2018-Sep-27 16:46:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8715	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

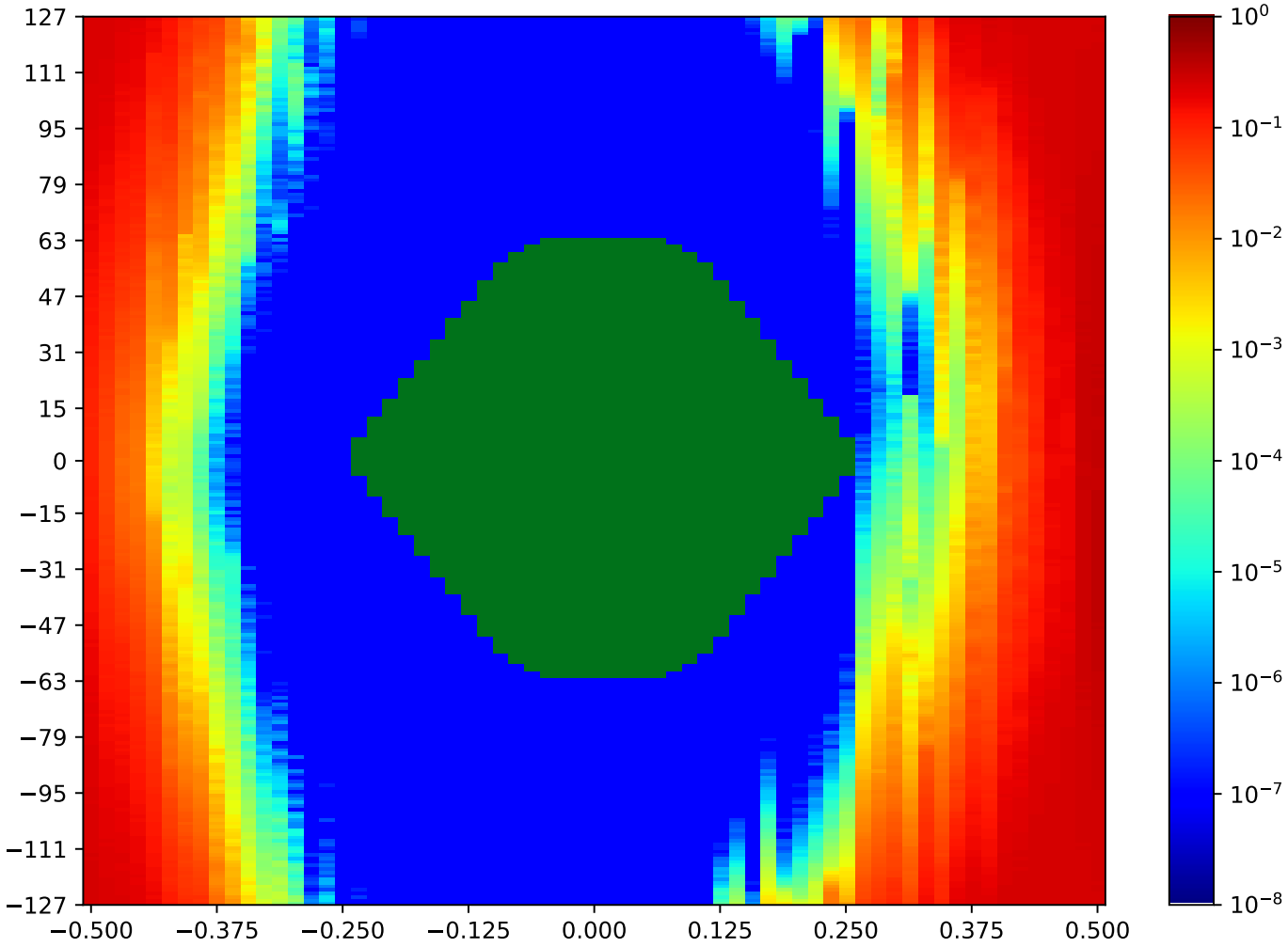


Figure 4.3: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.3 MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Table 4.3: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:46:42		2018-Sep-27 16:47:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8889	45	67.69%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

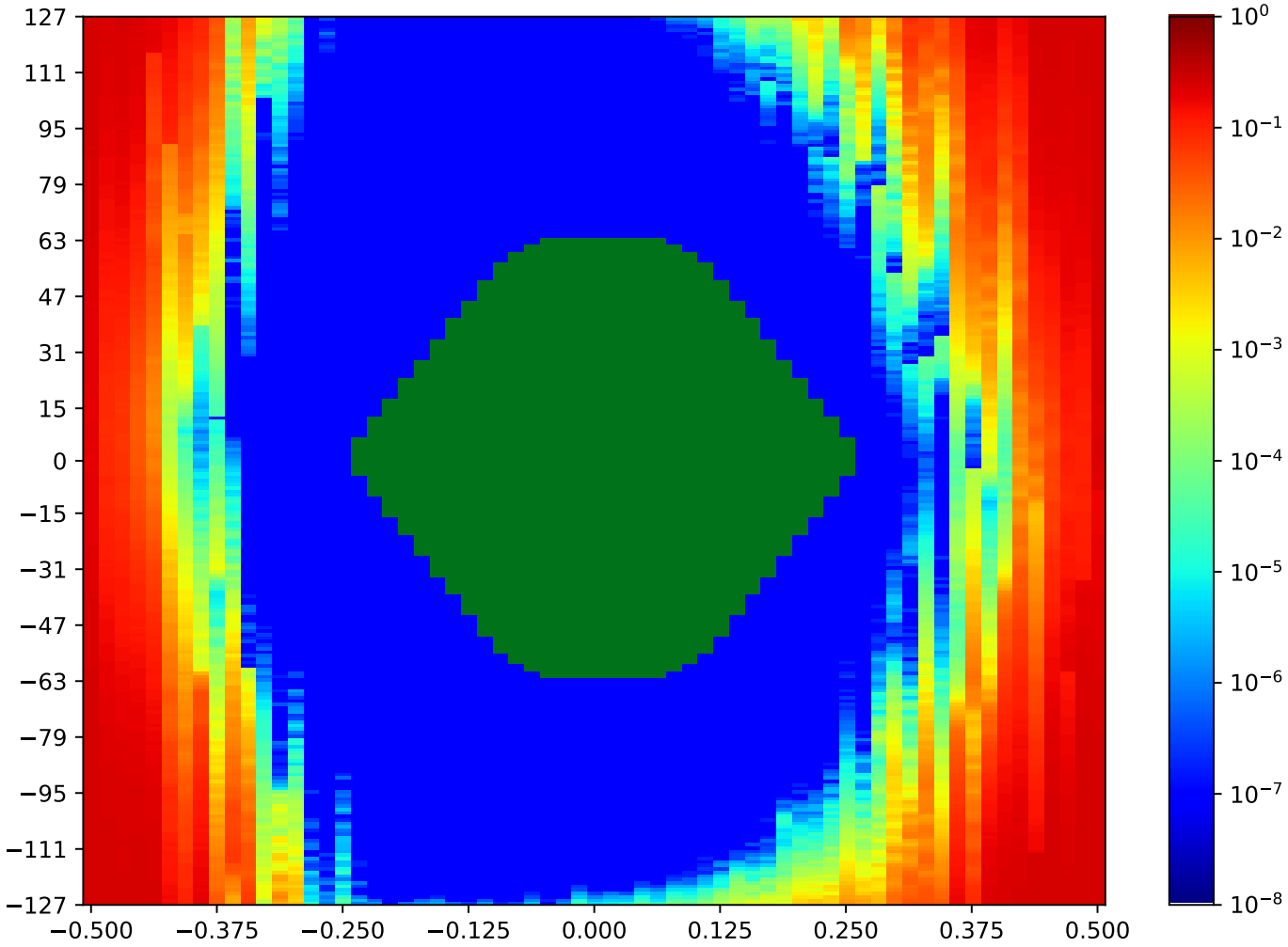


Figure 4.4: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.4 MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Table 4.4: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:45:00		2018-Sep-27 16:45:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8455	43	64.62%	250	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

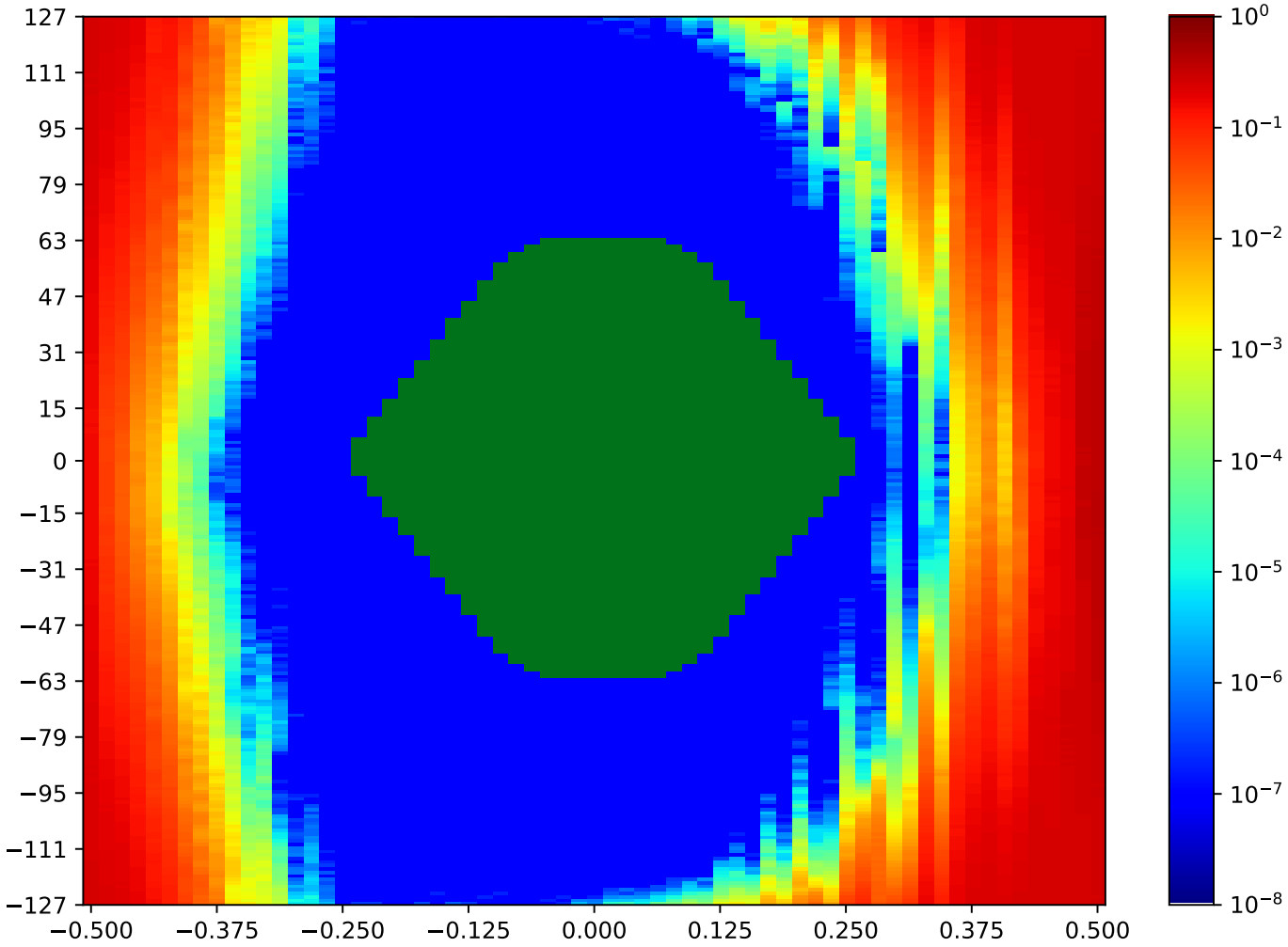


Figure 4.5: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.5 MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Table 4.5: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:50:17		2018-Sep-27 16:50:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8054	42	64.62%	233	91.37%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

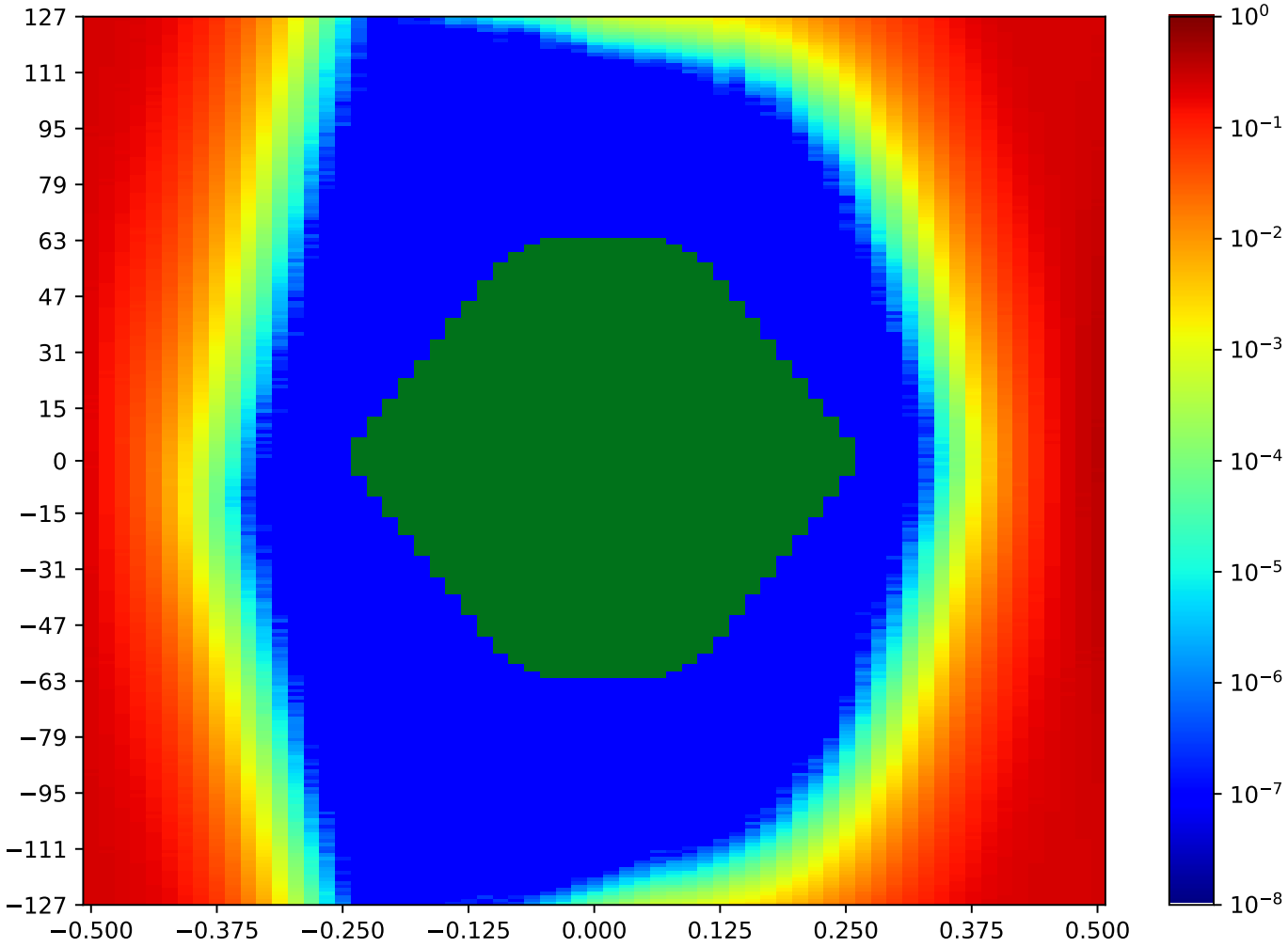


Figure 4.6: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.6 MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Table 4.6: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:44:40		2018-Sep-27 16:45:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8797	45	67.69%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

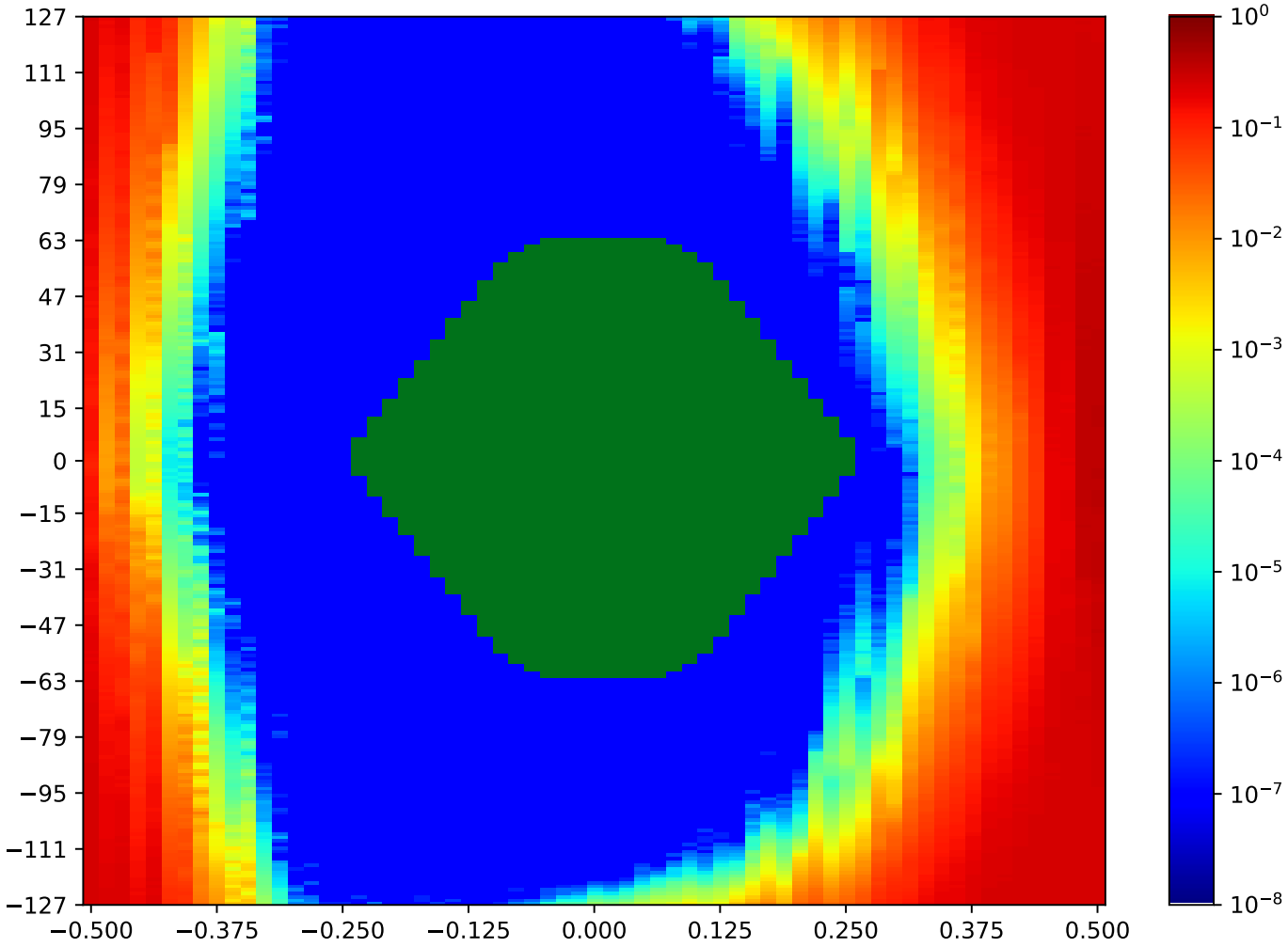


Figure 4.7: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.7 MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Table 4.7: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:52:20		2018-Sep-27 16:54:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8657	45	69.23%	230	90.20%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

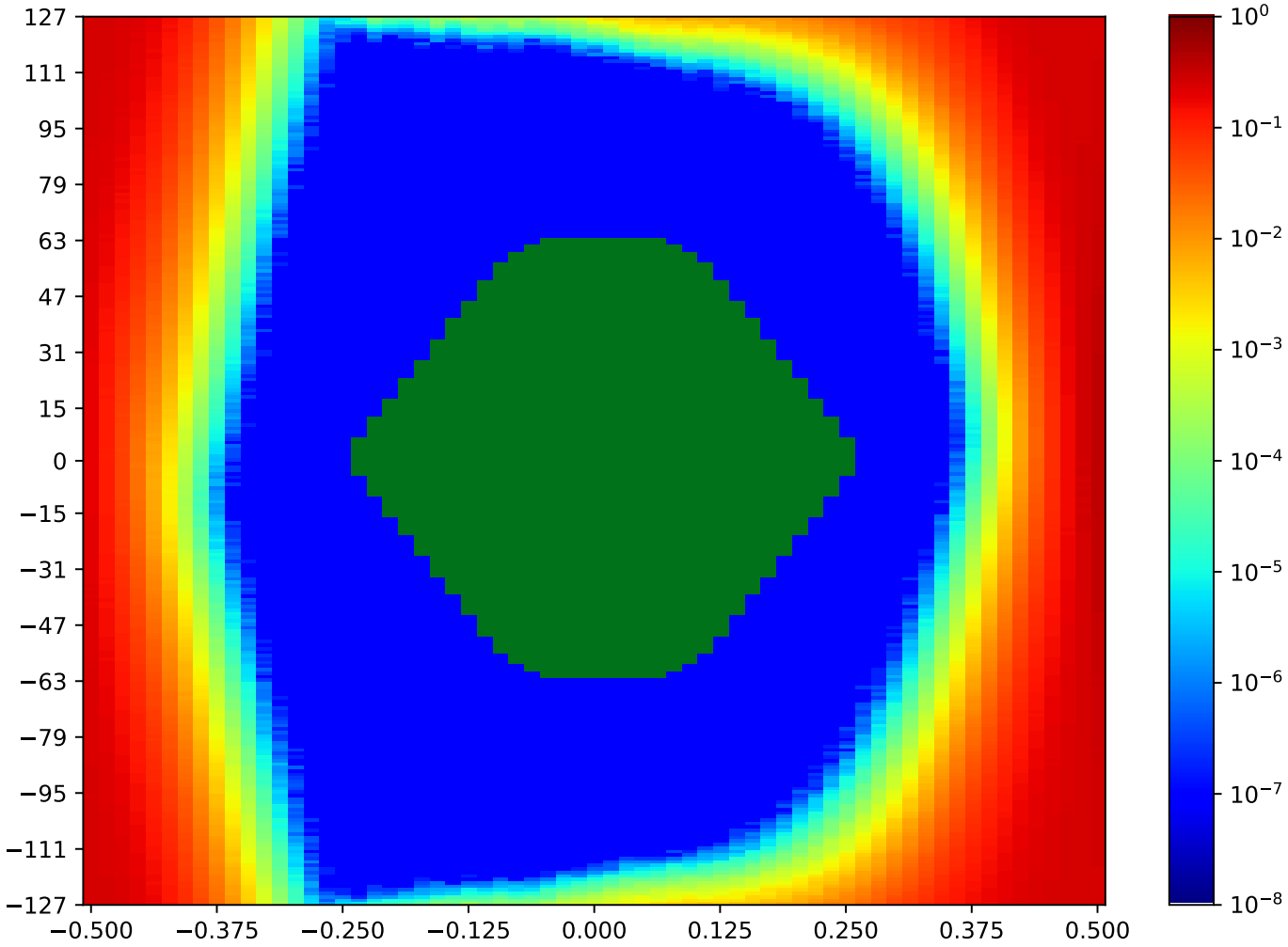


Figure 4.8: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.8 MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Table 4.8: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:45:20		2018-Sep-27 16:45:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9890	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

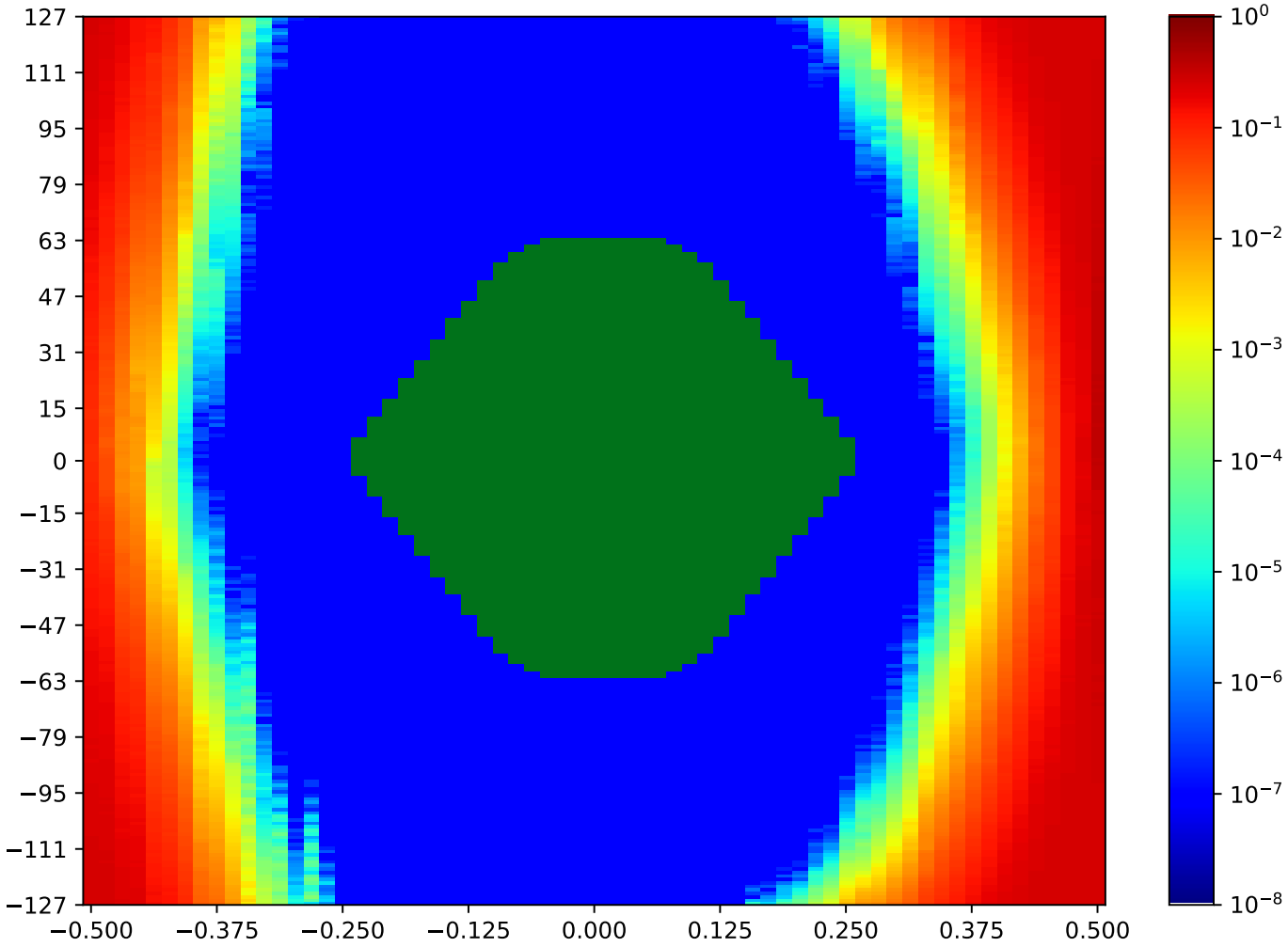


Figure 4.9: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.9 MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Table 4.9: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:50:42		2018-Sep-27 16:52:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8269	45	69.23%	223	87.06%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

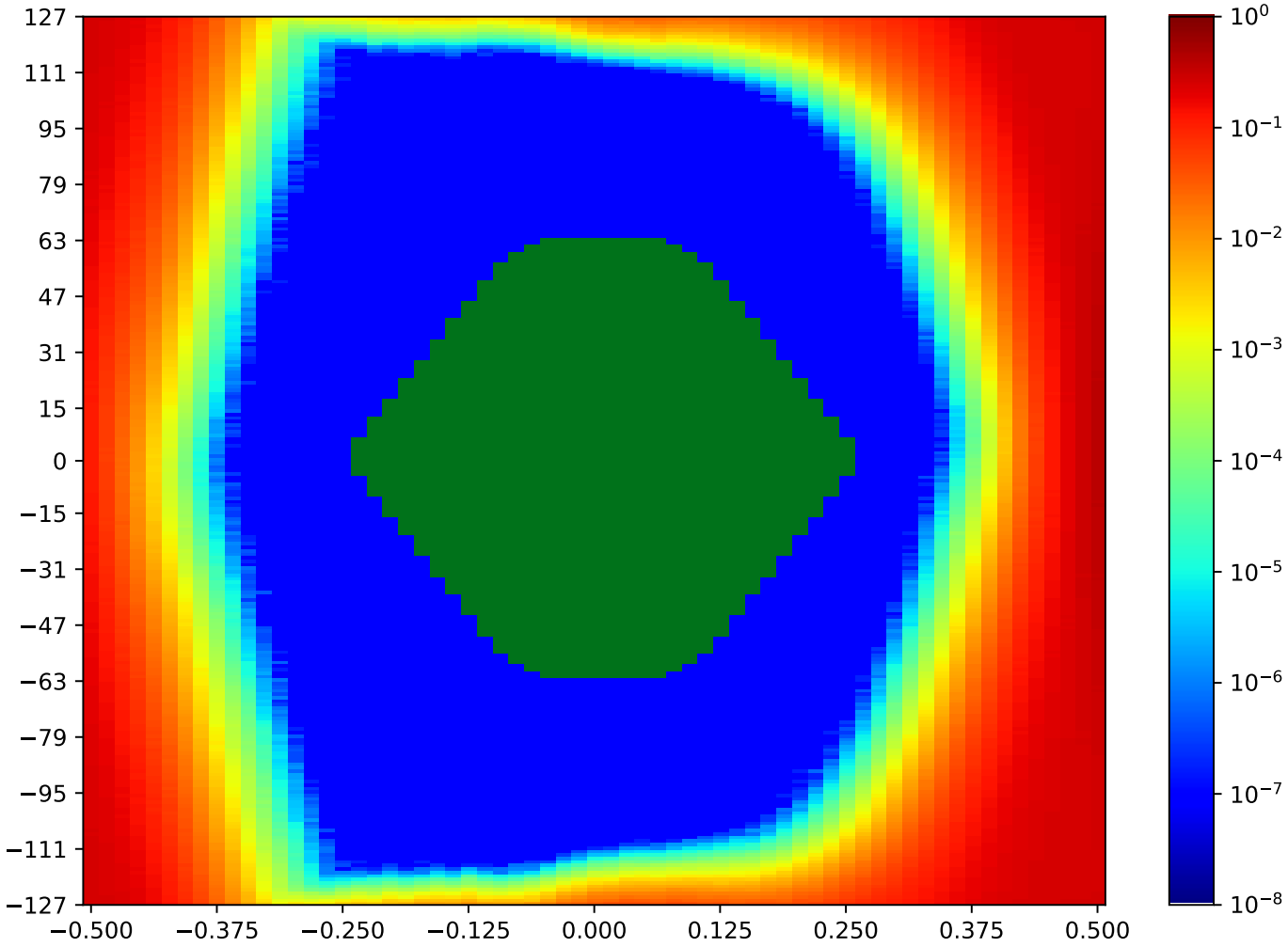


Figure 4.10: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.10 MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Table 4.10: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:46:01		2018-Sep-27 16:46:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9565	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

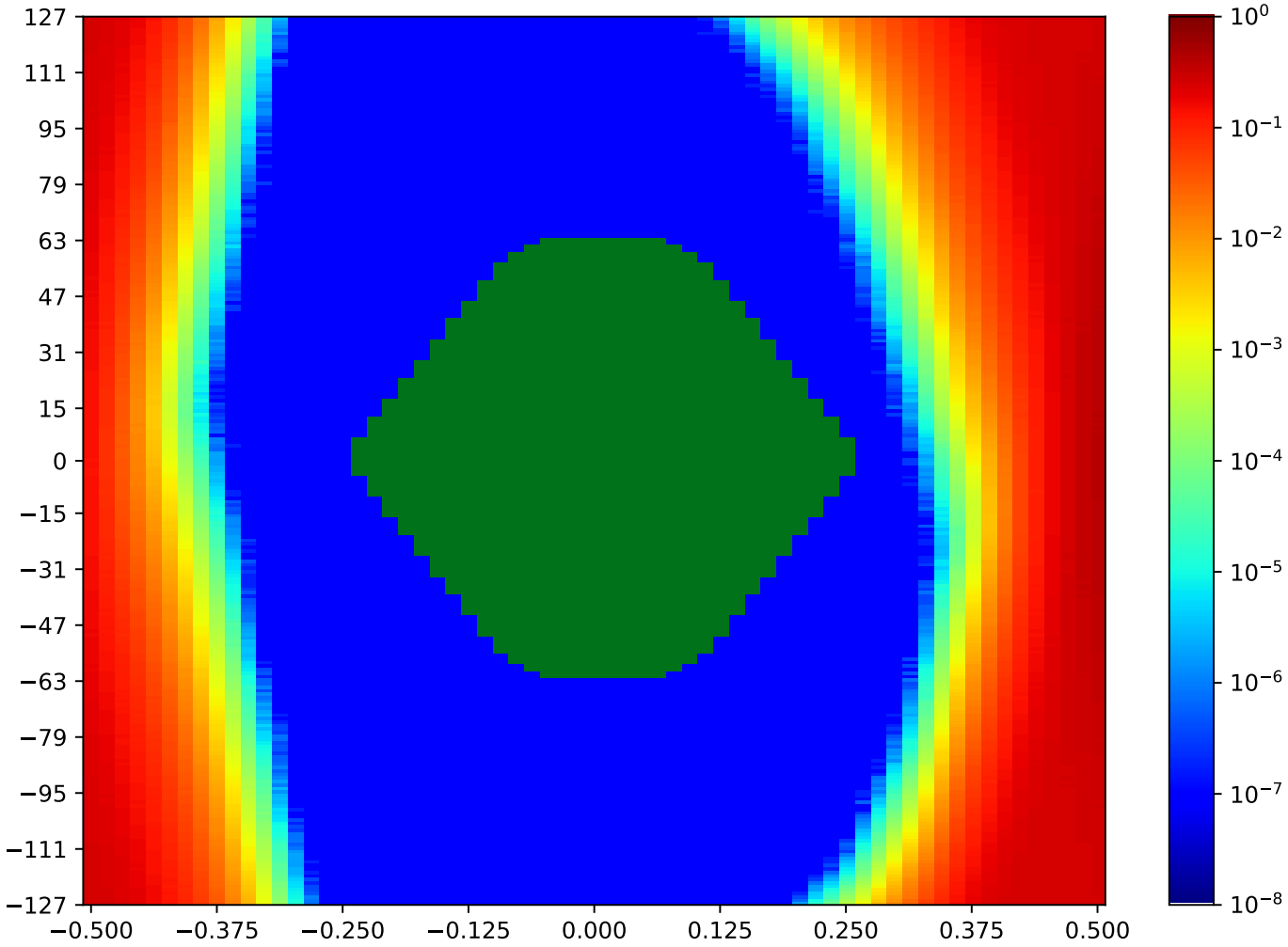


Figure 4.11: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.11 MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Table 4.11: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:48:38		2018-Sep-27 16:50:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8860	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

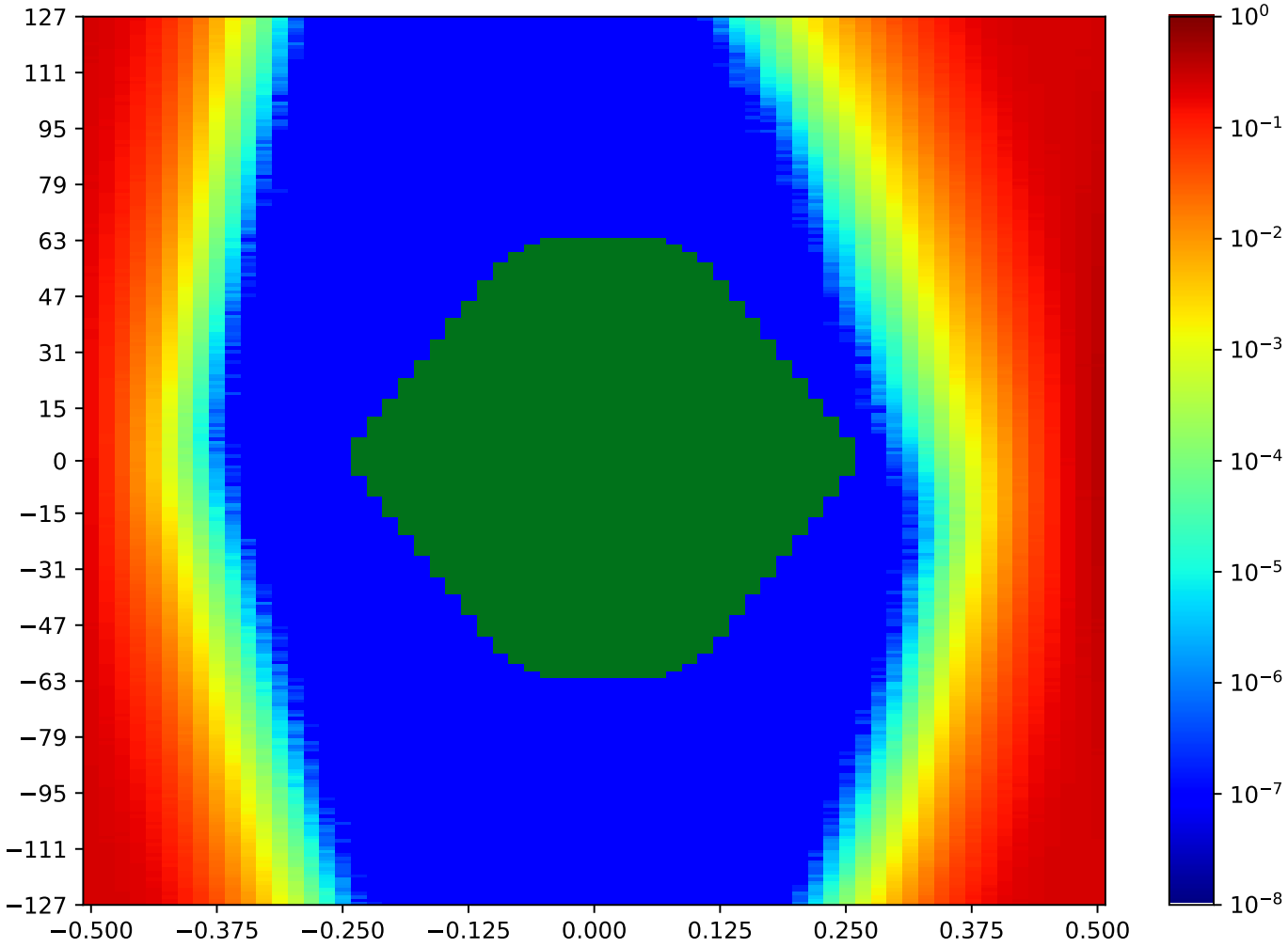


Figure 4.12: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.1.12 MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Table 4.12: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:47:02		2018-Sep-27 16:48:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9683	45	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

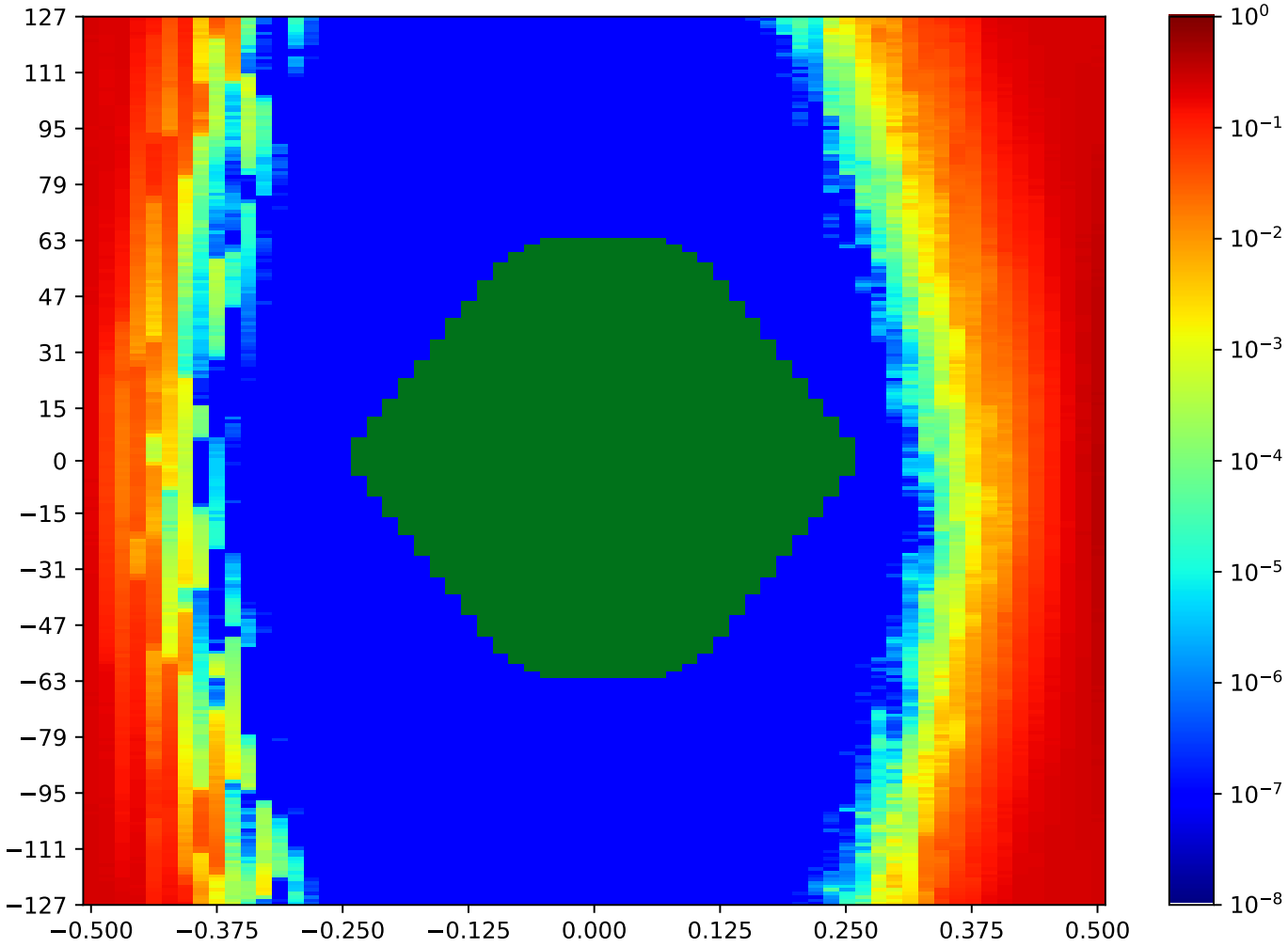


Figure 4.13: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2 MSP_A TX2 MSP_C RX16 Minipod Loopback

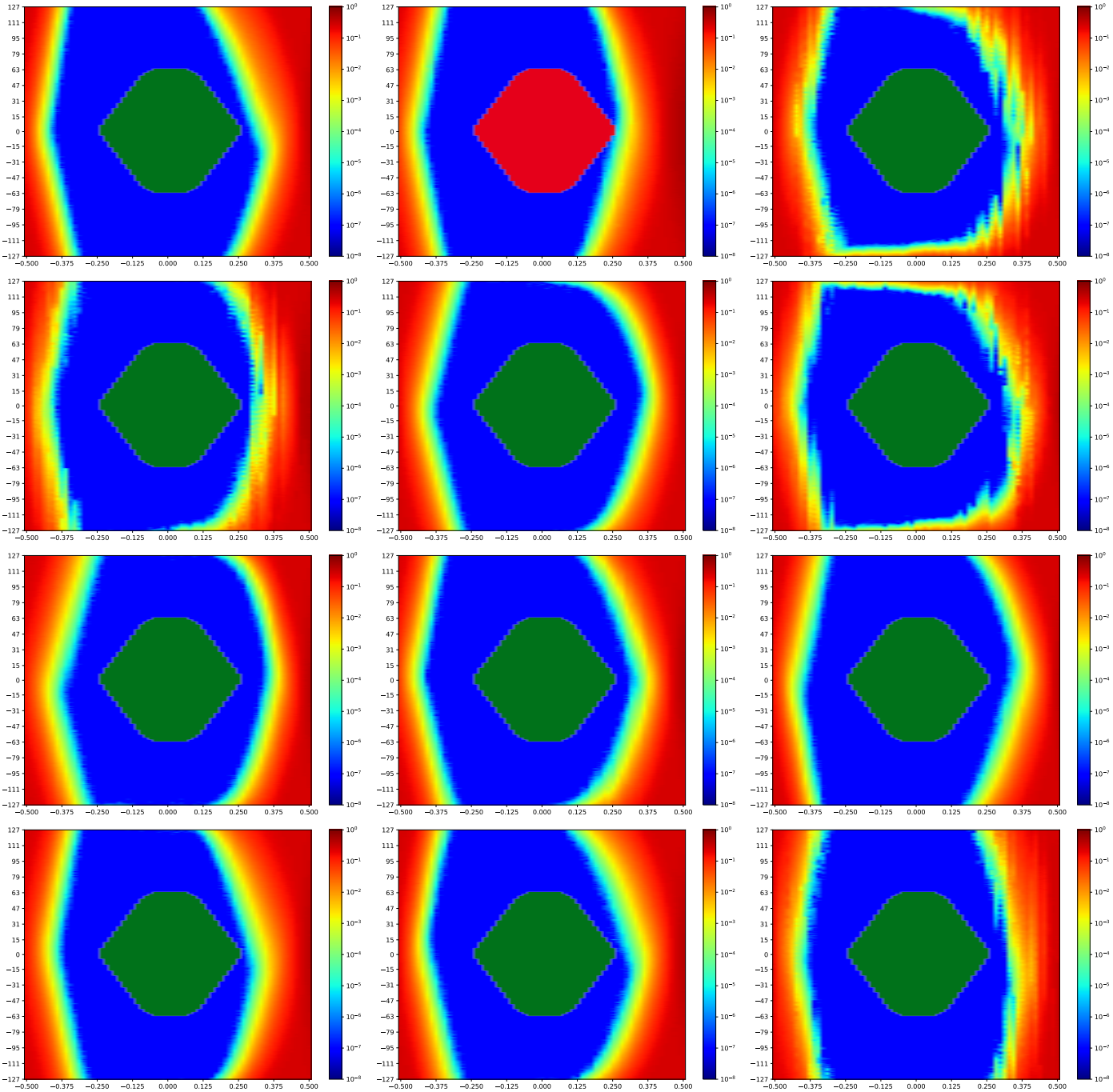


Figure 4.14: MSP_A TX2 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.27.

4.2.1 MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Table 4.13: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:55:00		2018-Sep-27 16:55:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9494	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

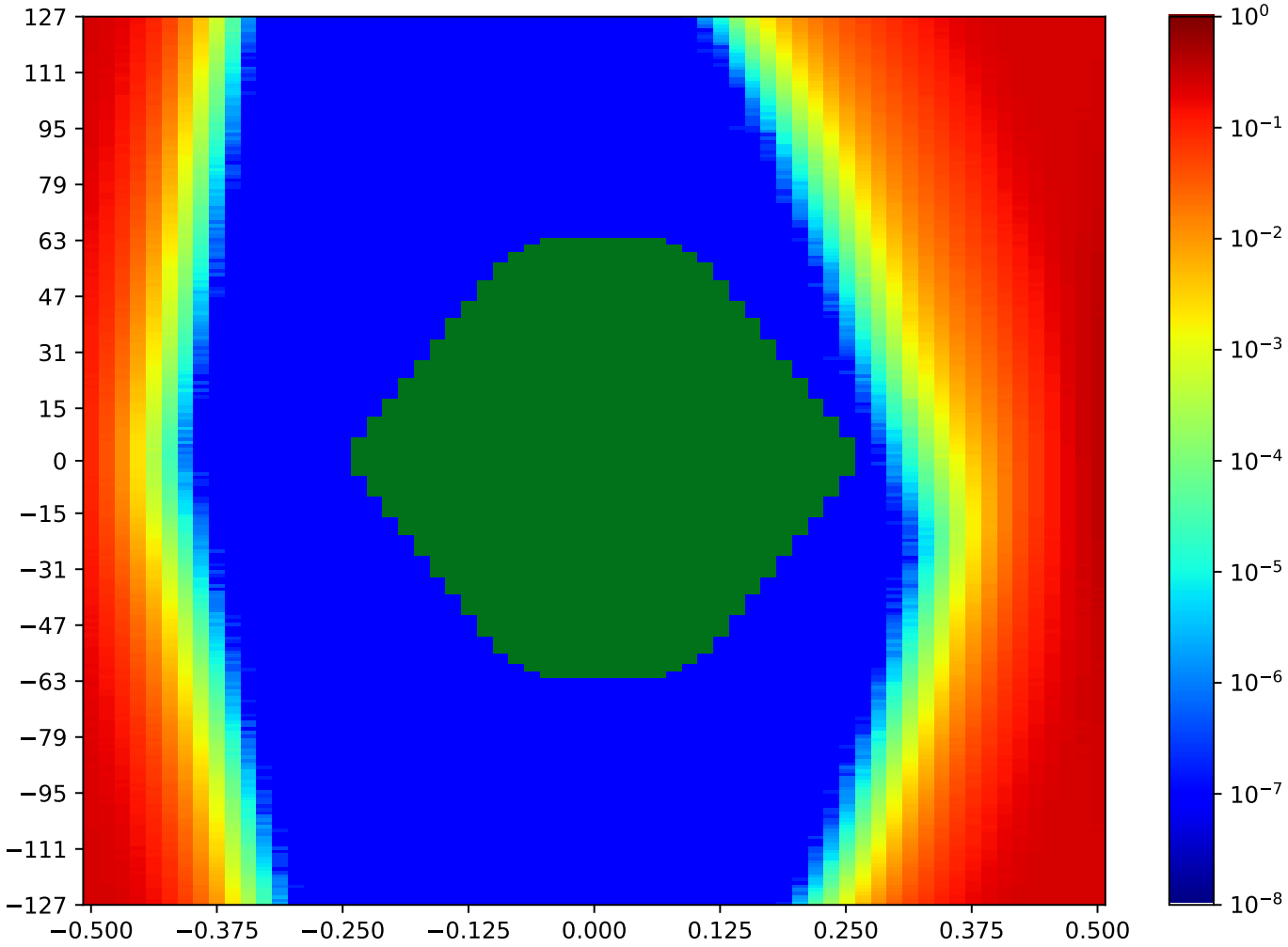


Figure 4.15: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.2 MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Table 4.14: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:54:20		2018-Sep-27 16:54:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9026	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

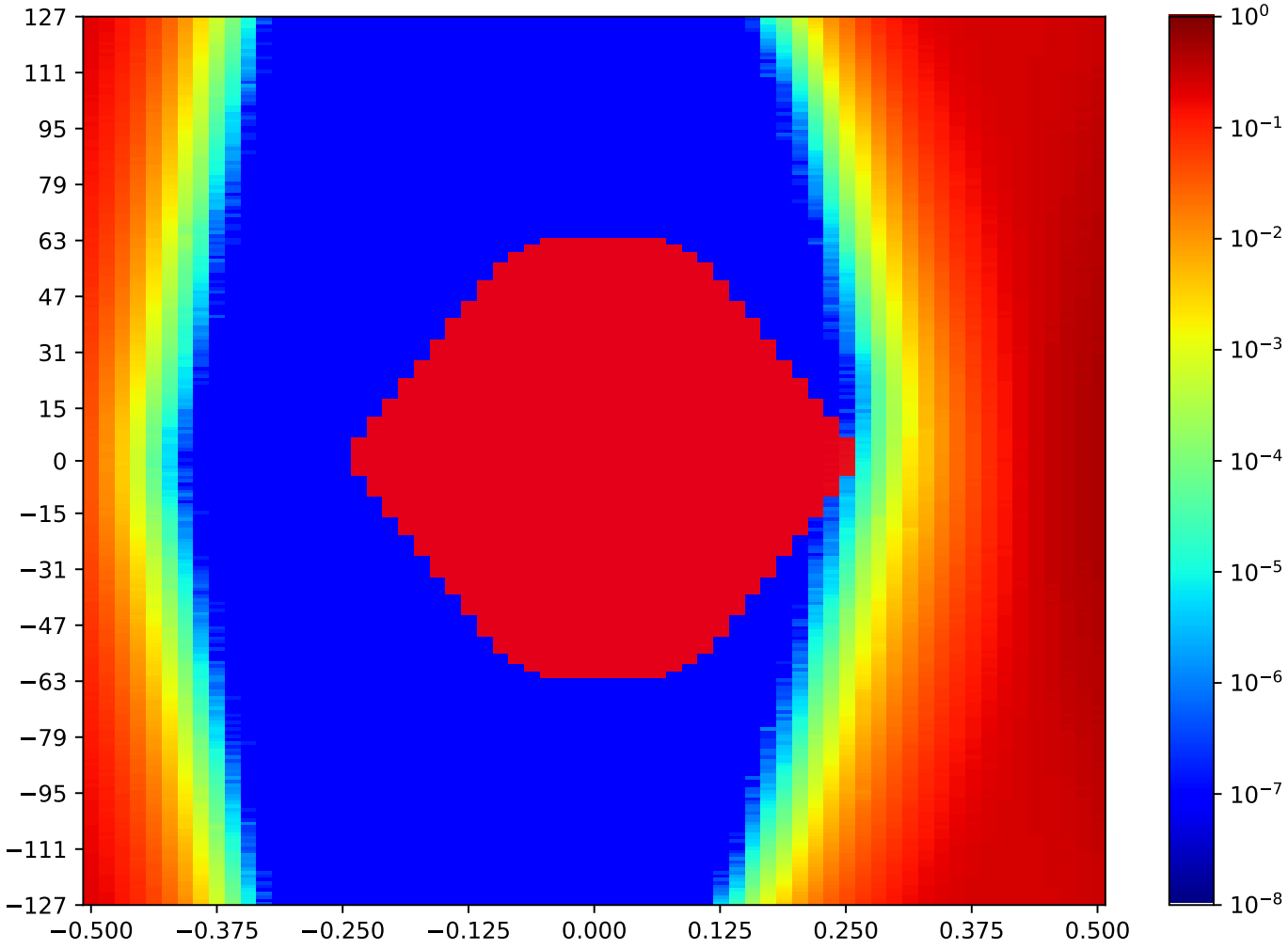


Figure 4.16: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.3 MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Table 4.15: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:56:06		2018-Sep-27 16:56:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8198	42	64.62%	229	89.41%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

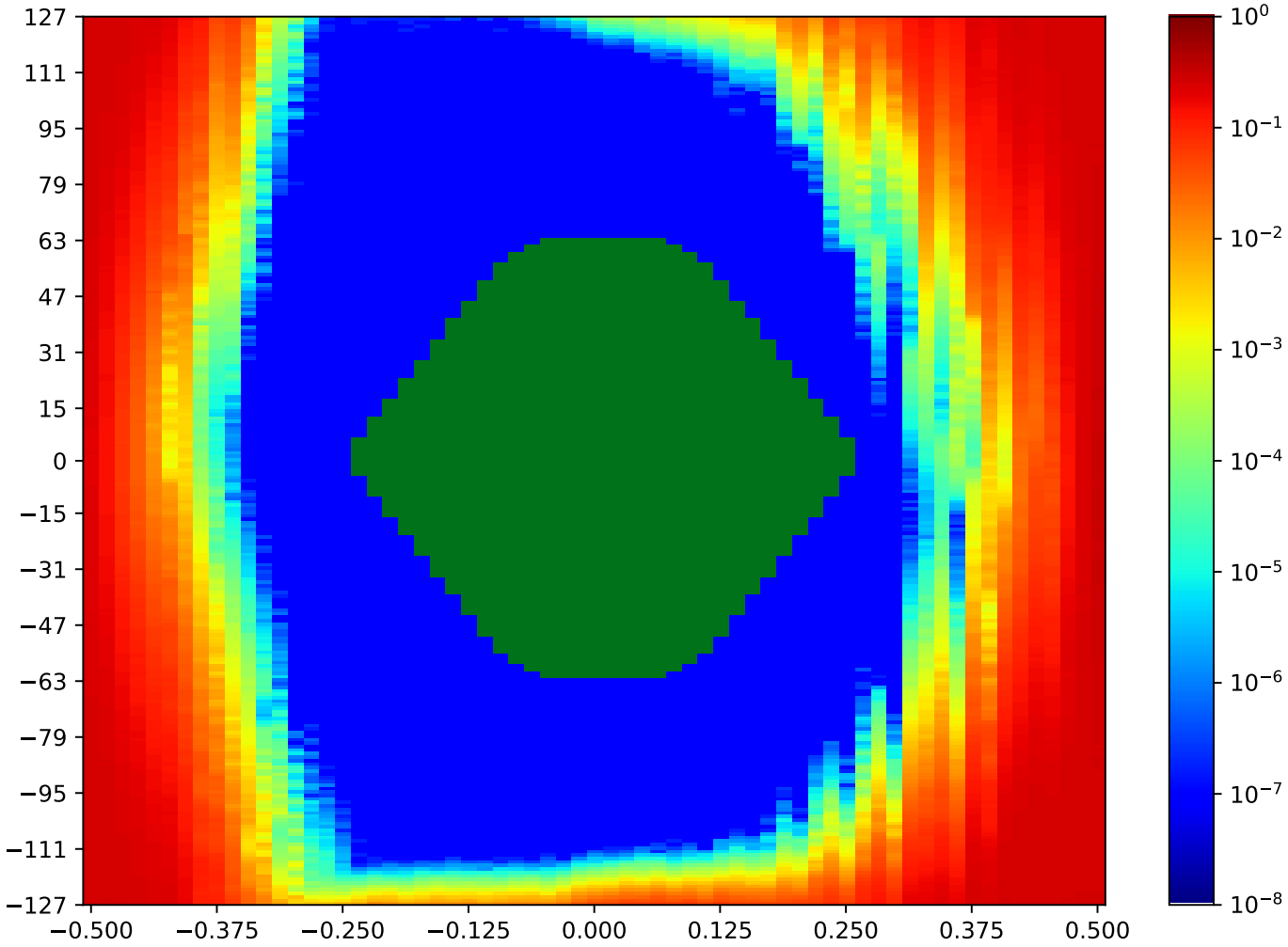


Figure 4.17: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.4 MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Table 4.16: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:54:00		2018-Sep-27 16:54:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9223	43	66.15%	253	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

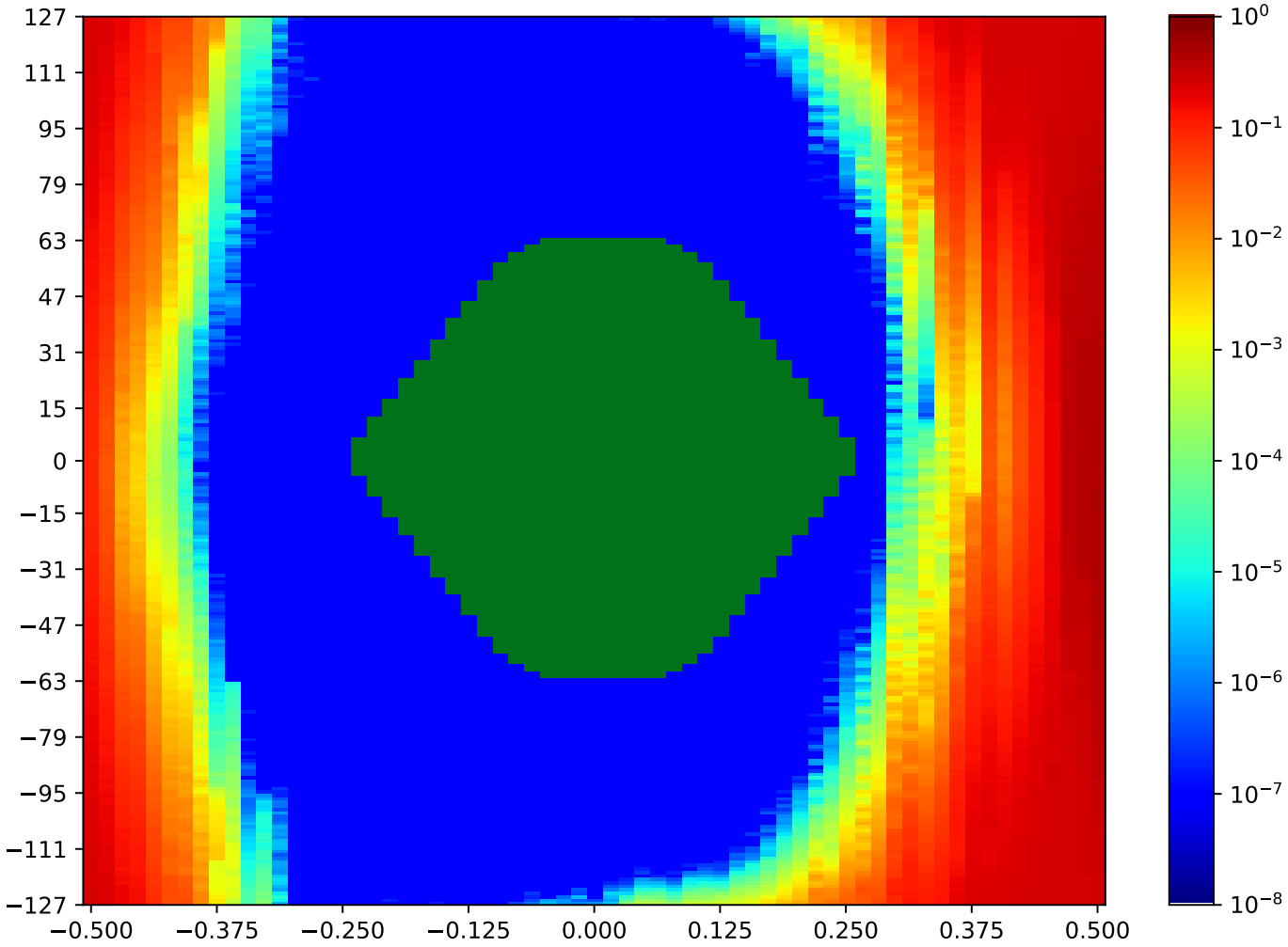


Figure 4.18: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.5 MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Table 4.17: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:57:07		2018-Sep-27 16:57:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9086	44	67.69%	251	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

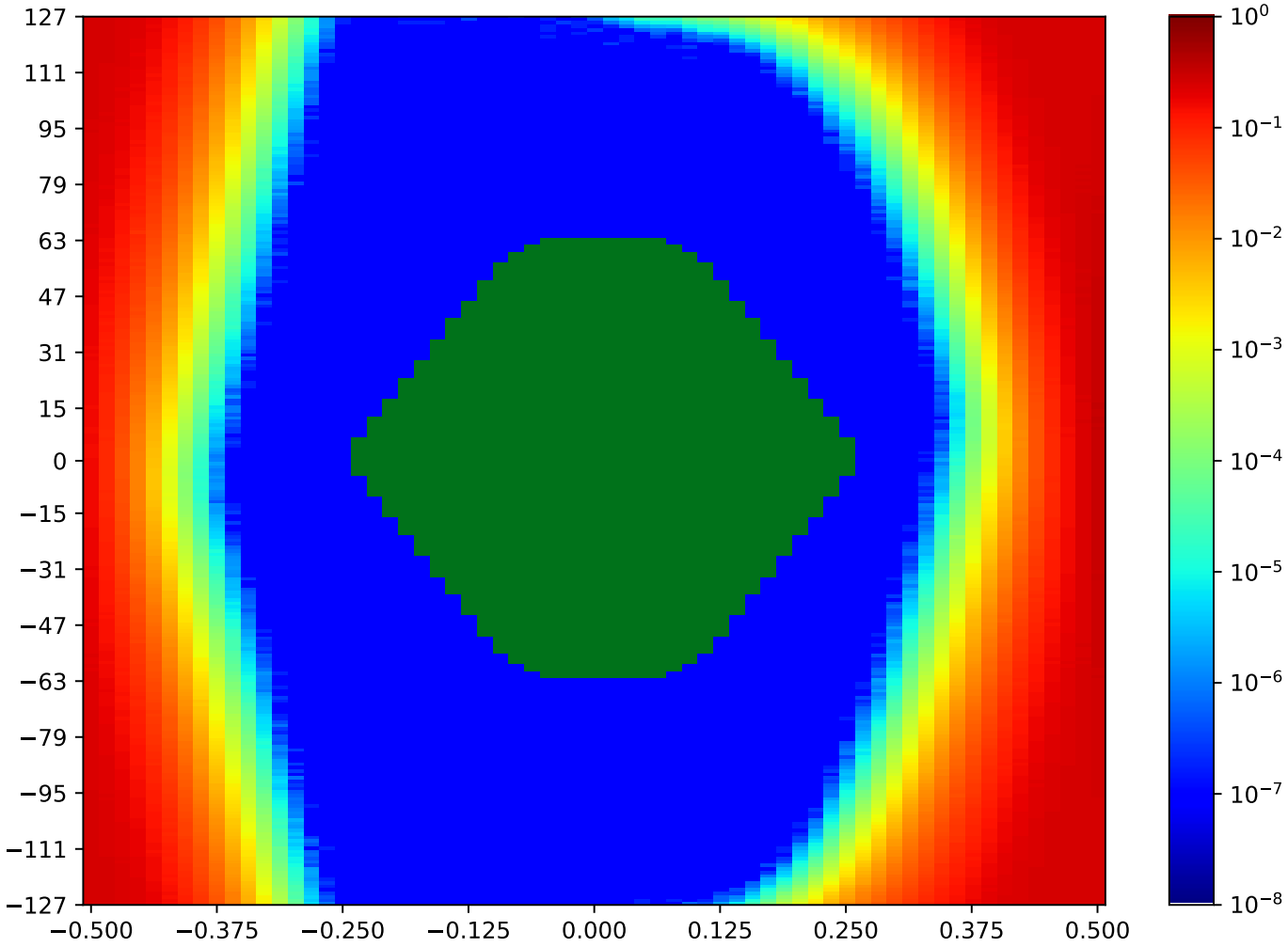


Figure 4.19: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.6 MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Table 4.18: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:54:40		2018-Sep-27 16:55:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8556	44	67.69%	226	87.45%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

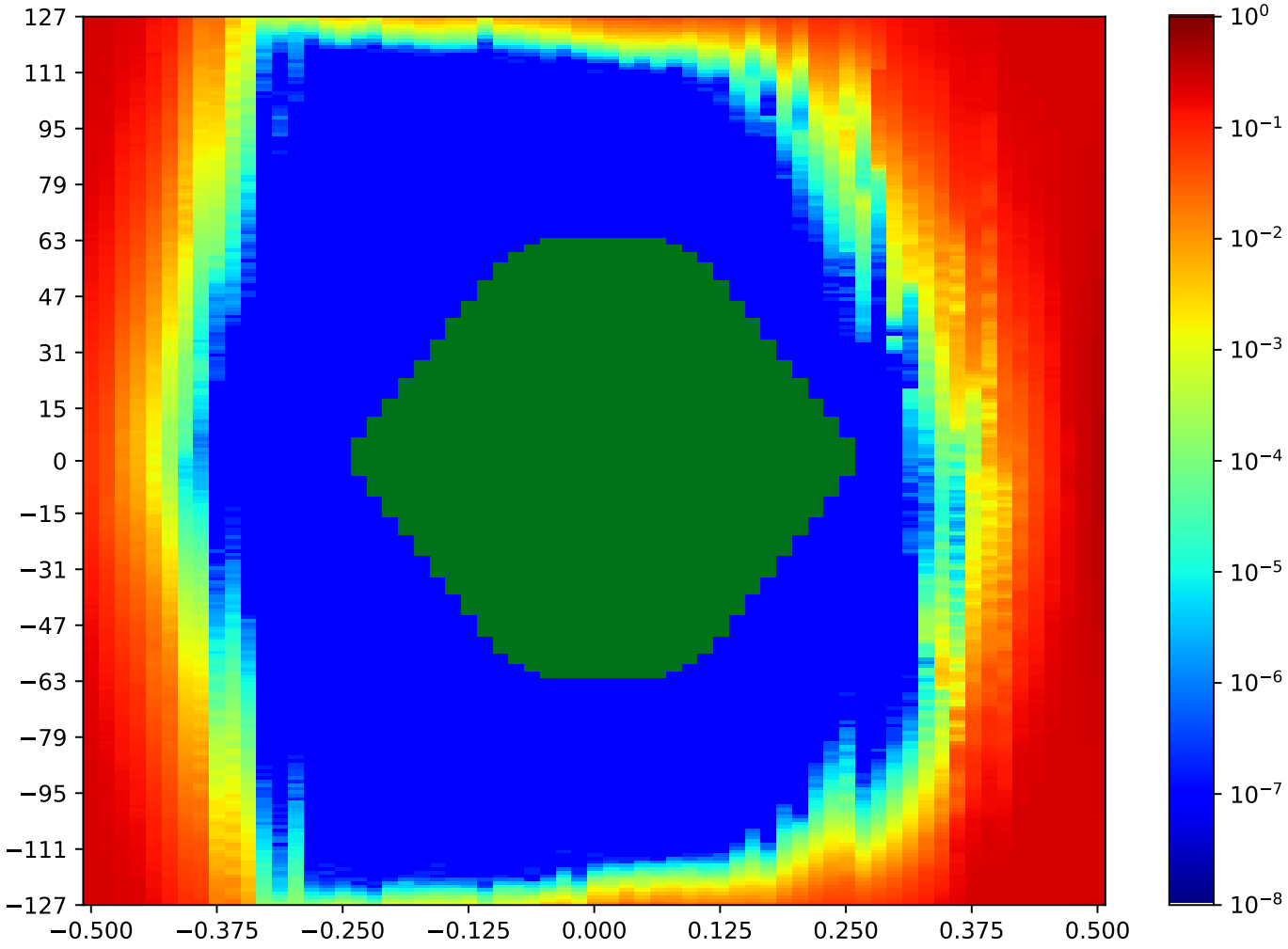


Figure 4.20: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.7 MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Table 4.19: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:57:48		2018-Sep-27 16:58:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8993	43	66.15%	253	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

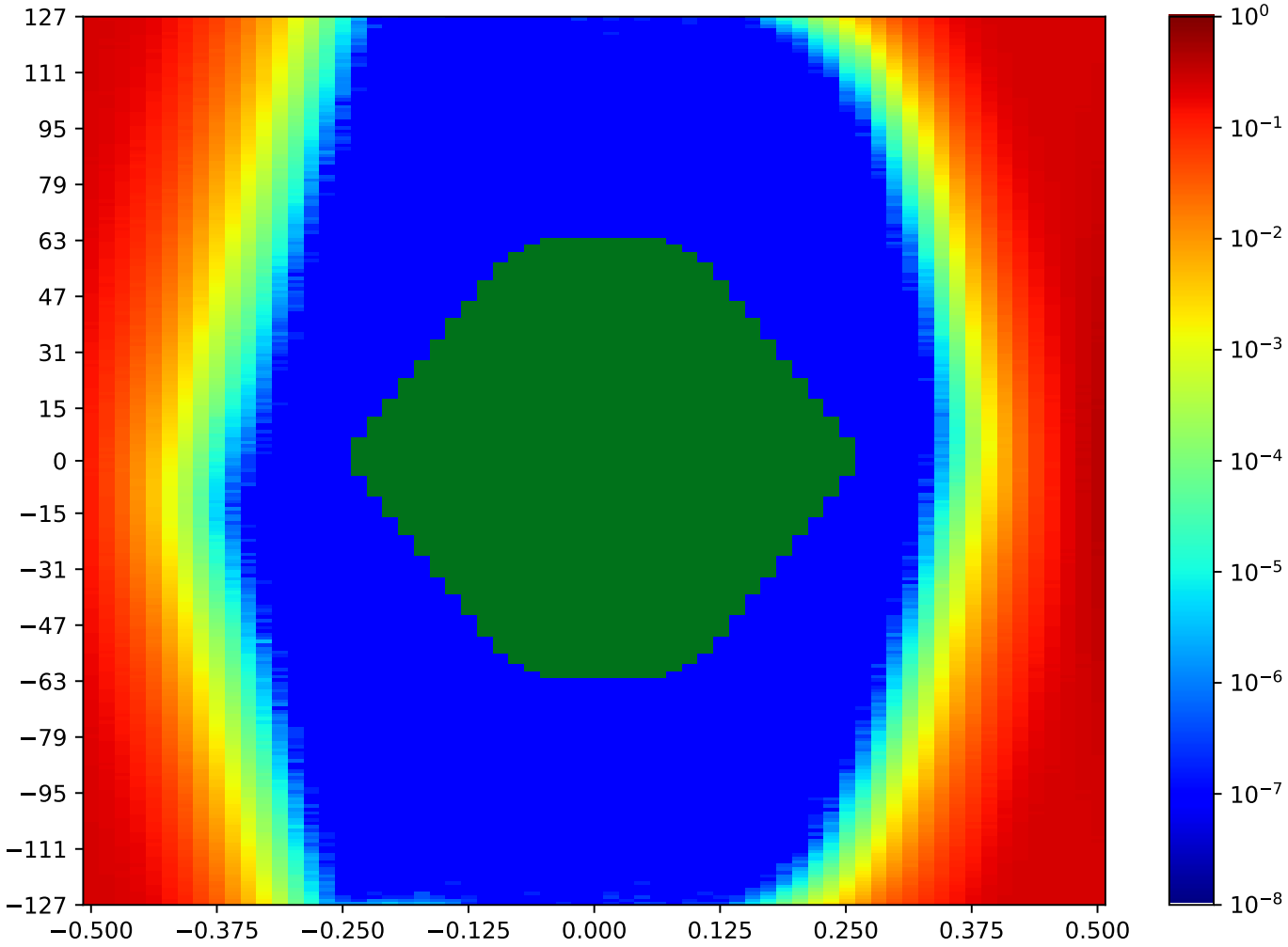


Figure 4.21: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.8 MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Table 4.20: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:55:20		2018-Sep-27 16:55:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9291	45	69.23%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

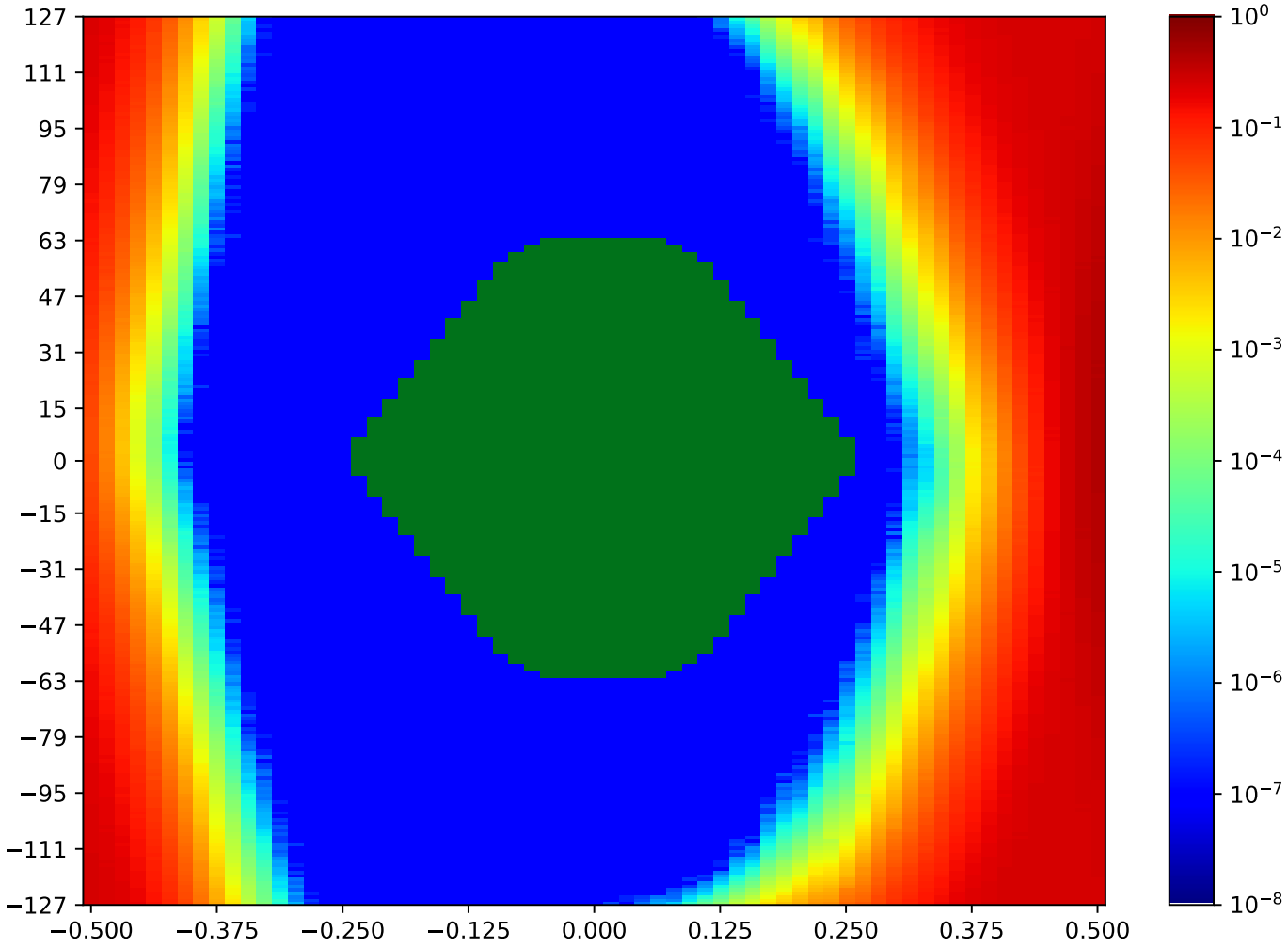


Figure 4.22: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.9 MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Table 4.21: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:57:27		2018-Sep-27 16:57:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9615	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

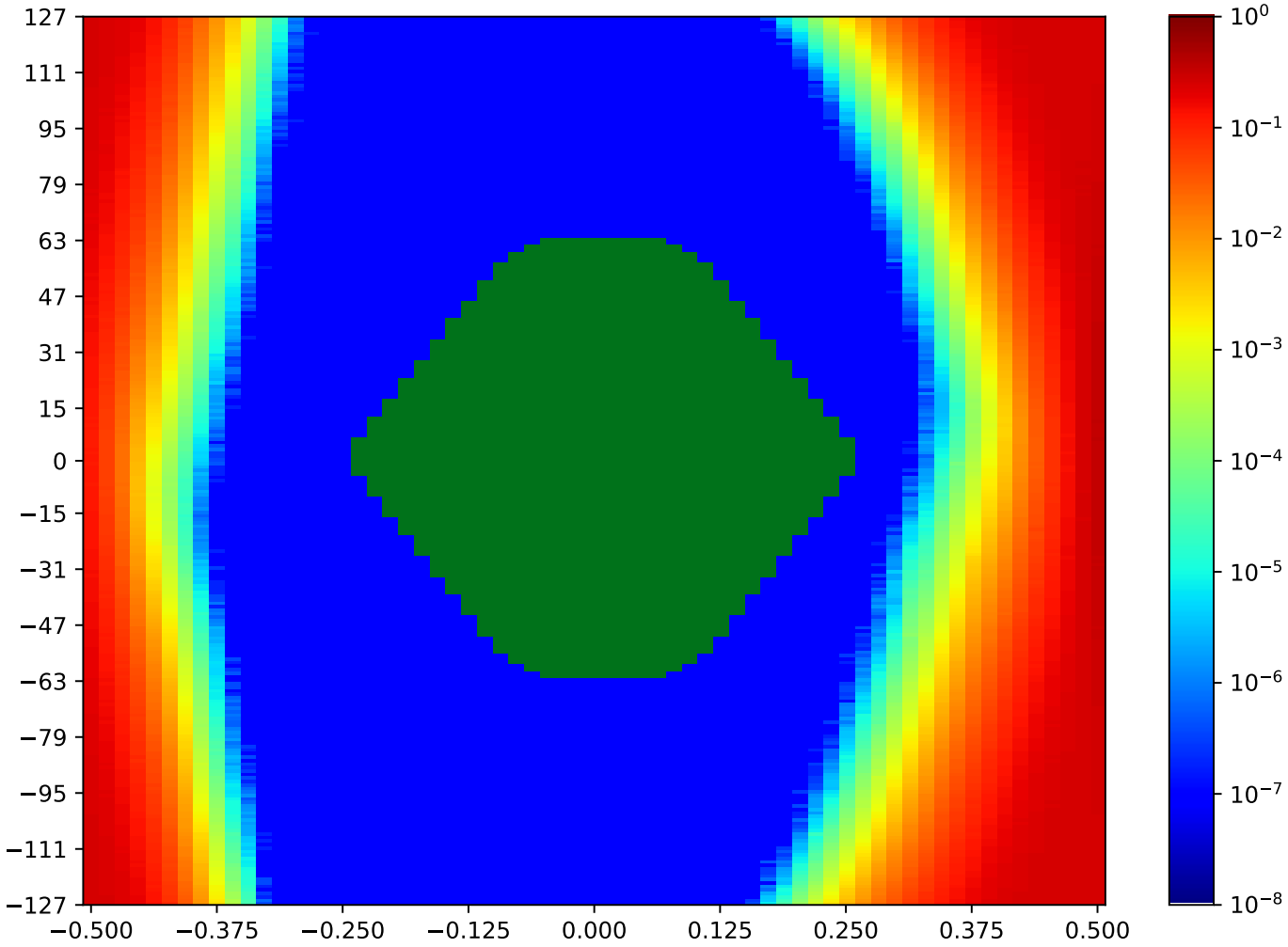


Figure 4.23: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.10 MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Table 4.22: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:55:41		2018-Sep-27 16:56:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8601	39	60.00%	250	97.65%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

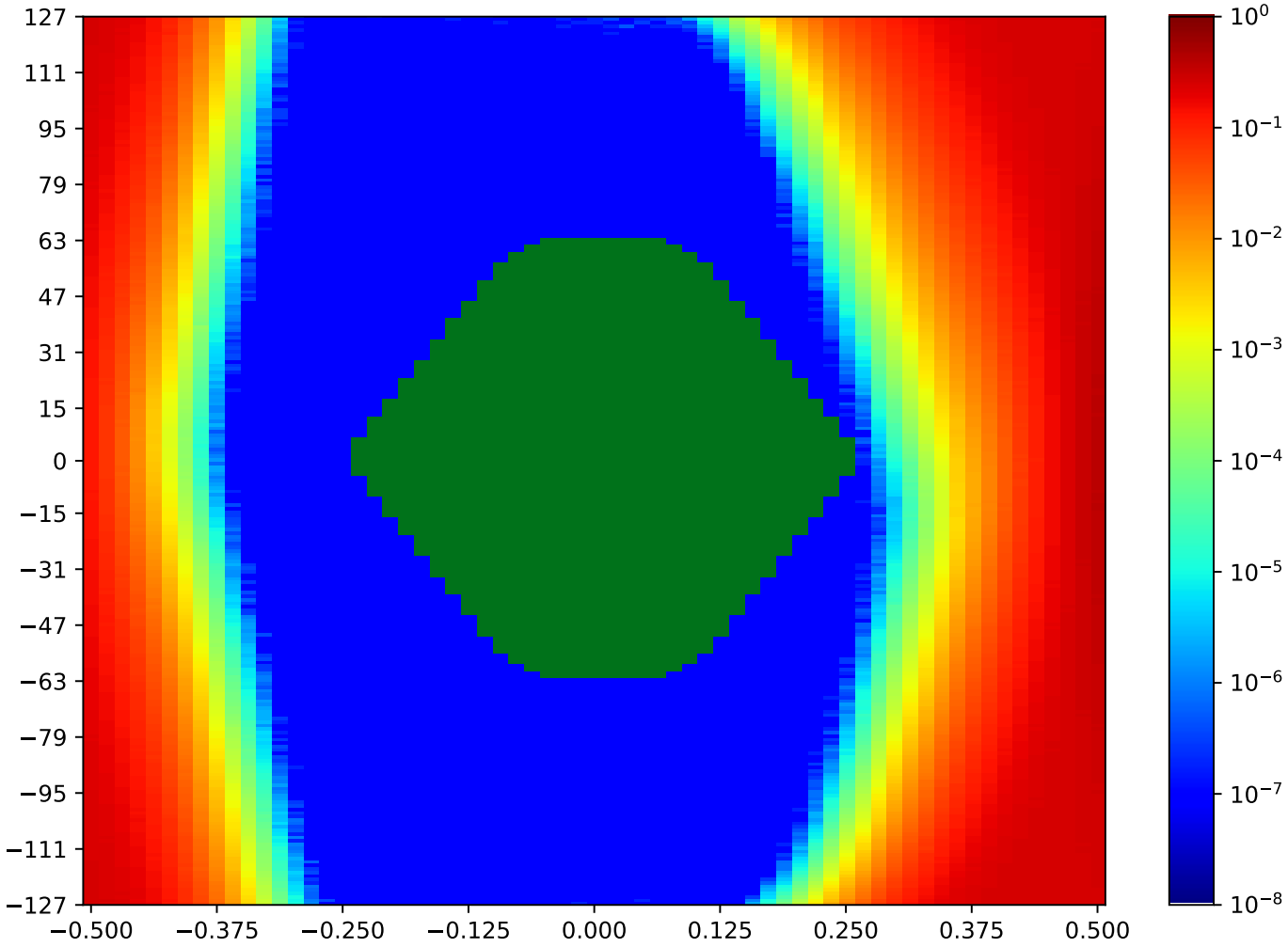


Figure 4.24: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.11 MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Table 4.23: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:56:47		2018-Sep-27 16:57:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8768	42	64.62%	254	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

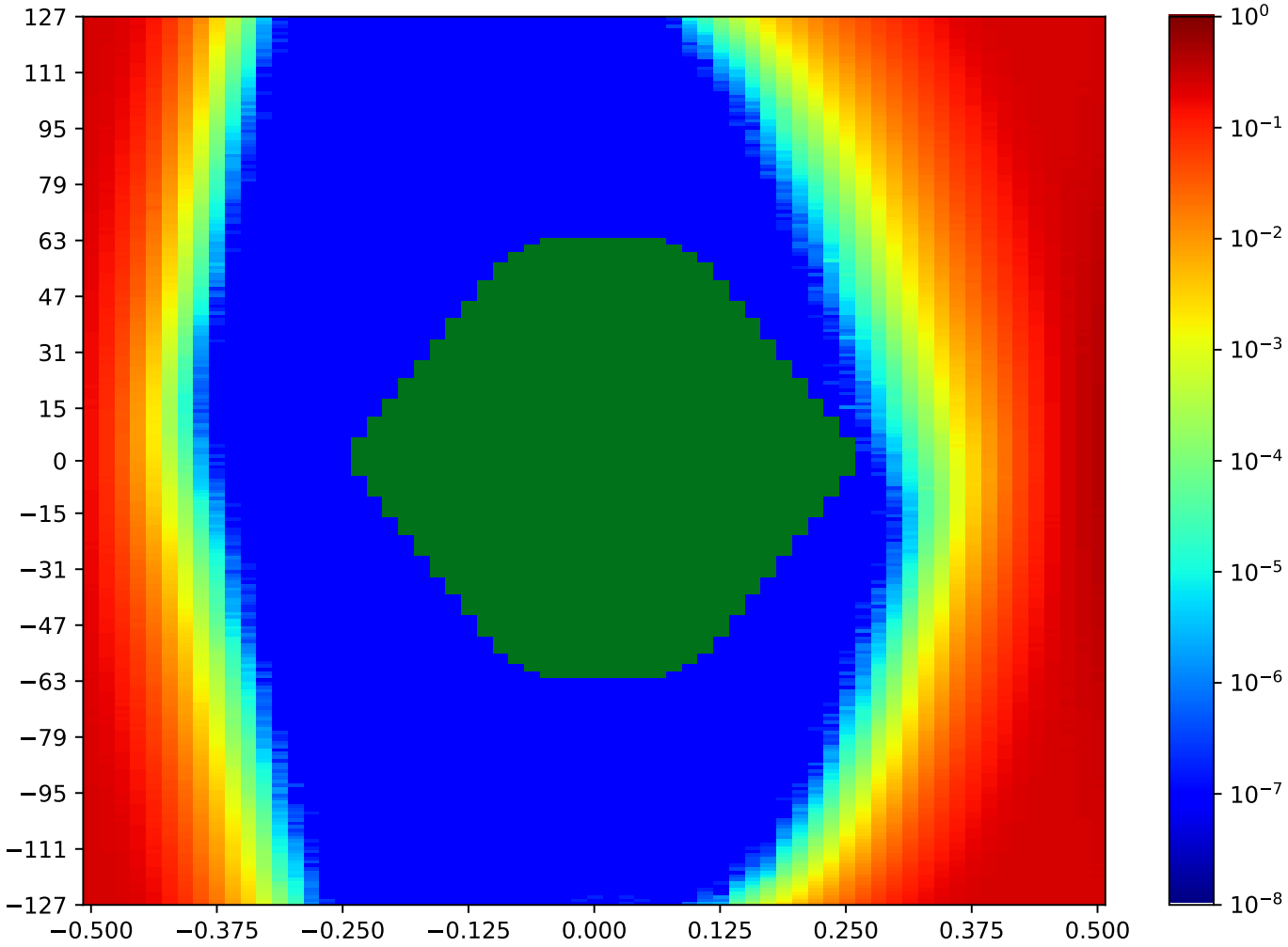


Figure 4.25: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.2.12 MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Table 4.24: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:56:26		2018-Sep-27 16:56:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9908	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

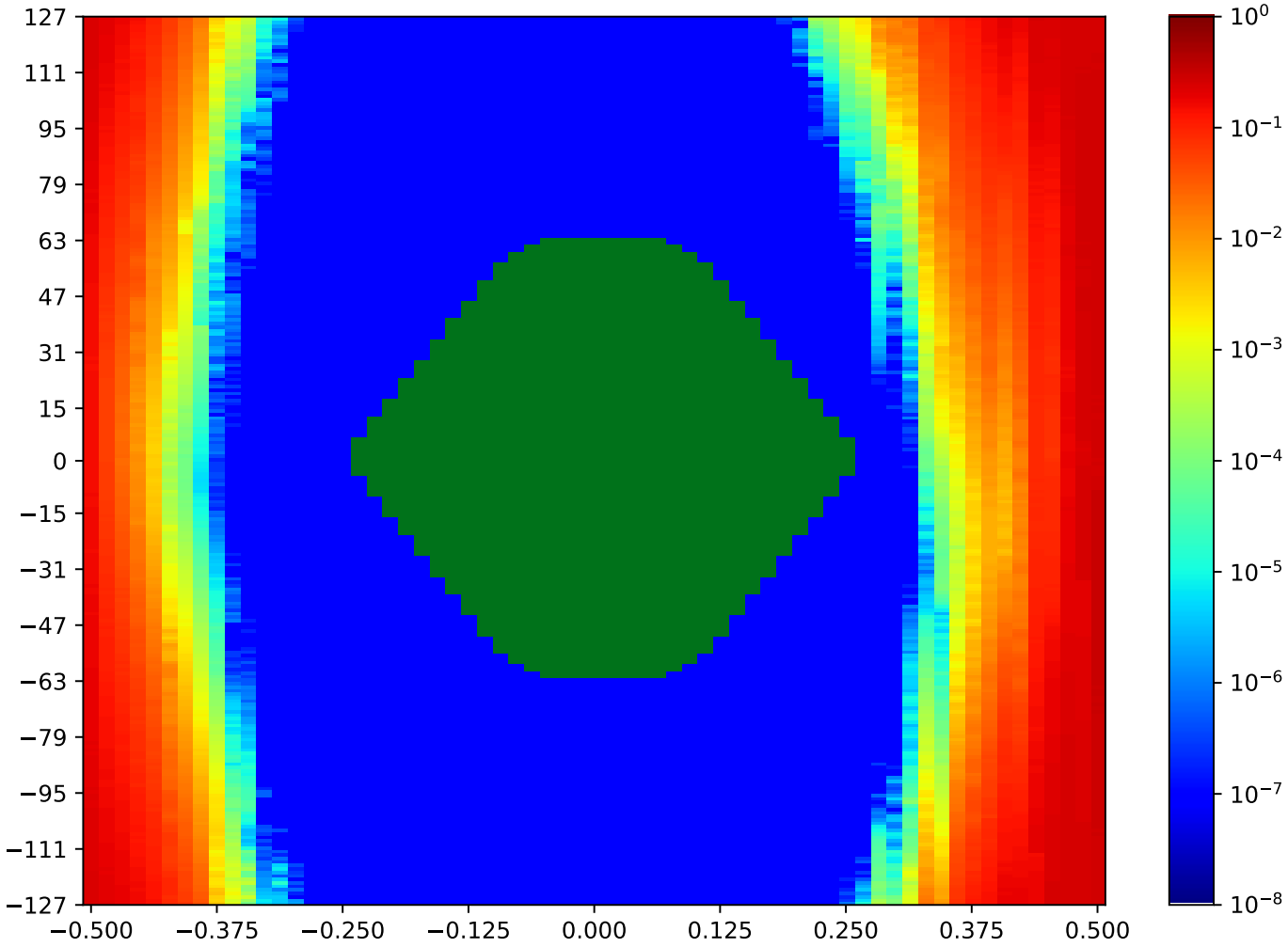


Figure 4.26: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3 MSP_C TX3 MSP_A RX6 Minipod Loopback

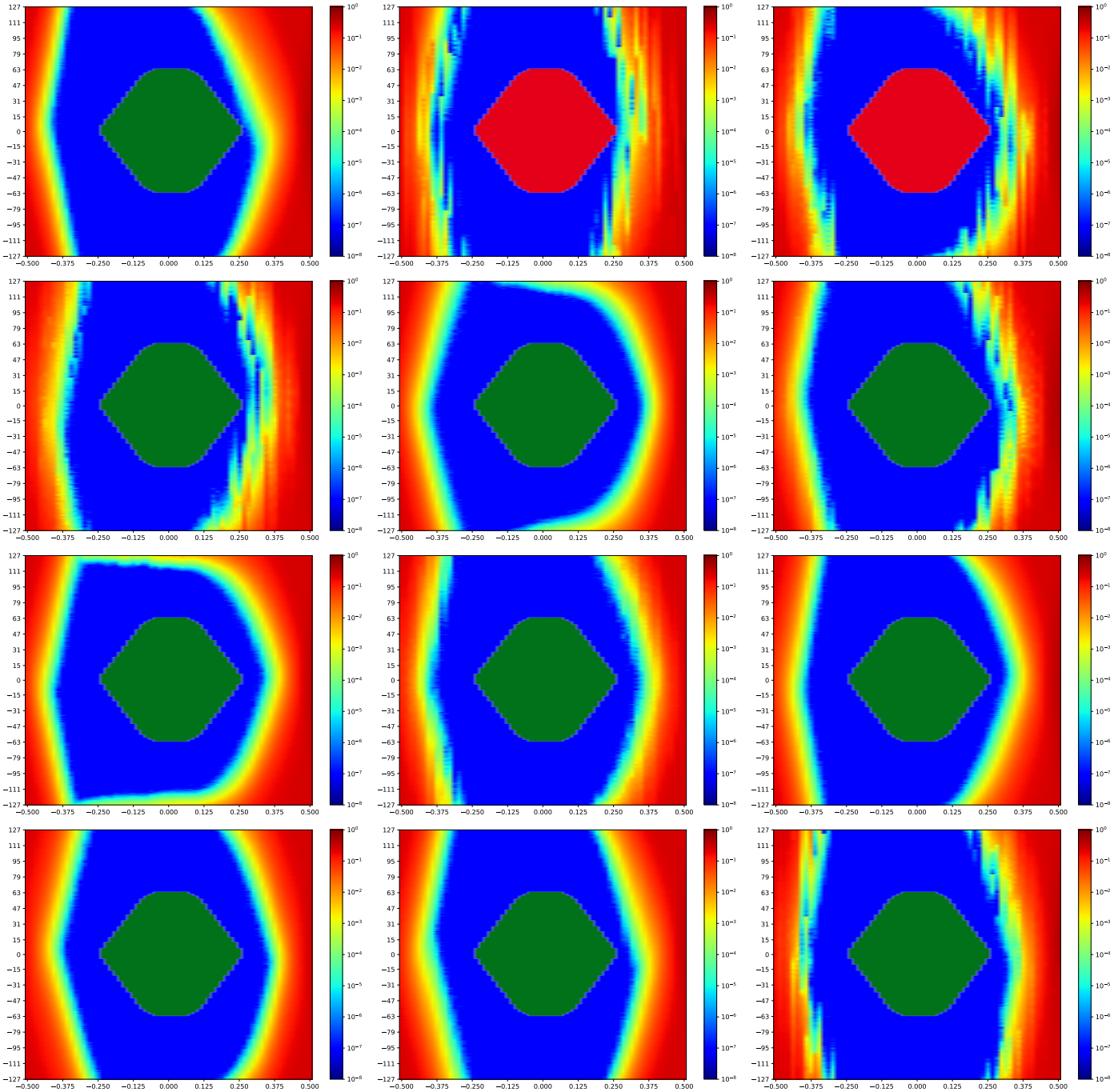


Figure 4.27: MSP_C TX3 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.40.

4.3.1 MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Table 4.25: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:59:09		2018-Sep-27 16:59:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9281	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

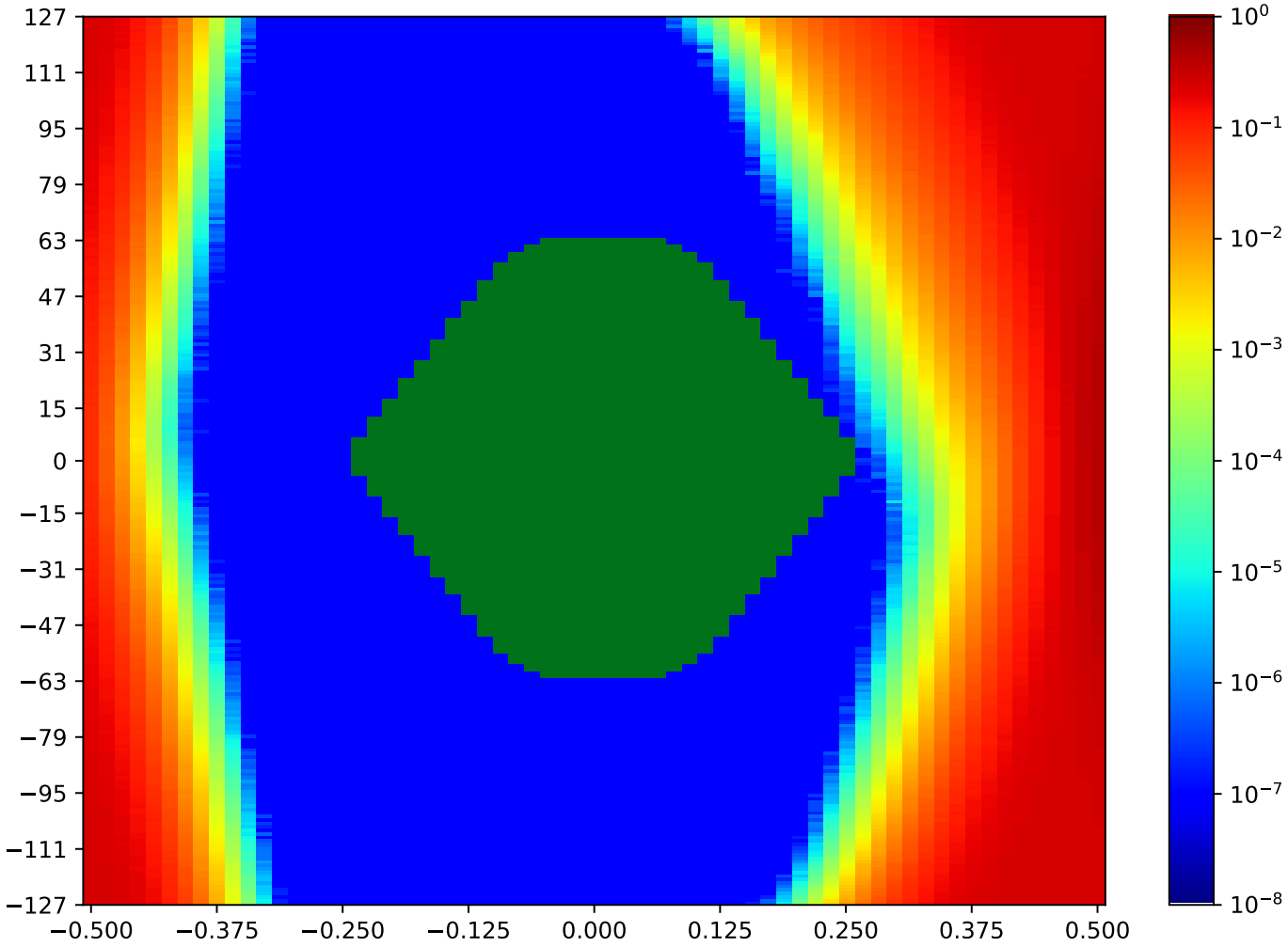


Figure 4.28: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.2 MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Table 4.26: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:59:51		2018-Sep-27 17:00:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8746	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

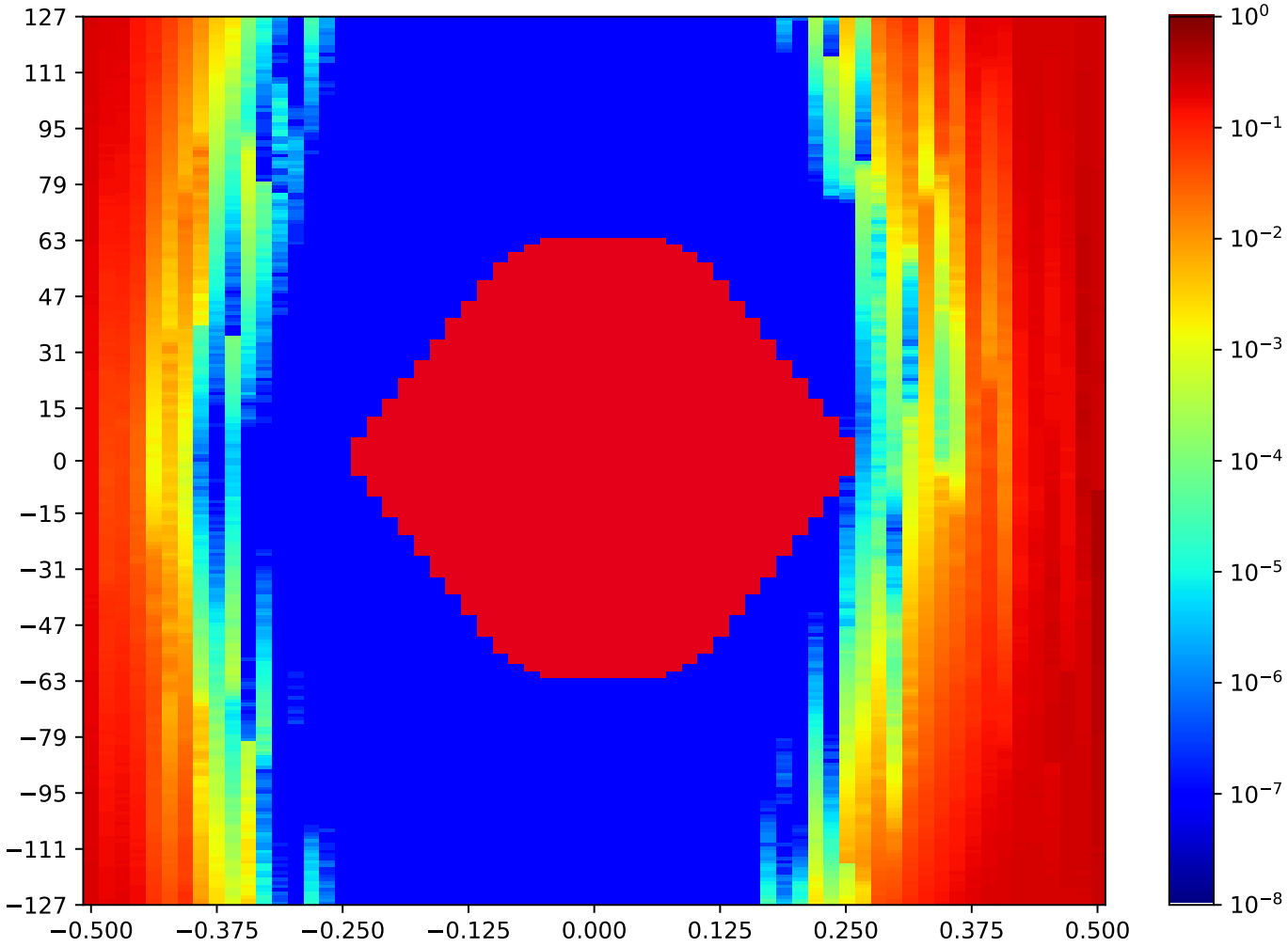


Figure 4.29: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.3 MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Table 4.27: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:00:12		2018-Sep-27 17:00:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8417	40	60.00%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

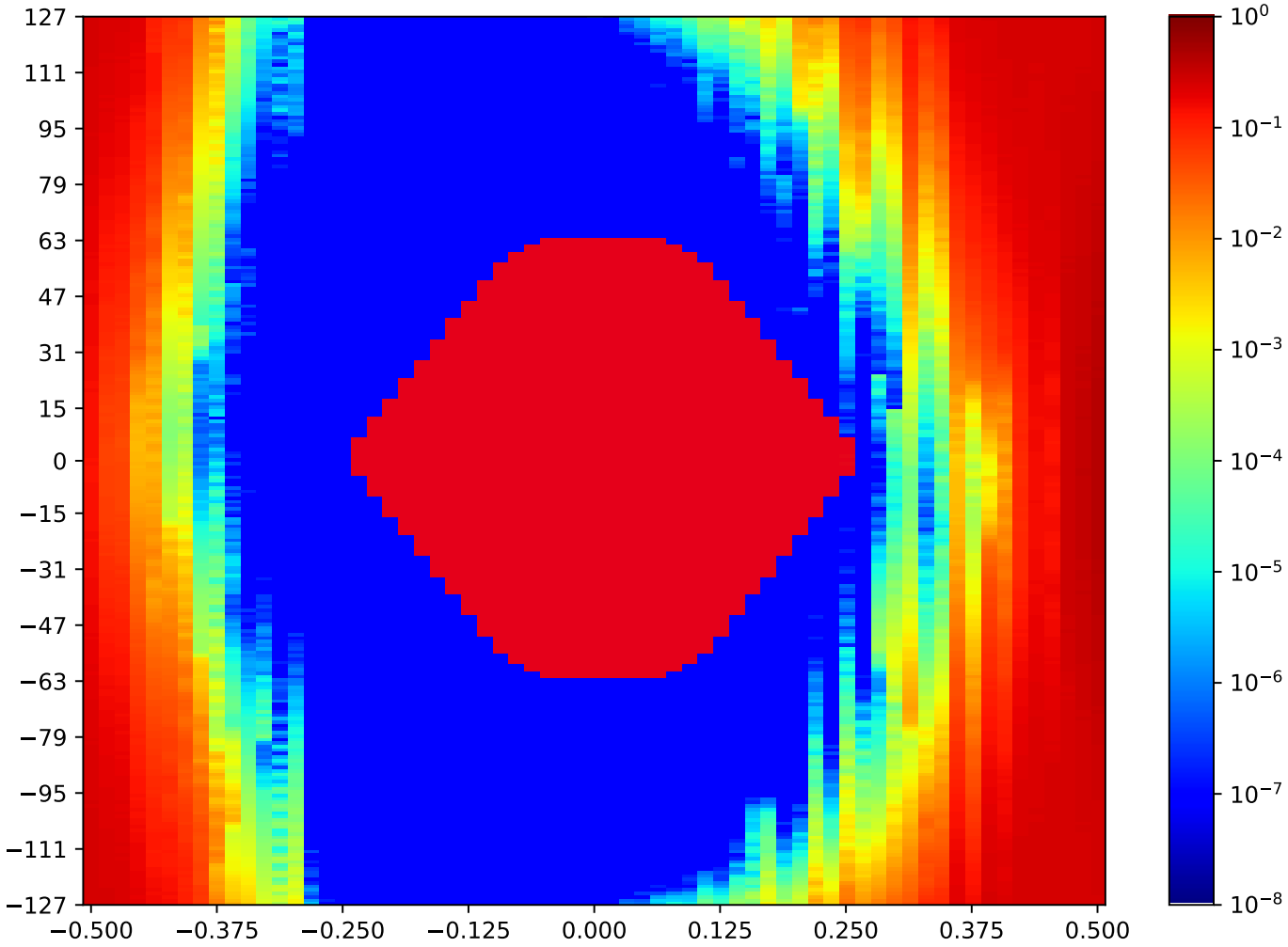


Figure 4.30: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.4 MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Table 4.28: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:58:29		2018-Sep-27 16:58:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8619	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

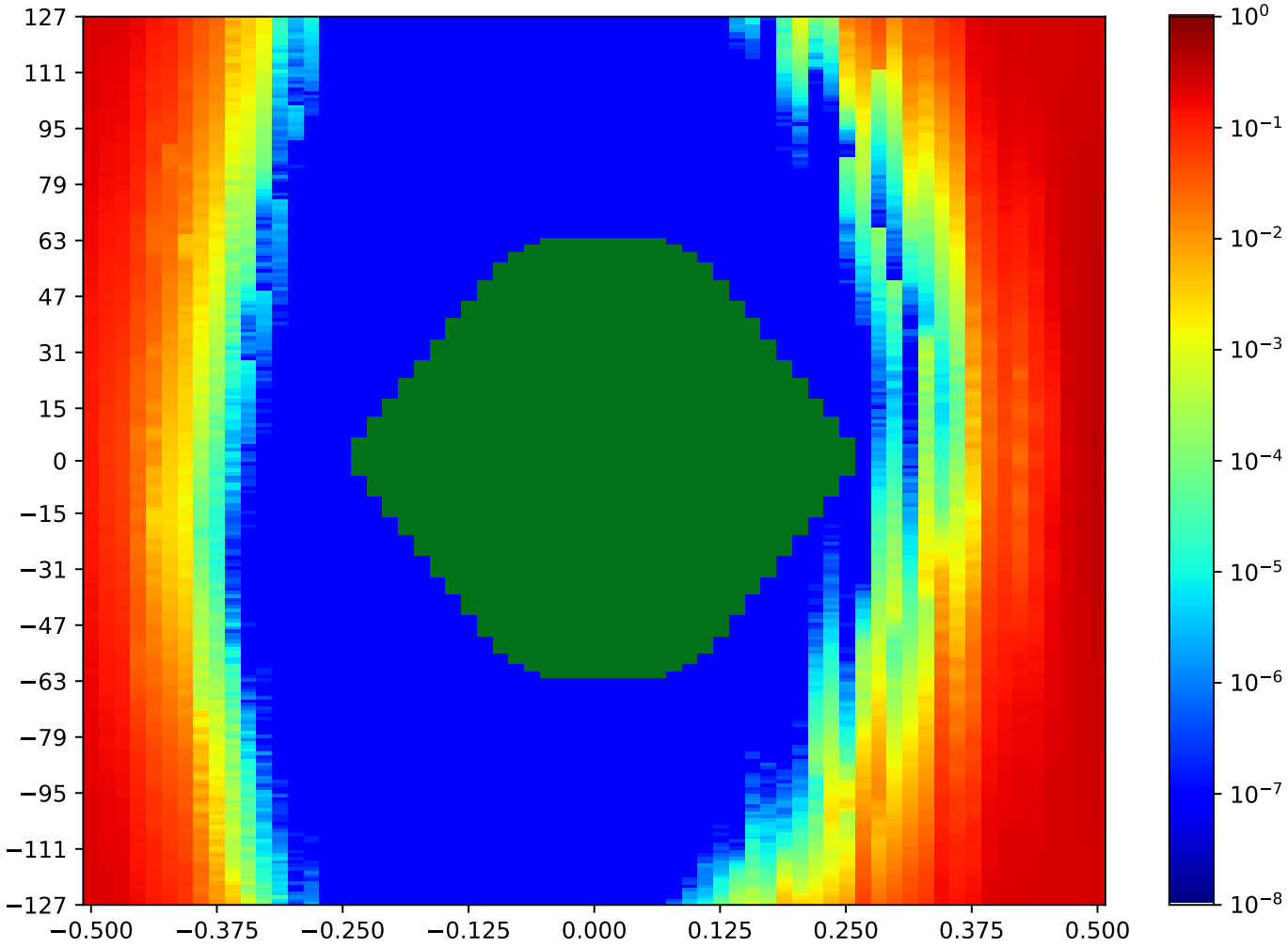


Figure 4.31: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.5 MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Table 4.29: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:01:13		2018-Sep-27 17:01:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8603	45	69.23%	229	88.63%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

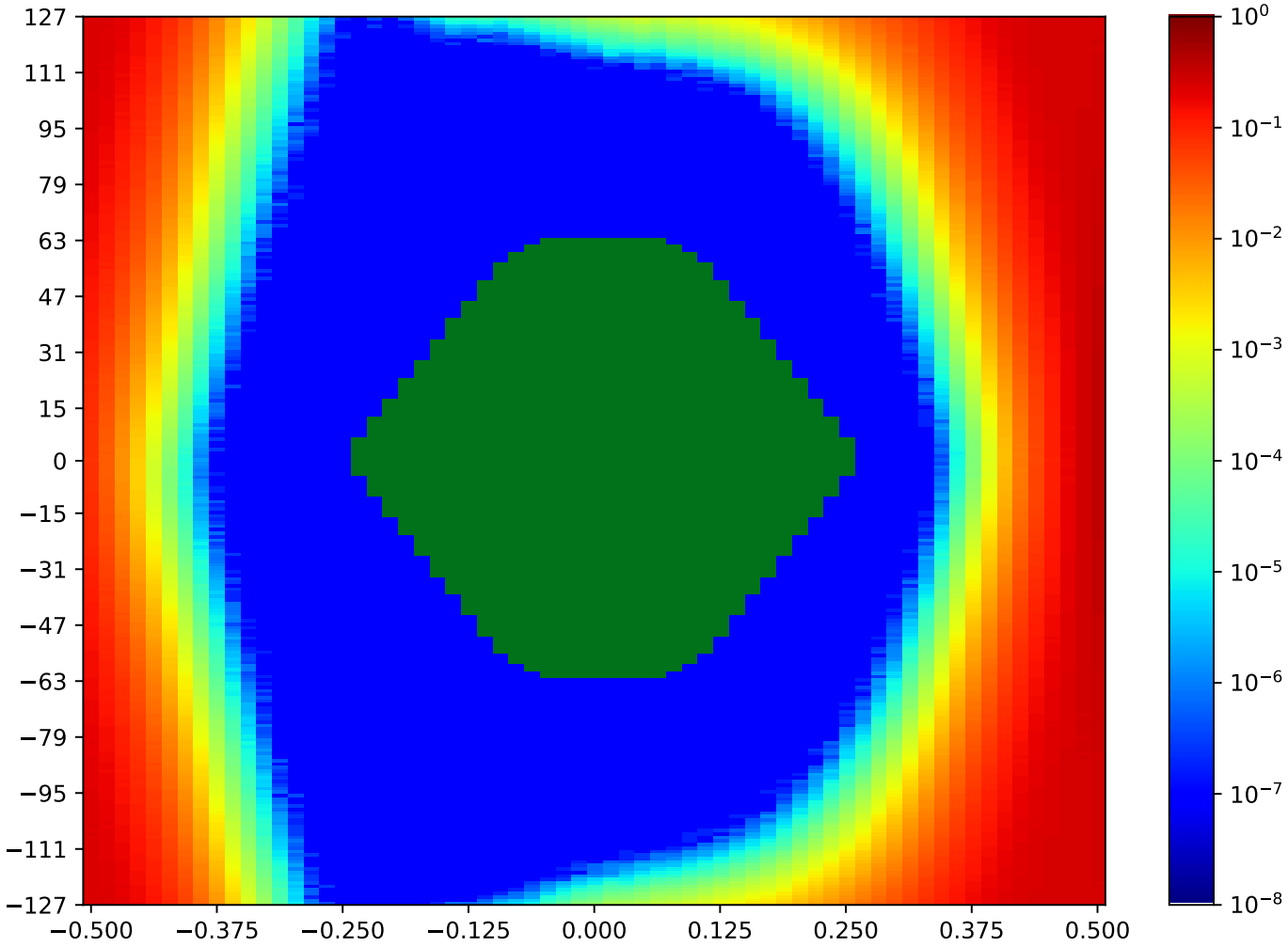


Figure 4.32: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.6 MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Table 4.30: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:58:09		2018-Sep-27 16:58:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9072	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

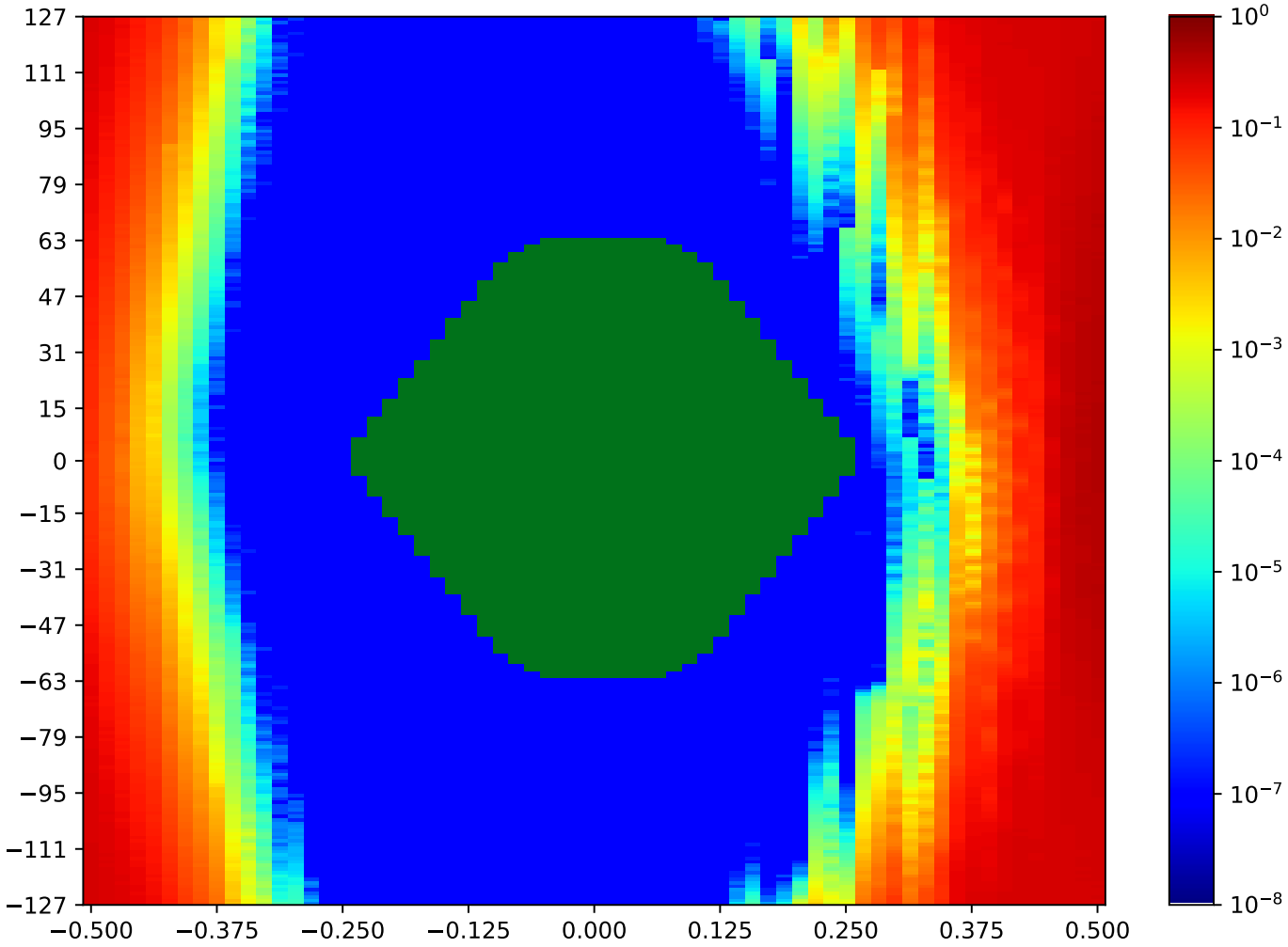


Figure 4.33: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.7 MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Table 4.31: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:01:58		2018-Sep-27 17:02:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8482	45	69.23%	221	86.67%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

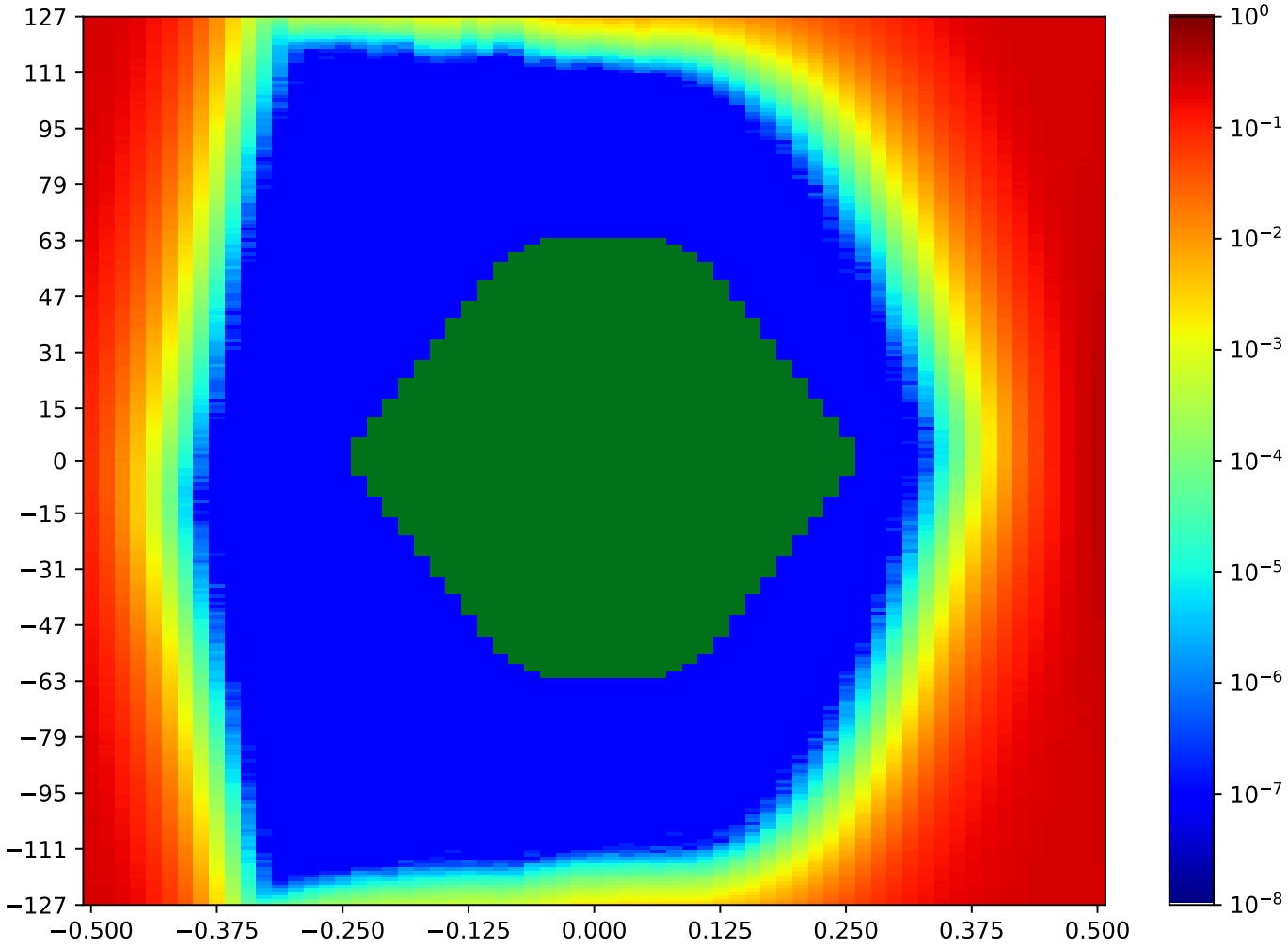


Figure 4.34: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.8 MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Table 4.32: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:58:49		2018-Sep-27 16:59:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9524	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

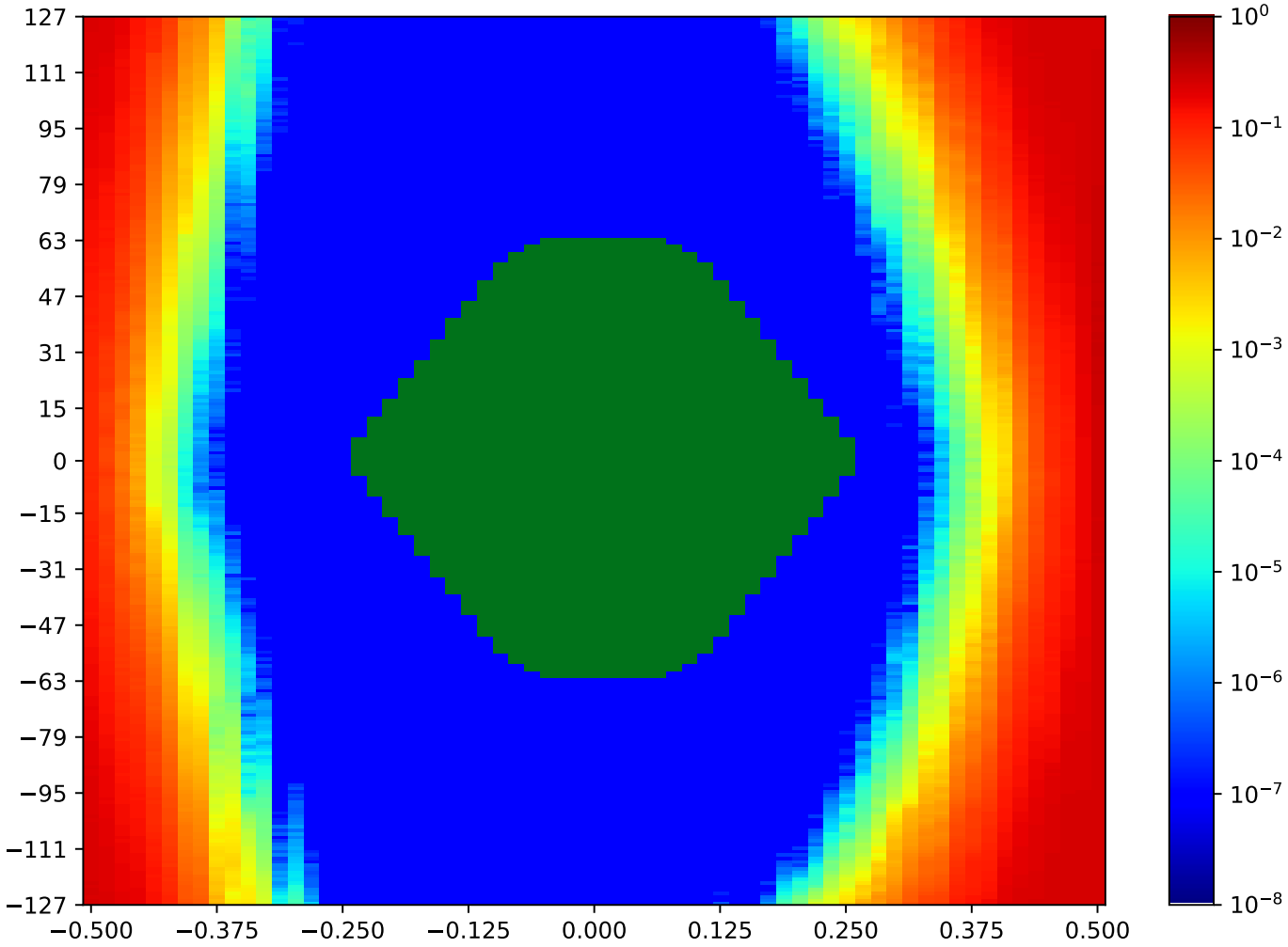


Figure 4.35: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.9 MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Table 4.33: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:01:37		2018-Sep-27 17:01:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9207	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

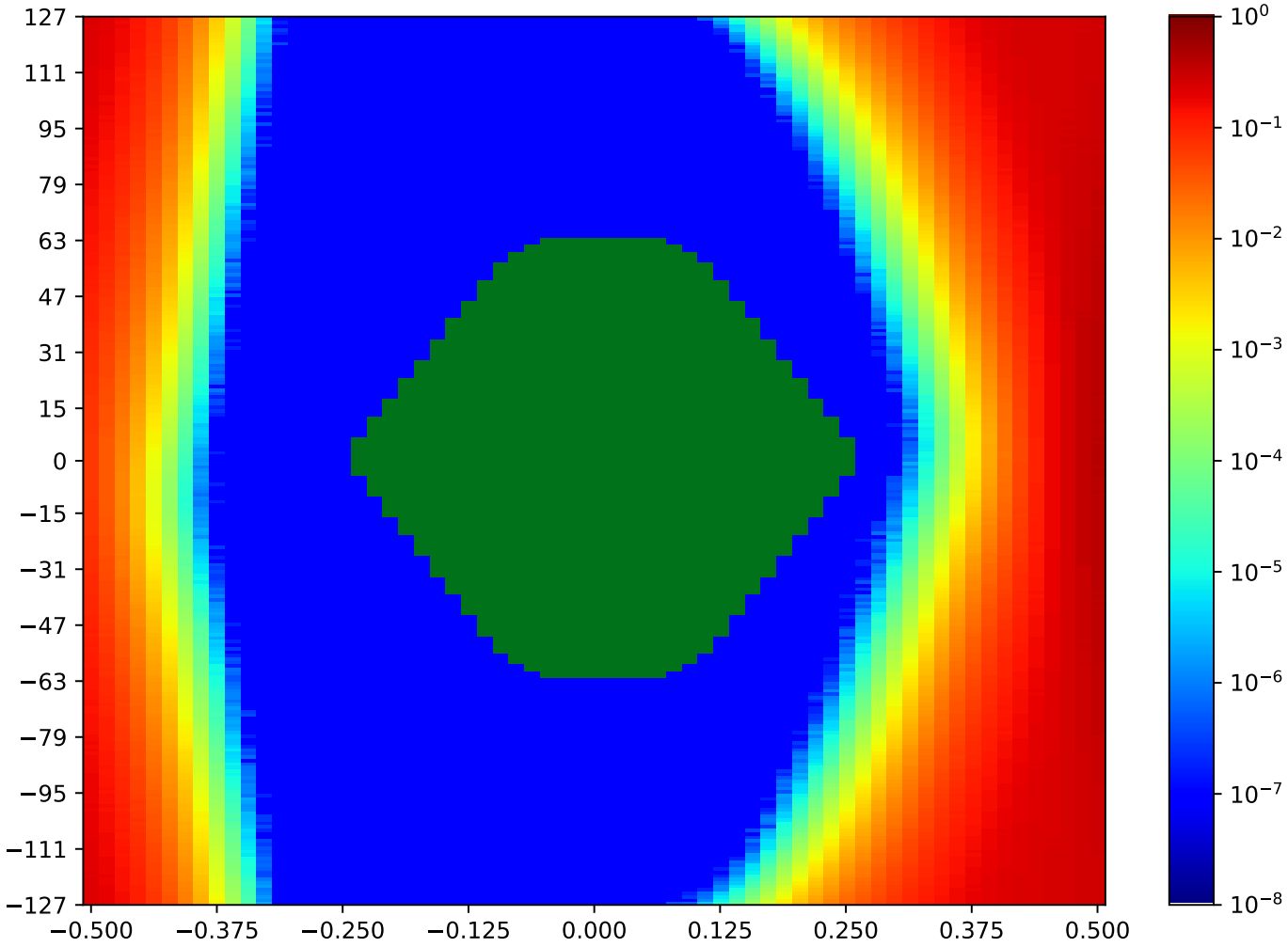


Figure 4.36: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.10 MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Table 4.34: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:59:30		2018-Sep-27 16:59:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9424	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

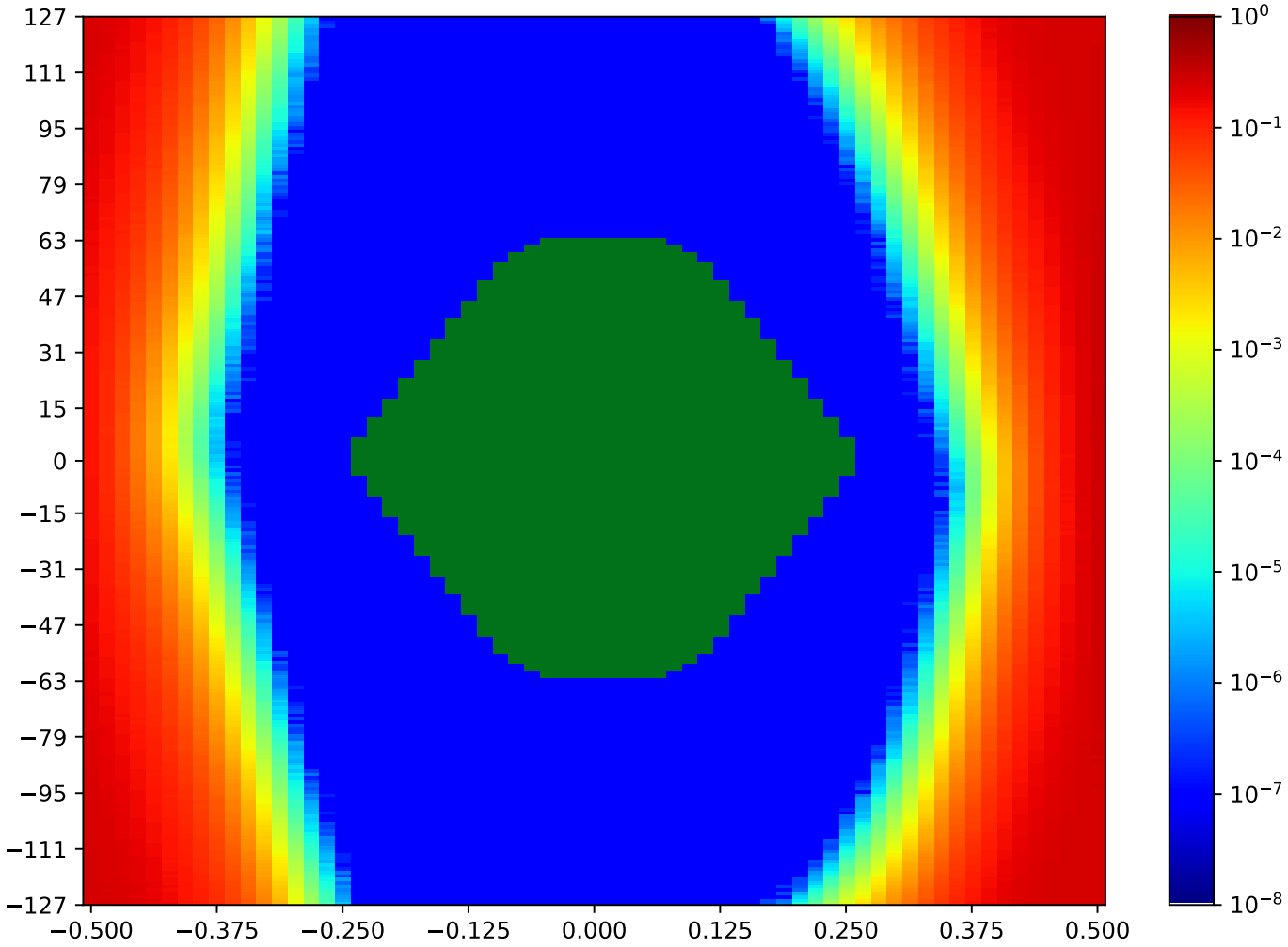


Figure 4.37: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.11 MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Table 4.35: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:00:52		2018-Sep-27 17:01:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9248	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

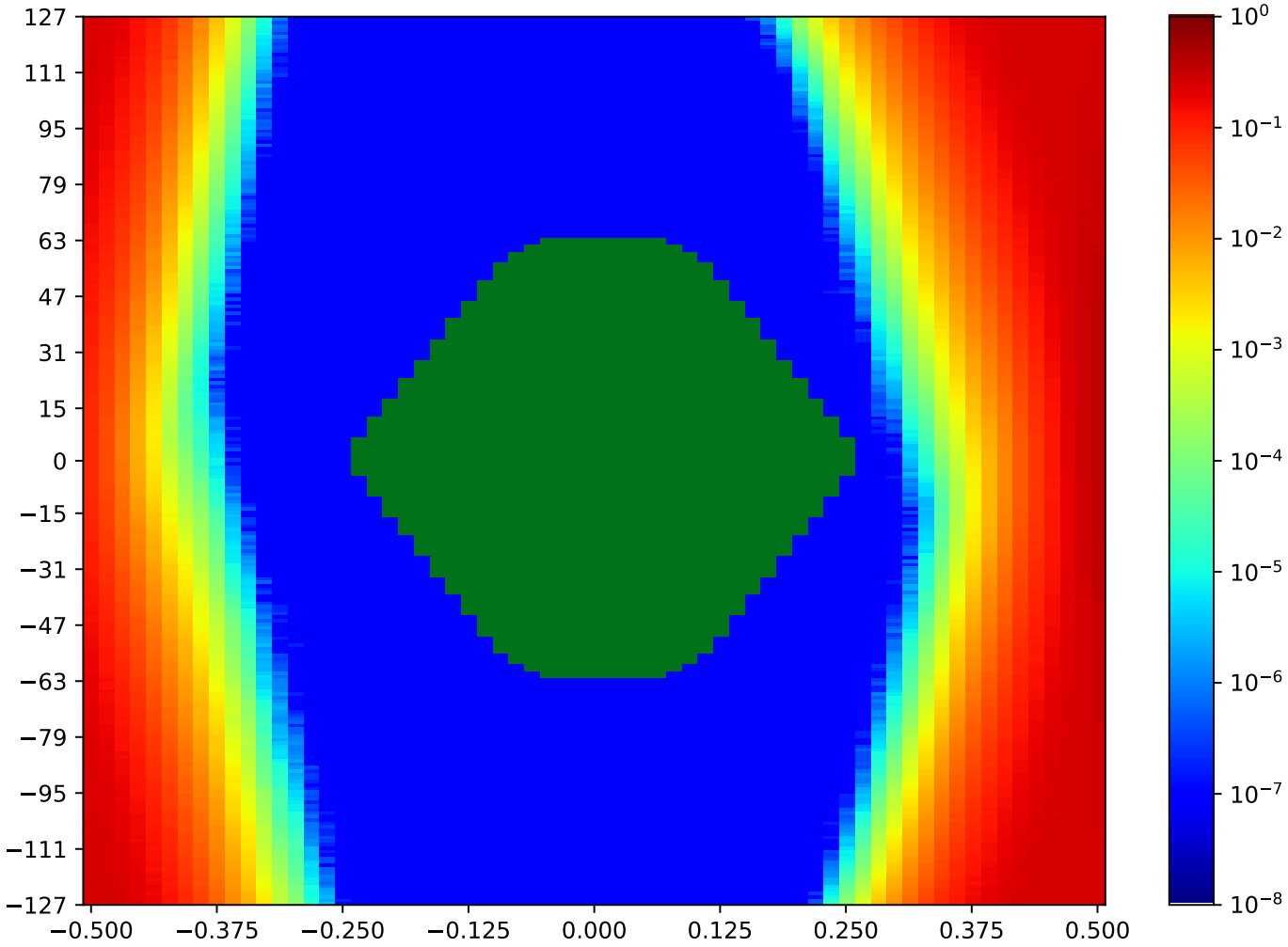


Figure 4.38: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.3.12 MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Table 4.36: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:00:32		2018-Sep-27 17:00:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9712	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

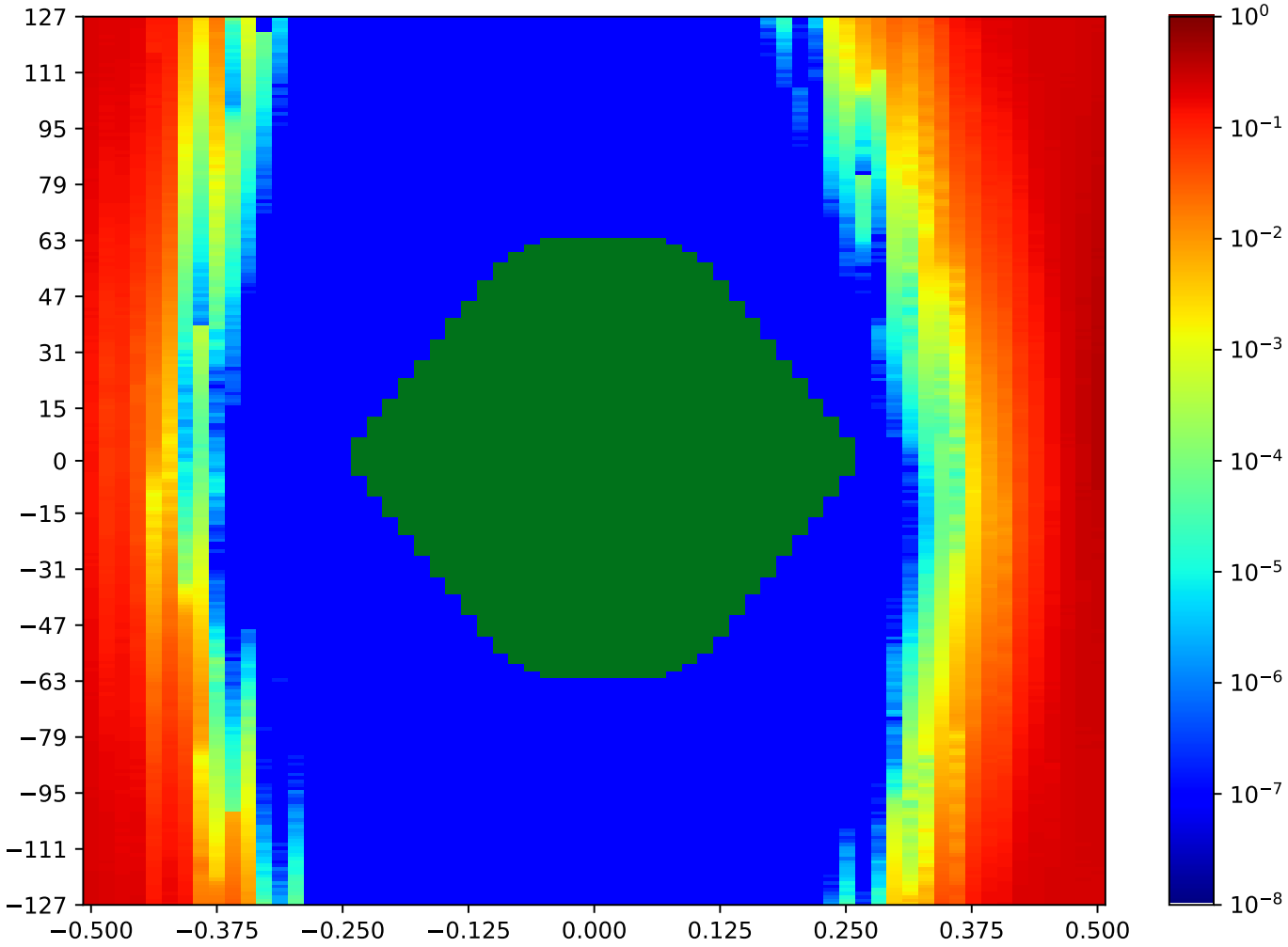


Figure 4.39: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4 MSP_C TX4 MSP_A RX7 Minipod Loopback

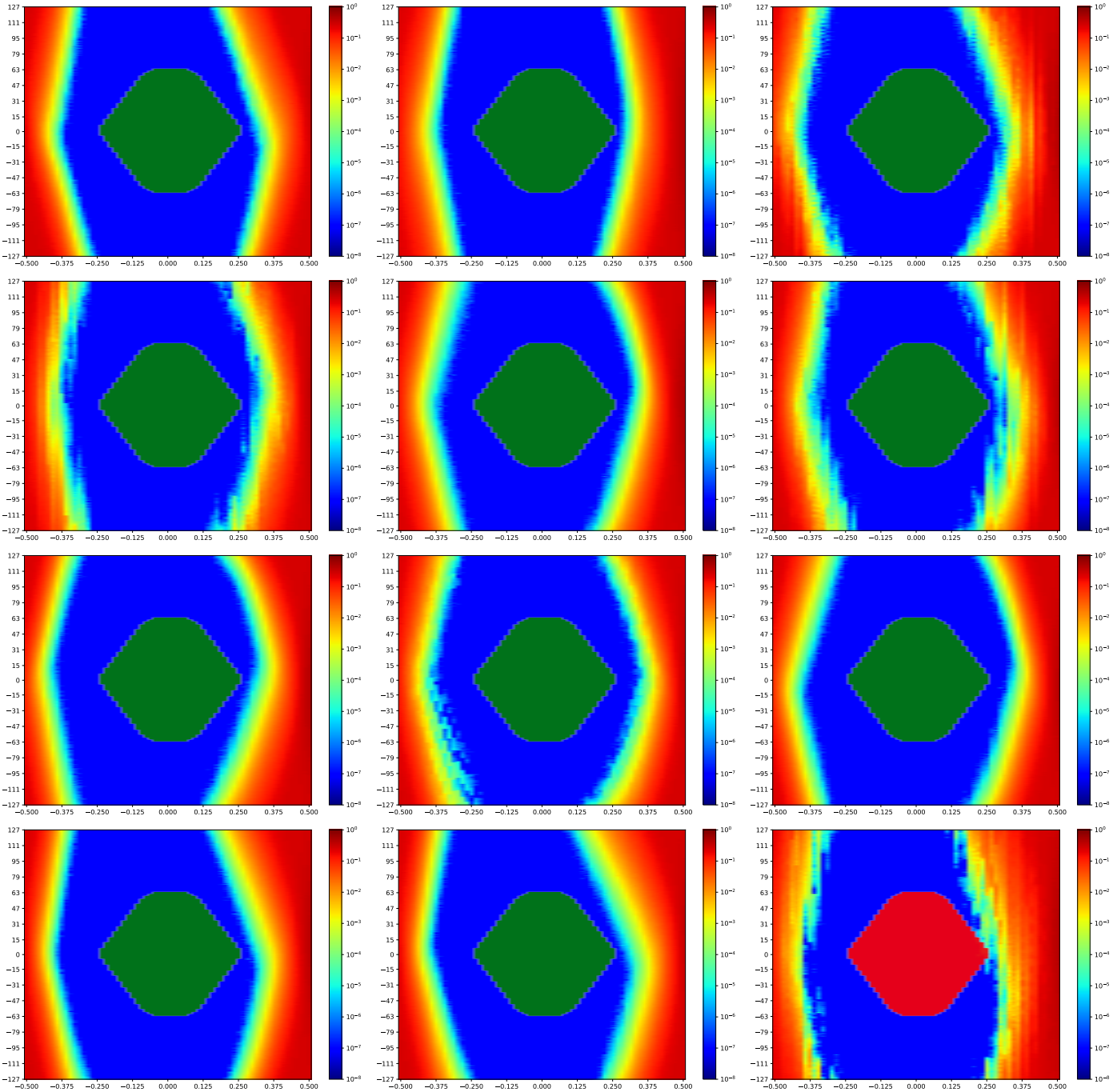


Figure 4.40: MSP_C TX4 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.53.

4.4.1 MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Table 4.37: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:03:19		2018-Sep-27 17:03:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9052	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

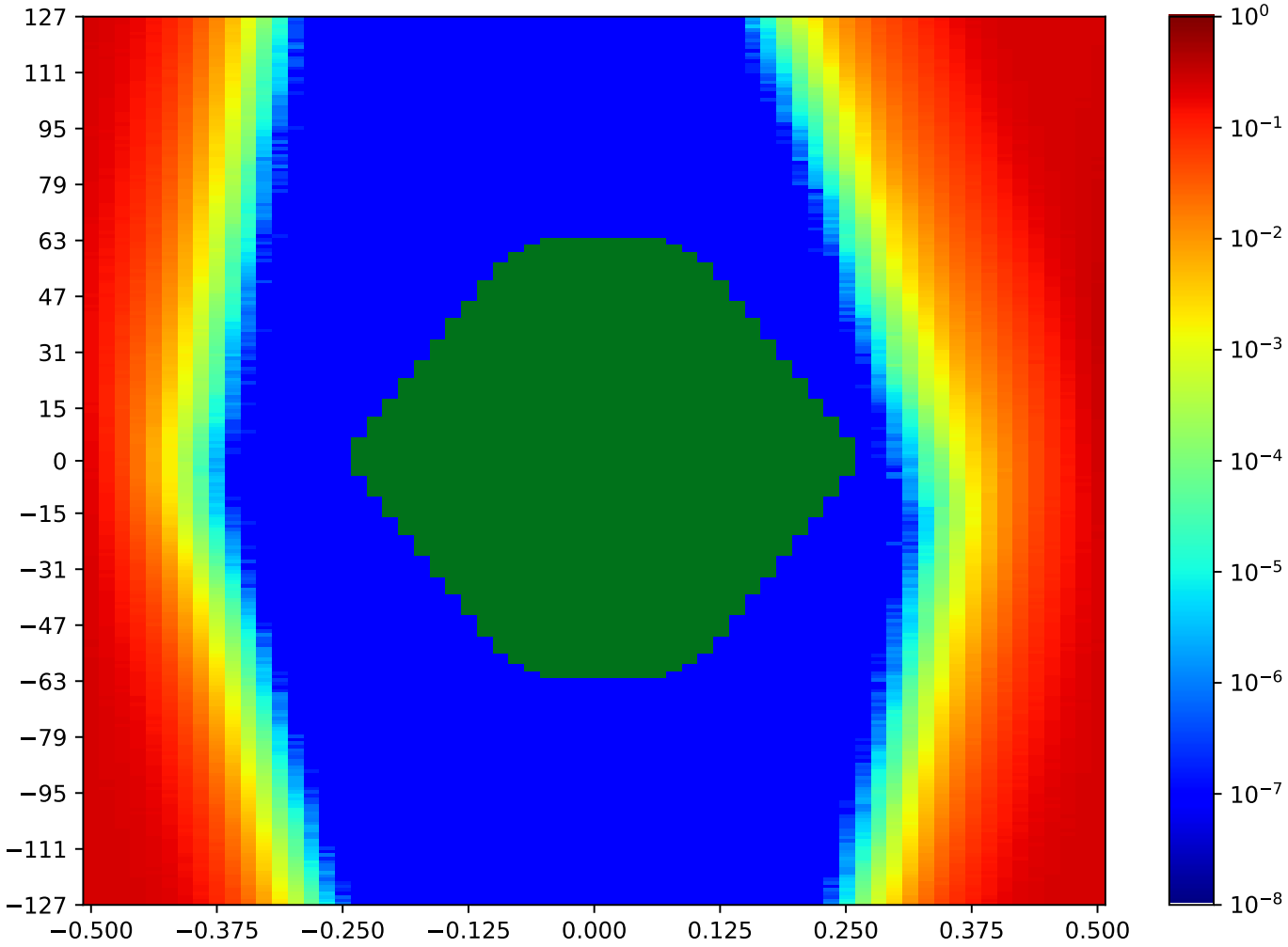


Figure 4.41: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.2 MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Table 4.38: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:02:38		2018-Sep-27 17:02:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8861	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

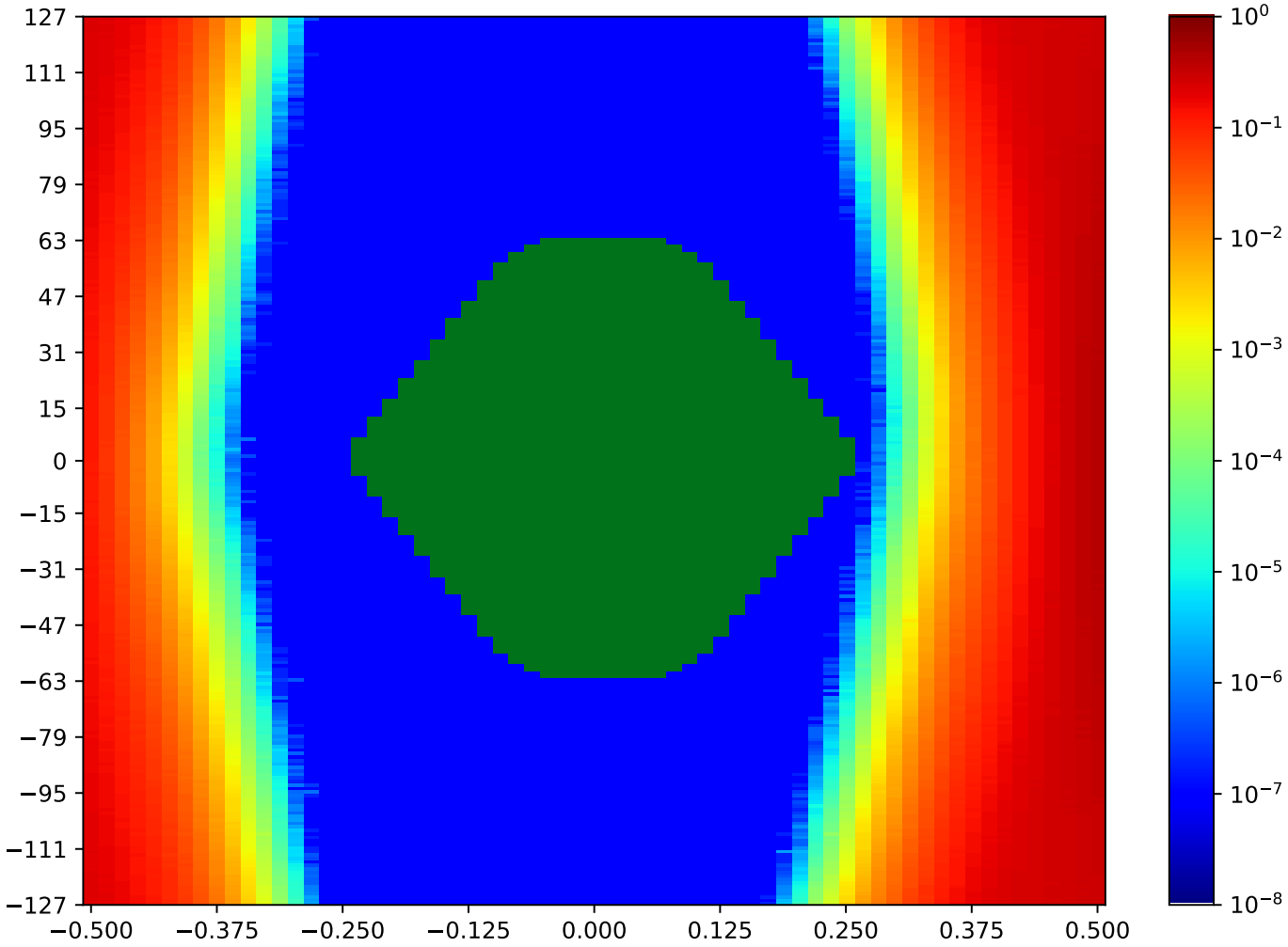


Figure 4.42: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.3 MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Table 4.39: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:04:20		2018-Sep-27 17:04:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8557	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

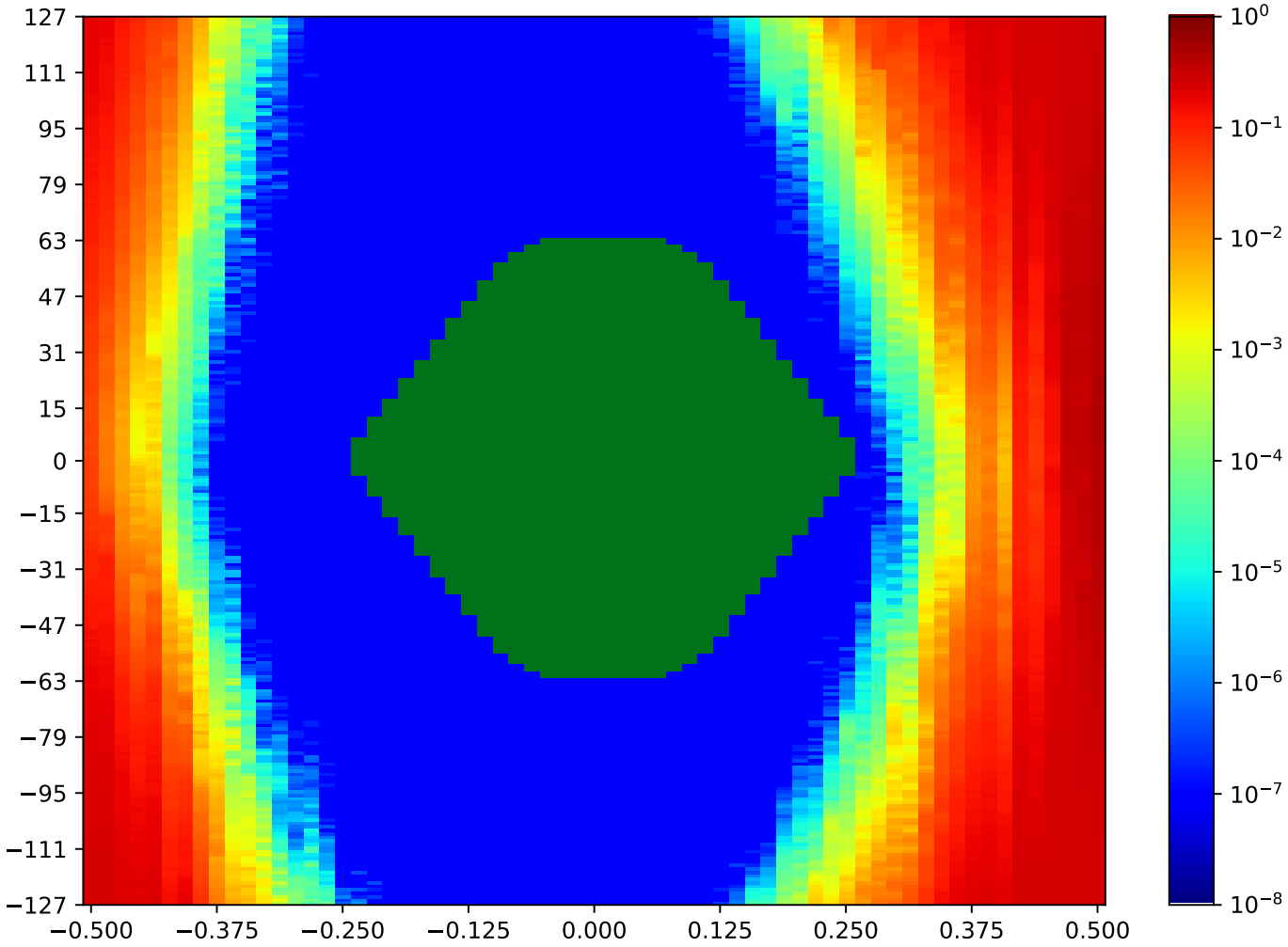


Figure 4.43: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.4 MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Table 4.40: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:02:18		2018-Sep-27 17:02:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8776	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

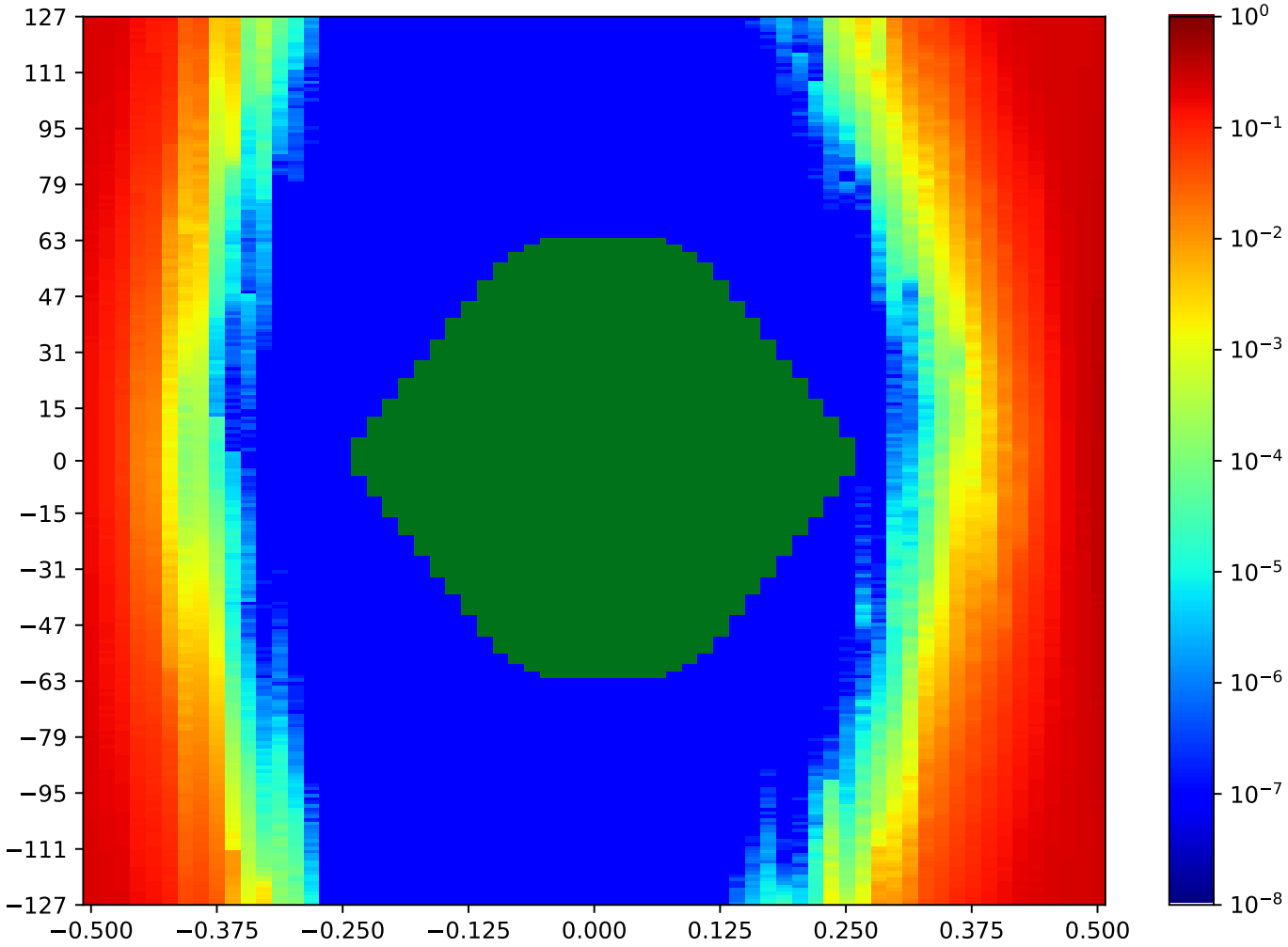


Figure 4.44: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.5 MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Table 4.41: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:05:21		2018-Sep-27 17:05:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8511	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

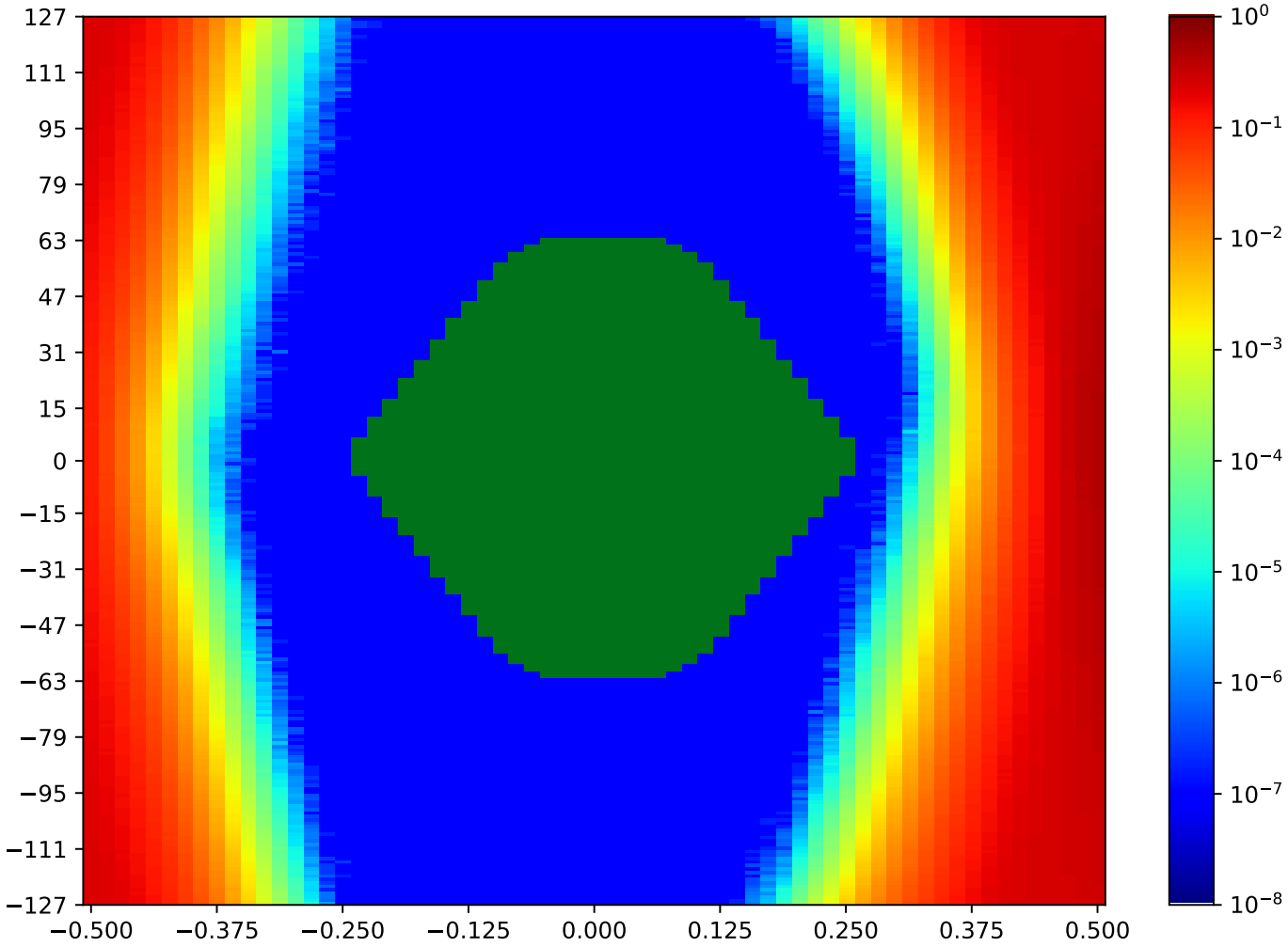


Figure 4.45: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.6 MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Table 4.42: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:02:59		2018-Sep-27 17:03:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7992	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

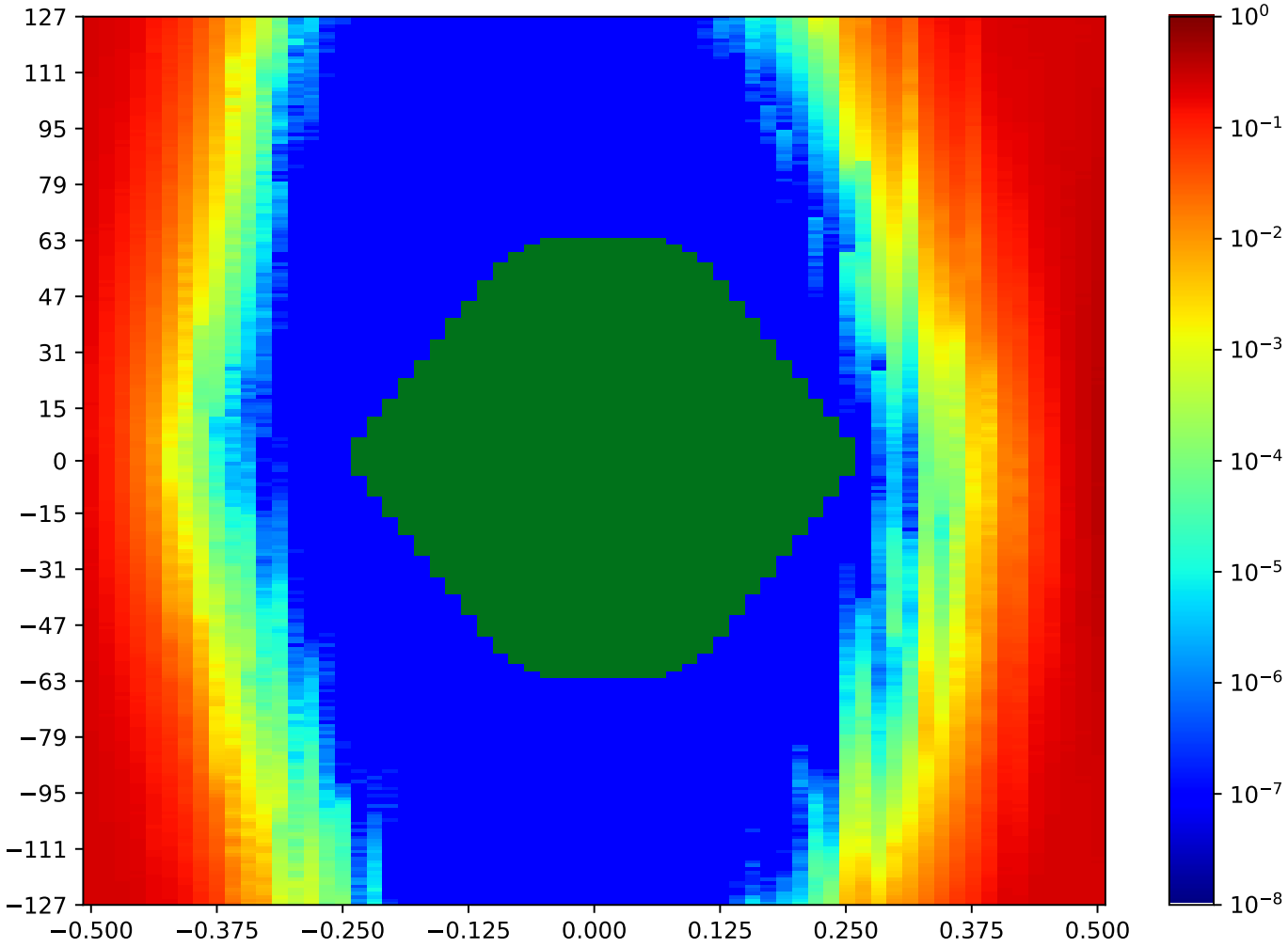


Figure 4.46: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.7 MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Table 4.43: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:06:05		2018-Sep-27 17:06:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9053	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

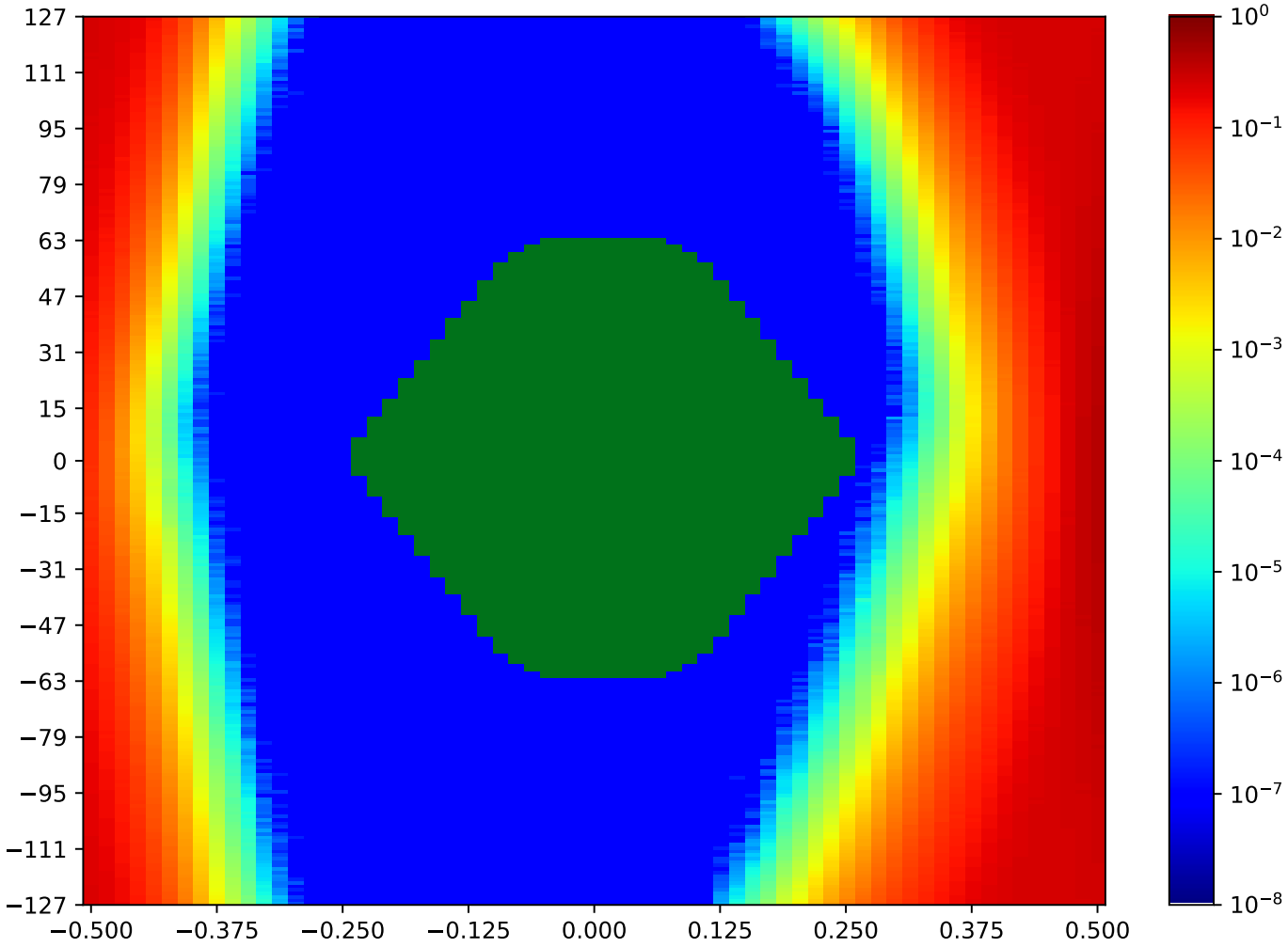


Figure 4.47: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.8 MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Table 4.44: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:03:40		2018-Sep-27 17:04:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9053	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

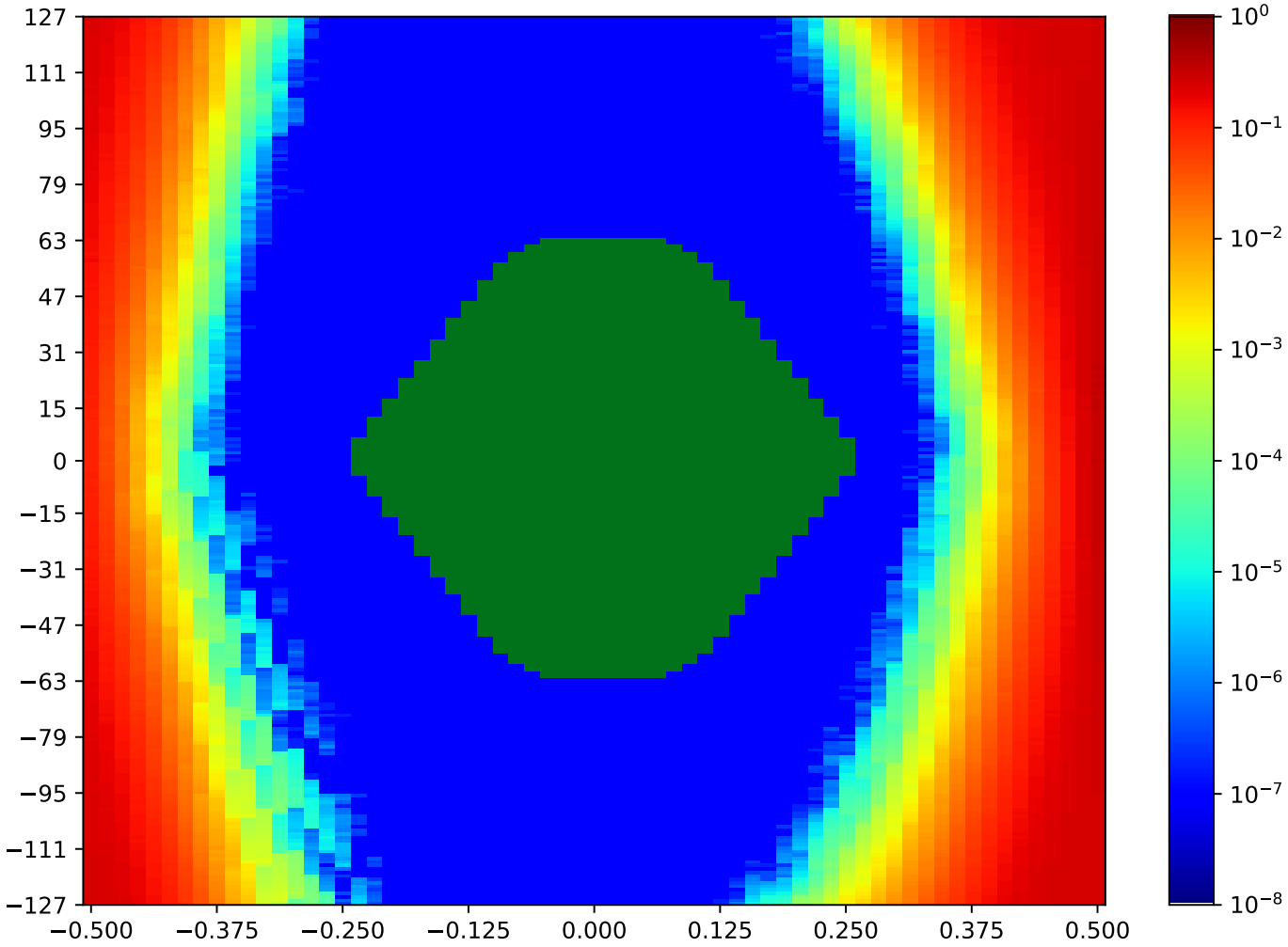


Figure 4.48: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.9 MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Table 4.45: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:05:45		2018-Sep-27 17:06:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9389	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

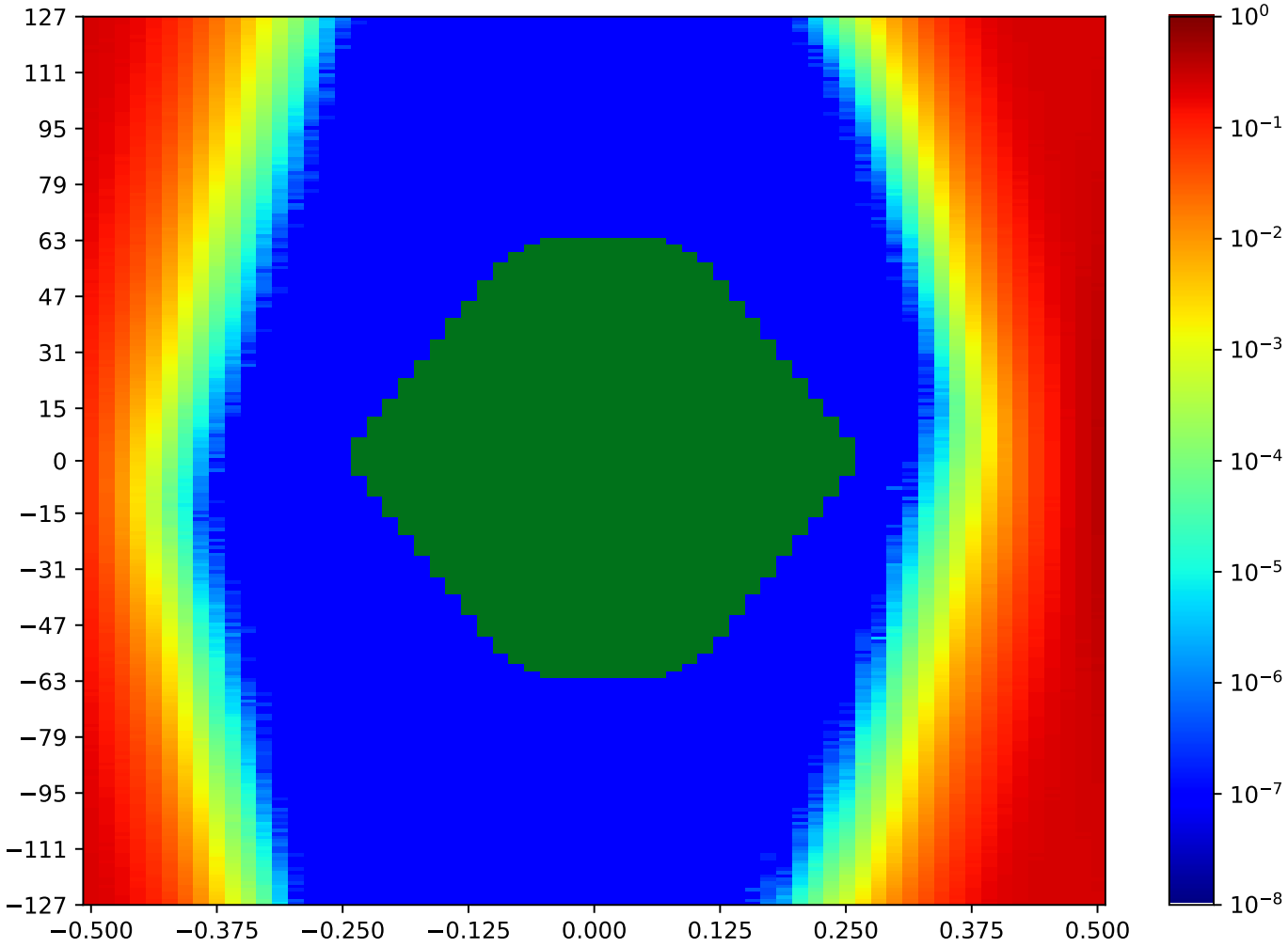


Figure 4.49: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.10 MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Table 4.46: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:04:00		2018-Sep-27 17:04:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9187	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

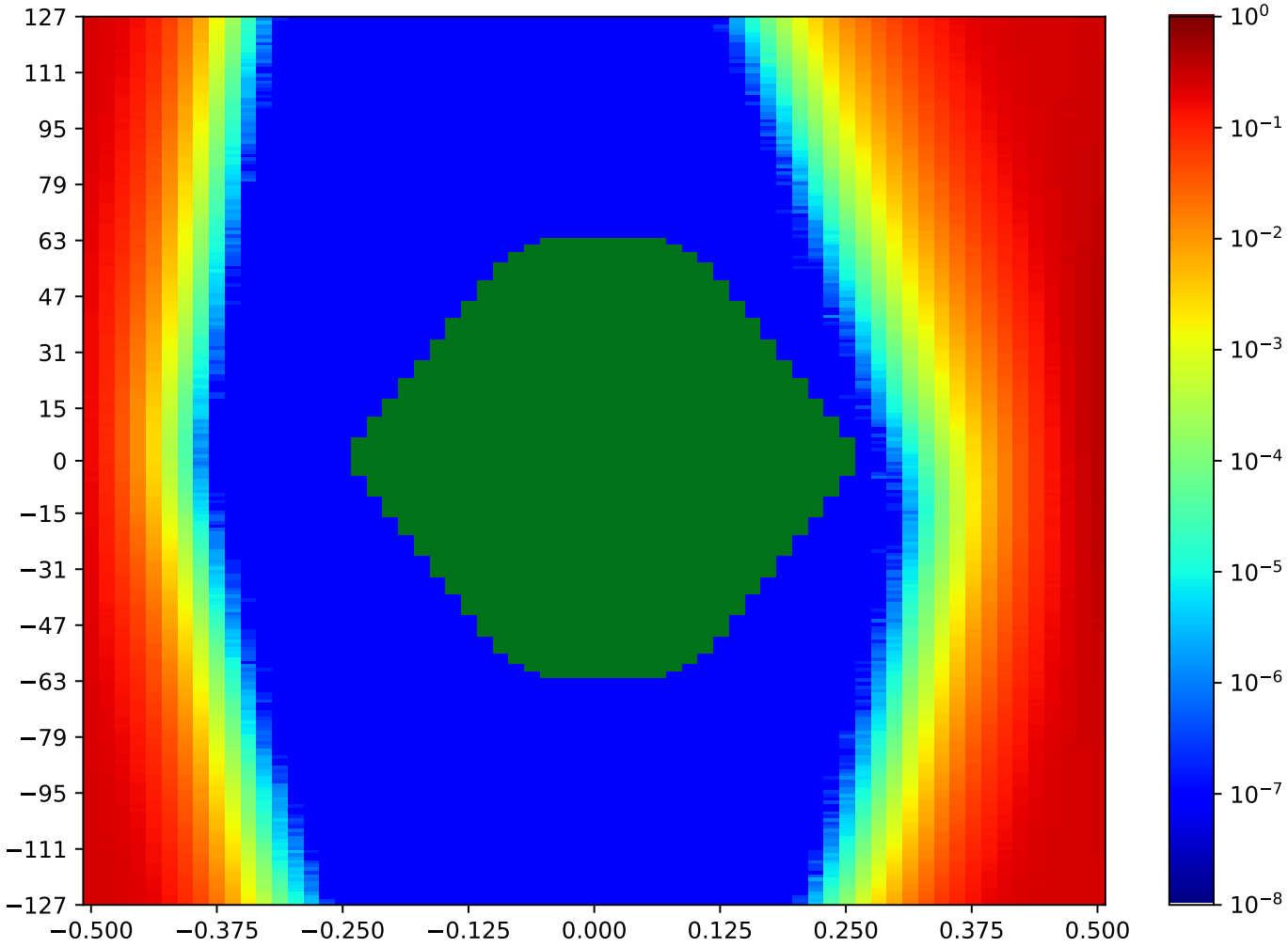


Figure 4.50: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.11 MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Table 4.47: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:05:01		2018-Sep-27 17:05:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8629	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

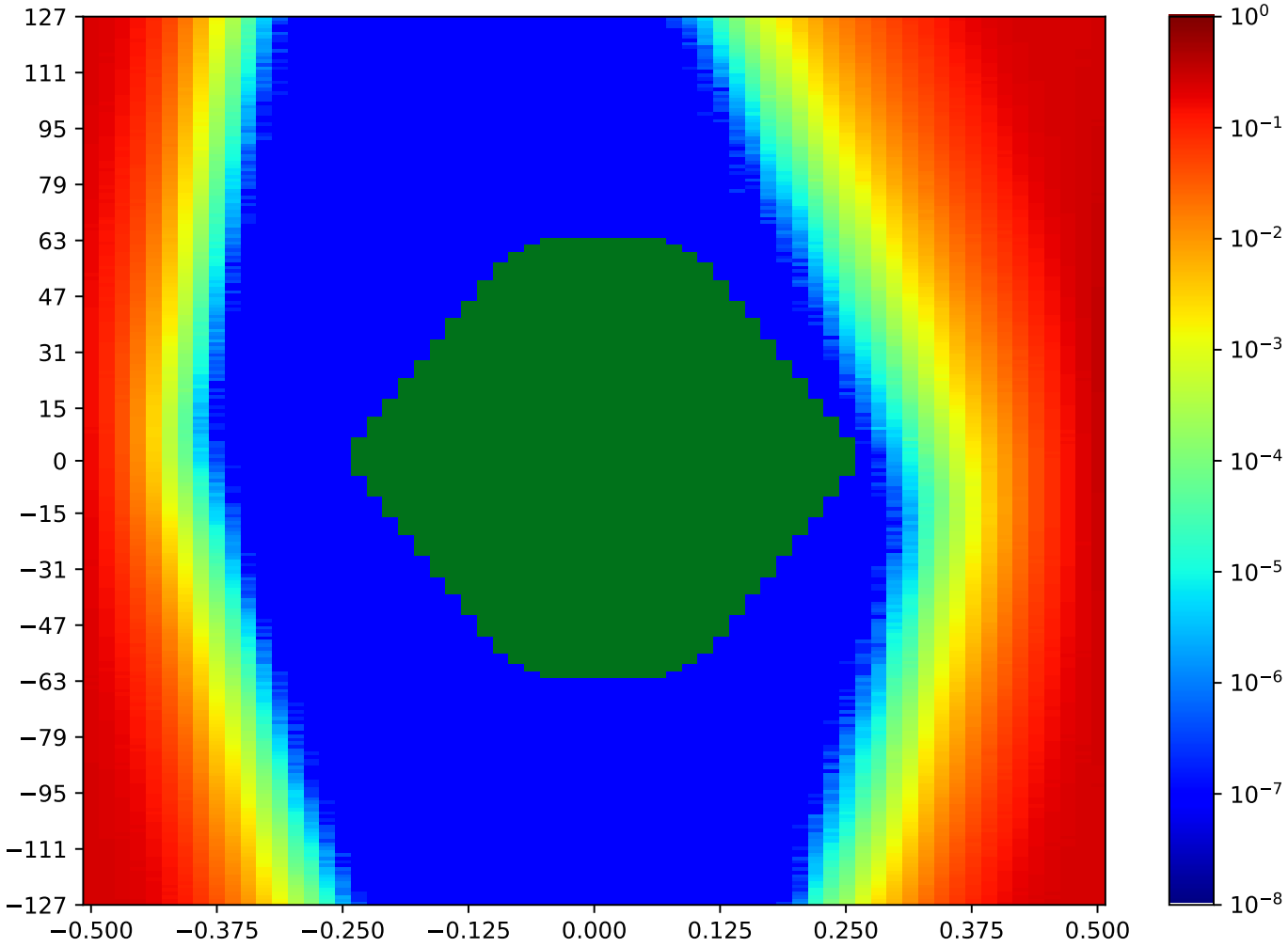


Figure 4.51: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.4.12 MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Table 4.48: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:04:41		2018-Sep-27 17:05:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8902	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

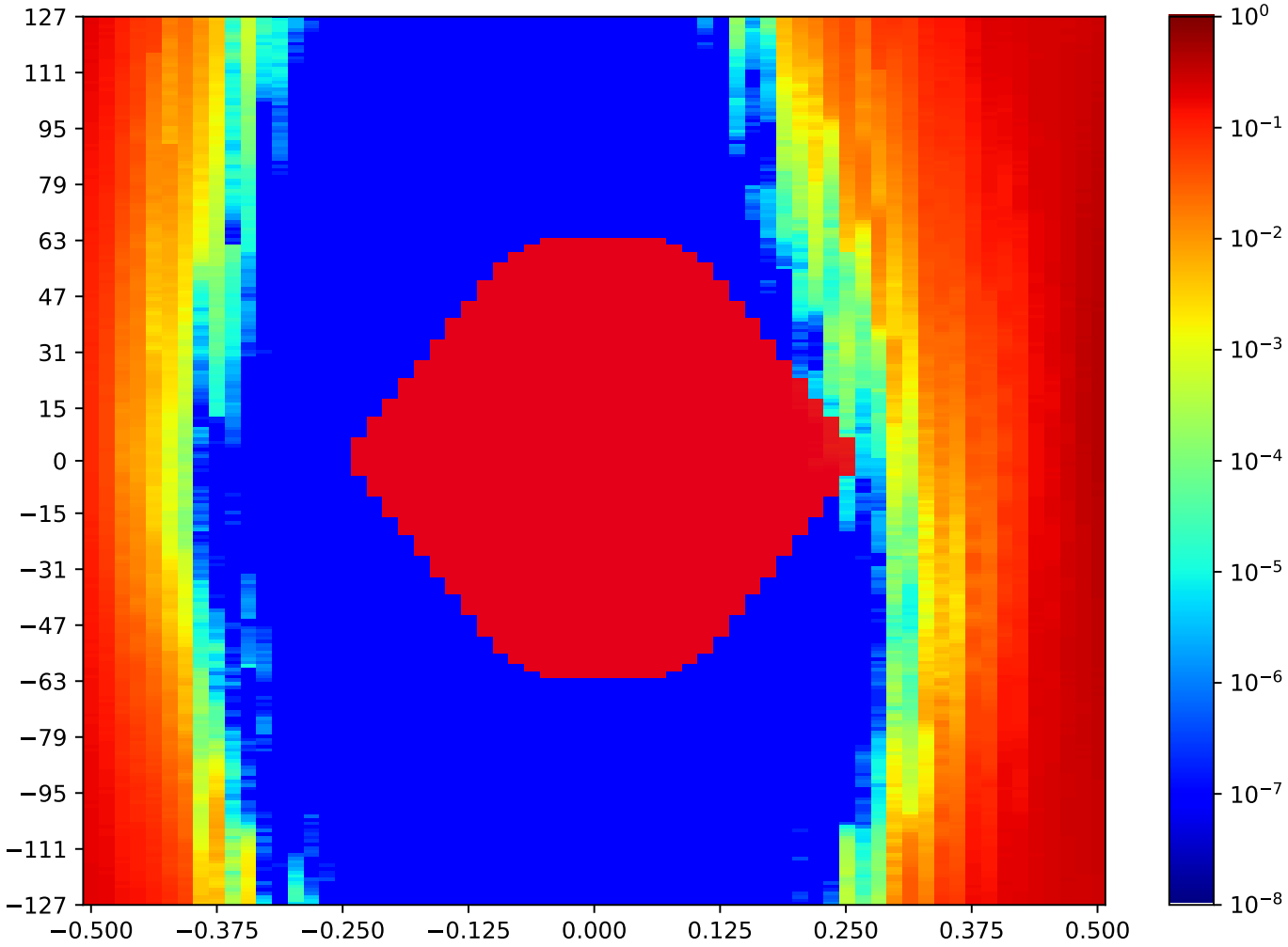


Figure 4.52: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.62.

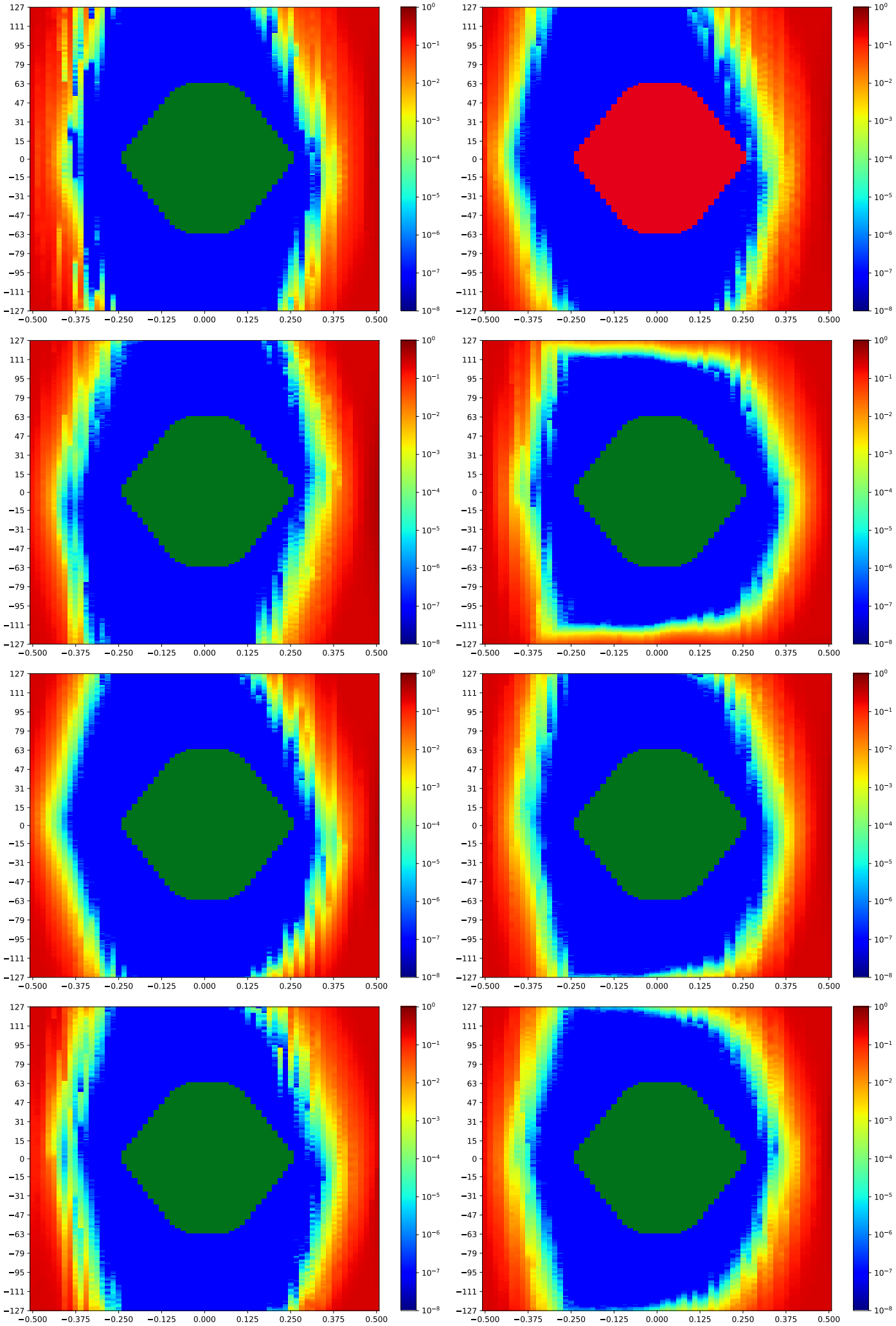


Figure 4.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

4.5.1 TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Table 4.49: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:07:31		2018-Sep-27 17:07:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9257	44	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

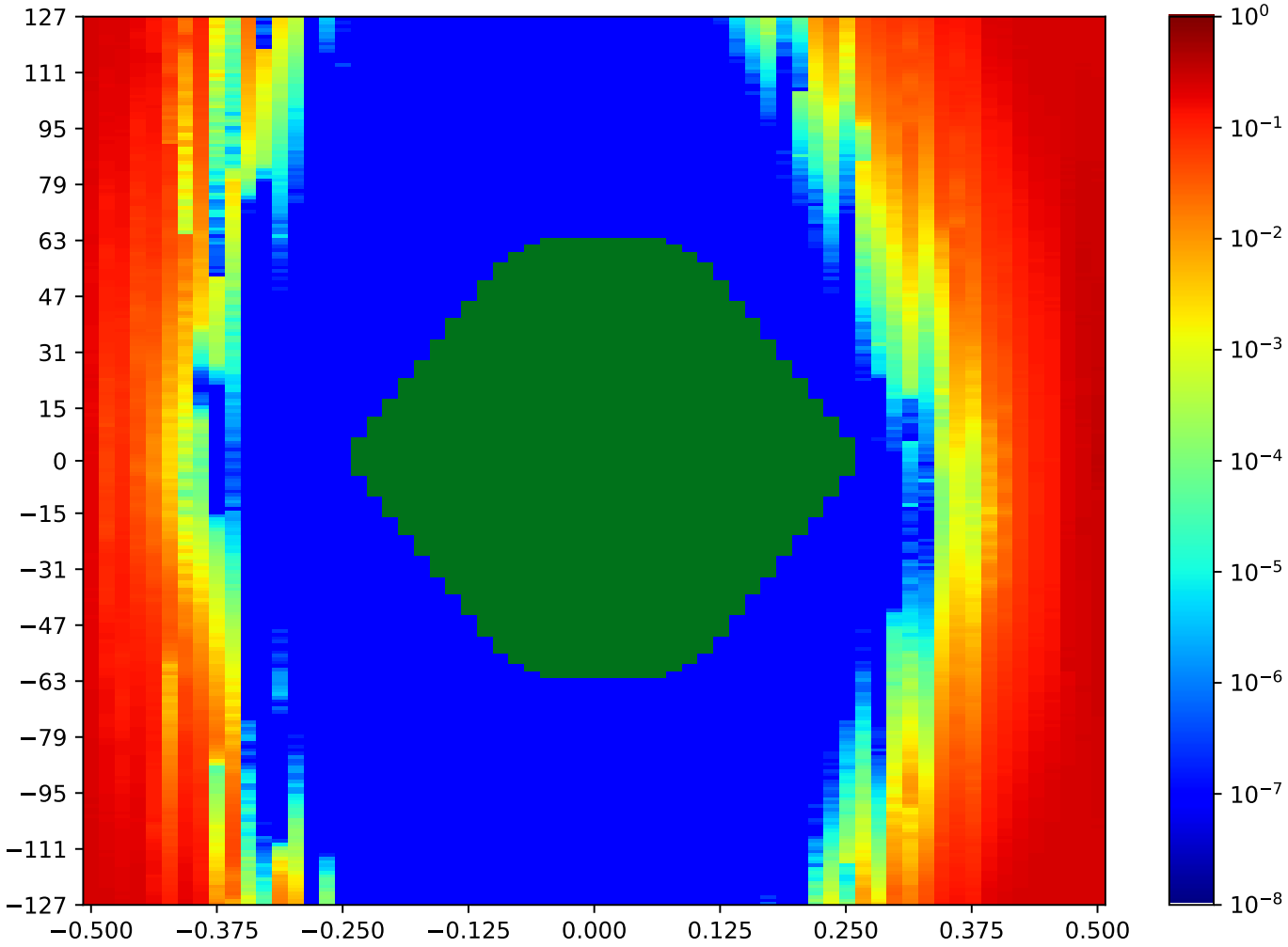


Figure 4.54: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.2 TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Table 4.50: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:06:50		2018-Sep-27 17:07:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8865	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

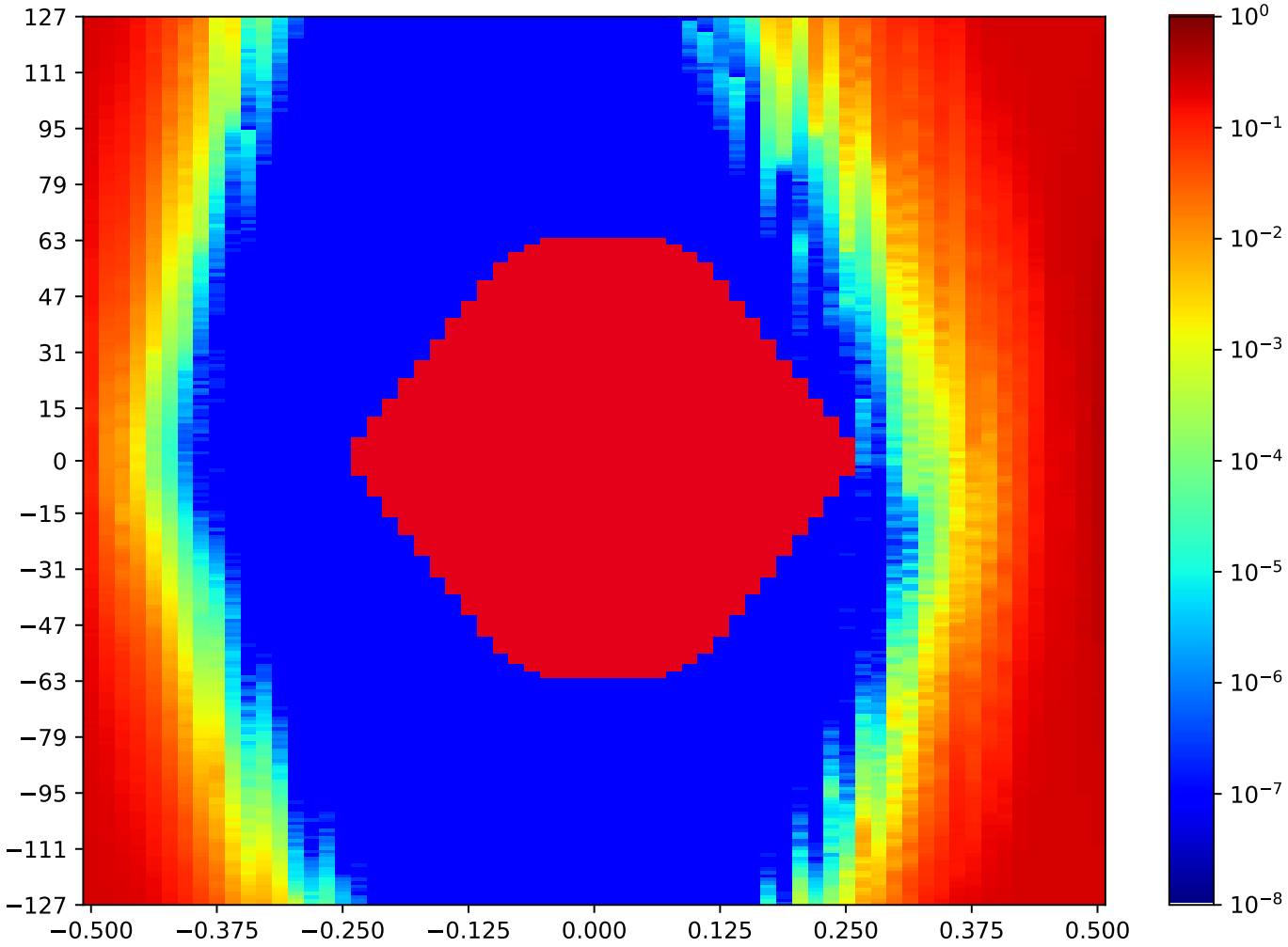


Figure 4.55: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.3 TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Table 4.51: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:08:12		2018-Sep-27 17:08:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8728	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

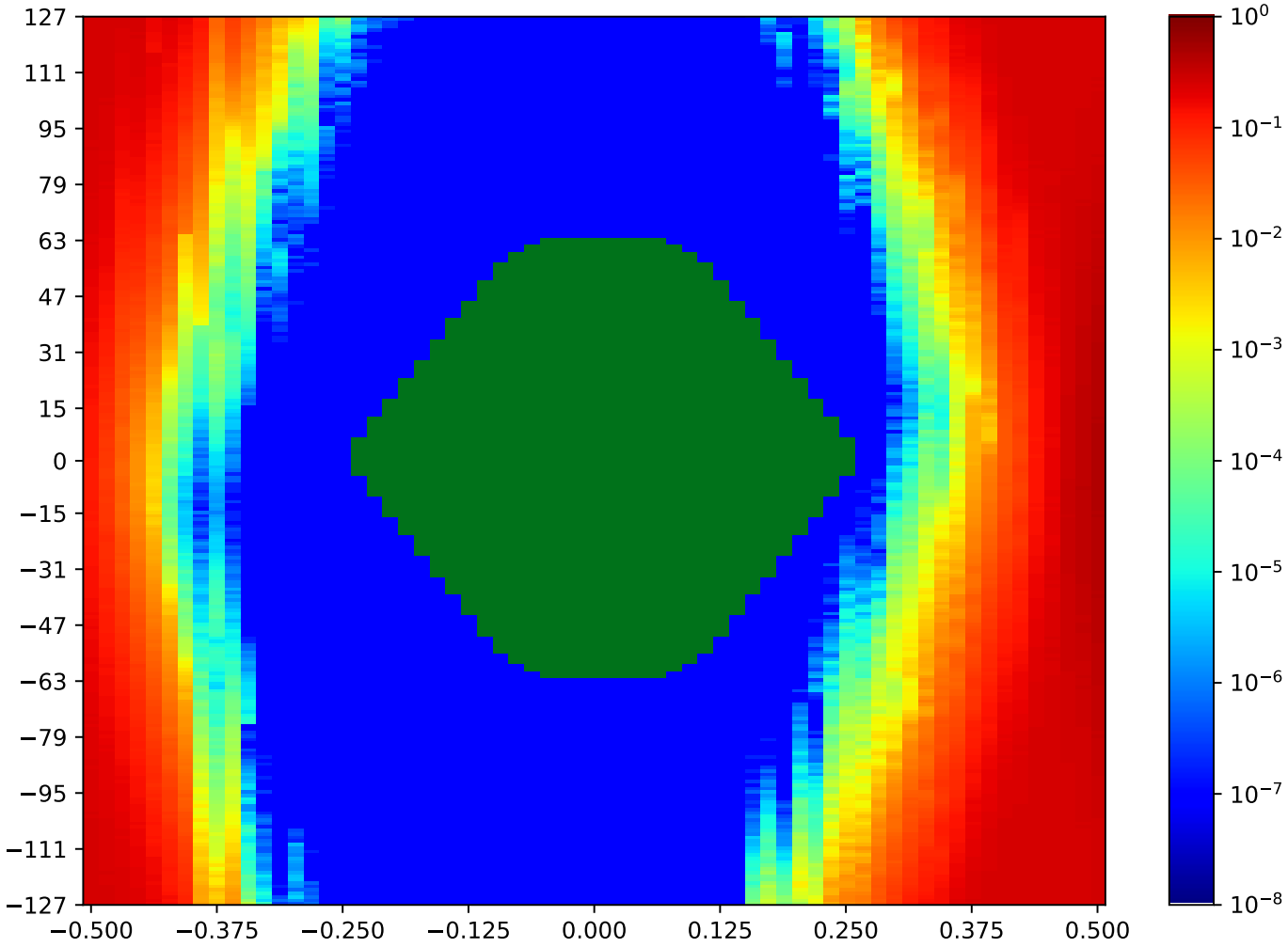


Figure 4.56: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.4 TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Table 4.52: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:07:11		2018-Sep-27 17:07:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7758	43	66.15%	218	85.49%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

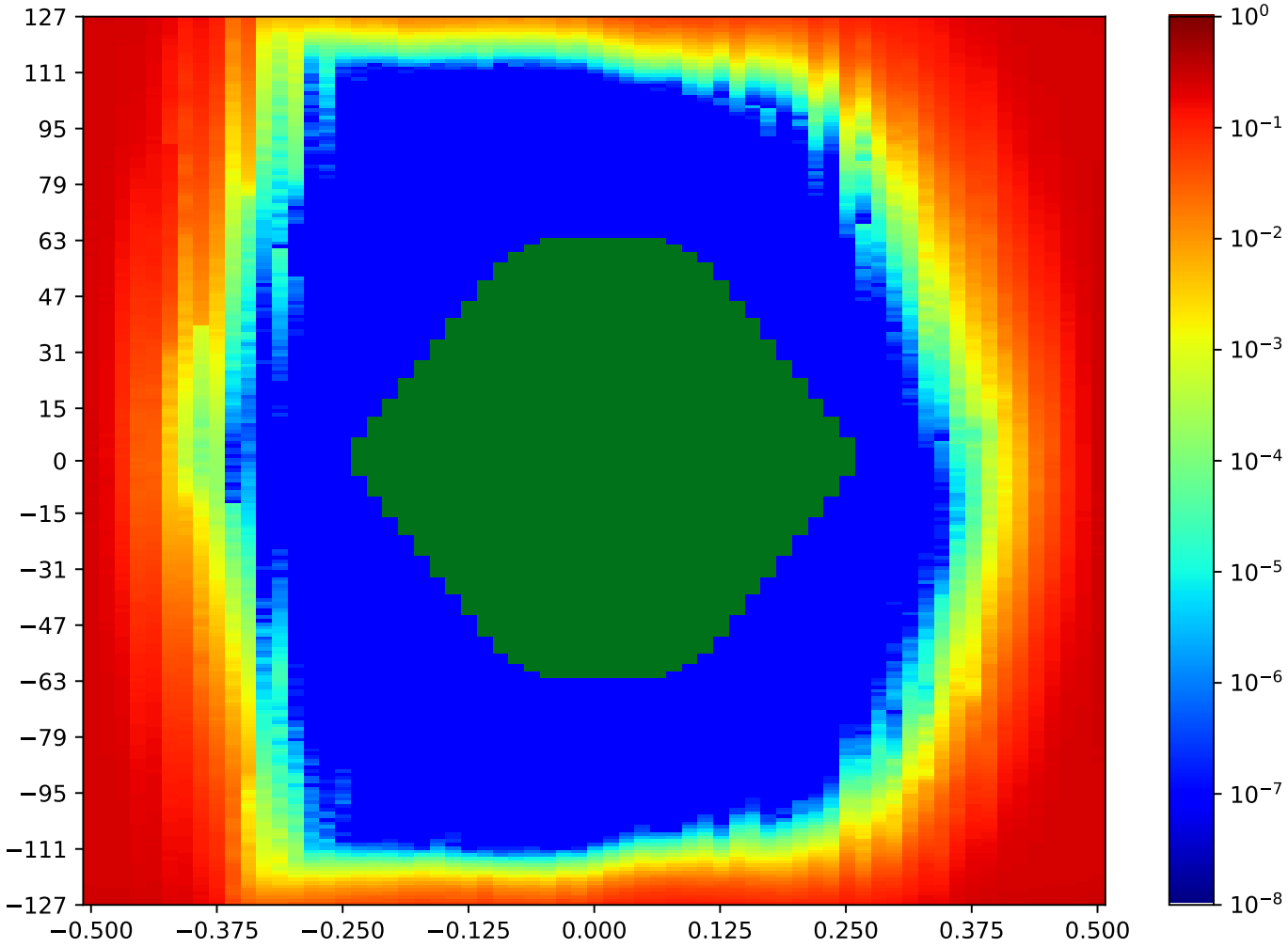


Figure 4.57: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.5 TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Table 4.53: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:08:53		2018-Sep-27 17:09:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9135	45	69.23%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

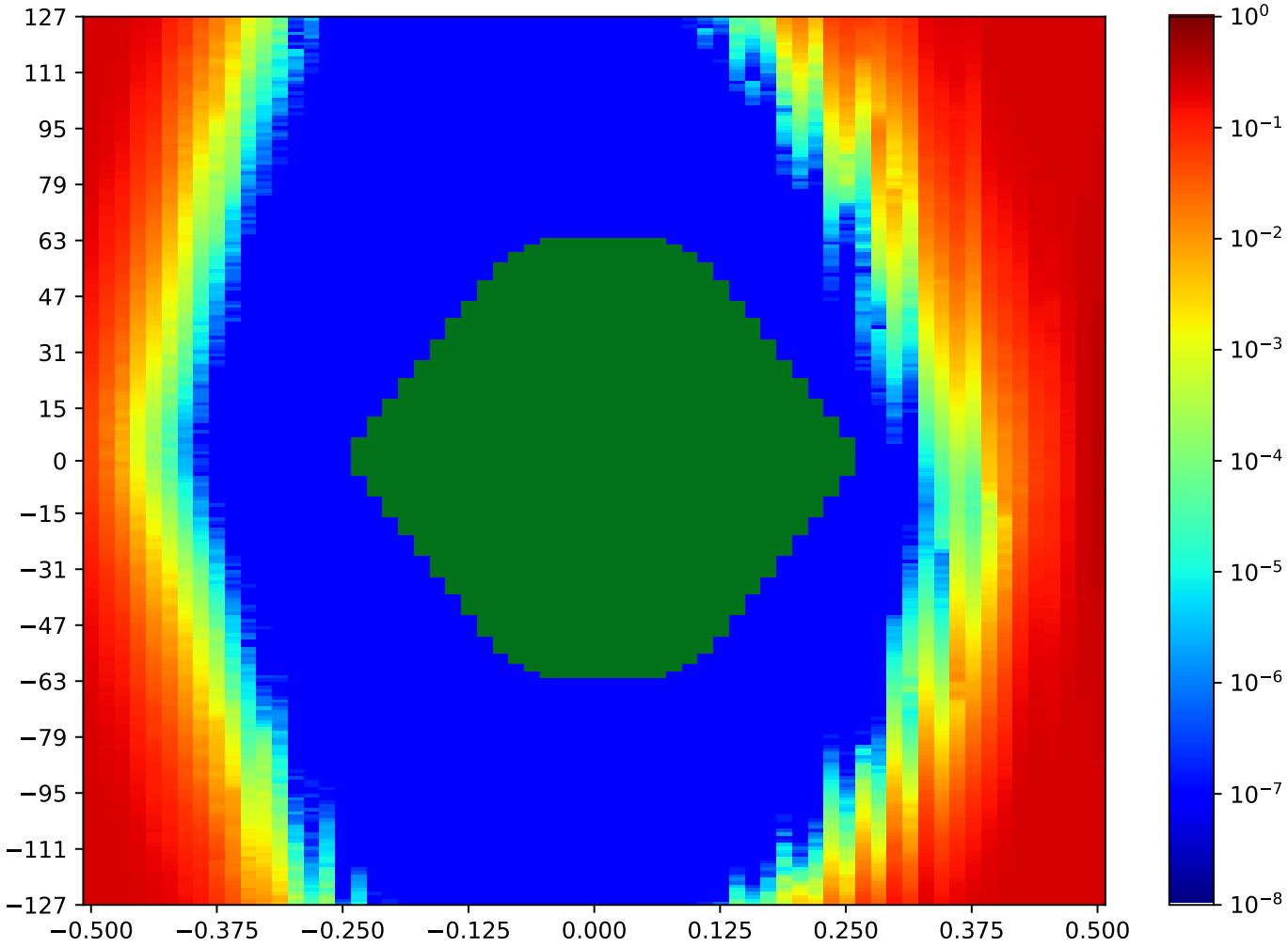


Figure 4.58: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.6 TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Table 4.54: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:06:30		2018-Sep-27 17:06:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8394	40	61.54%	248	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

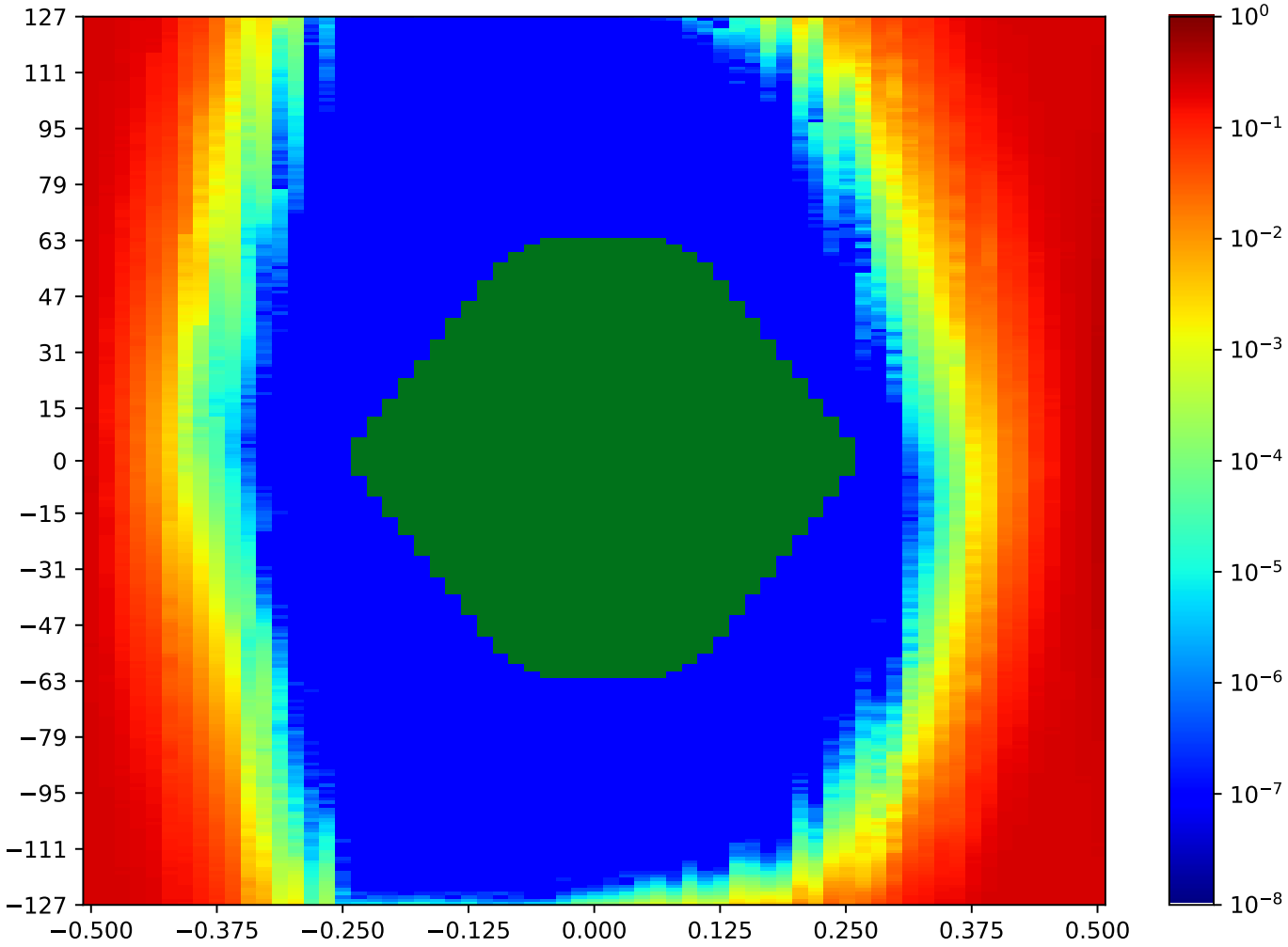


Figure 4.59: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.7 TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Table 4.55: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:07:51		2018-Sep-27 17:08:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9004	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

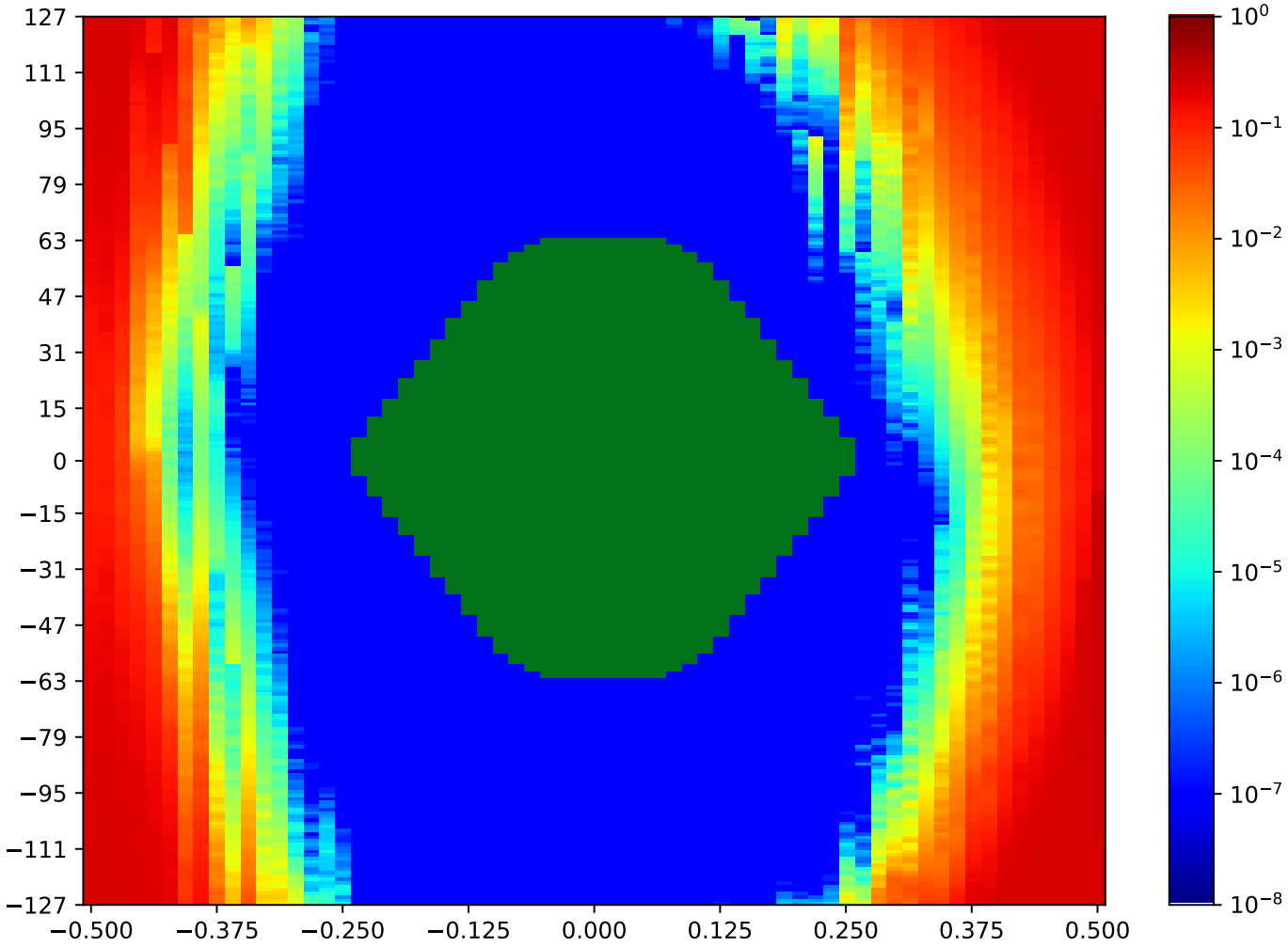


Figure 4.60: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.5.8 TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Table 4.56: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:08:32		2018-Sep-27 17:08:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8189	42	64.62%	237	92.55%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

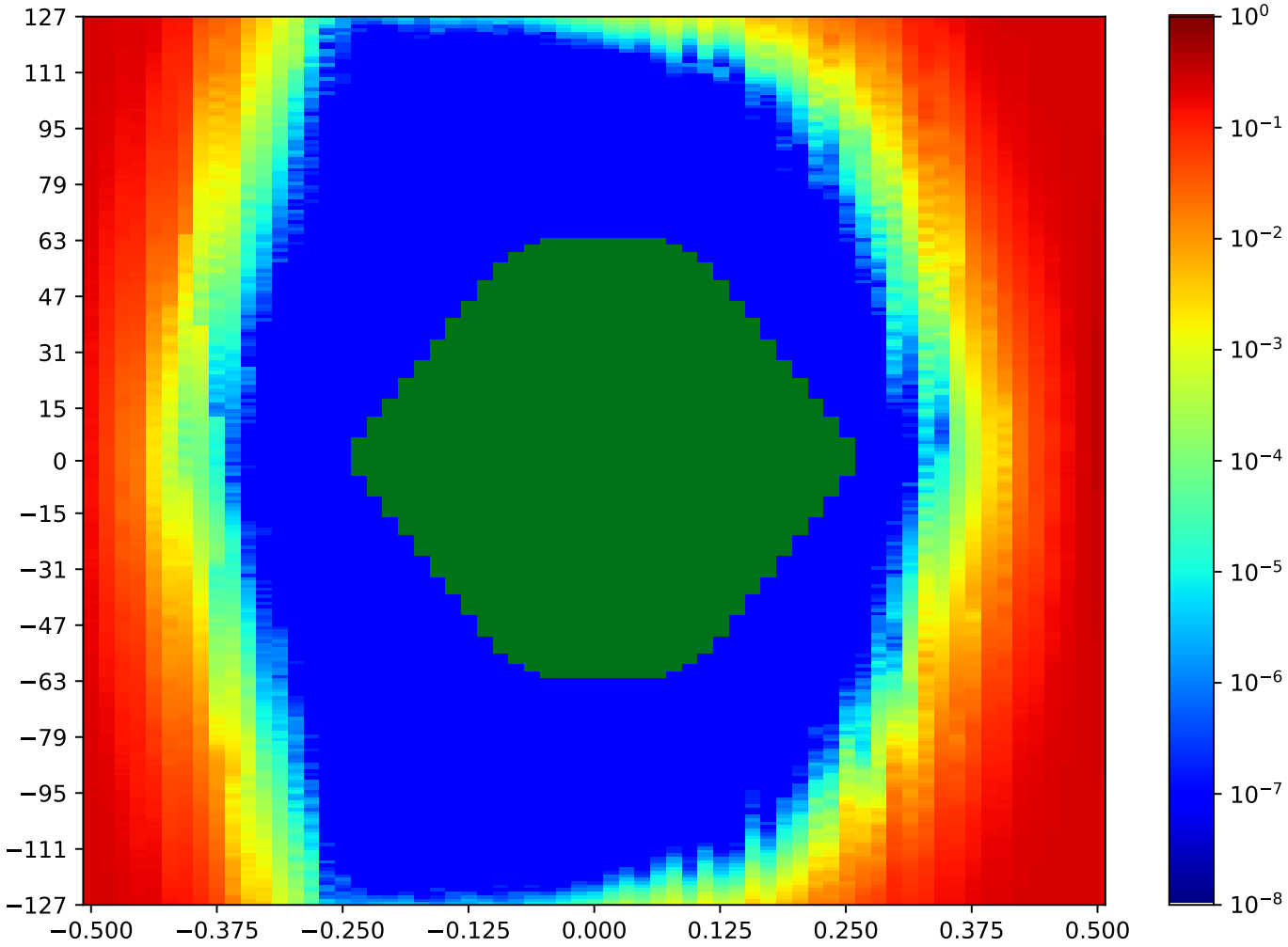


Figure 4.61: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.6 TRP J1 QSFP Loopback

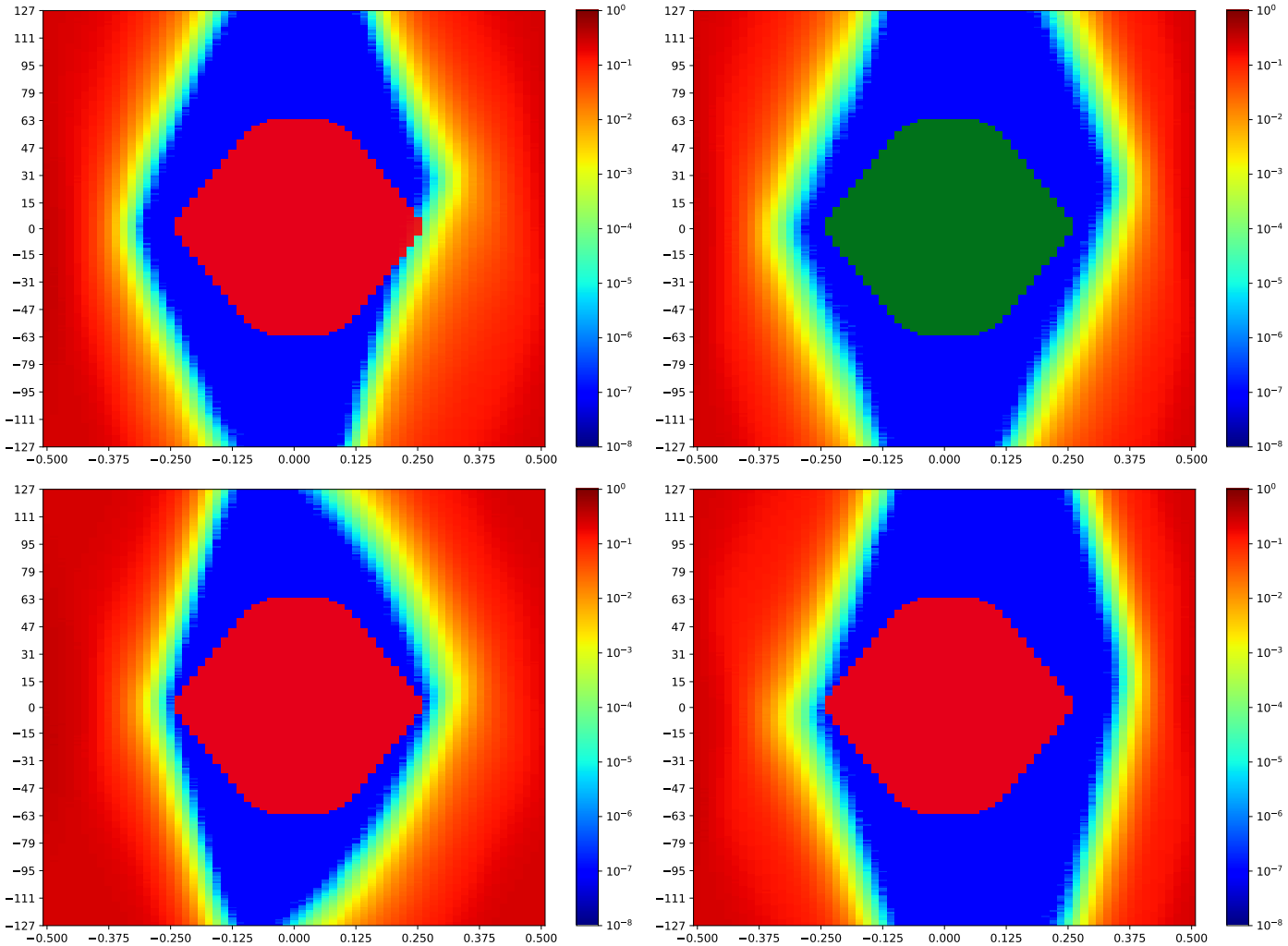


Figure 4.62: TRP J1 QSFP Loopback

A cross-reference to Figure 4.62. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.67.

4.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 4.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:09:13		2018-Sep-27 17:09:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6320	34	52.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

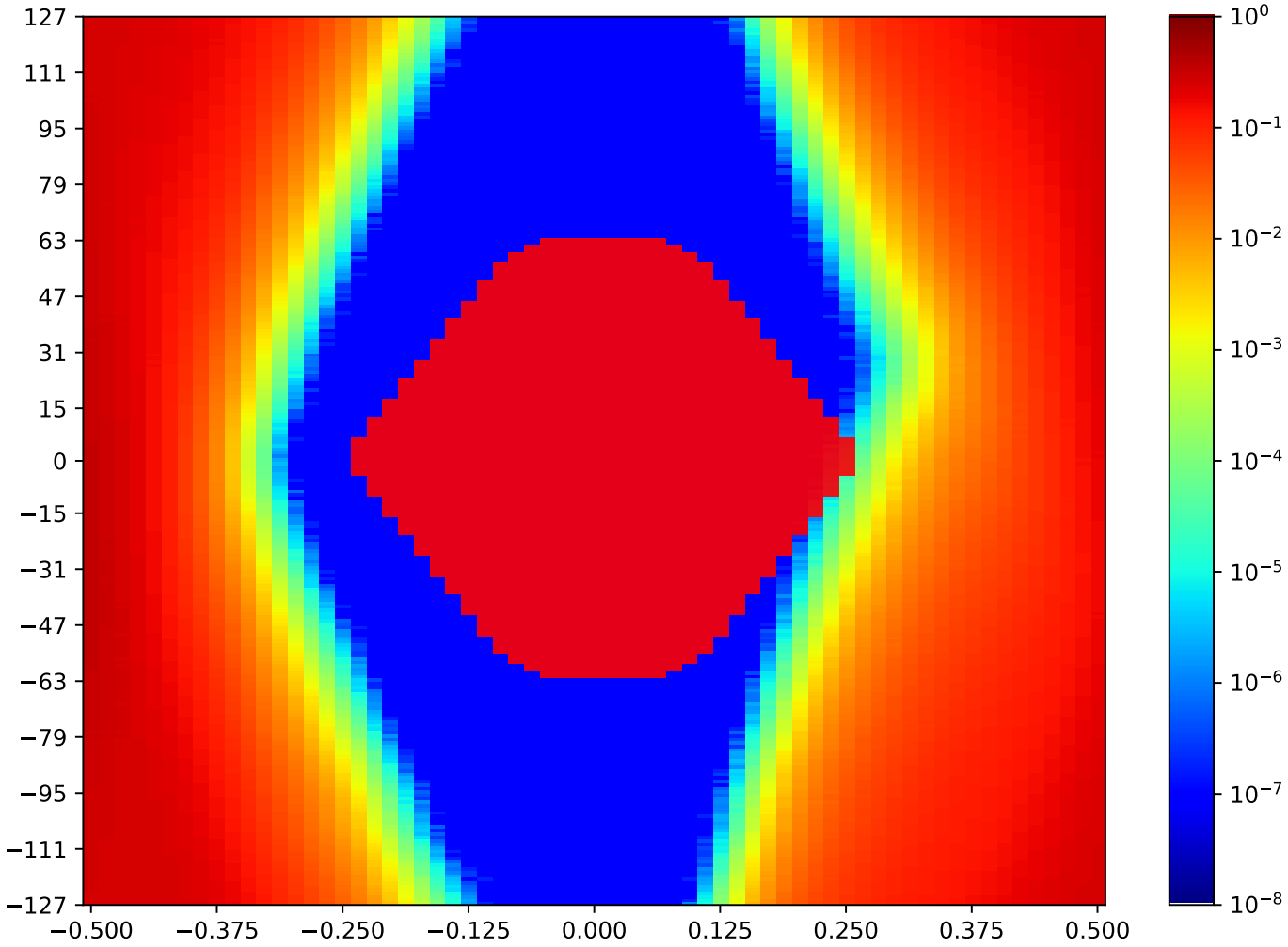


Figure 4.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 4.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:09:33		2018-Sep-27 17:09:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6746	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

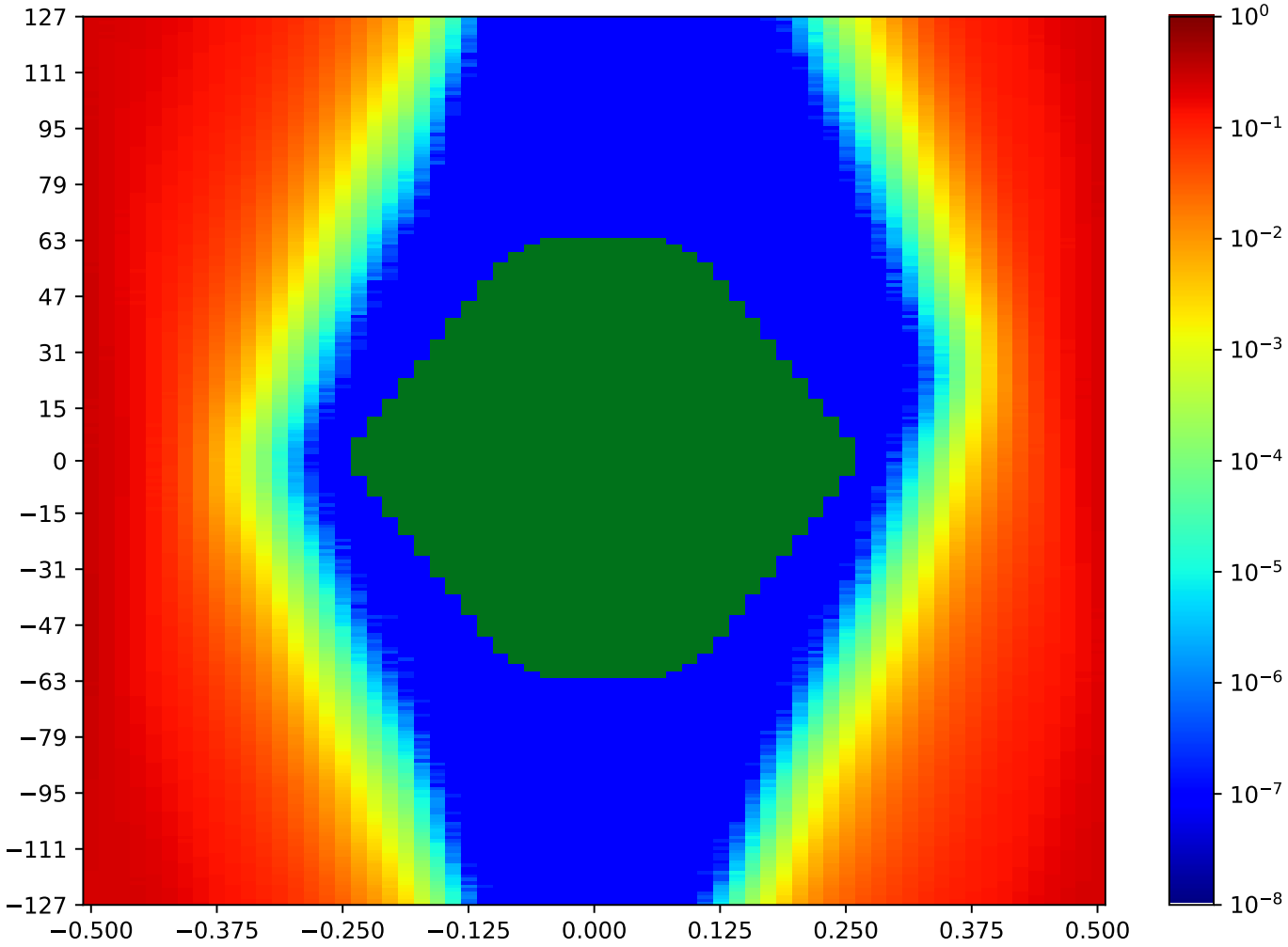


Figure 4.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 4.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:09:54		2018-Sep-27 17:10:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	5311	31	47.69%	243	94.12%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

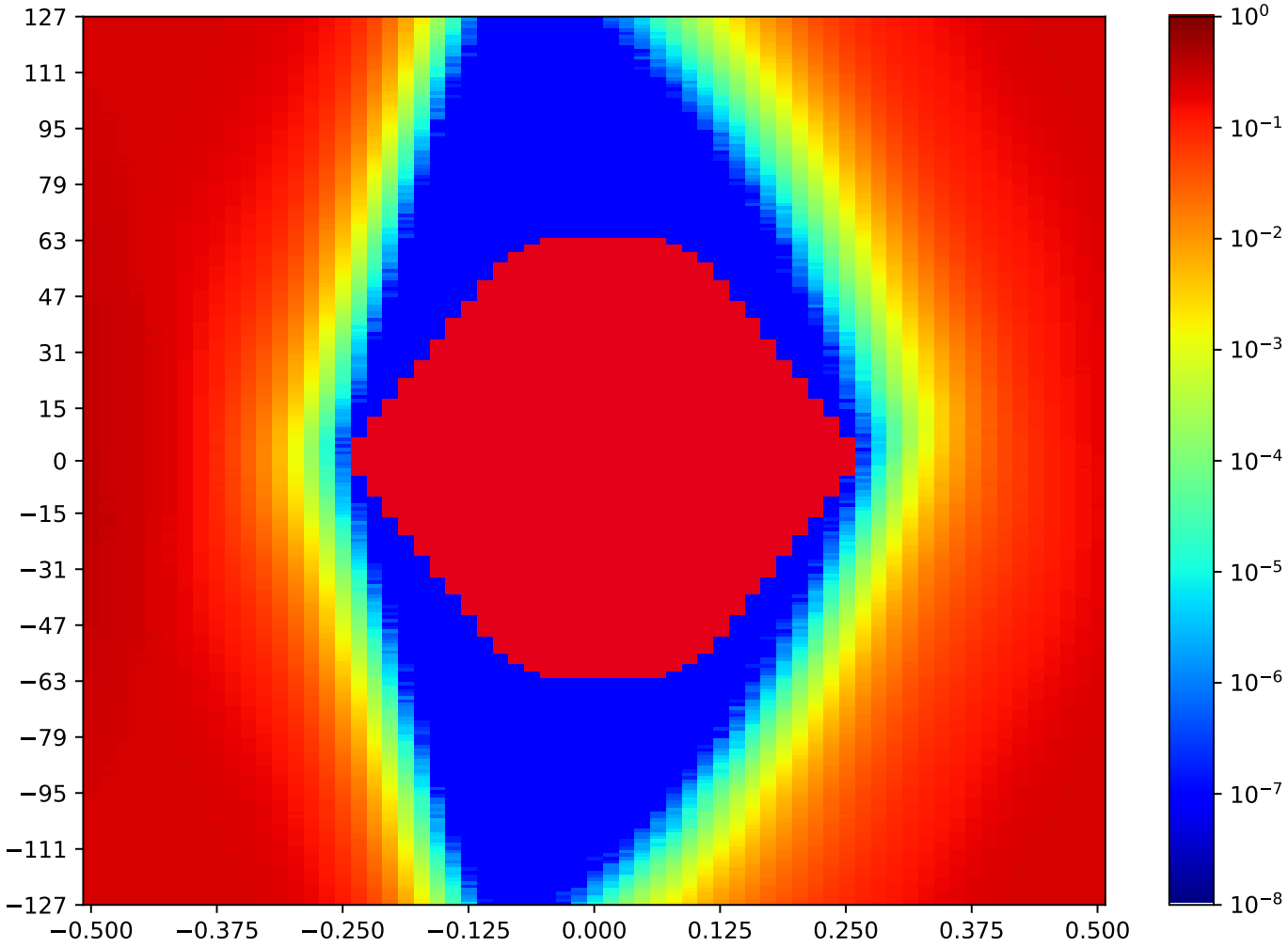


Figure 4.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 4.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:10:15		2018-Sep-27 17:10:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7264	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

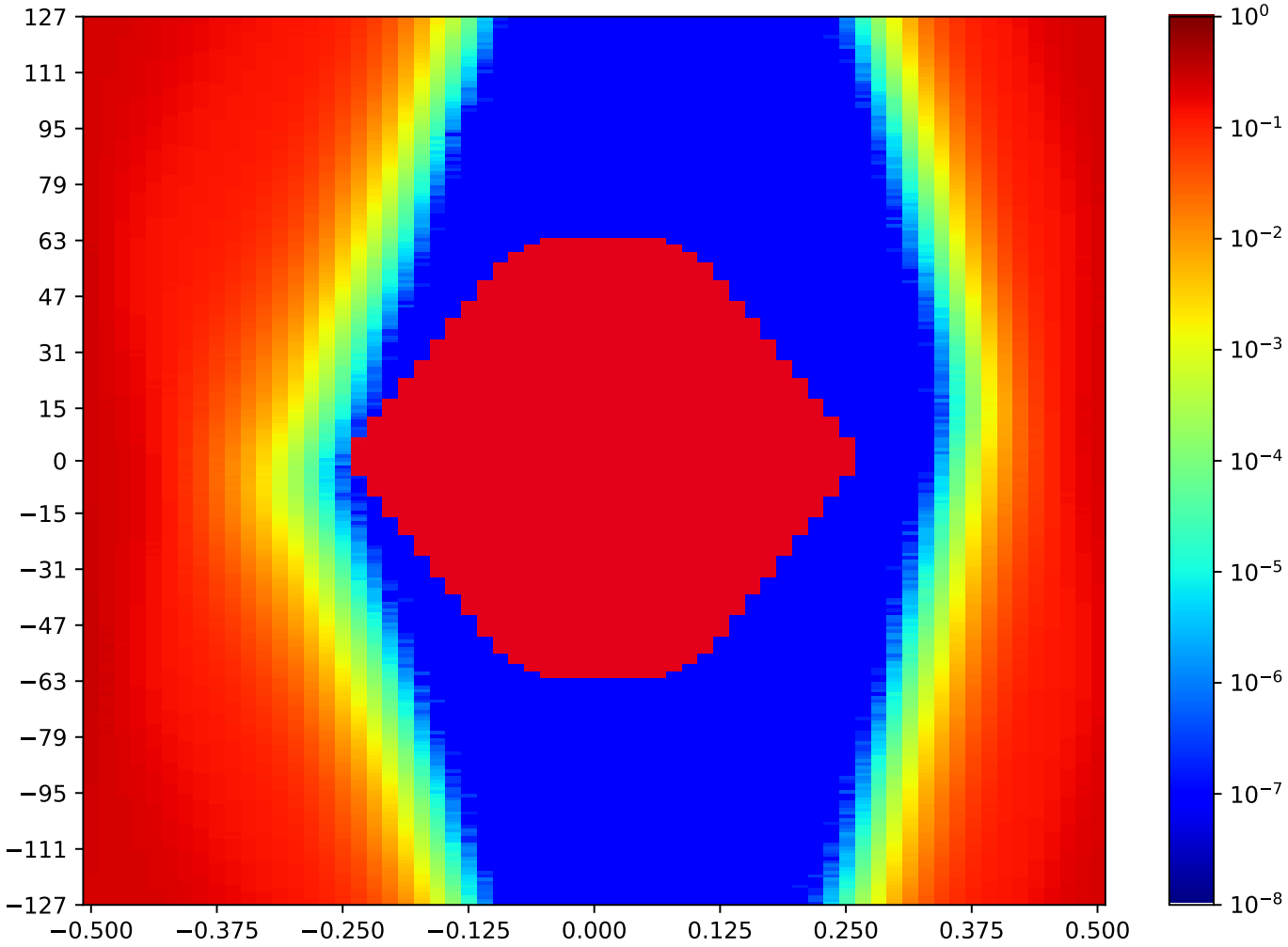


Figure 4.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.7 TRP J3 SFP Loopback

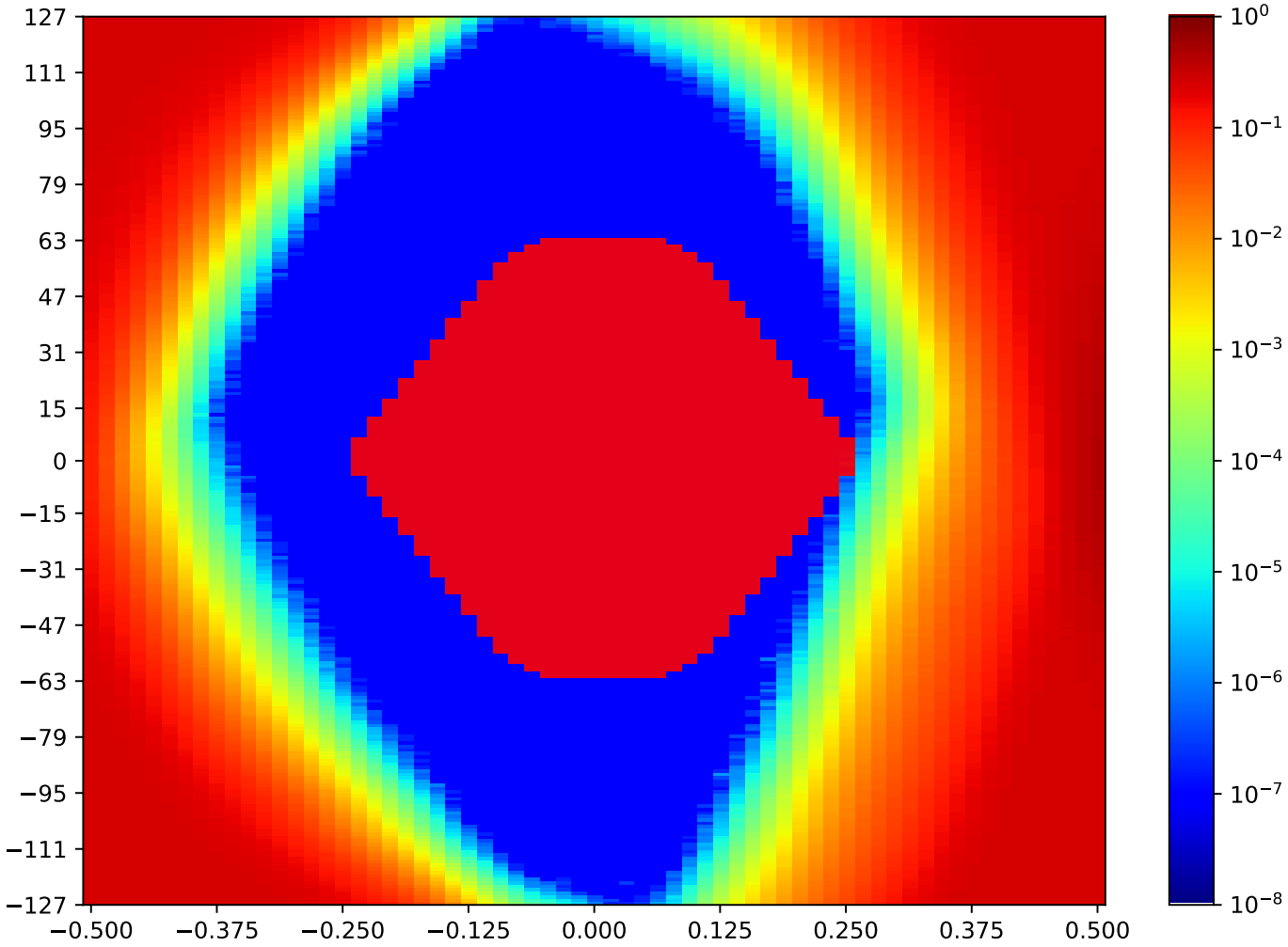


Figure 4.67: TRP J3 SFP Loopback

A cross-reference to Figure 4.67. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.69.

4.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 4.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:10:36		2018-Sep-27 17:10:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6571	36	55.38%	243	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

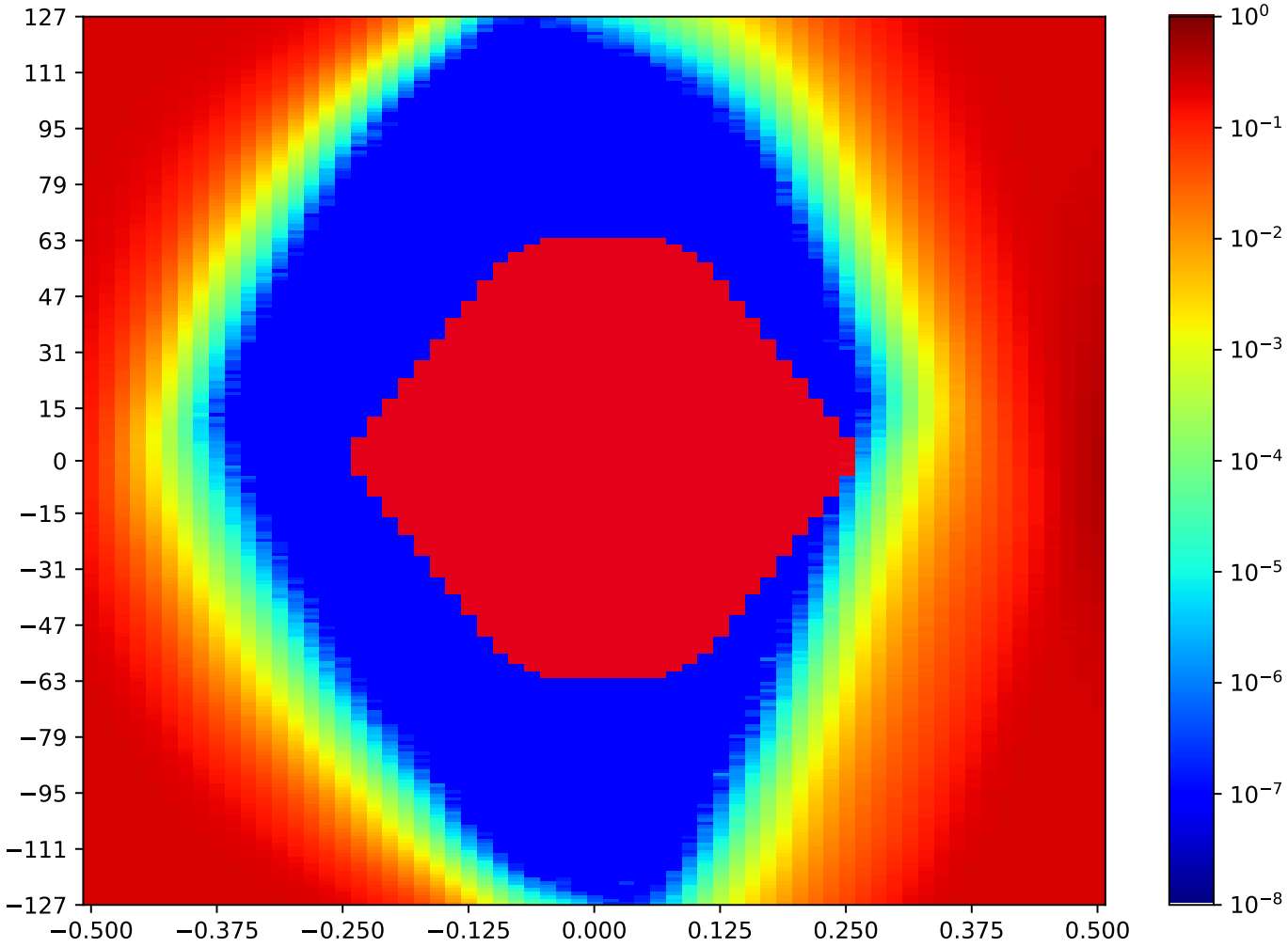


Figure 4.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 4.67. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8 MSP_A TRP On board links

A cross-reference to Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.98.

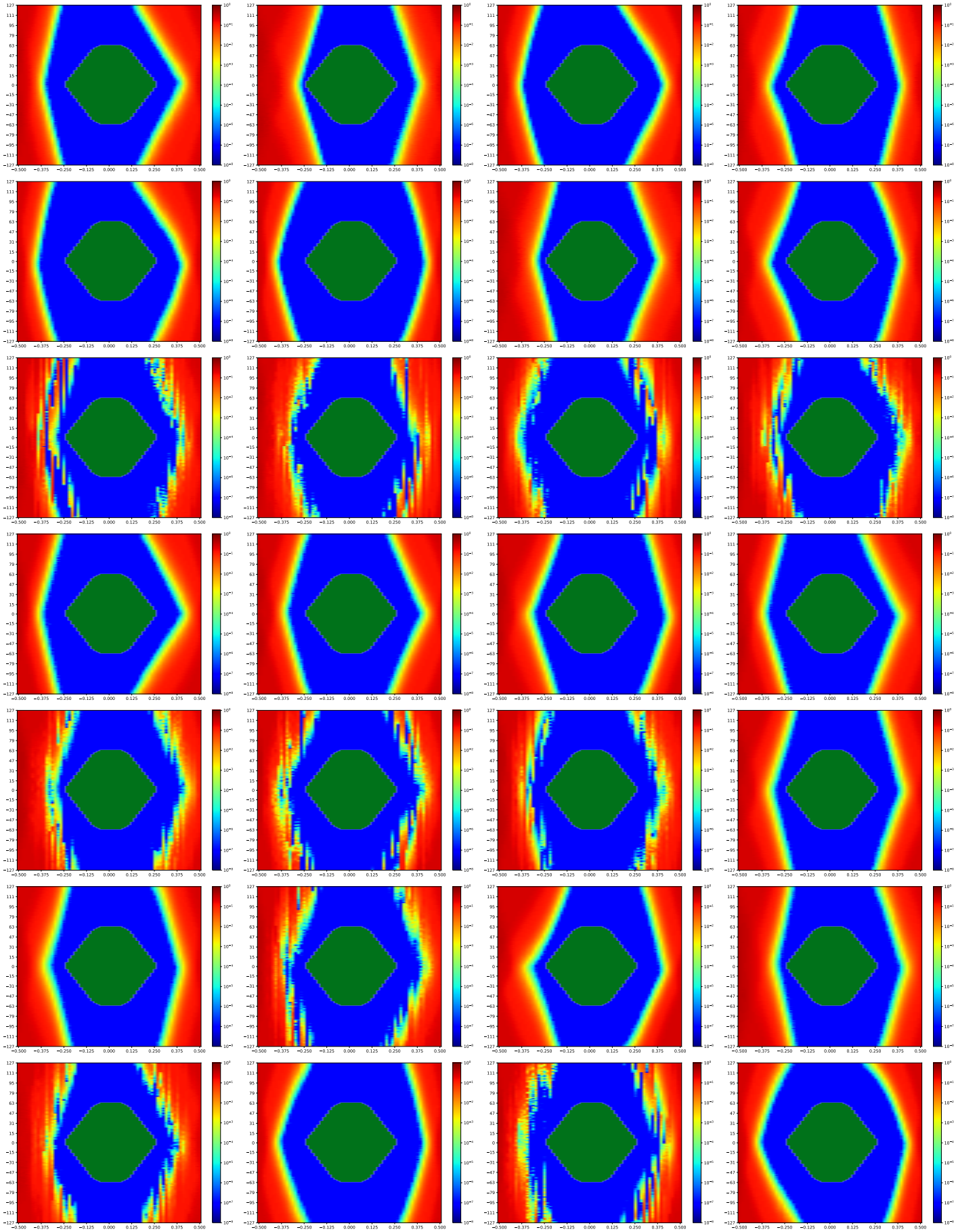


Figure 4.69: MSP_A TRP On board links

4.8.1 MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Table 4.62: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:10:56		2018-Sep-27 17:11:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8740	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

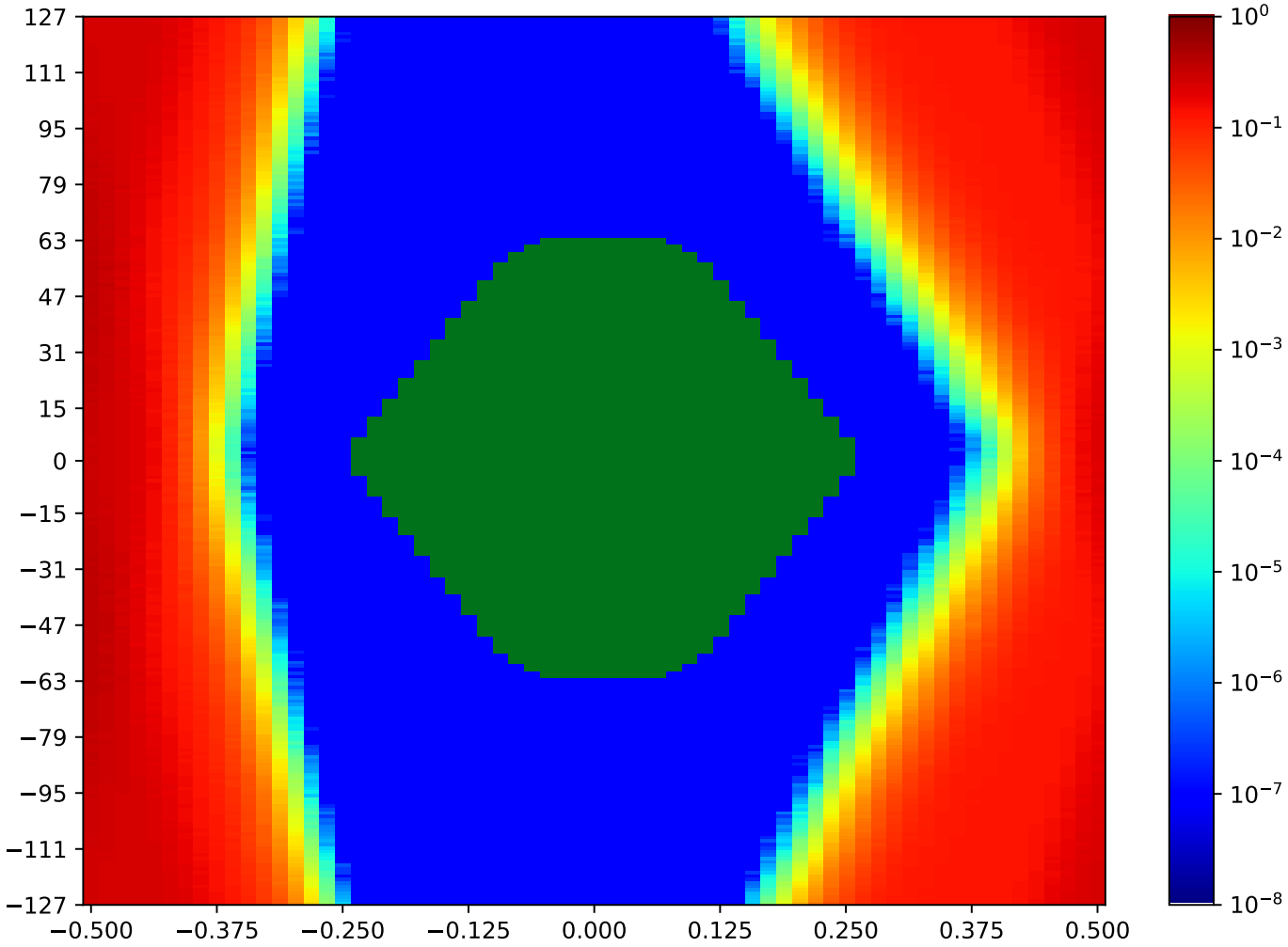


Figure 4.70: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.2 MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Table 4.63: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:11:16		2018-Sep-27 17:11:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7753	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

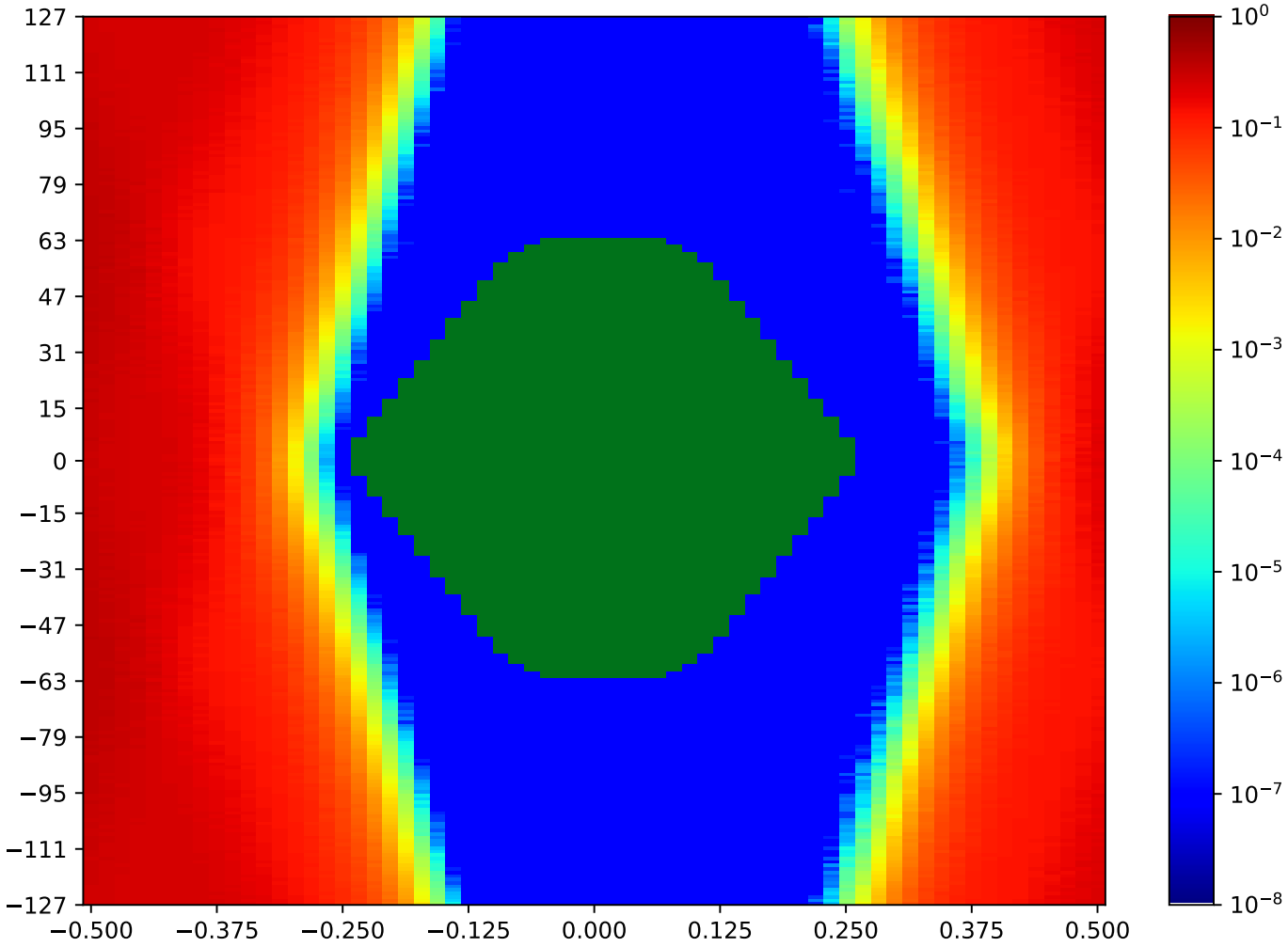


Figure 4.71: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.3 MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Table 4.64: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:11:37		2018-Sep-27 17:11:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9522	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

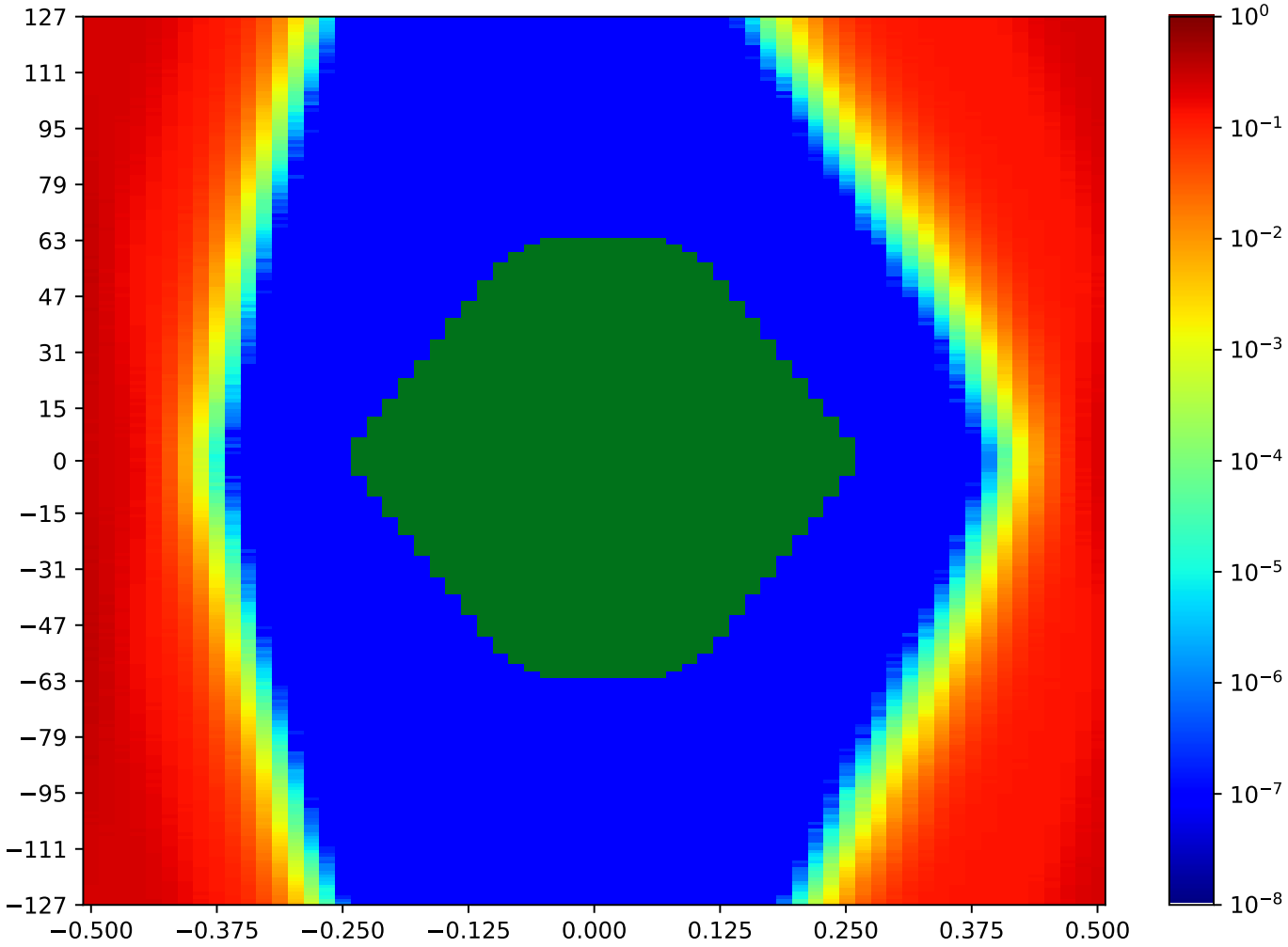


Figure 4.72: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.4 MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Table 4.65: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:11:57		2018-Sep-27 17:12:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8692	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

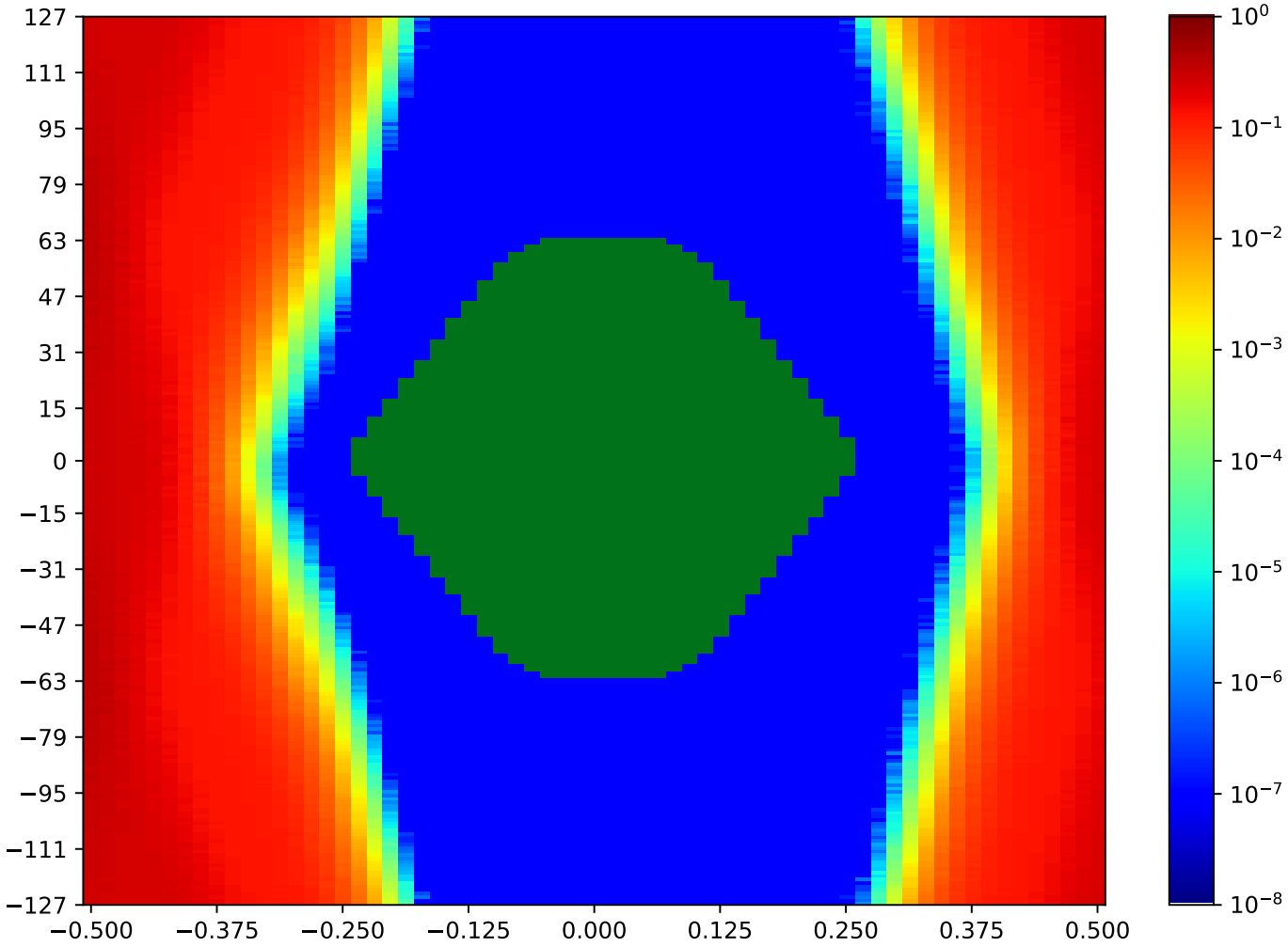


Figure 4.73: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.5 MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Table 4.66: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:12:18		2018-Sep-27 17:12:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9918	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

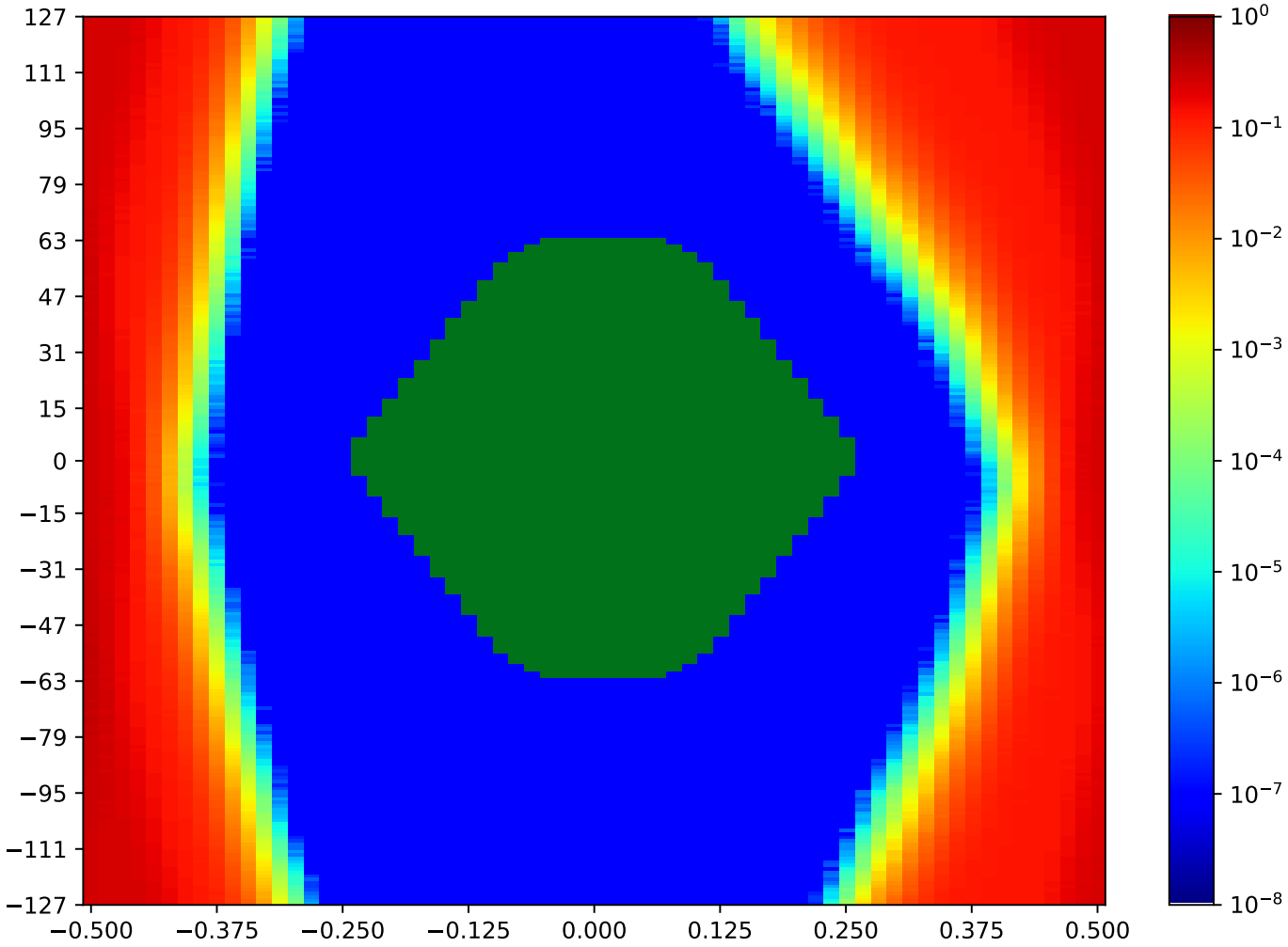


Figure 4.74: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.6 MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Table 4.67: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:12:38		2018-Sep-27 17:12:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10795	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

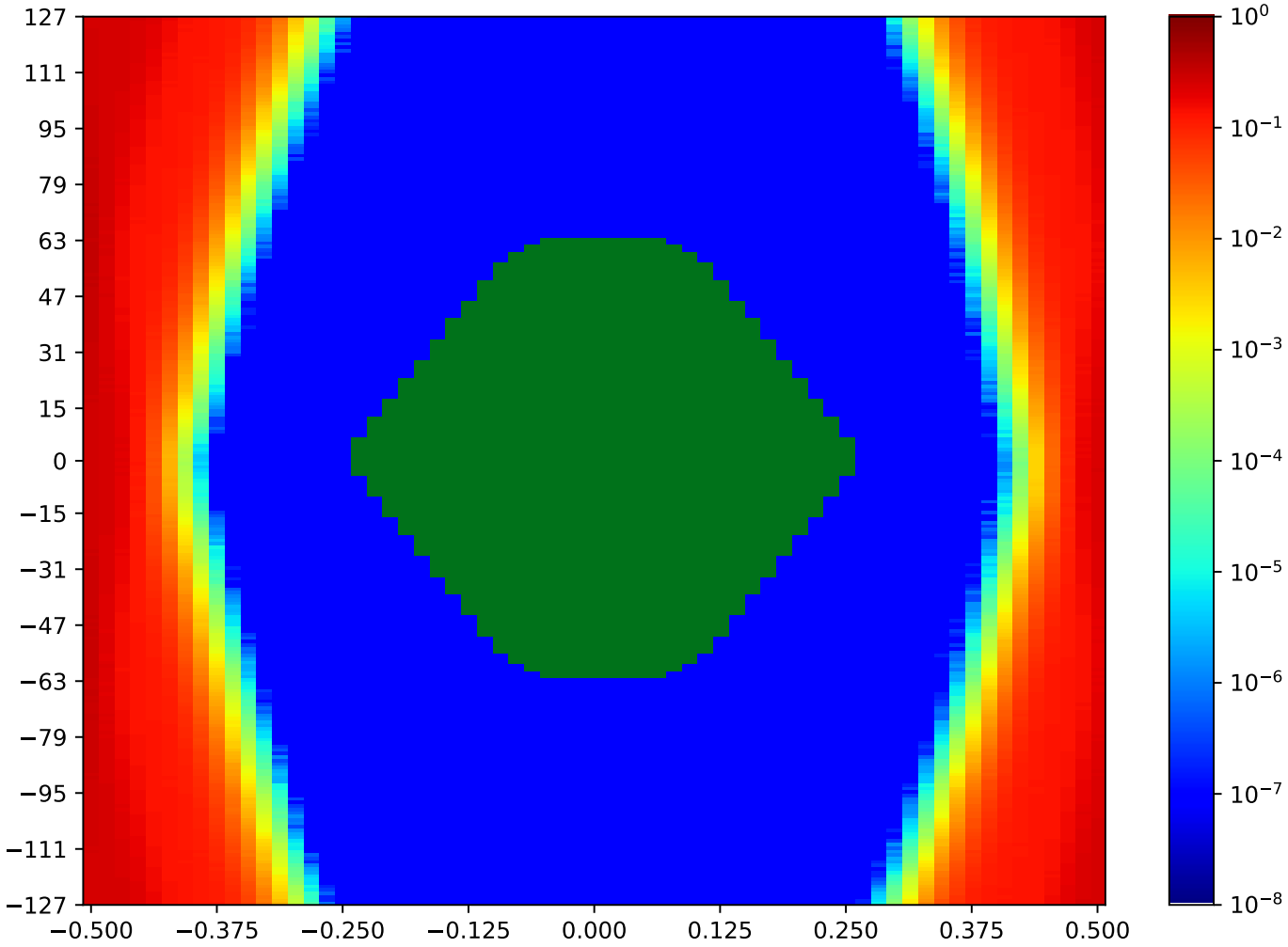


Figure 4.75: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.7 MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Table 4.68: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:12:58		2018-Sep-27 17:13:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7801	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

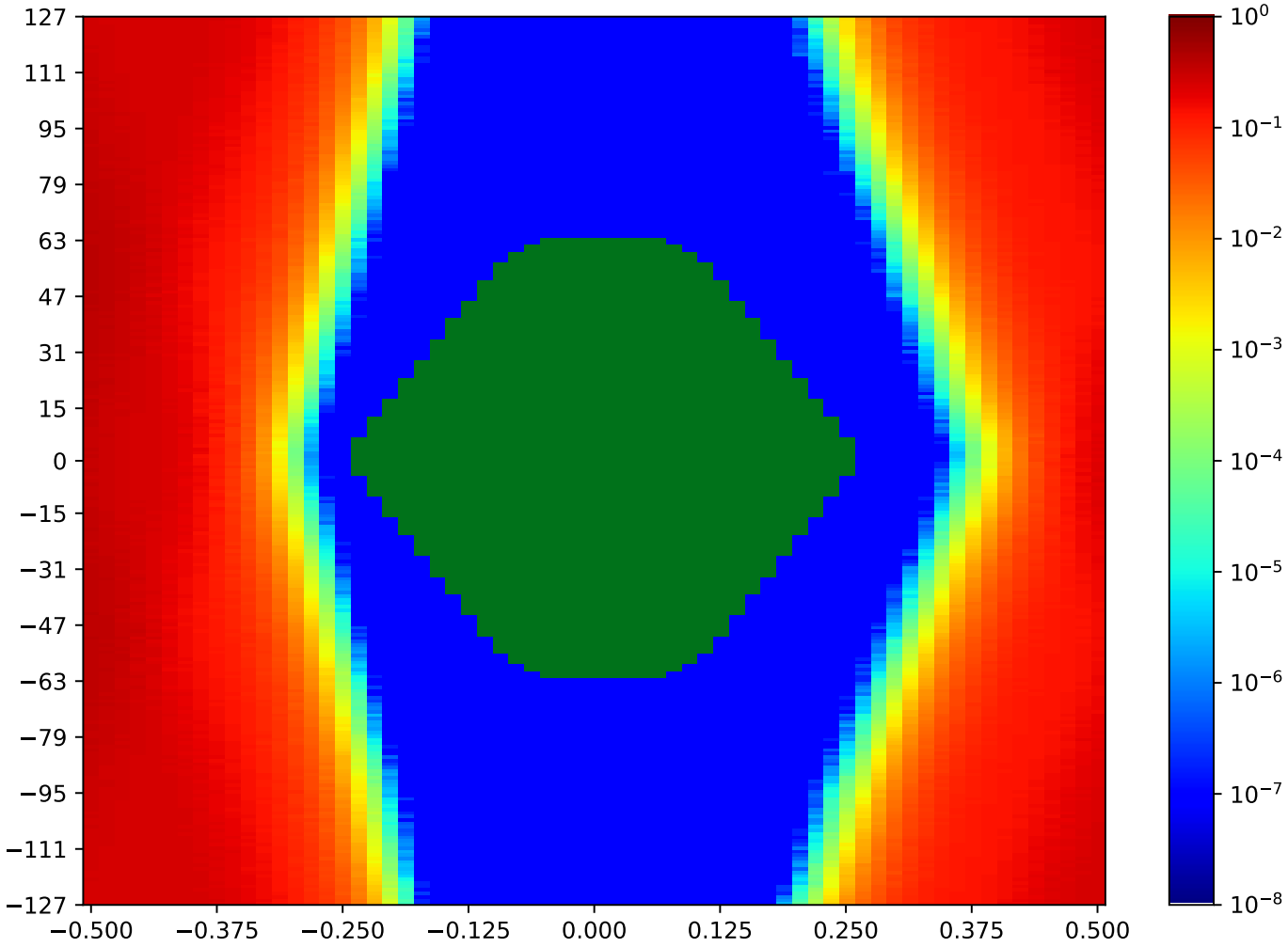


Figure 4.76: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.8 MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Table 4.69: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:13:19		2018-Sep-27 17:13:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8450	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

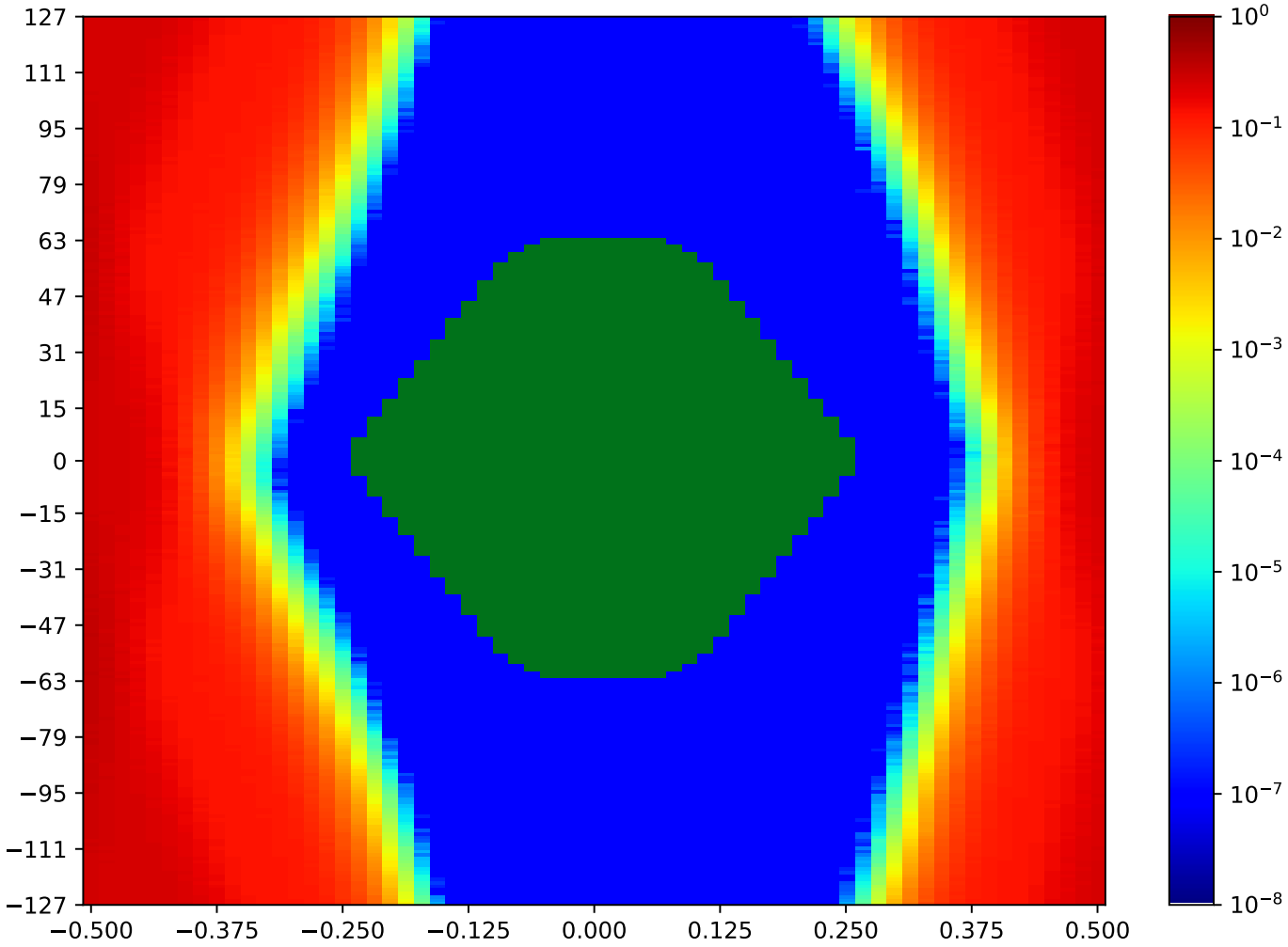


Figure 4.77: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.9 MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Table 4.70: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:13:39		2018-Sep-27 17:13:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8995	46	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

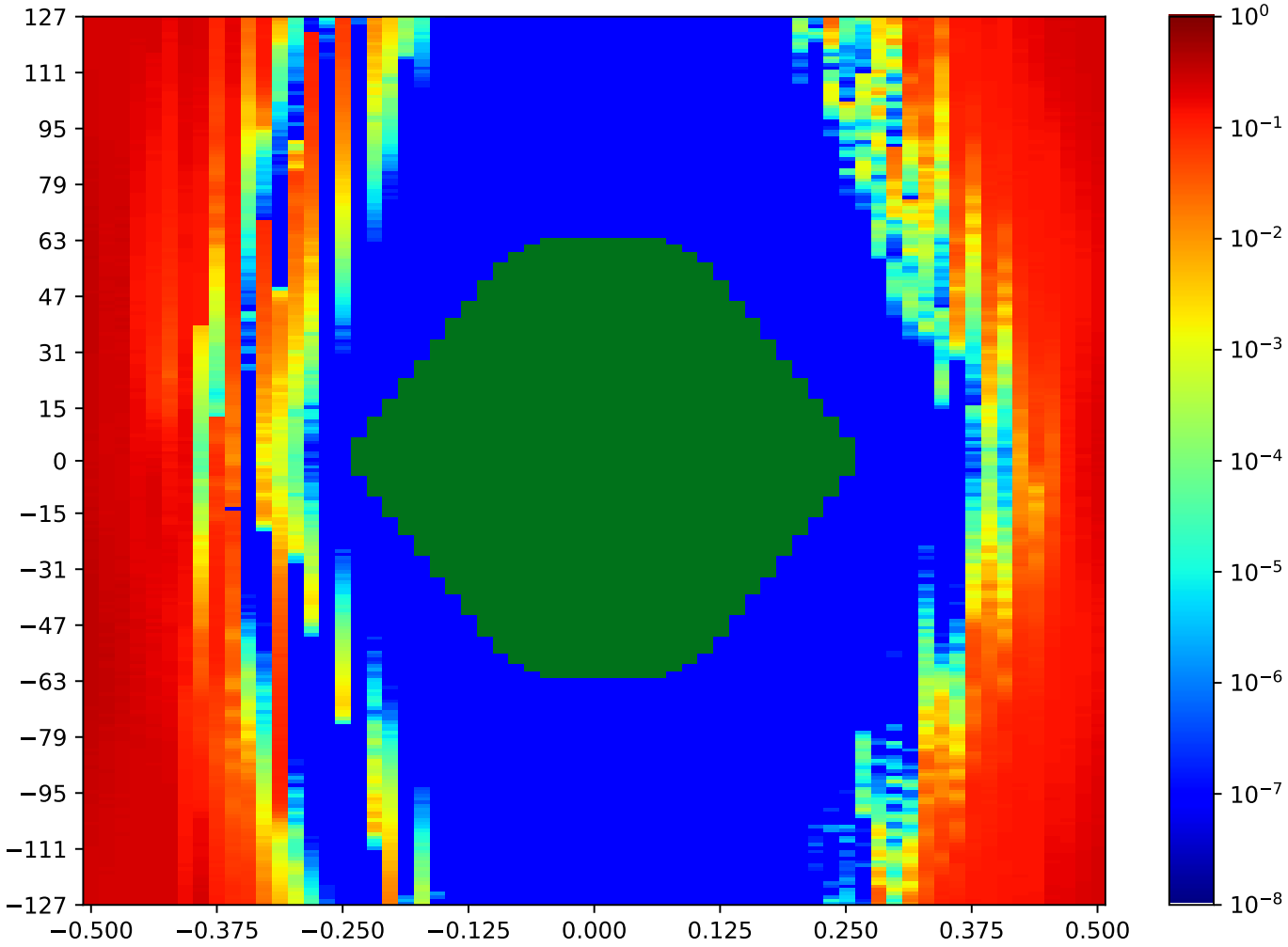


Figure 4.78: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.10 MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Table 4.71: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:13:59		2018-Sep-27 17:14:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8705	45	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

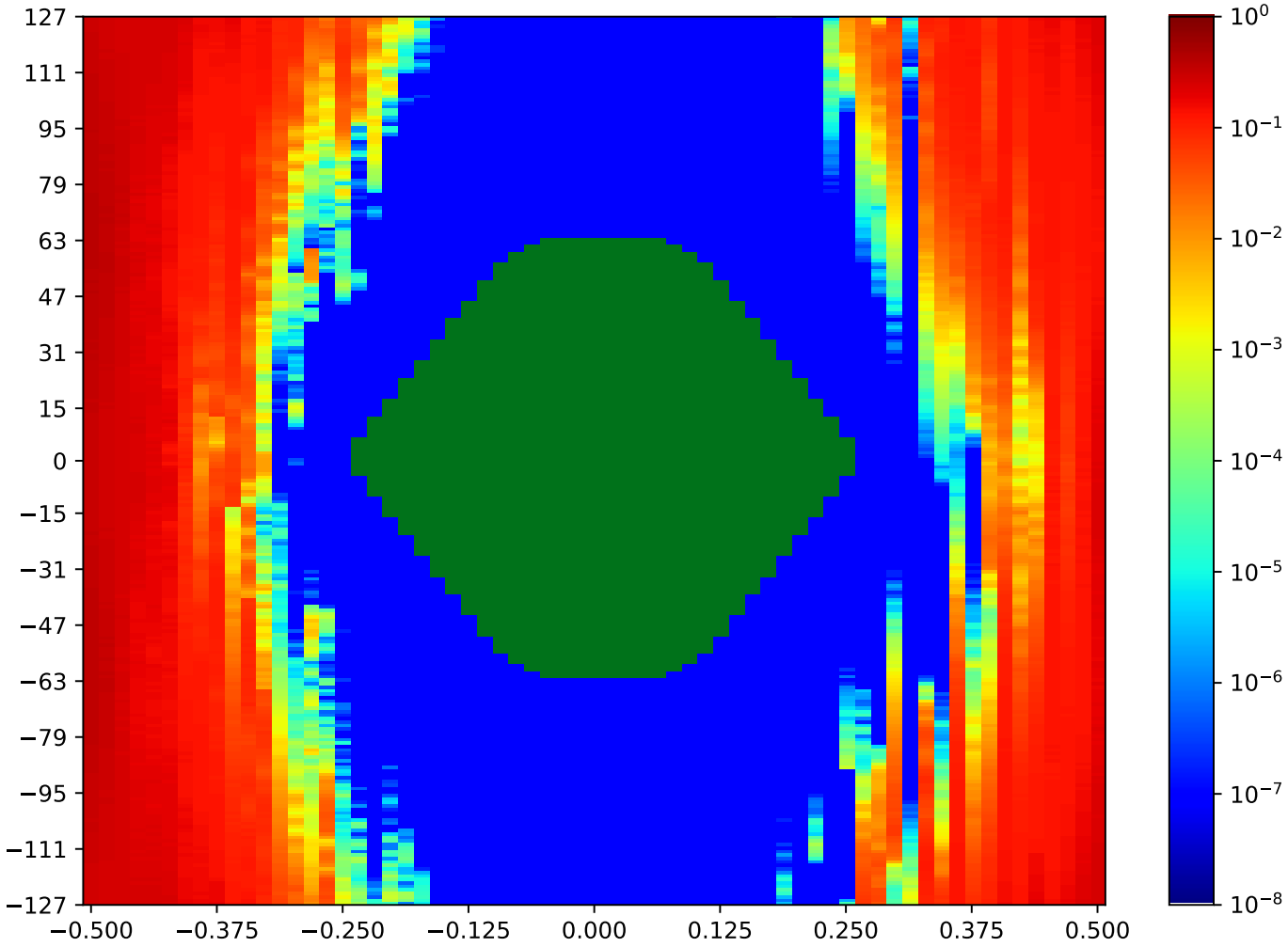


Figure 4.79: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.11 MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Table 4.72: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:14:20		2018-Sep-27 17:14:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9208	46	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

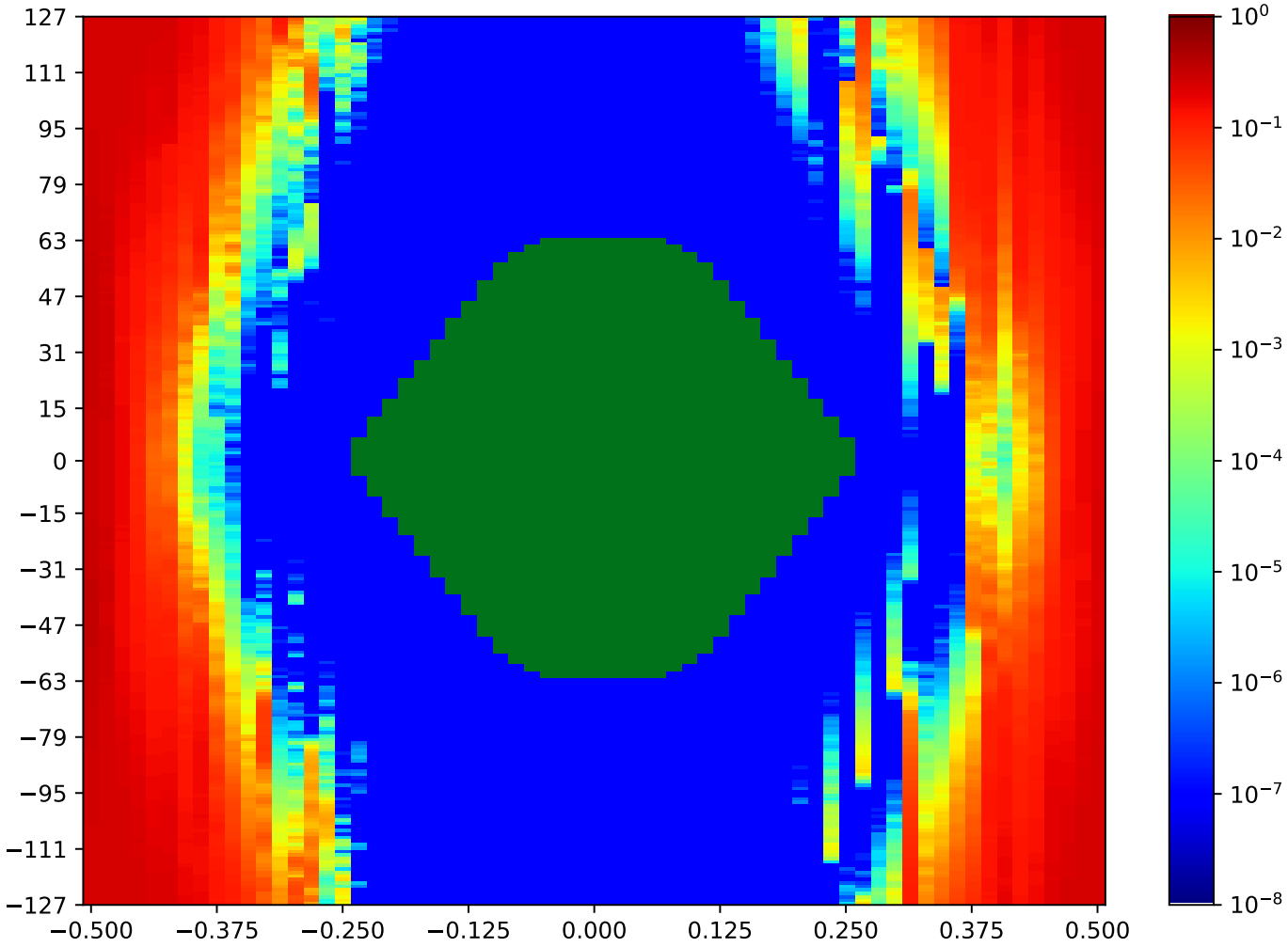


Figure 4.80: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.12 MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Table 4.73: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:14:40		2018-Sep-27 17:15:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8410	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

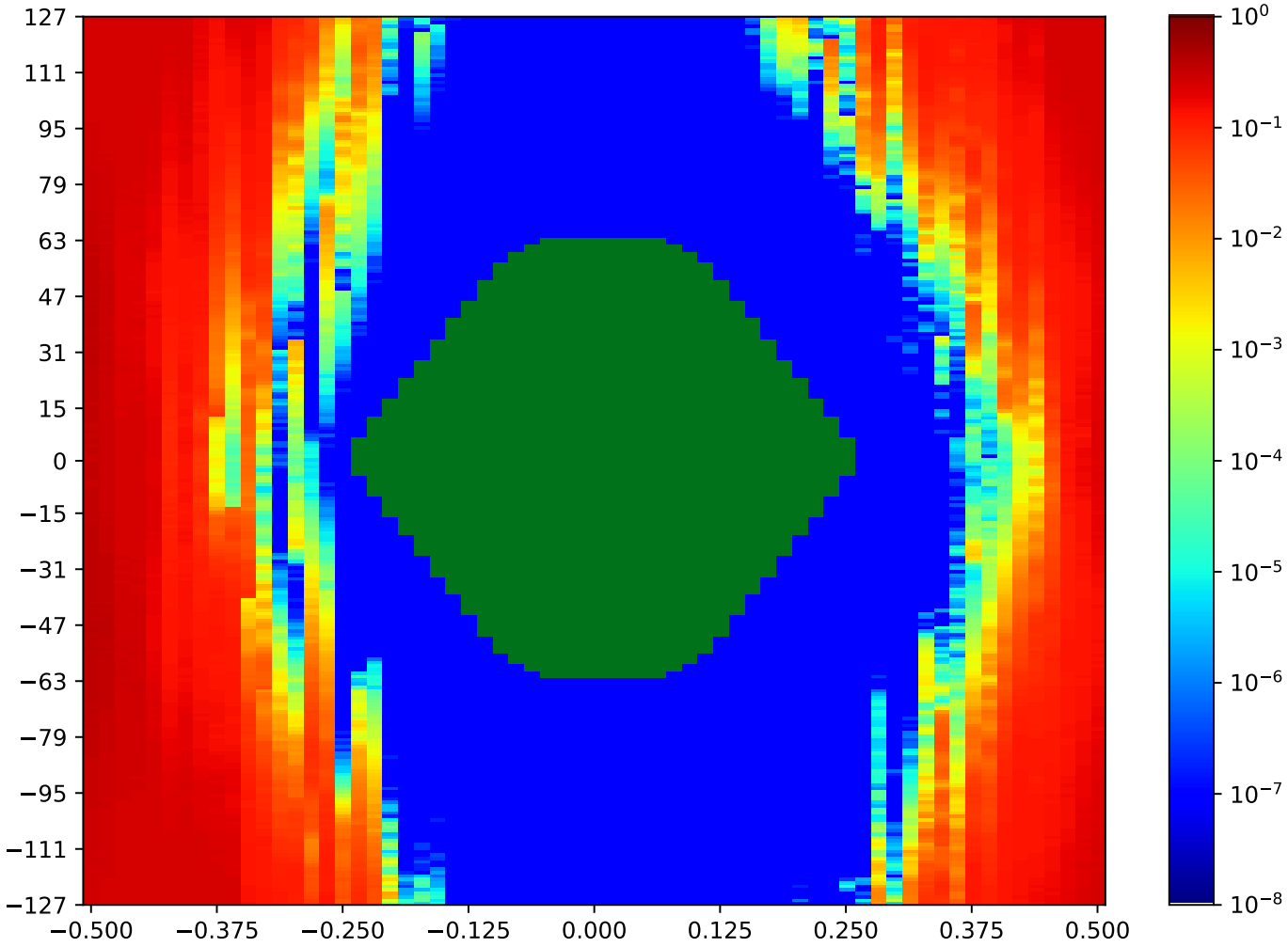


Figure 4.81: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.13 MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Table 4.74: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:15:01		2018-Sep-27 17:15:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9039	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

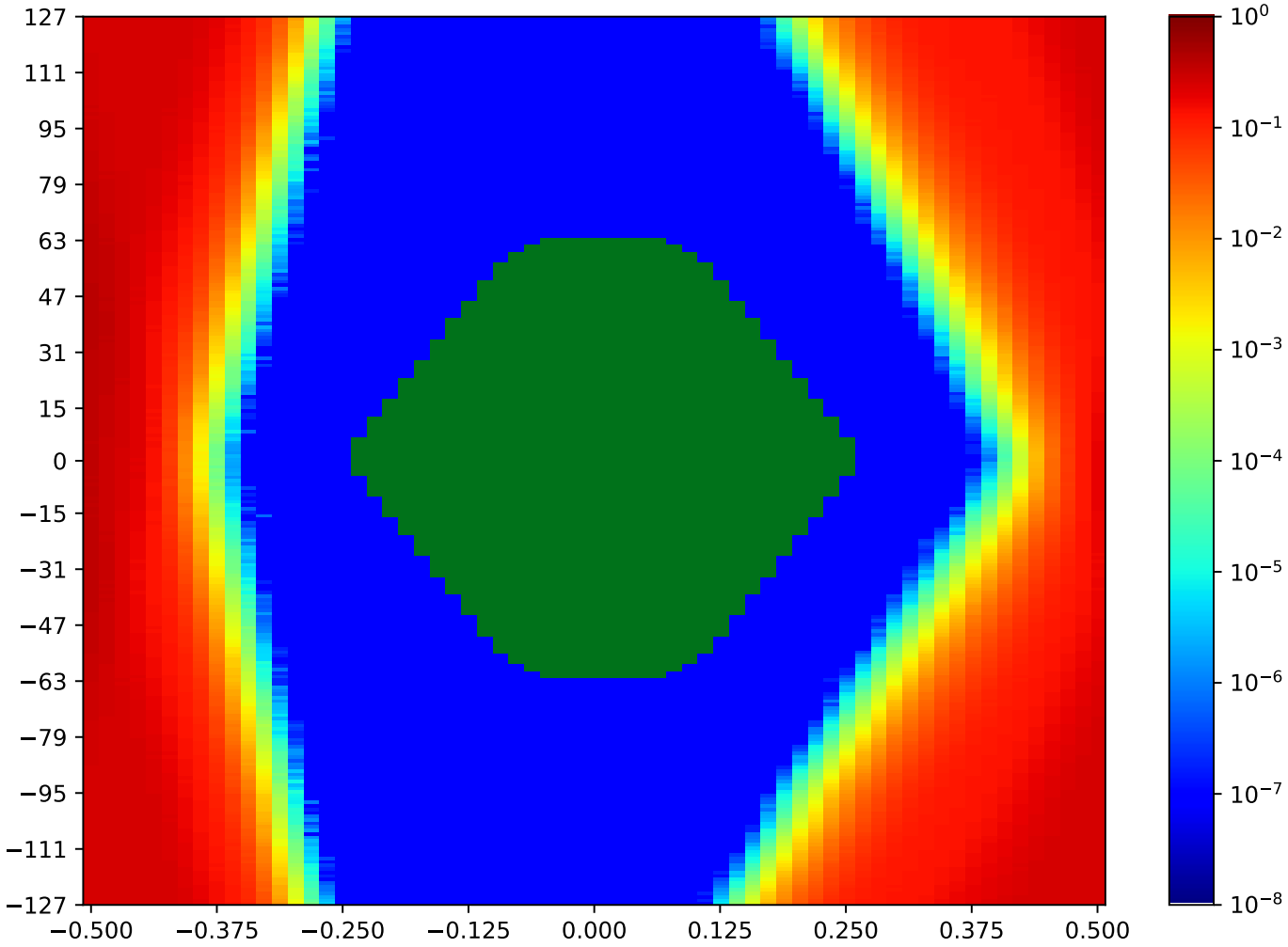


Figure 4.82: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.14 MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Table 4.75: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:15:22		2018-Sep-27 17:15:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8903	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

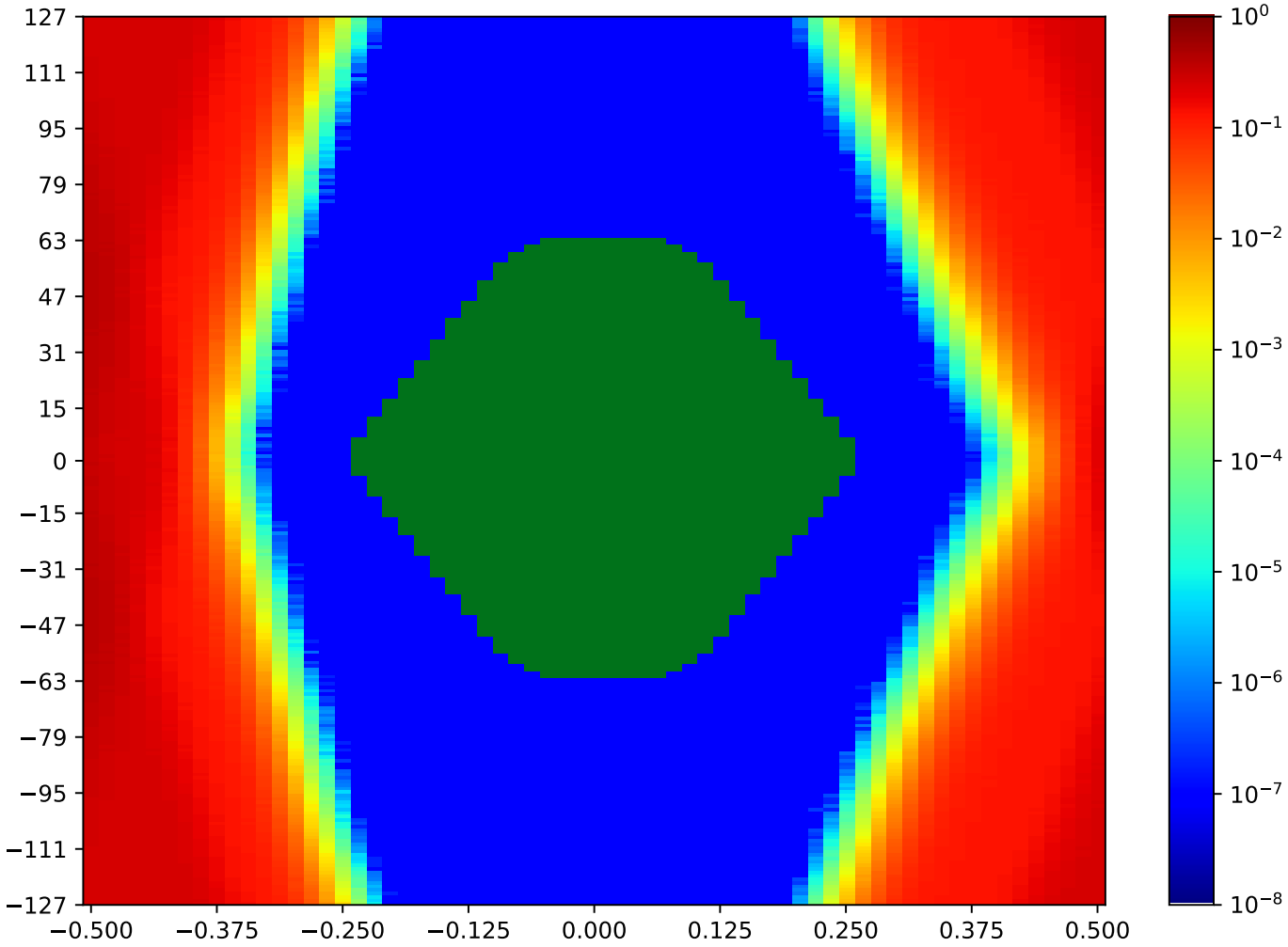


Figure 4.83: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.15 MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Table 4.76: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:15:42		2018-Sep-27 17:16:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9036	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

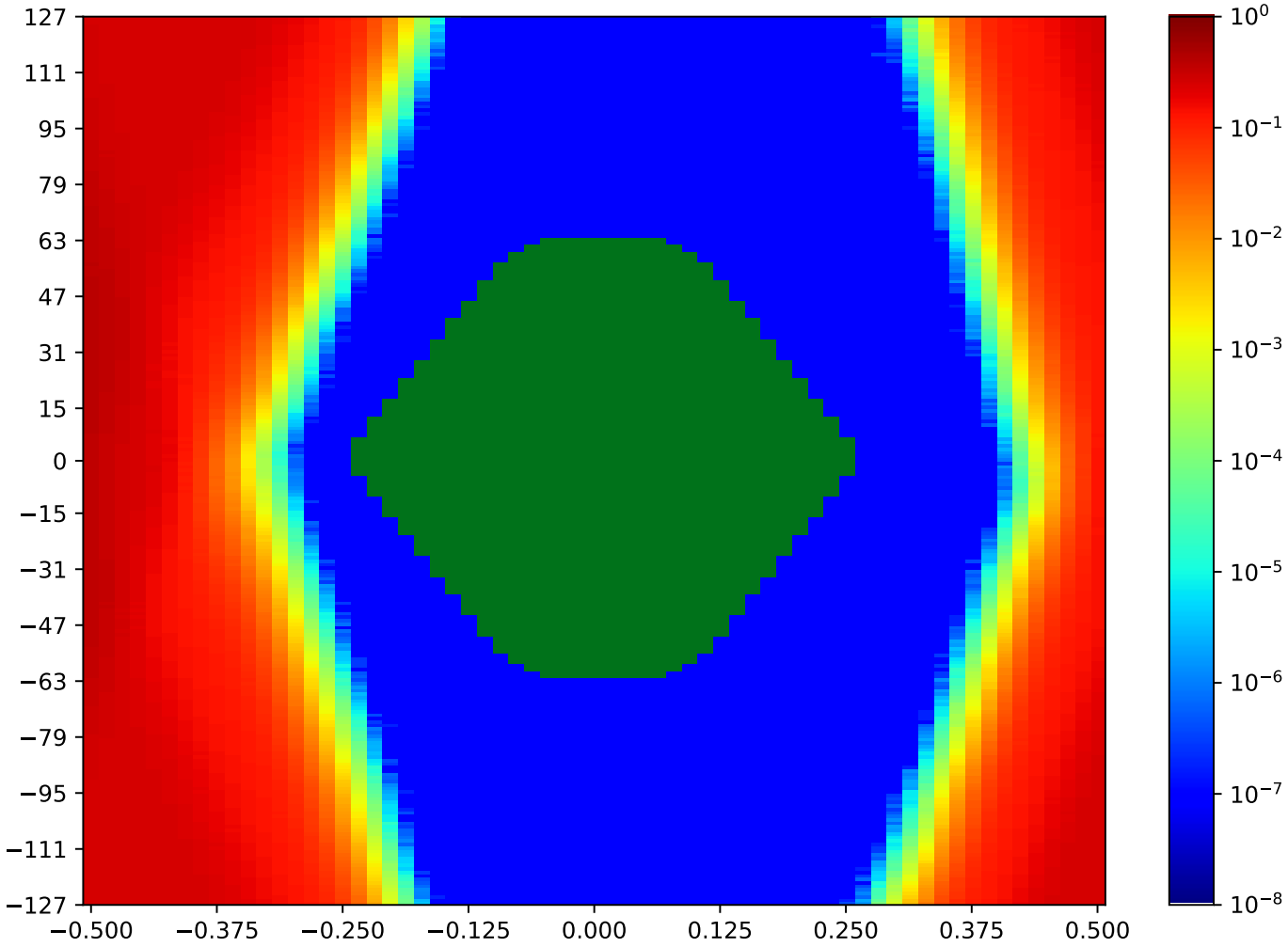


Figure 4.84: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.16 MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Table 4.77: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:16:02		2018-Sep-27 17:16:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8508	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

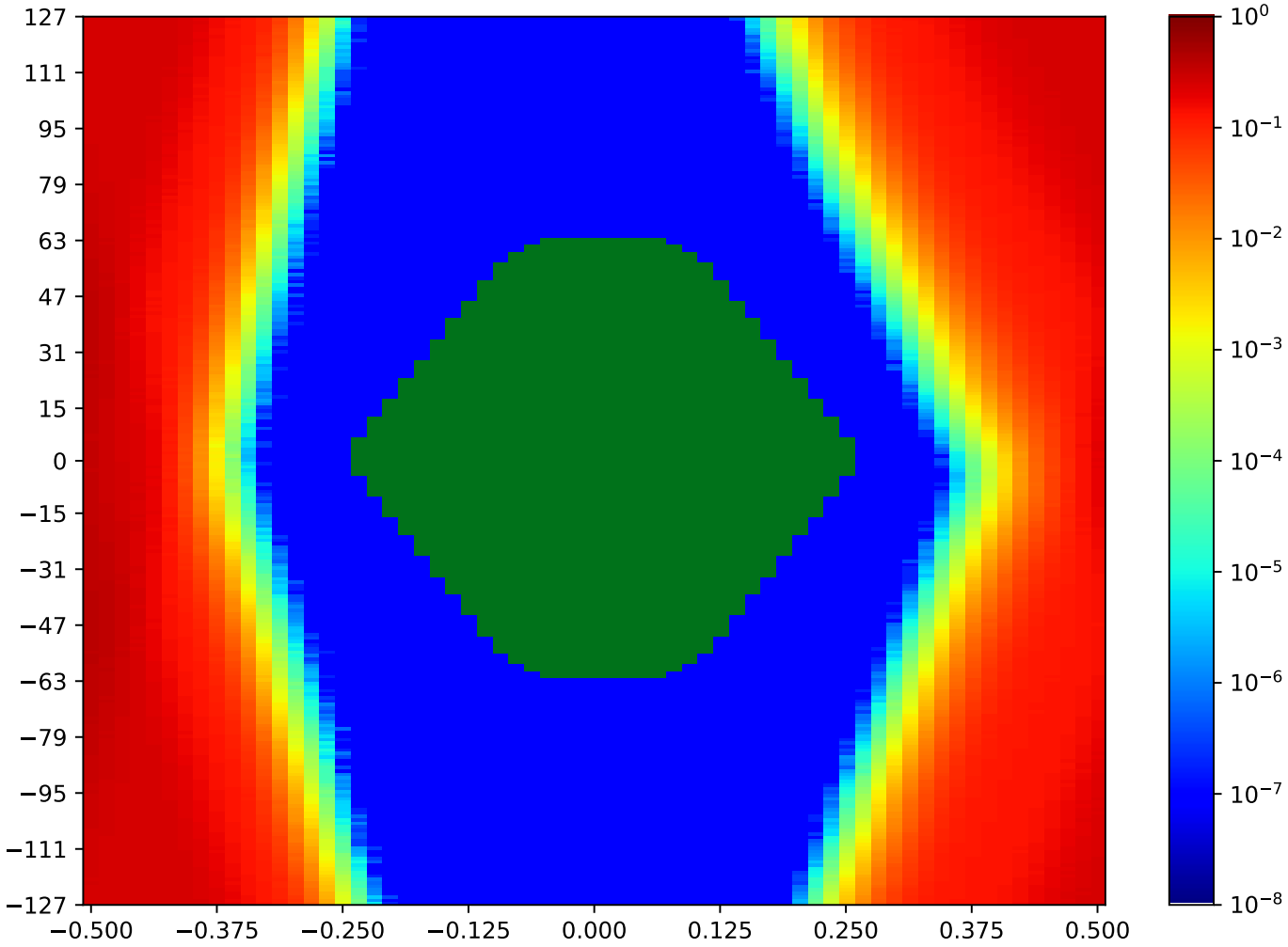


Figure 4.85: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.17 MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Table 4.78: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:16:23		2018-Sep-27 17:16:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8676	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

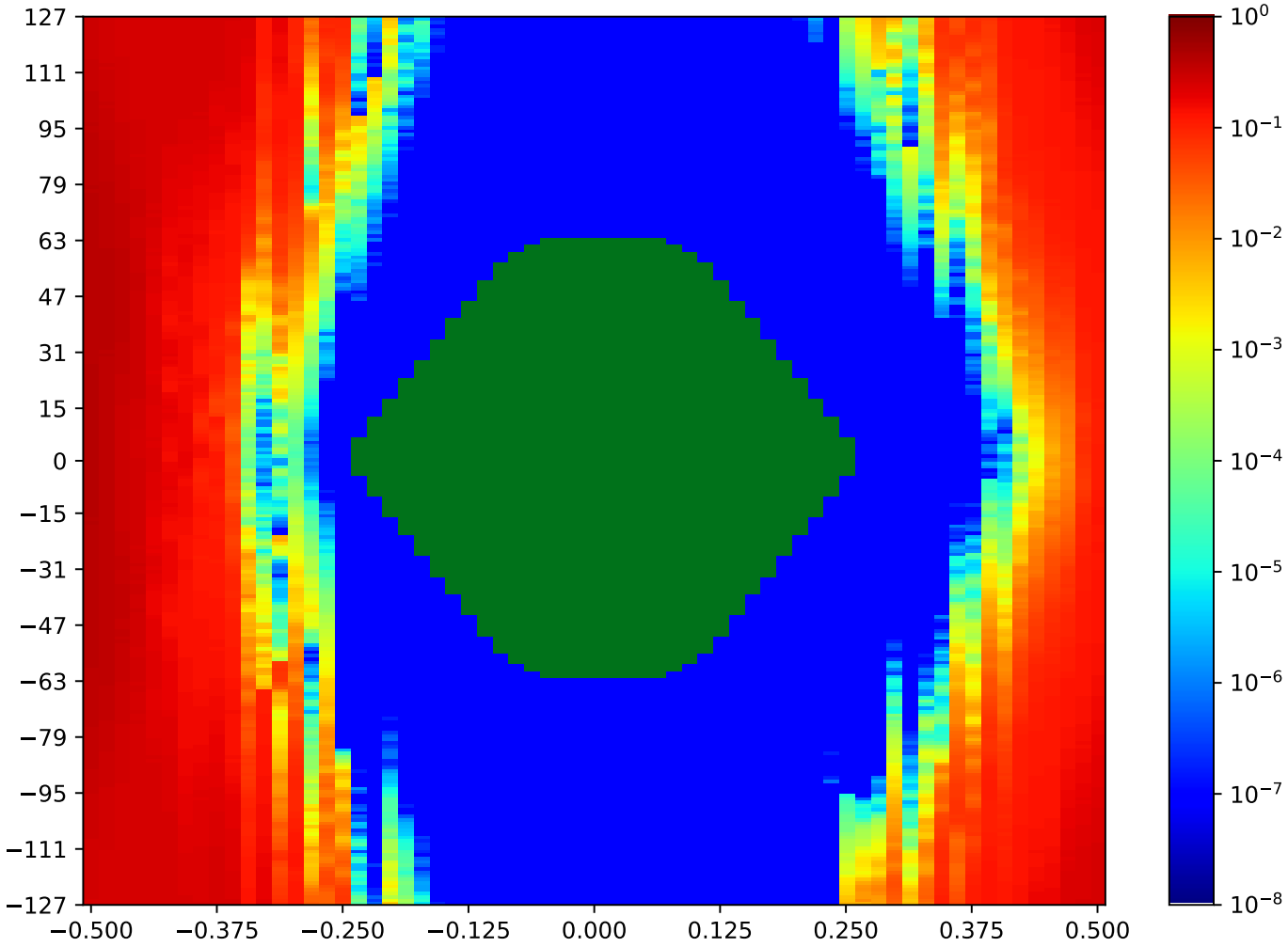


Figure 4.86: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.18 MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Table 4.79: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:16:43		2018-Sep-27 17:17:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9027	49	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

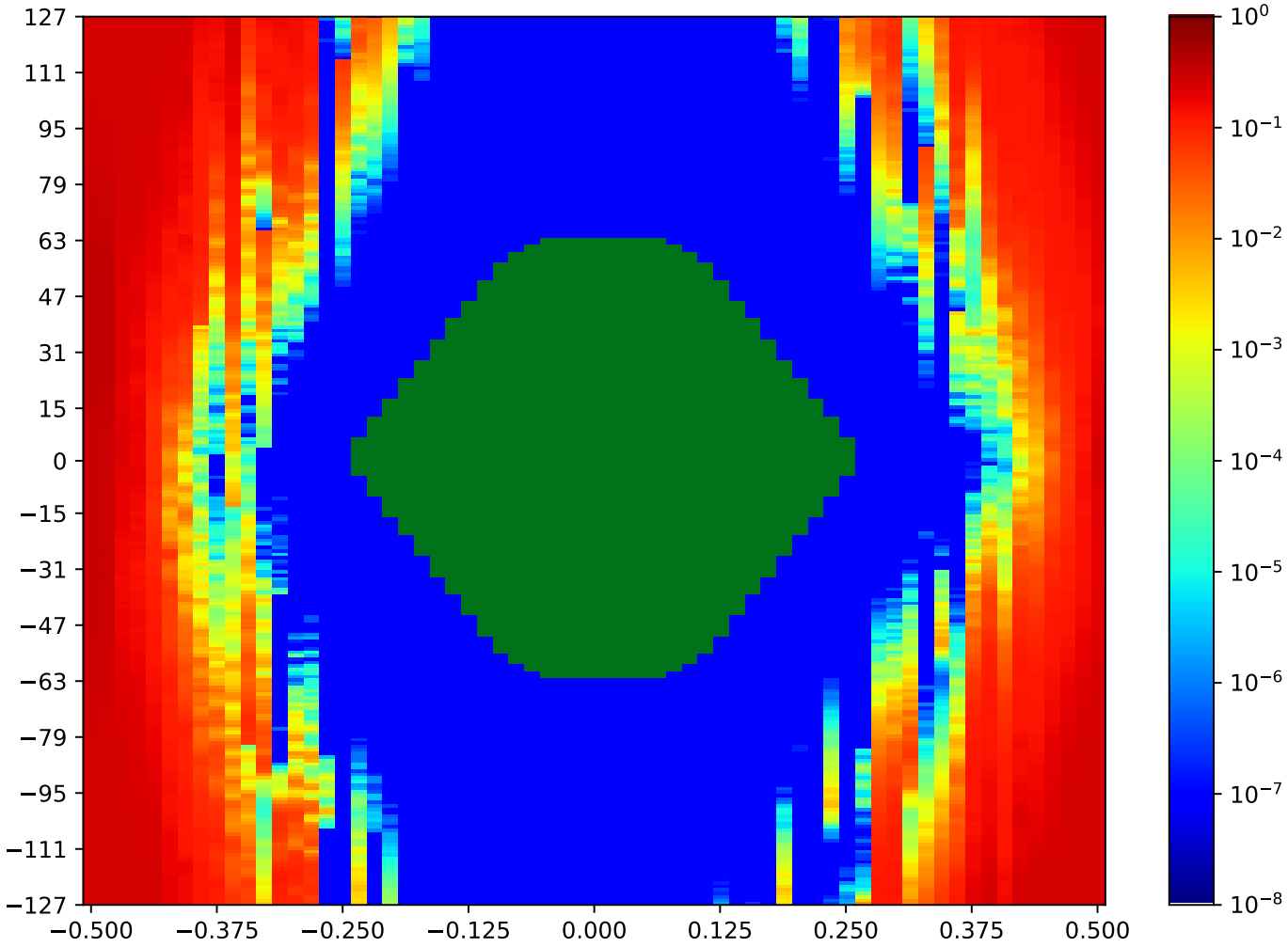


Figure 4.87: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.19 MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Table 4.80: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:17:03		2018-Sep-27 17:17:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8980	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

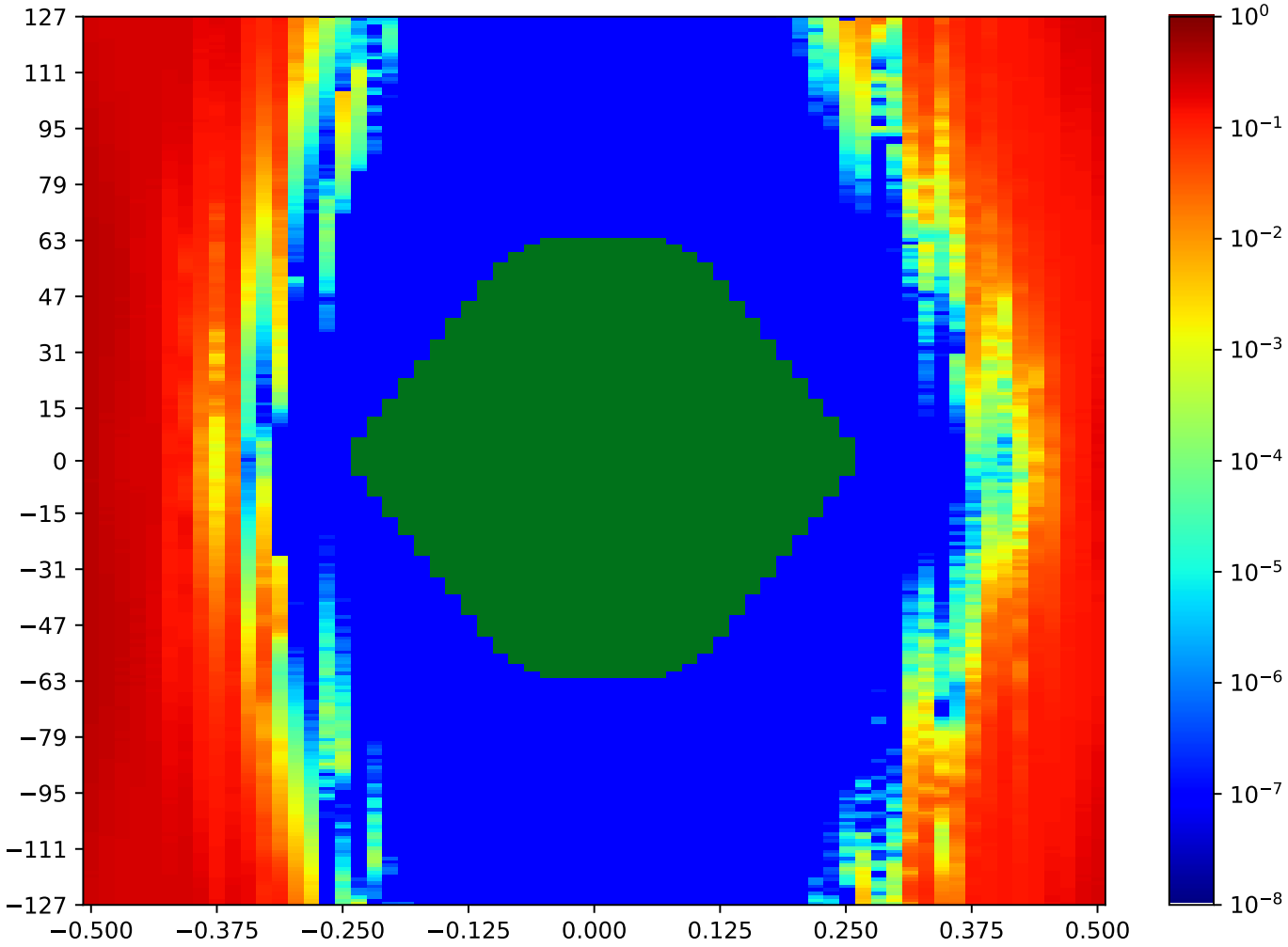


Figure 4.88: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.20 MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Table 4.81: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:17:24		2018-Sep-27 17:17:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8608	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

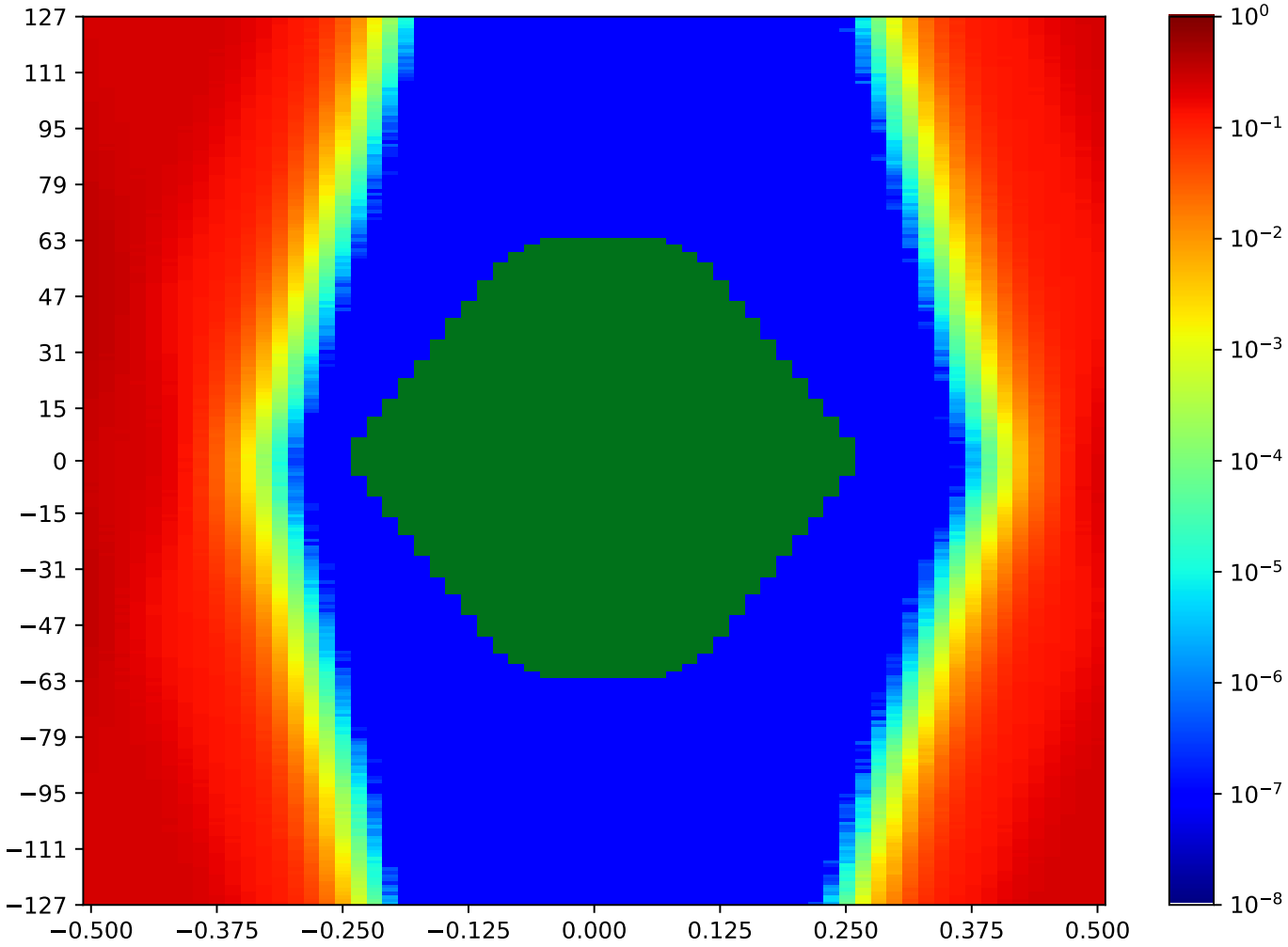


Figure 4.89: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.21 MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Table 4.82: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:17:44		2018-Sep-27 17:18:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8900	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

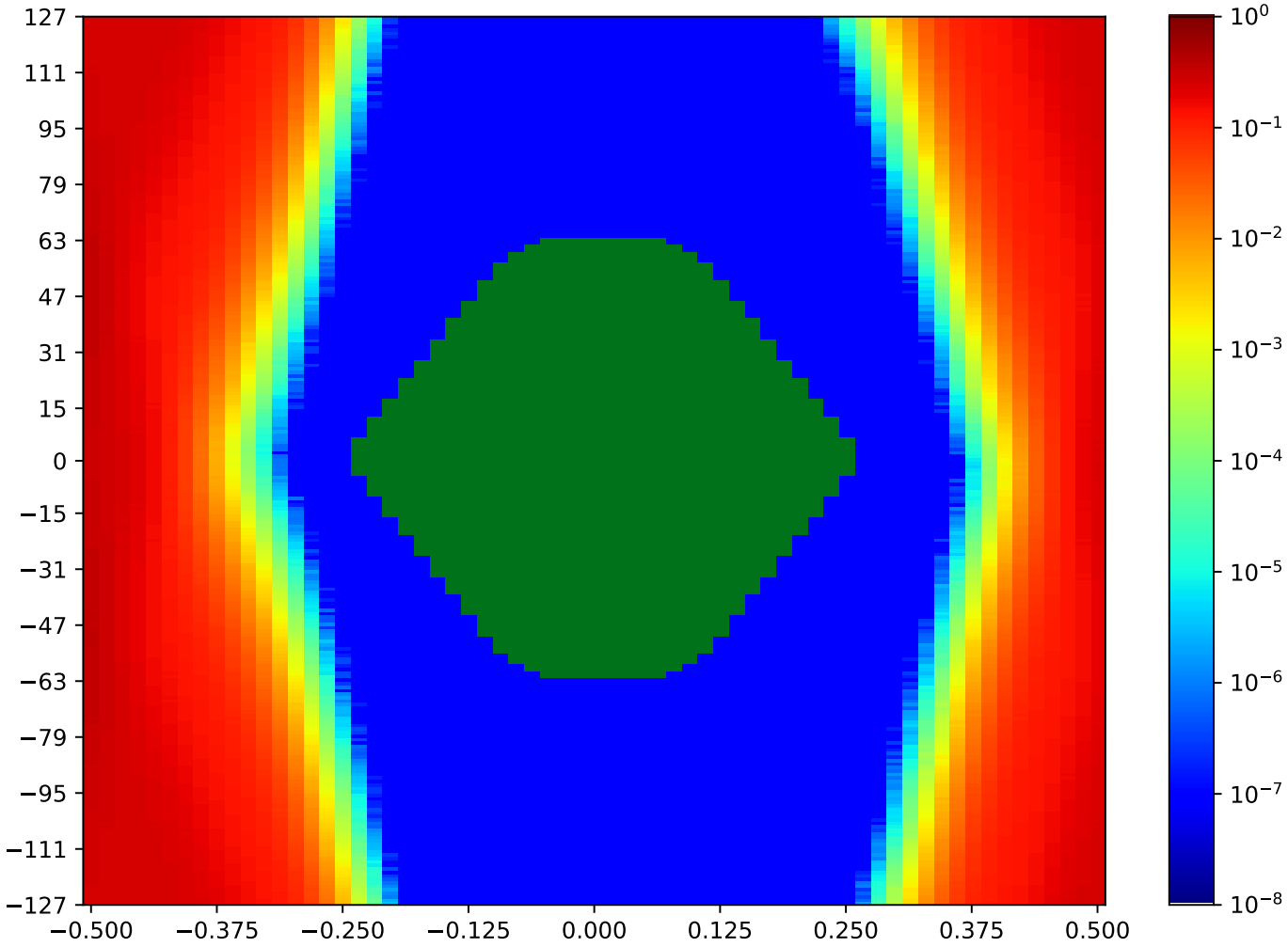


Figure 4.90: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.22 MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Table 4.83: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:18:04		2018-Sep-27 17:18:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8933	48	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

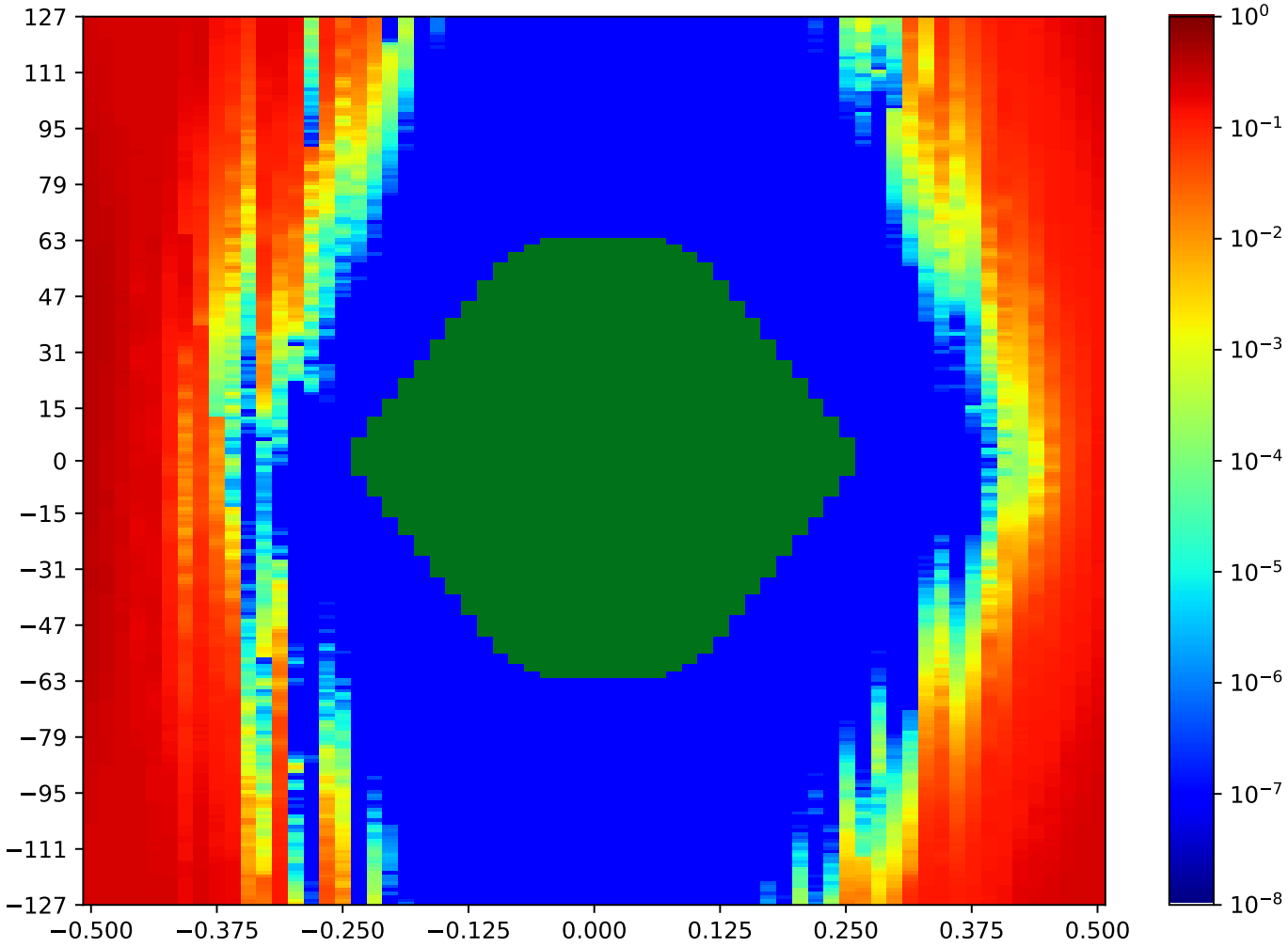


Figure 4.91: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.23 MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Table 4.84: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:18:25		2018-Sep-27 17:18:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8248	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

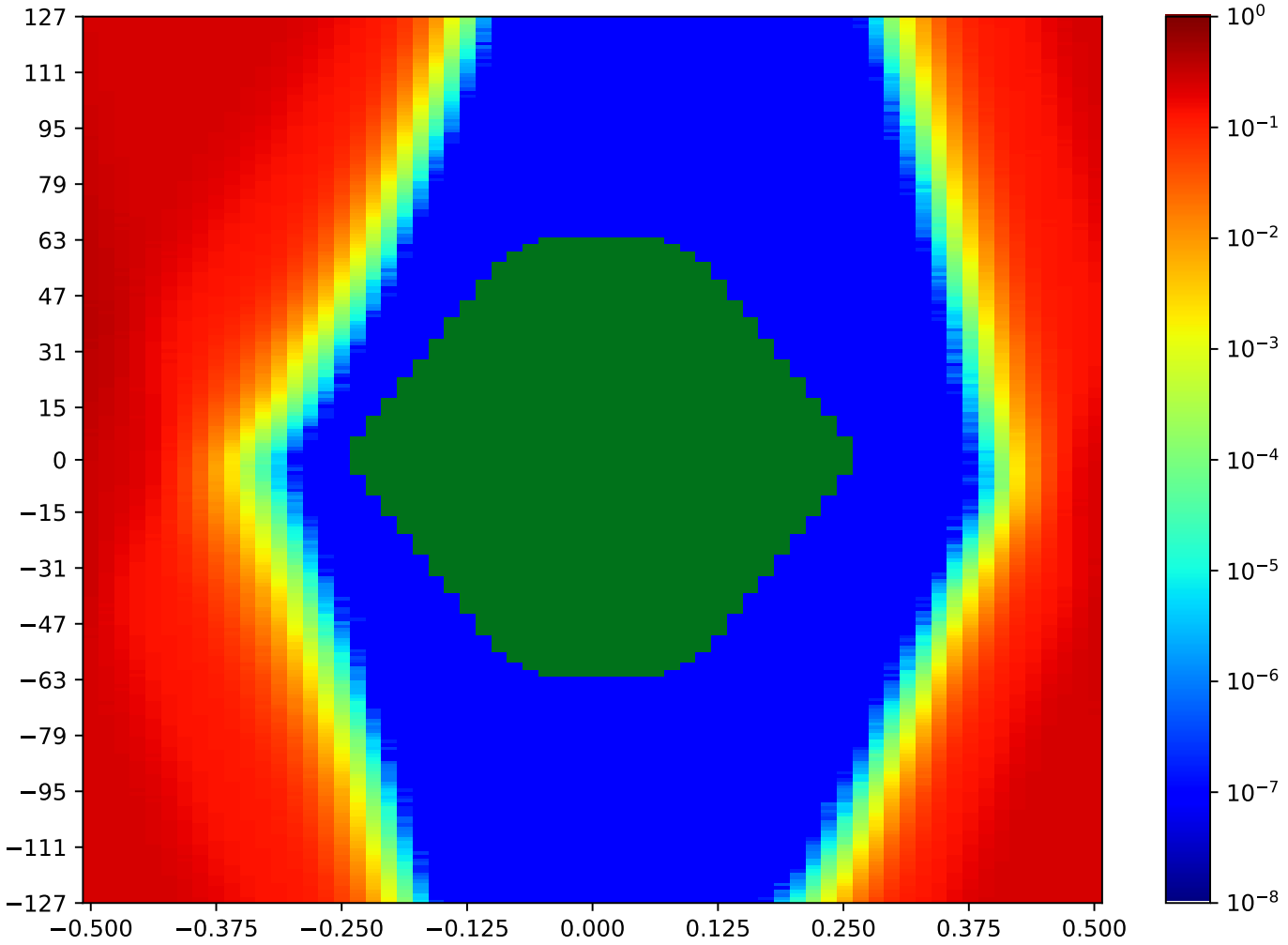


Figure 4.92: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.24 MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Table 4.85: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:18:45		2018-Sep-27 17:19:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8629	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

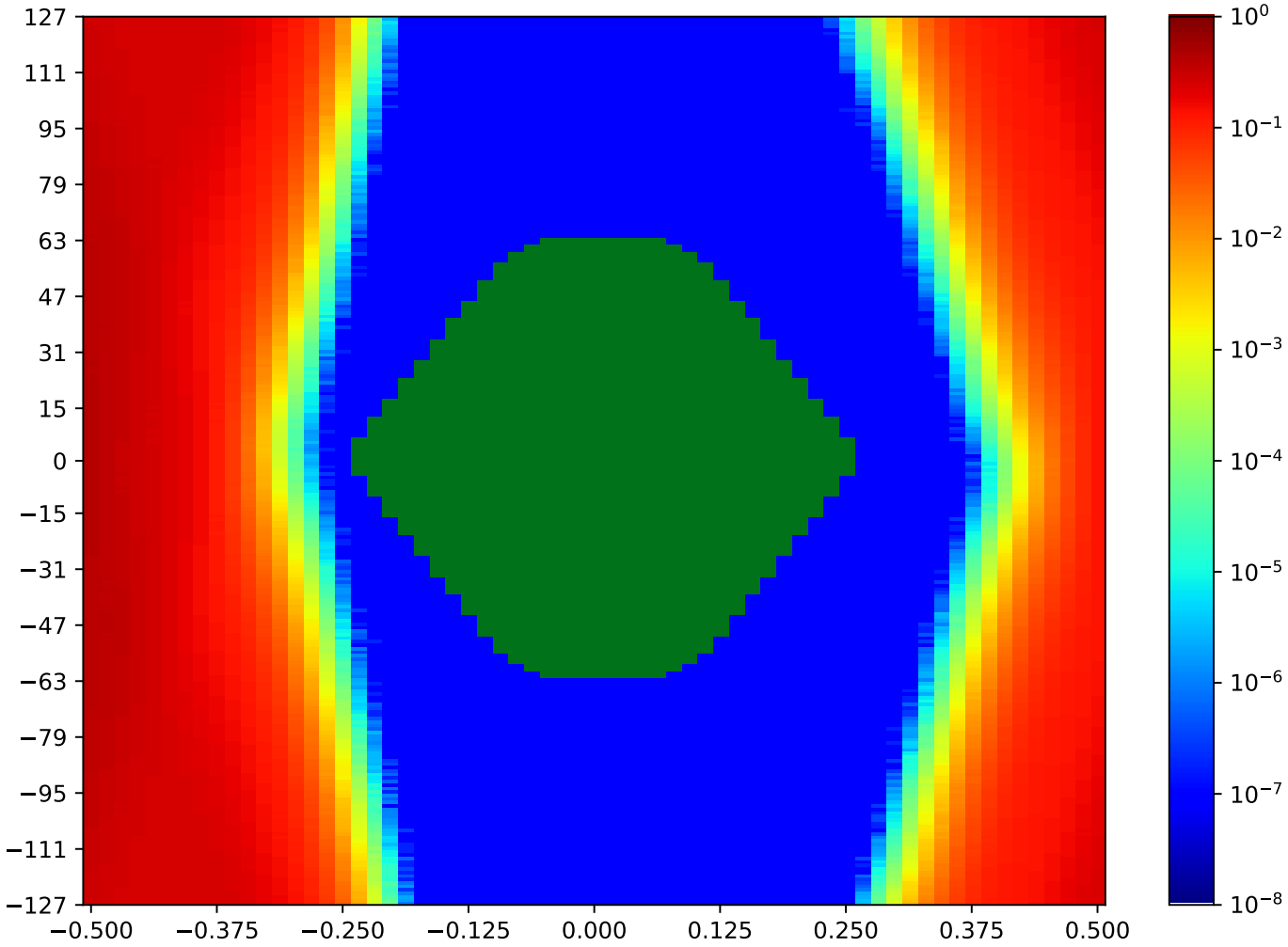


Figure 4.93: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.25 MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Table 4.86: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:19:06		2018-Sep-27 17:19:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8082	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

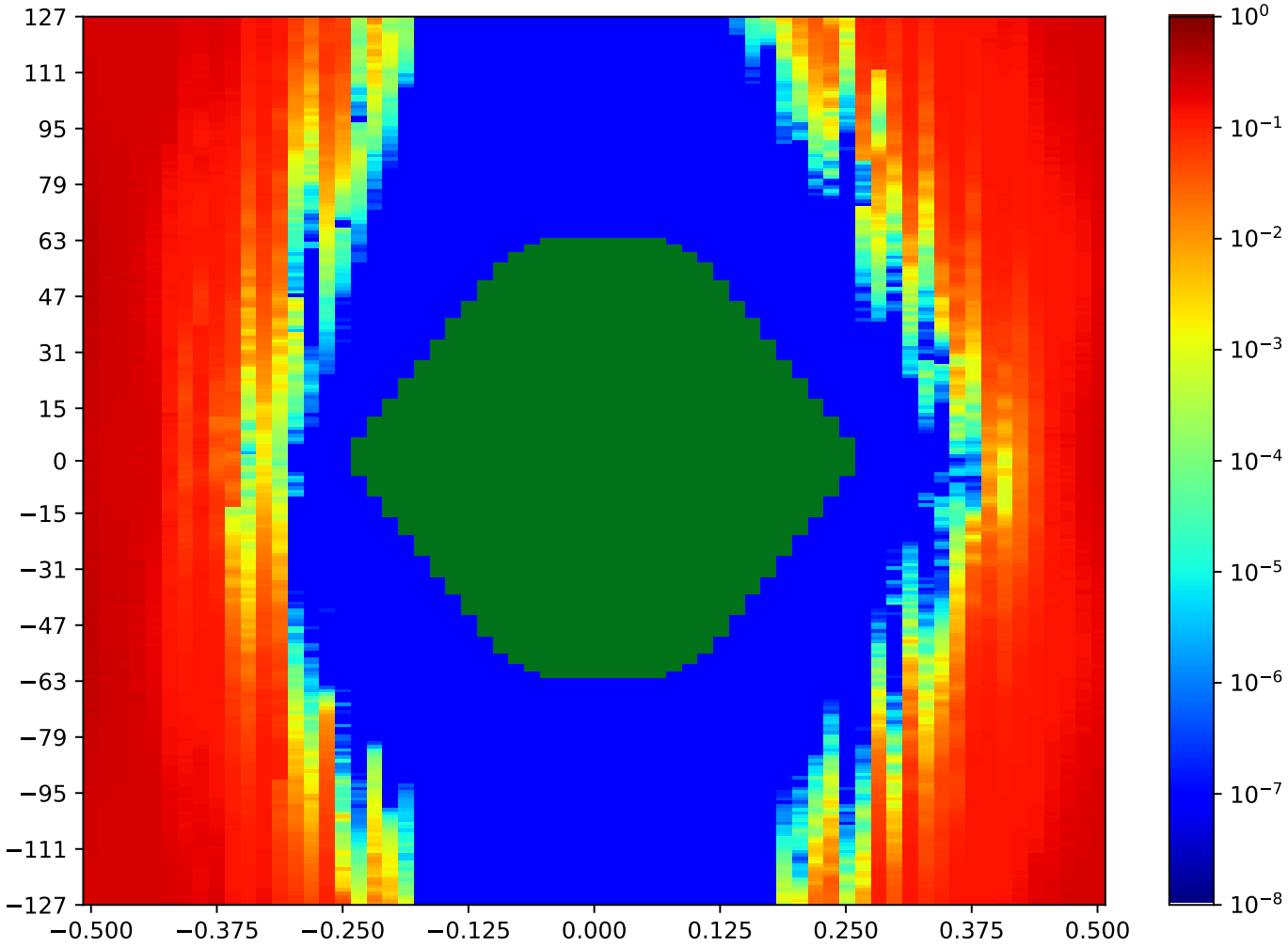


Figure 4.94: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.26 MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Table 4.87: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:19:26		2018-Sep-27 17:19:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10222	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

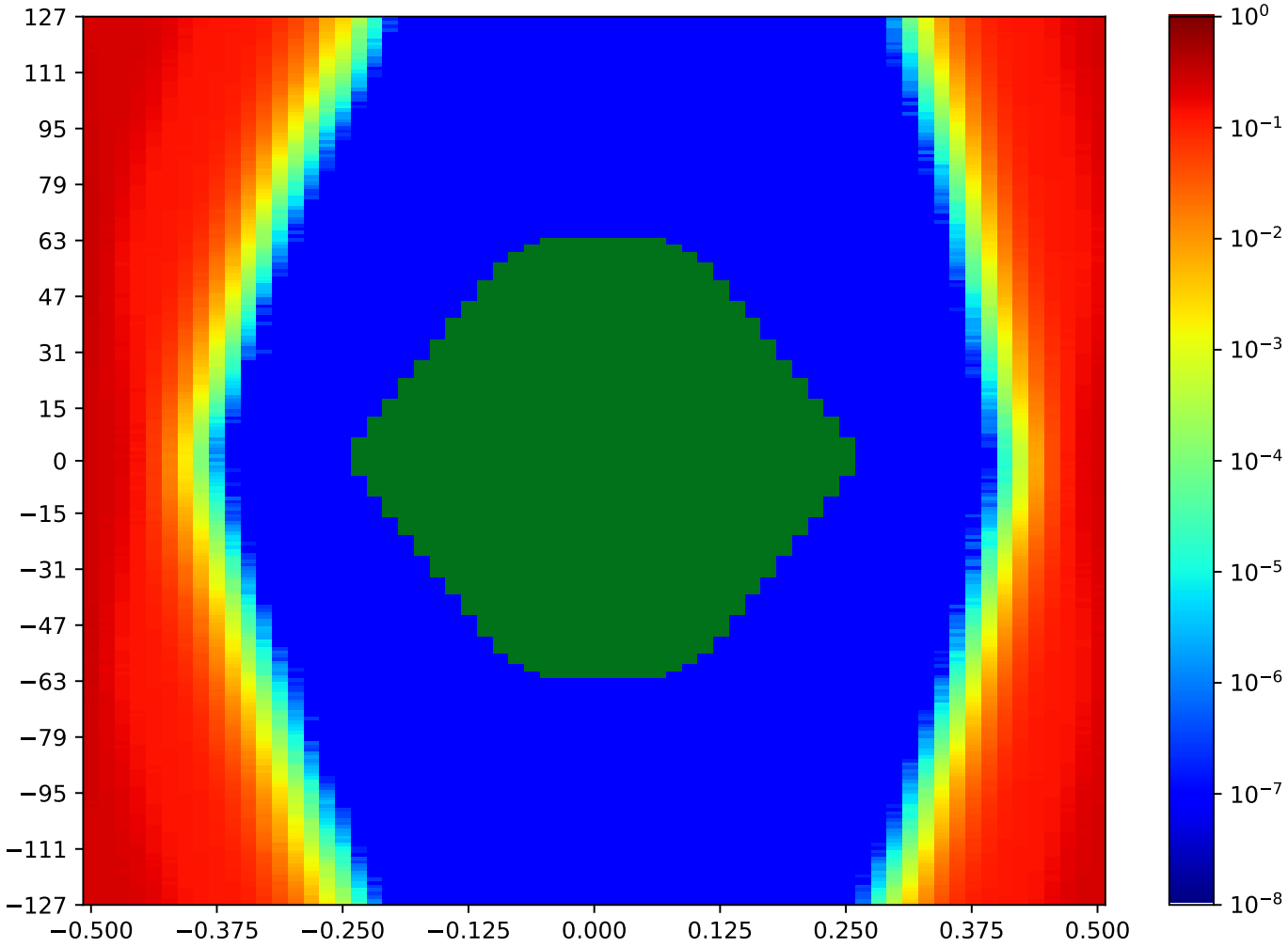


Figure 4.95: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.27 MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Table 4.88: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:19:46		2018-Sep-27 17:20:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9305	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

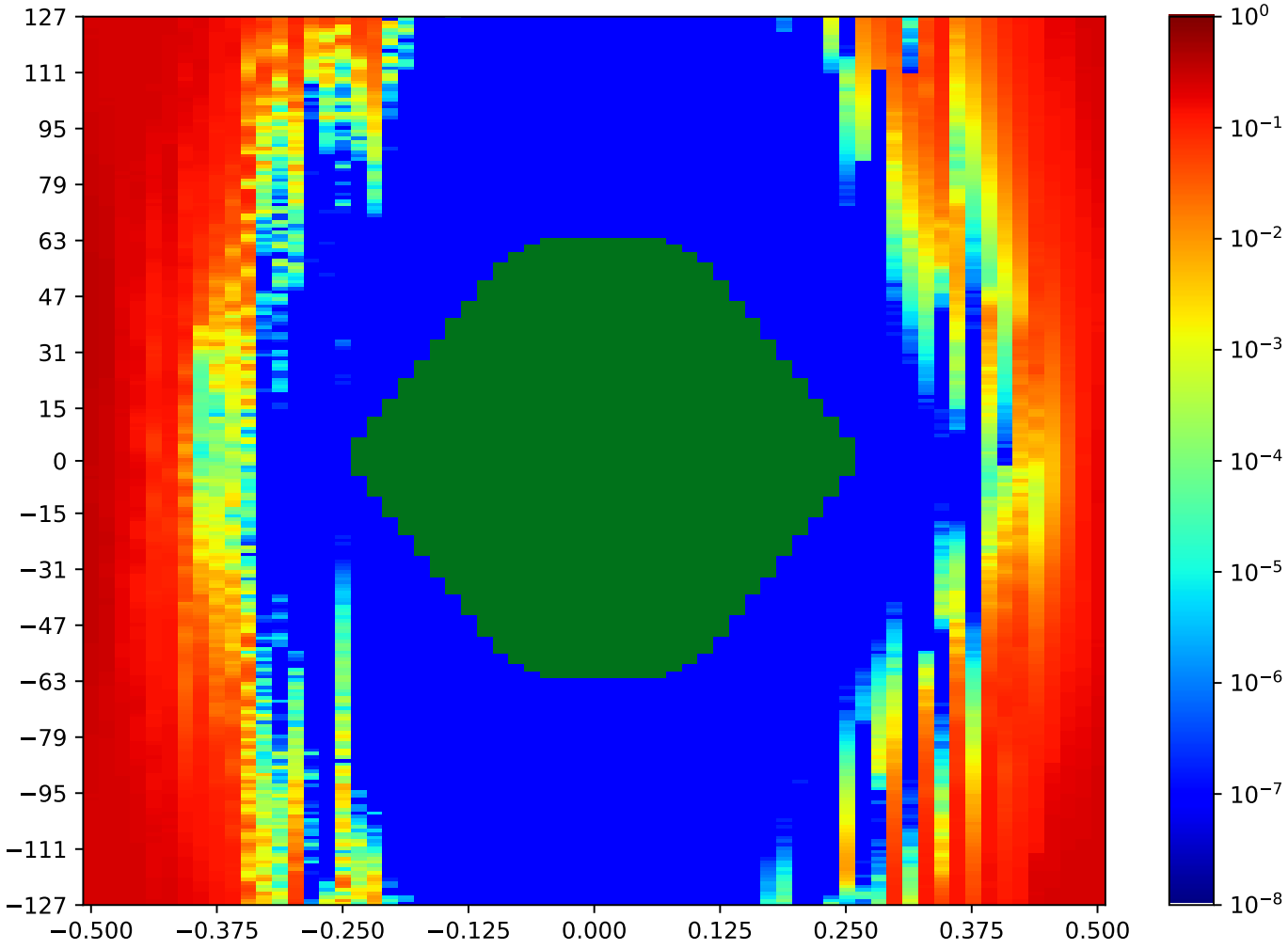


Figure 4.96: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.8.28 MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Table 4.89: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:20:07		2018-Sep-27 17:20:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9768	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

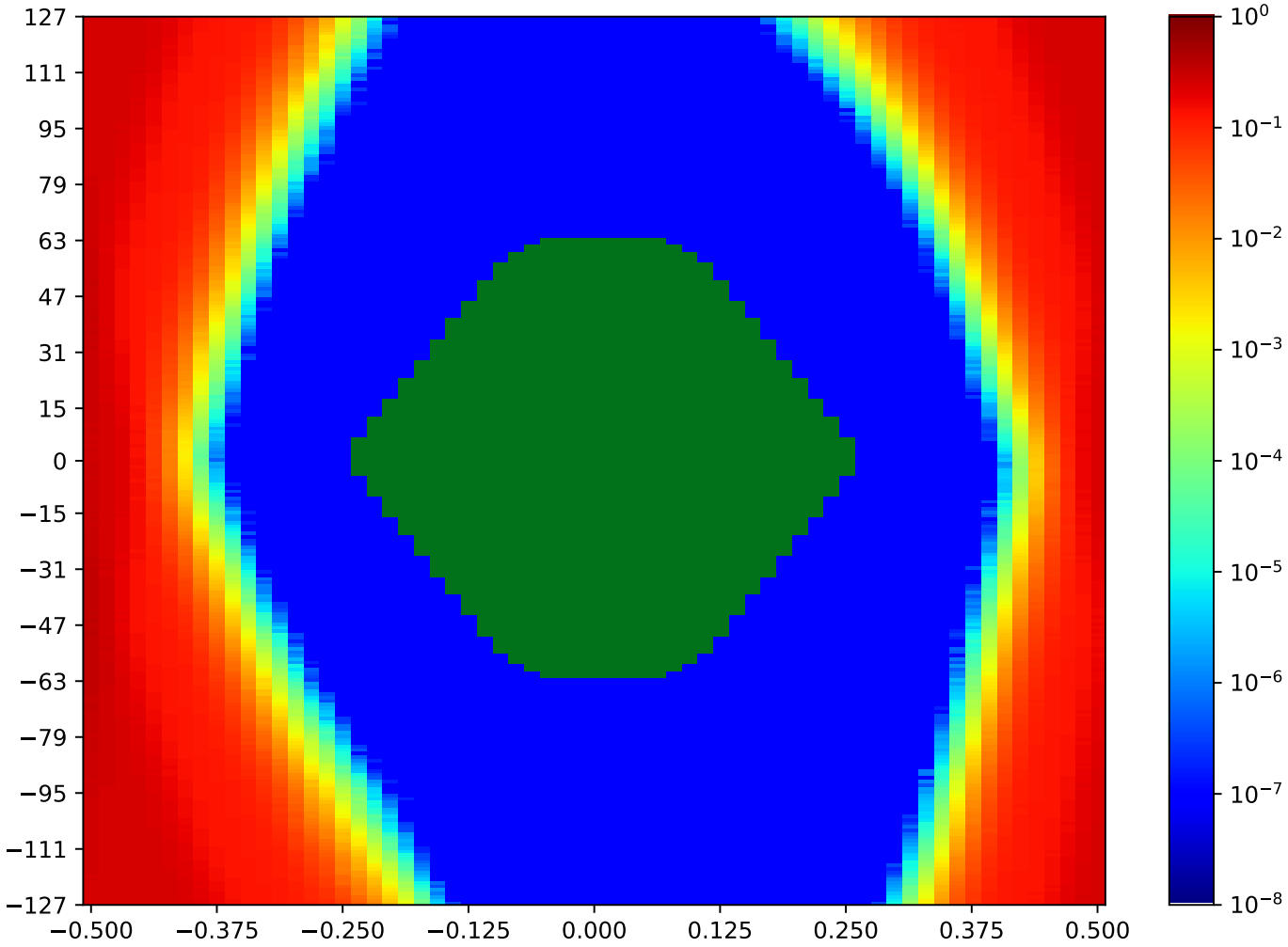


Figure 4.97: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9 MSP_C TRP On board links

A cross-reference to Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.127.

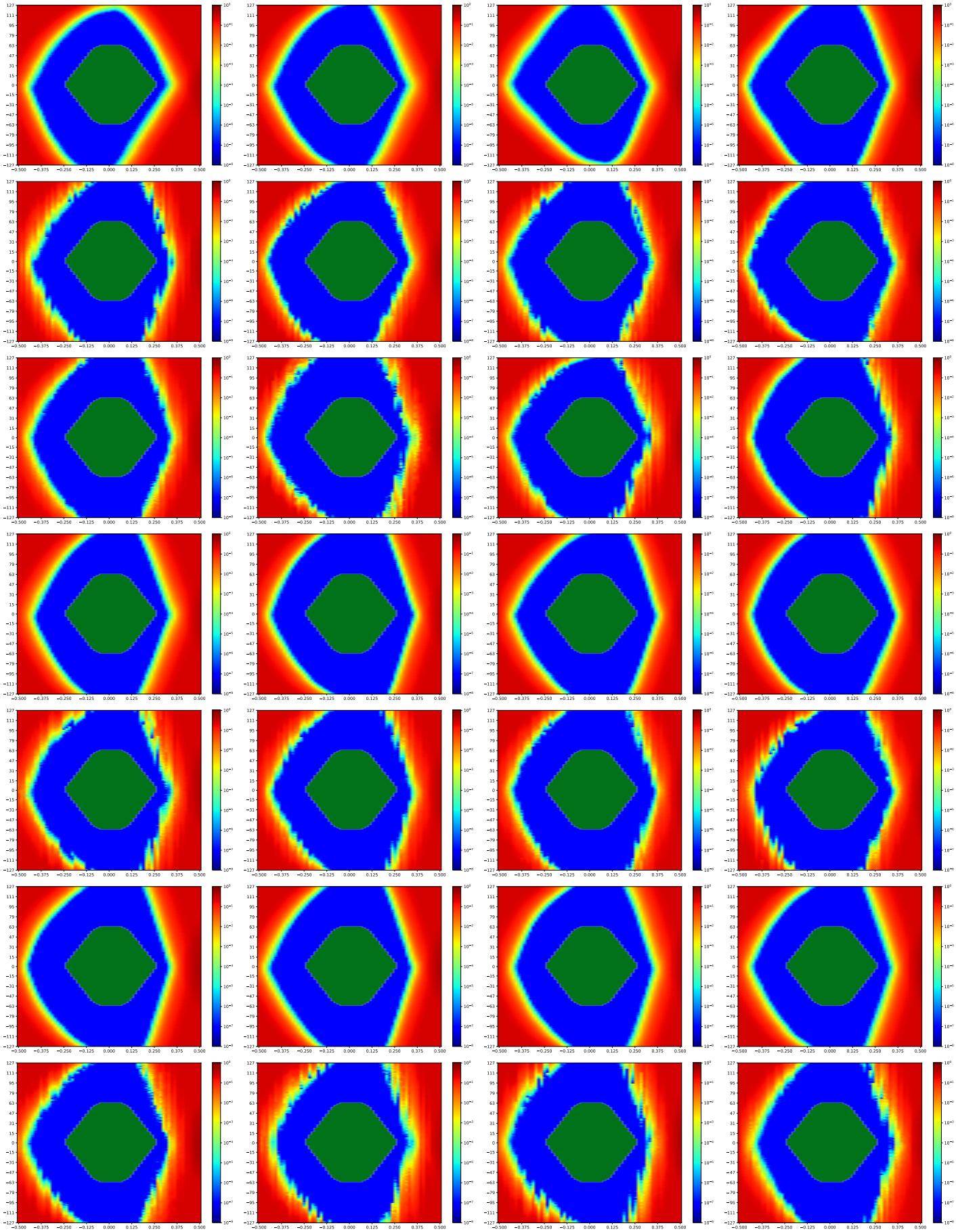


Figure 4.98: MSP_C TRP On board links

4.9.1 MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Table 4.90: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:20:28		2018-Sep-27 17:20:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7289	45	69.23%	243	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

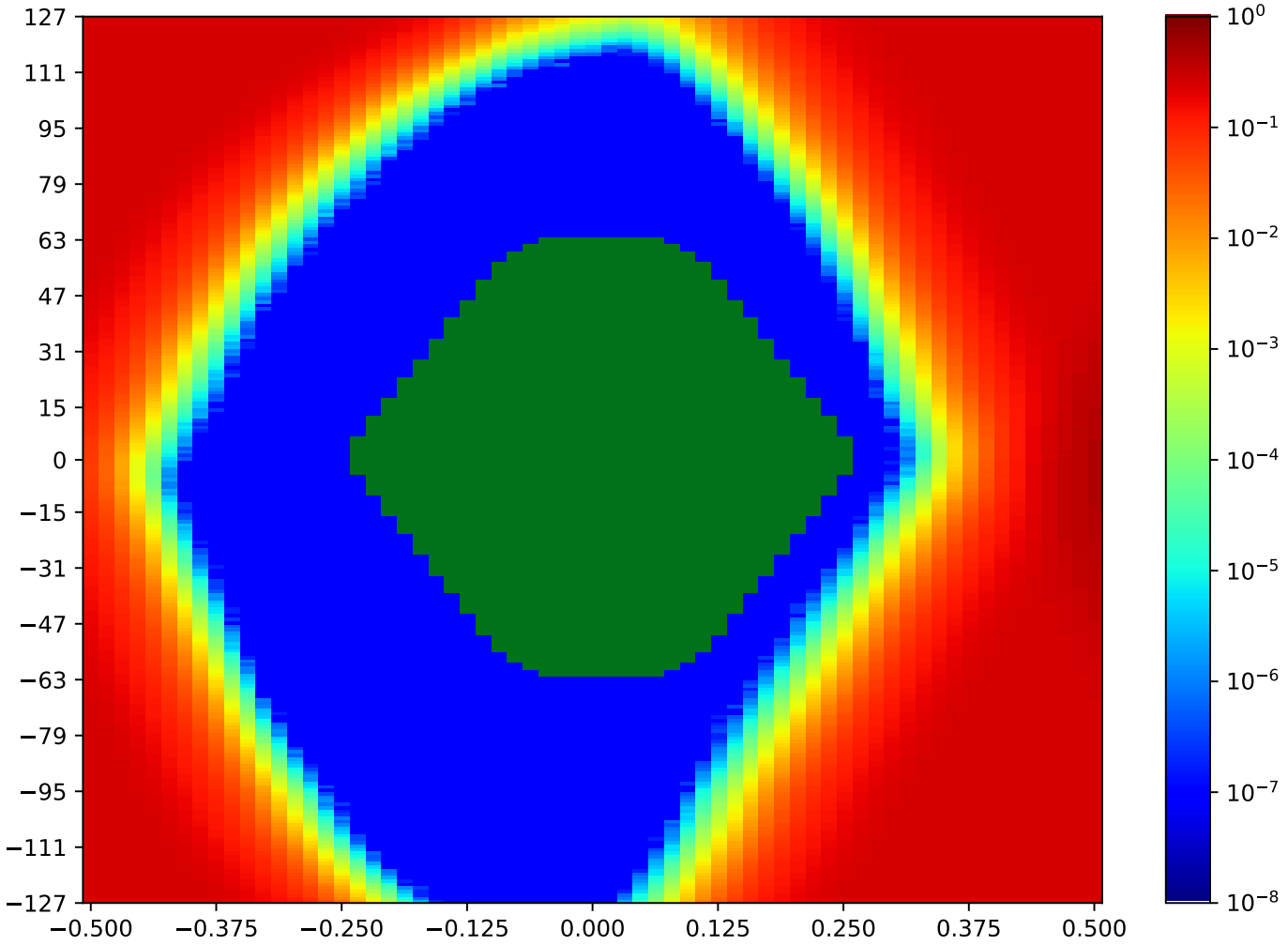


Figure 4.99: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.2 MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Table 4.91: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:20:48		2018-Sep-27 17:21:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7647	45	69.23%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

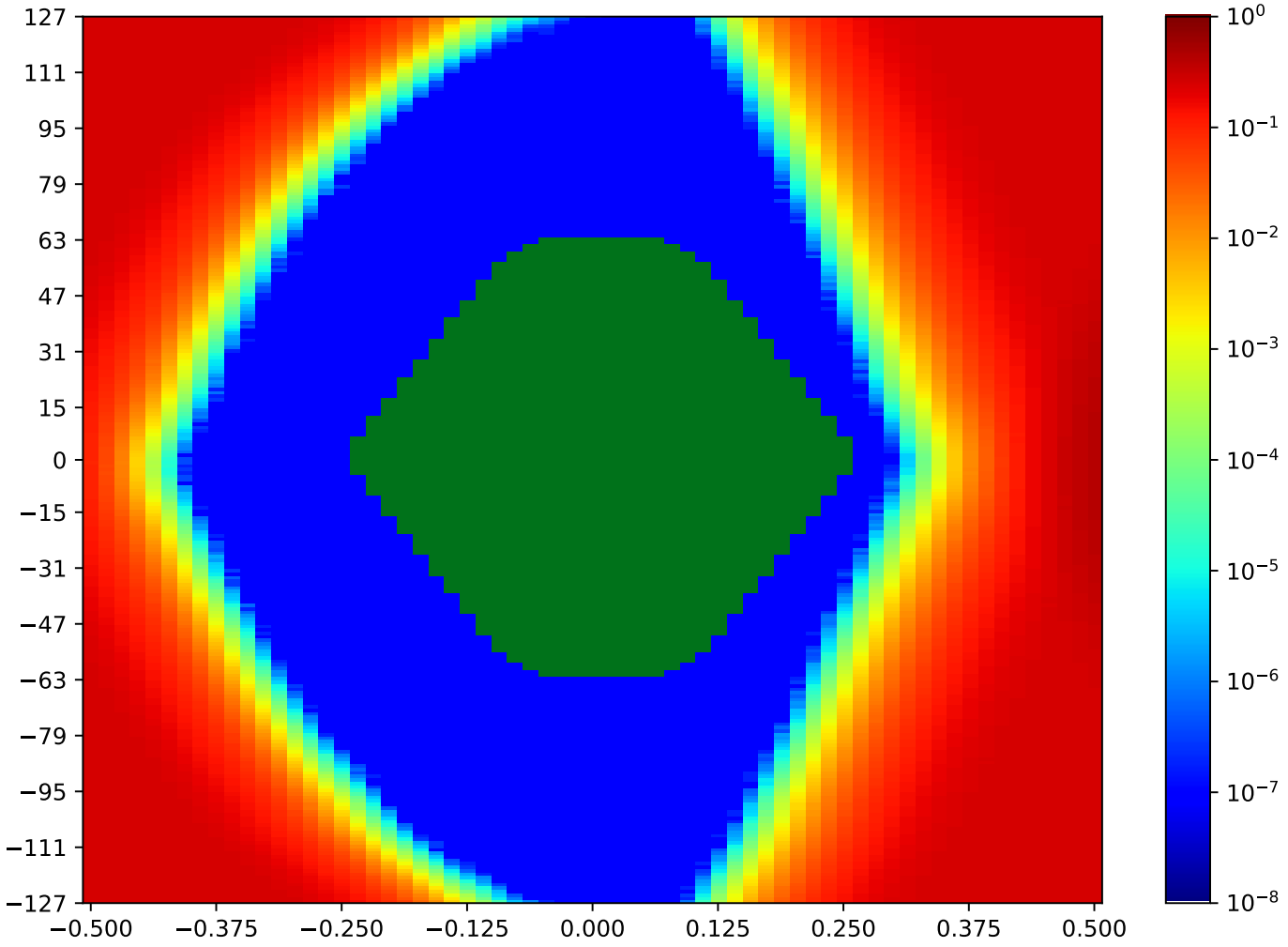


Figure 4.100: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.3 MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Table 4.92: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:21:08		2018-Sep-27 17:21:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7237	44	67.69%	244	95.29%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

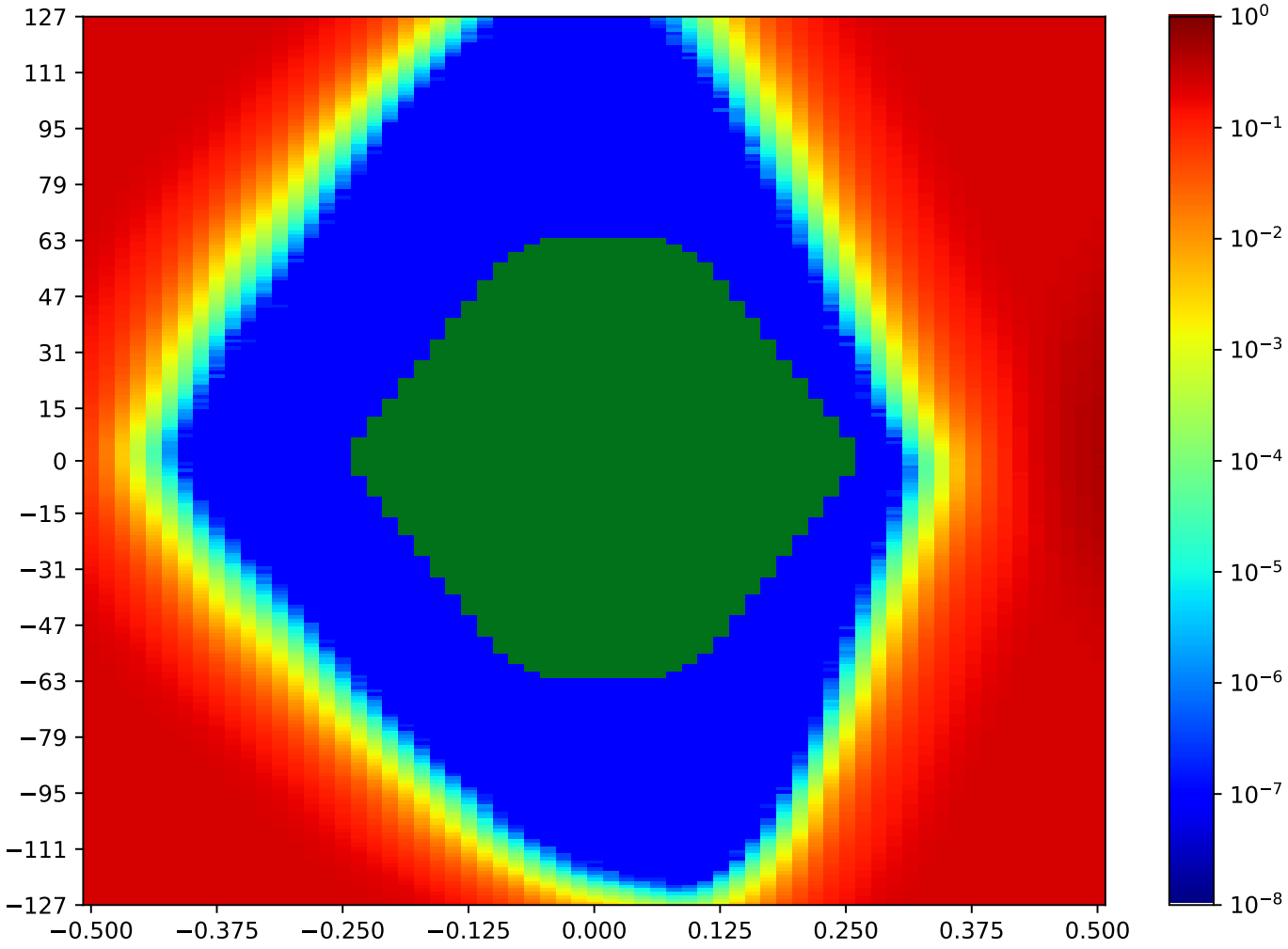


Figure 4.101: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.4 MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Table 4.93: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:21:29		2018-Sep-27 17:21:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8569	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

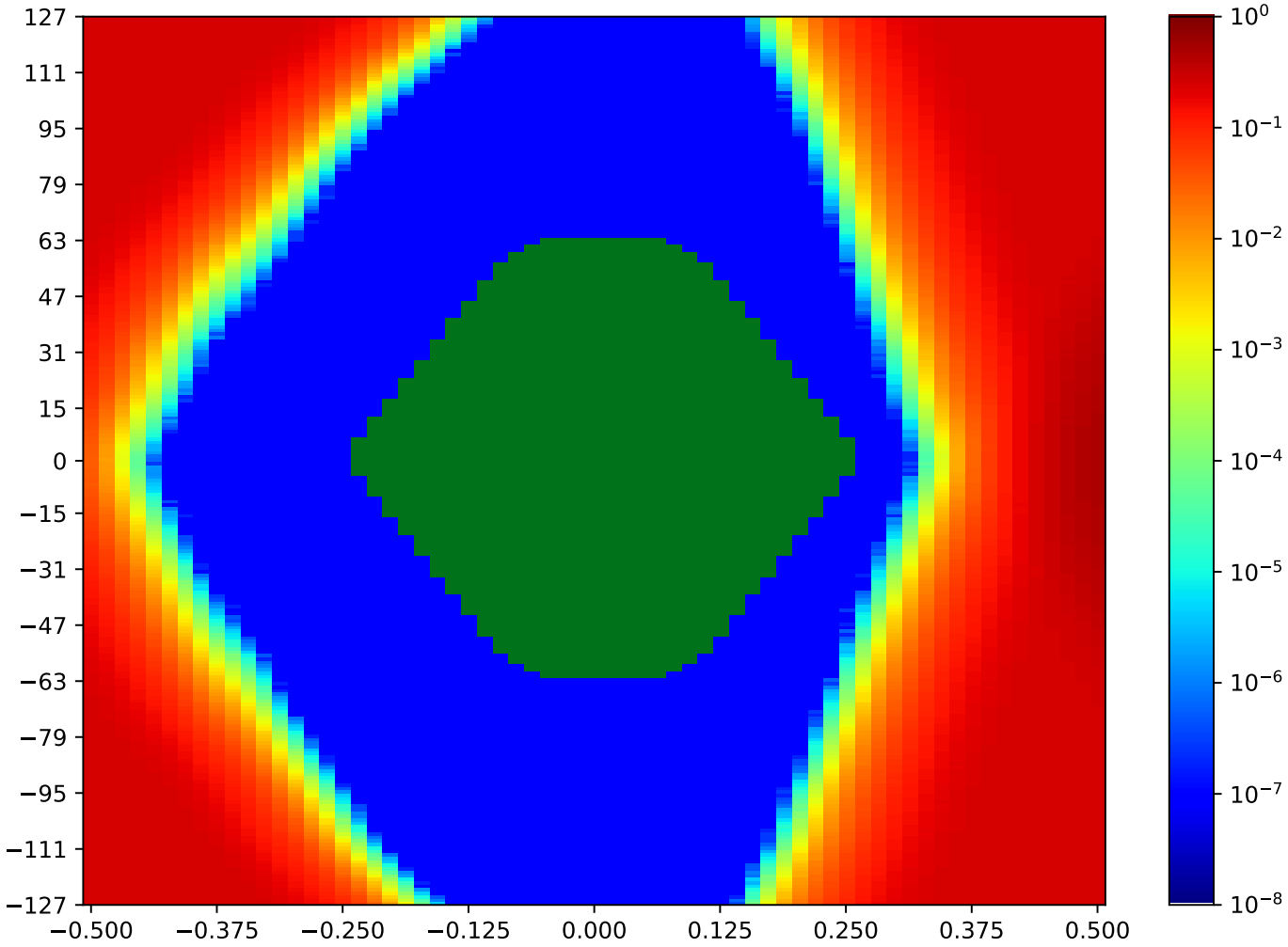


Figure 4.102: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.5 MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Table 4.94: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:21:50		2018-Sep-27 17:22:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8625	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

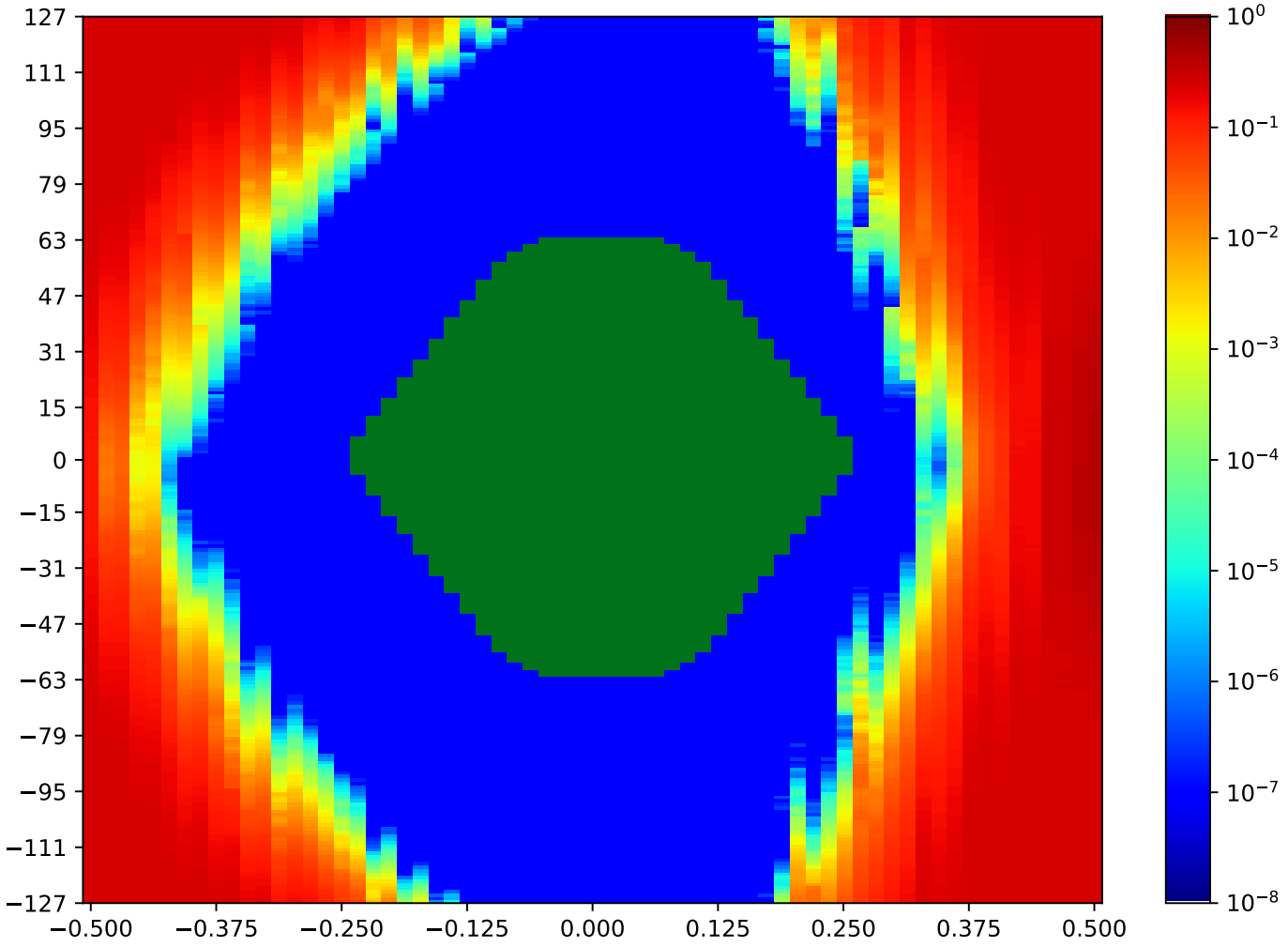


Figure 4.103: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.6 MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Table 4.95: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:22:10		2018-Sep-27 17:22:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8721	48	73.85%	254	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

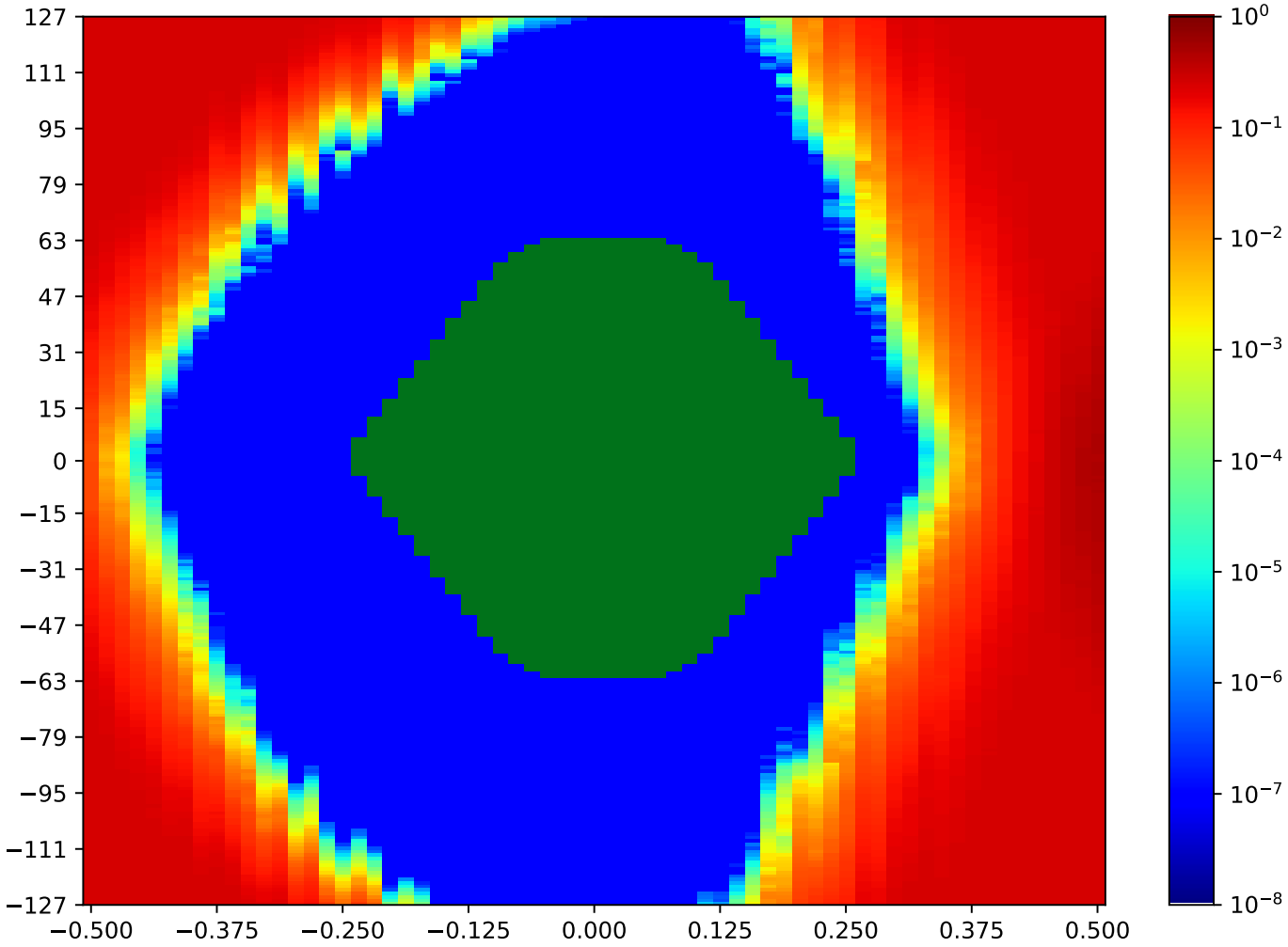


Figure 4.104: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.7 MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Table 4.96: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:22:31		2018-Sep-27 17:22:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8872	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

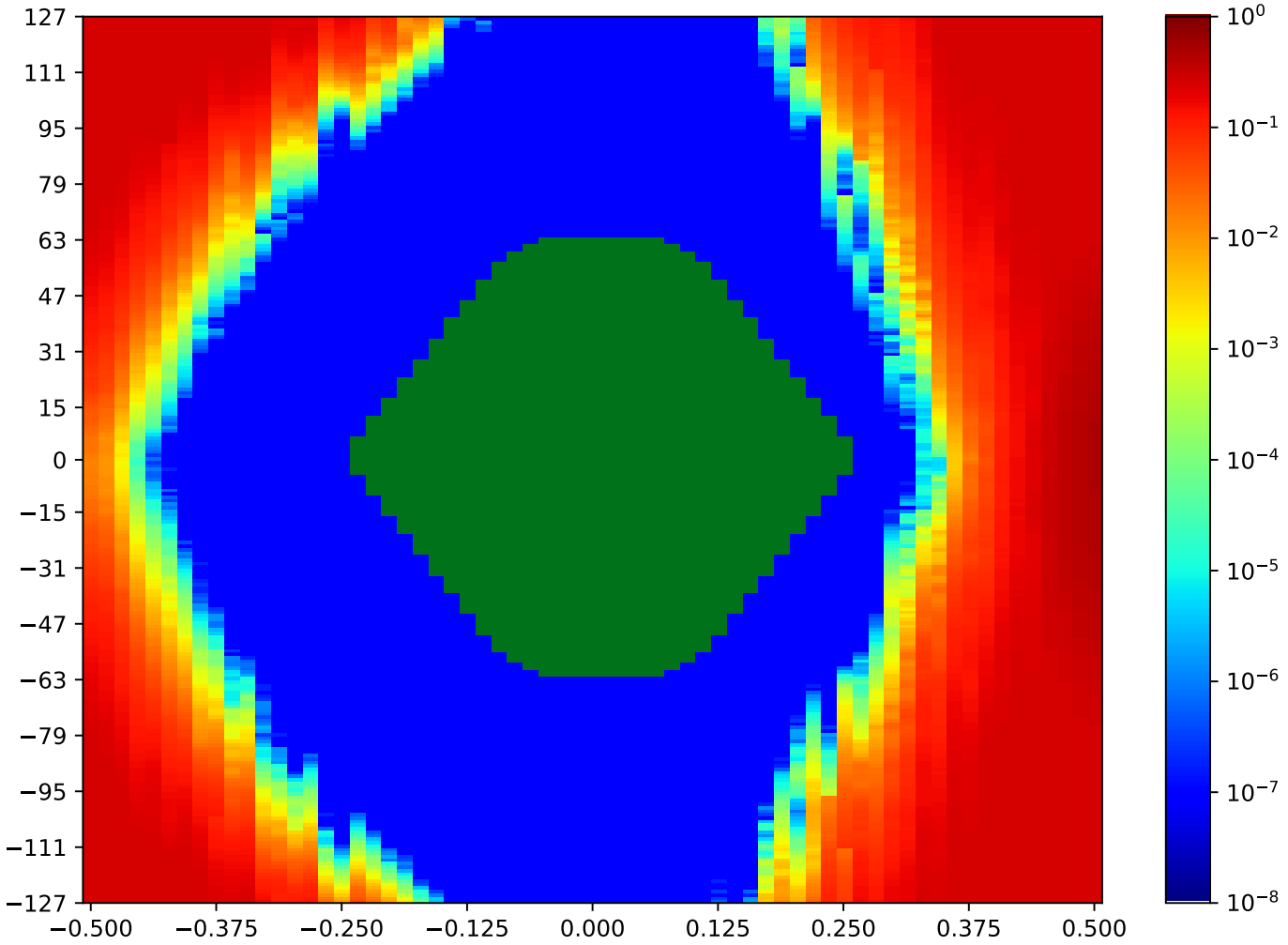


Figure 4.105: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.8 MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Table 4.97: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:22:51		2018-Sep-27 17:23:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9100	49	75.38%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

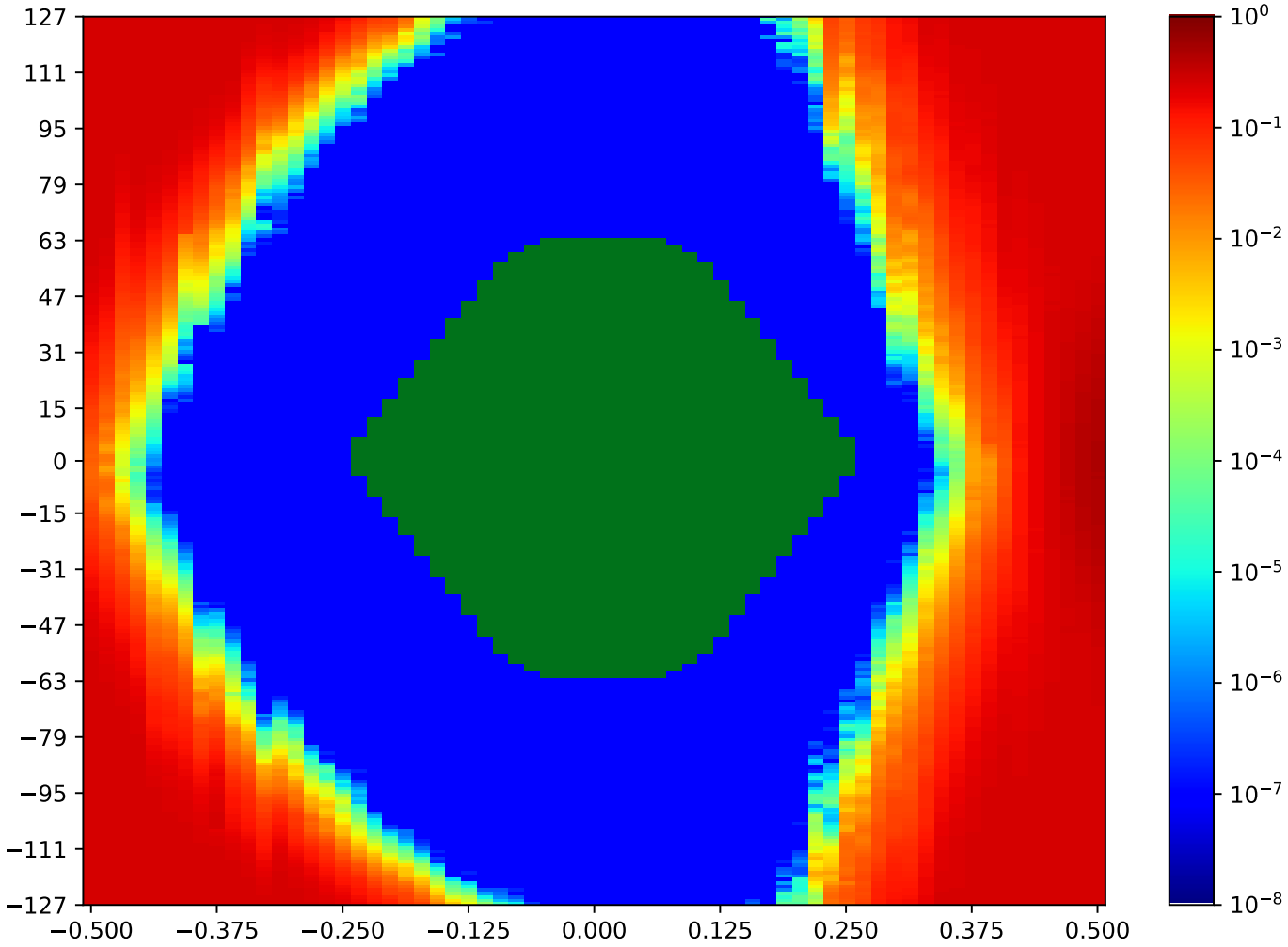


Figure 4.106: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.9 MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Table 4.98: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:23:11		2018-Sep-27 17:23:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8875	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

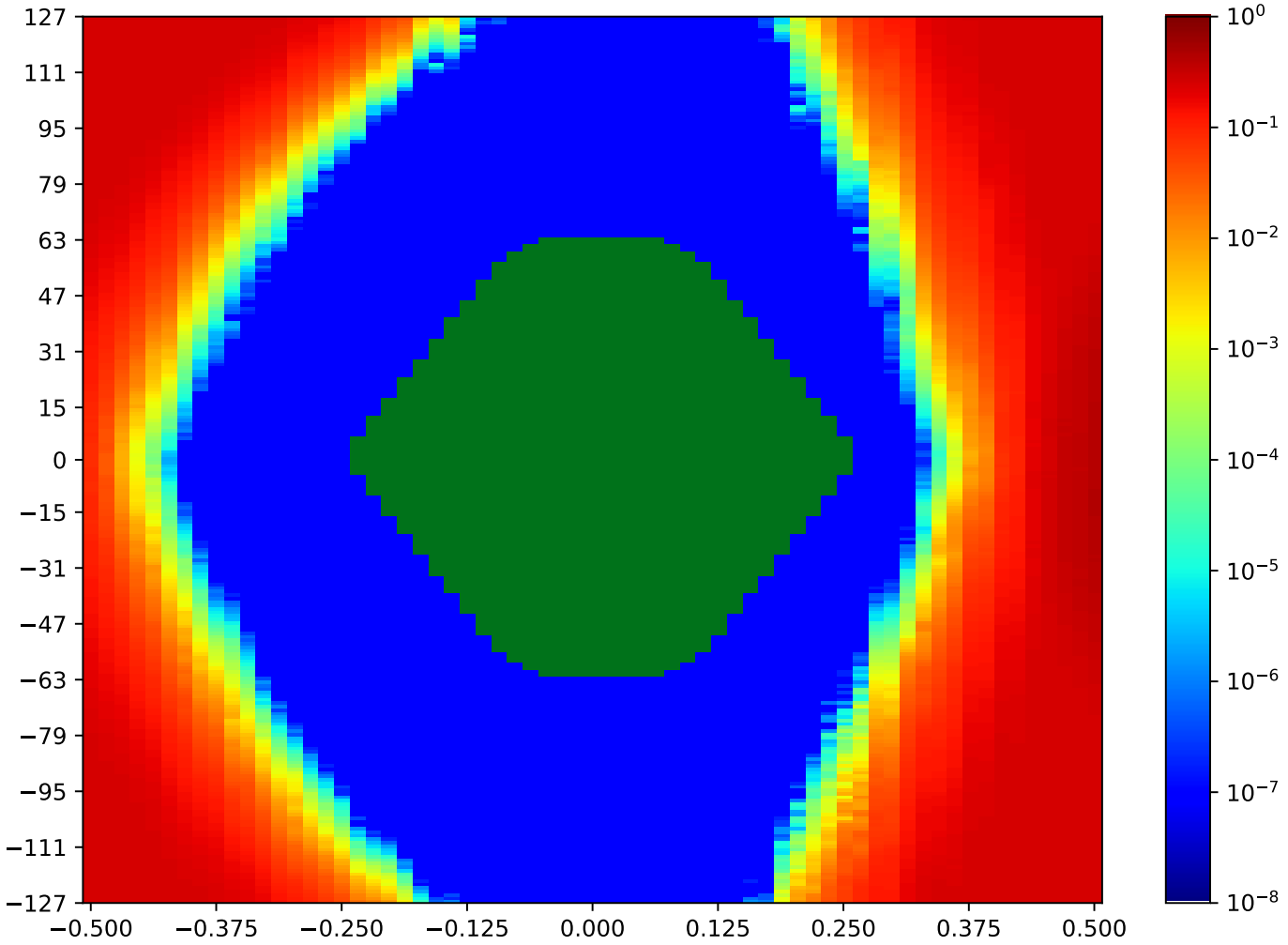


Figure 4.107: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.10 MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Table 4.99: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:23:32		2018-Sep-27 17:23:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9068	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

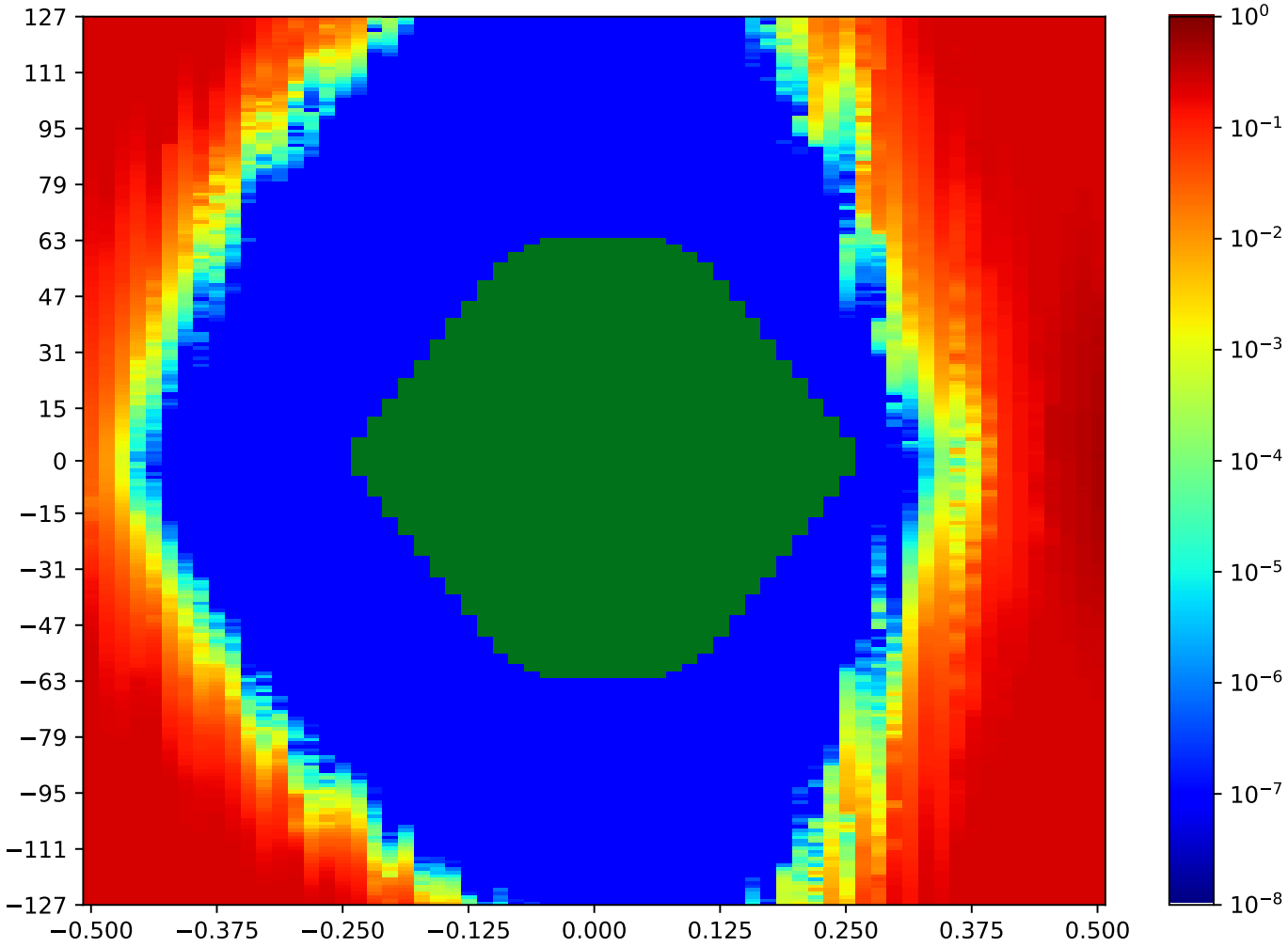


Figure 4.108: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.11 MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Table 4.100: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:23:52		2018-Sep-27 17:24:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8236	49	73.85%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

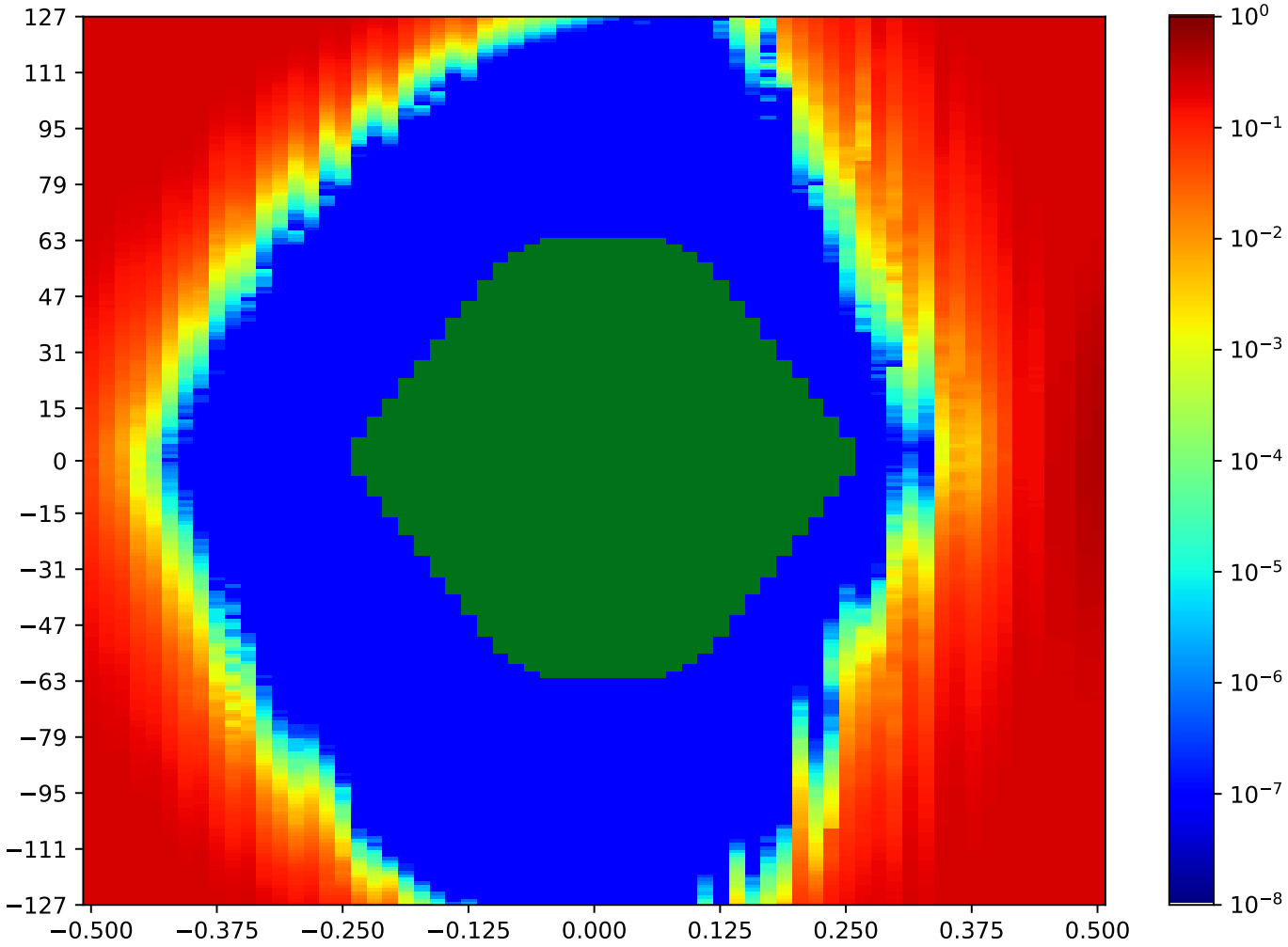


Figure 4.109: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.12 MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Table 4.101: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:24:12		2018-Sep-27 17:24:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8975	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

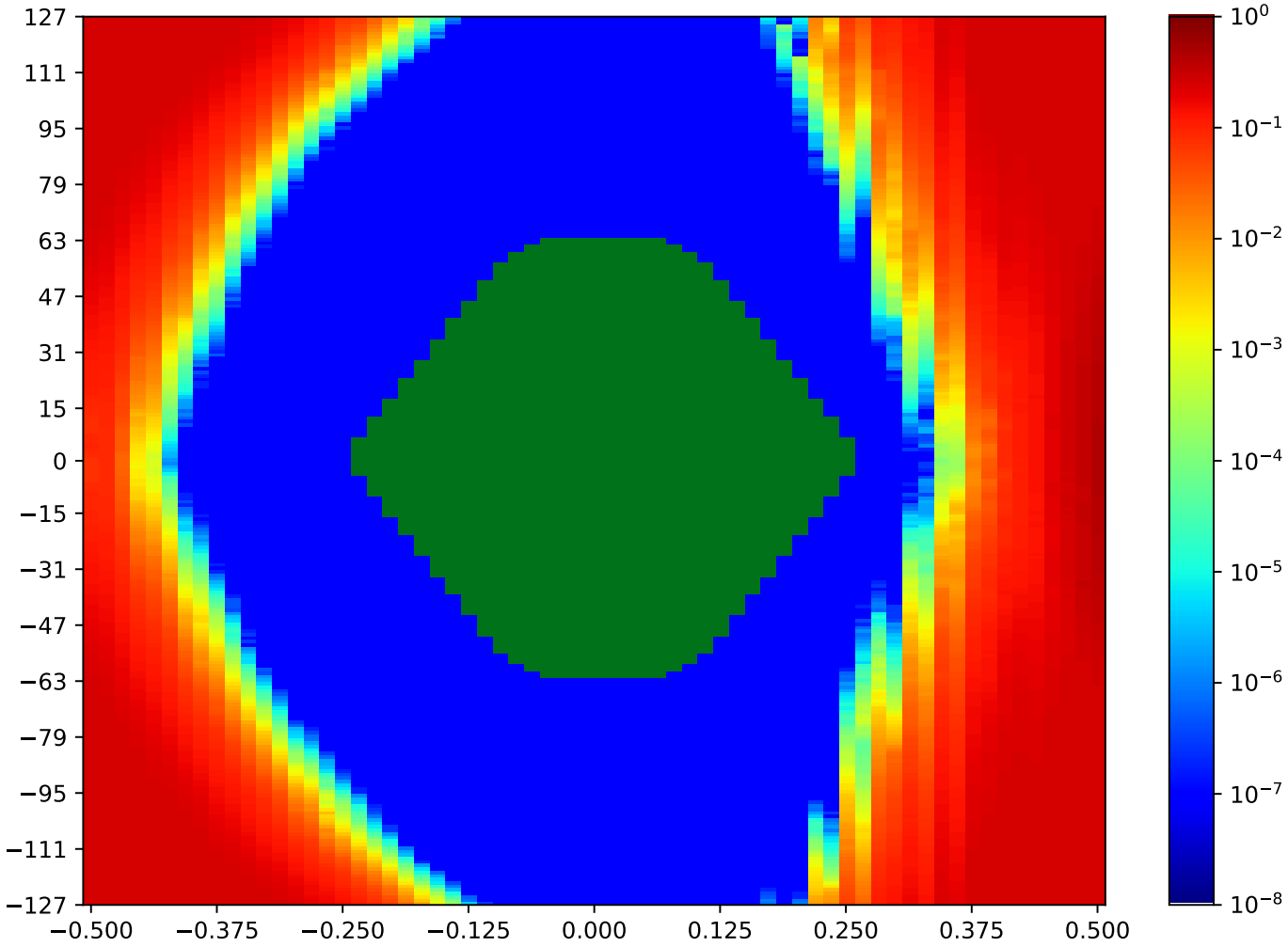


Figure 4.110: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.13 MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Table 4.102: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:24:33		2018-Sep-27 17:24:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8256	45	69.23%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

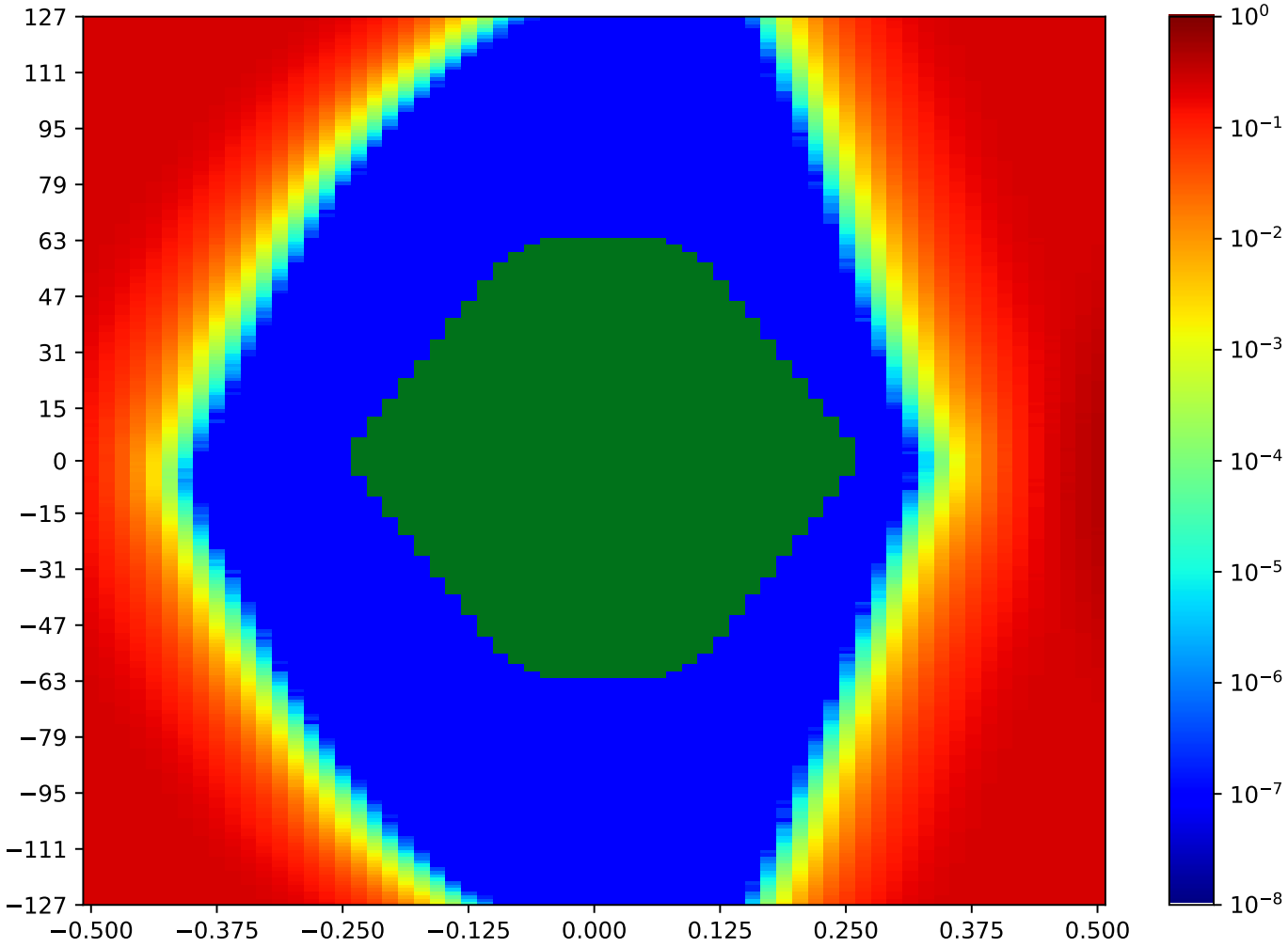


Figure 4.111: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.14 MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Table 4.103: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:24:53		2018-Sep-27 17:25:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9190	48	73.85%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

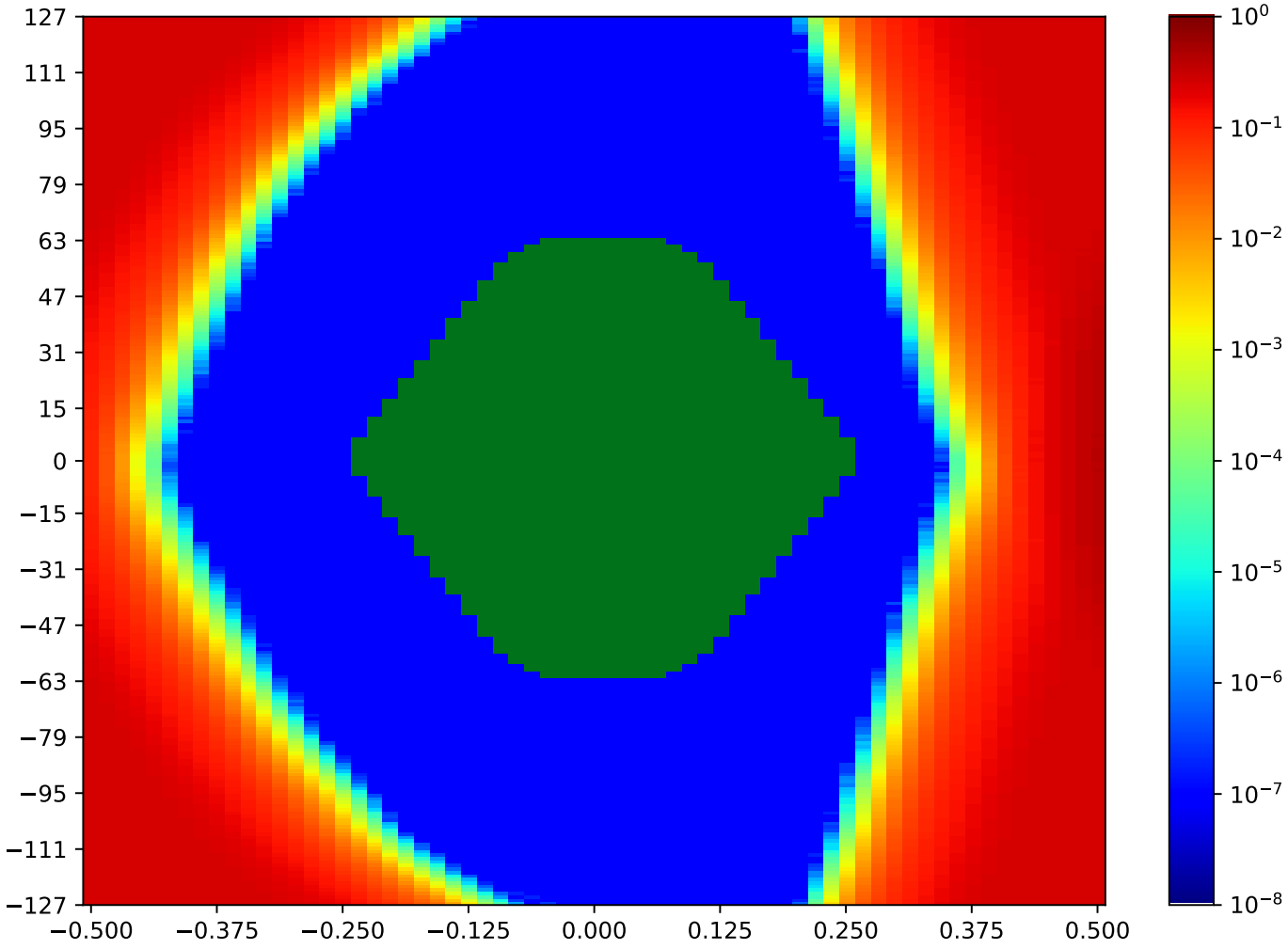


Figure 4.112: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.15 MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Table 4.104: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:25:14		2018-Sep-27 17:25:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8838	48	73.85%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

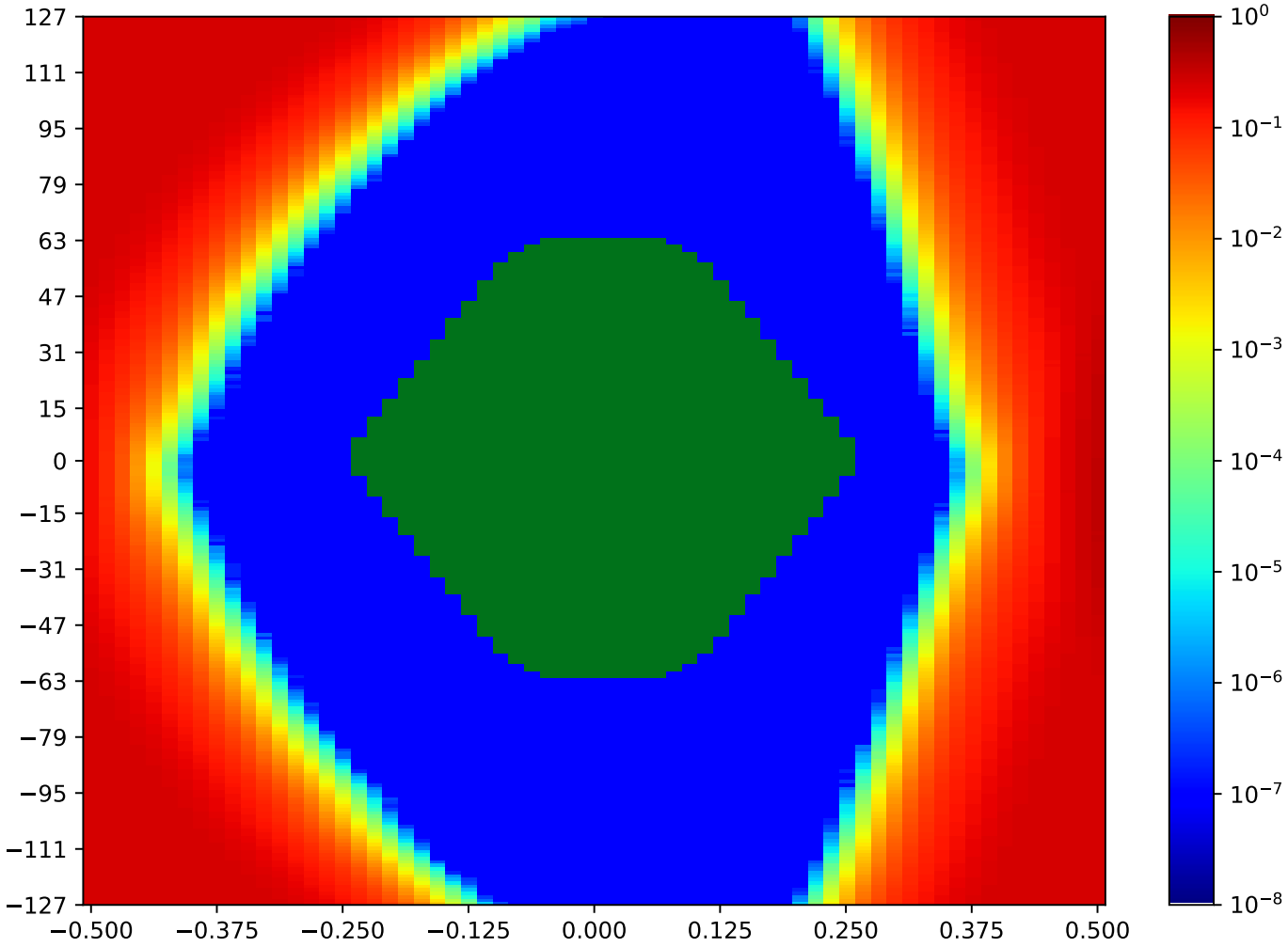


Figure 4.113: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.16 MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Table 4.105: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:25:34		2018-Sep-27 17:25:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9126	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

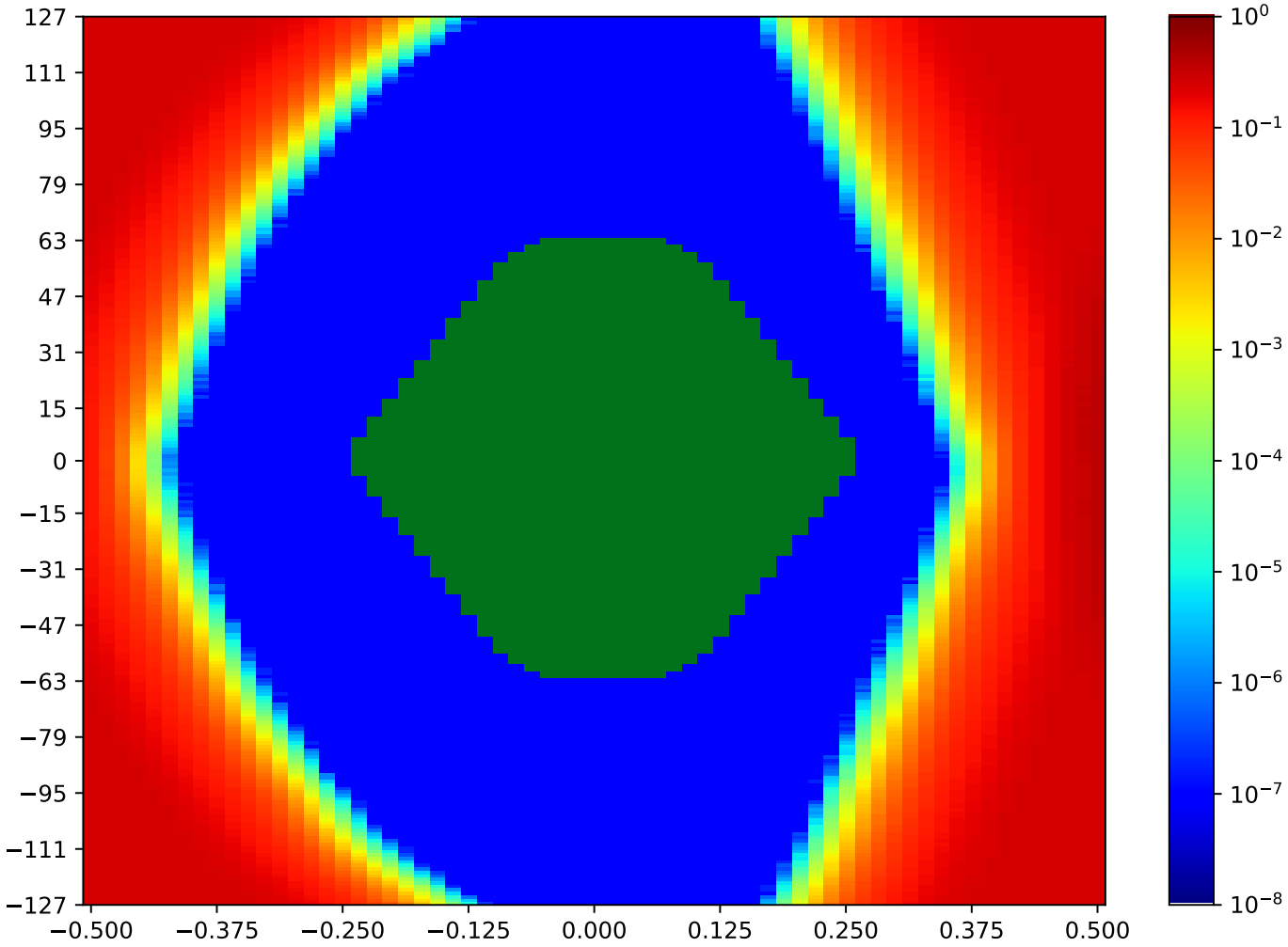


Figure 4.114: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.17 MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Table 4.106: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:25:54		2018-Sep-27 17:26:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8641	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

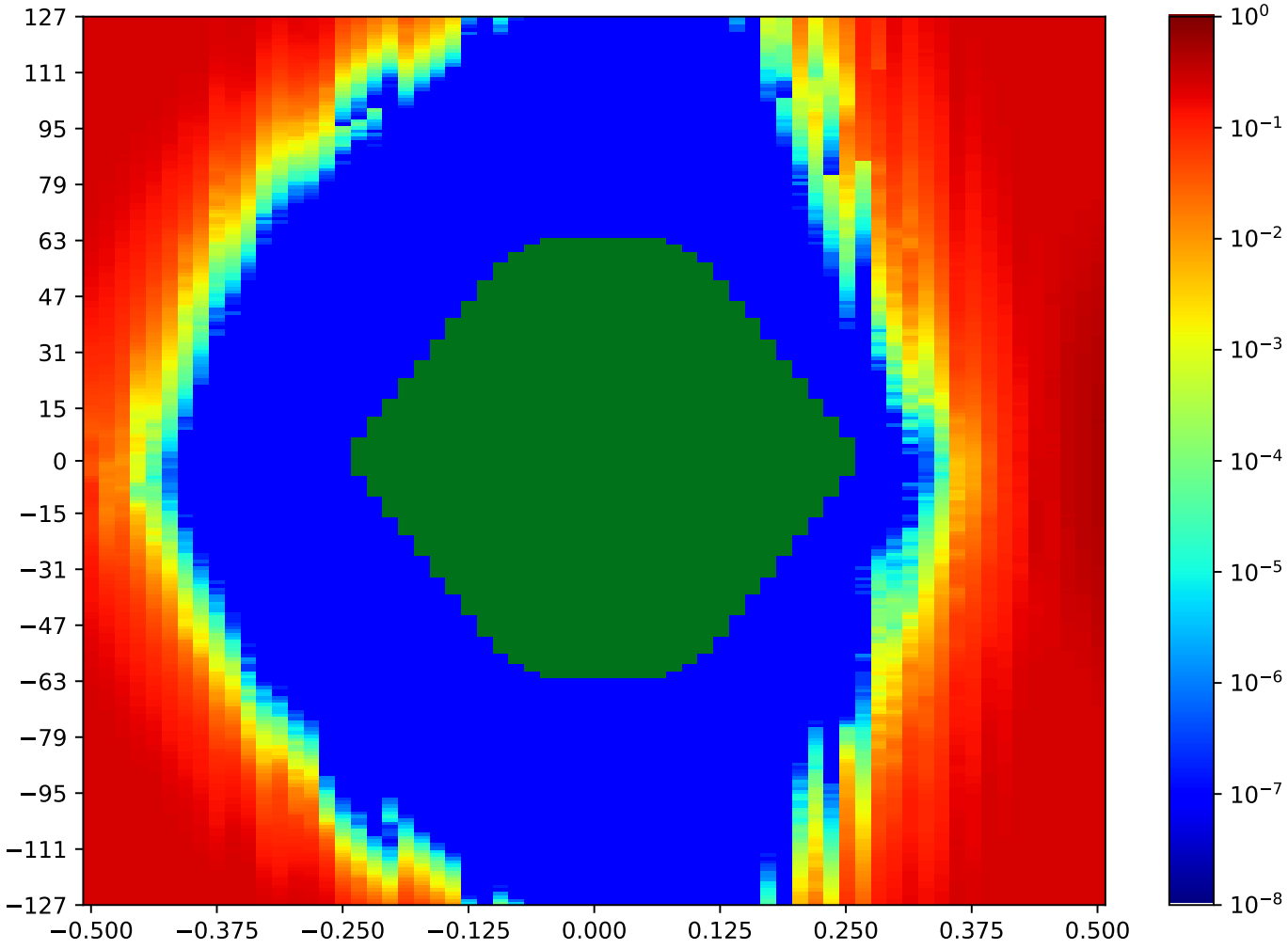


Figure 4.115: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.18 MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Table 4.107: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:26:15		2018-Sep-27 17:26:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8913	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

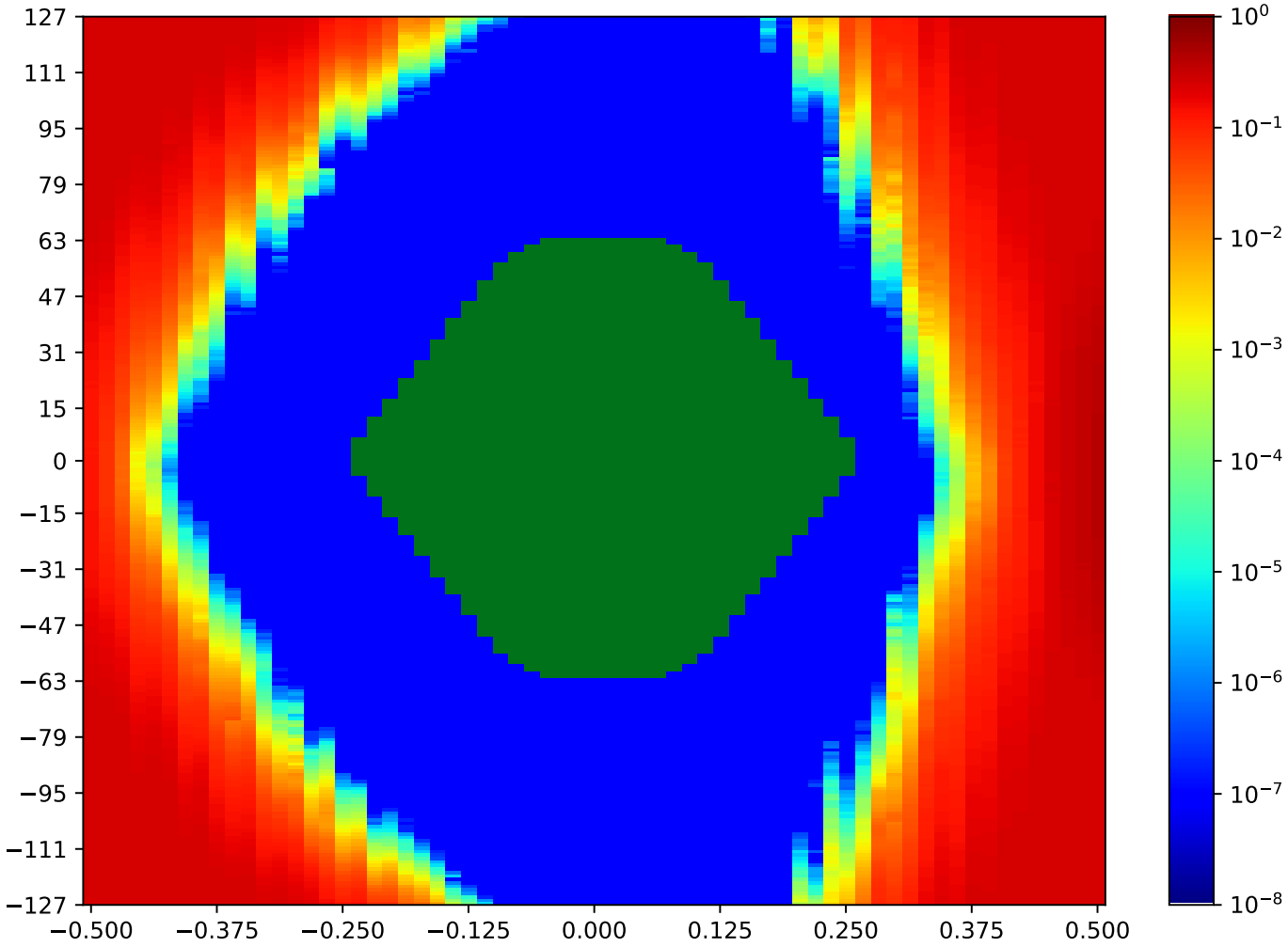


Figure 4.116: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.19 MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Table 4.108: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:26:35		2018-Sep-27 17:26:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9327	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

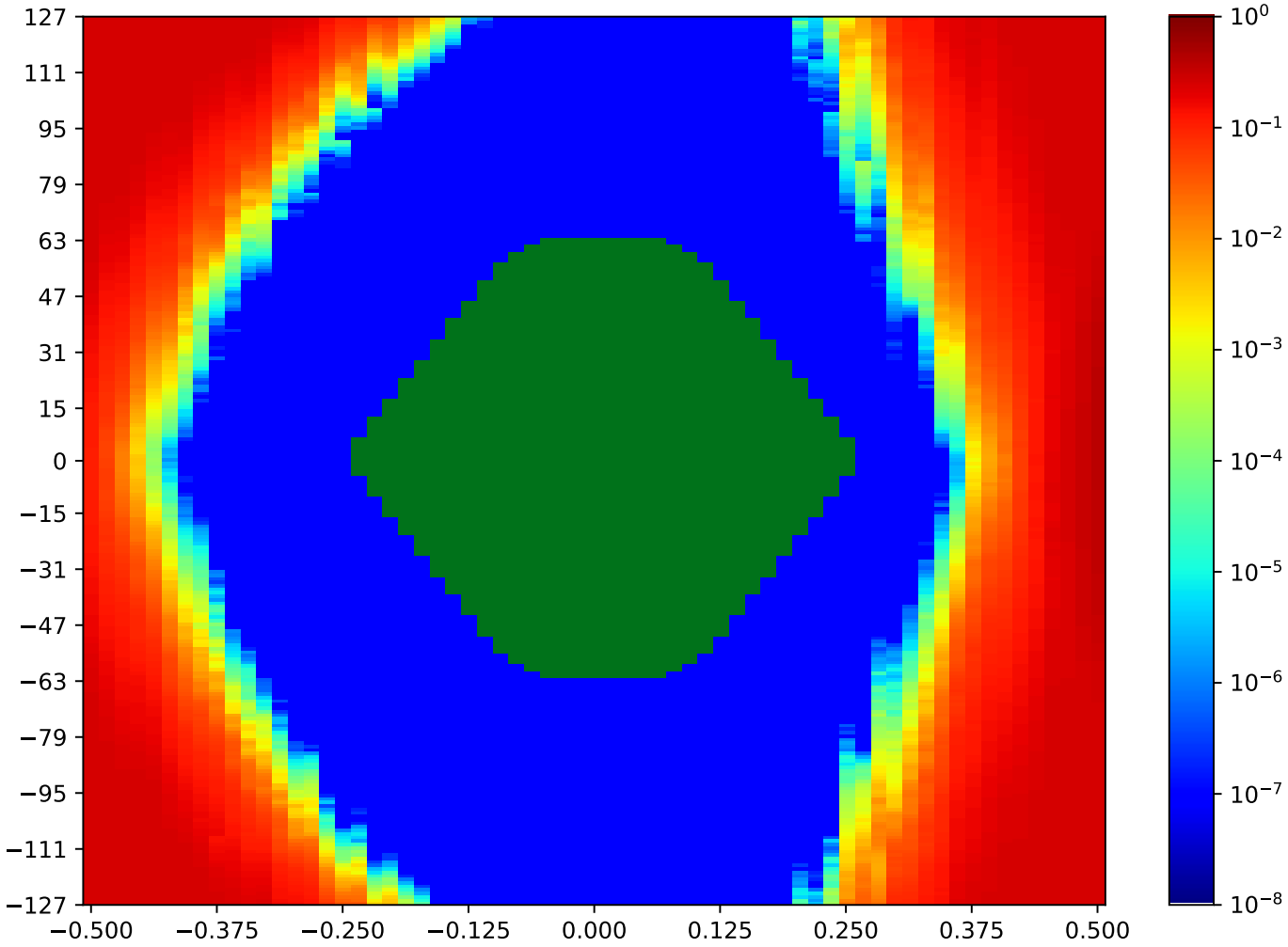


Figure 4.117: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.20 MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Table 4.109: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:26:55		2018-Sep-27 17:27:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8853	48	73.85%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

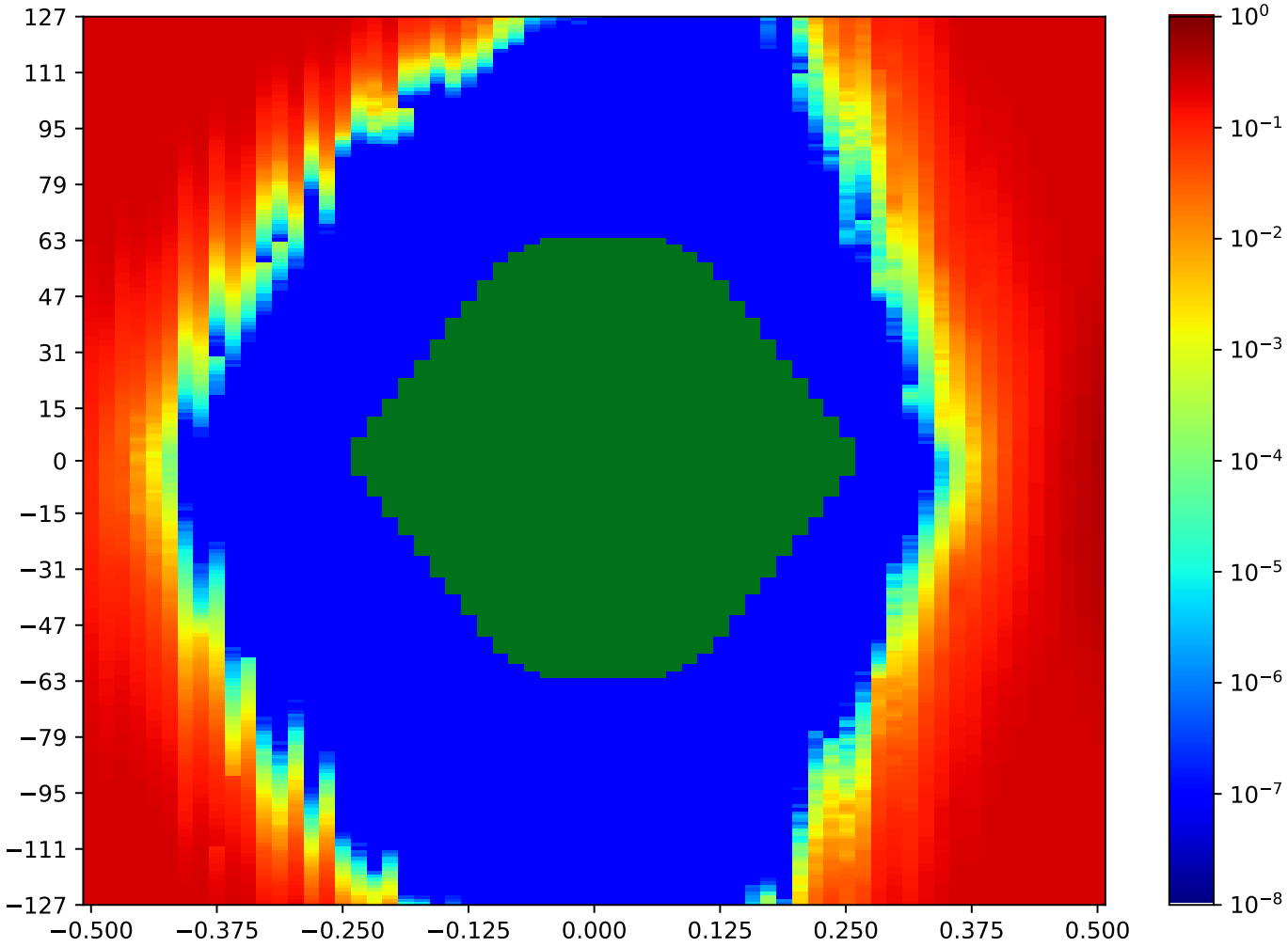


Figure 4.118: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.21 MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Table 4.110: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:27:16		2018-Sep-27 17:27:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9158	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

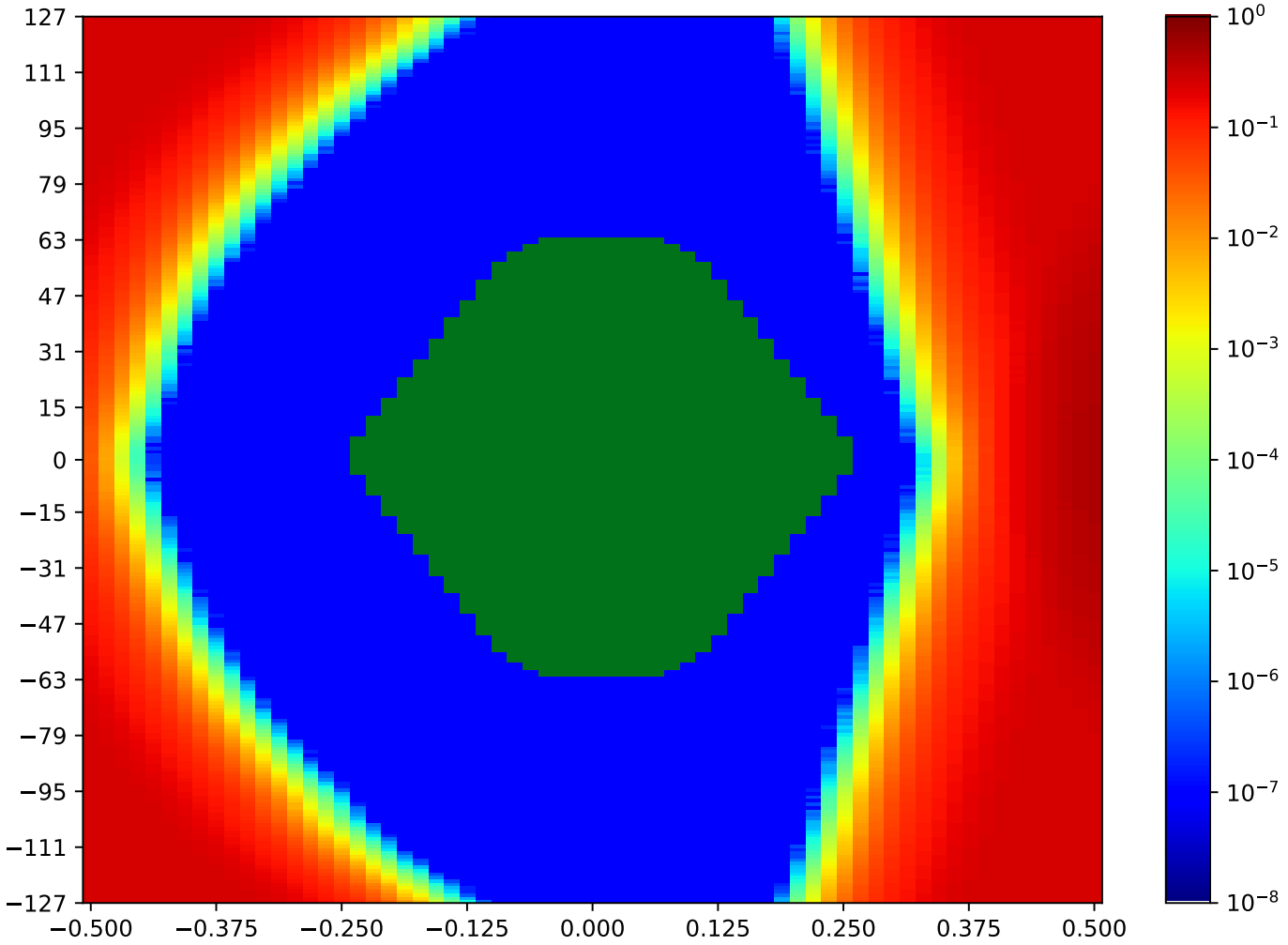


Figure 4.119: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.22 MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Table 4.111: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:27:36		2018-Sep-27 17:27:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9076	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

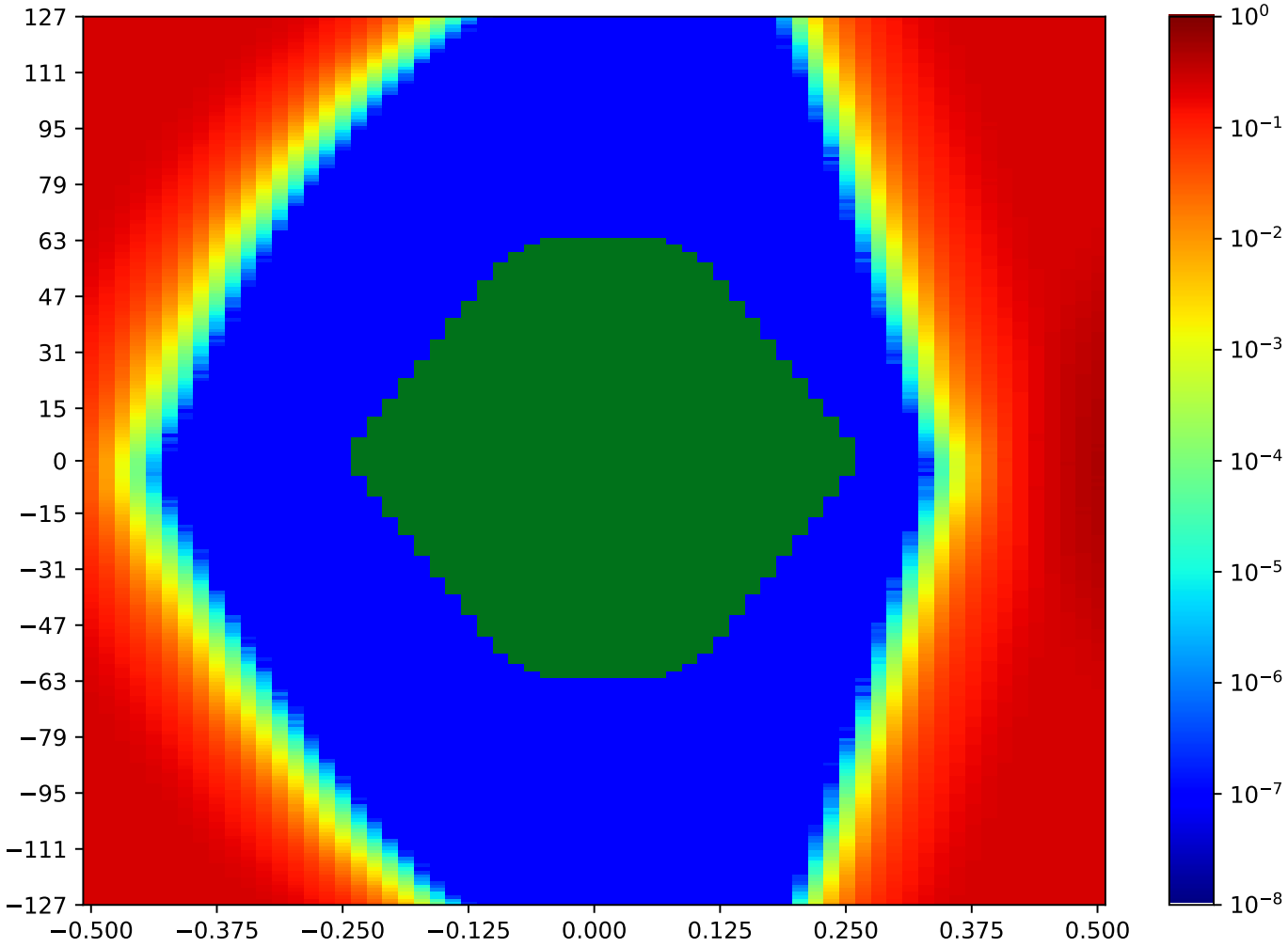


Figure 4.120: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.23 MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Table 4.112: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:27:57		2018-Sep-27 17:28:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8855	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

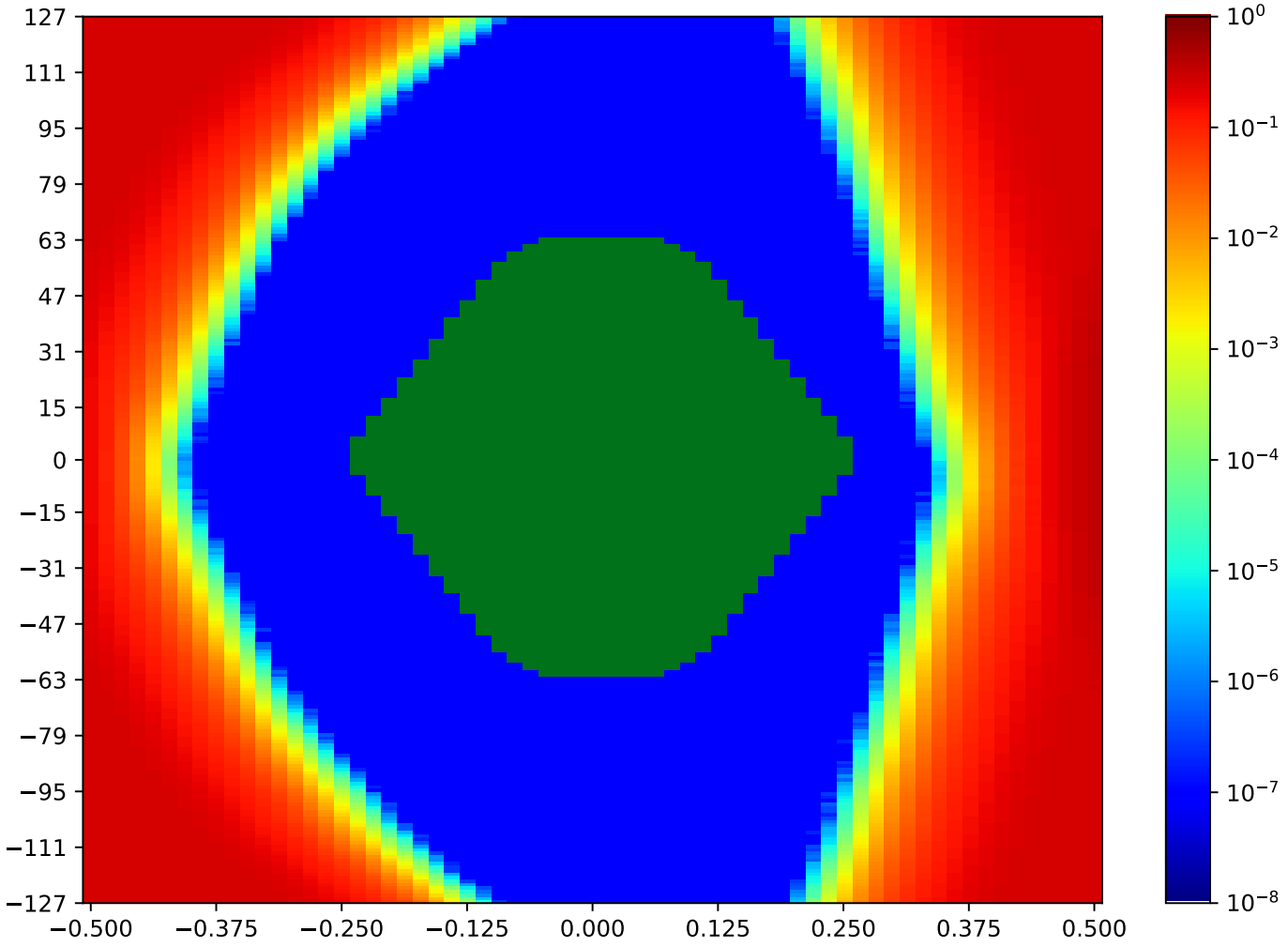


Figure 4.121: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.24 MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Table 4.113: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:28:17		2018-Sep-27 17:28:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8634	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

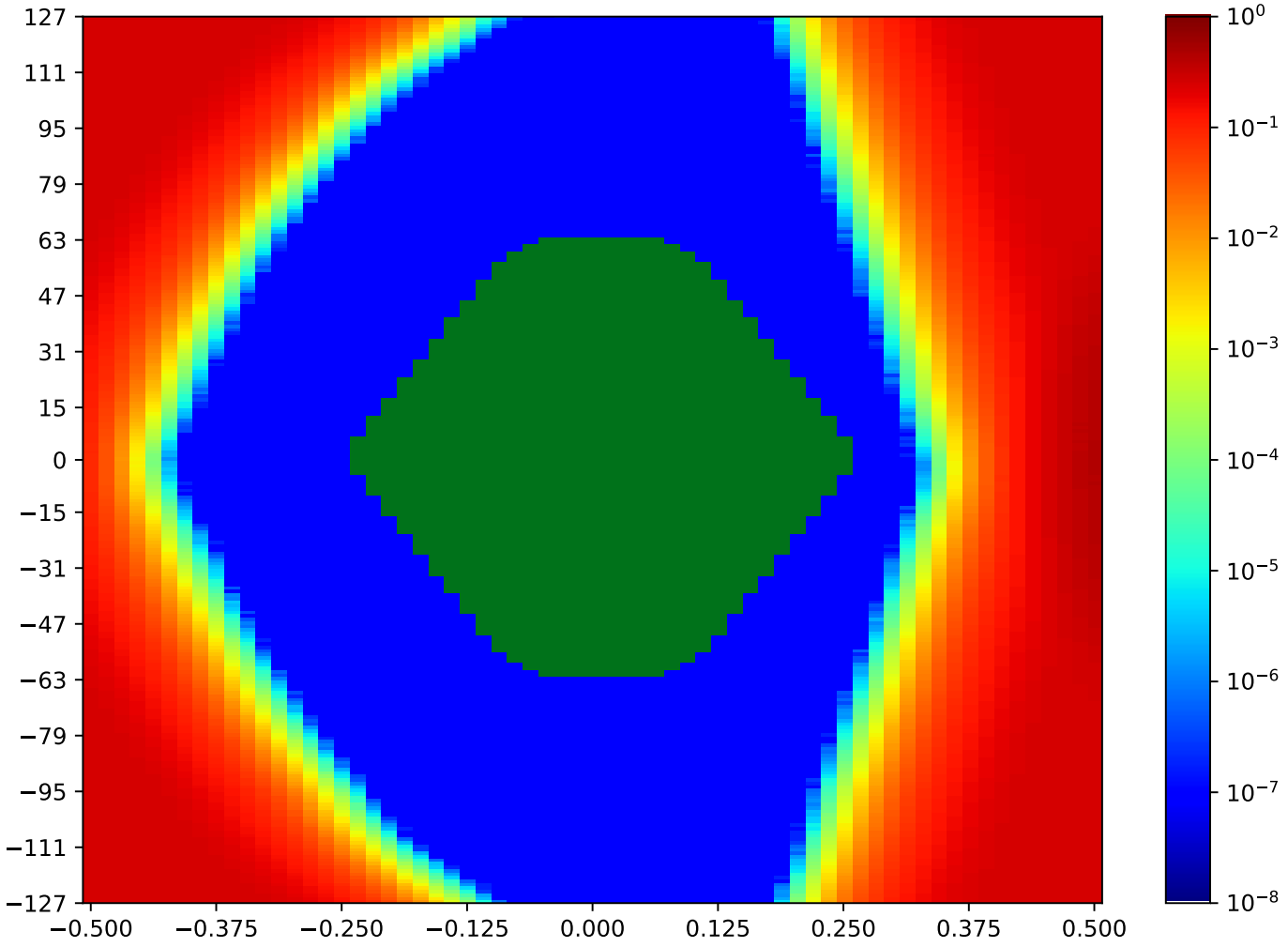


Figure 4.122: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.25 MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Table 4.114: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:28:37		2018-Sep-27 17:28:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8699	48	73.85%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

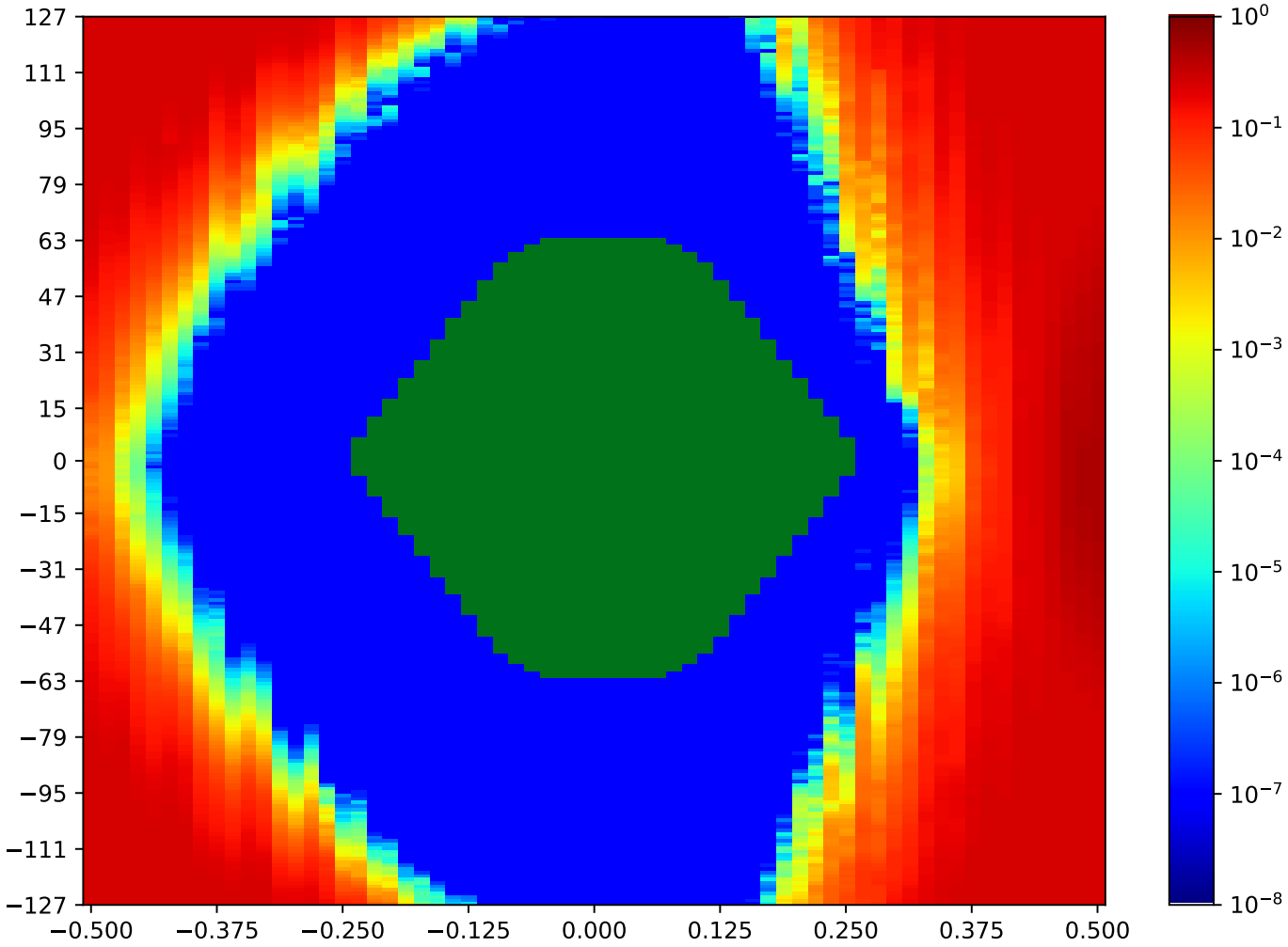


Figure 4.123: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.26 MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Table 4.115: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:28:58		2018-Sep-27 17:29:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8557	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

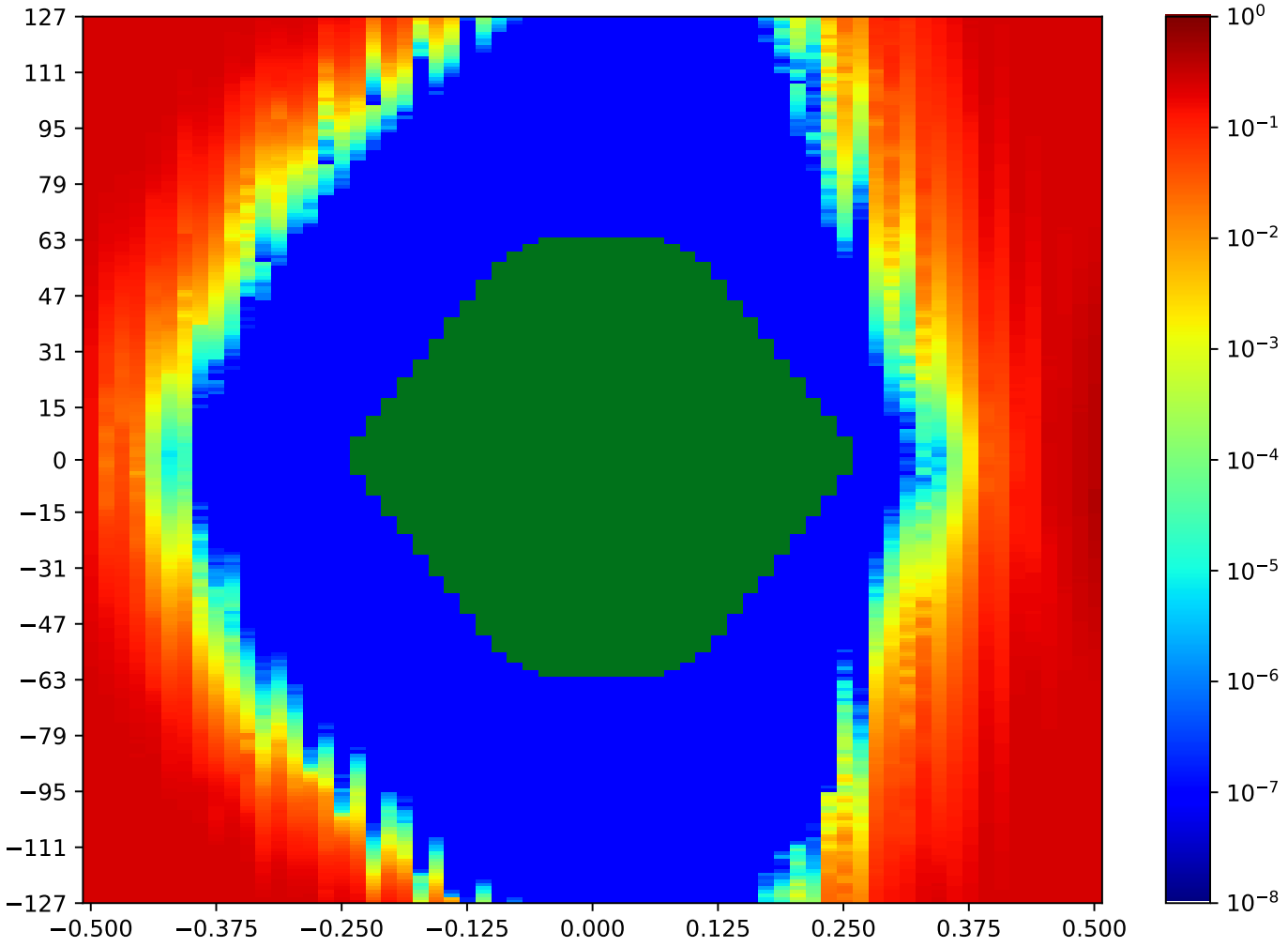


Figure 4.124: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.27 MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Table 4.116: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:29:18		2018-Sep-27 17:29:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8924	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

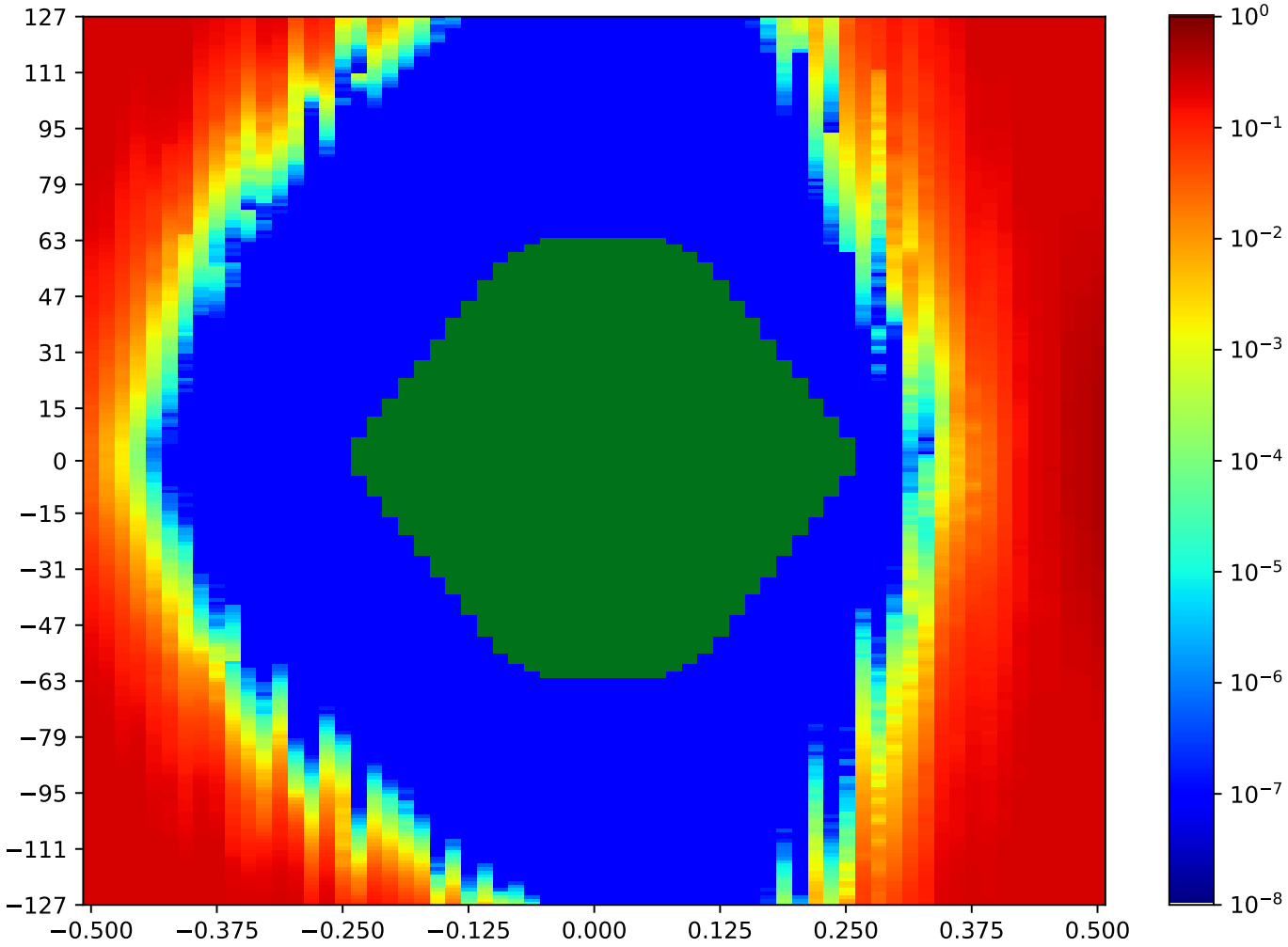


Figure 4.125: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.9.28 MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Table 4.117: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:29:38		2018-Sep-27 17:29:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8770	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

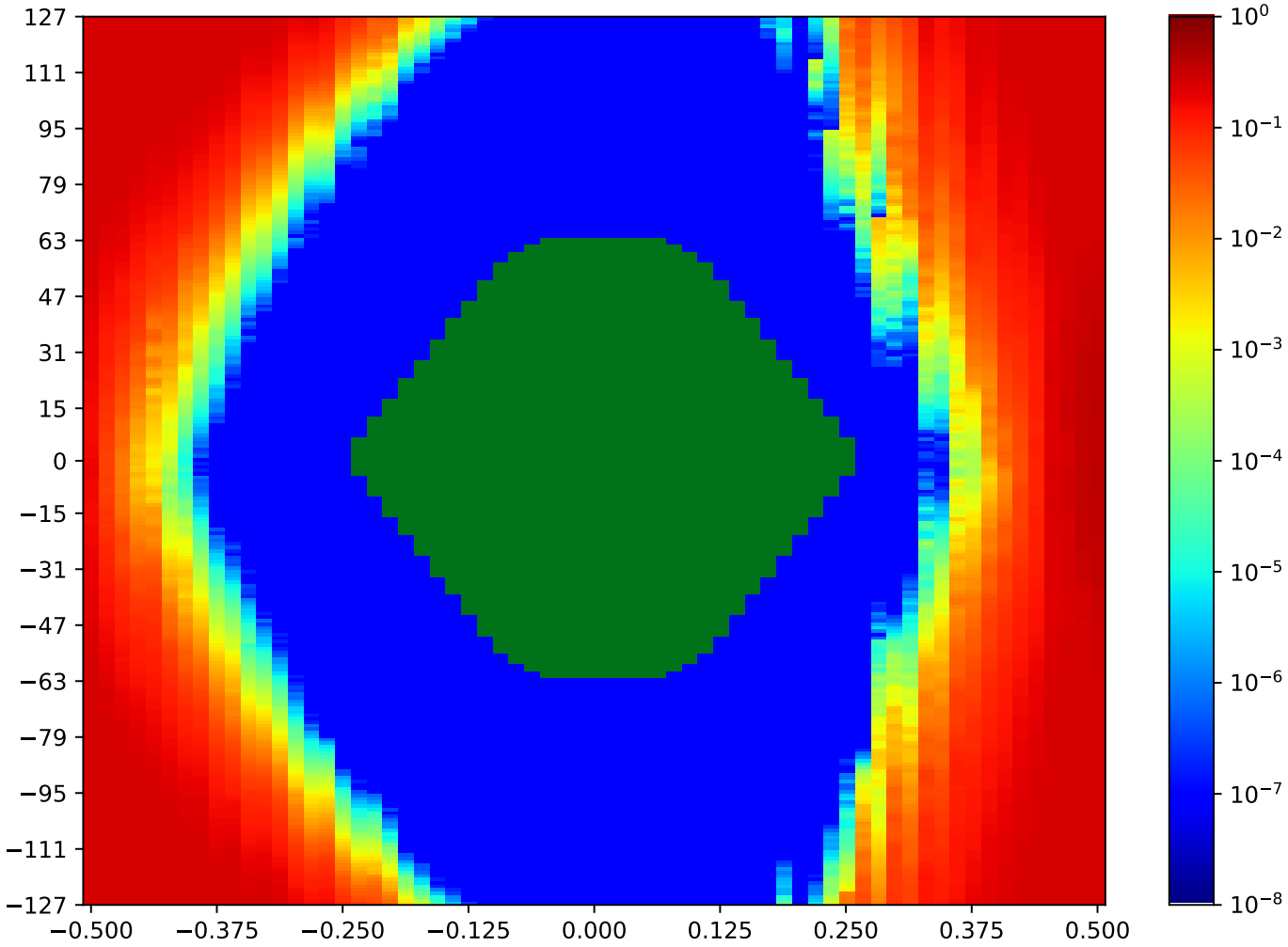


Figure 4.126: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10 MSP_A TX1 MSP_C RX17 Minipod Loopback

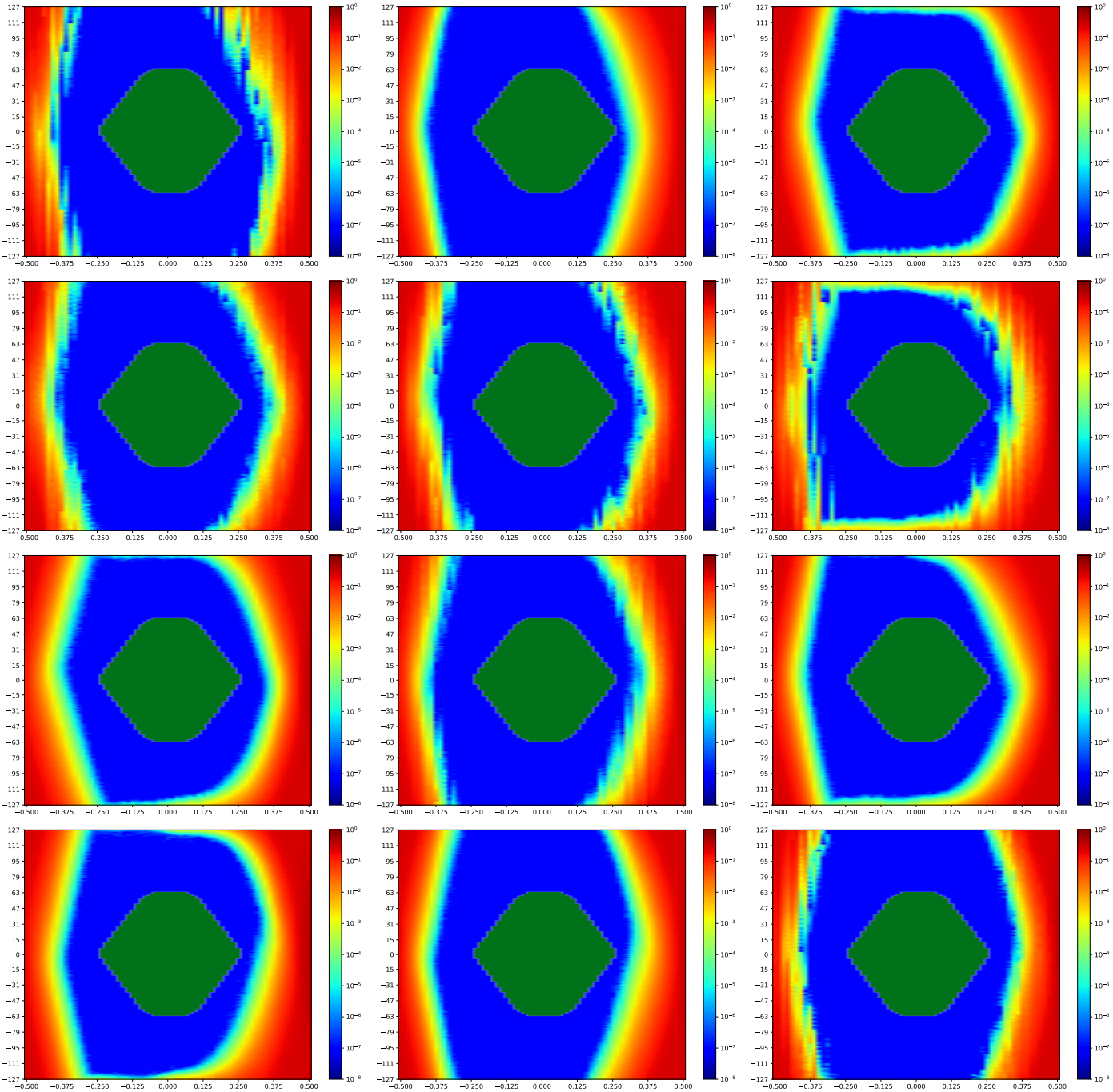


Figure 4.127: MSP_A TX1 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.140.

4.10.1 MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Table 4.118: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:12:42		2018-Sep-27 16:13:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9954	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

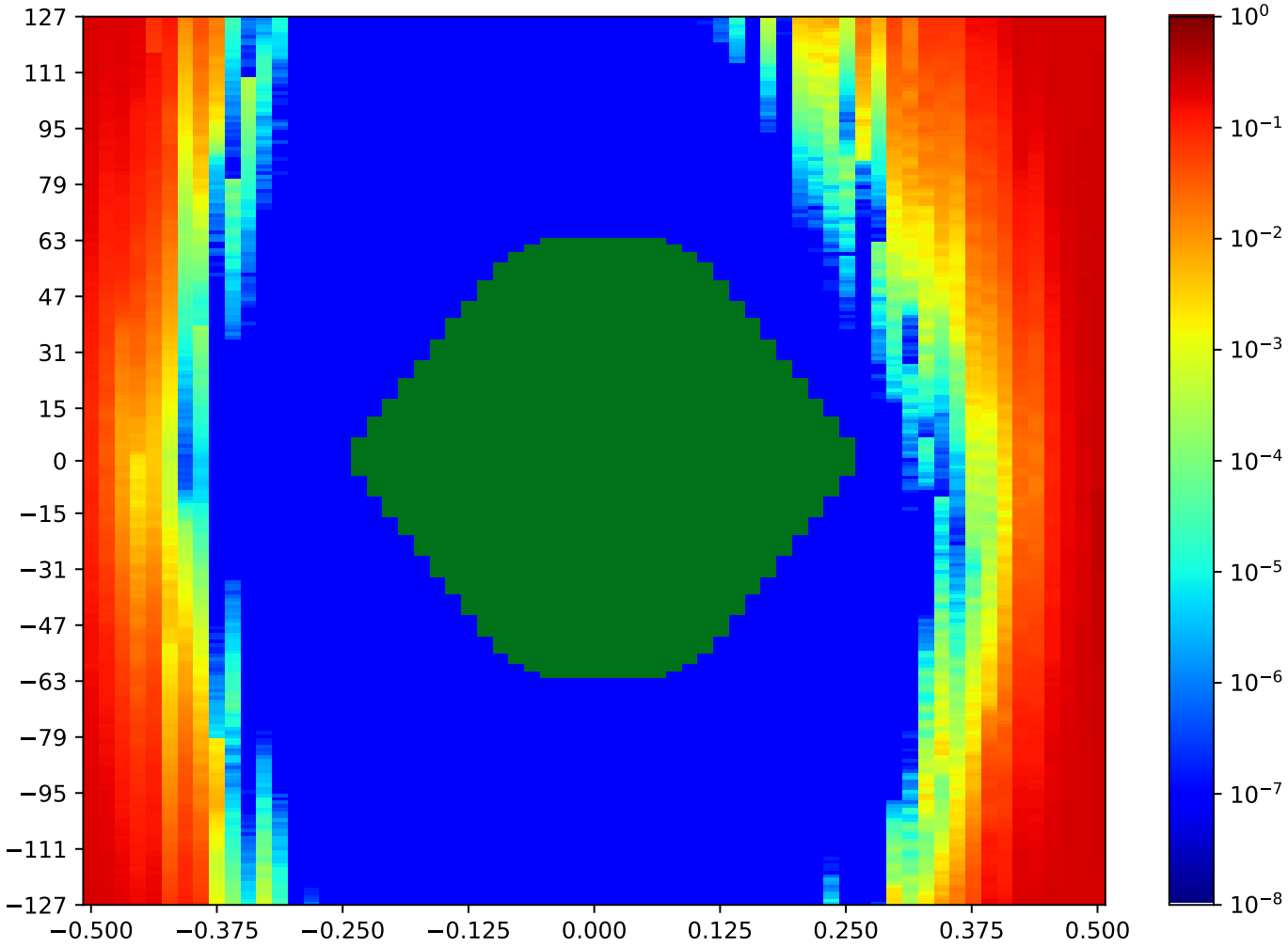


Figure 4.128: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.2 MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Table 4.119: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:13:23		2018-Sep-27 16:13:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9345	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

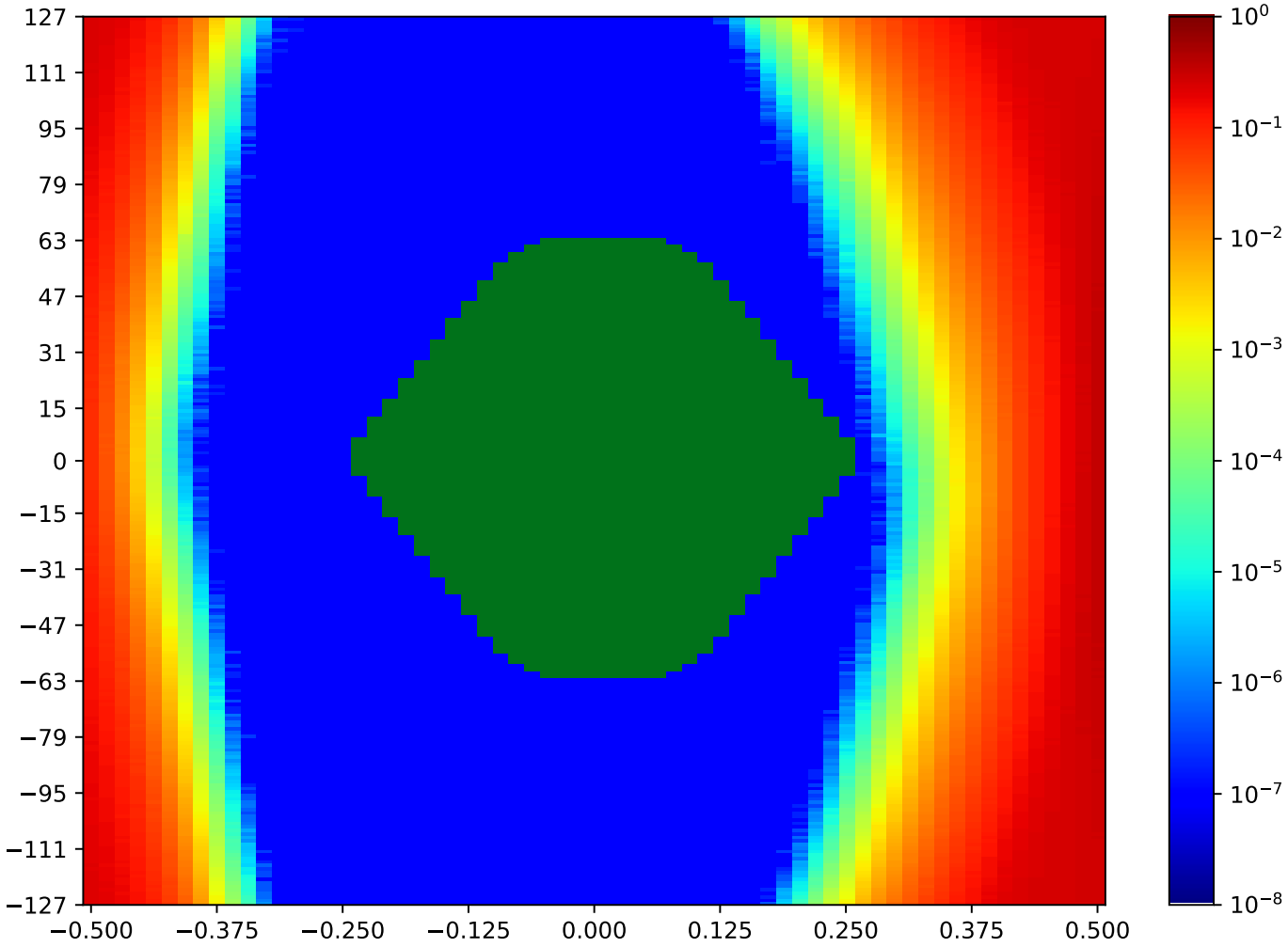


Figure 4.129: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.3 MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Table 4.120: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:13:44		2018-Sep-27 16:14:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8325	43	66.15%	236	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

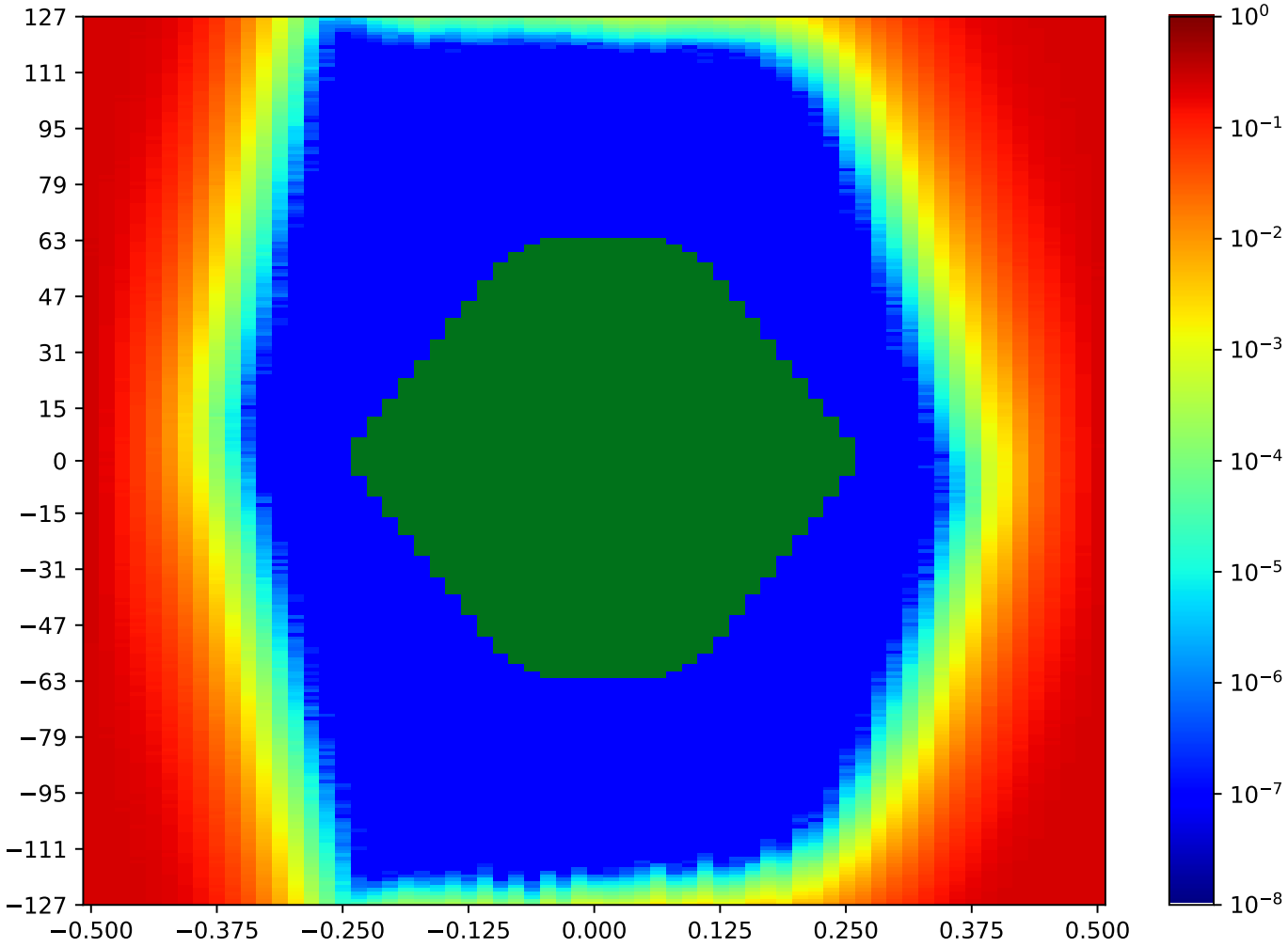


Figure 4.130: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.4 MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Table 4.121: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:12:02		2018-Sep-27 16:12:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9204	45	69.23%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

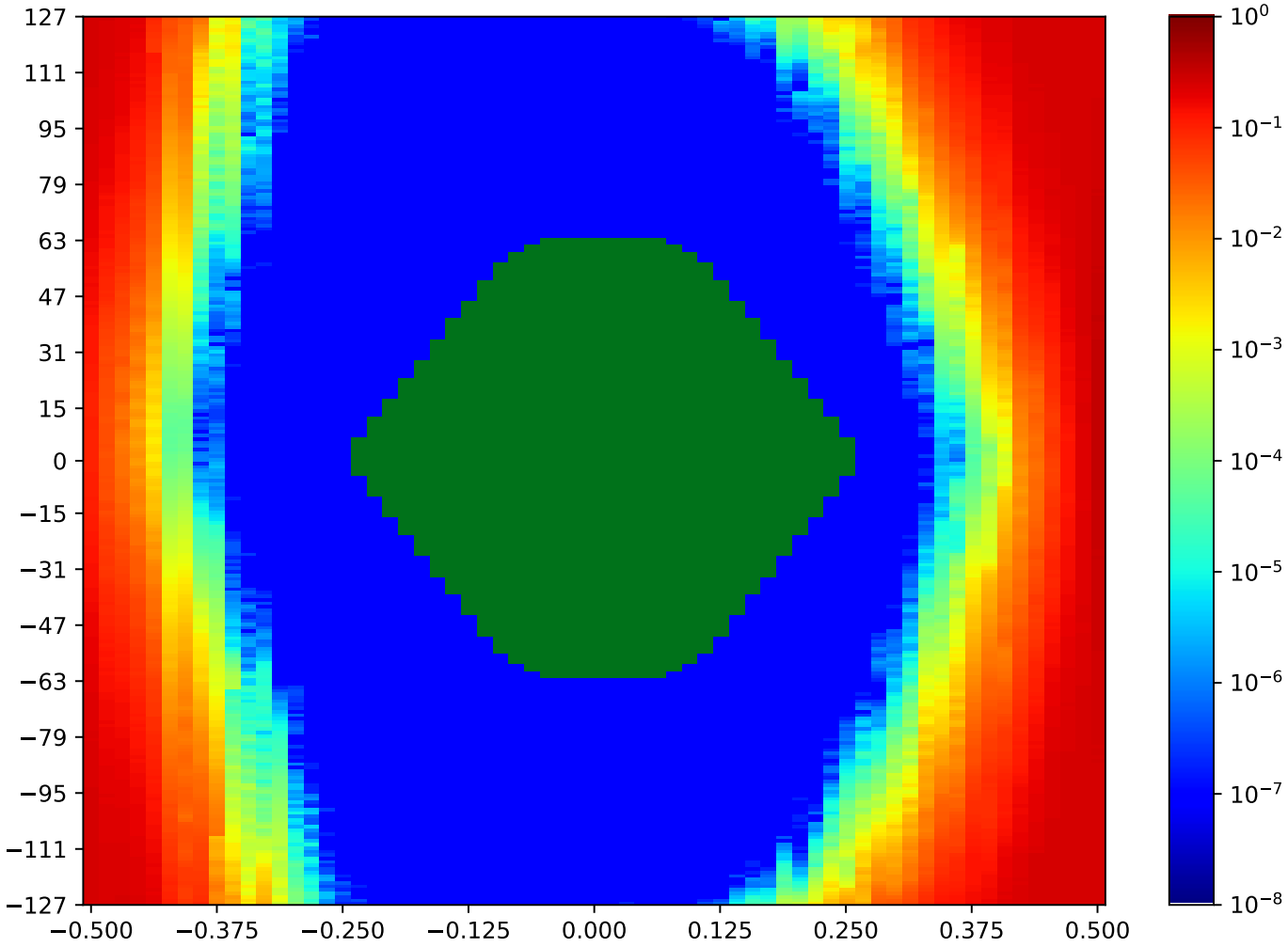


Figure 4.131: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.5 MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Table 4.122: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:14:45		2018-Sep-27 16:15:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9245	44	67.69%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

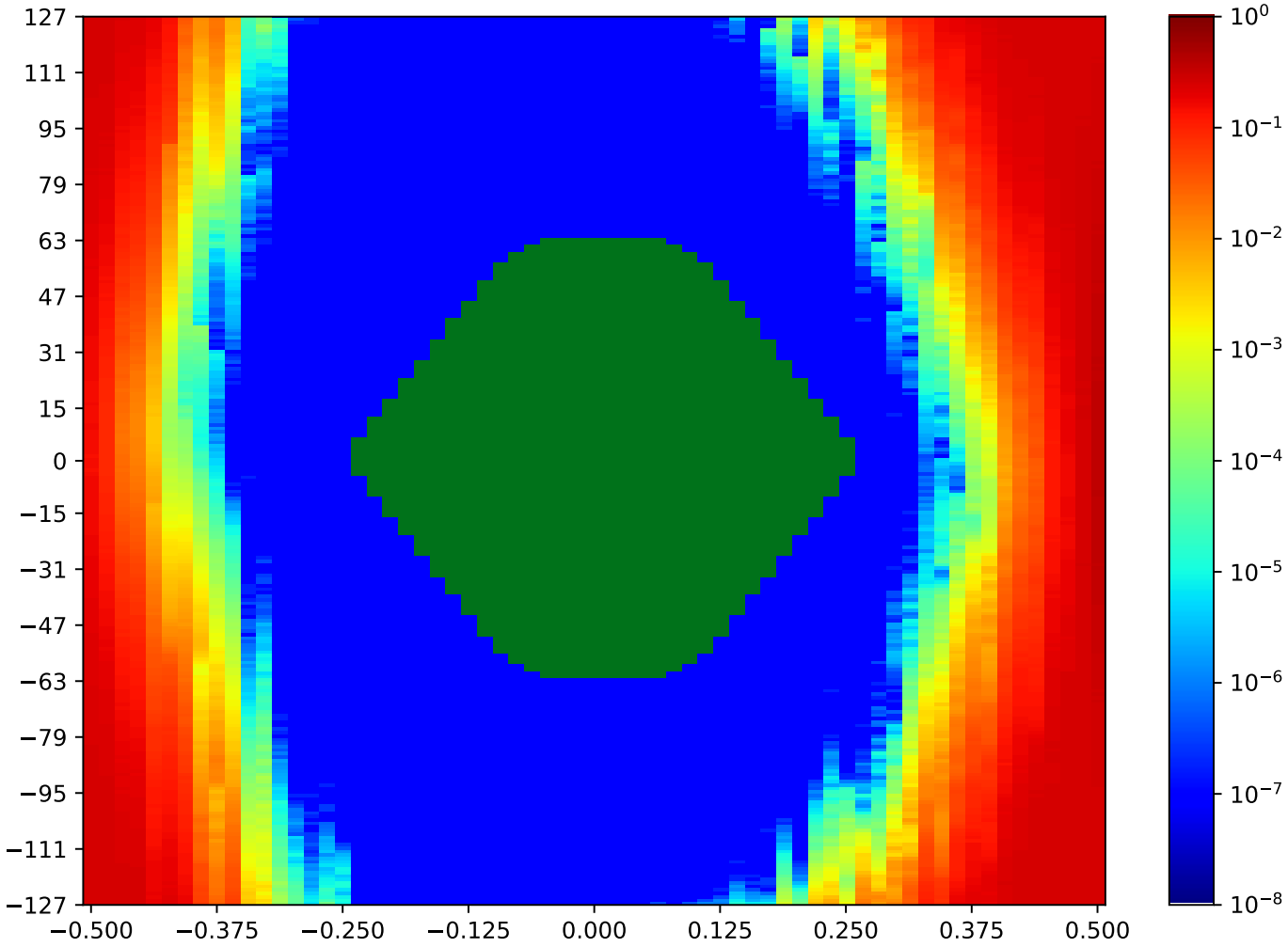


Figure 4.132: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.6 MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Table 4.123: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:11:42		2018-Sep-27 16:12:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7778	42	63.08%	221	86.67%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

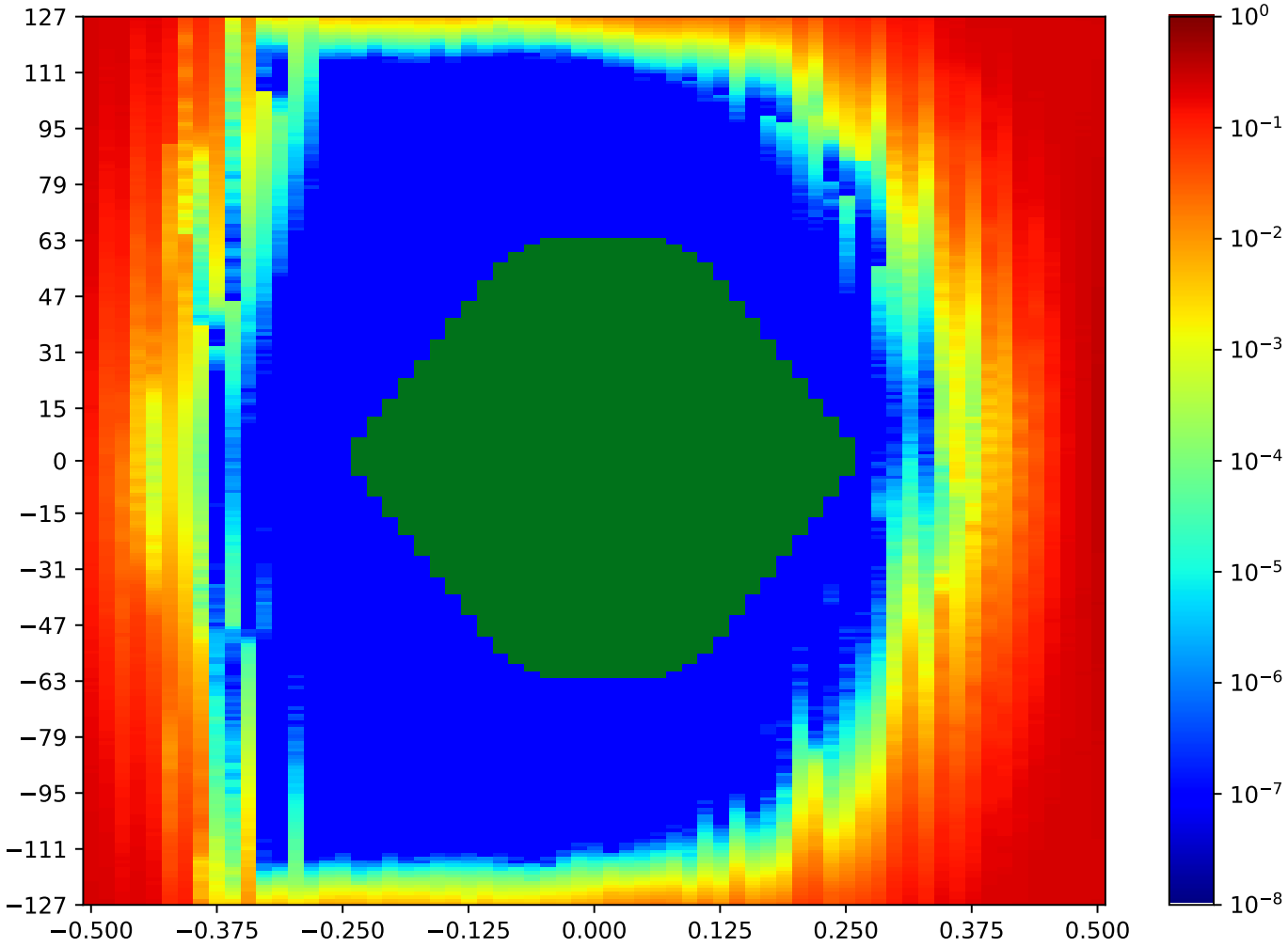


Figure 4.133: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.7 MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Table 4.124: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:15:26		2018-Sep-27 16:15:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8250	43	66.15%	239	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

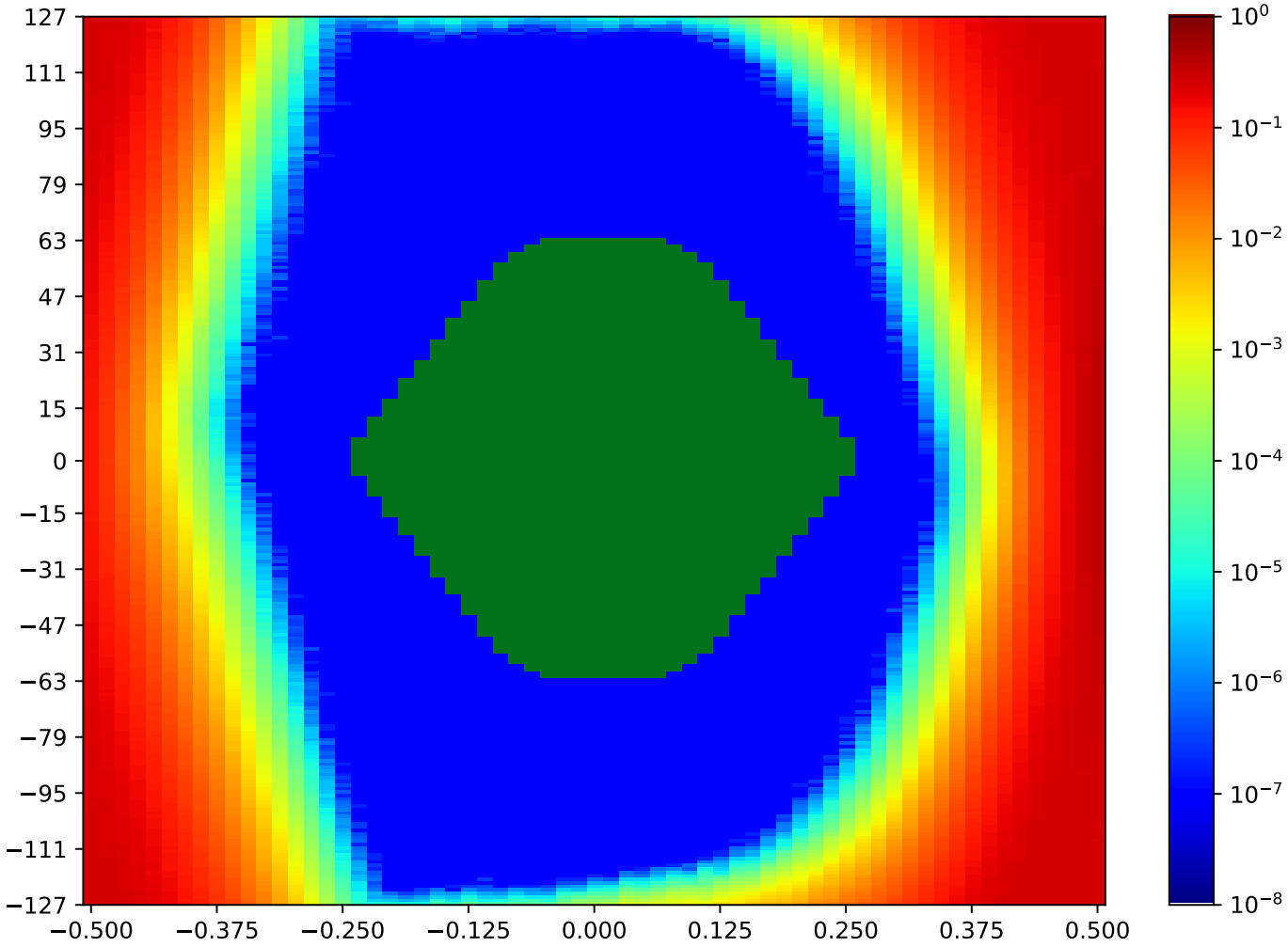


Figure 4.134: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.8 MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Table 4.125: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:12:22		2018-Sep-27 16:12:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9363	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

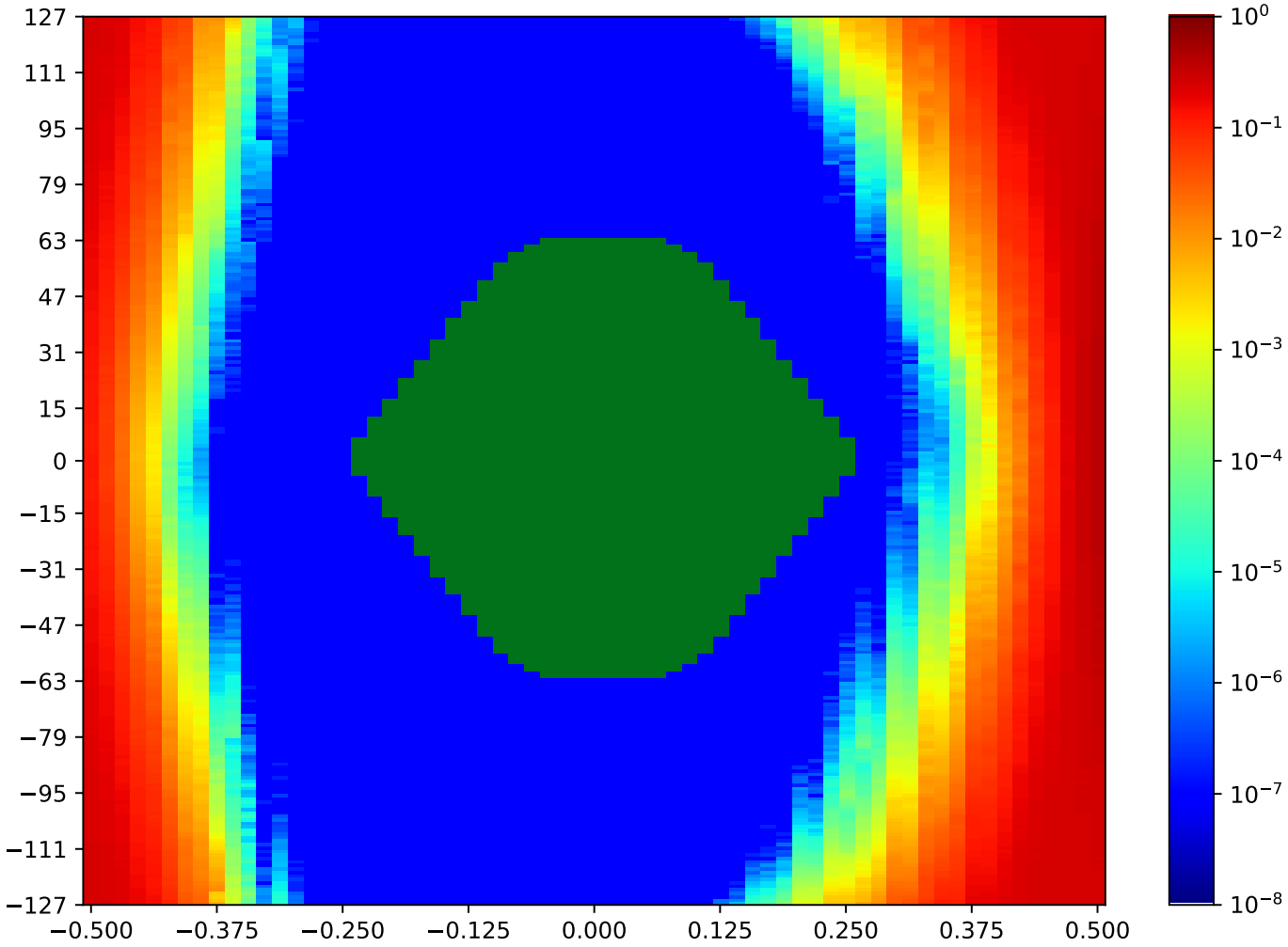


Figure 4.135: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.9 MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Table 4.126: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:15:05		2018-Sep-27 16:15:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8329	42	64.62%	237	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

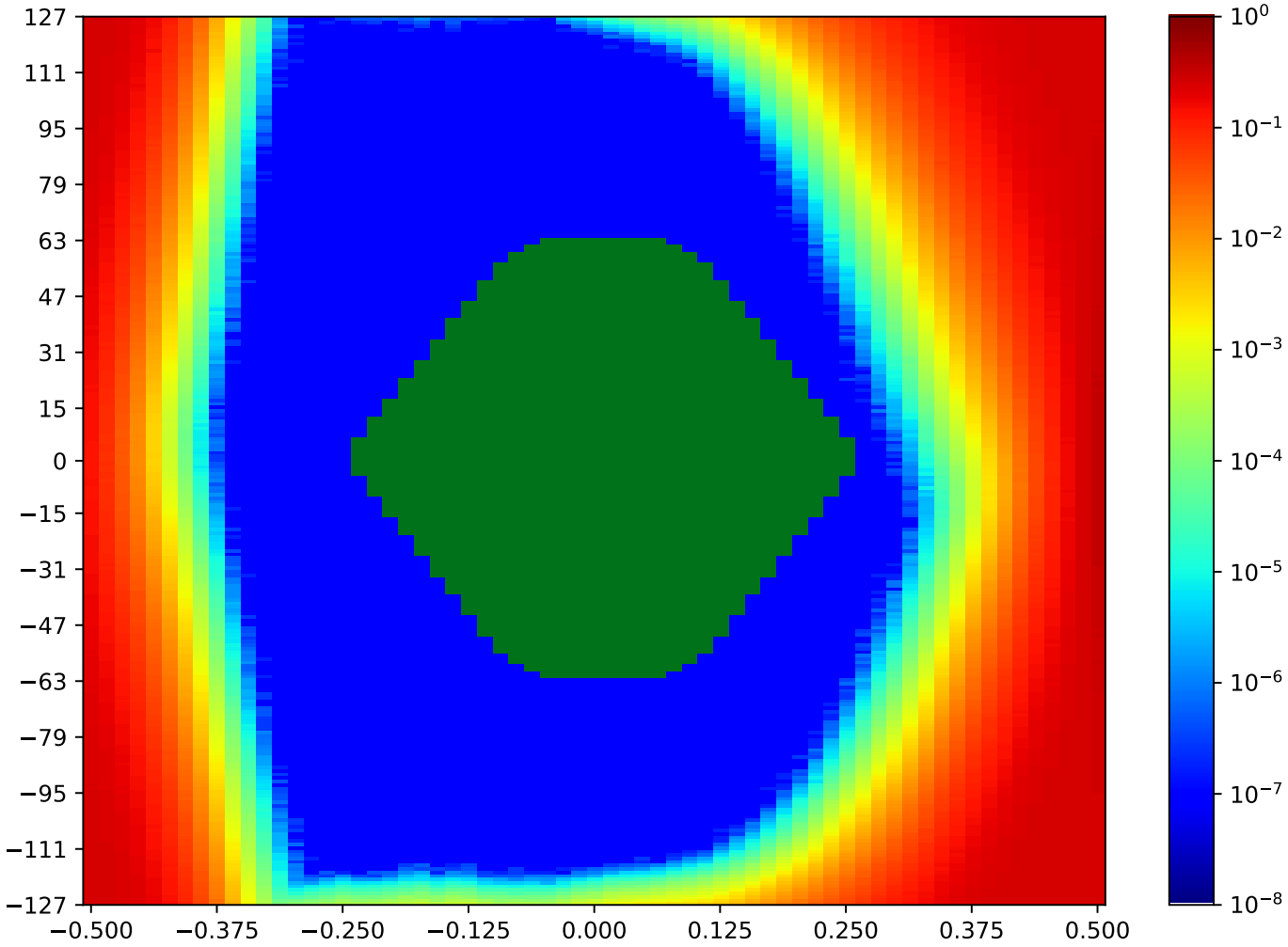


Figure 4.136: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.10 MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Table 4.127: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:13:03		2018-Sep-27 16:13:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8261	41	63.08%	234	90.98%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

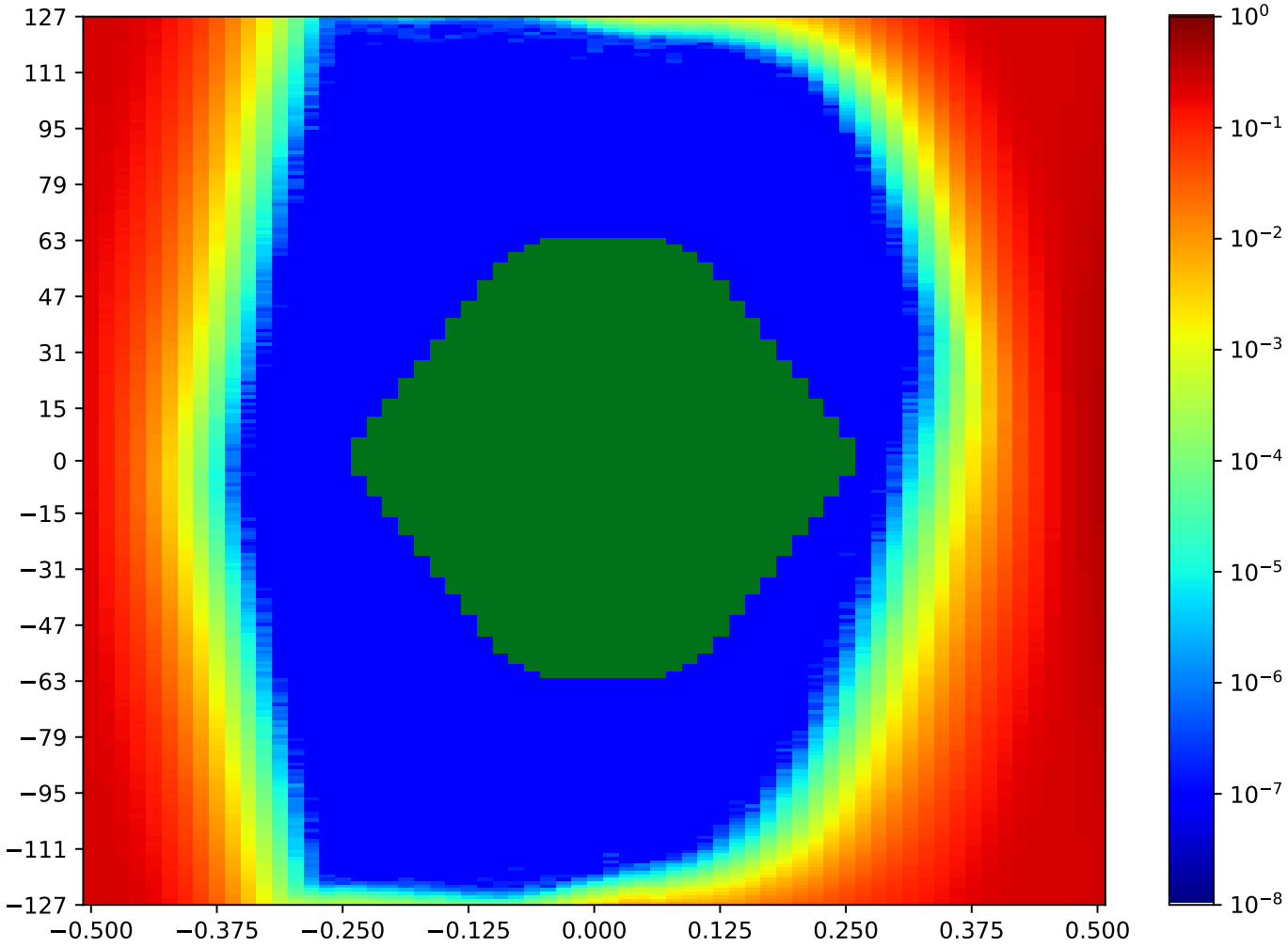


Figure 4.137: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.11 MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Table 4.128: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:14:24		2018-Sep-27 16:14:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9219	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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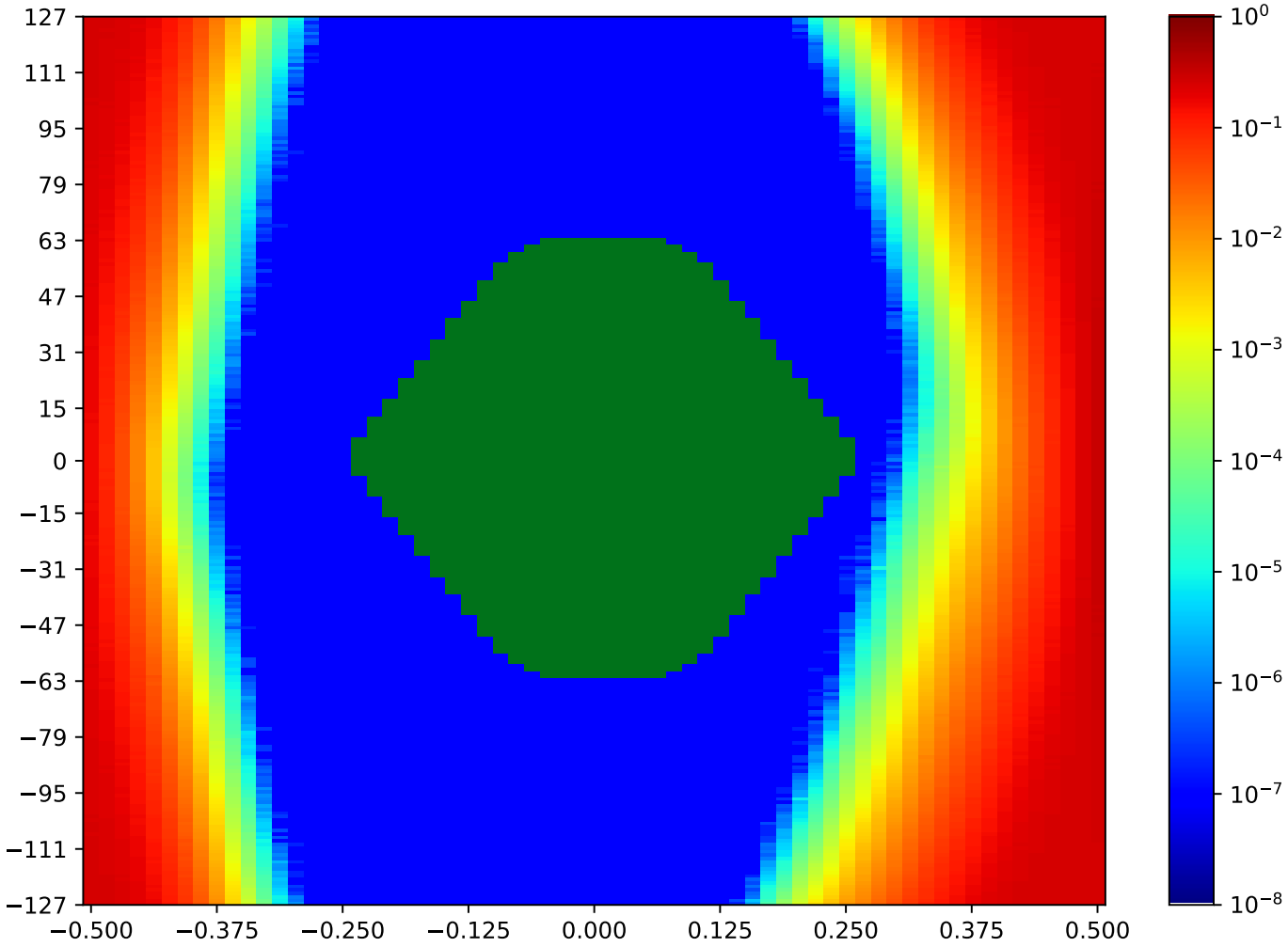


Figure 4.138: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.10.12 MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Table 4.129: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:14:04		2018-Sep-27 16:14:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10245	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

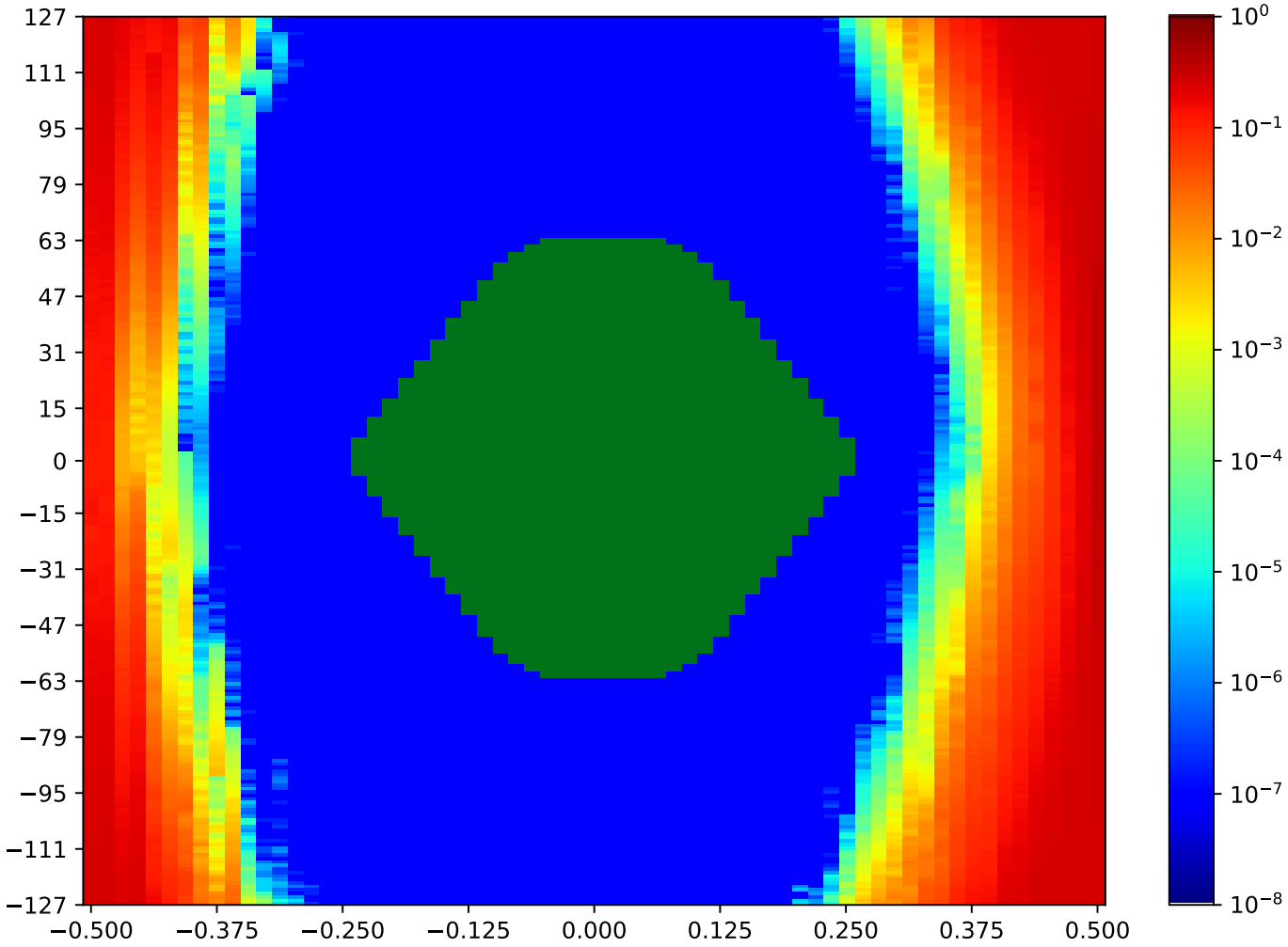


Figure 4.139: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11 MSP_A TX2 MSP_C RX18 Minipod Loopback

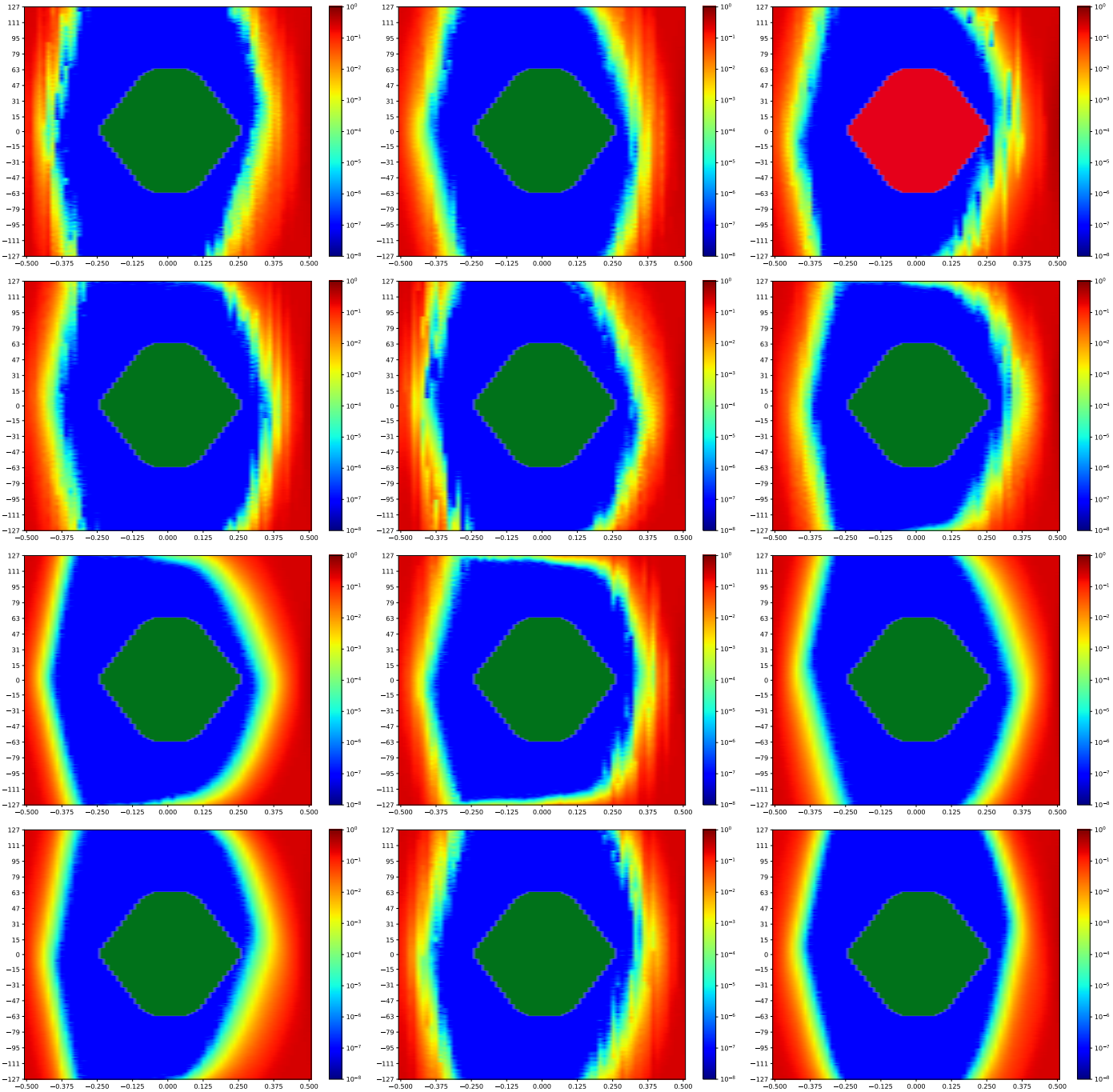


Figure 4.140: MSP_A TX2 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.153.

4.11.1 MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Table 4.130: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:16:55		2018-Sep-27 16:17:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9366	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

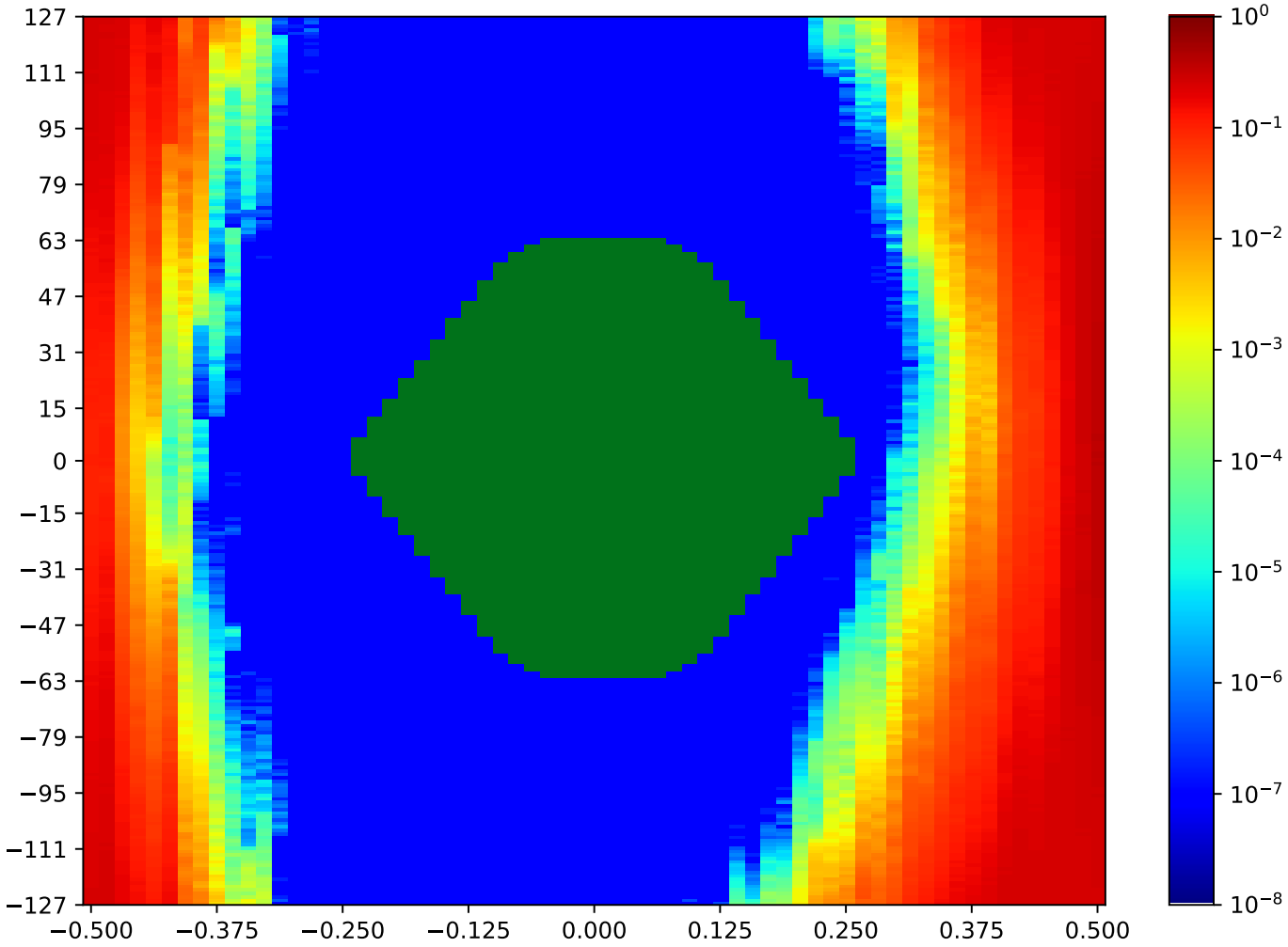


Figure 4.141: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.2 MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Table 4.131: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:16:14		2018-Sep-27 16:16:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9040	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

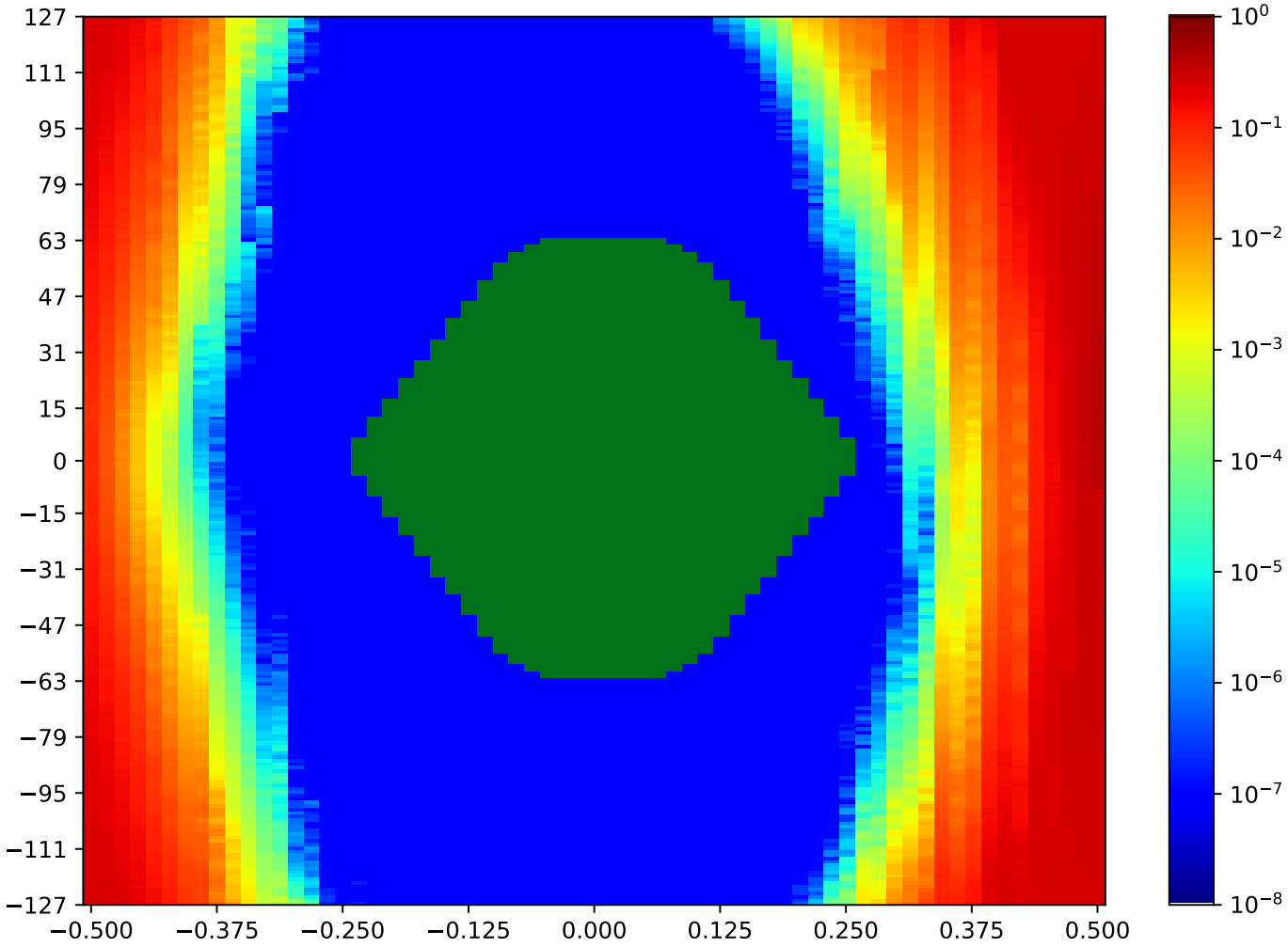


Figure 4.142: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.3 MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Table 4.132: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:17:57		2018-Sep-27 16:18:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8723	41	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

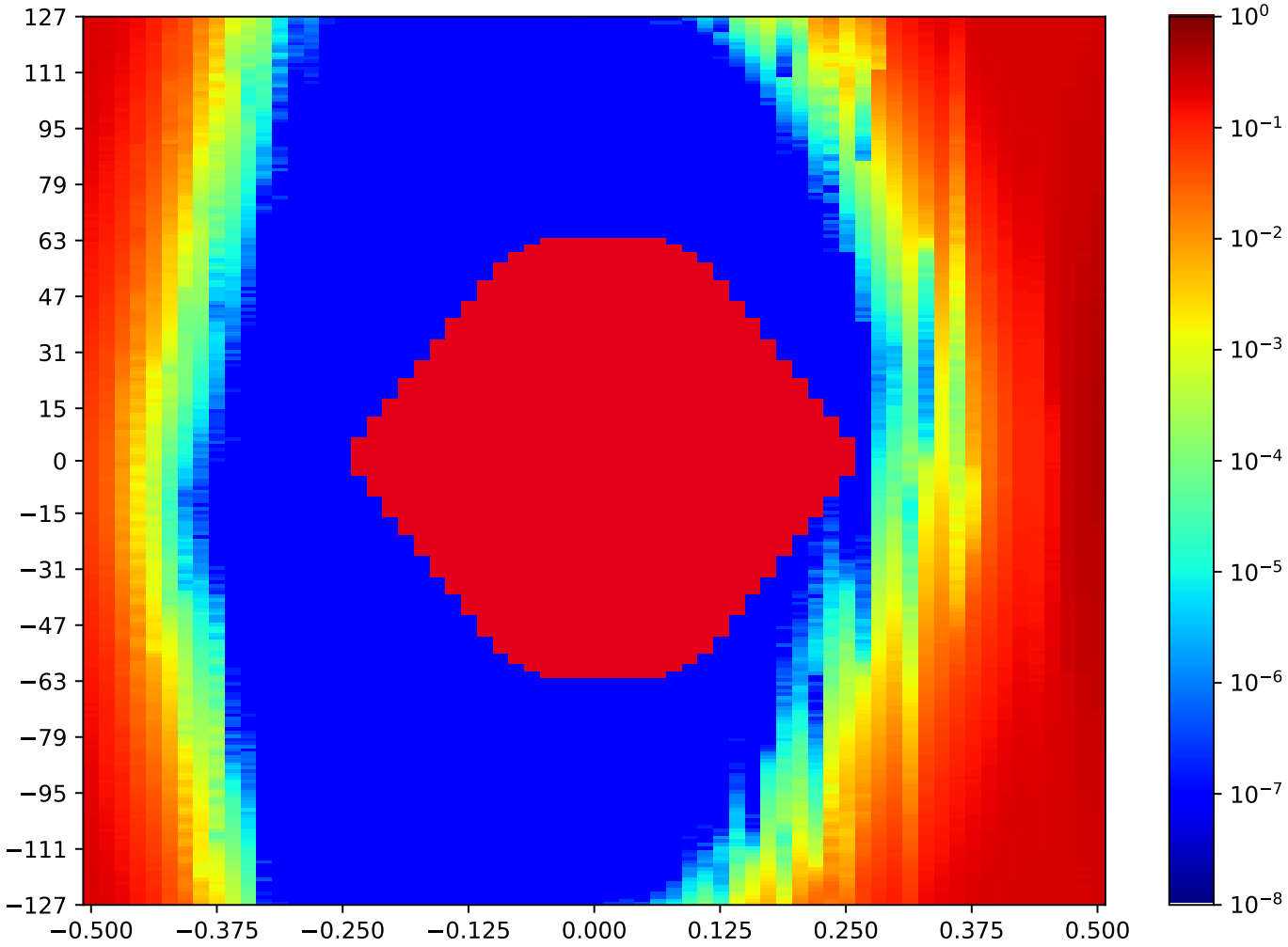


Figure 4.143: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.4 MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Table 4.133: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:15:53		2018-Sep-27 16:16:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9314	43	66.15%	252	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

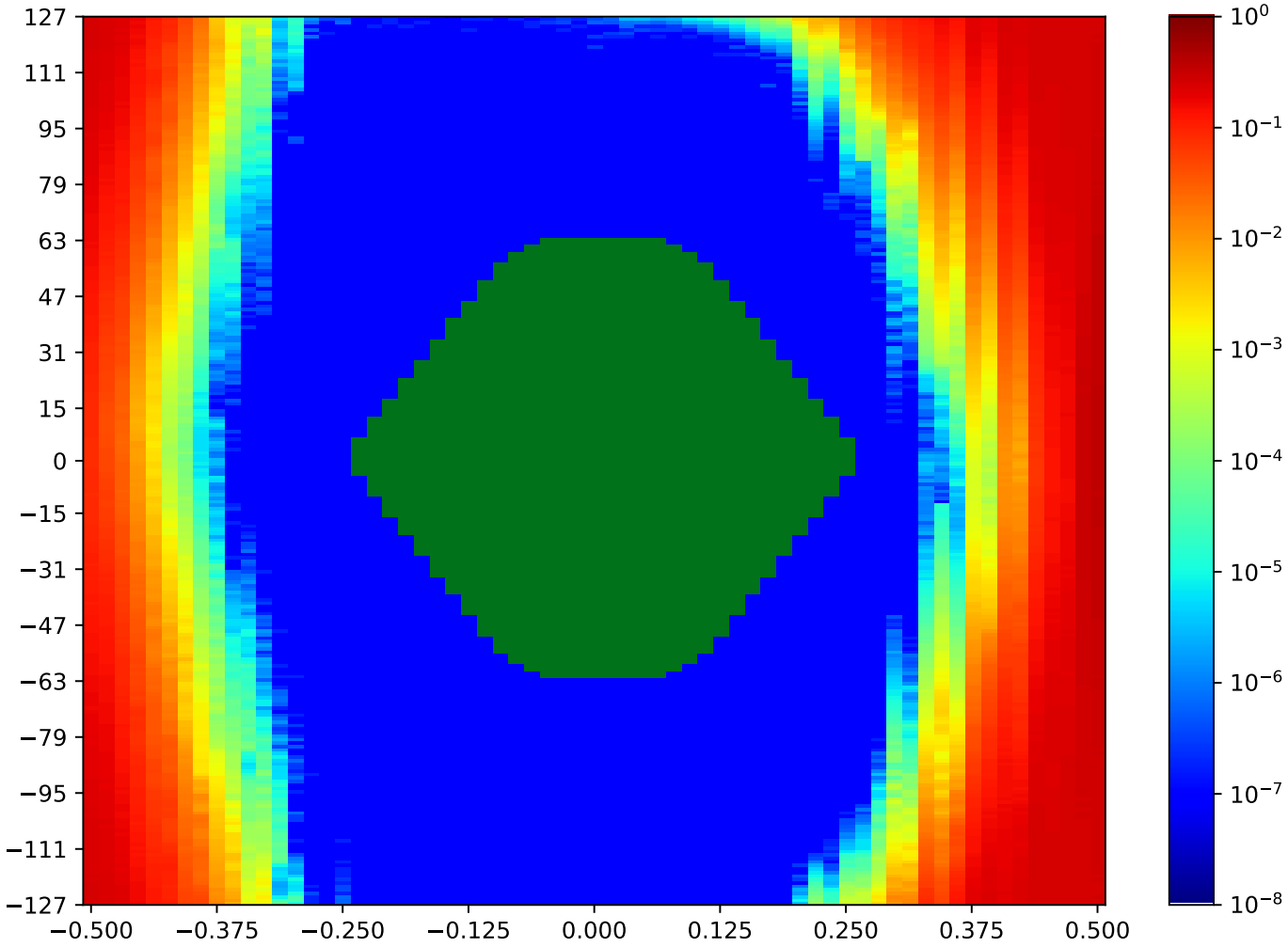


Figure 4.144: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.5 MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Table 4.134: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:18:58		2018-Sep-27 16:19:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9059	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

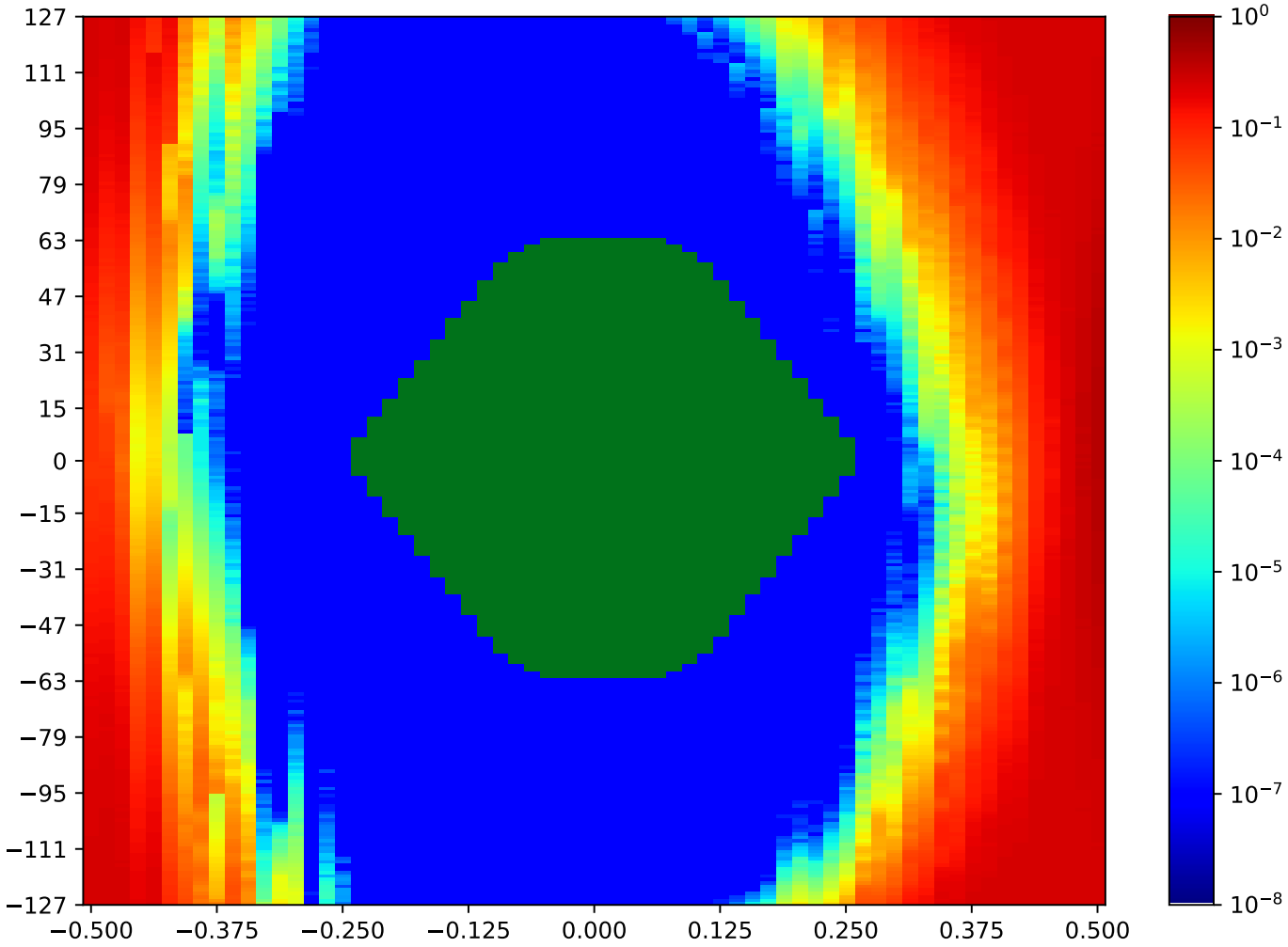


Figure 4.145: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.6 MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Table 4.135: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:16:34		2018-Sep-27 16:16:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8330	42	64.62%	240	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

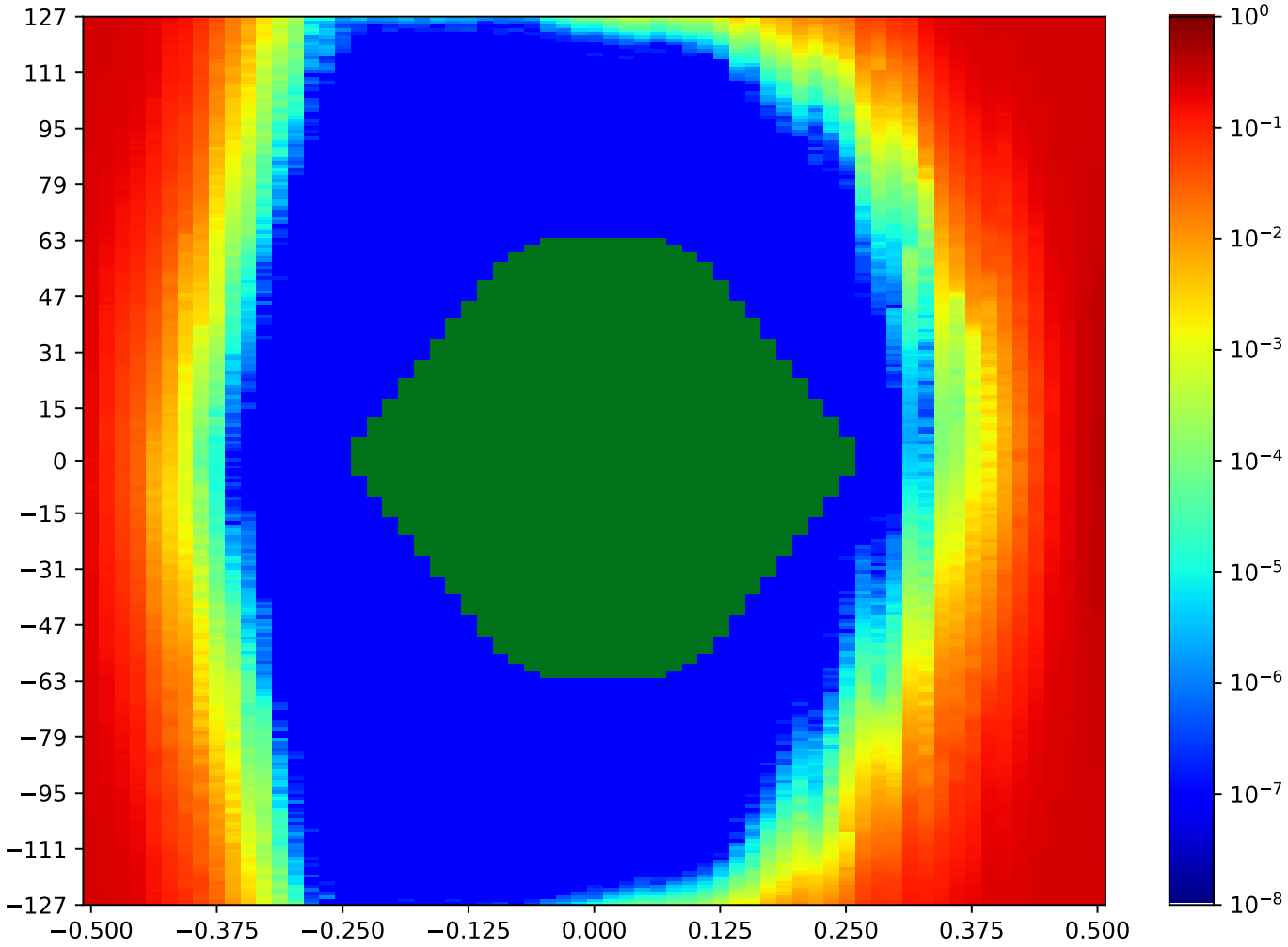


Figure 4.146: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.7 MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Table 4.136: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:19:39		2018-Sep-27 16:19:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8648	42	64.62%	234	91.37%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

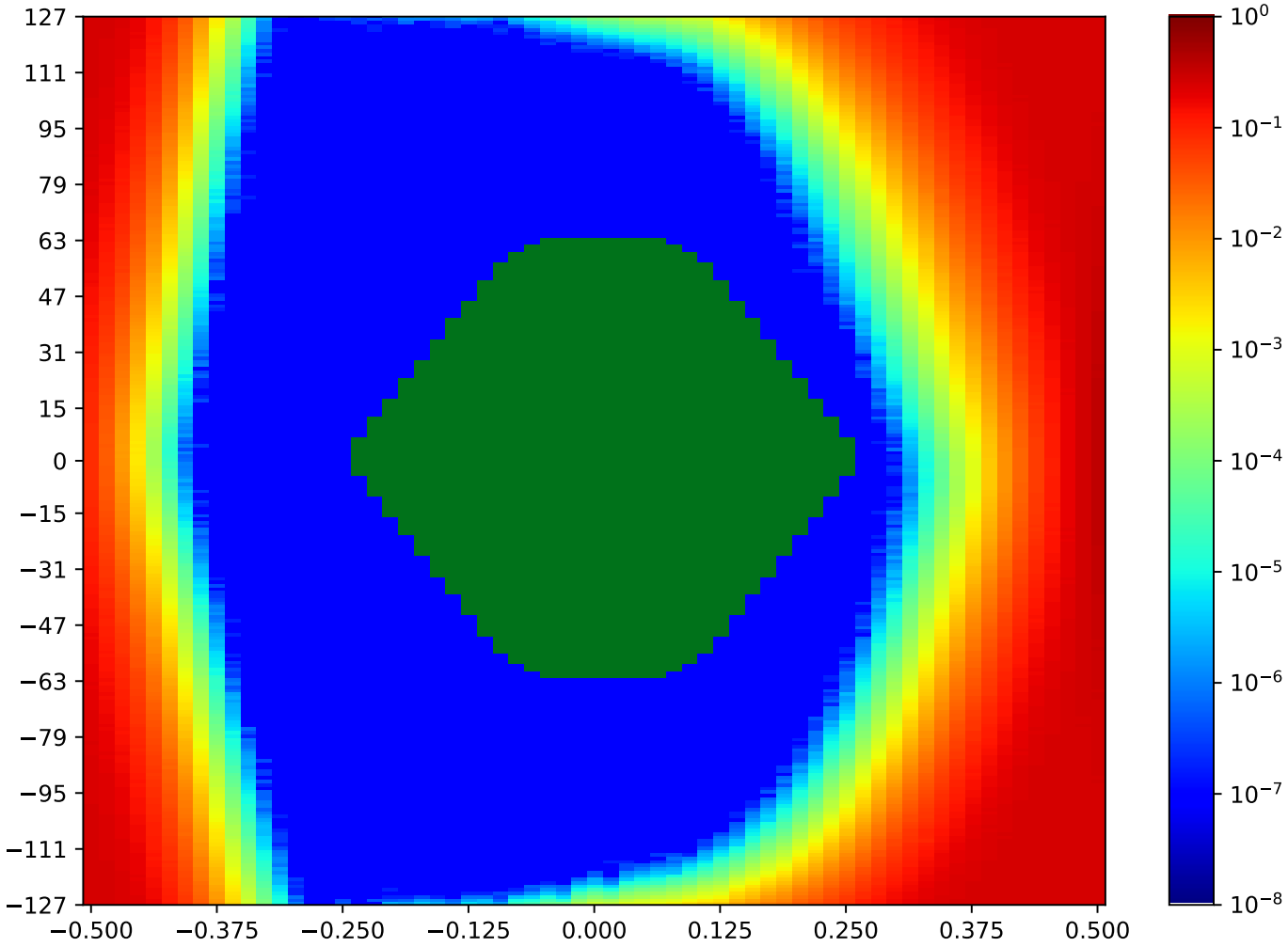


Figure 4.147: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.8 MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Table 4.137: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:17:16		2018-Sep-27 16:17:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8583	44	67.69%	233	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

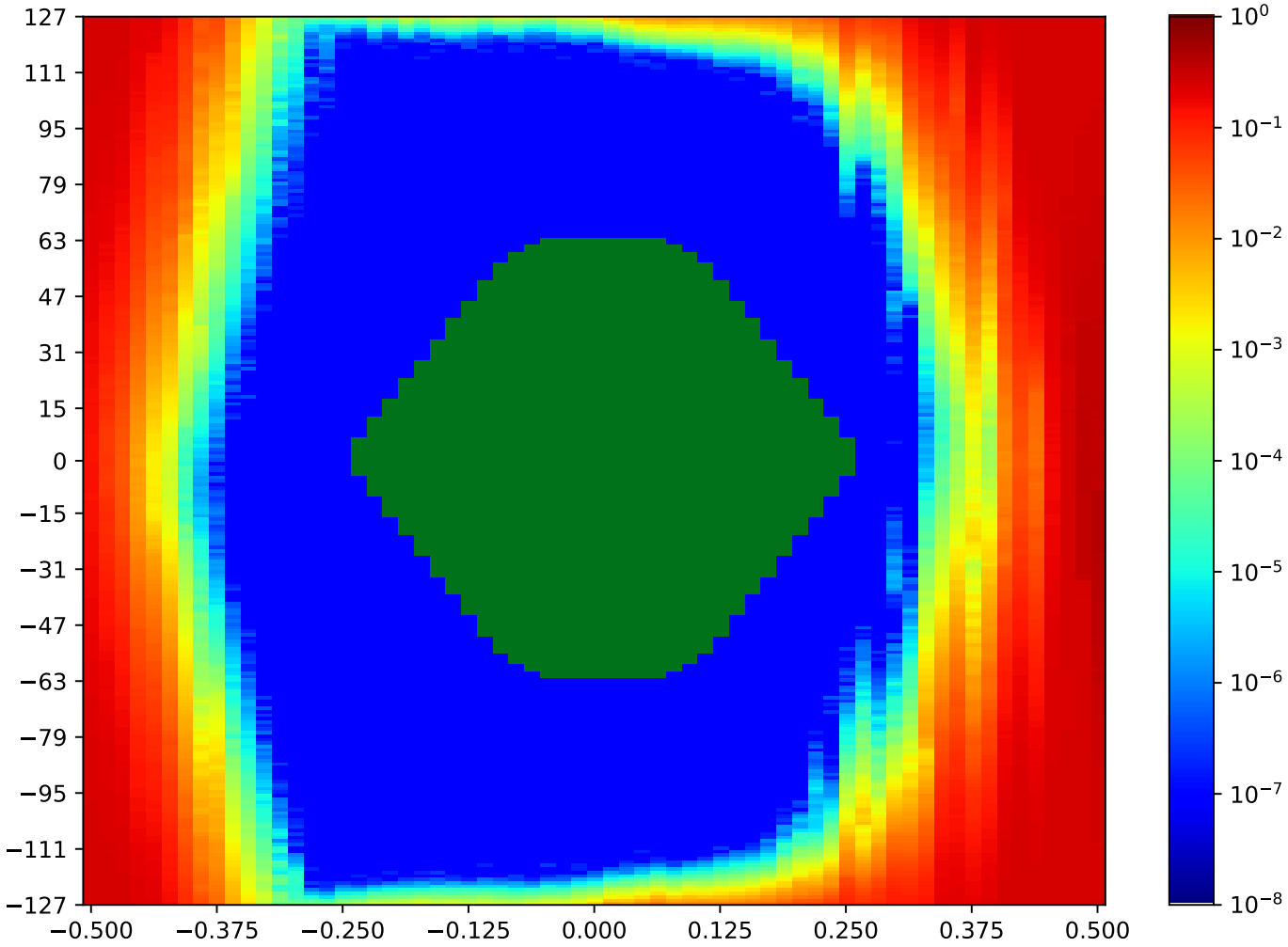


Figure 4.148: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.9 MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Table 4.138: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:19:19		2018-Sep-27 16:19:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8829	43	66.15%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

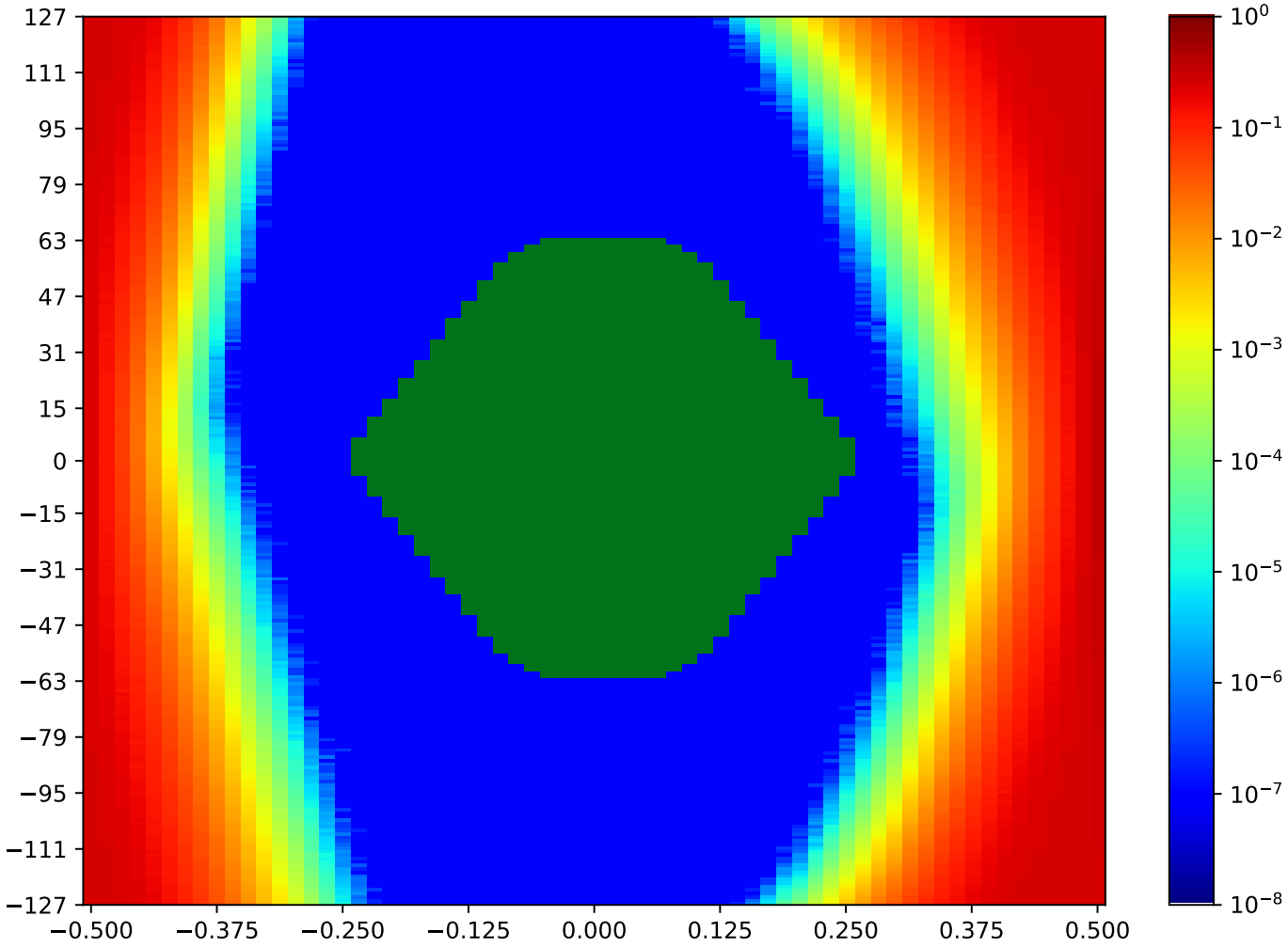


Figure 4.149: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.10 MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Table 4.139: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:17:36		2018-Sep-27 16:17:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8664	40	61.54%	247	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

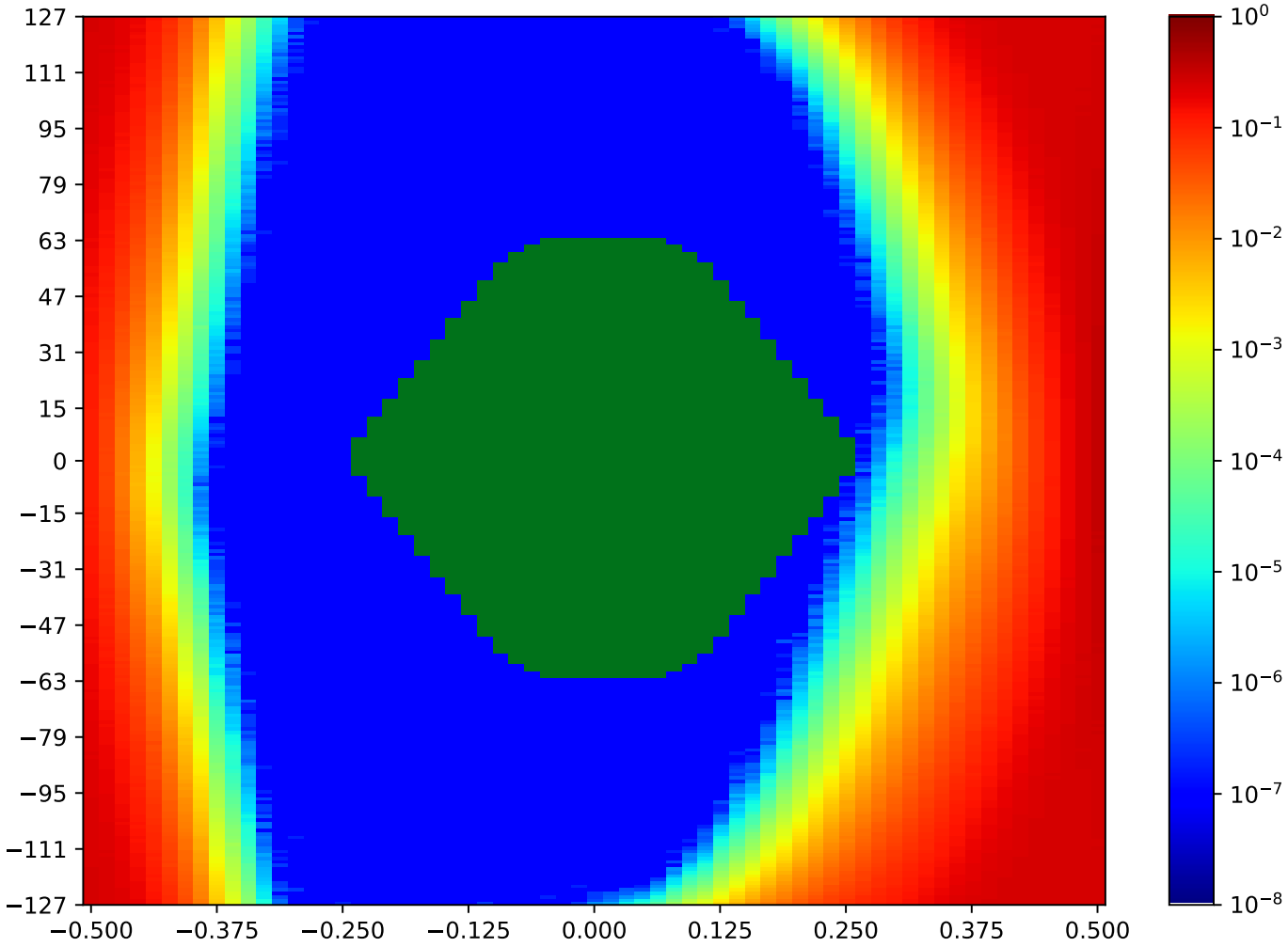


Figure 4.150: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.11 MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Table 4.140: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:18:37		2018-Sep-27 16:18:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9239	43	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

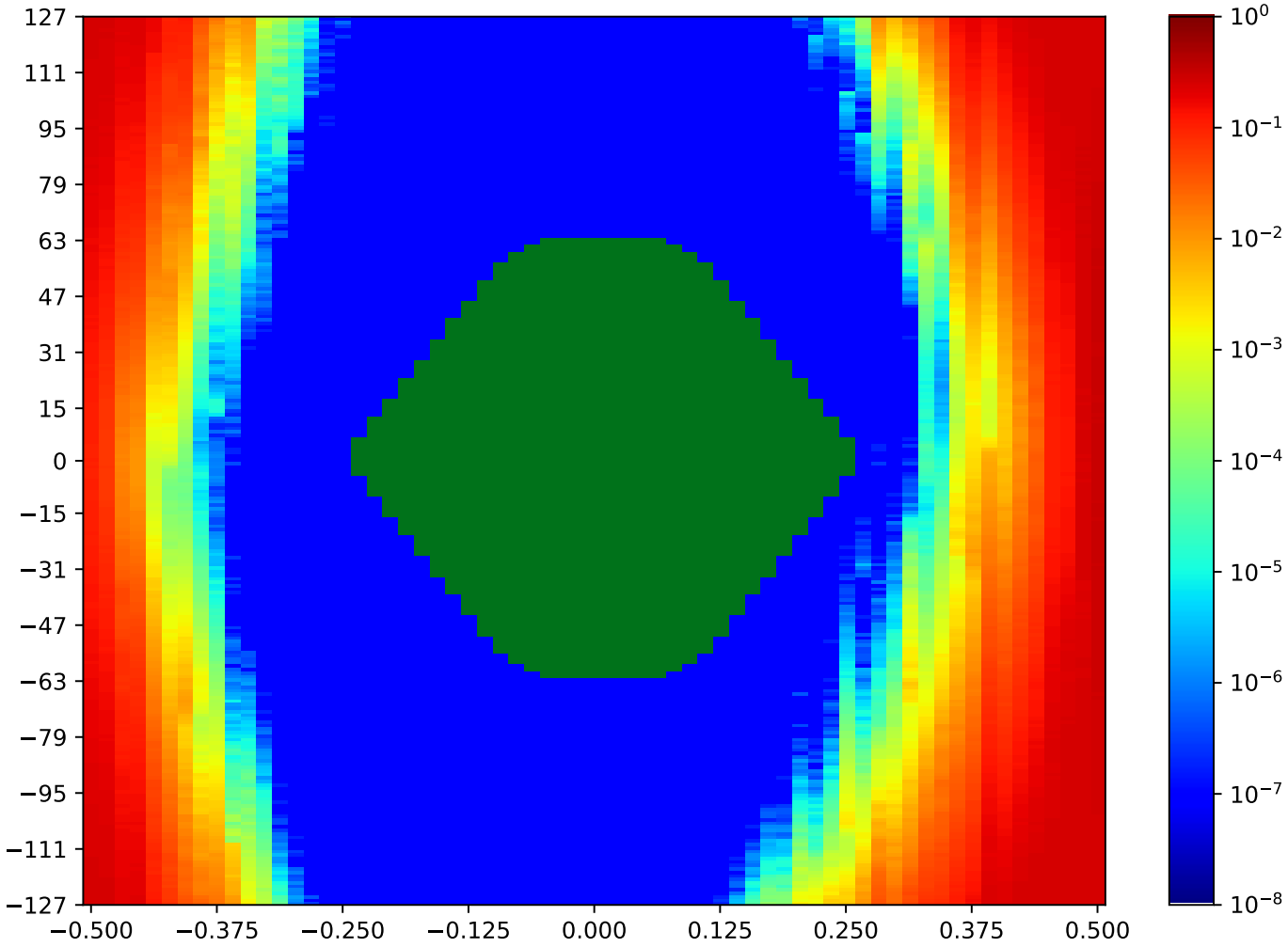


Figure 4.151: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.11.12 MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Table 4.141: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:18:17		2018-Sep-27 16:18:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9537	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

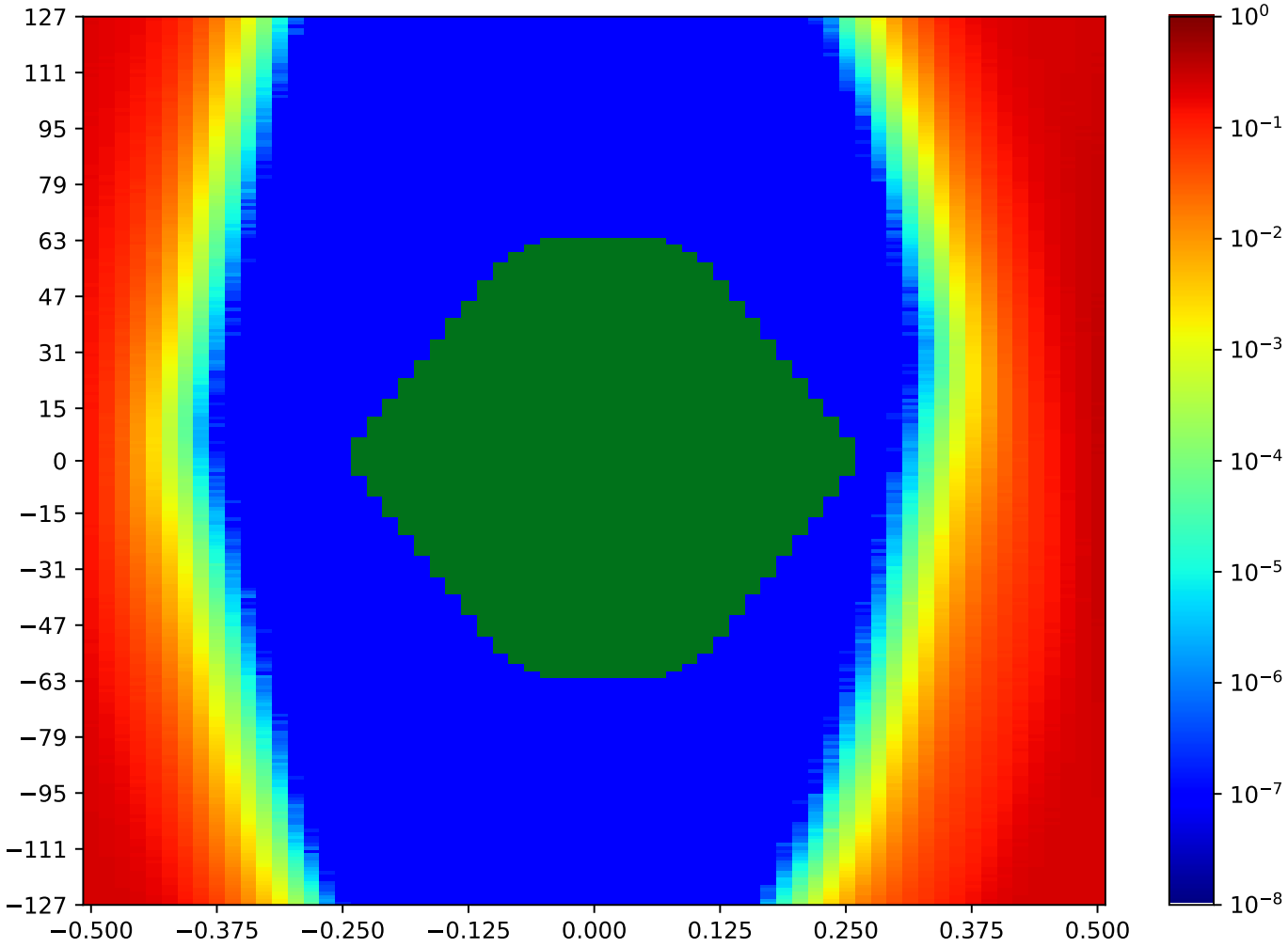


Figure 4.152: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12 MSP_C TX3 MSP_A RX8 Minipod Loopback

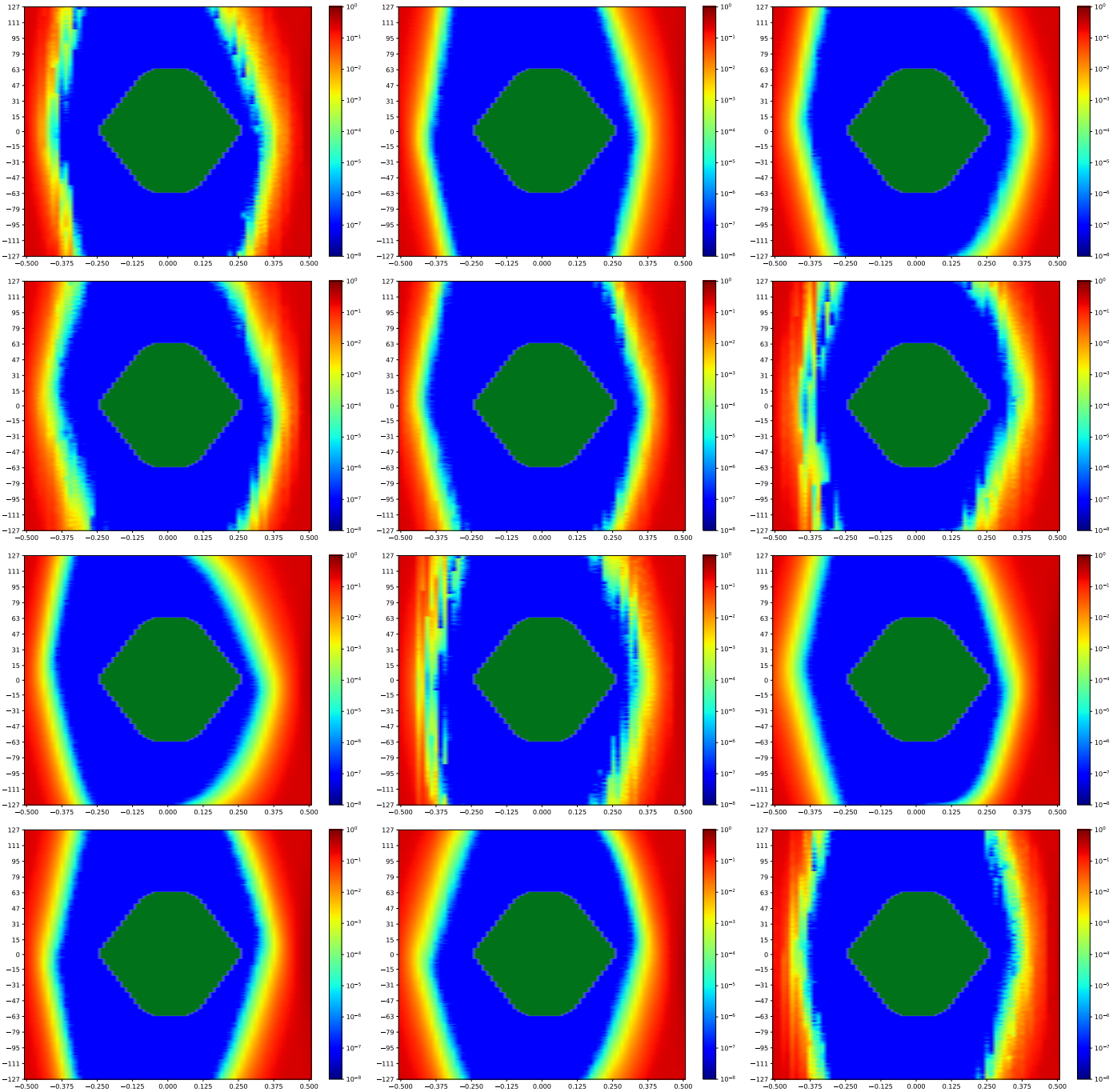


Figure 4.153: MSP_C TX3 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.166.

4.12.1 MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Table 4.142: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:21:02		2018-Sep-27 16:21:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9533	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

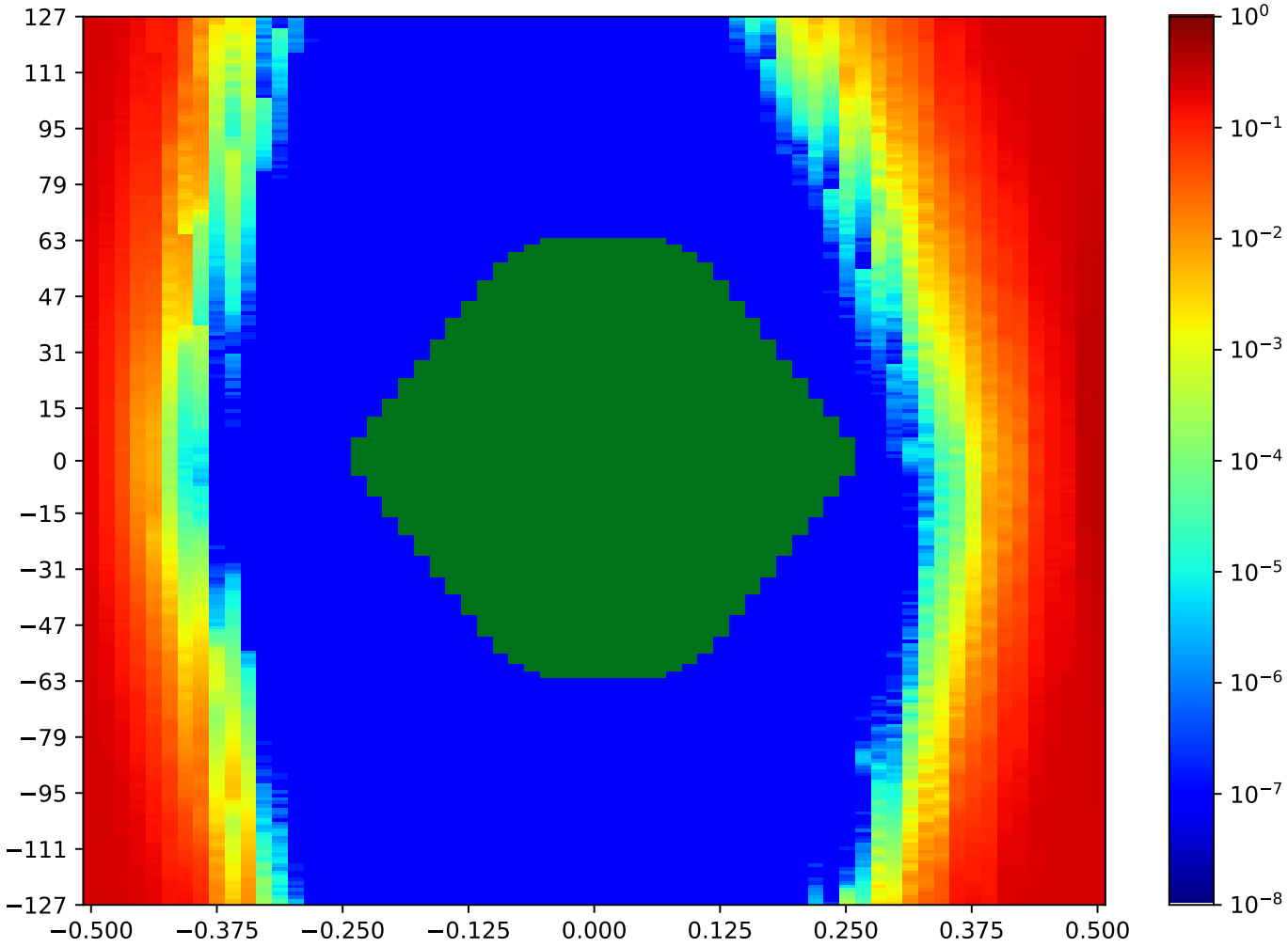


Figure 4.154: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.2 MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Table 4.143: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:21:43		2018-Sep-27 16:22:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9705	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

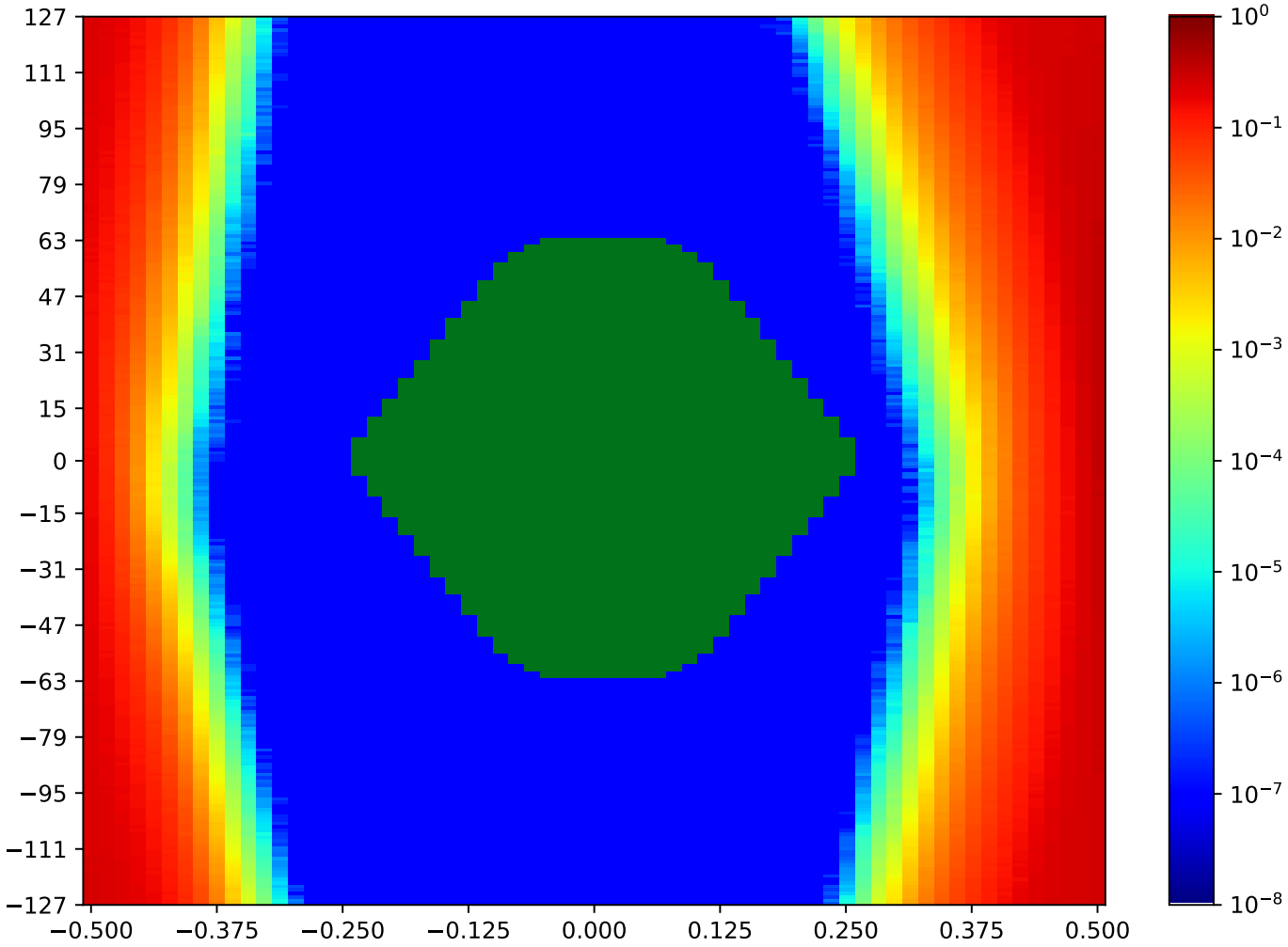


Figure 4.155: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.3 MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Table 4.144: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:22:03		2018-Sep-27 16:22:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9390	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

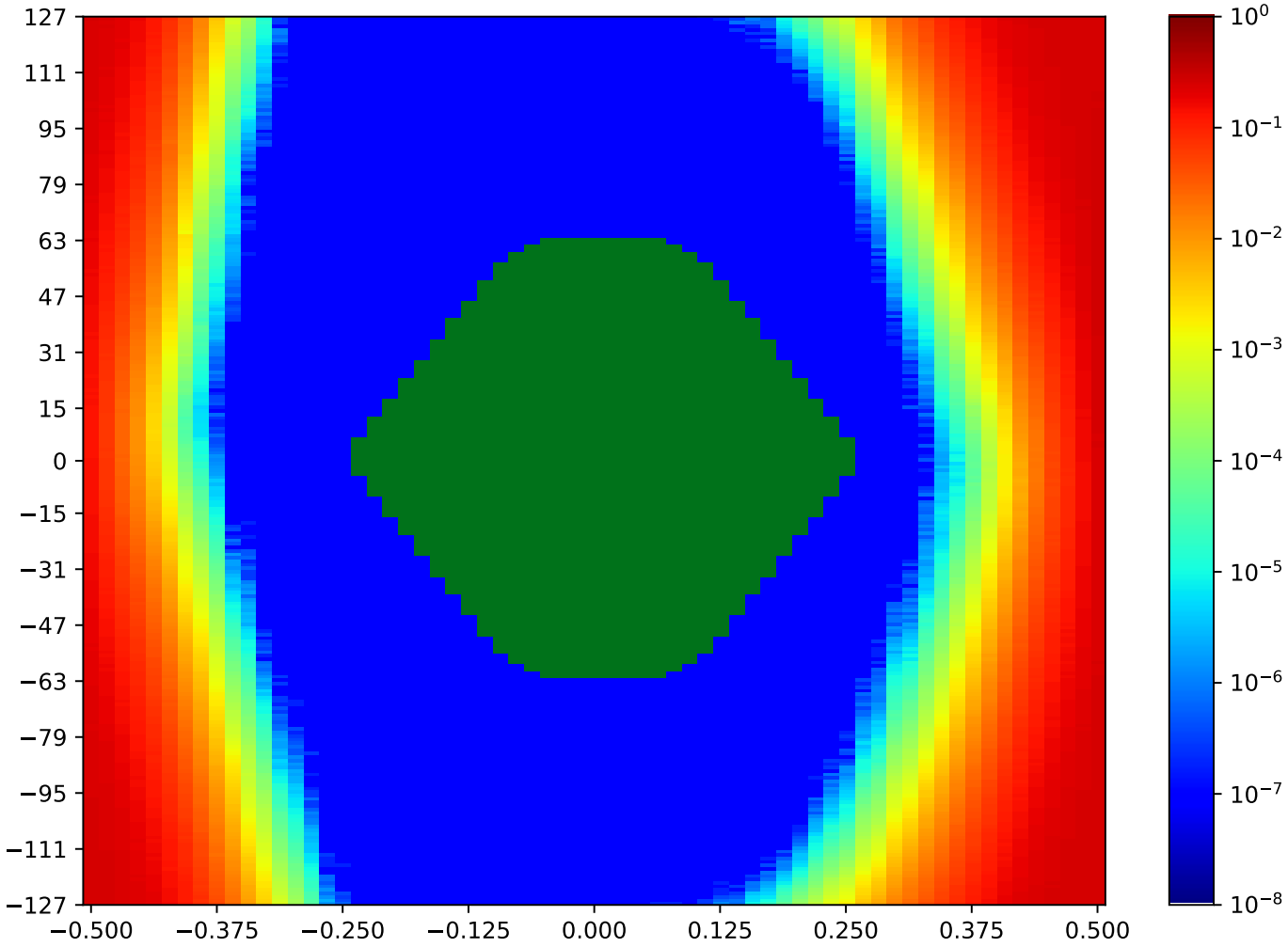


Figure 4.156: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.4 MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Table 4.145: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:20:20		2018-Sep-27 16:20:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9465	44	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

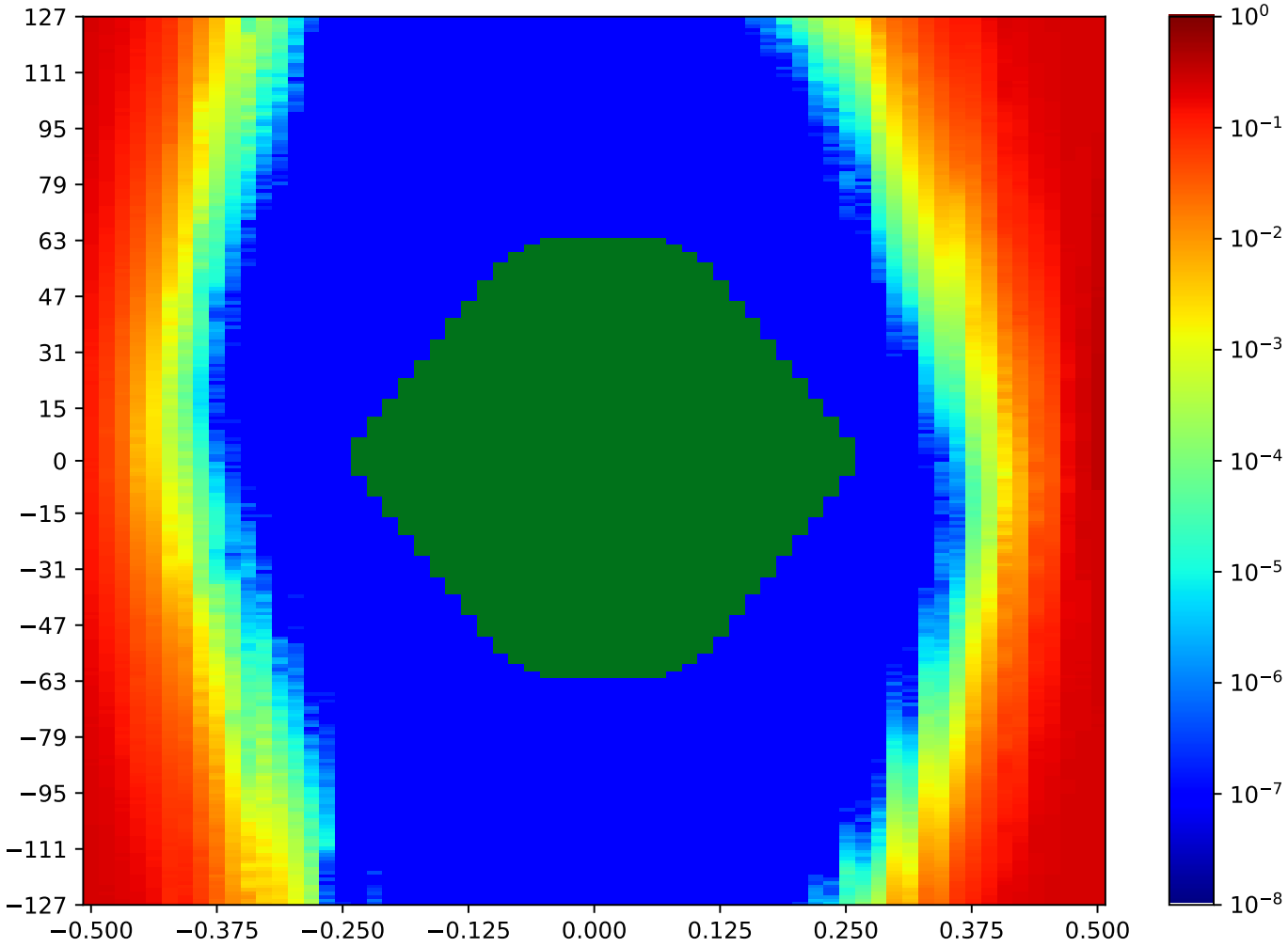


Figure 4.157: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.5 MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Table 4.146: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:23:05		2018-Sep-27 16:23:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9853	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

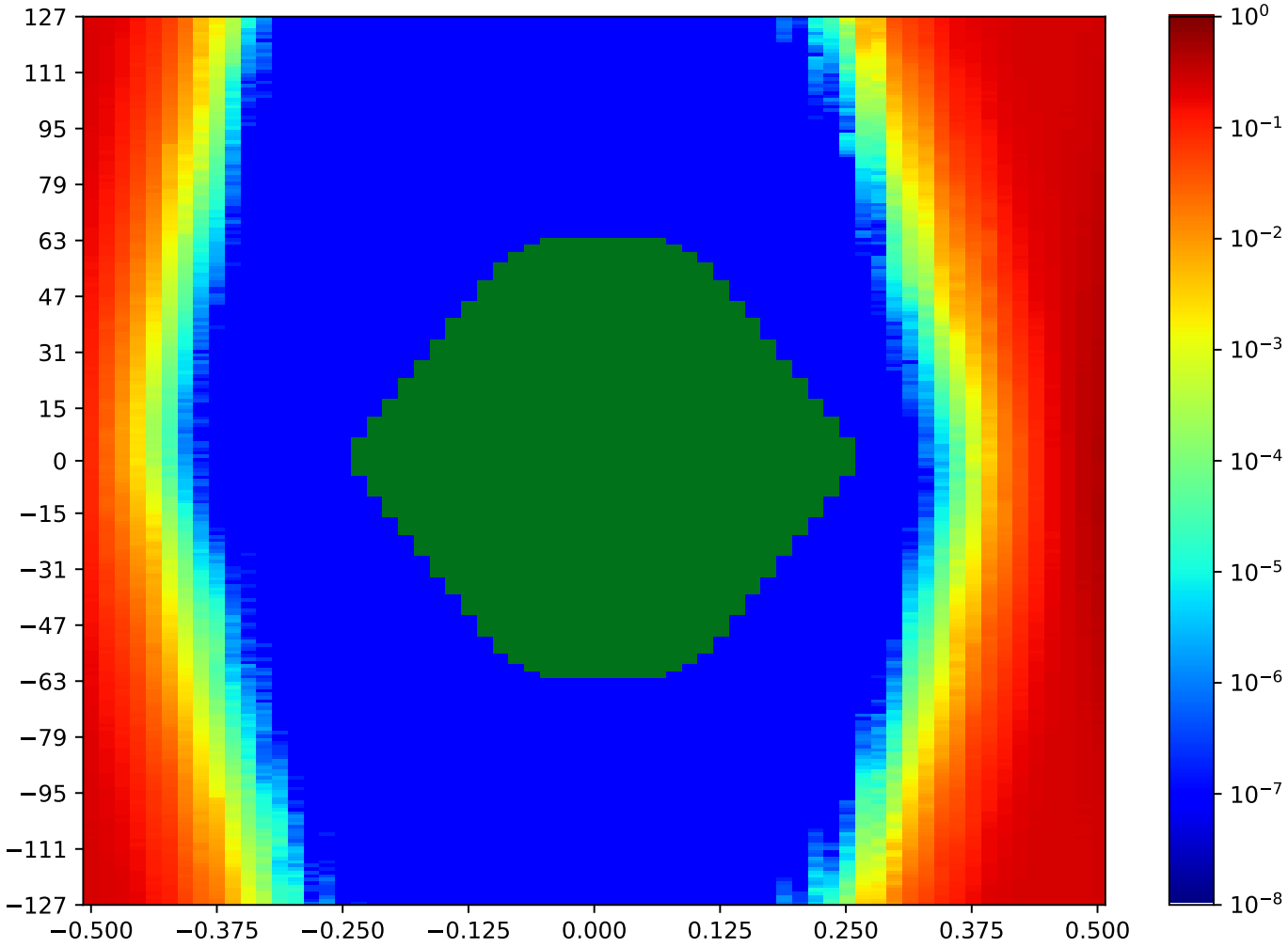


Figure 4.158: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.6 MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Table 4.147: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:20:00		2018-Sep-27 16:20:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8887	43	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

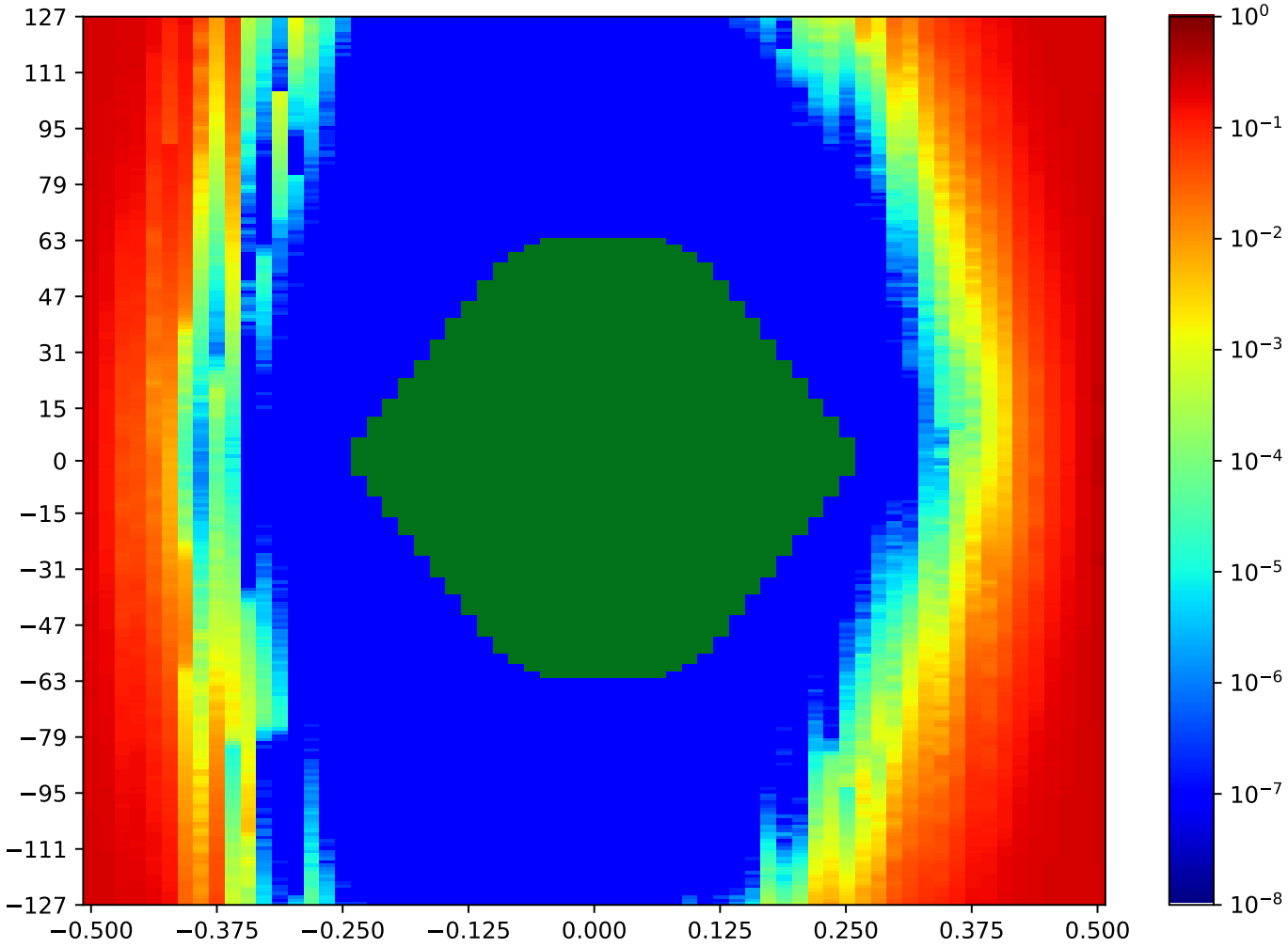


Figure 4.159: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.7 MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Table 4.148: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:23:46		2018-Sep-27 16:24:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8742	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

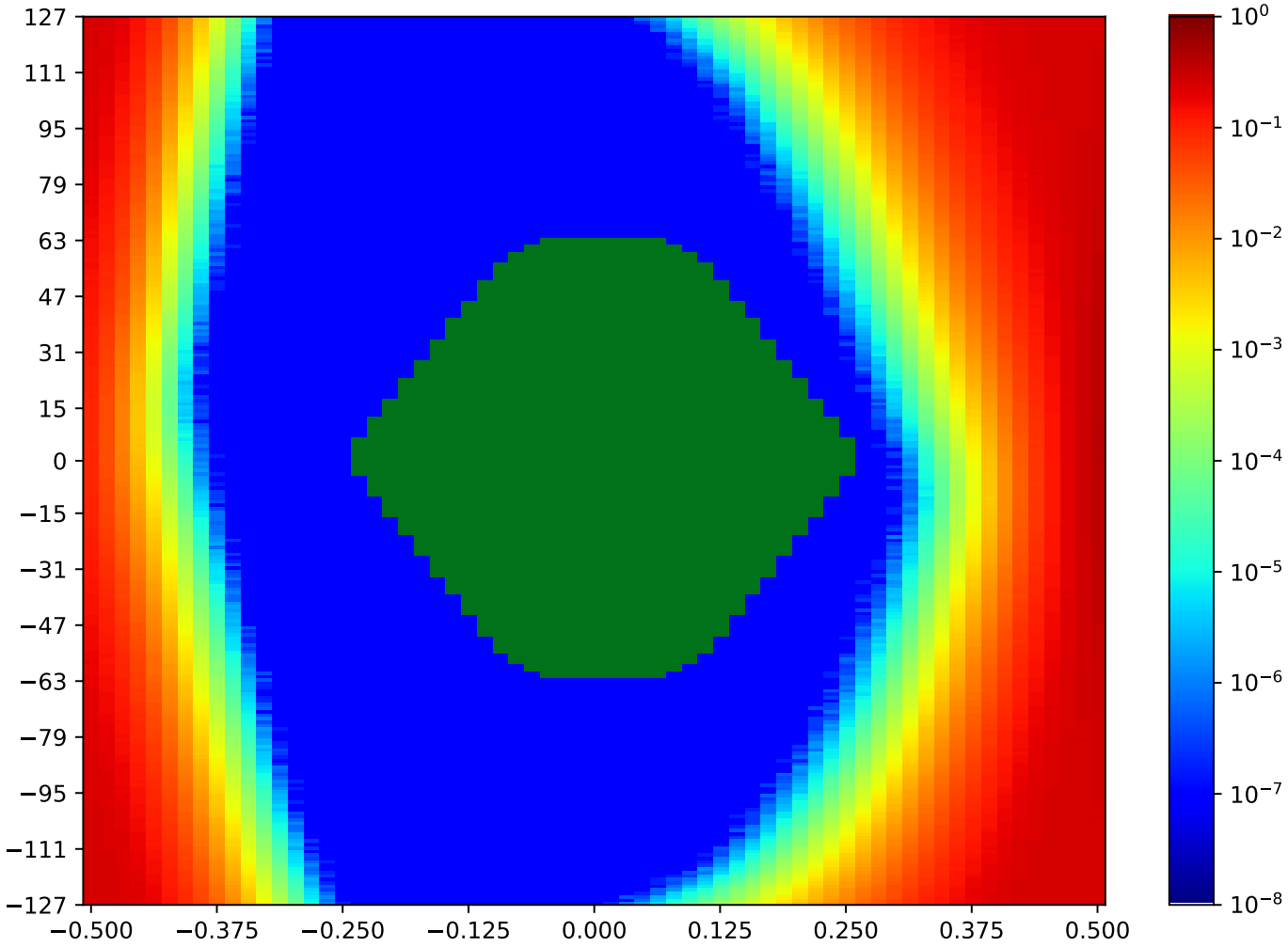


Figure 4.160: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.8 MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Table 4.149: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:20:41		2018-Sep-27 16:21:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9221	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

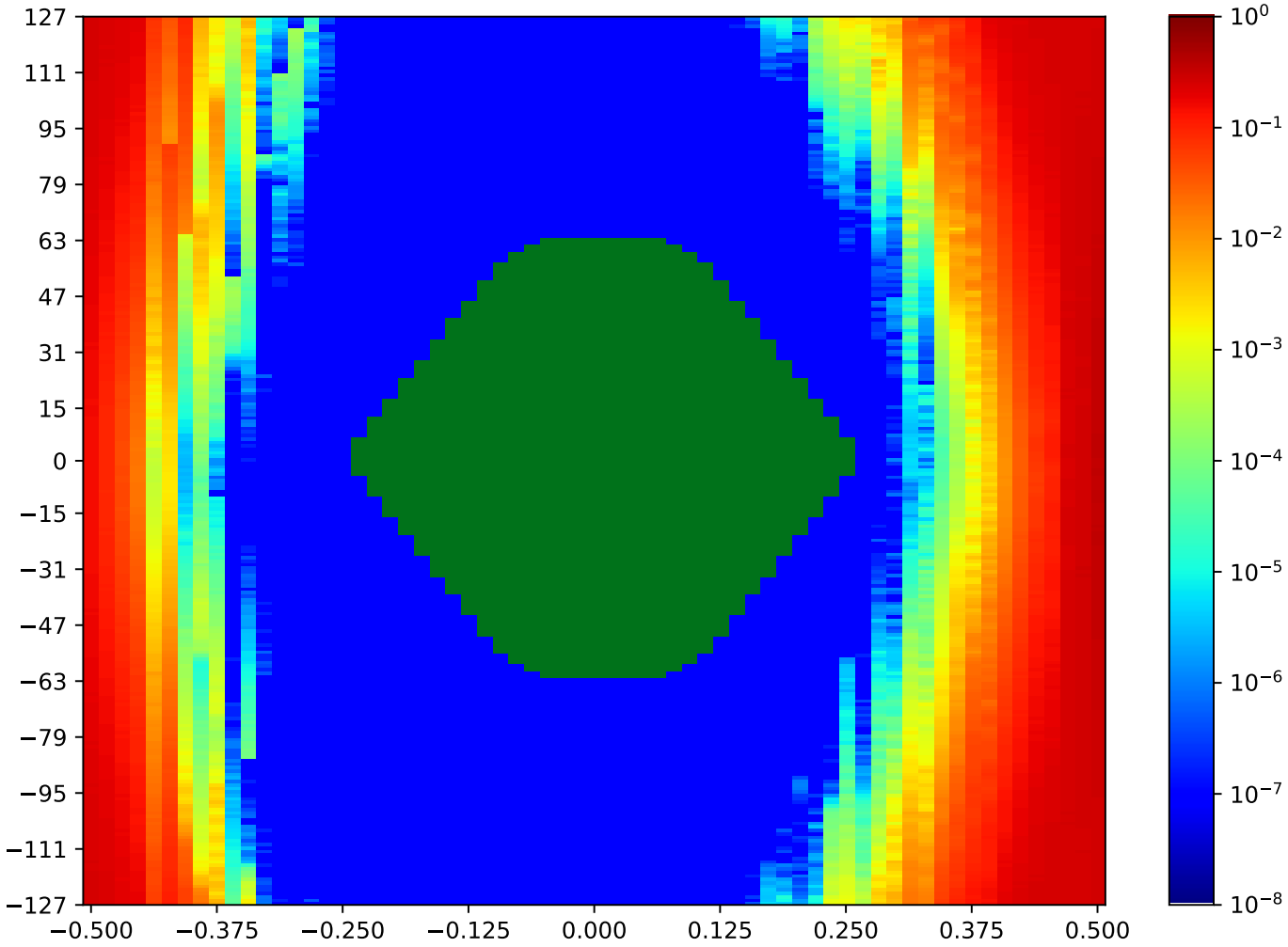


Figure 4.161: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.9 MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Table 4.150: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:23:26		2018-Sep-27 16:23:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8798	40	60.00%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

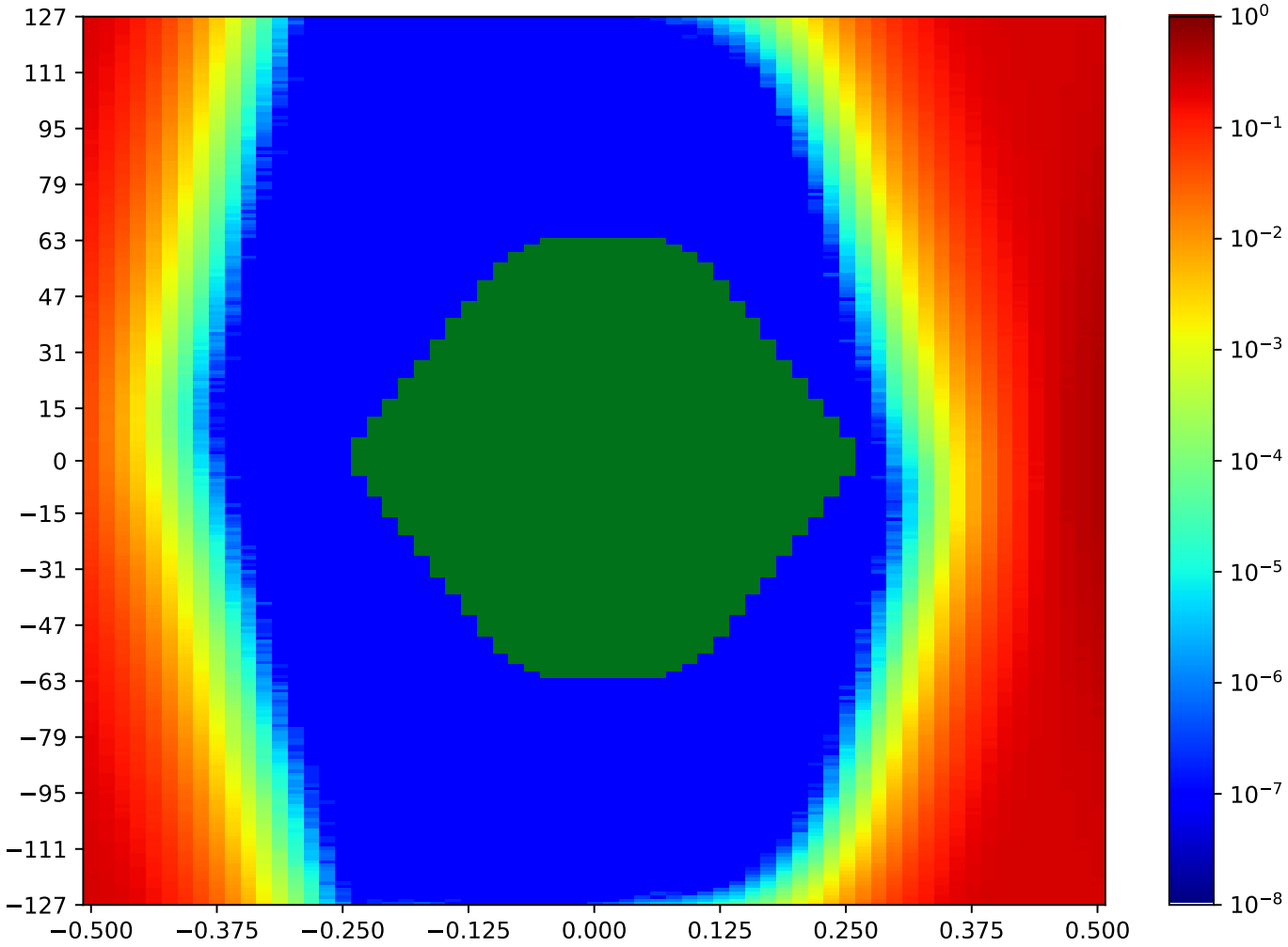


Figure 4.162: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.10 MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Table 4.151: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:21:22		2018-Sep-27 16:21:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9421	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

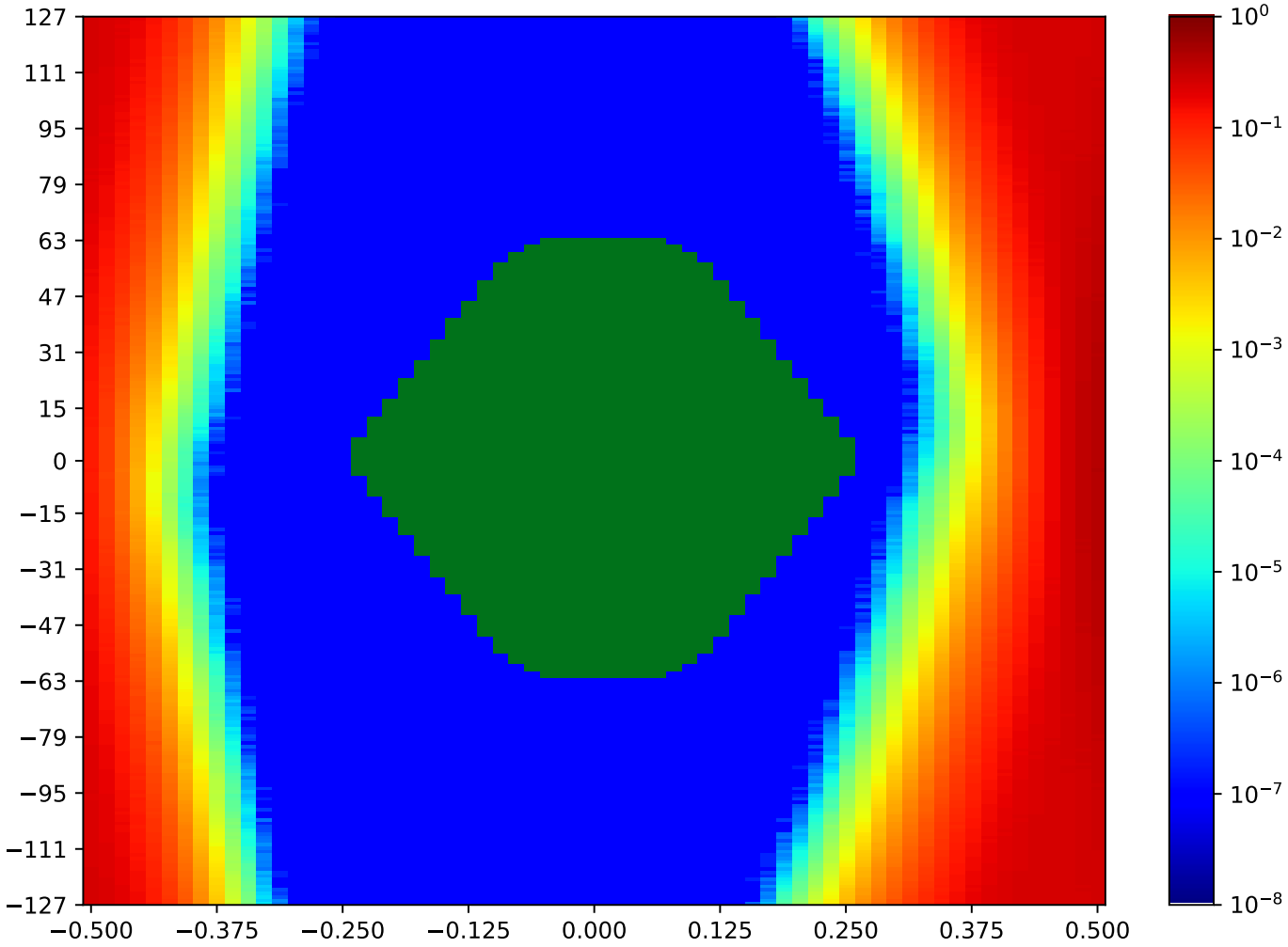


Figure 4.163: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.11 MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Table 4.152: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:22:45		2018-Sep-27 16:23:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8925	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

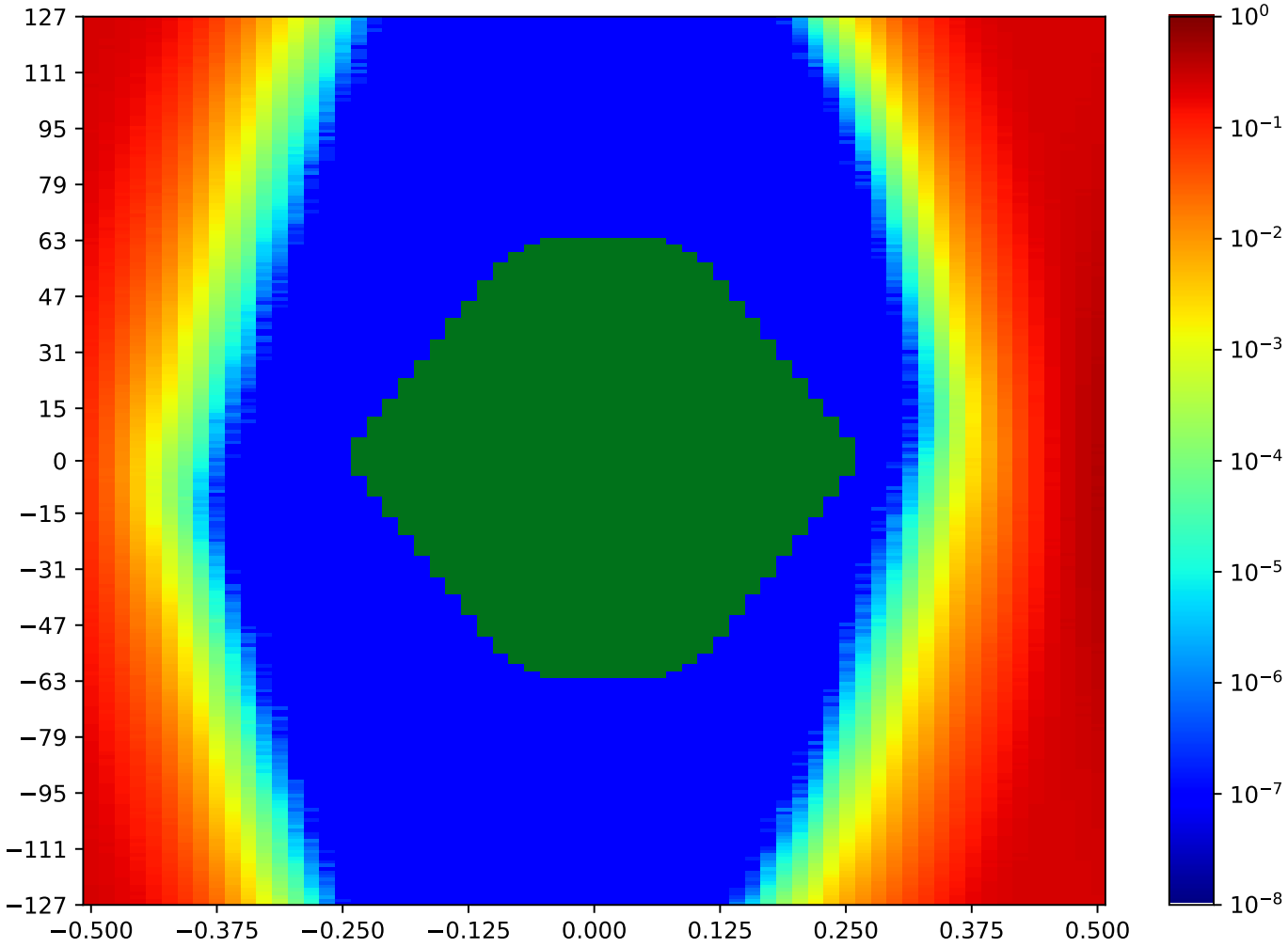


Figure 4.164: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.12.12 MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Table 4.153: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:22:24		2018-Sep-27 16:22:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9980	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

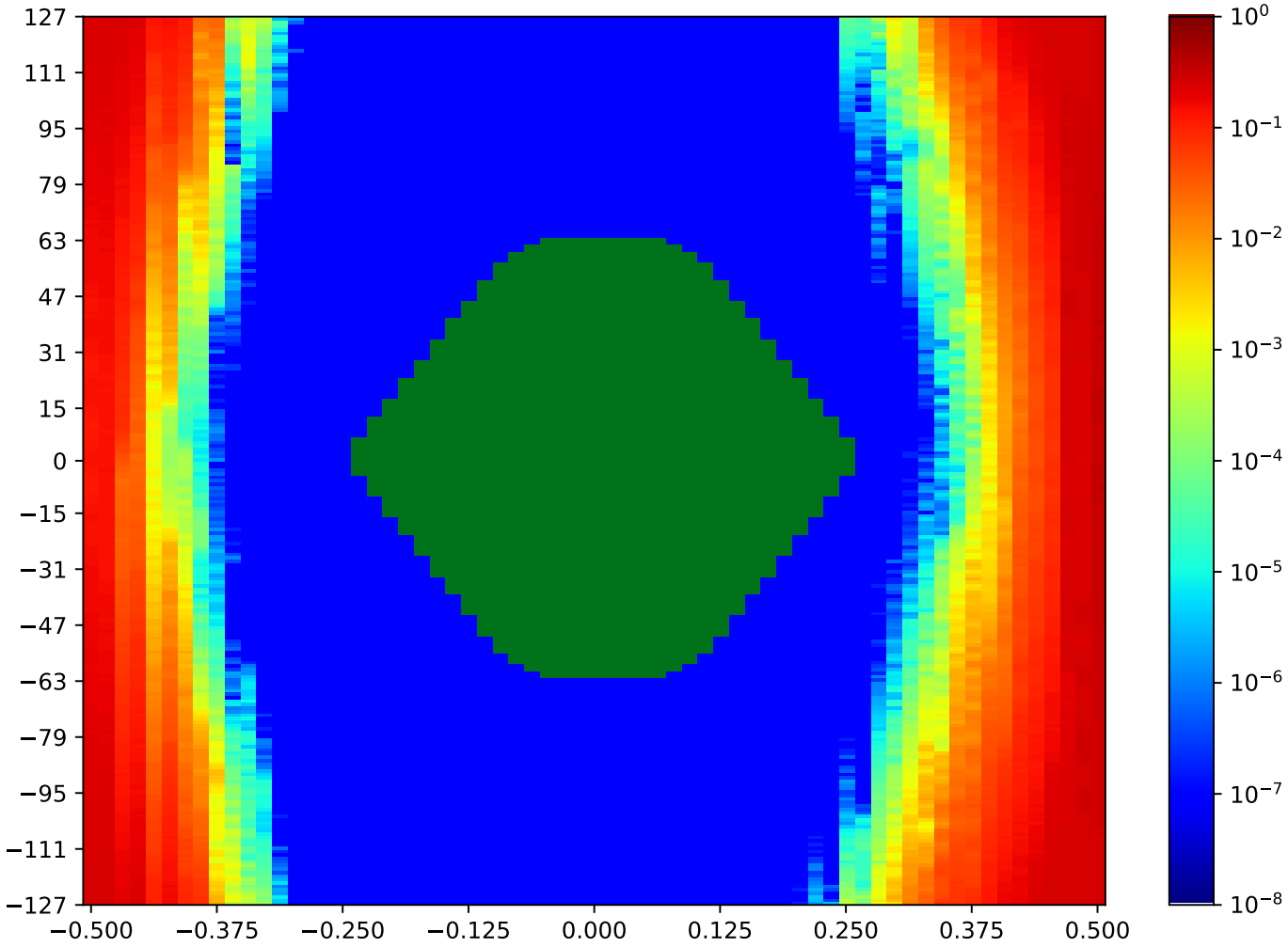


Figure 4.165: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13 MSP_C TX4 MSP_A RX9 Minipod Loopback

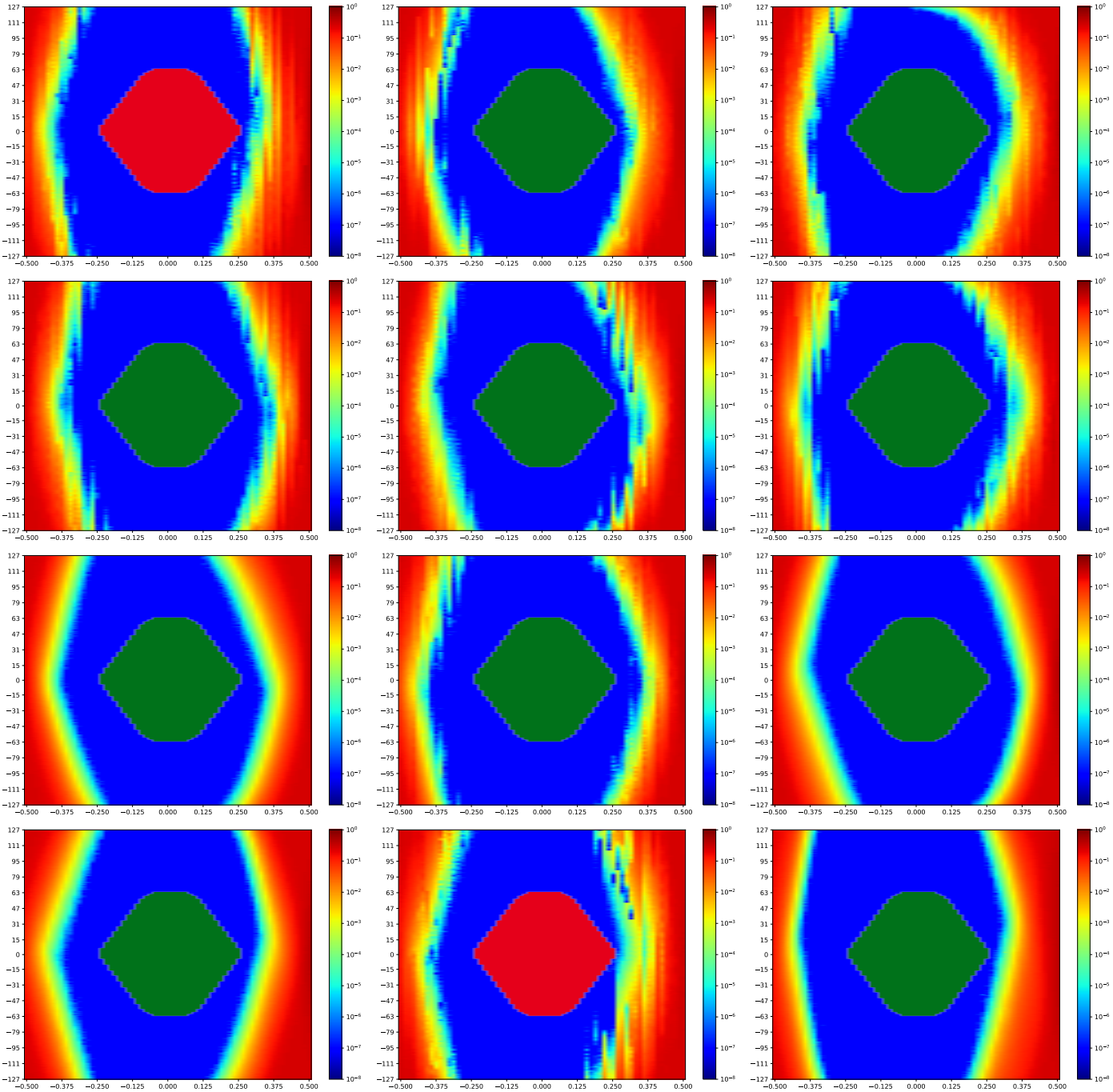


Figure 4.166: MSP_C TX4 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.179.

4.13.1 MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Table 4.154: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:25:12		2018-Sep-27 16:25:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9339	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

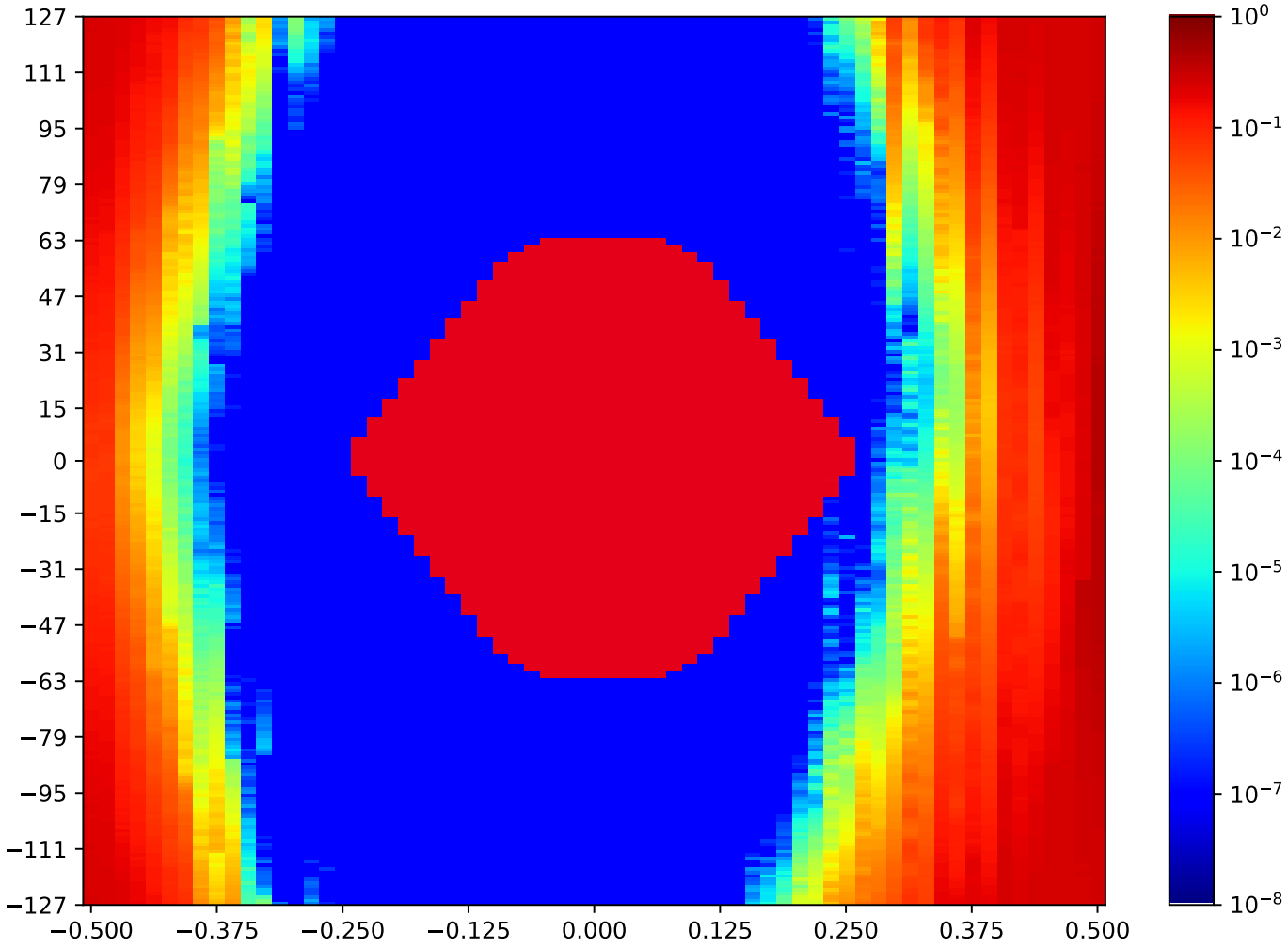


Figure 4.167: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.2 MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Table 4.155: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:24:30		2018-Sep-27 16:24:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8470	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

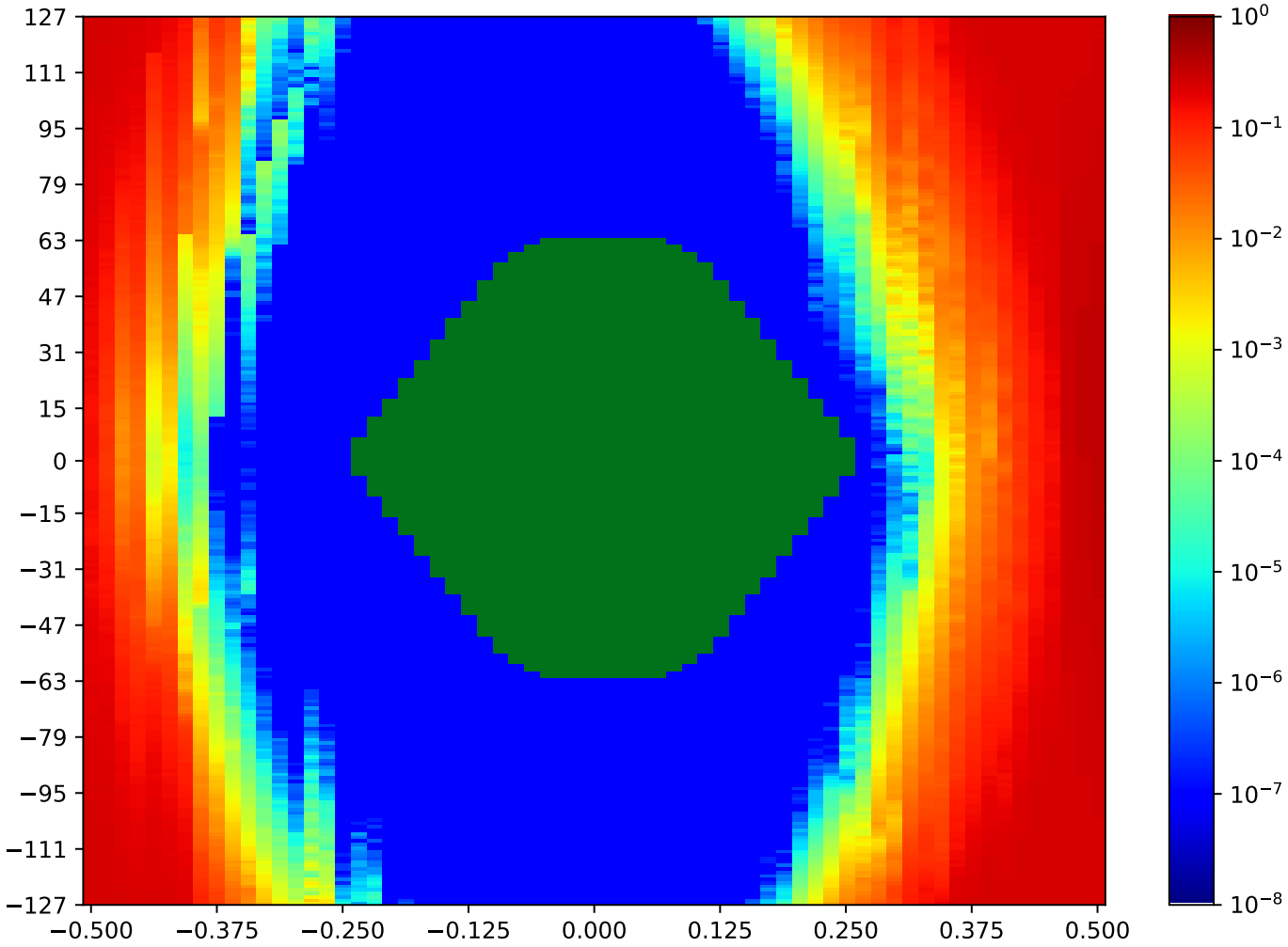


Figure 4.168: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.3 MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Table 4.156: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:26:18		2018-Sep-27 16:26:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8330	41	63.08%	248	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

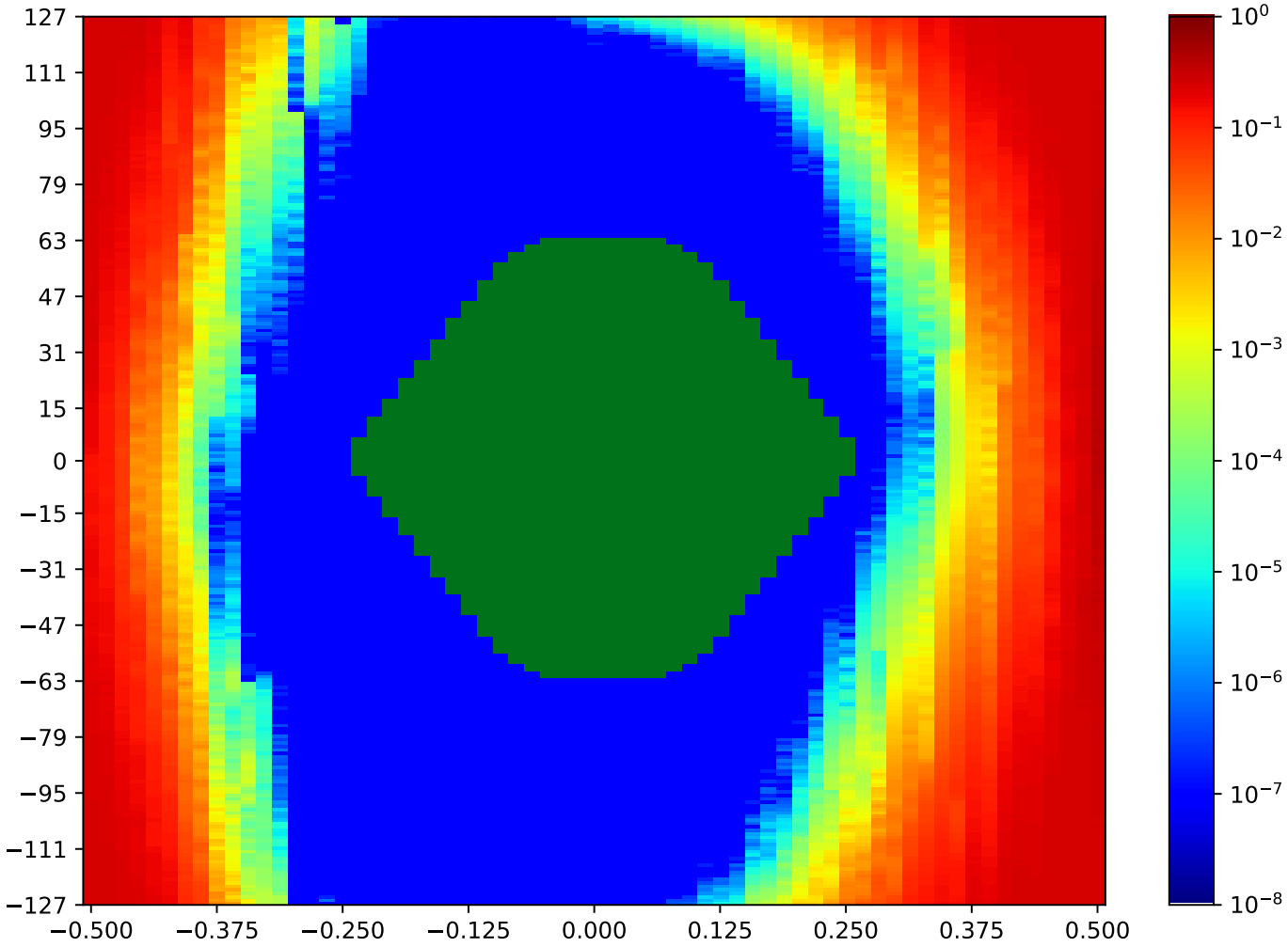


Figure 4.169: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.4 MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Table 4.157: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:24:10		2018-Sep-27 16:24:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9080	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

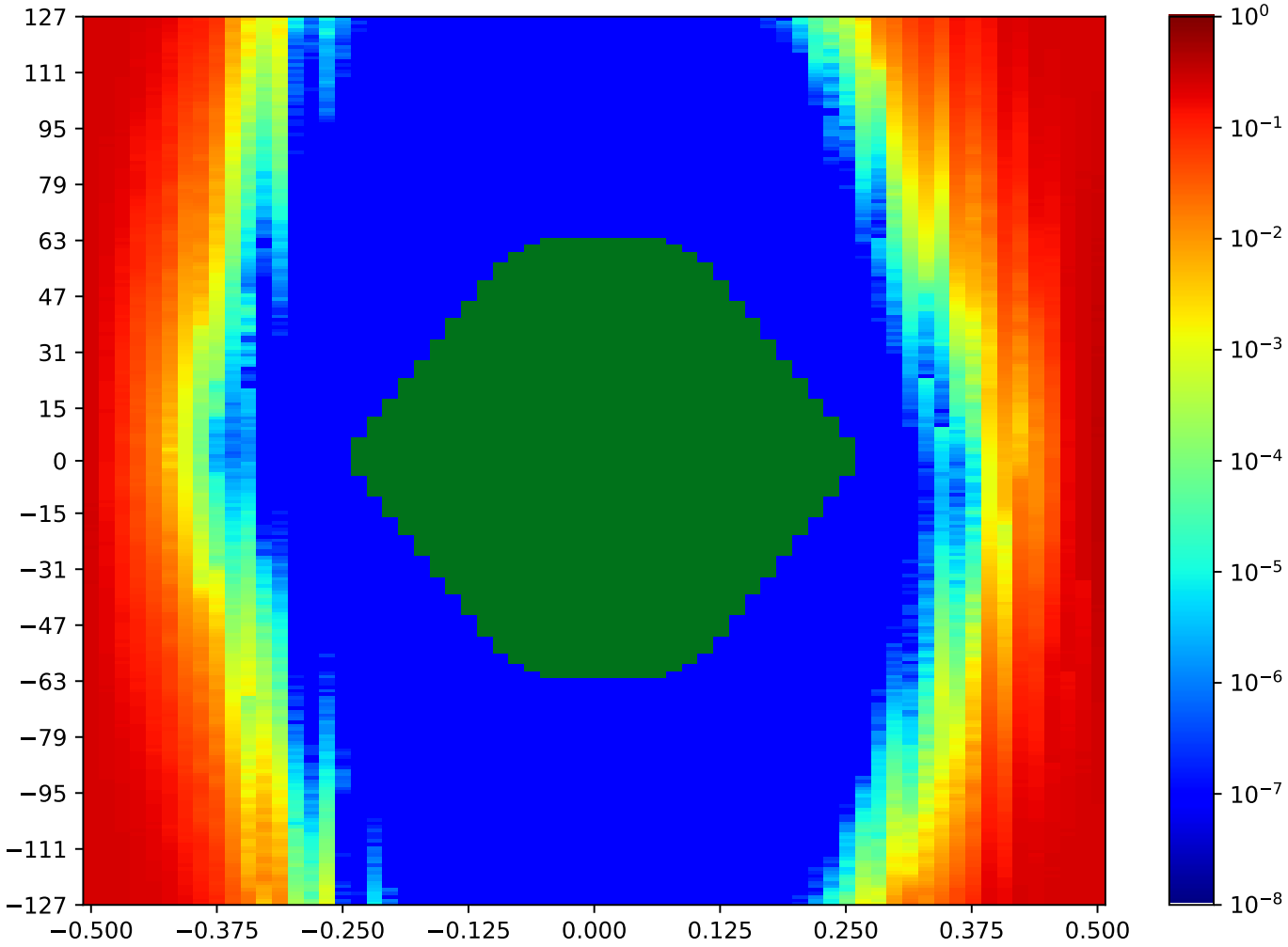


Figure 4.170: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.5 MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Table 4.158: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:27:20		2018-Sep-27 16:27:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8626	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

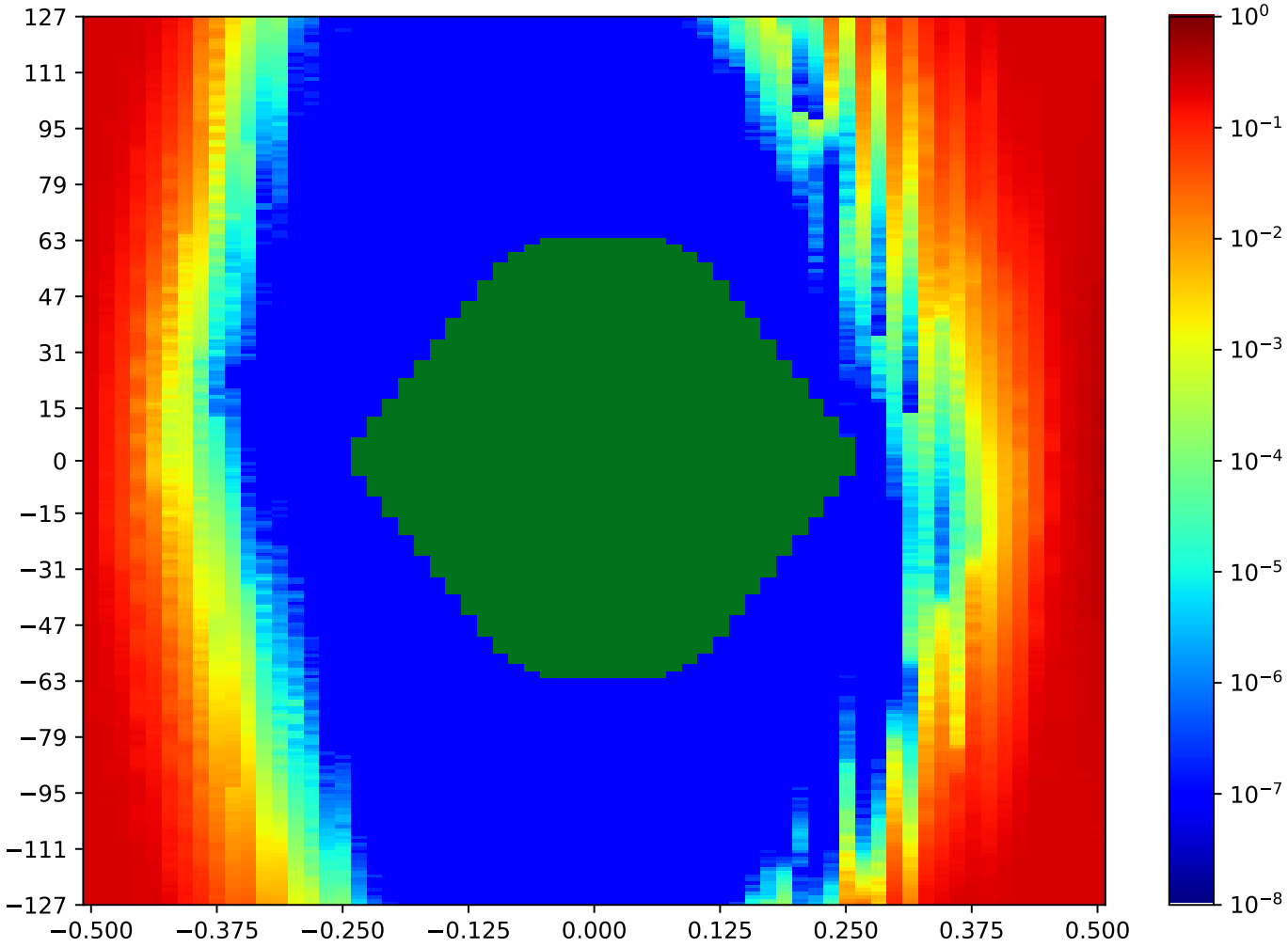


Figure 4.171: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.6 MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Table 4.159: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:24:51		2018-Sep-27 16:25:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8840	43	64.62%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

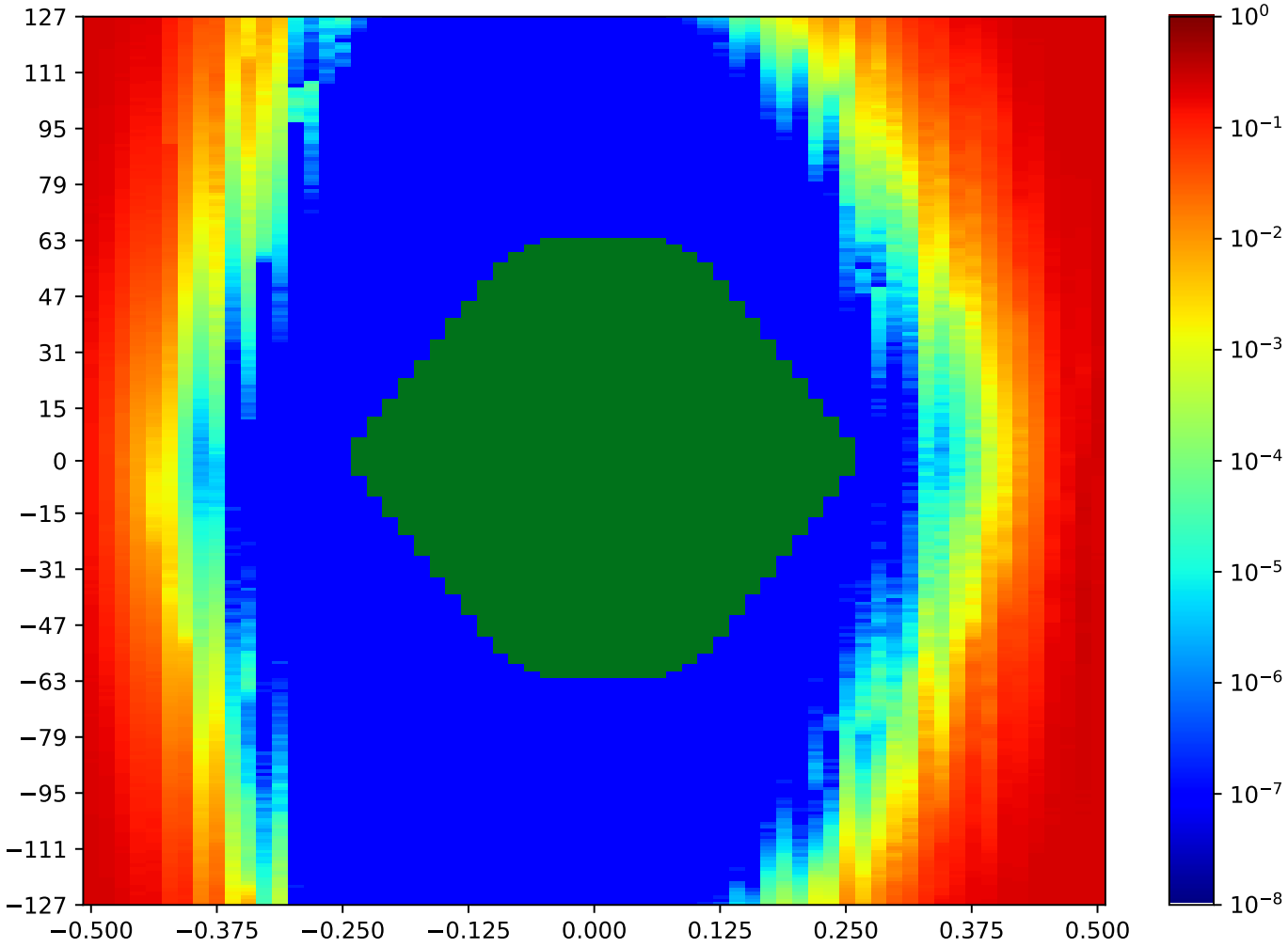


Figure 4.172: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.7 MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Table 4.160: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:28:01		2018-Sep-27 16:28:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8832	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

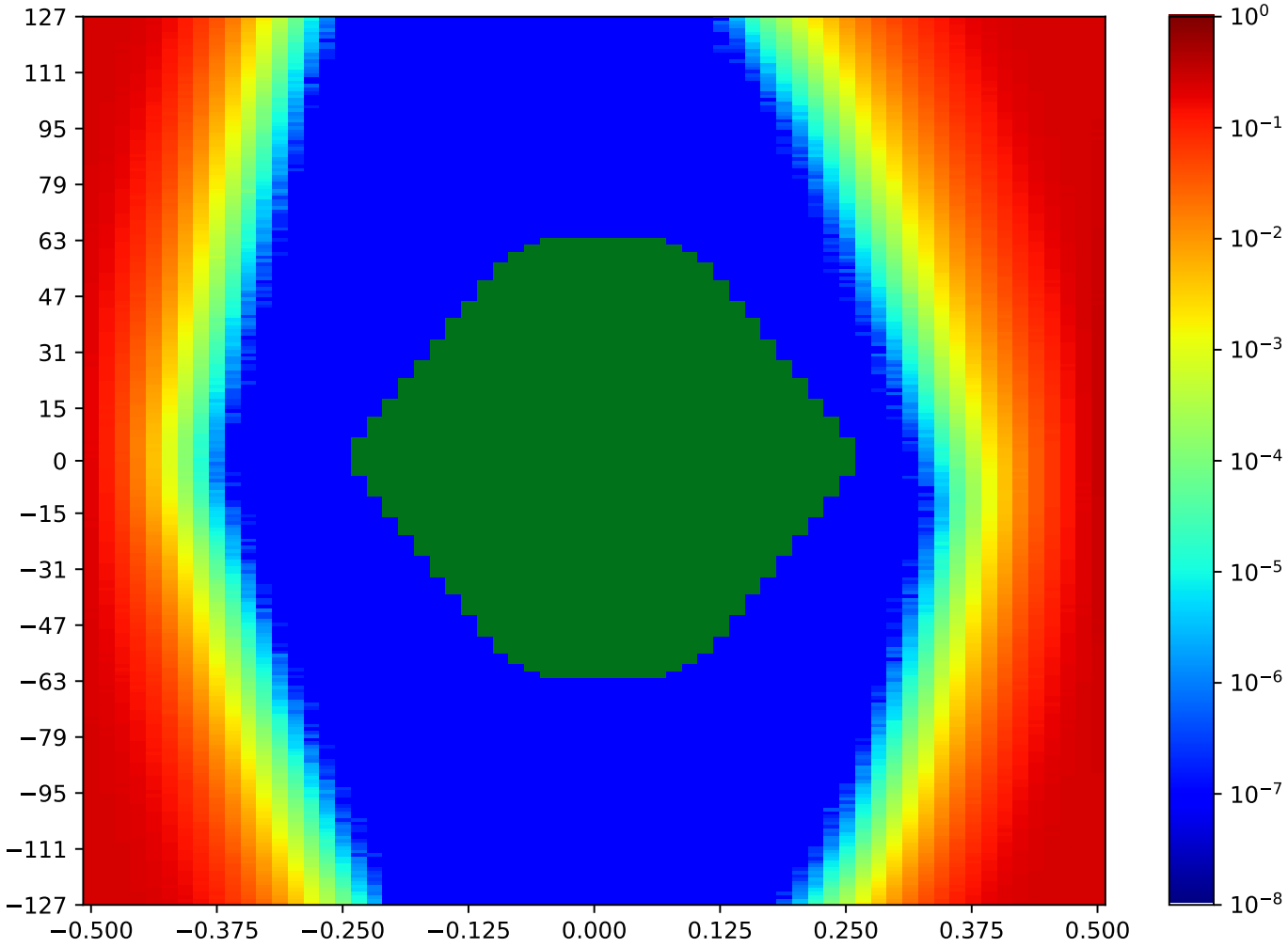


Figure 4.173: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.8 MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Table 4.161: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:25:38		2018-Sep-27 16:25:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9755	47	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

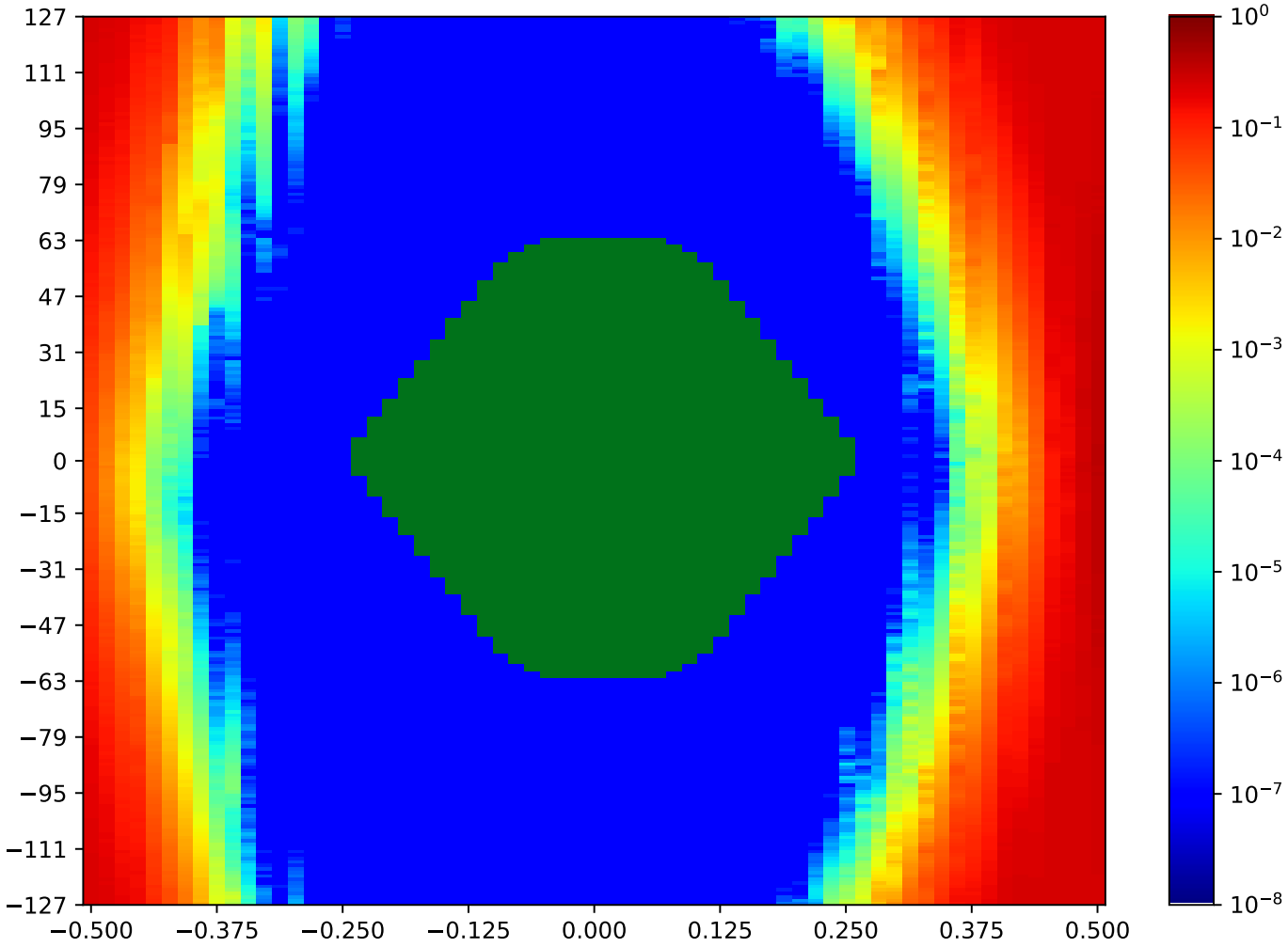


Figure 4.174: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.9 MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Table 4.162: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:27:40		2018-Sep-27 16:28:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9128	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

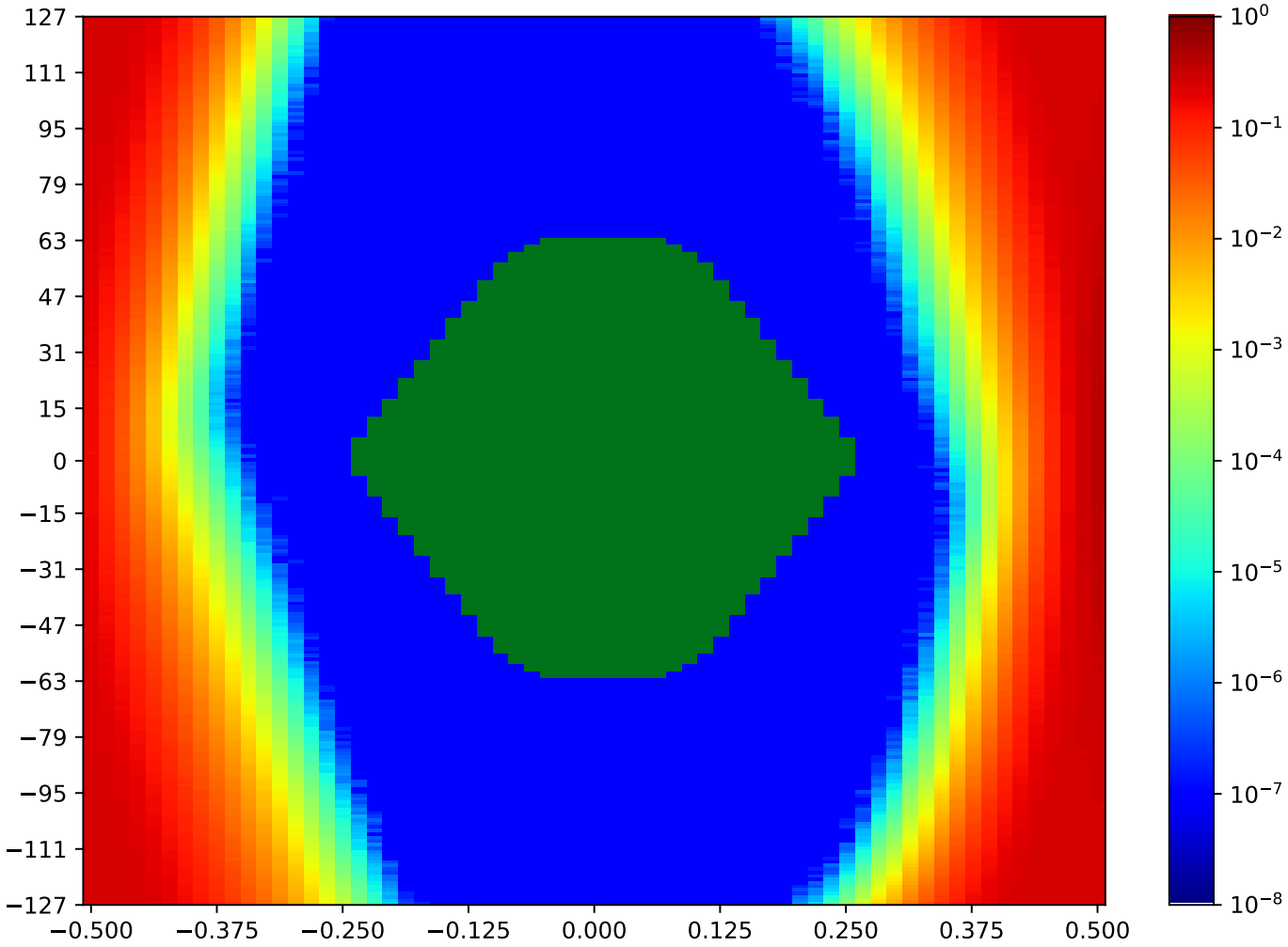


Figure 4.175: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.10 MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Table 4.163: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:25:58		2018-Sep-27 16:26:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8896	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

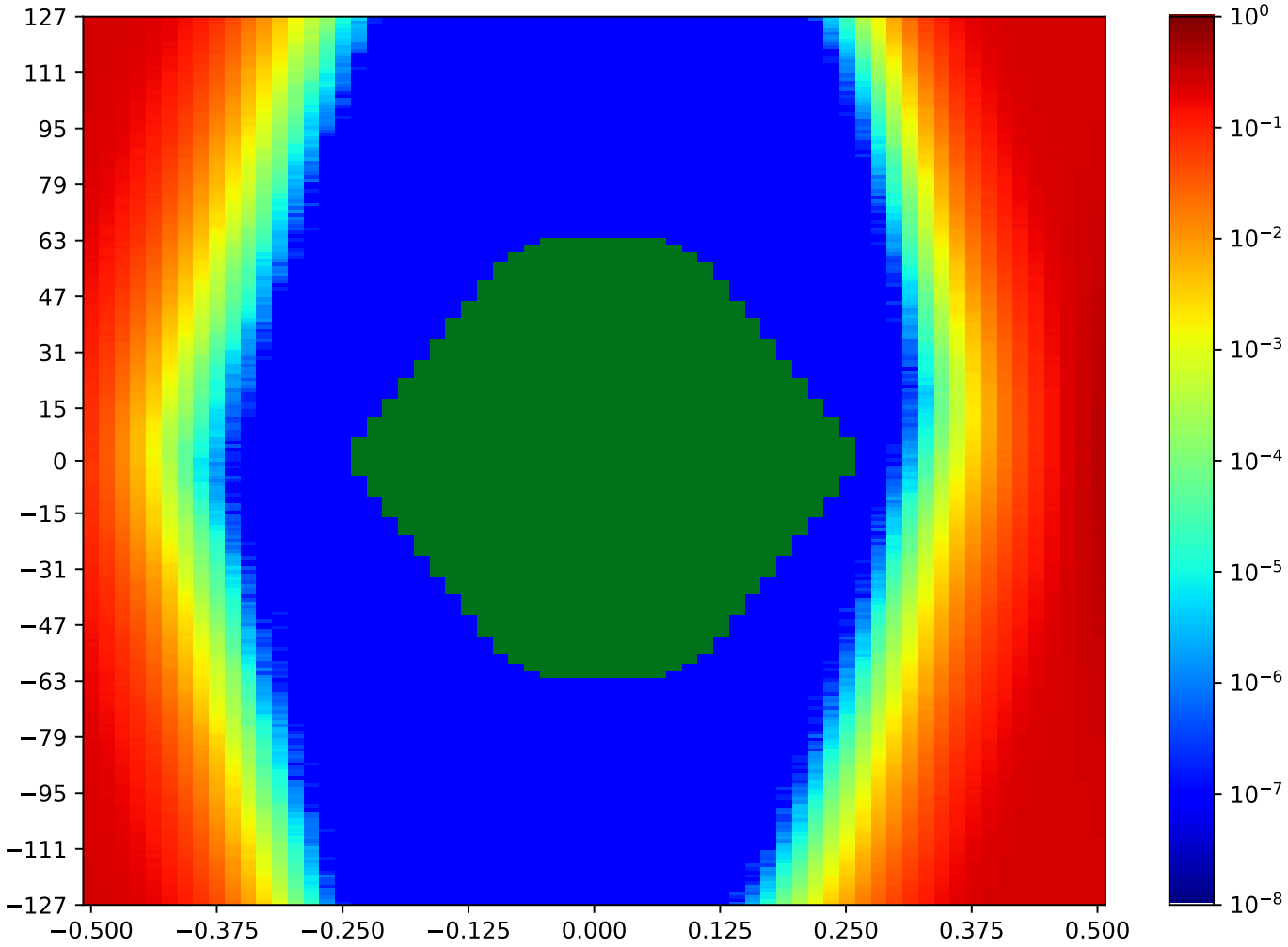


Figure 4.176: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.11 MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Table 4.164: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:27:00		2018-Sep-27 16:27:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8668	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

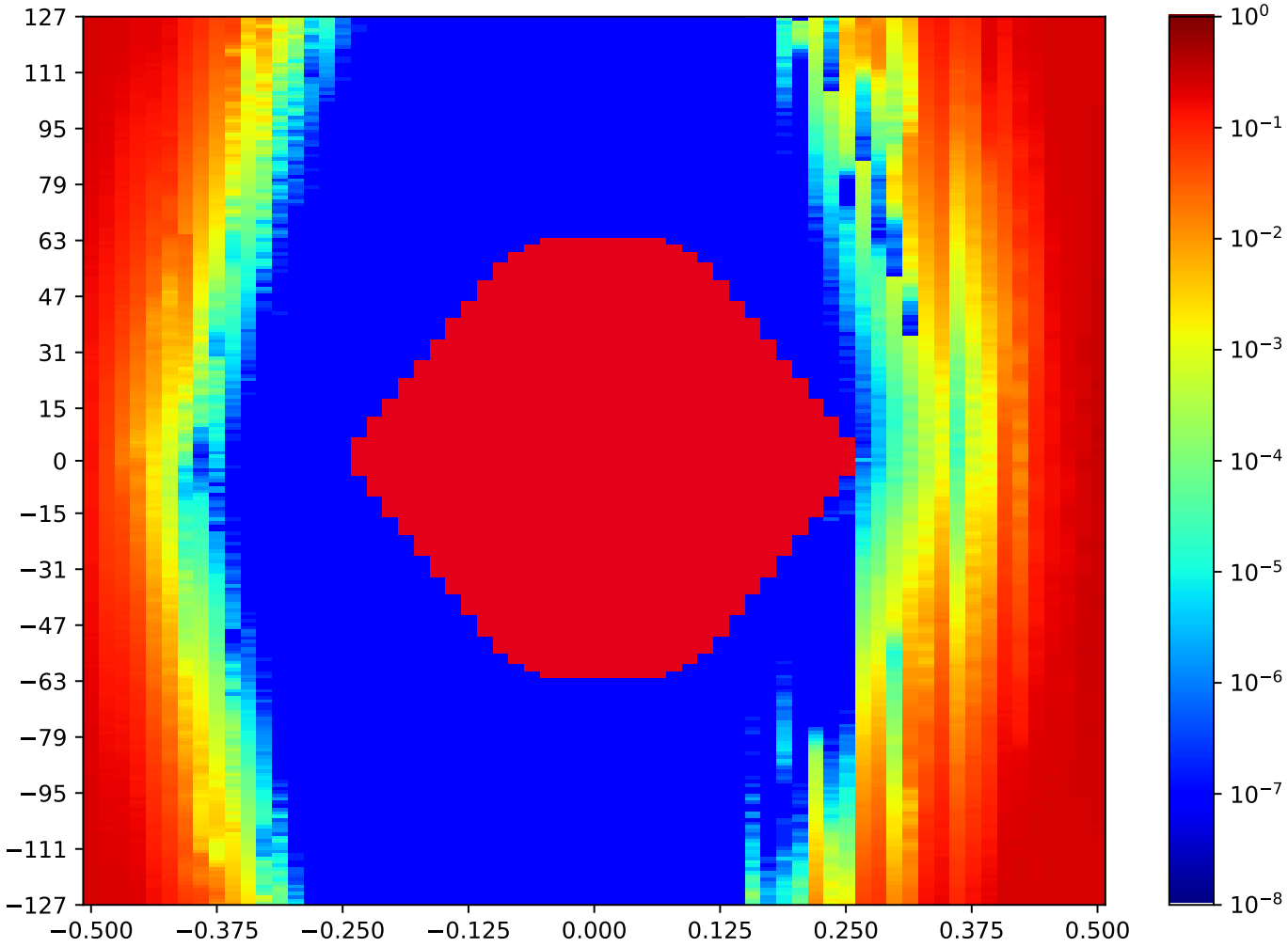


Figure 4.177: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.13.12 MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Table 4.165: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:26:39		2018-Sep-27 16:26:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9855	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

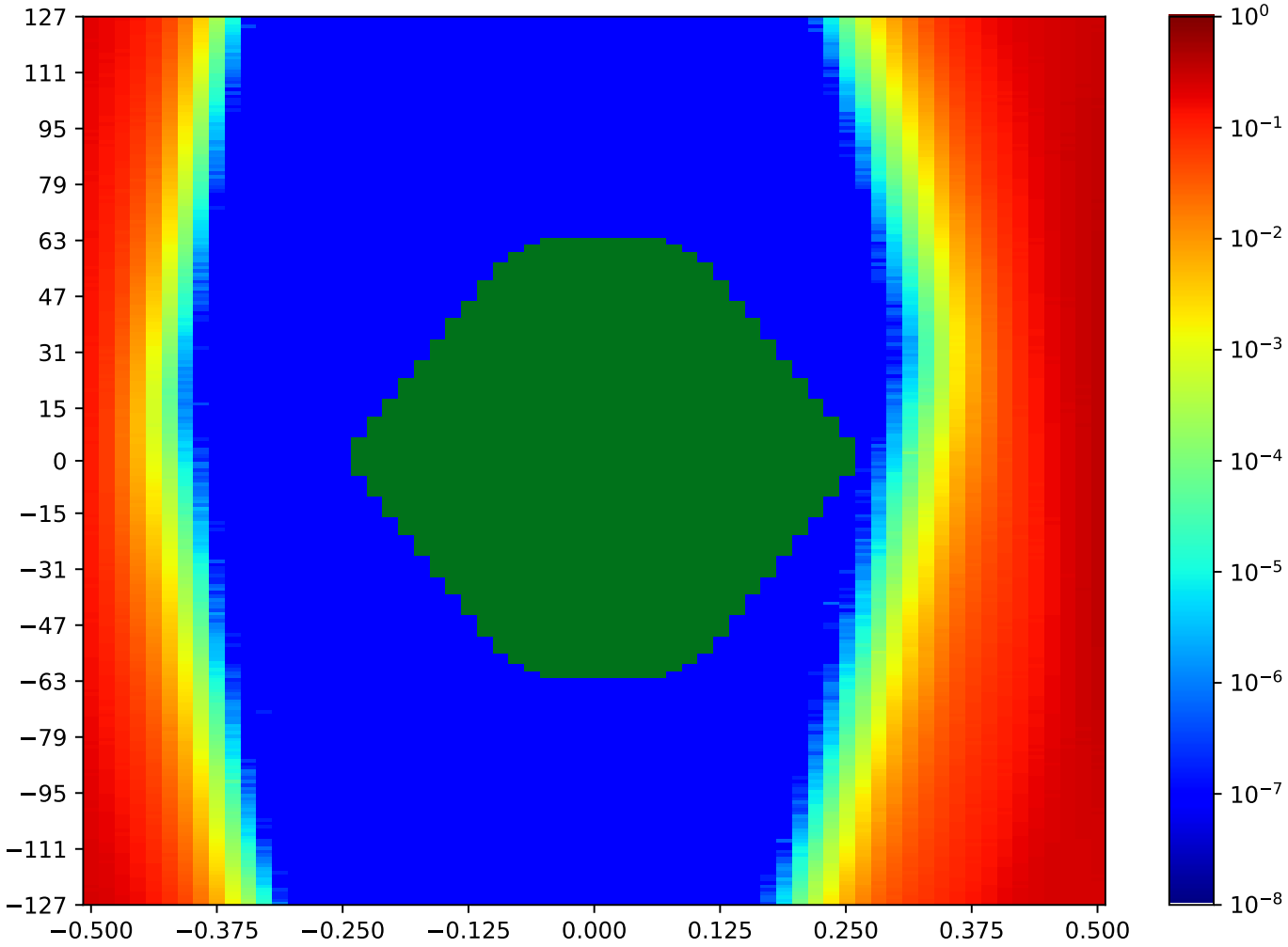


Figure 4.178: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.188.

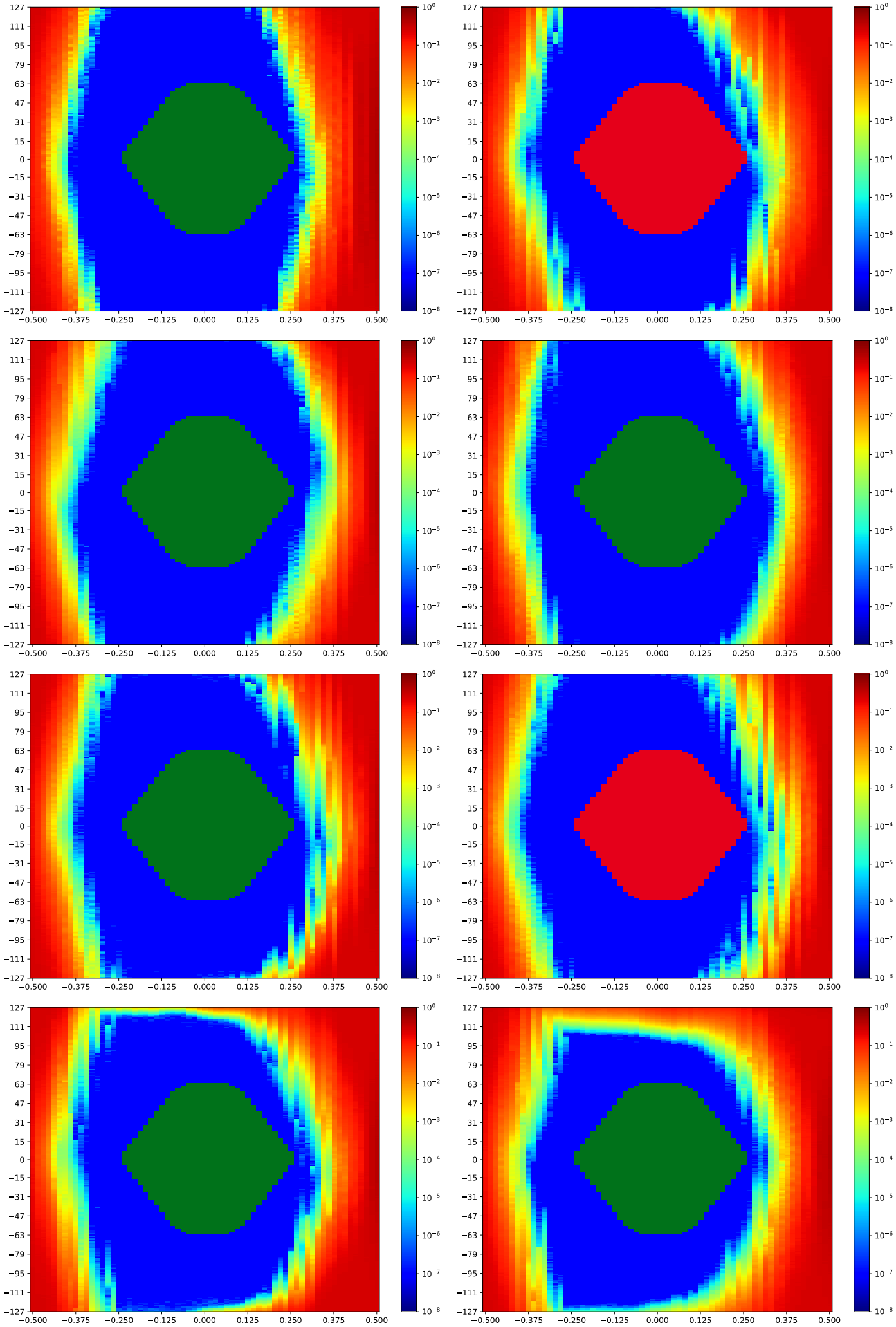


Figure 4.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback

4.14.1 TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Table 4.166: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:29:23		2018-Sep-27 16:29:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9168	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

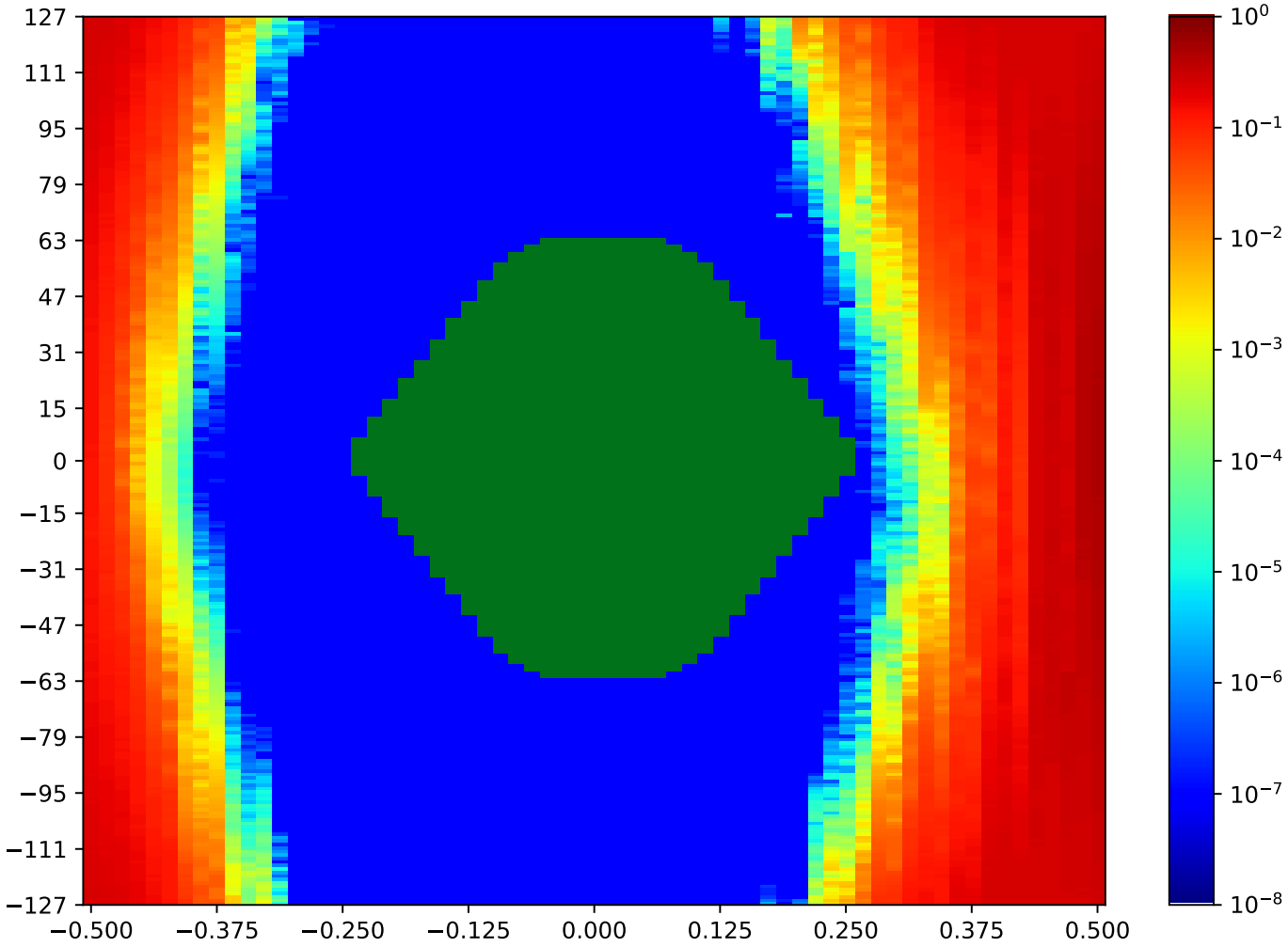


Figure 4.180: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.2 TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Table 4.167: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:28:43		2018-Sep-27 16:29:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8044	37	56.92%	255	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

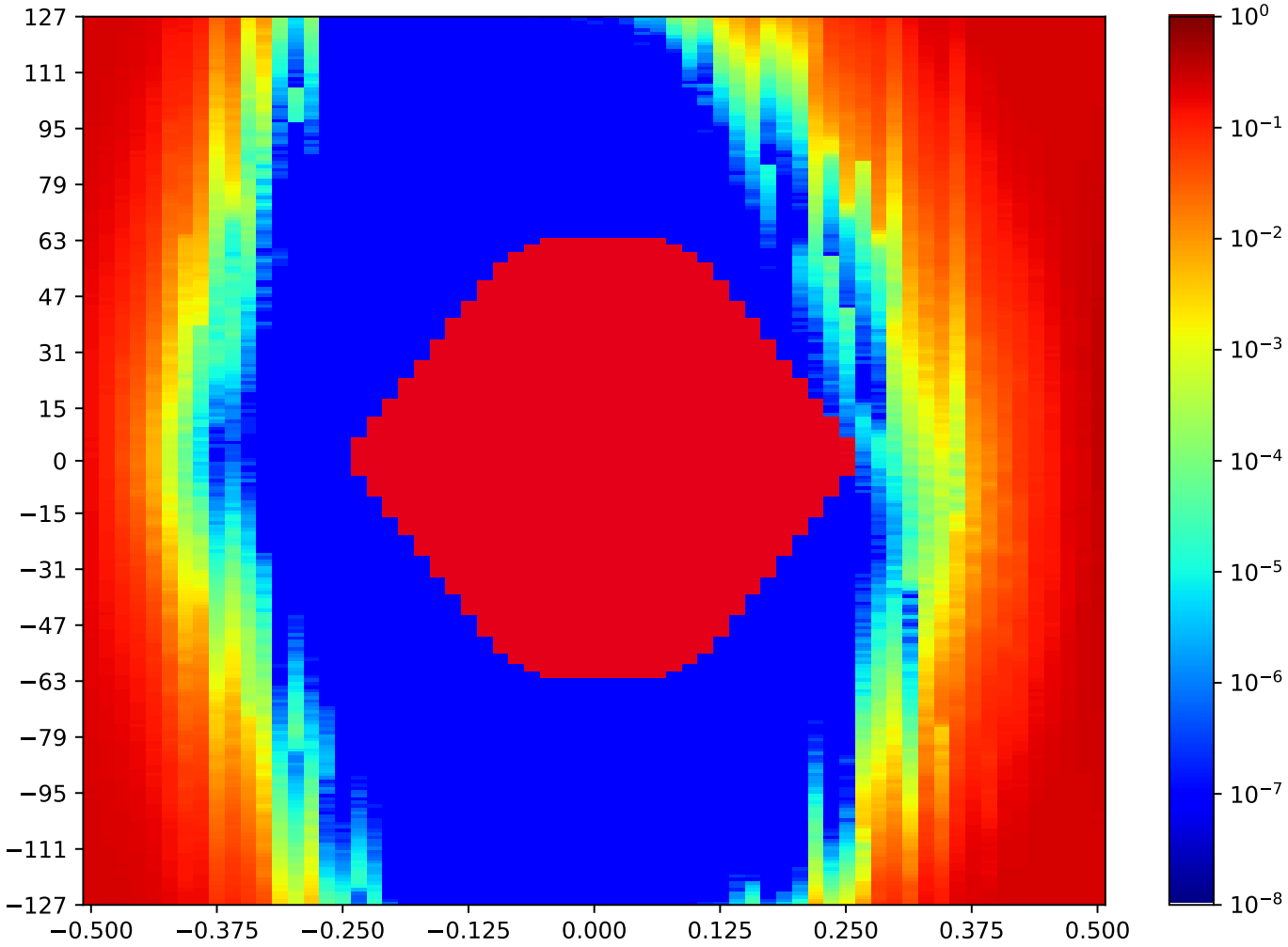


Figure 4.181: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.3 TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Table 4.168: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:30:04		2018-Sep-27 16:30:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8999	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

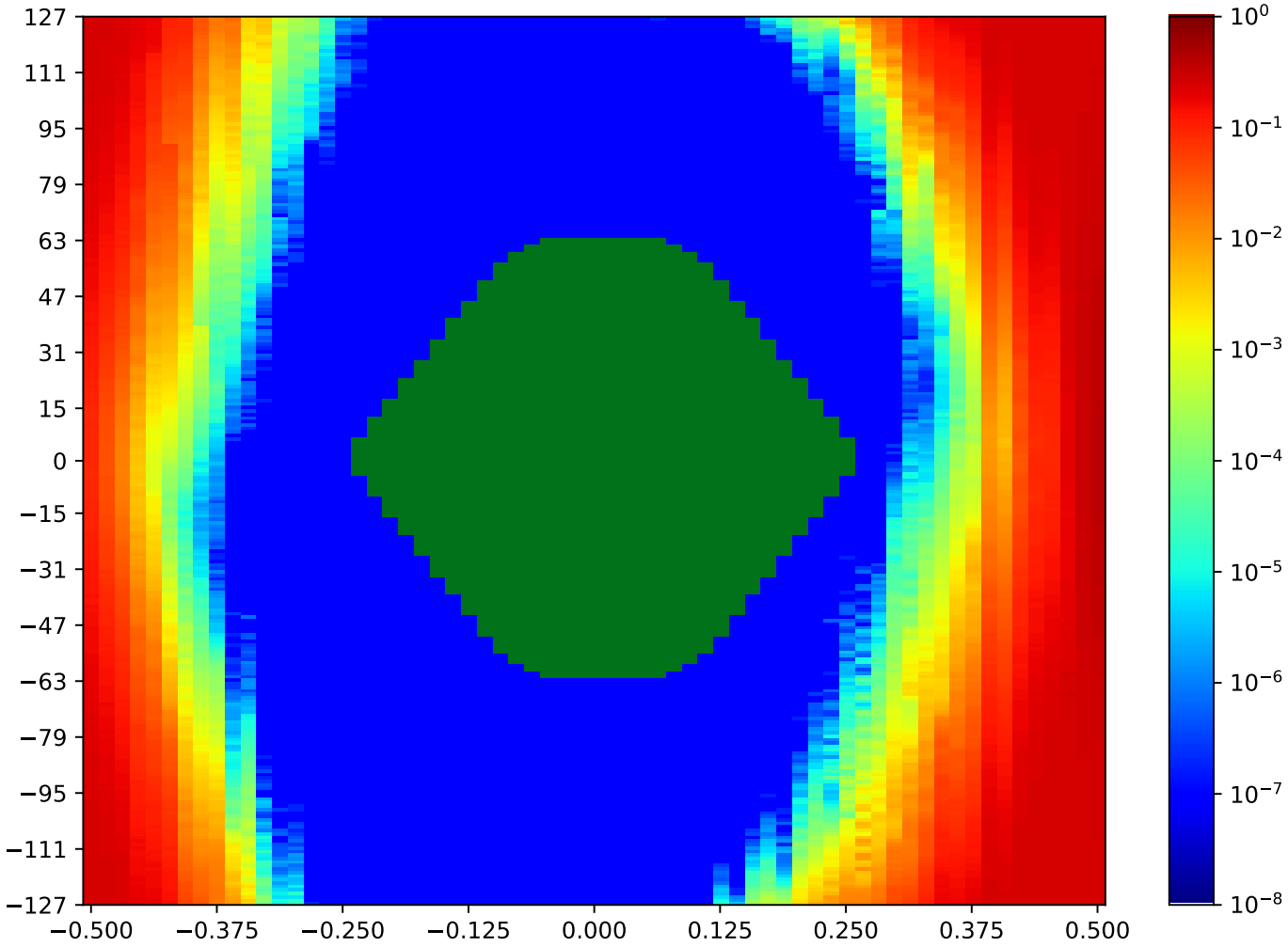


Figure 4.182: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.4 TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Table 4.169: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:29:03		2018-Sep-27 16:29:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9217	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

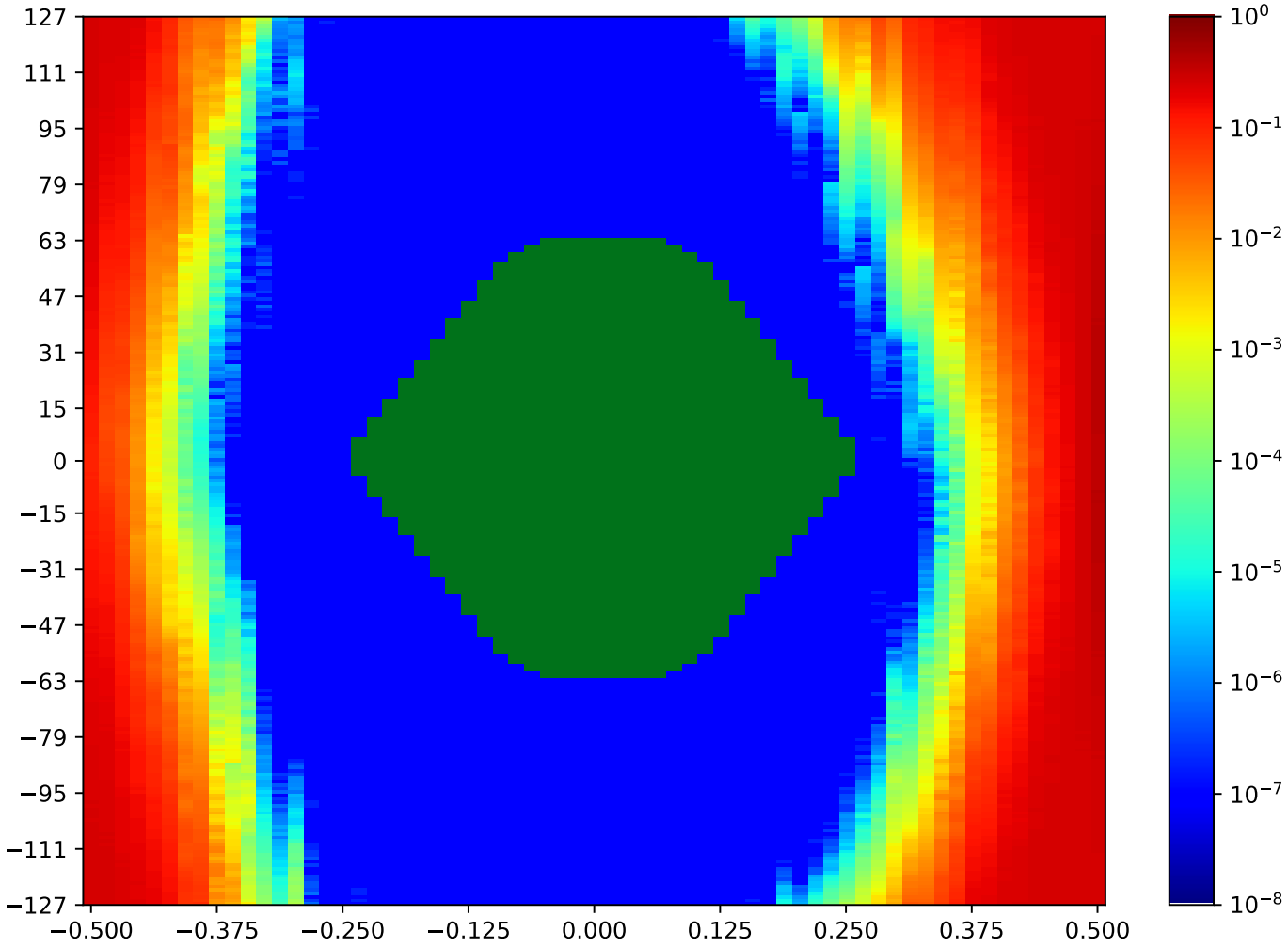


Figure 4.183: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.5 TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Table 4.170: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:30:45		2018-Sep-27 16:31:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8631	41	61.54%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

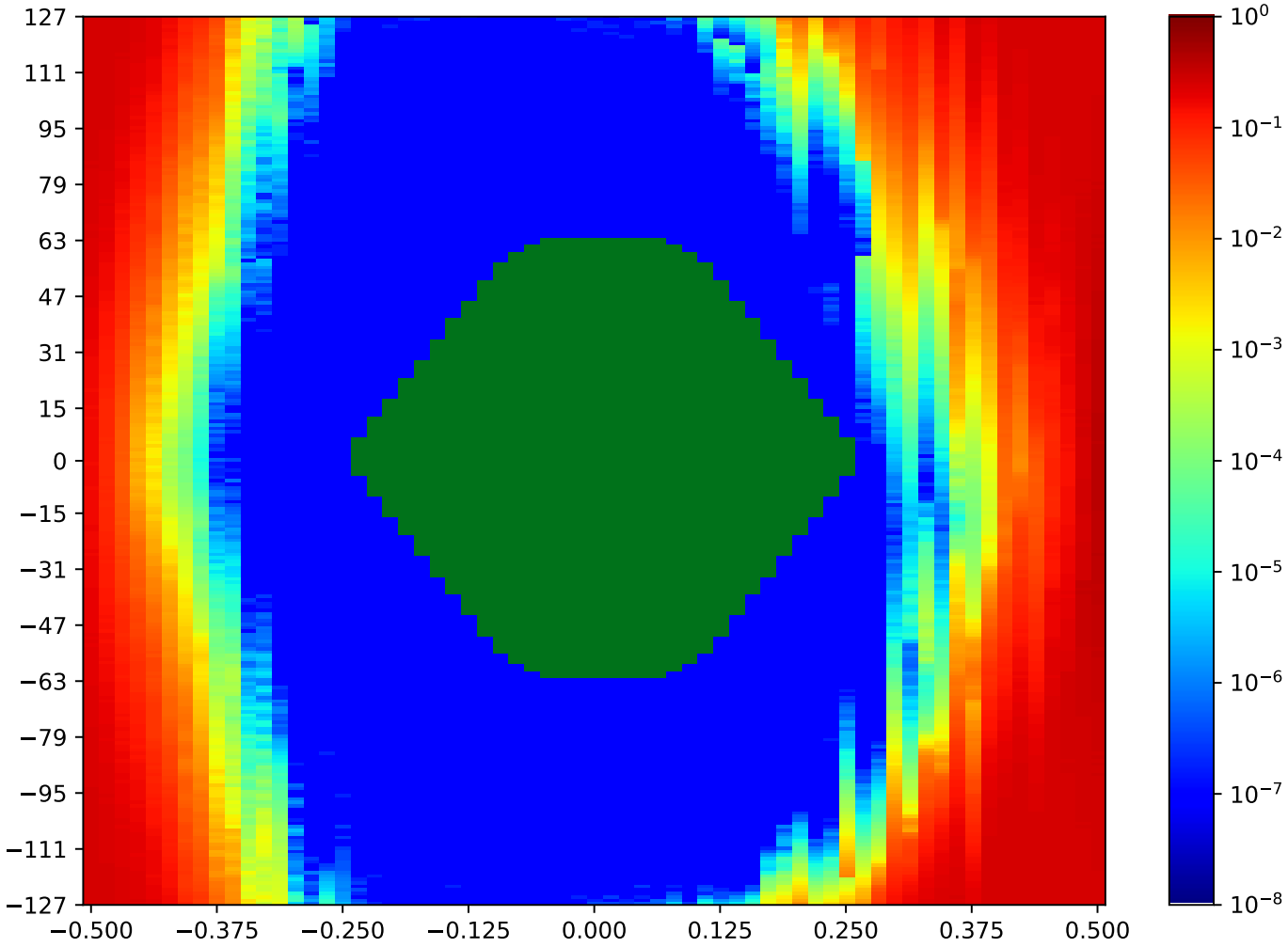


Figure 4.184: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.6 TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Table 4.171: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:28:22		2018-Sep-27 16:28:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8697	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

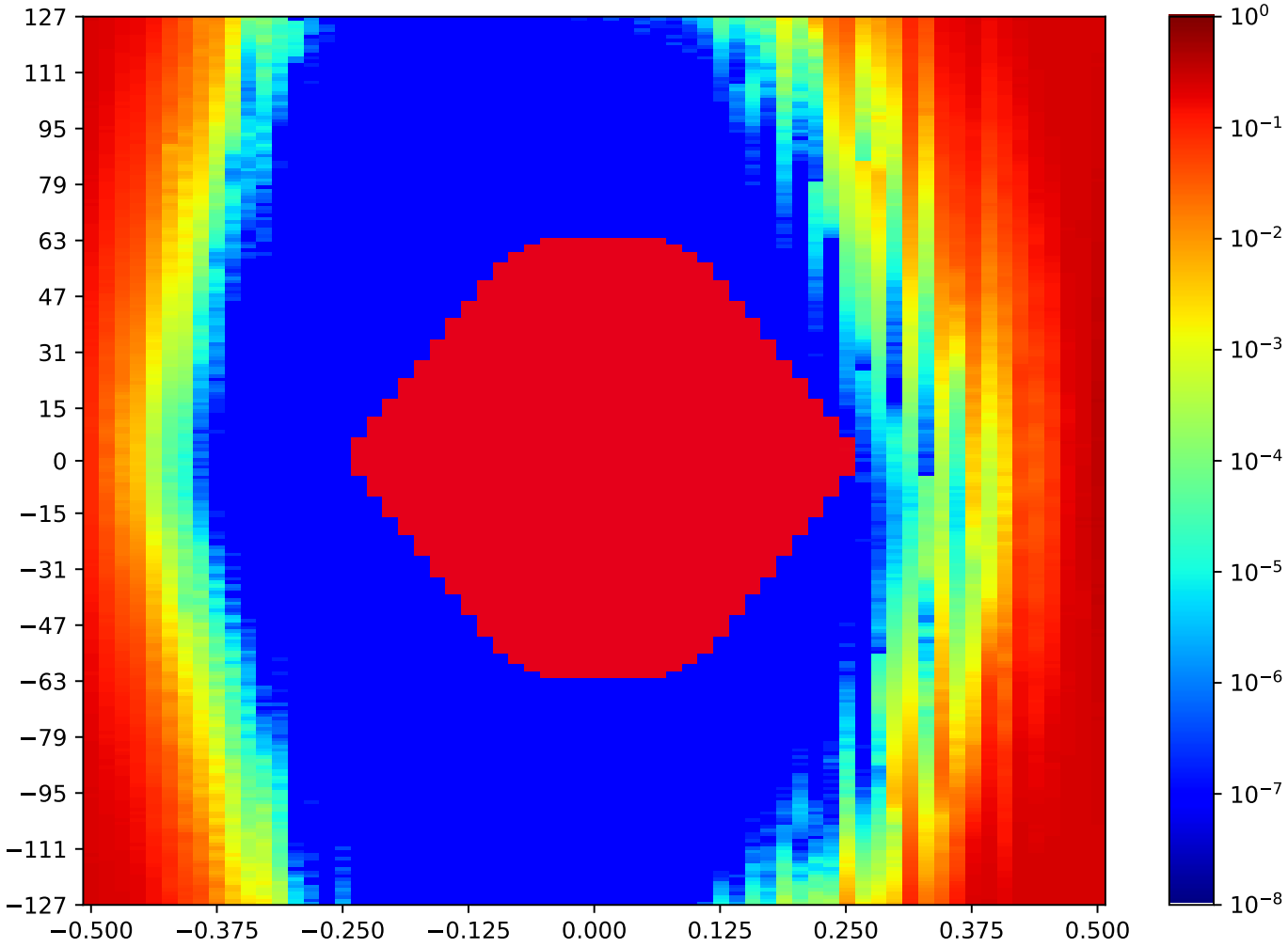


Figure 4.185: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.7 TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Table 4.172: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:29:44		2018-Sep-27 16:30:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7847	42	63.08%	229	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

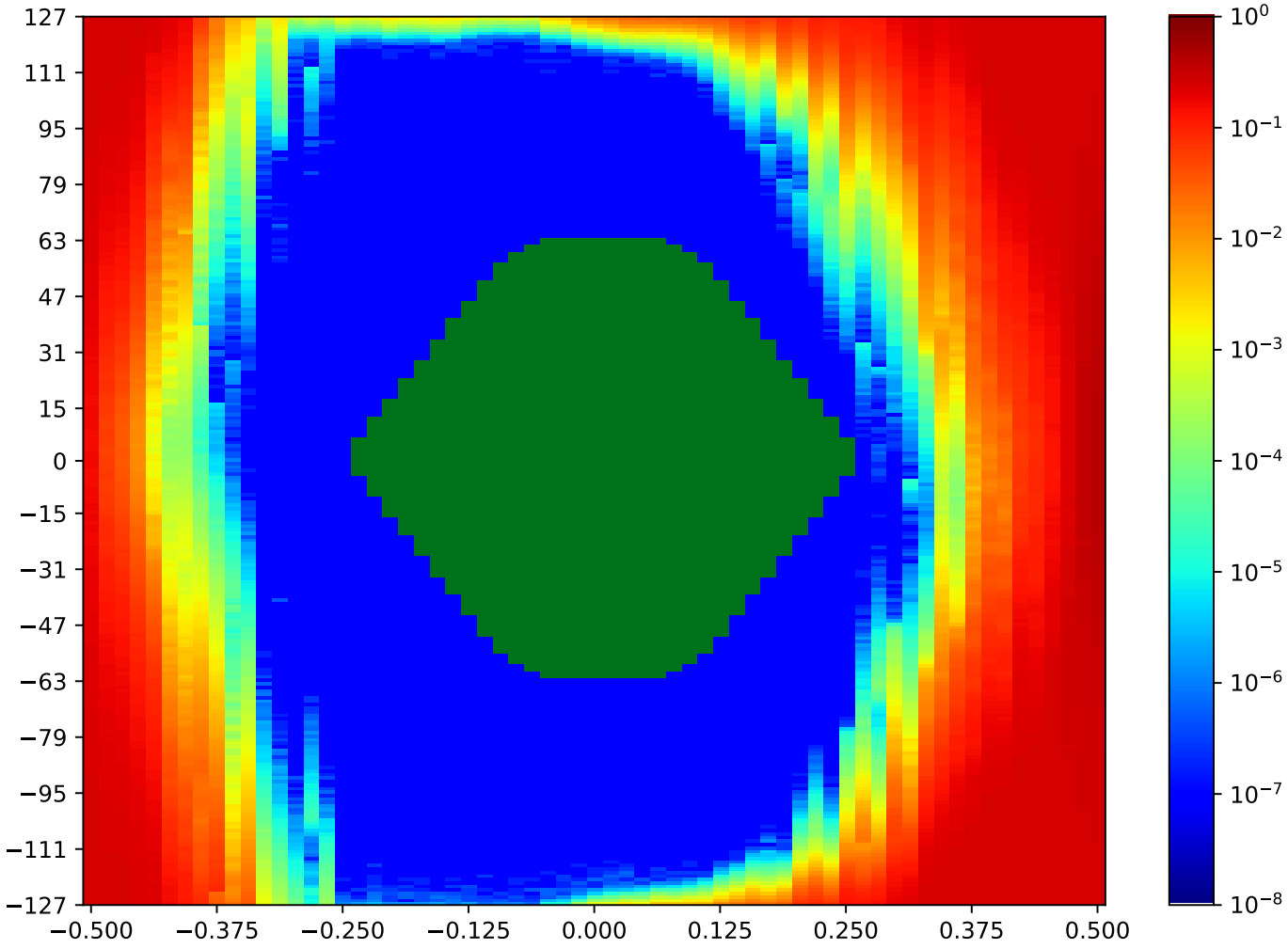


Figure 4.186: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.14.8 TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Table 4.173: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:30:25		2018-Sep-27 16:30:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7261	40	61.54%	215	84.31%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

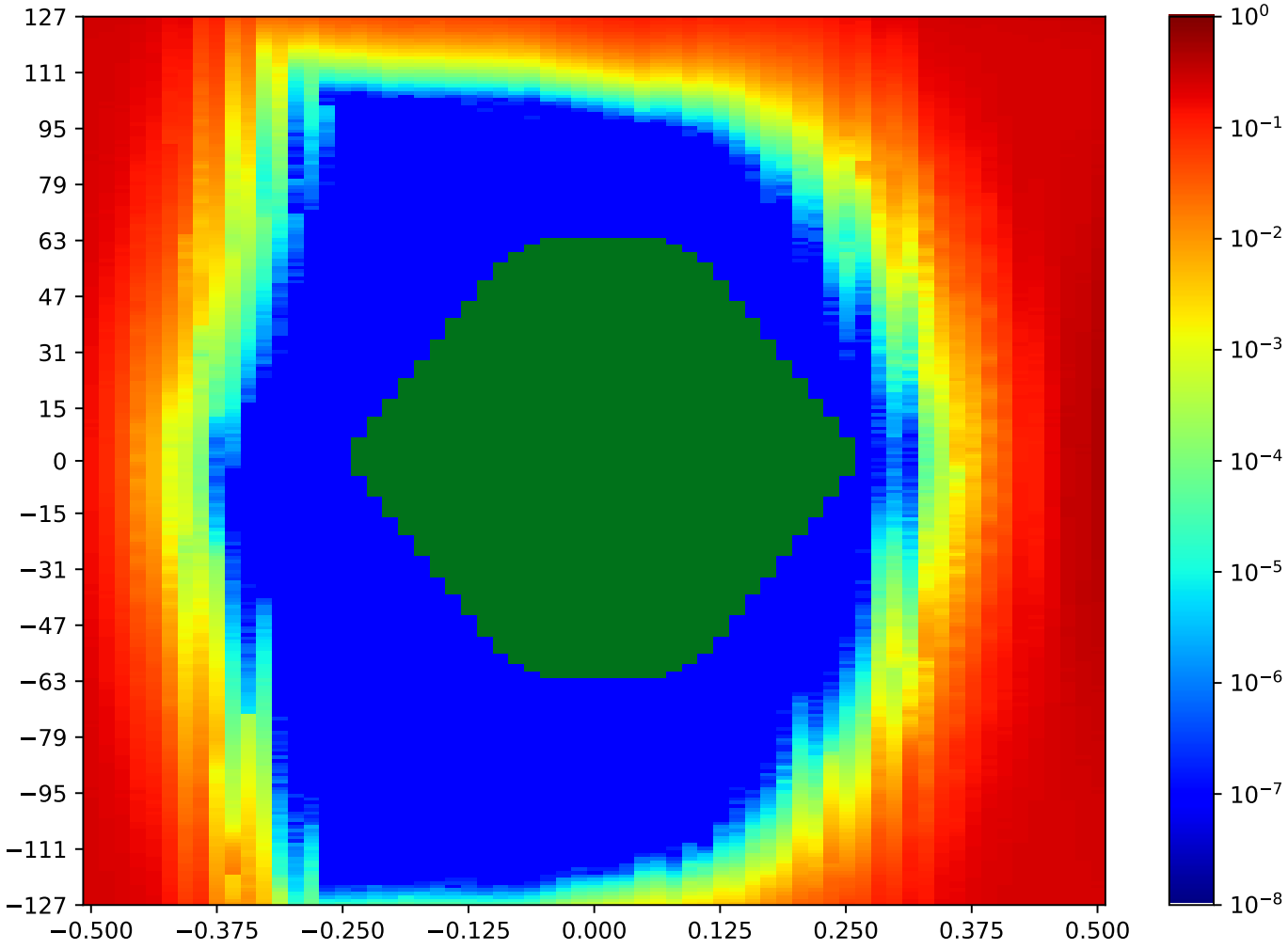


Figure 4.187: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15 MSP_A TX1 MSP_C RX10 Minipod Loopback

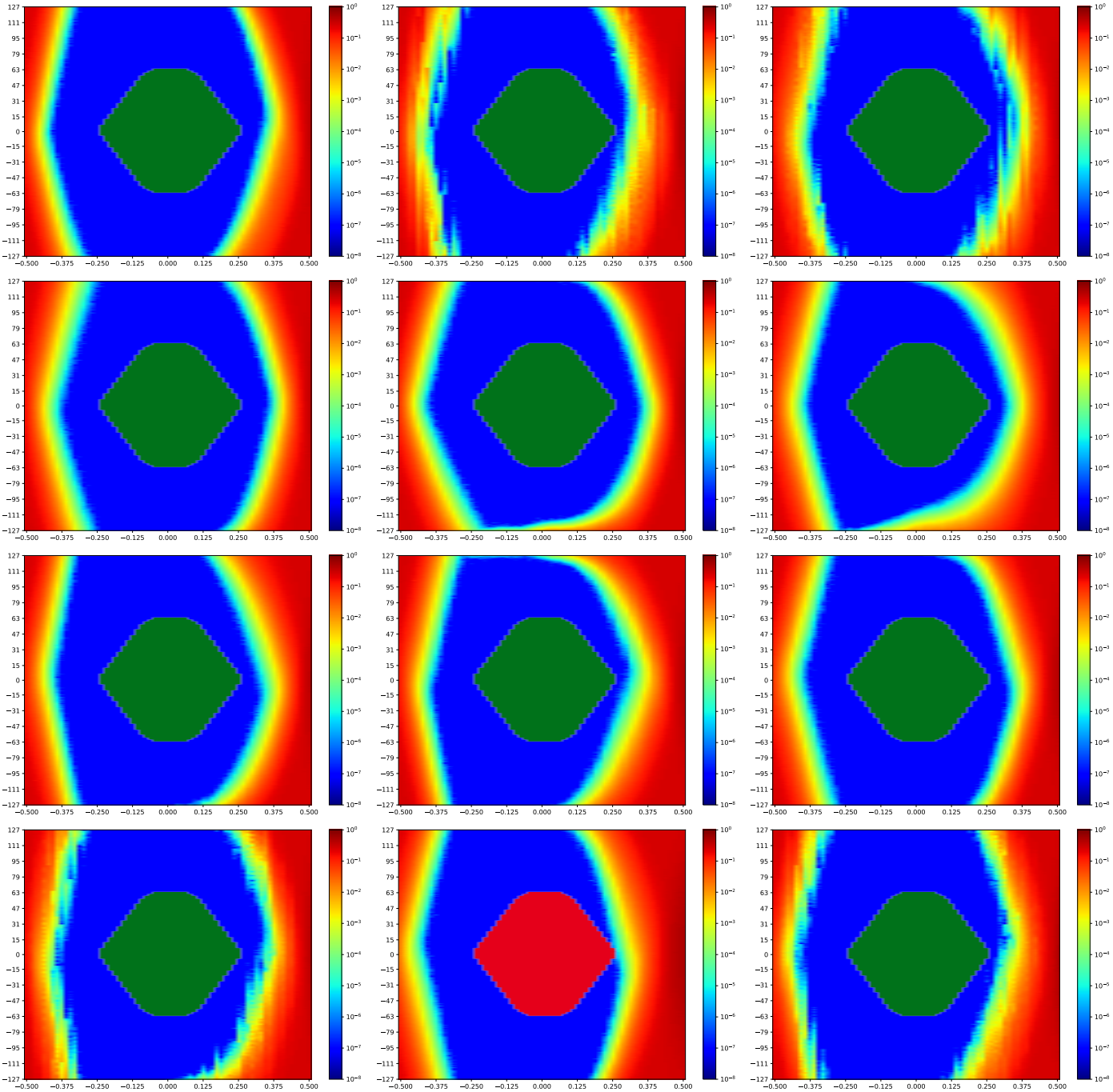


Figure 4.188: MSP_A TX1 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.201.

4.15.1 MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Table 4.174: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:44:03		2018-Sep-27 15:44:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9981	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

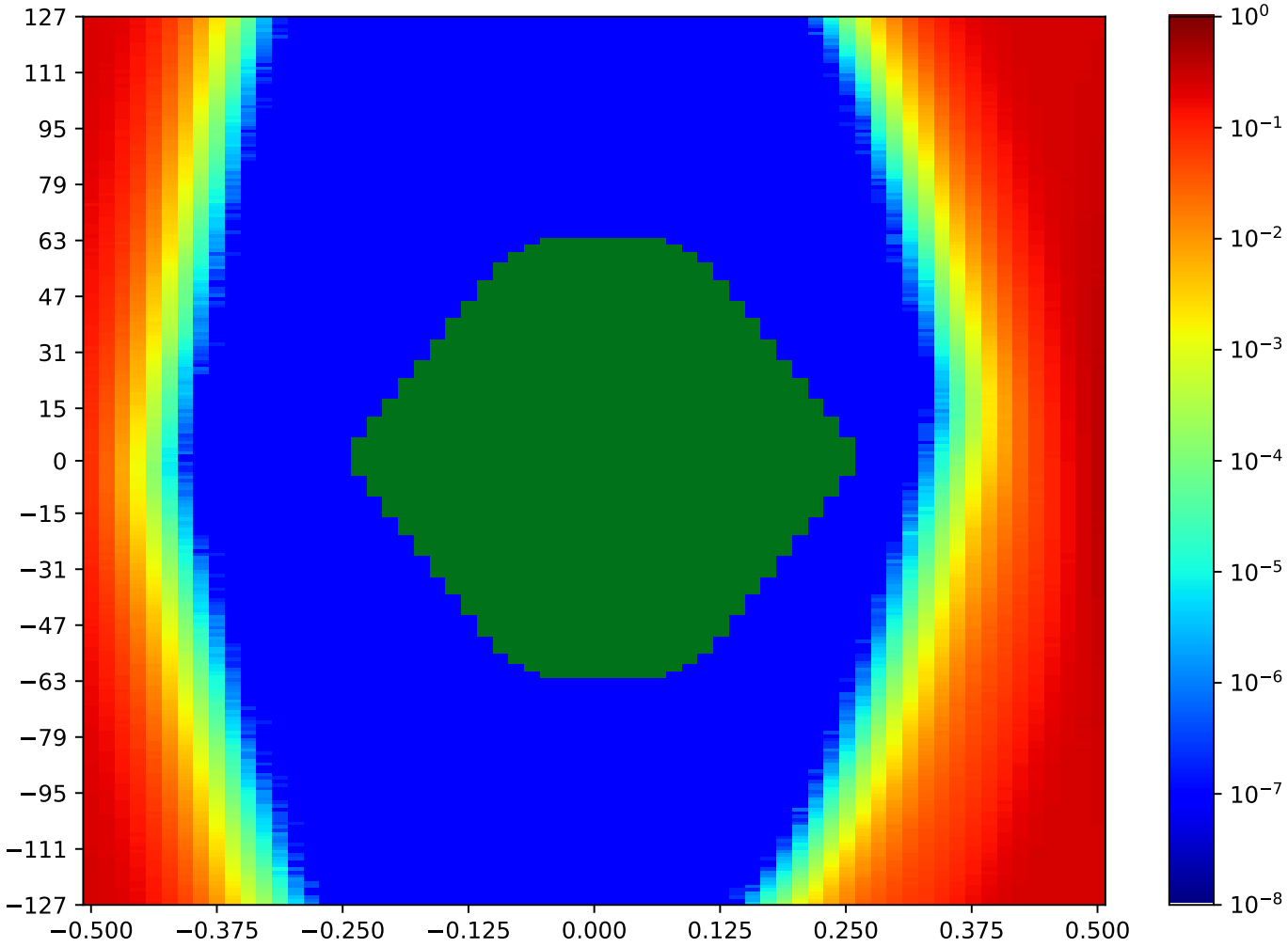


Figure 4.189: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.2 MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Table 4.175: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:44:44		2018-Sep-27 15:45:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8863	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

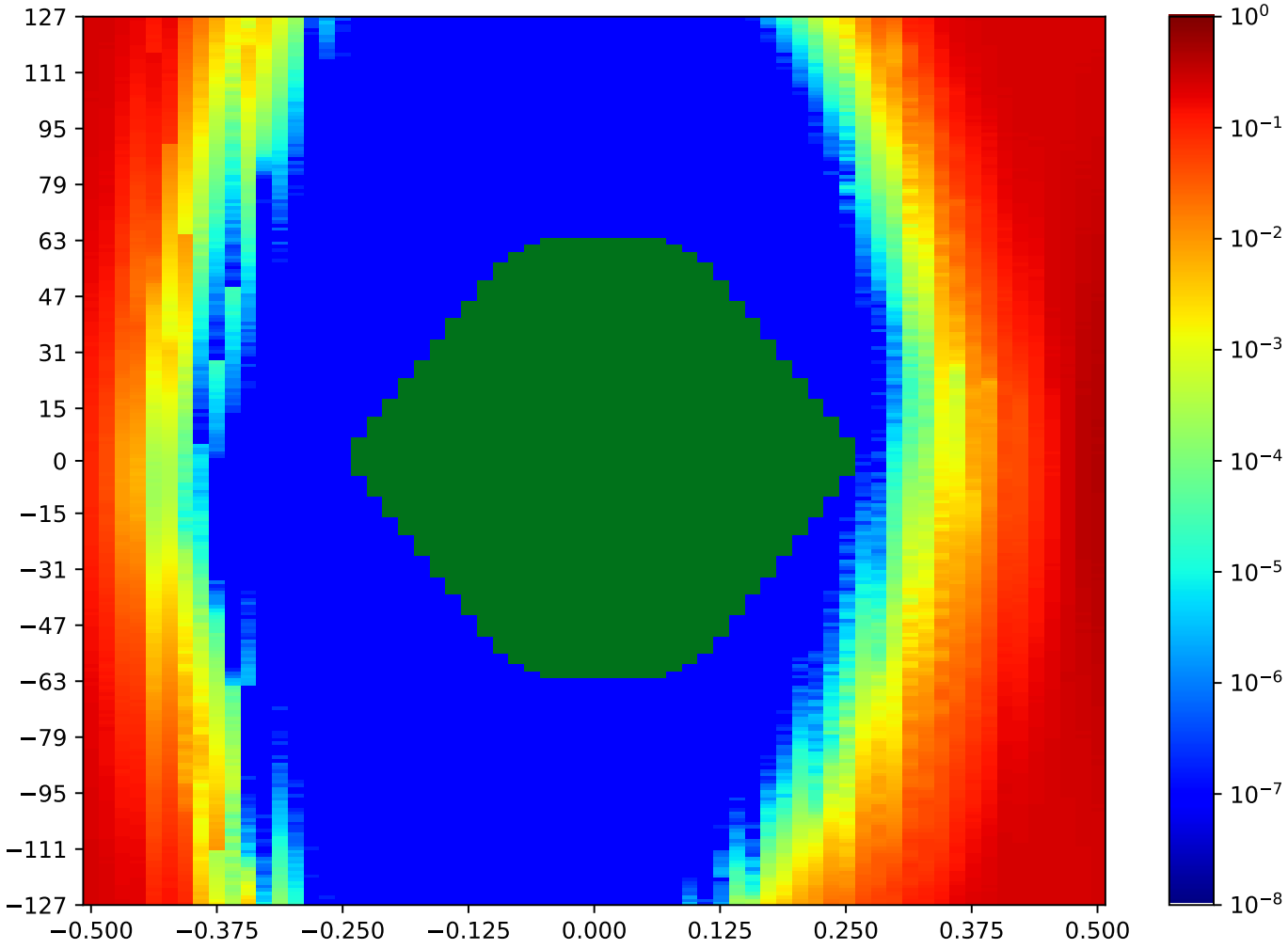


Figure 4.190: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.3 MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Table 4.176: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:45:04		2018-Sep-27 15:45:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8913	43	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

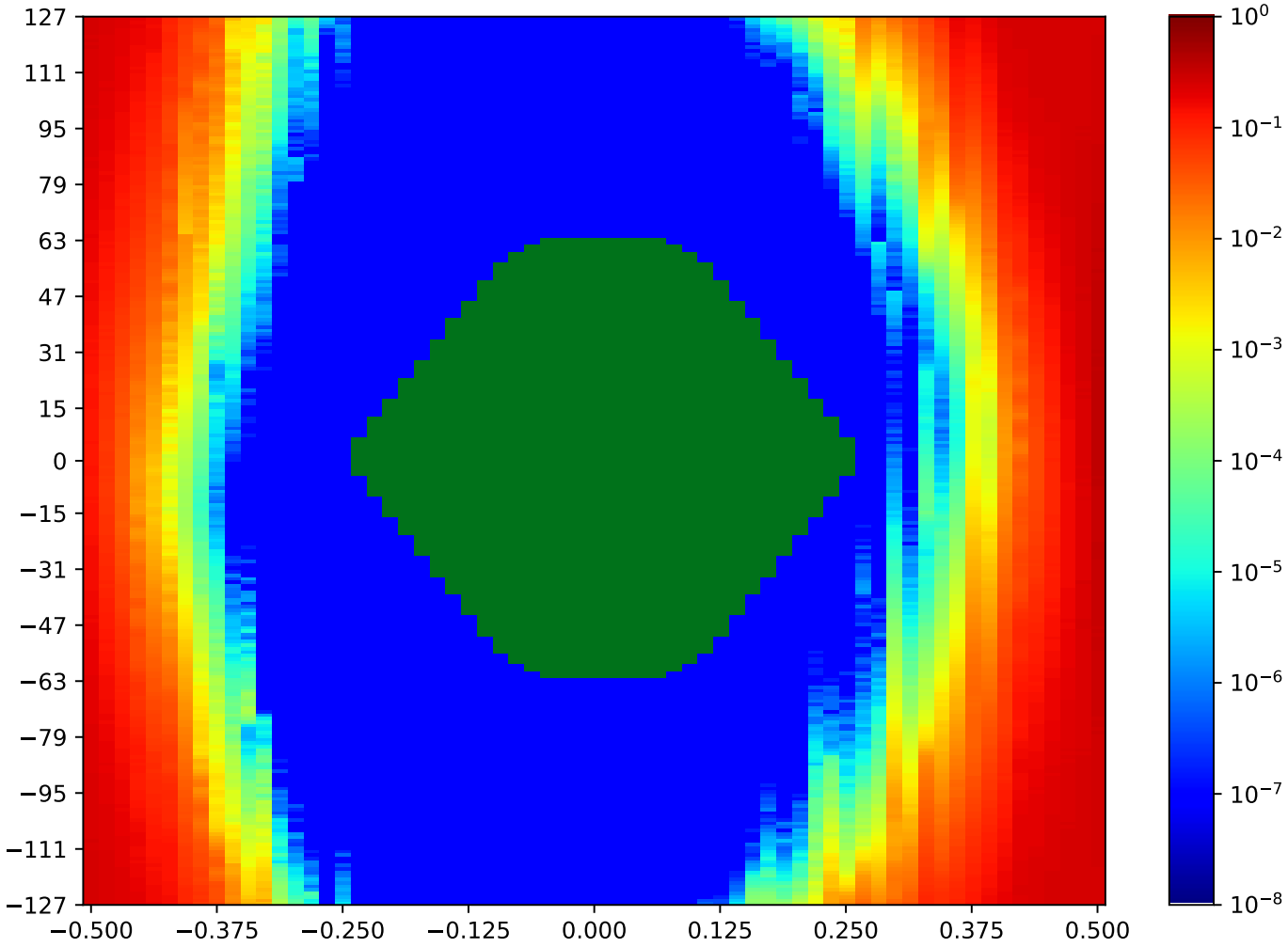


Figure 4.191: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.4 MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Table 4.177: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:43:23		2018-Sep-27 15:43:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9420	46	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

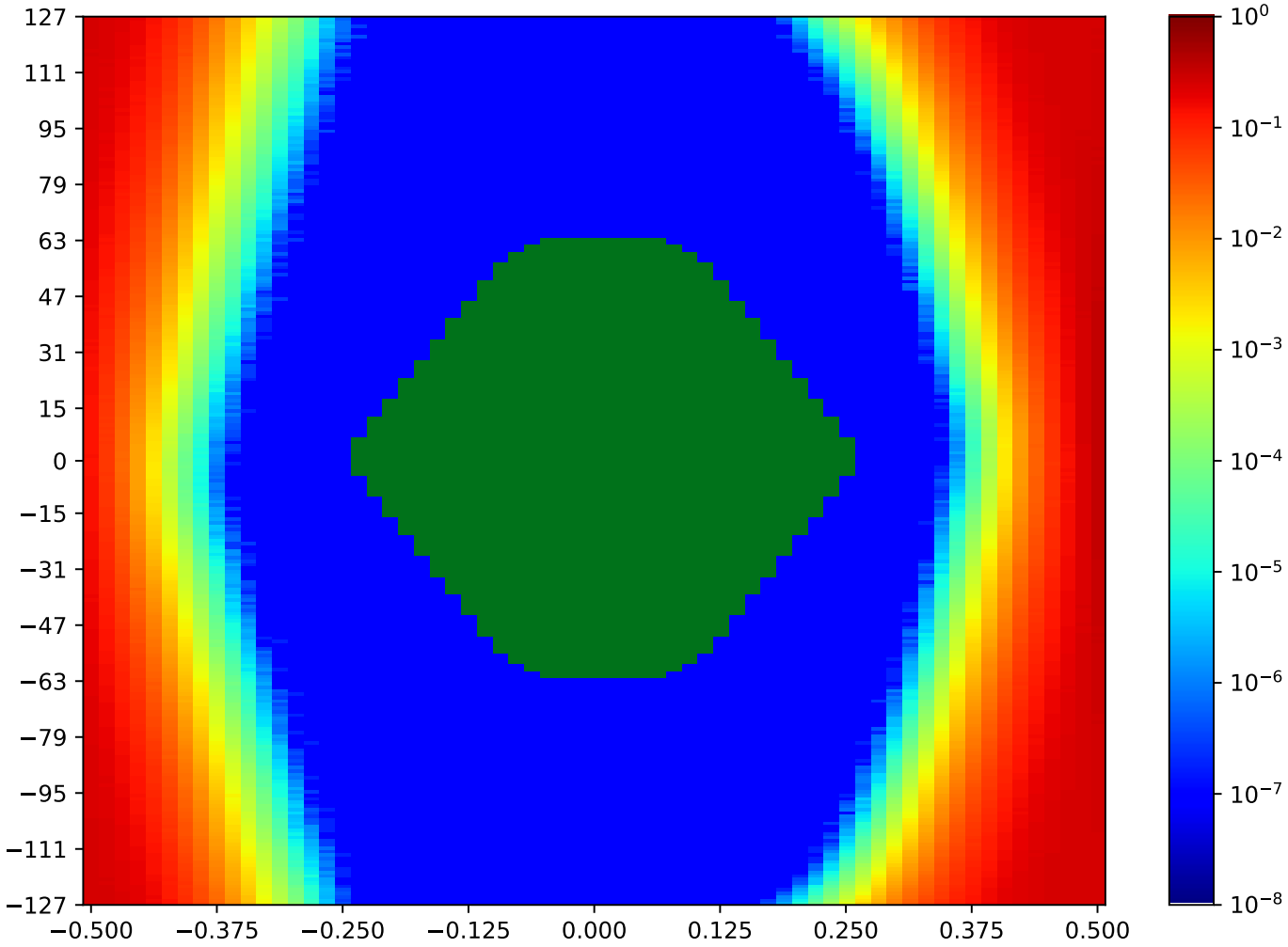


Figure 4.192: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.5 MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Table 4.178: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:46:10		2018-Sep-27 15:46:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8789	46	70.77%	242	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

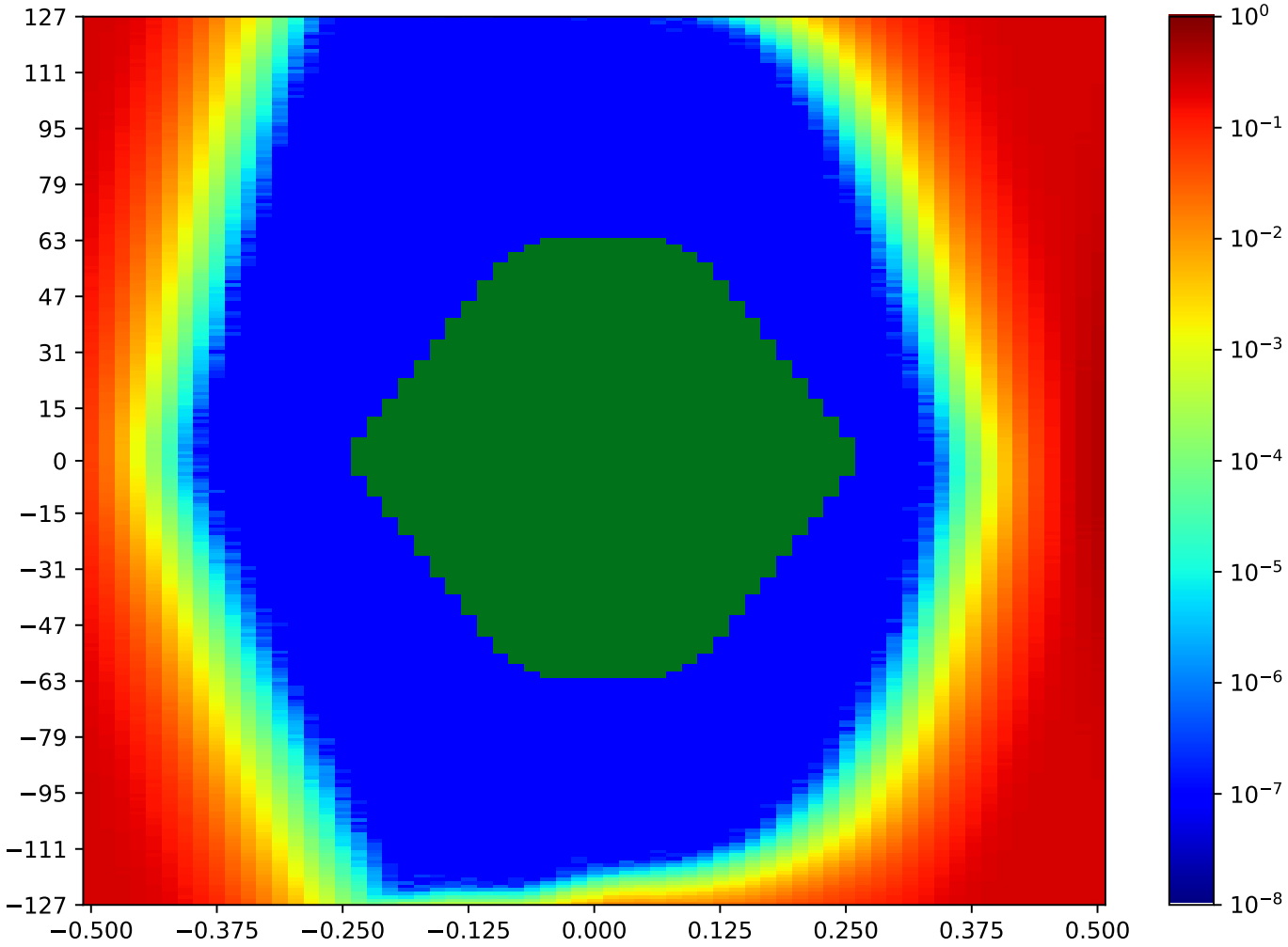


Figure 4.193: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.6 MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Table 4.179: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:43:03		2018-Sep-27 15:43:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7893	43	66.15%	223	87.45%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

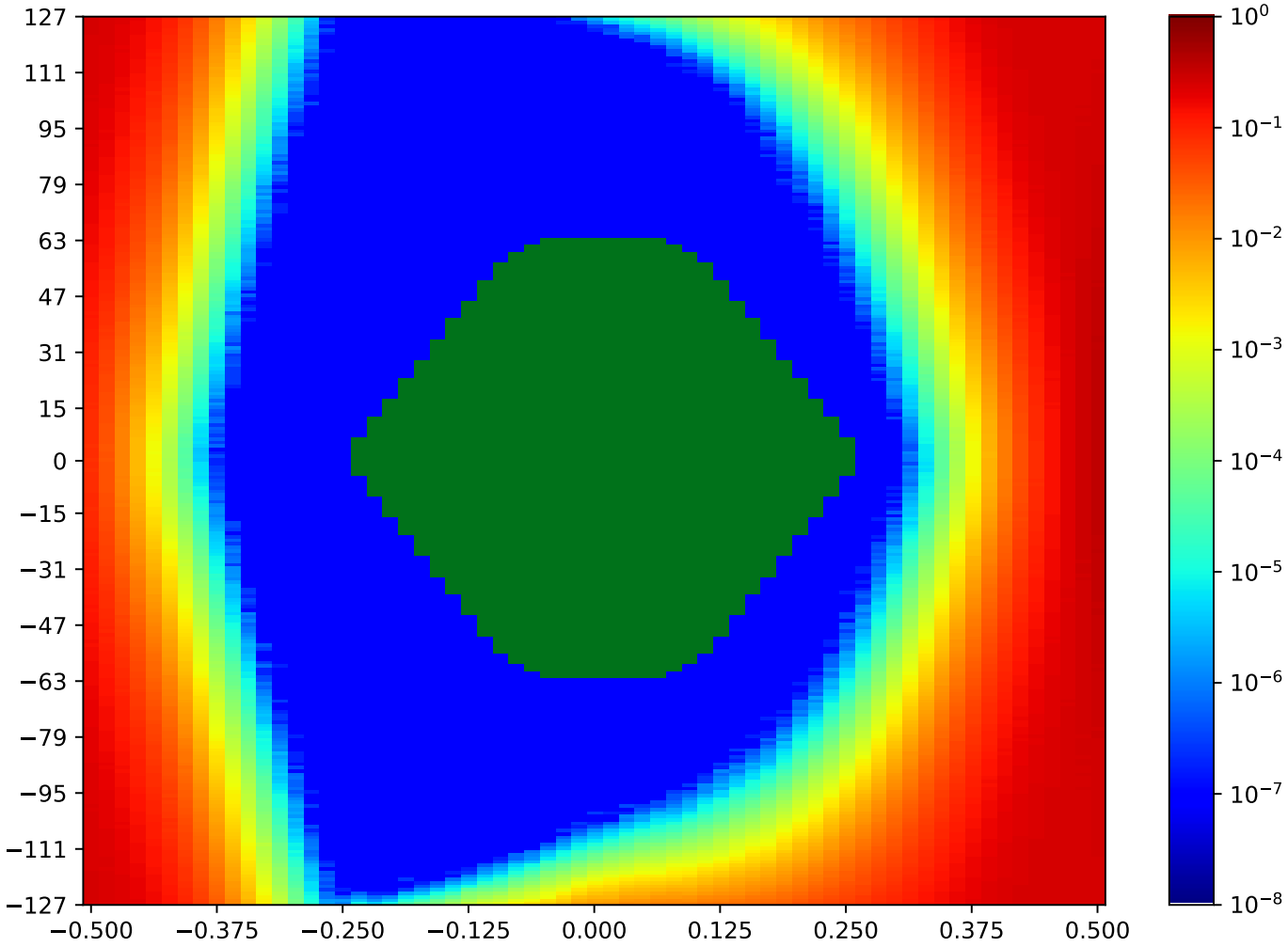


Figure 4.194: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.7 MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Table 4.180: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:46:56		2018-Sep-27 15:47:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9290	43	66.15%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

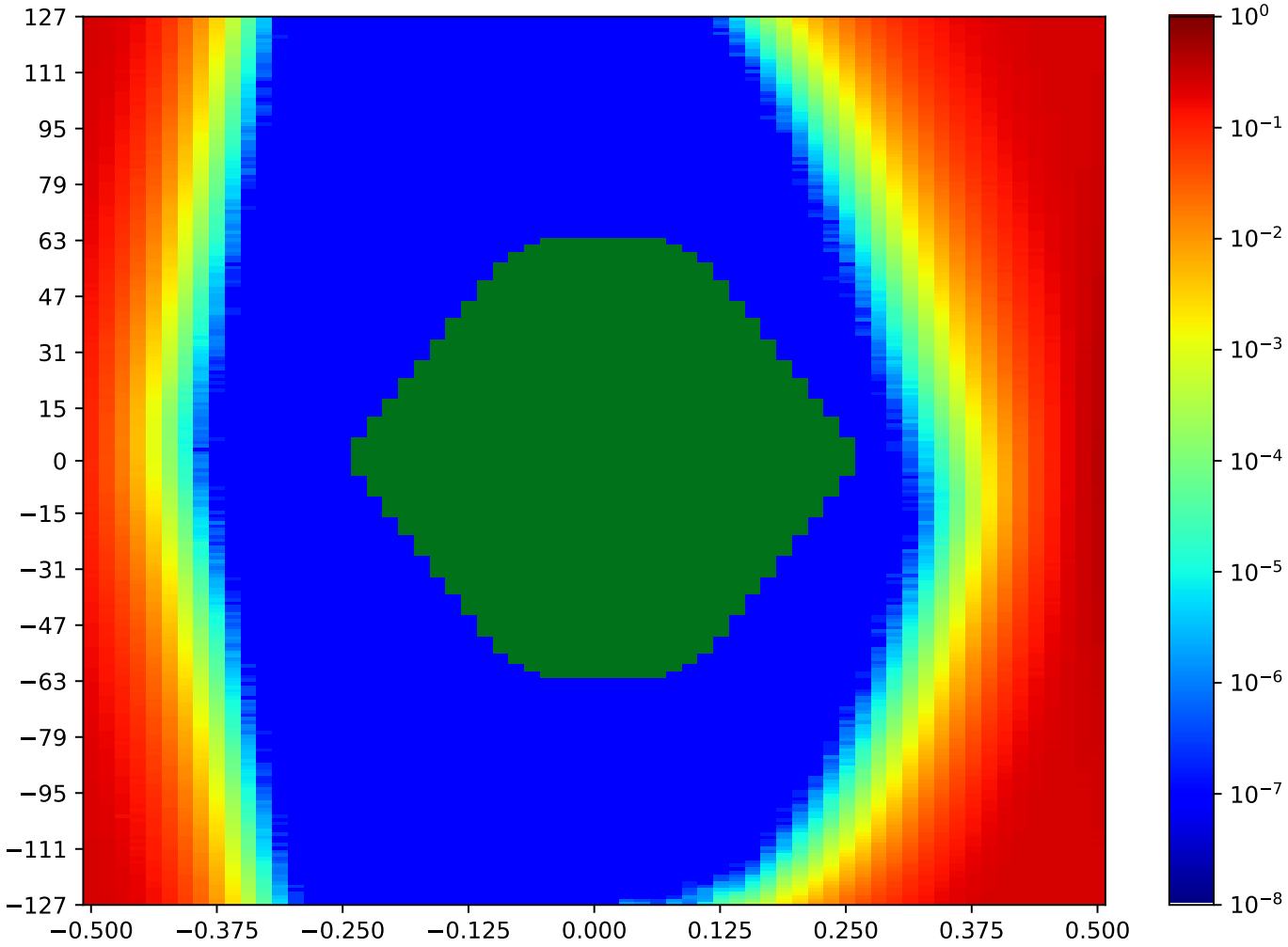


Figure 4.195: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.8 MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Table 4.181: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:43:43		2018-Sep-27 15:44:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8418	40	61.54%	248	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

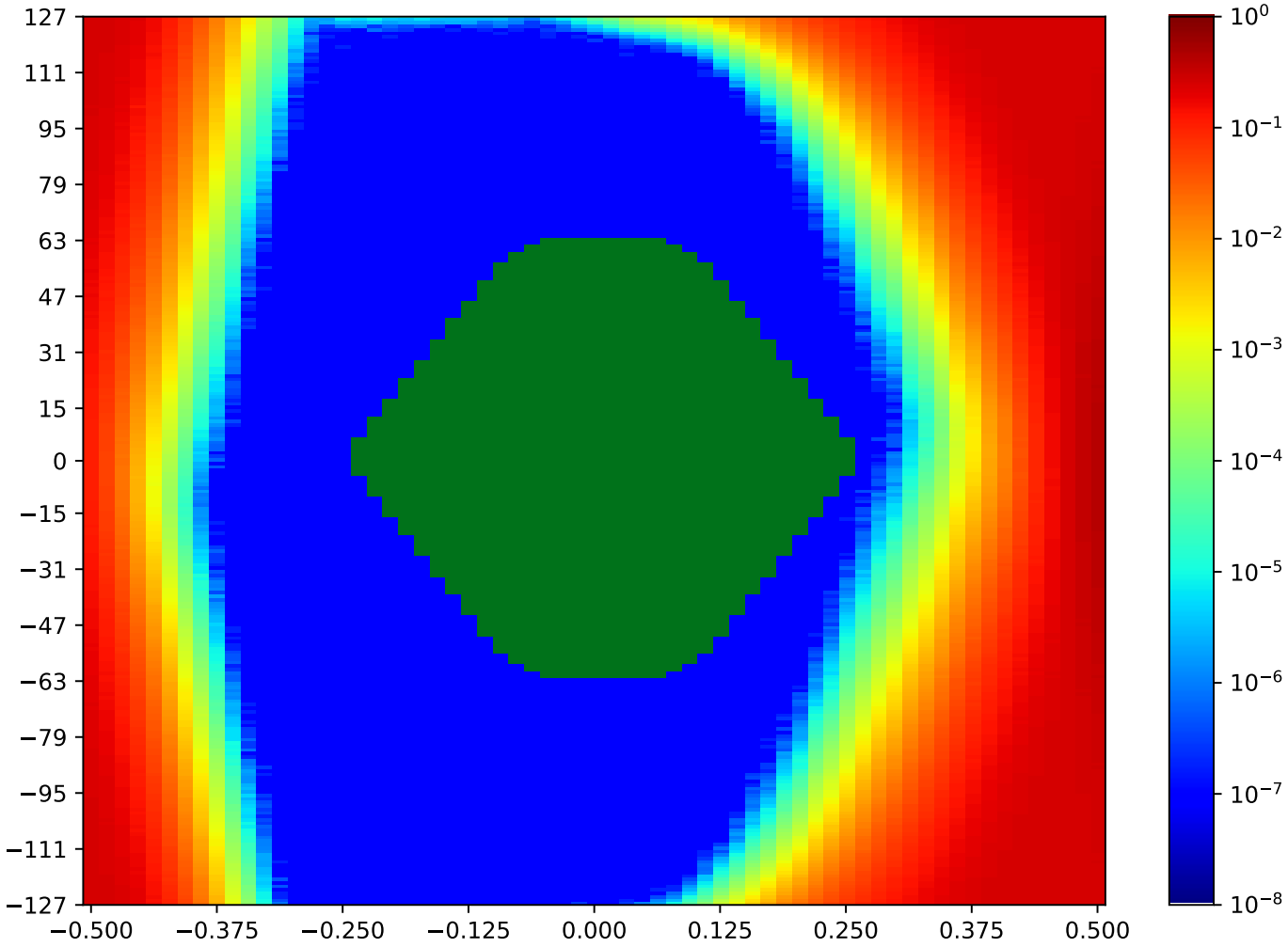


Figure 4.196: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.9 MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Table 4.182: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:46:30		2018-Sep-27 15:46:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9223	43	66.15%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

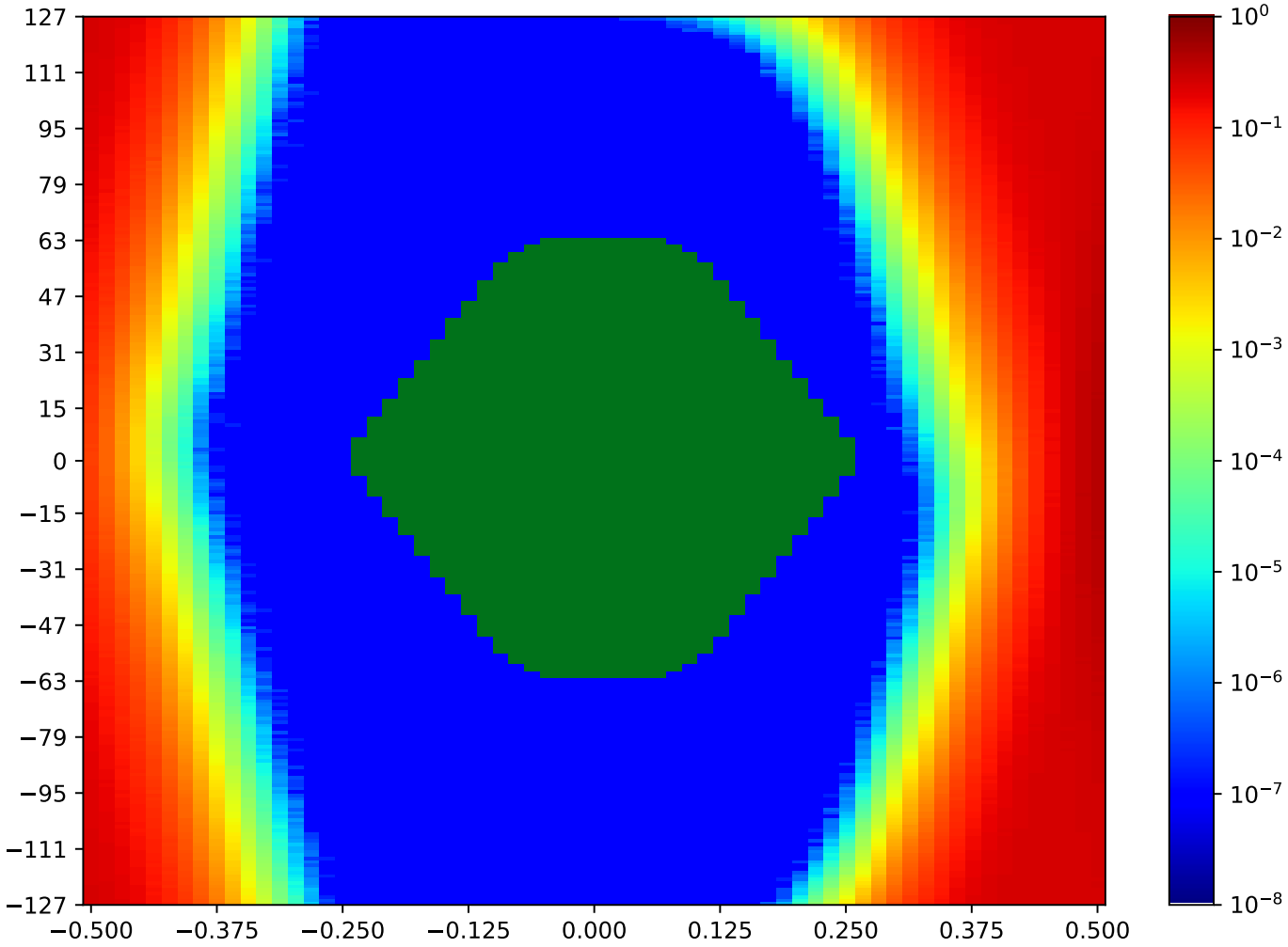


Figure 4.197: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.10 MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Table 4.183: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:44:23		2018-Sep-27 15:44:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9412	43	66.15%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

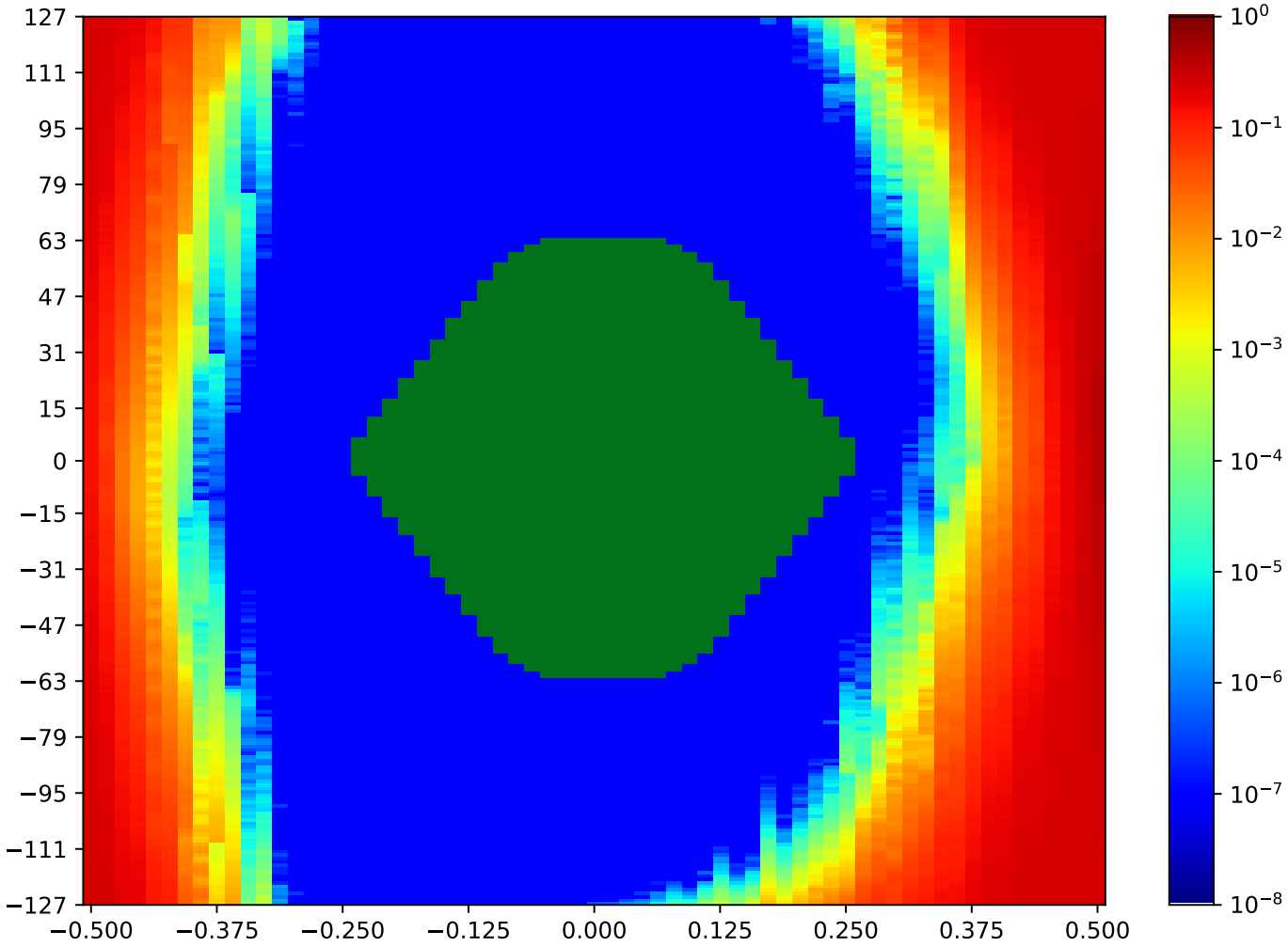


Figure 4.198: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.11 MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Table 4.184: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:45:44		2018-Sep-27 15:46:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9030	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

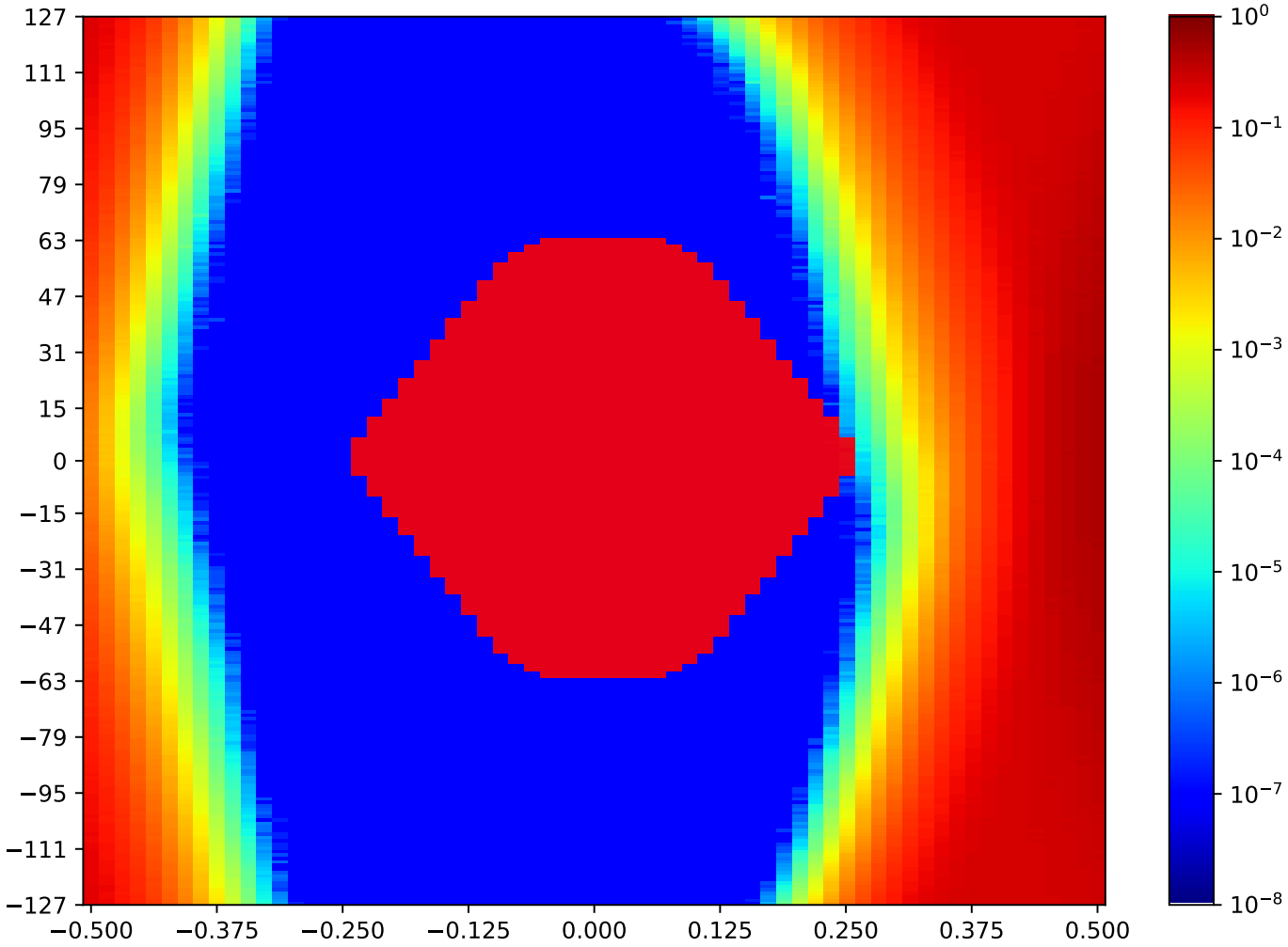


Figure 4.199: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.15.12 MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Table 4.185: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:45:24		2018-Sep-27 15:45:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9437	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

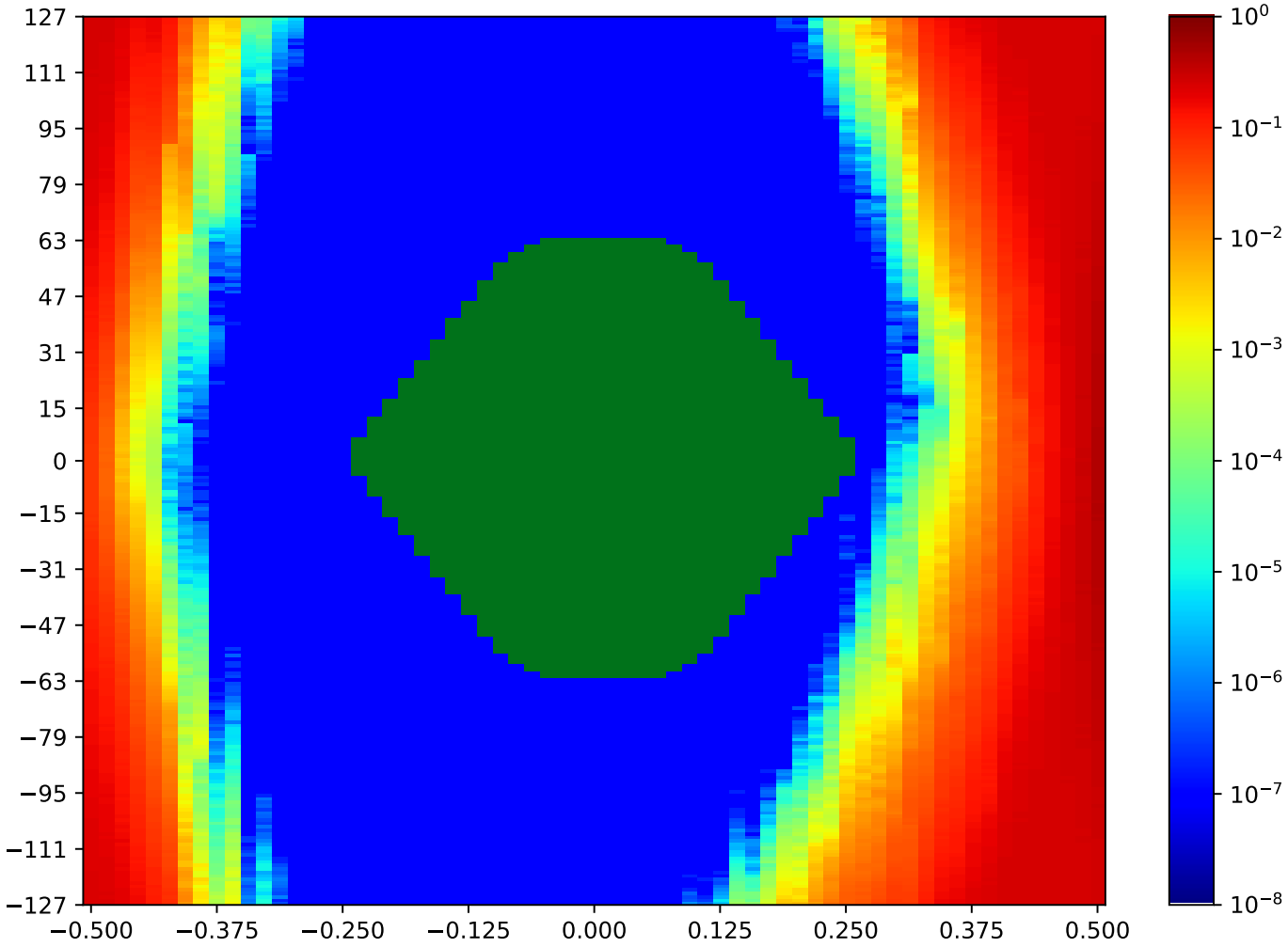


Figure 4.200: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16 MSP_A TX2 MSP_C RX11 Minipod Loopback

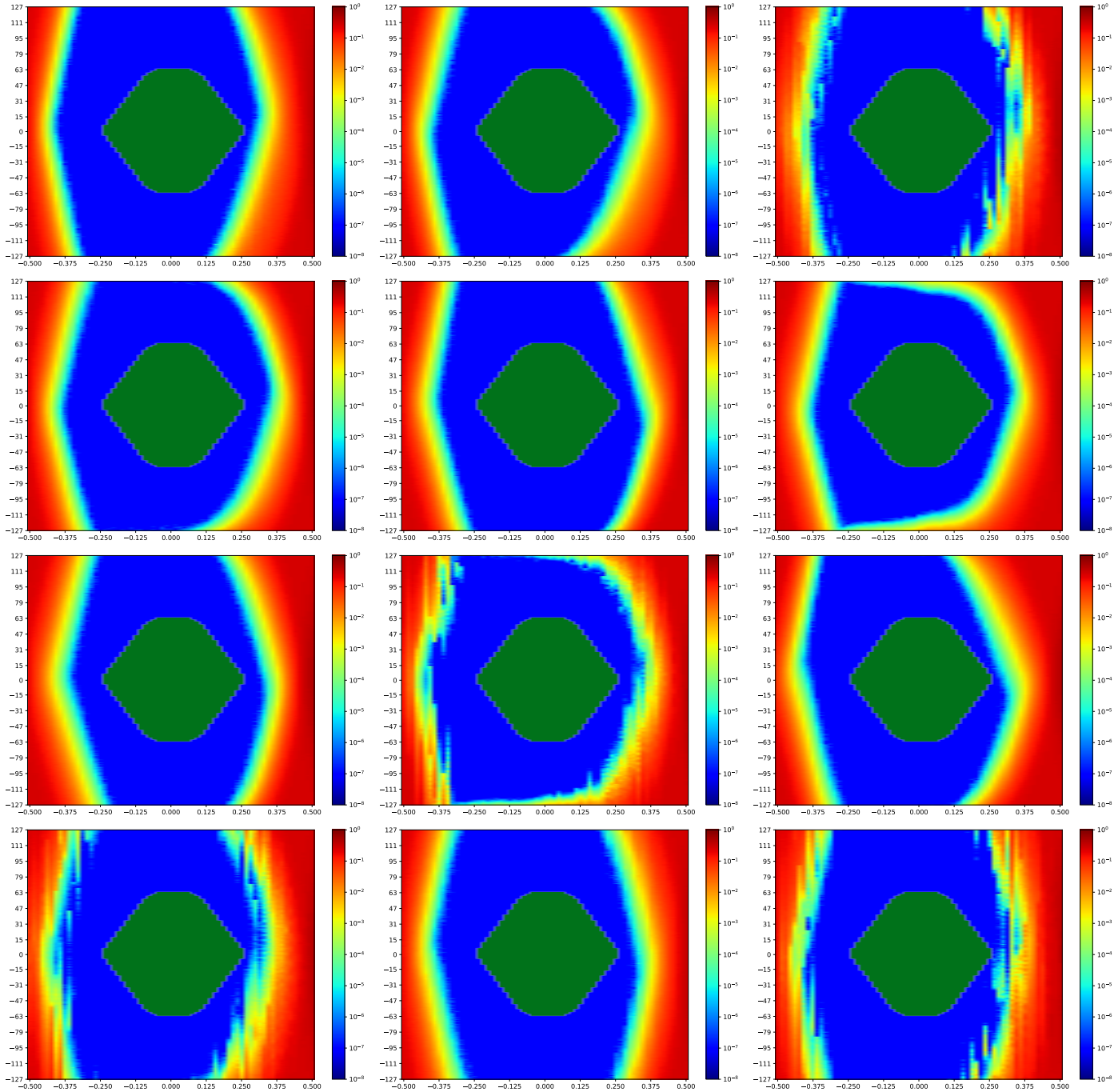


Figure 4.201: MSP_A TX2 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.214.

4.16.1 MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Table 4.186: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:48:16		2018-Sep-27 15:48:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9408	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

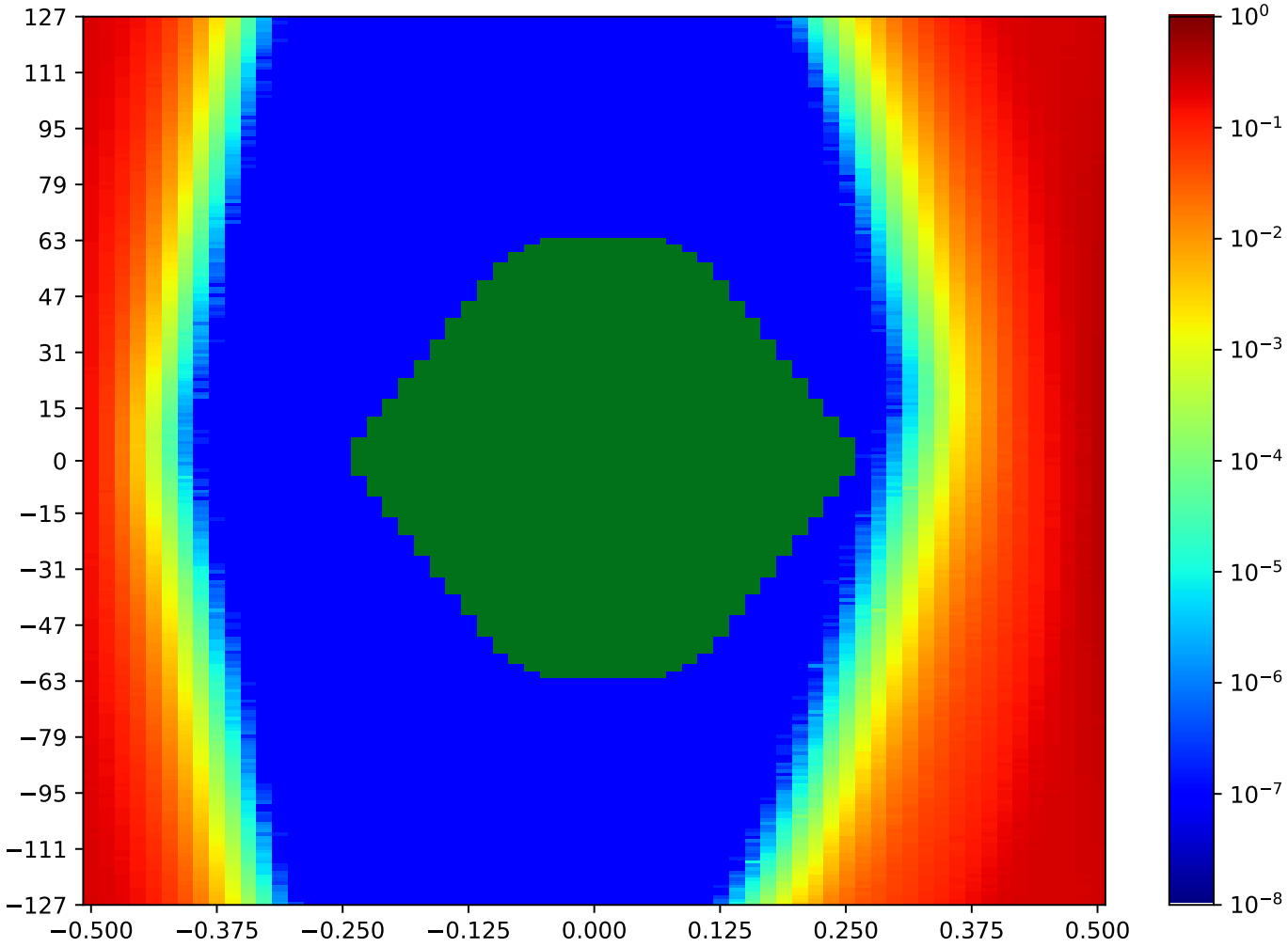


Figure 4.202: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.2 MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Table 4.187: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:47:36		2018-Sep-27 15:47:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8888	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

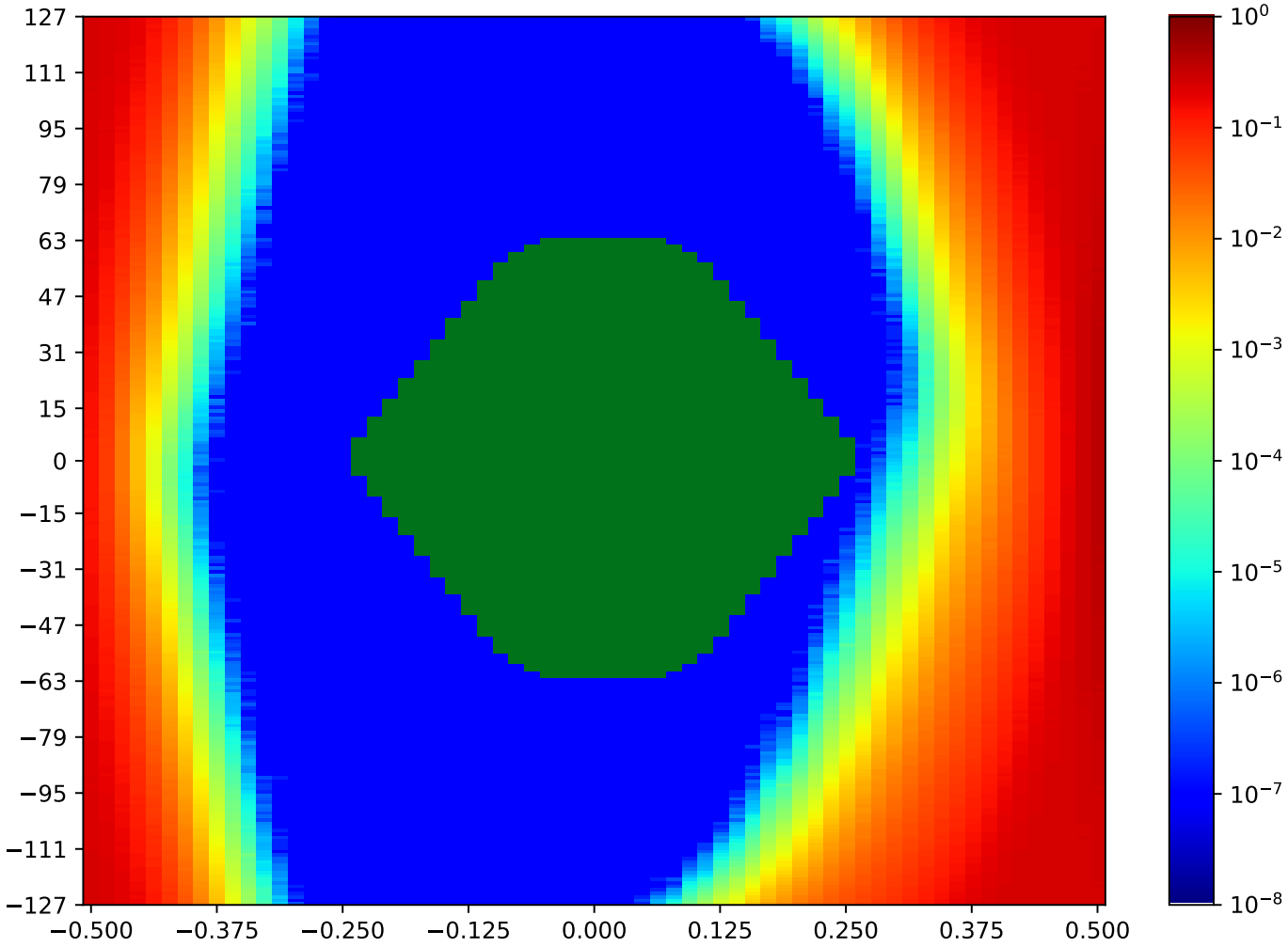


Figure 4.203: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.3 MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Table 4.188: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:49:18		2018-Sep-27 15:49:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9223	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

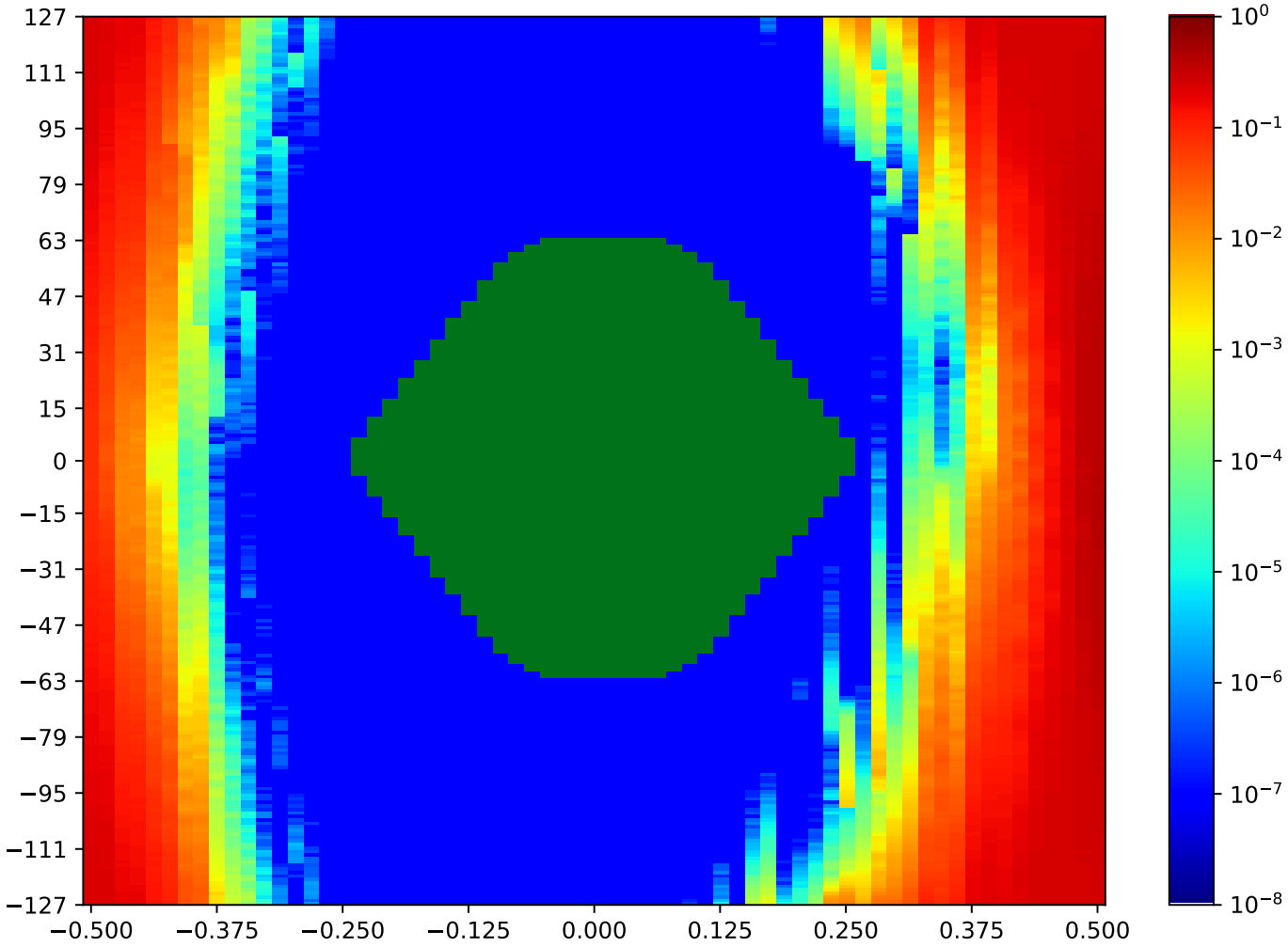


Figure 4.204: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.4 MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Table 4.189: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:47:16		2018-Sep-27 15:47:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9034	43	66.15%	248	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

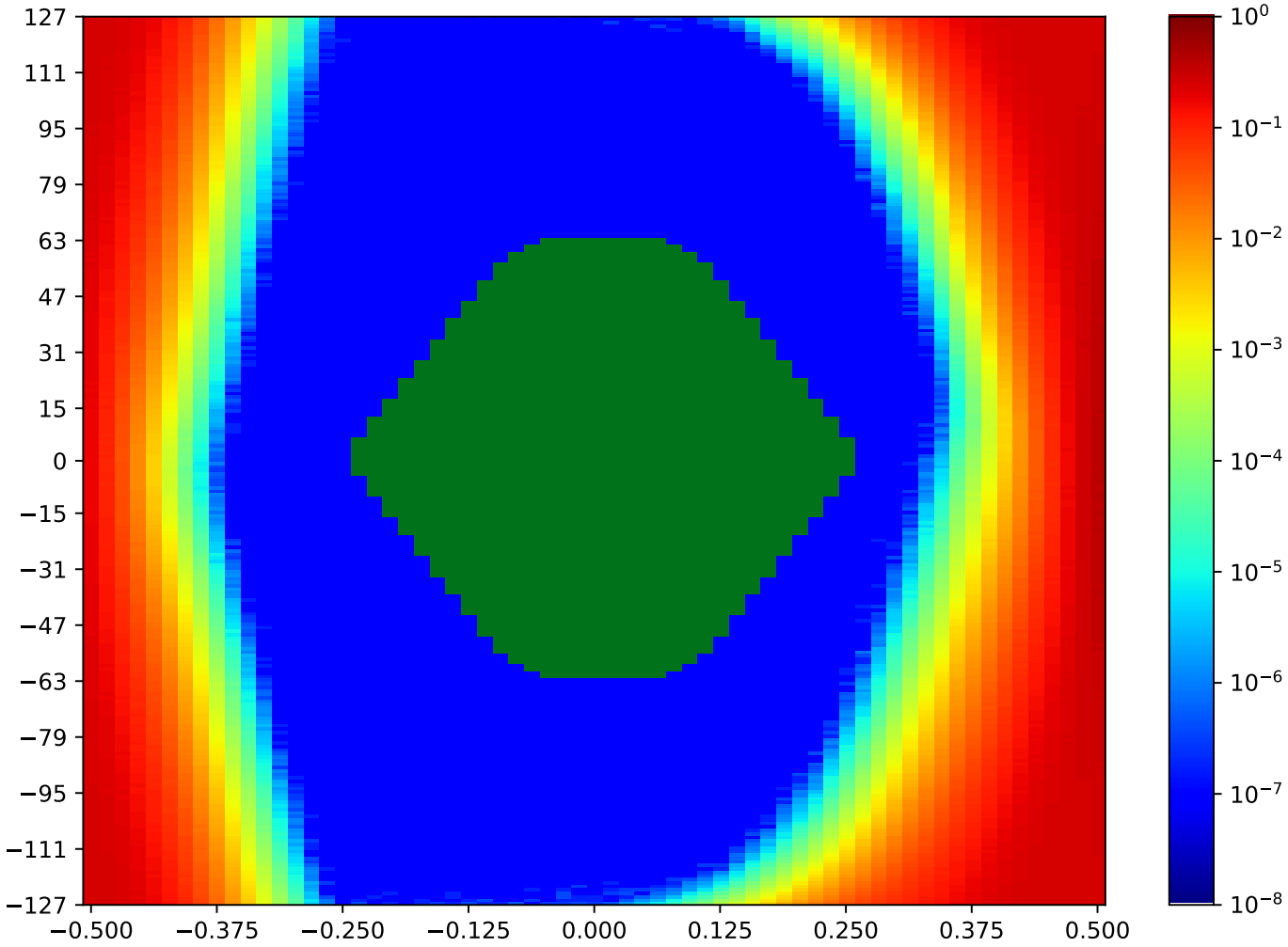


Figure 4.205: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.5 MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Table 4.190: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:50:19		2018-Sep-27 15:50:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9427	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

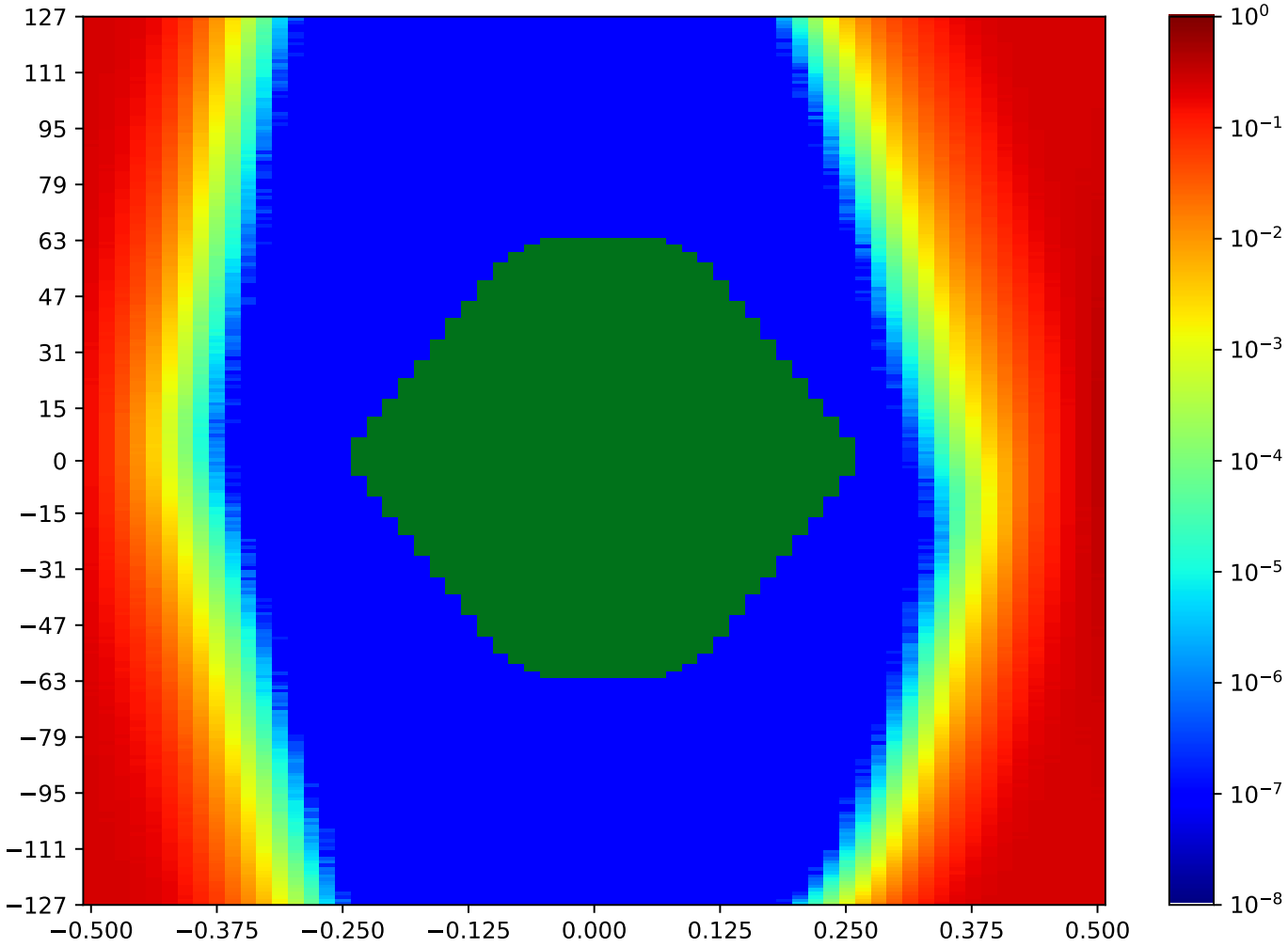


Figure 4.206: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.6 MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Table 4.191: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:47:56		2018-Sep-27 15:48:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7961	42	64.62%	223	87.45%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

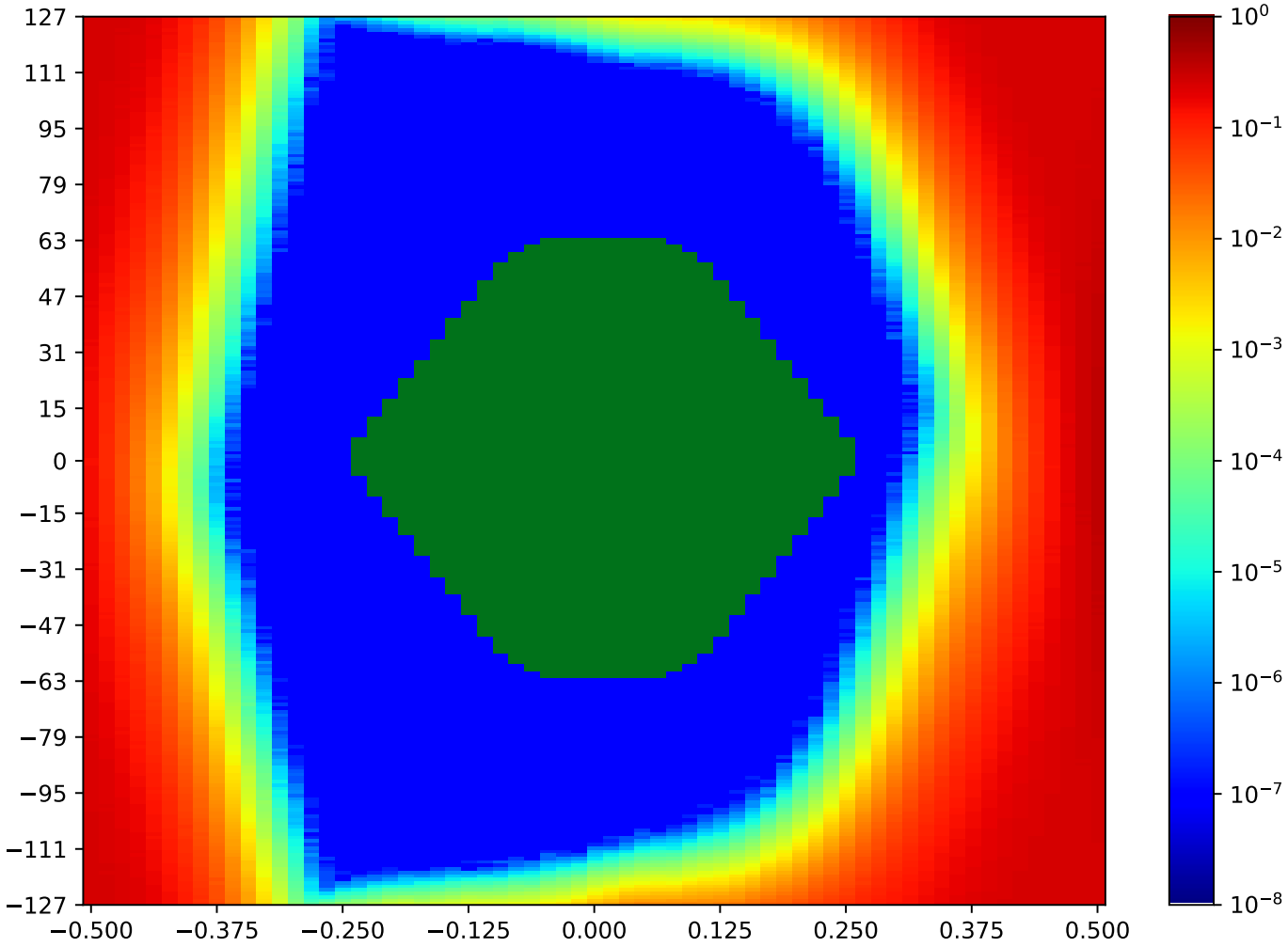


Figure 4.207: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.7 MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Table 4.192: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:50:59		2018-Sep-27 15:51:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8654	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

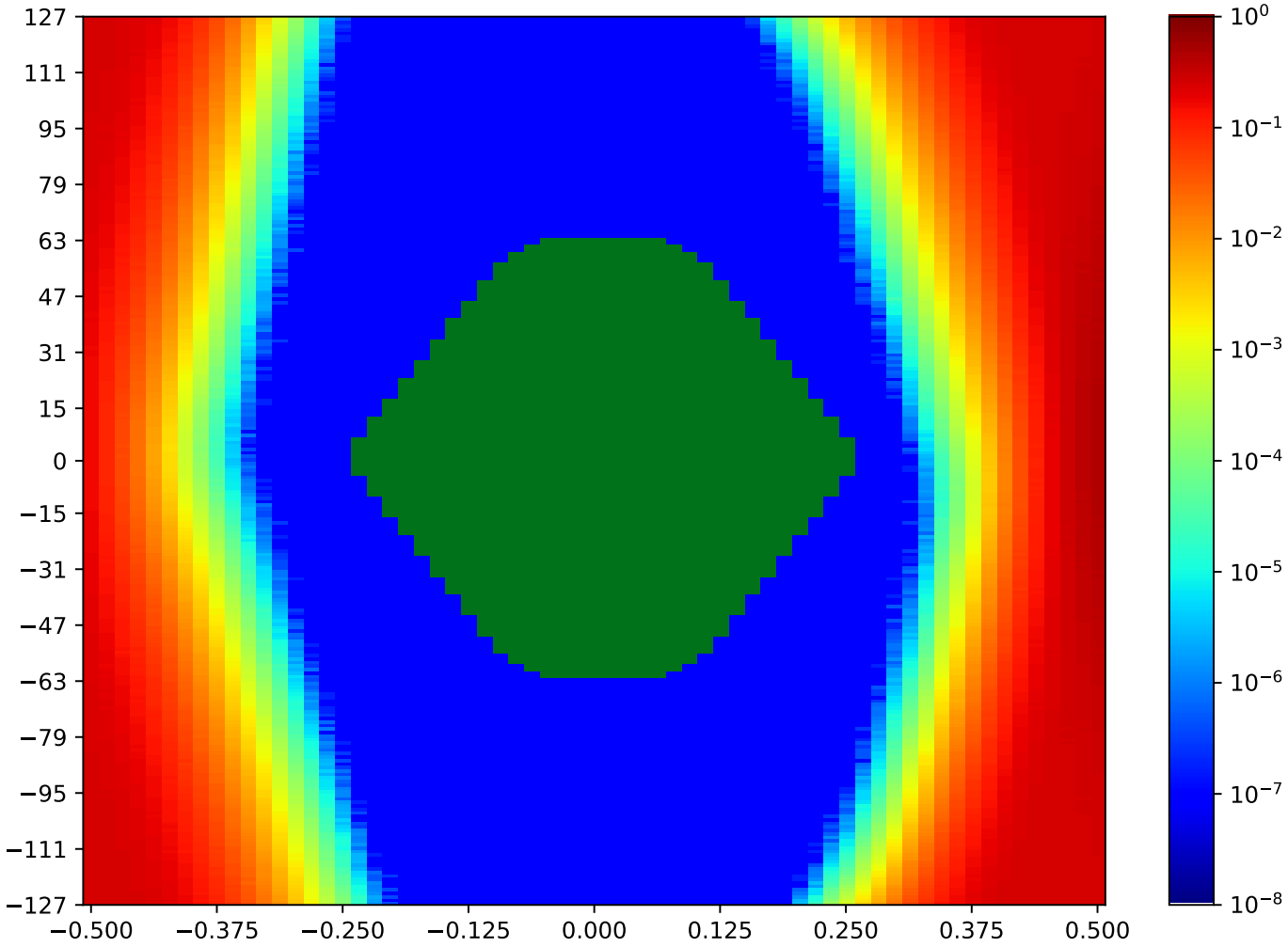


Figure 4.208: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.8 MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Table 4.193: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:48:37		2018-Sep-27 15:48:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9041	45	69.23%	237	92.94%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

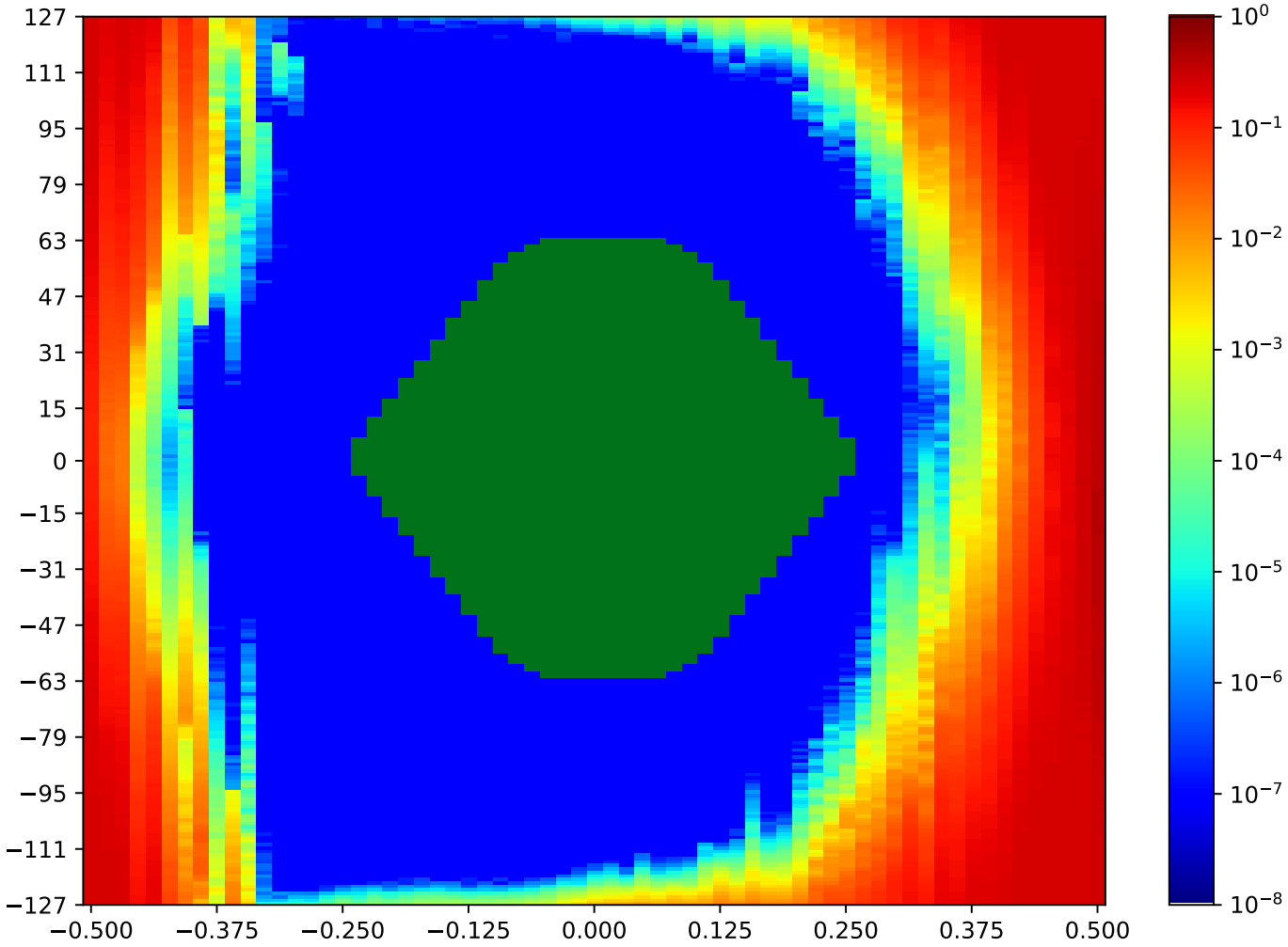


Figure 4.209: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.9 MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Table 4.194: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:50:39		2018-Sep-27 15:50:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8876	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

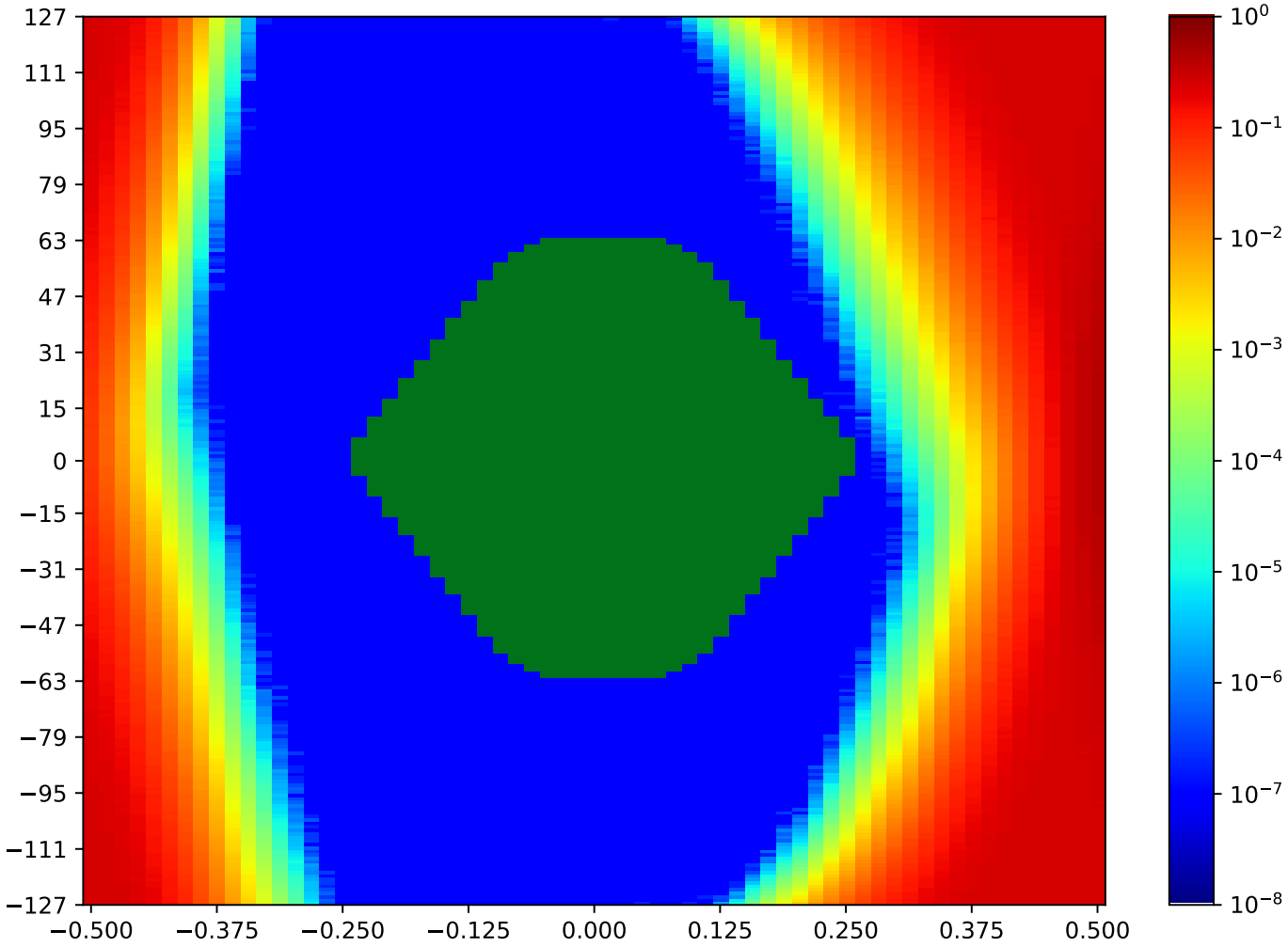


Figure 4.210: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.10 MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Table 4.195: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:48:57		2018-Sep-27 15:49:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9019	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

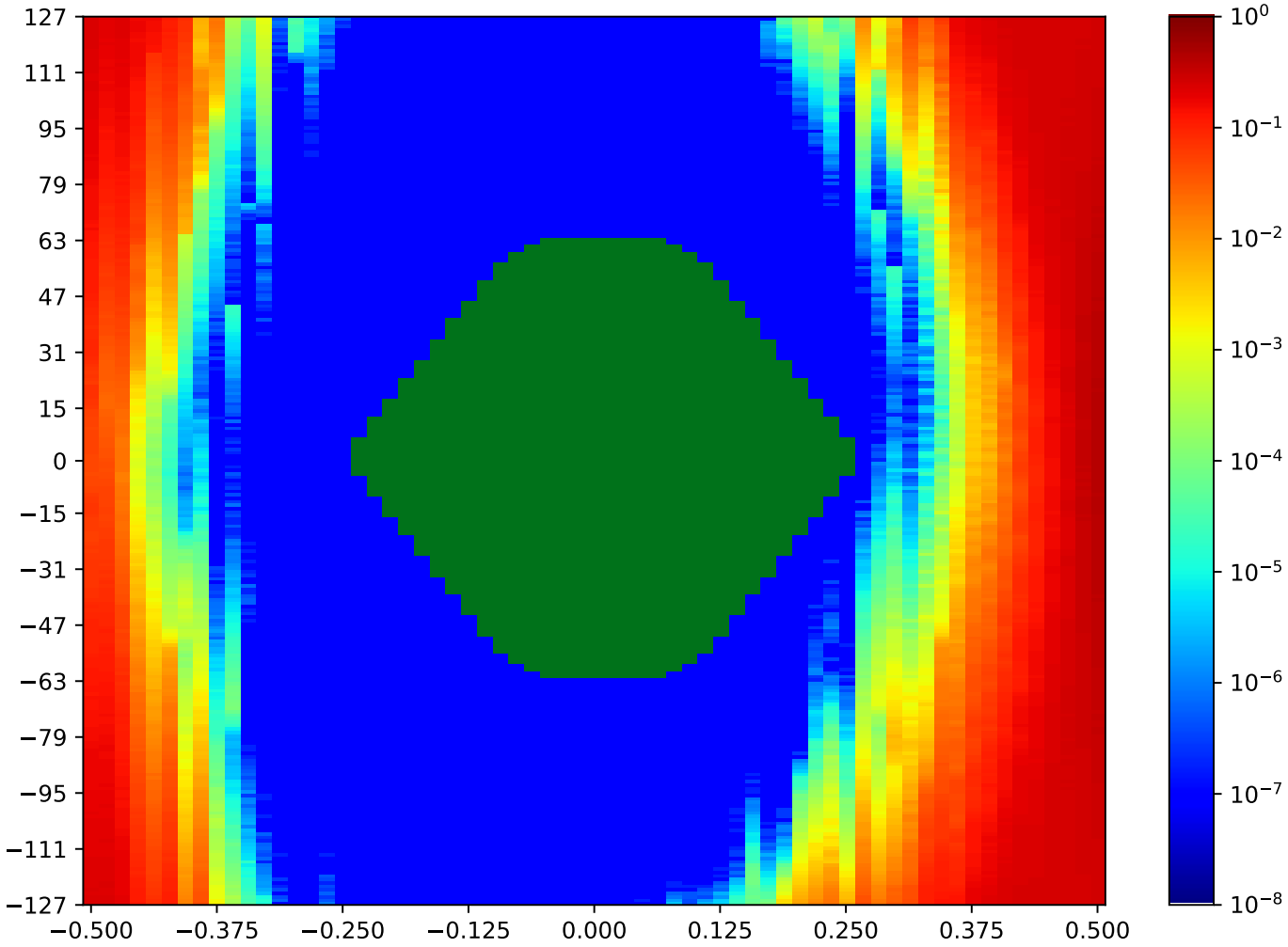


Figure 4.211: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.11 MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Table 4.196: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:49:58		2018-Sep-27 15:50:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9415	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

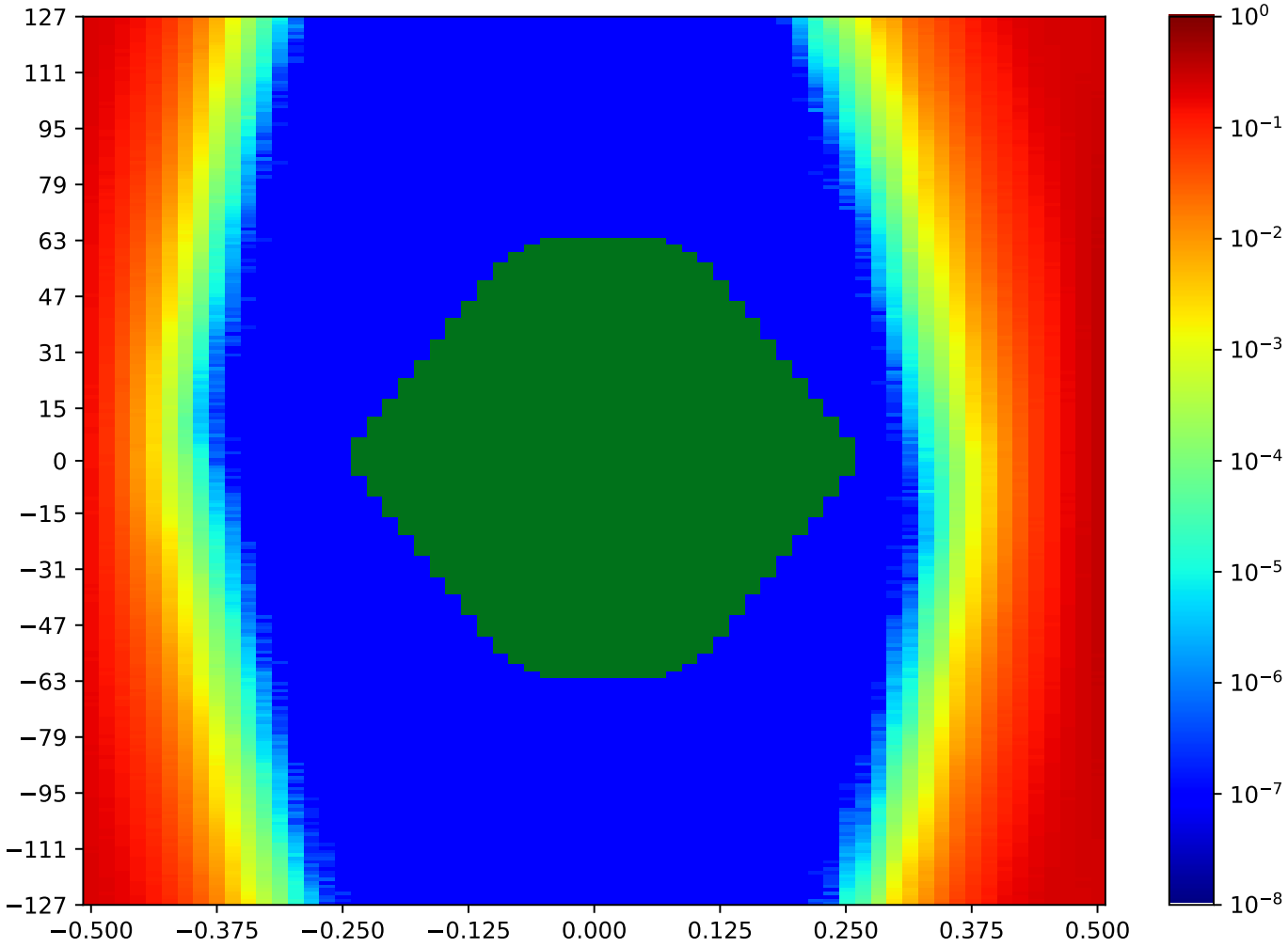


Figure 4.212: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.16.12 MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Table 4.197: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:49:38		2018-Sep-27 15:49:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9626	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

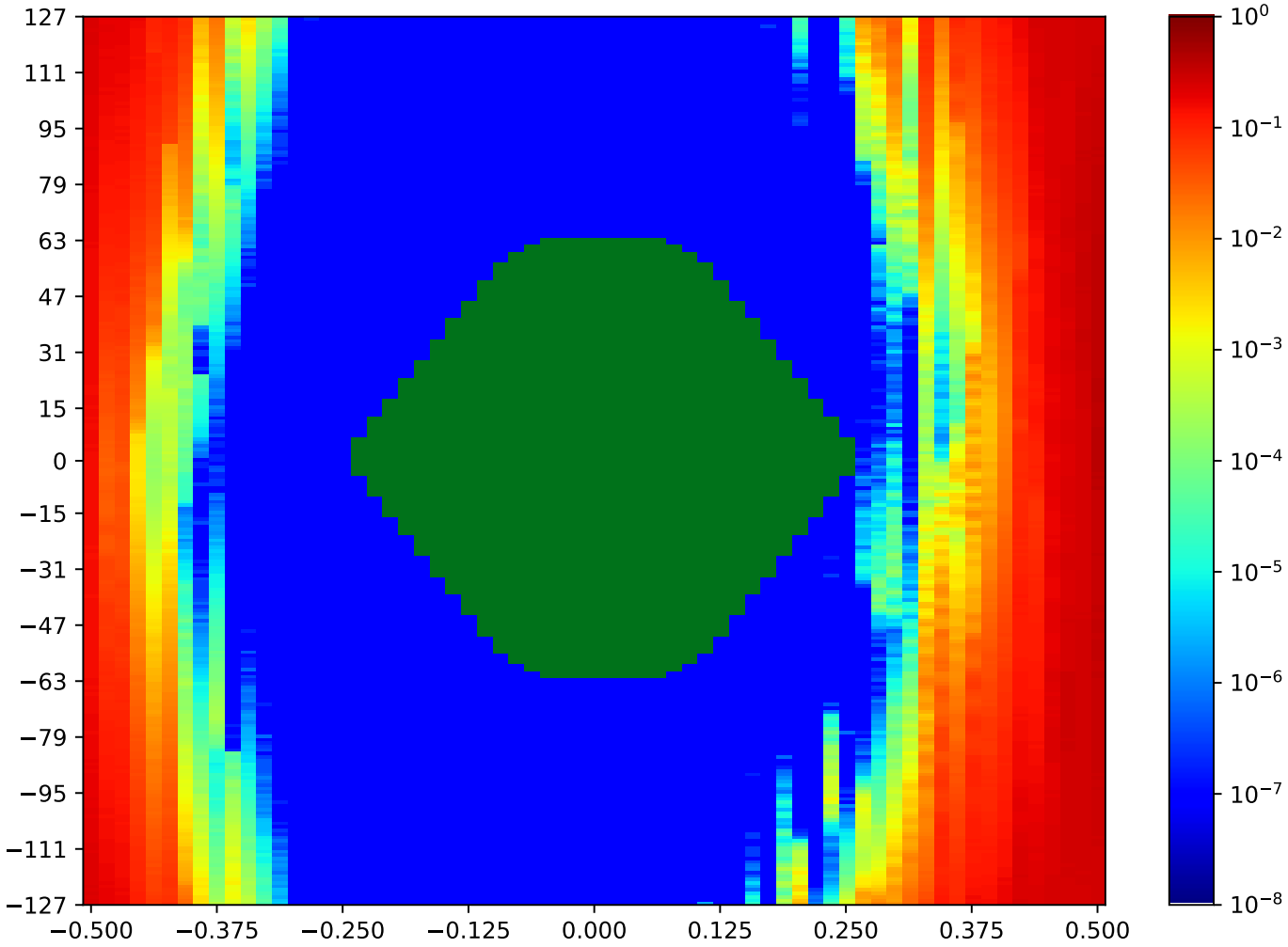


Figure 4.213: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17 MSP_C TX3 MSP_A RX1 Minipod Loopback

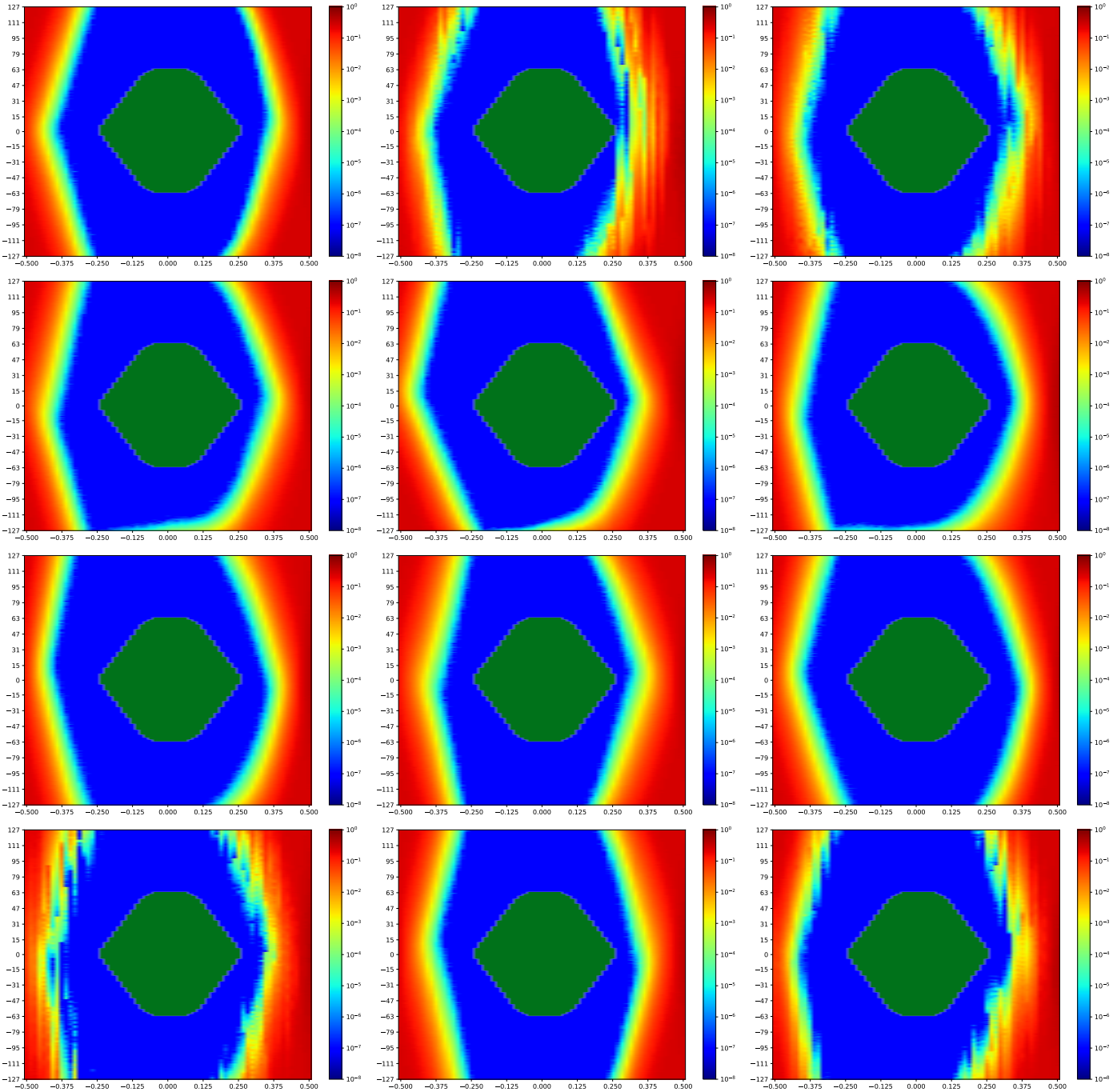


Figure 4.214: MSP_C TX3 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.227.

4.17.1 MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Table 4.198: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:52:21		2018-Sep-27 15:52:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9646	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

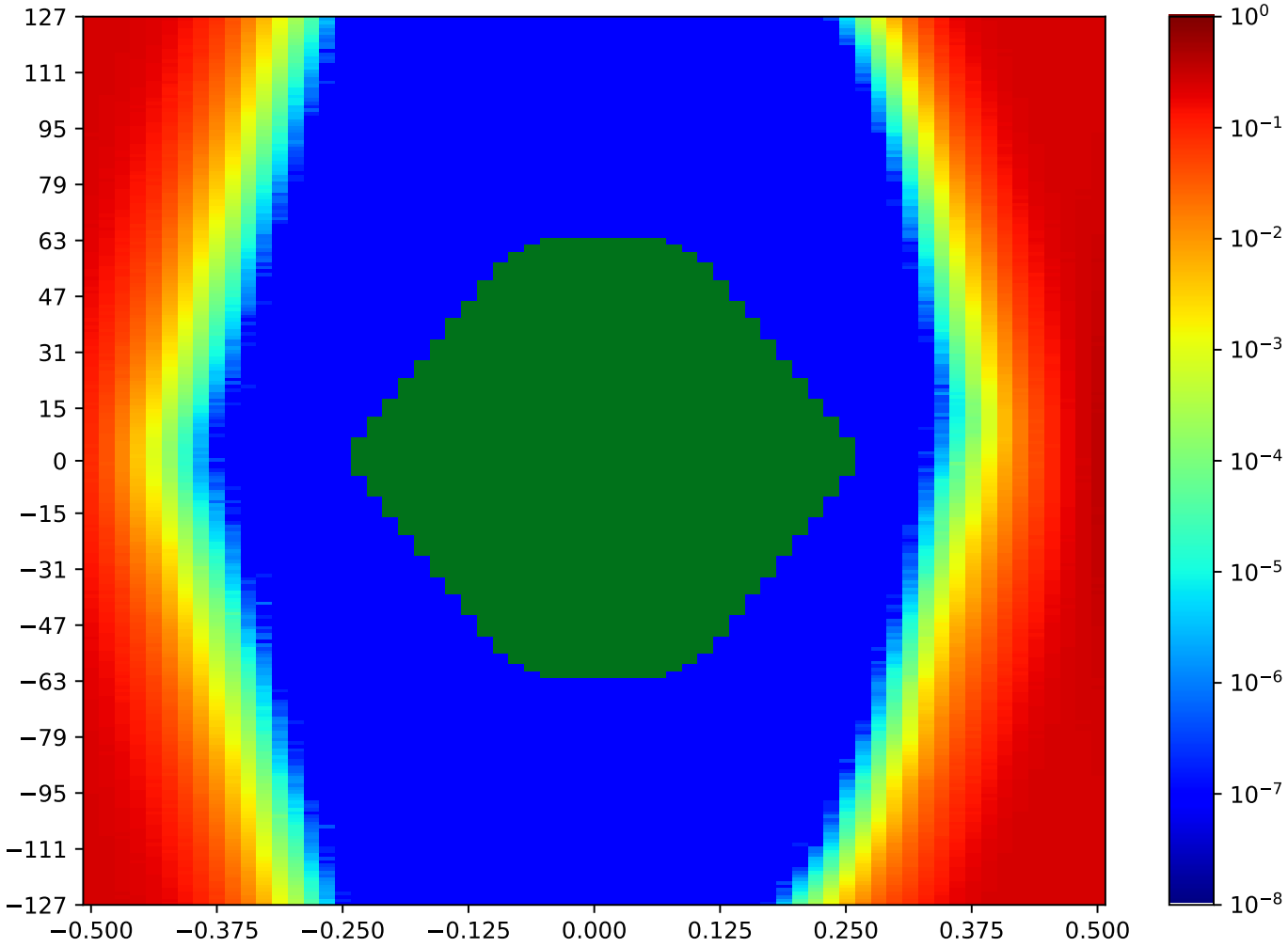


Figure 4.215: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.2 MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Table 4.199: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:53:02		2018-Sep-27 15:53:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8697	43	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

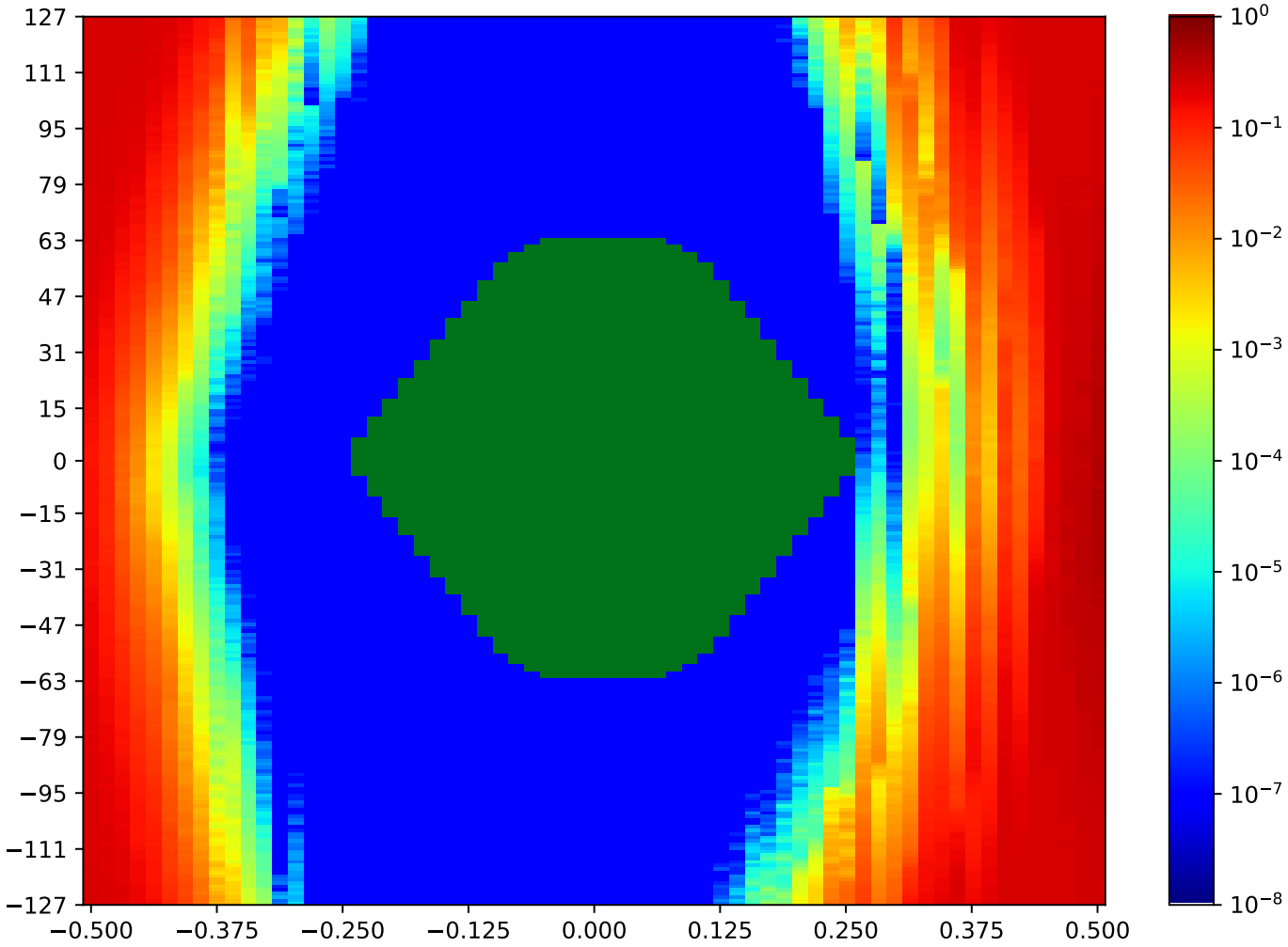


Figure 4.216: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.3 MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Table 4.200: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:53:22		2018-Sep-27 15:53:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9028	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

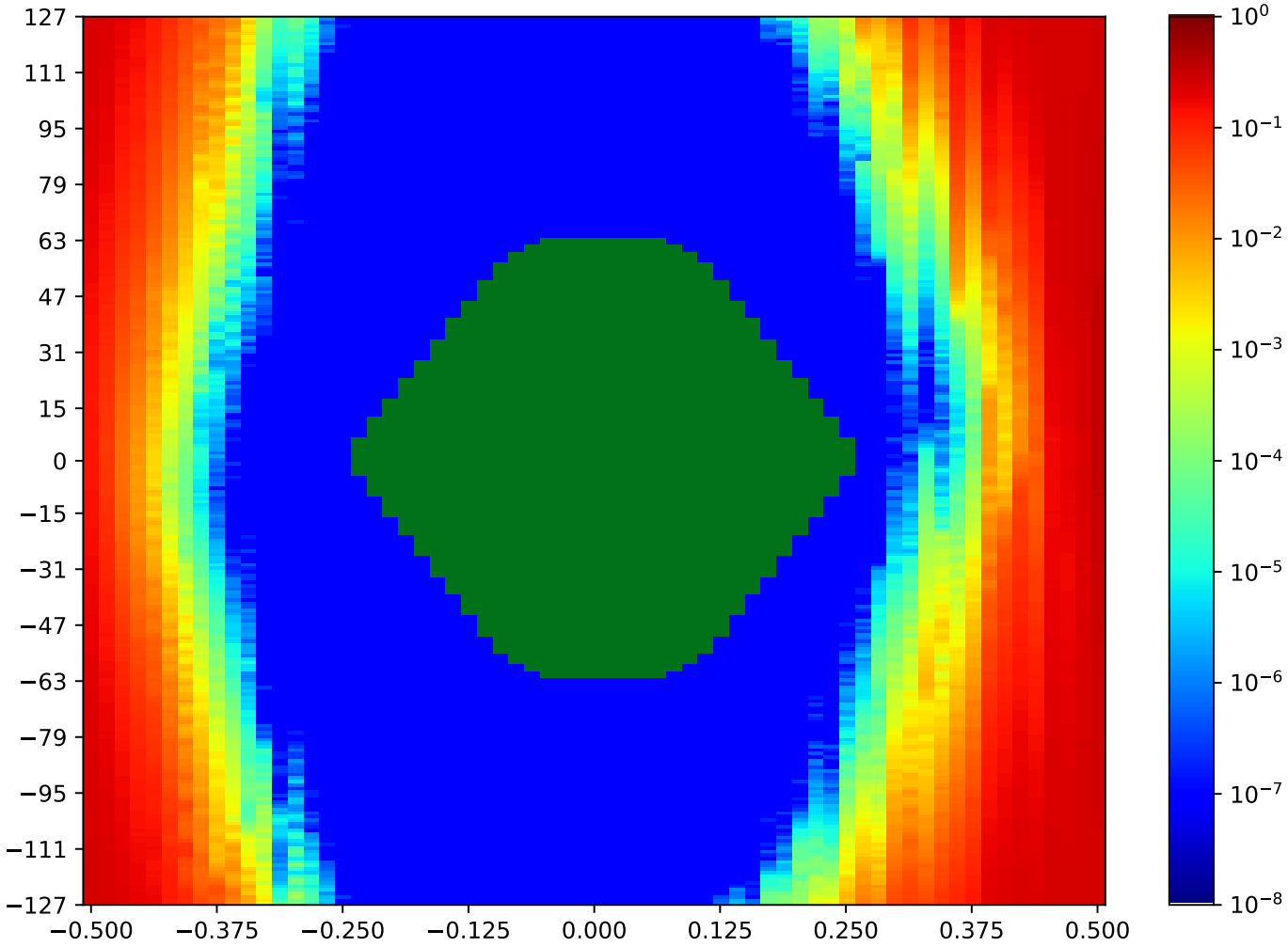


Figure 4.217: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.4 MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Table 4.201: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:51:40		2018-Sep-27 15:52:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8699	43	66.15%	239	93.73%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

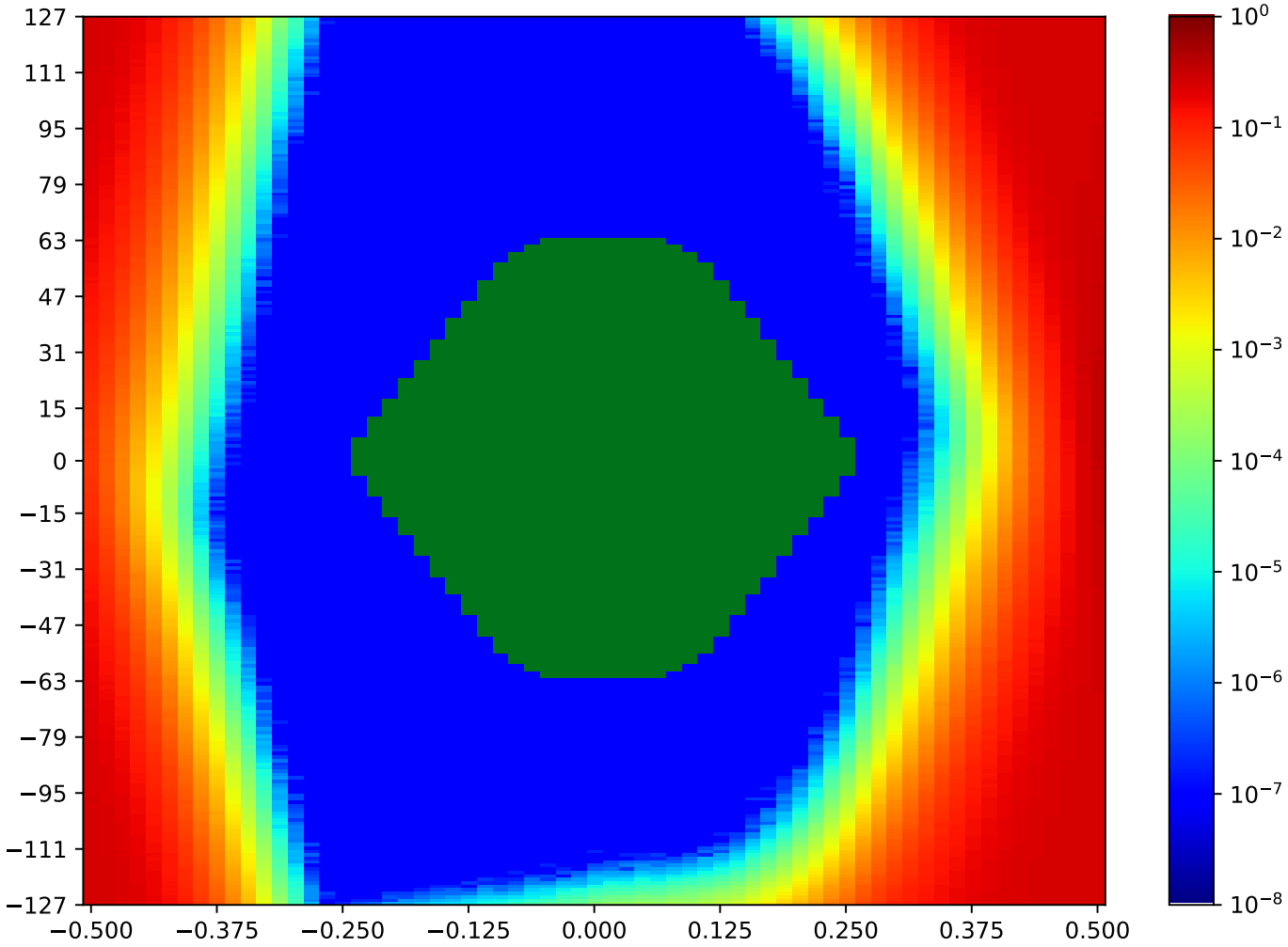


Figure 4.218: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.5 MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Table 4.202: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:54:24		2018-Sep-27 15:54:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8587	43	66.15%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

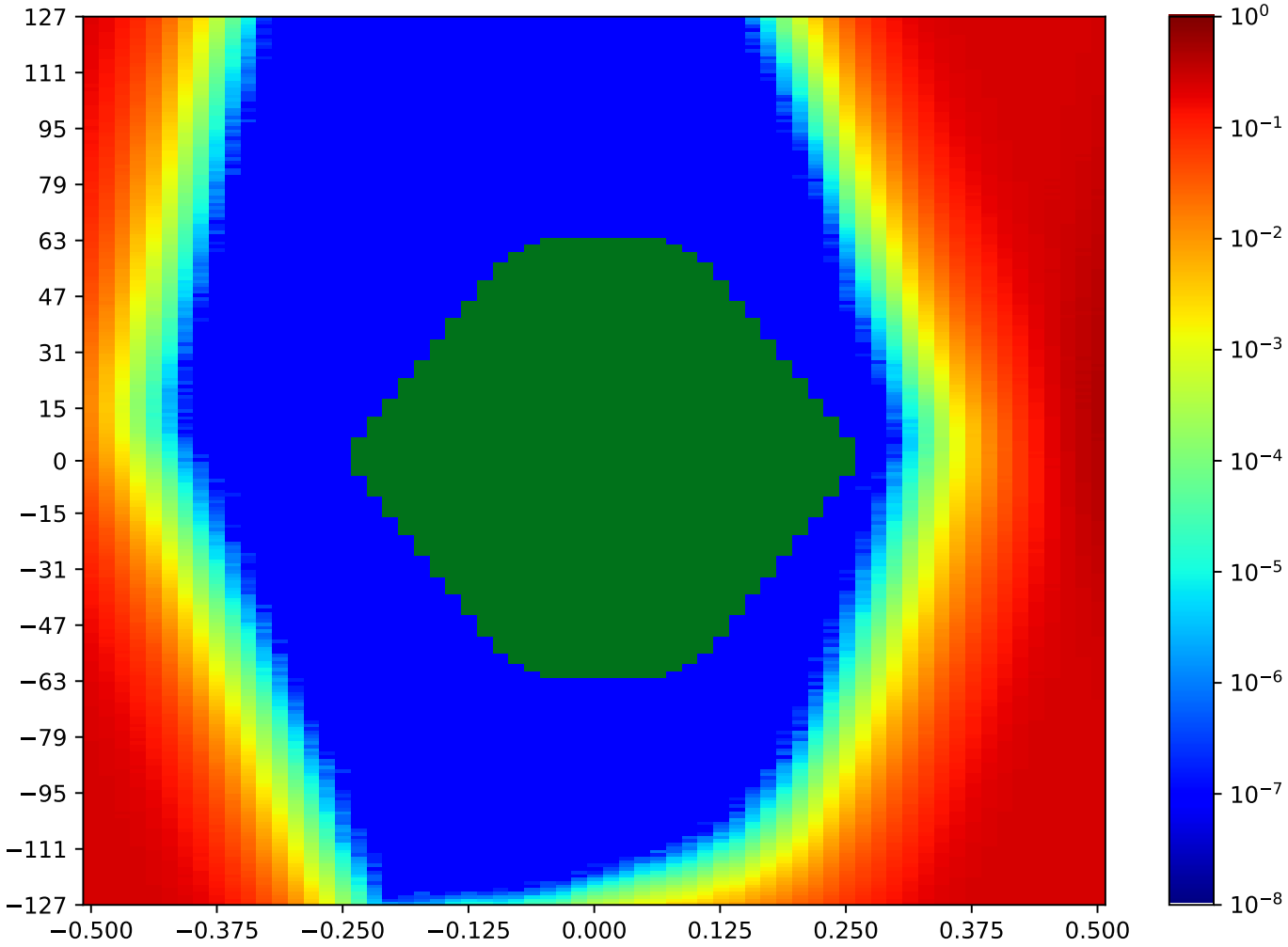


Figure 4.219: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.6 MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Table 4.203: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:51:20		2018-Sep-27 15:51:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8781	44	67.69%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

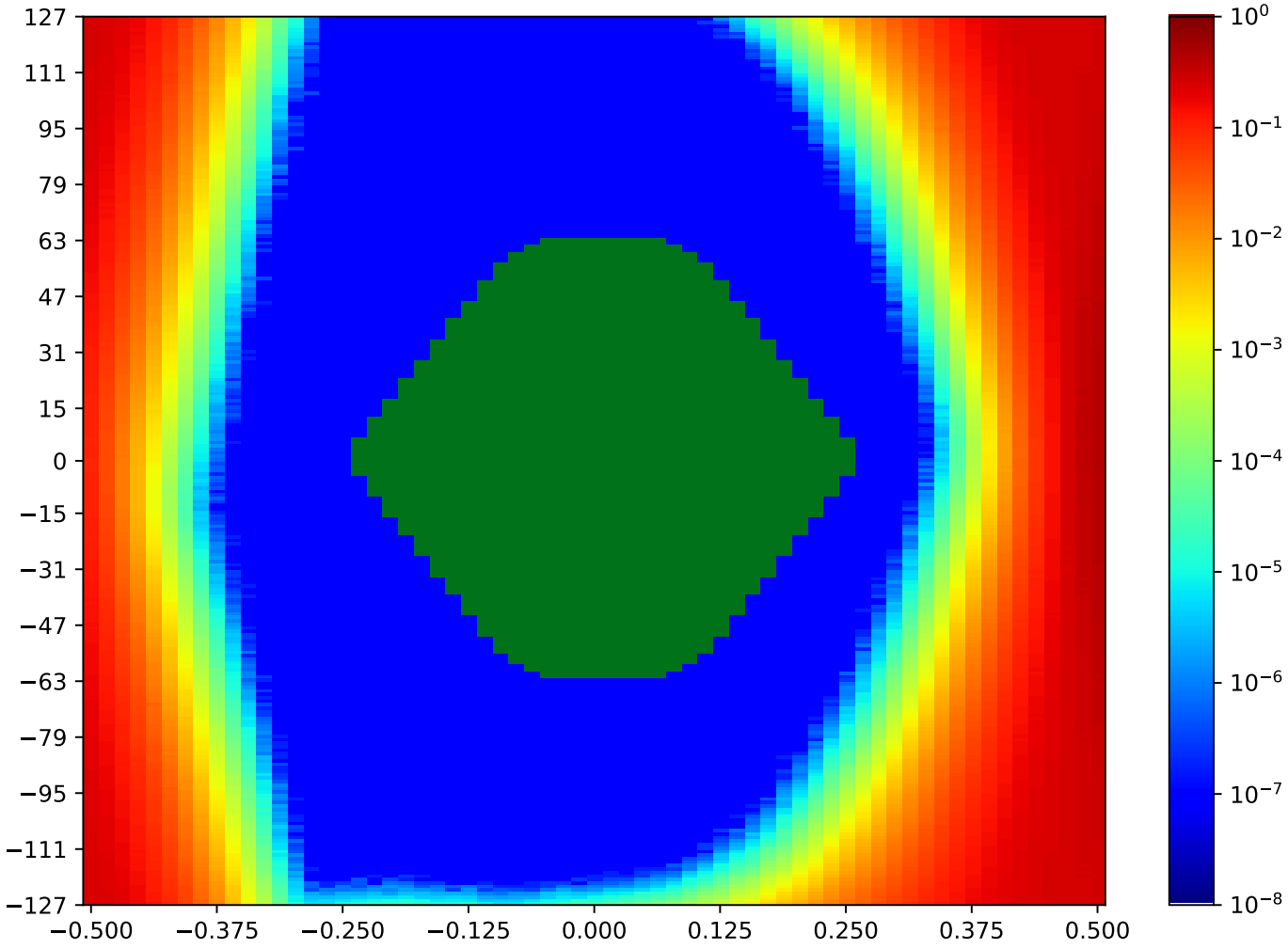


Figure 4.220: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.7 MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Table 4.204: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:55:05		2018-Sep-27 15:55:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9711	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

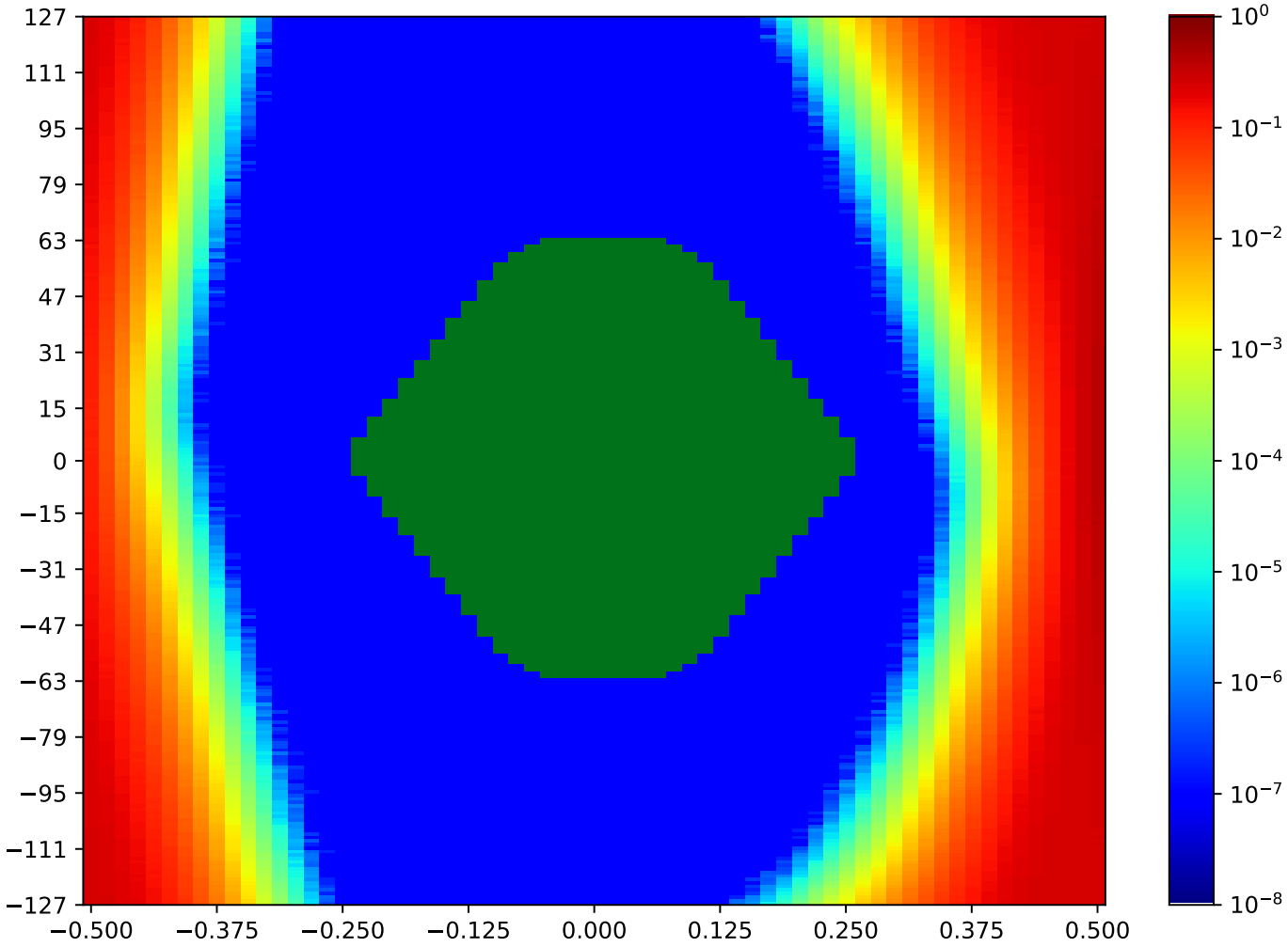


Figure 4.221: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.8 MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Table 4.205: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:52:01		2018-Sep-27 15:52:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8413	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

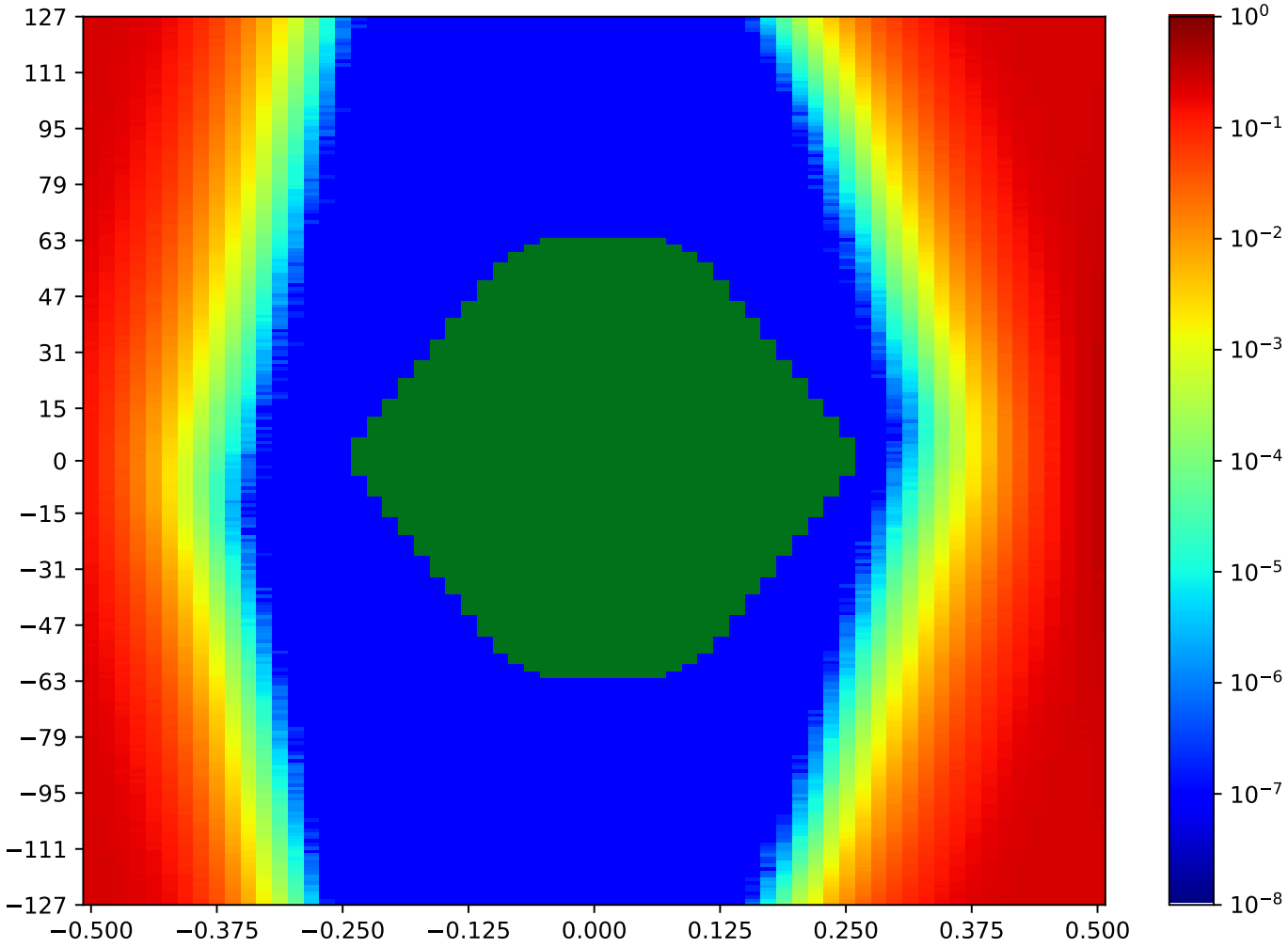


Figure 4.222: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.9 MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Table 4.206: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:54:45		2018-Sep-27 15:55:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9405	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

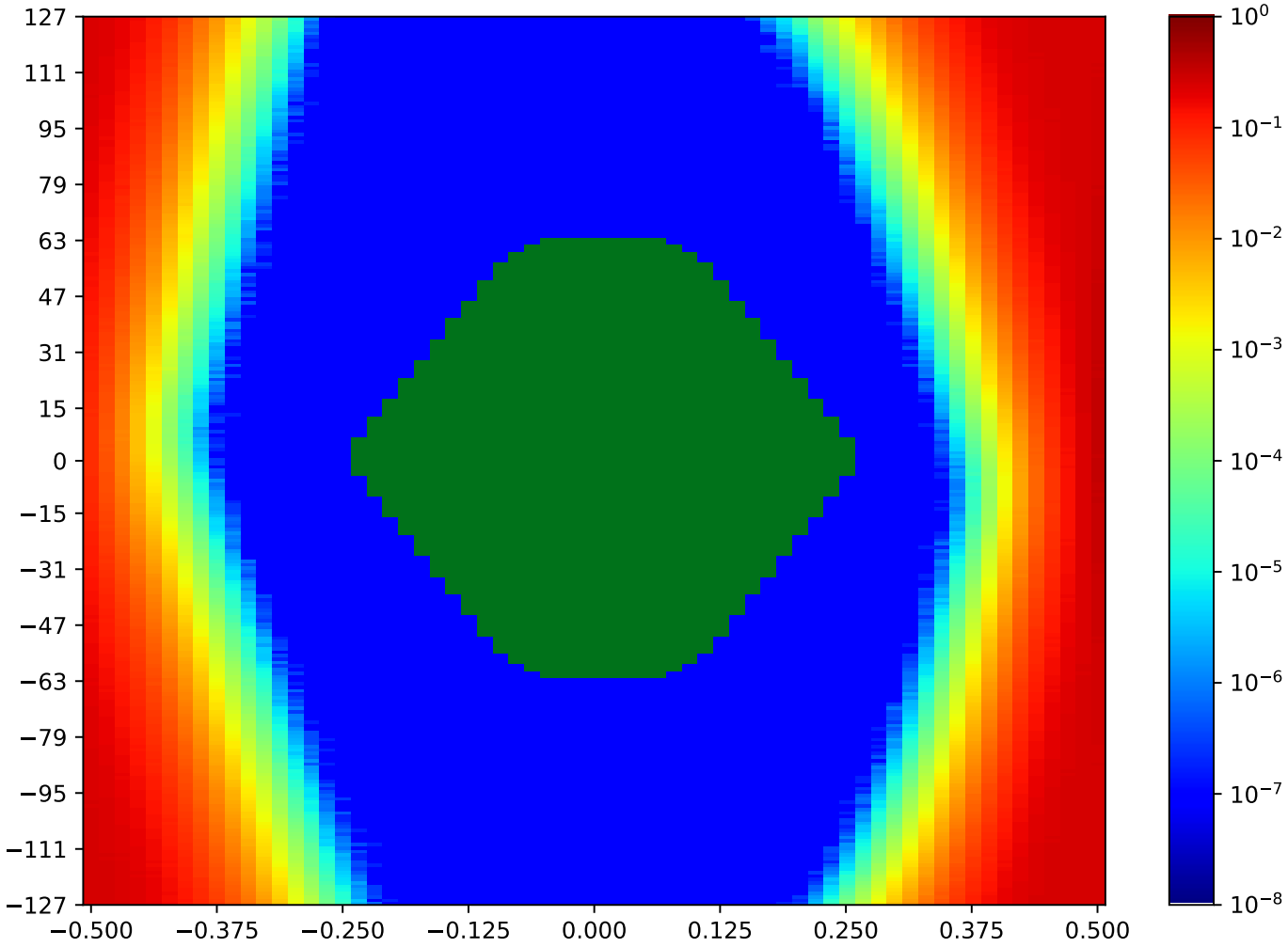


Figure 4.223: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.10 MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Table 4.207: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:52:42		2018-Sep-27 15:53:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9412	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

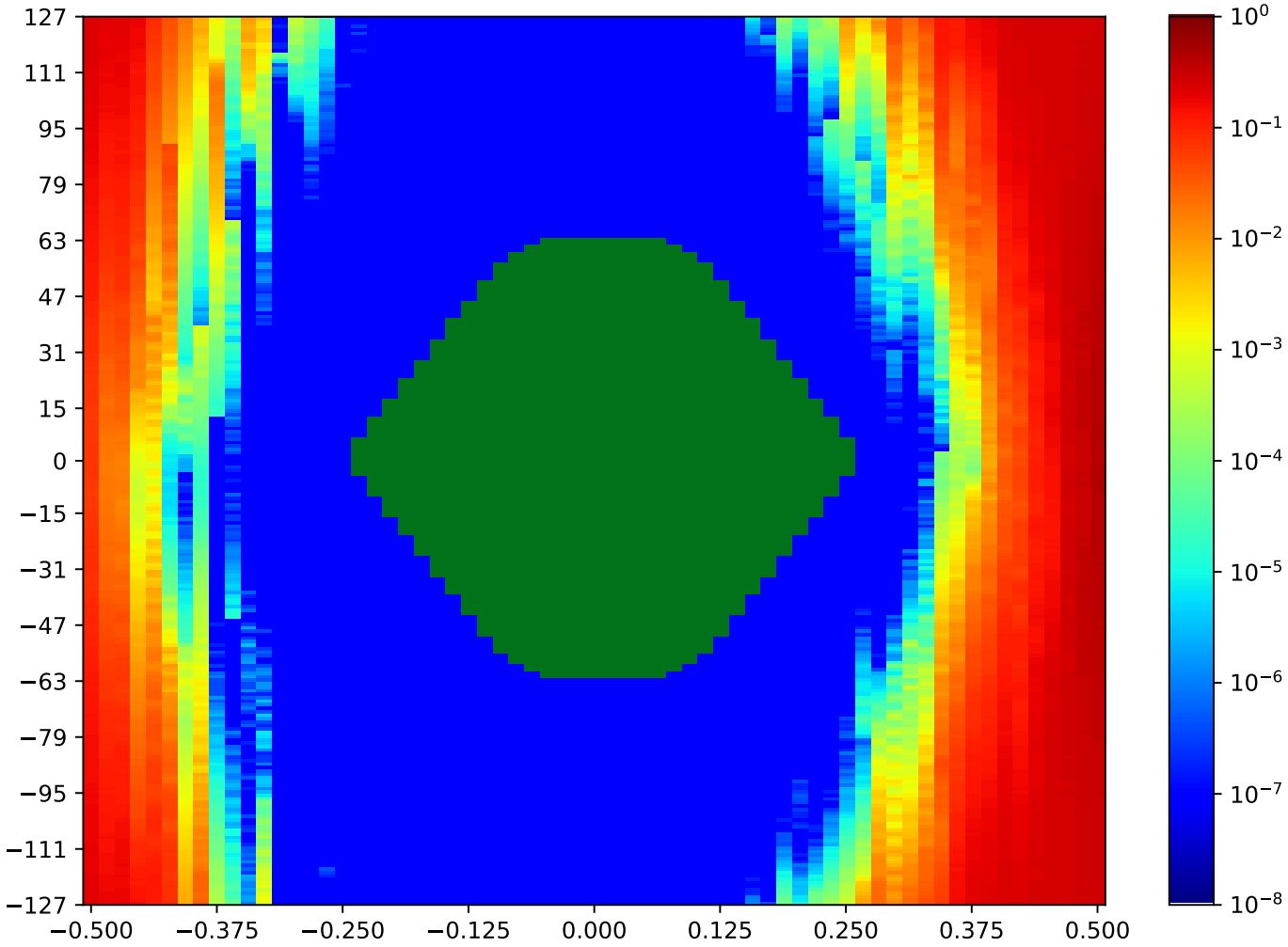


Figure 4.224: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.11 MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Table 4.208: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:54:04		2018-Sep-27 15:54:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9140	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

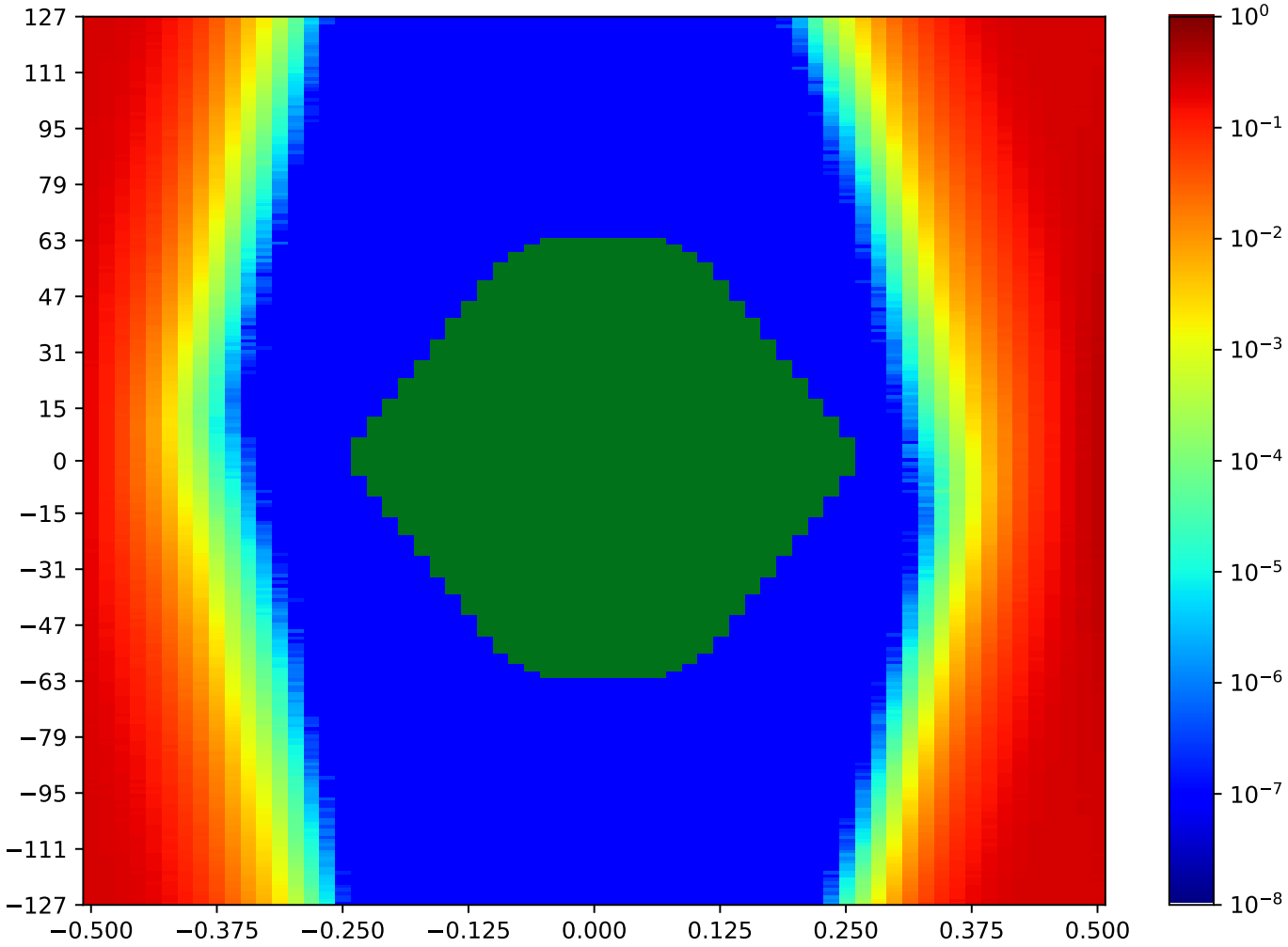


Figure 4.225: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.17.12 MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Table 4.209: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:53:43		2018-Sep-27 15:54:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9606	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

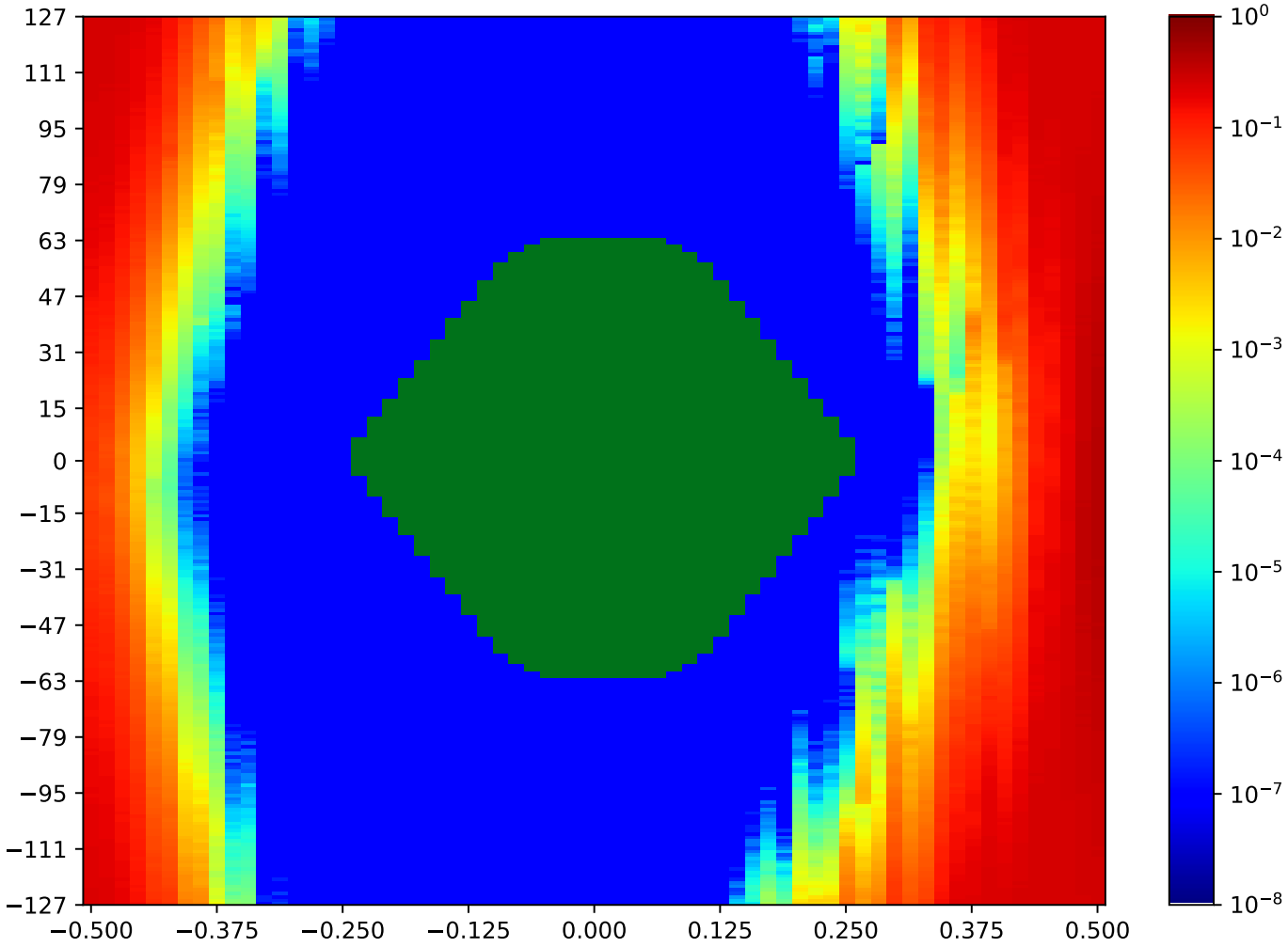


Figure 4.226: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18 MSP_C TX4 MSP_A RX2 Minipod Loopback

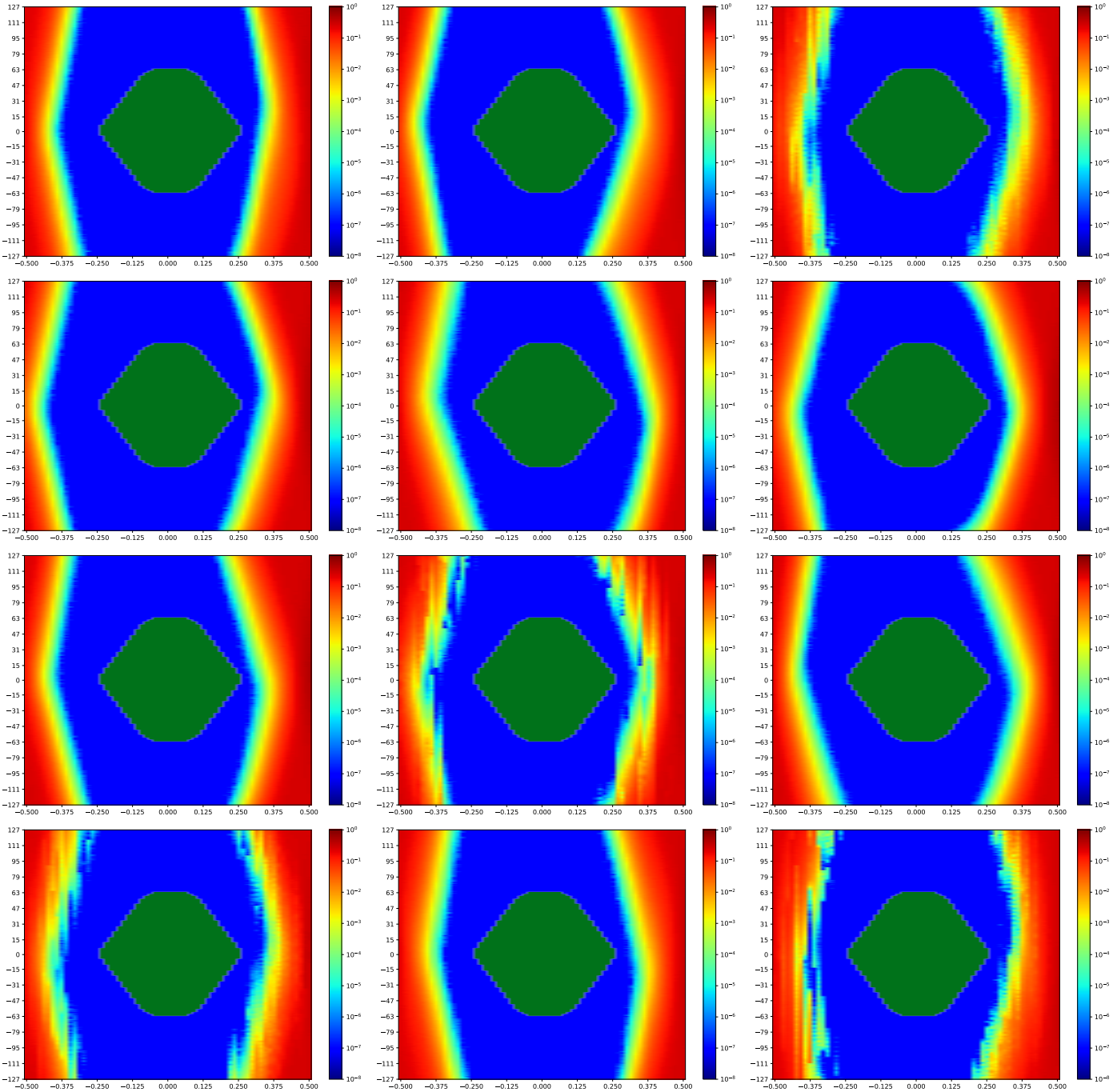


Figure 4.227: MSP_C TX4 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.240.

4.18.1 MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Table 4.210: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:56:27		2018-Sep-27 15:56:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9794	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

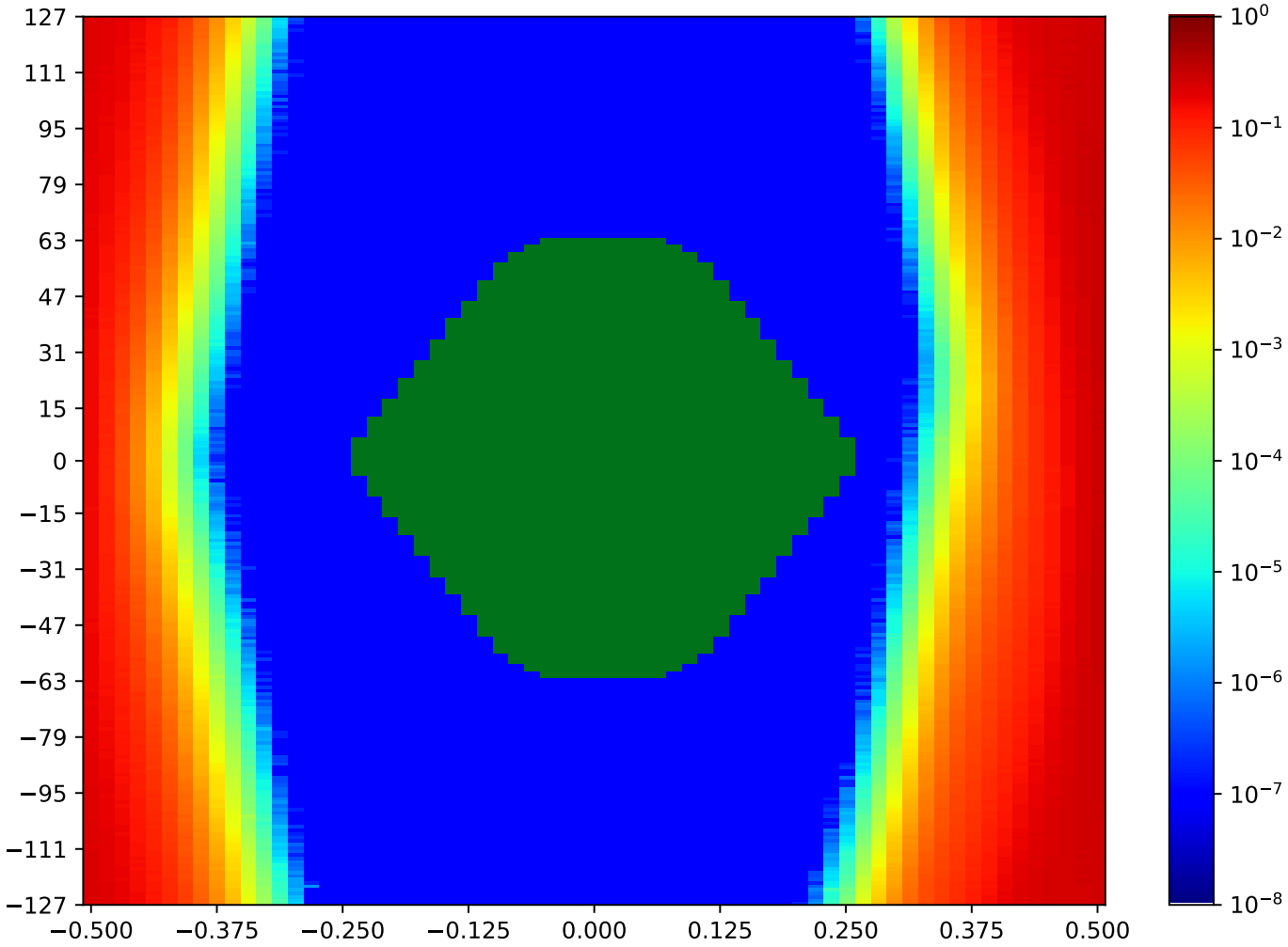


Figure 4.228: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.2 MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Table 4.211: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:55:46		2018-Sep-27 15:56:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9510	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

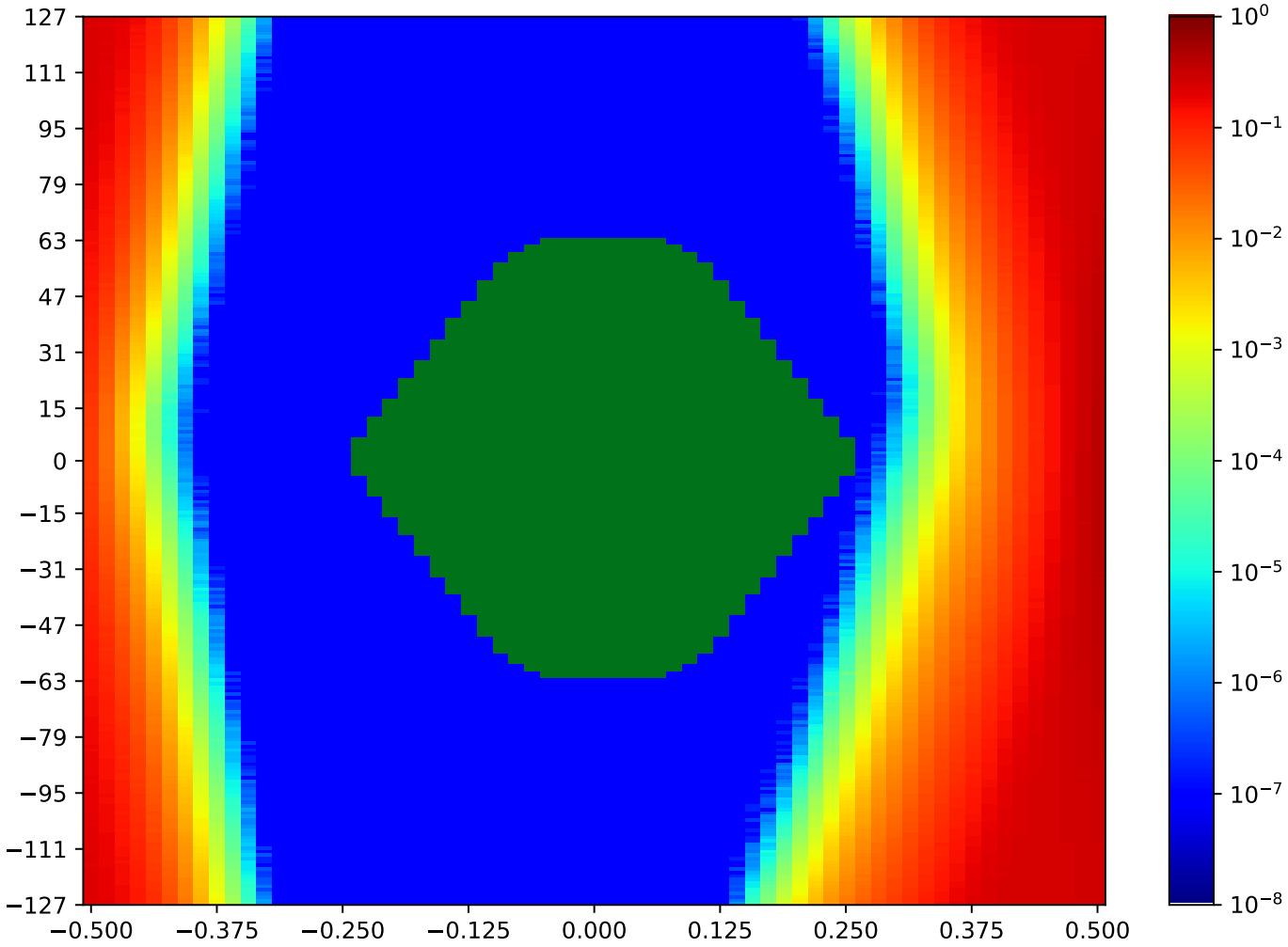


Figure 4.229: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.3 MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Table 4.212: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:57:29		2018-Sep-27 15:57:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9230	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

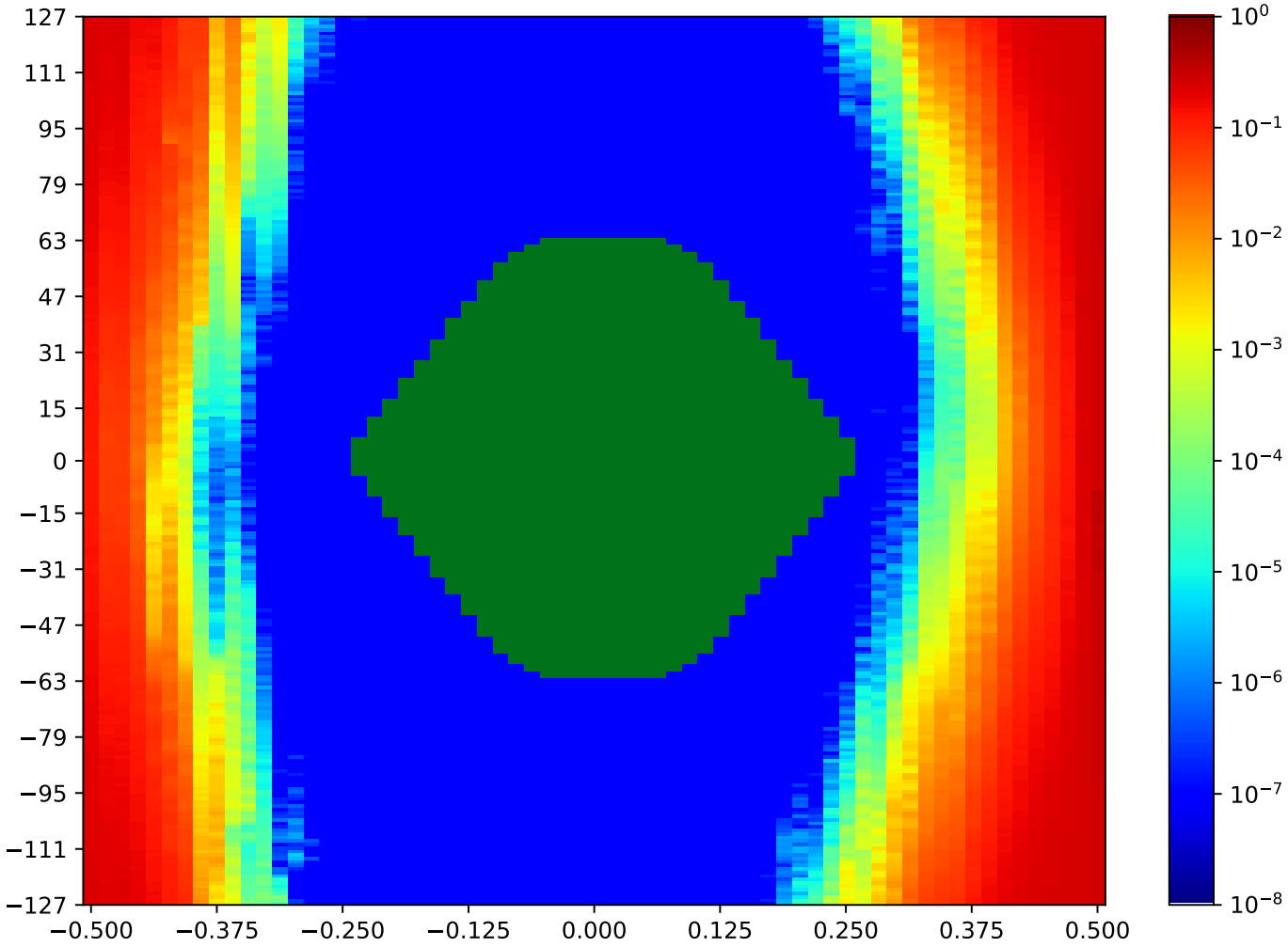


Figure 4.230: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.4 MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Table 4.213: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:55:26		2018-Sep-27 15:55:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9979	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

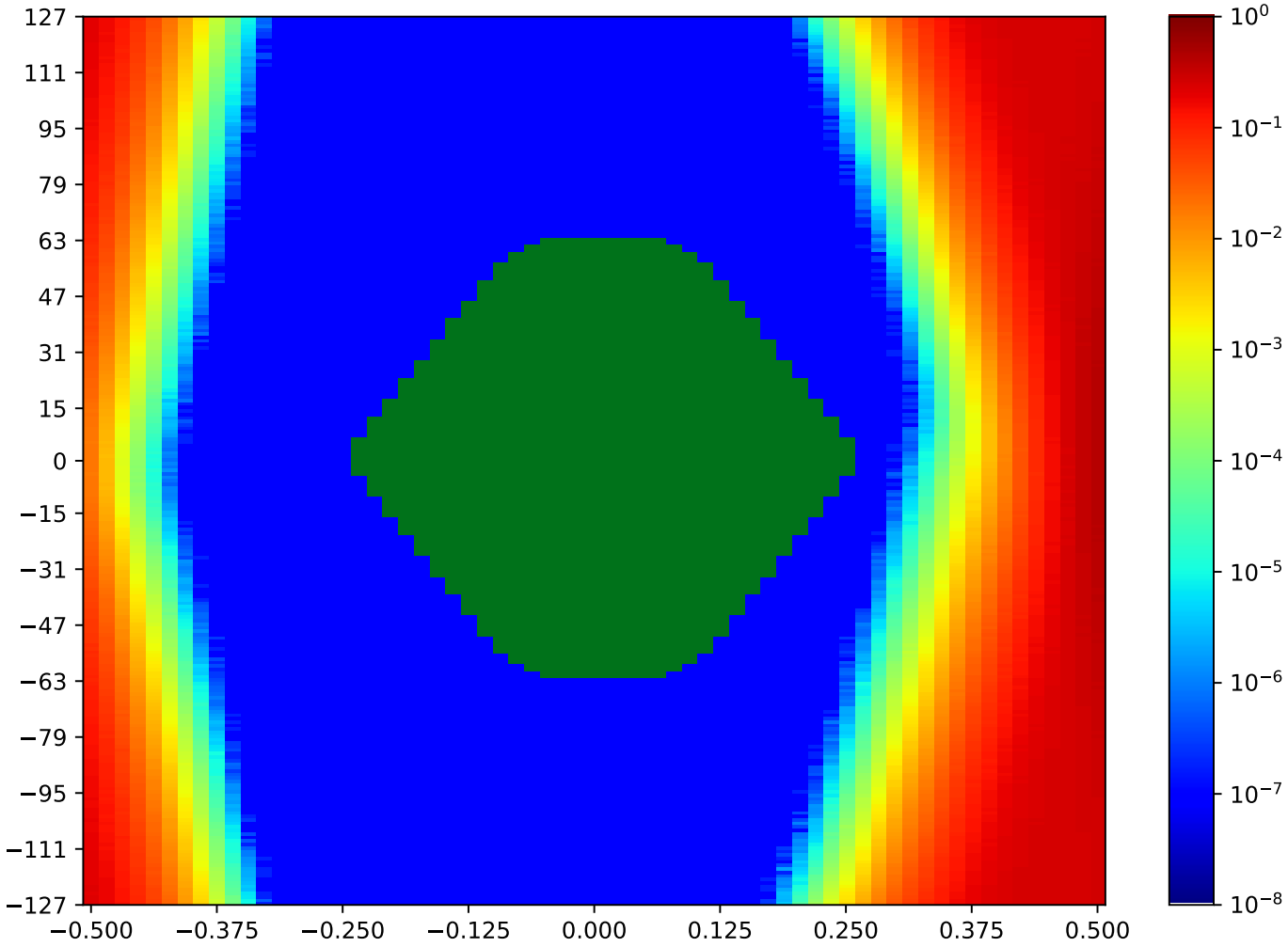


Figure 4.231: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.5 MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Table 4.214: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:58:31		2018-Sep-27 15:58:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8997	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

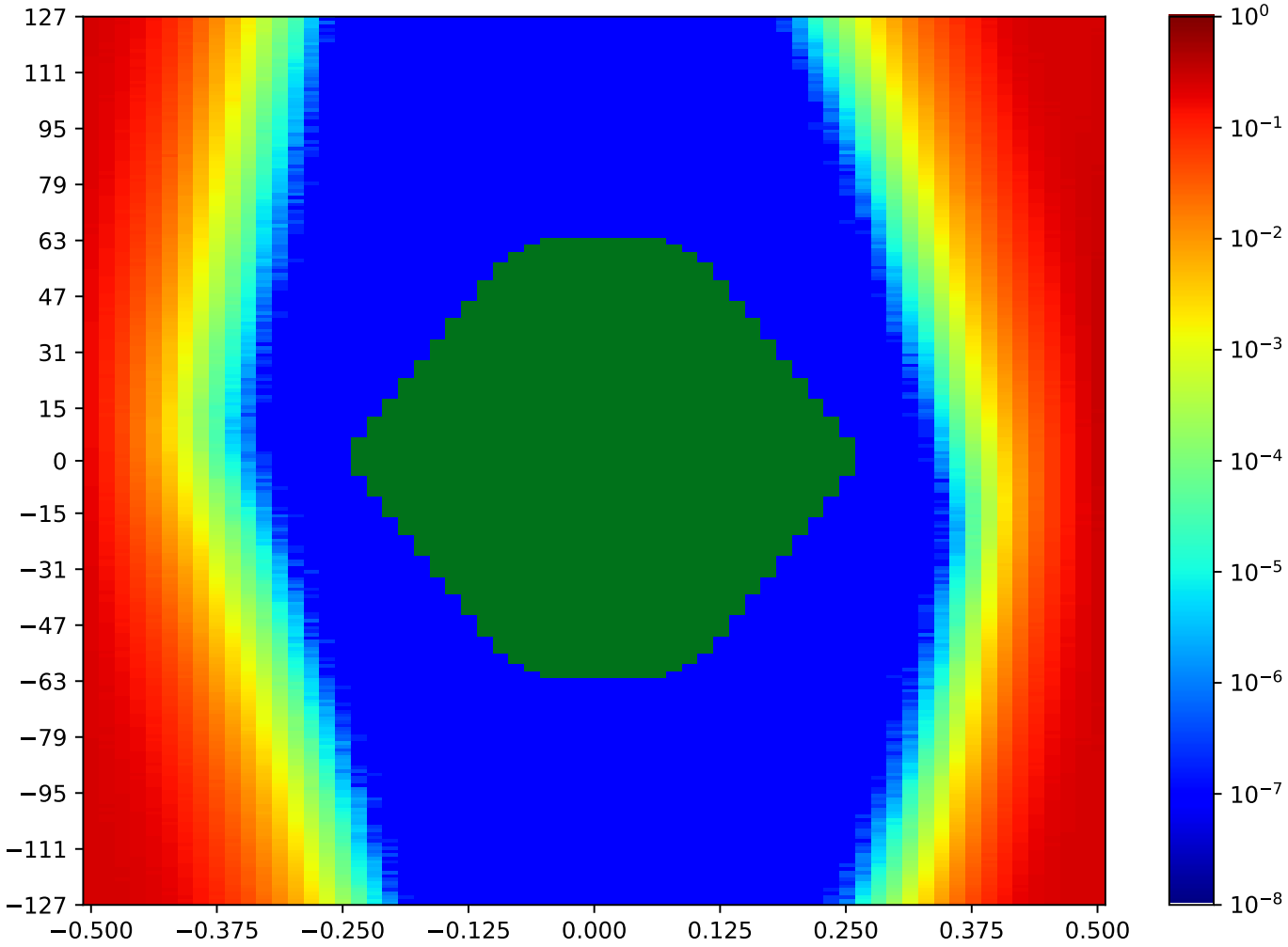


Figure 4.232: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.6 MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Table 4.215: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:56:07		2018-Sep-27 15:56:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9196	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

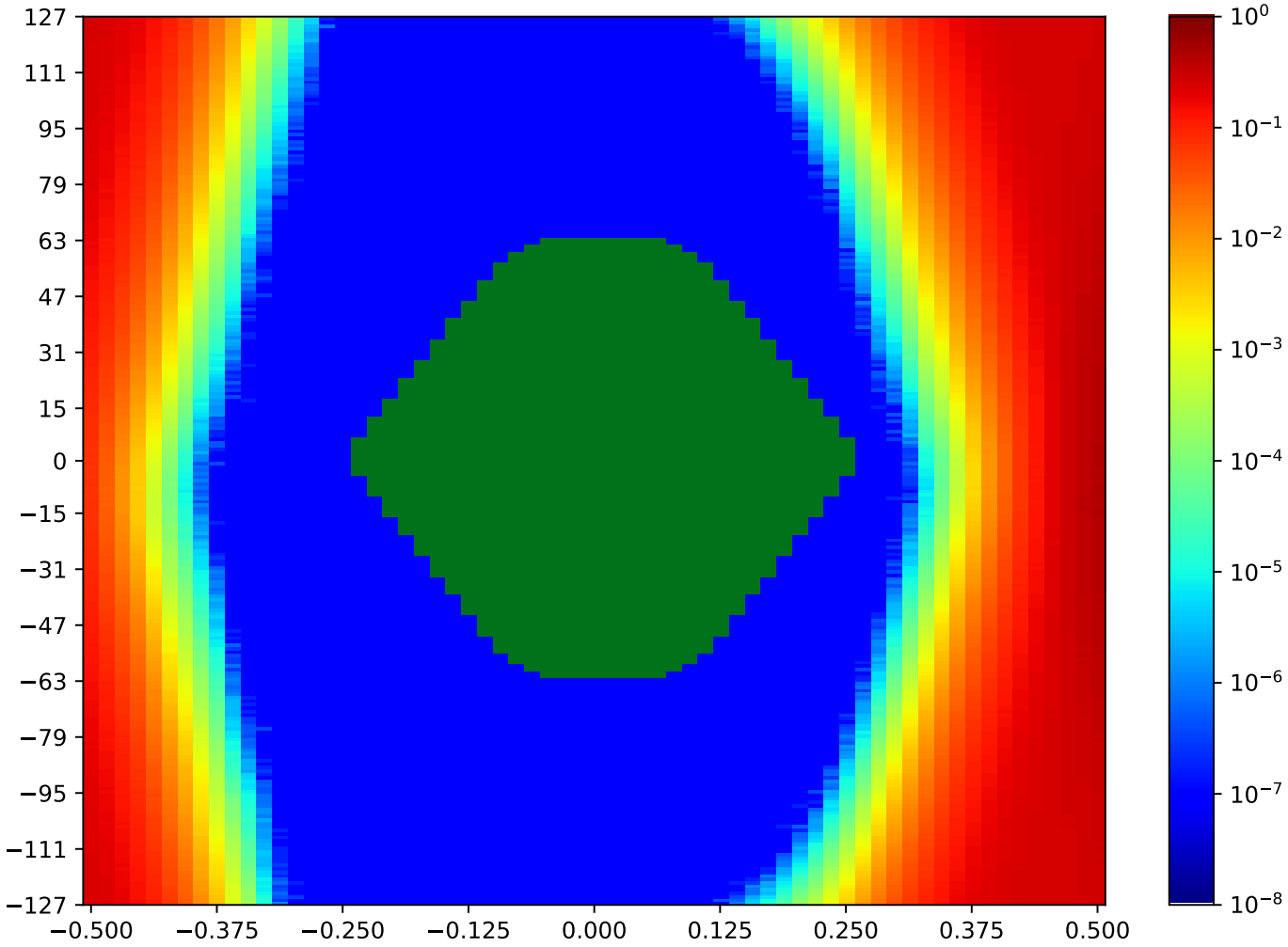


Figure 4.233: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.7 MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Table 4.216: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:59:12		2018-Sep-27 15:59:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9232	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

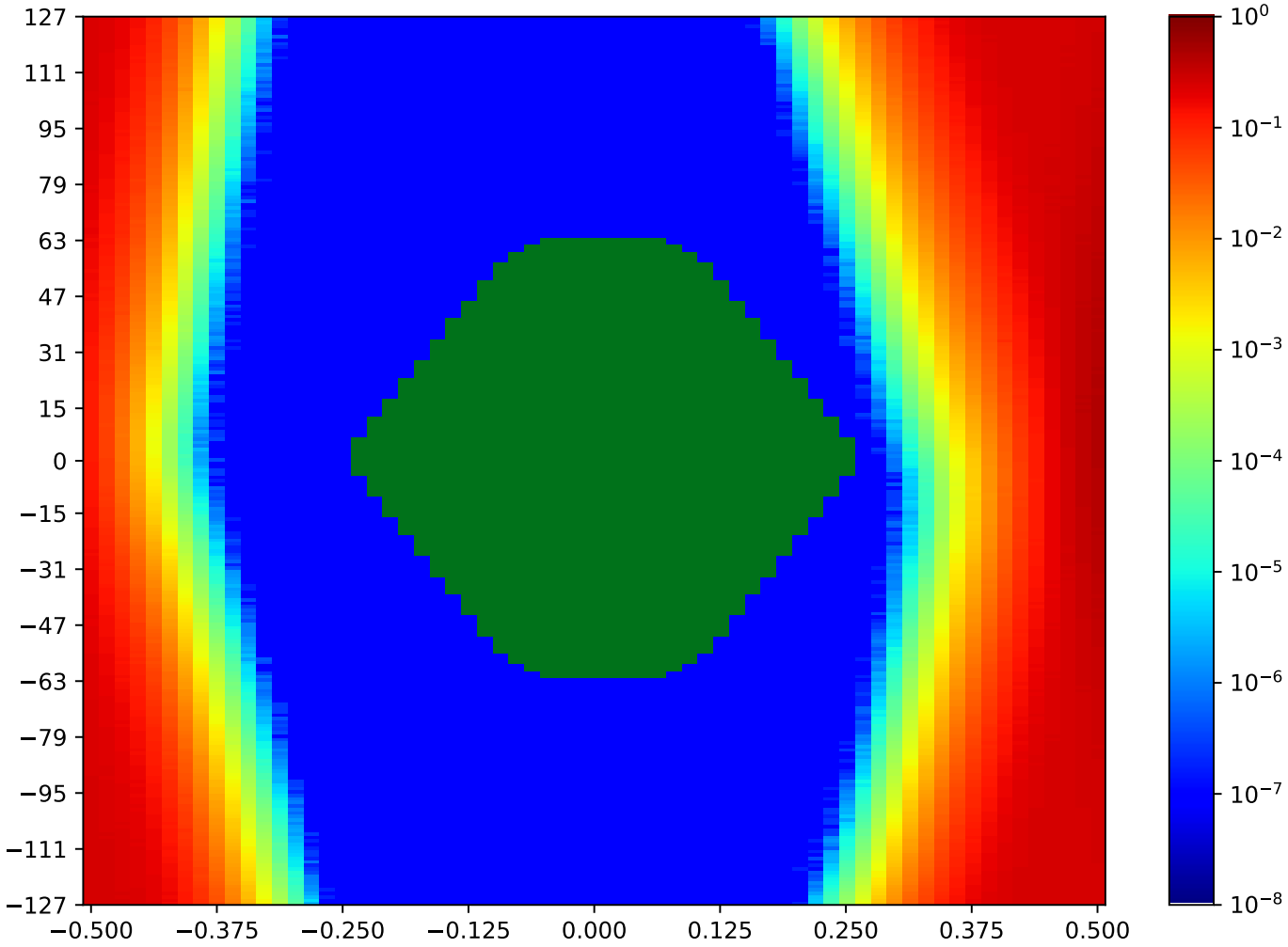


Figure 4.234: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.8 MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Table 4.217: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:56:48		2018-Sep-27 15:57:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9307	44	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

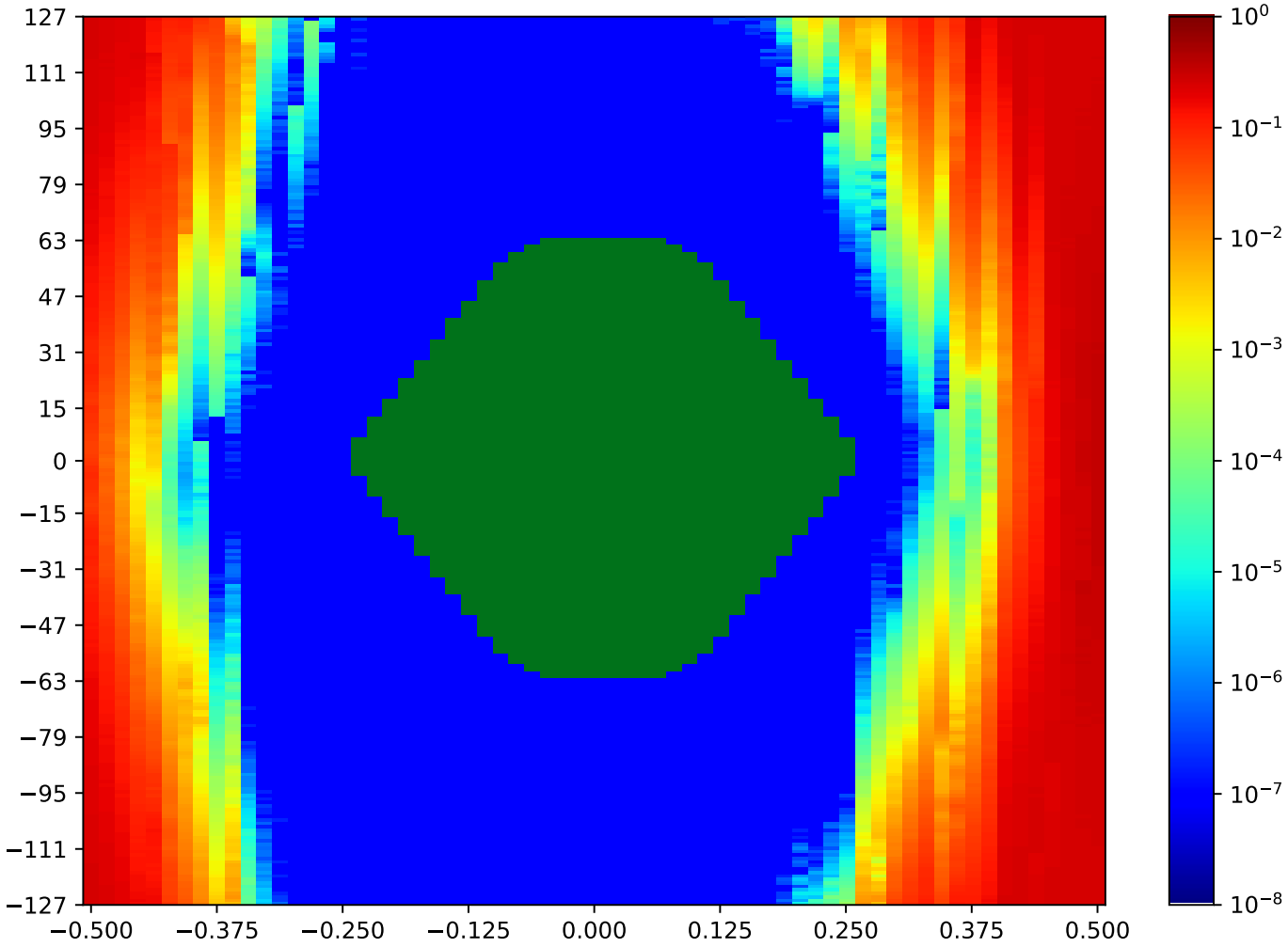


Figure 4.235: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.9 MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Table 4.218: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:58:51		2018-Sep-27 15:59:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9211	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

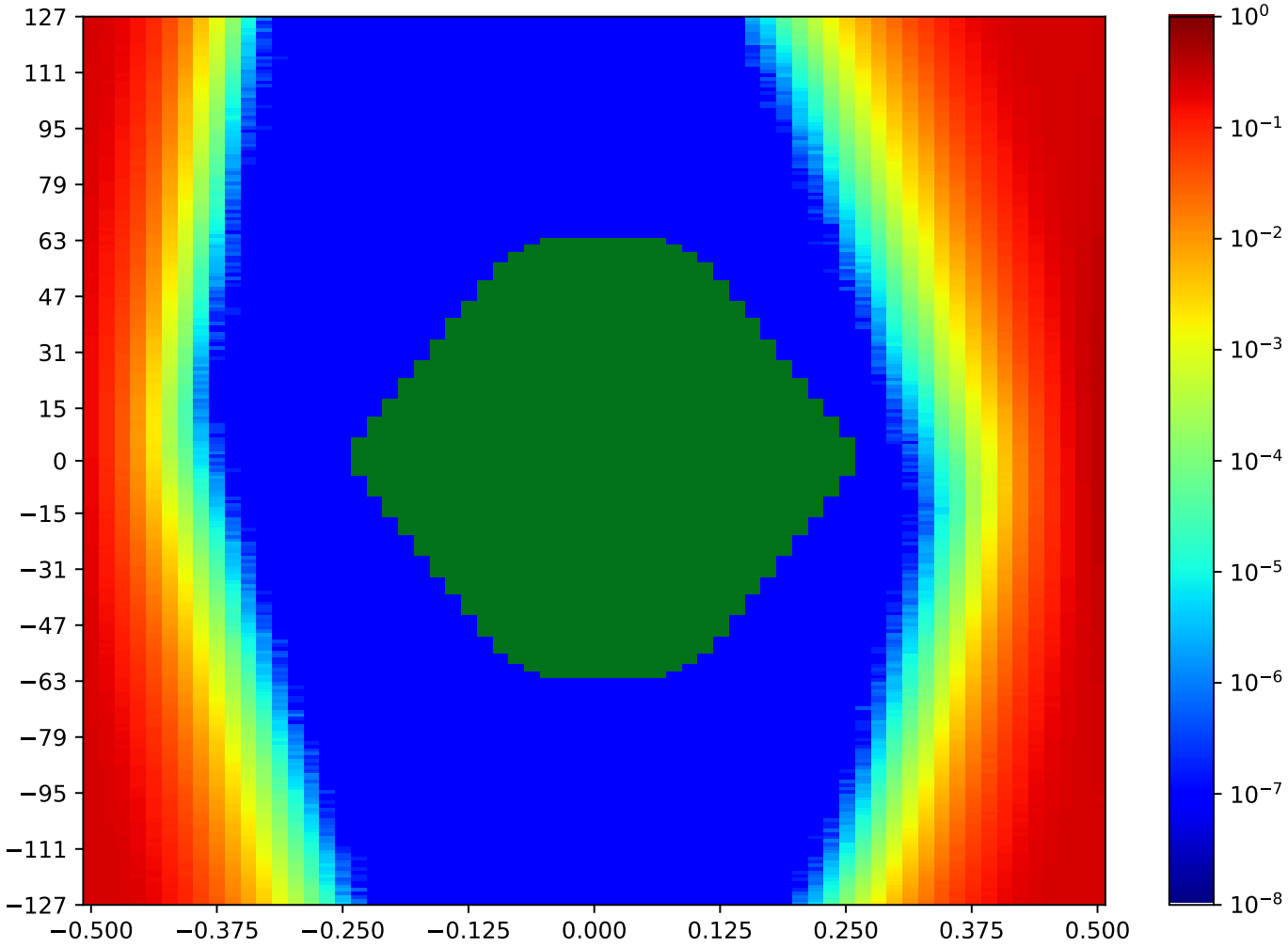


Figure 4.236: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.10 MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Table 4.219: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:57:09		2018-Sep-27 15:57:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9500	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

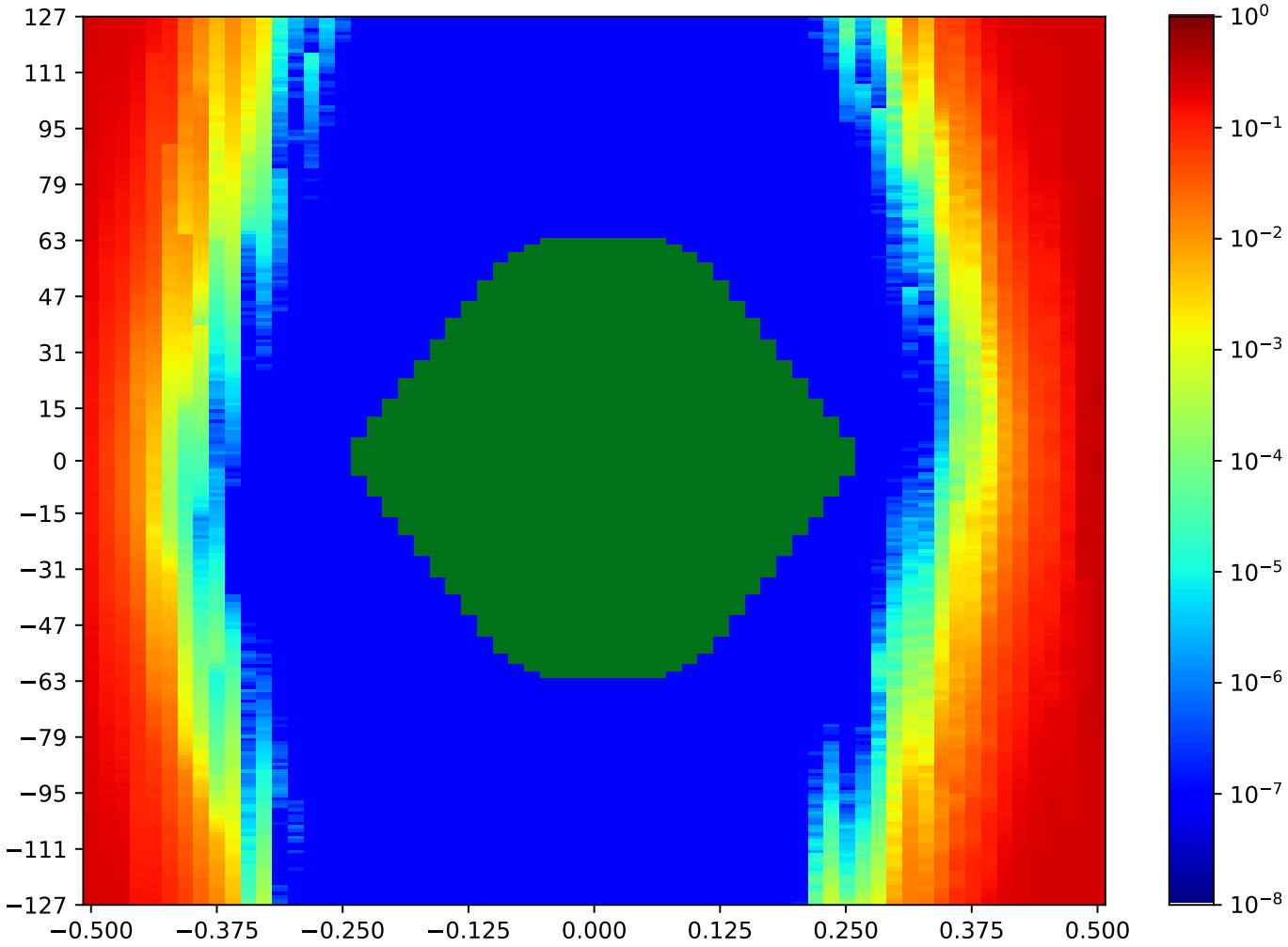


Figure 4.237: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.11 MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Table 4.220: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:58:10		2018-Sep-27 15:58:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9294	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

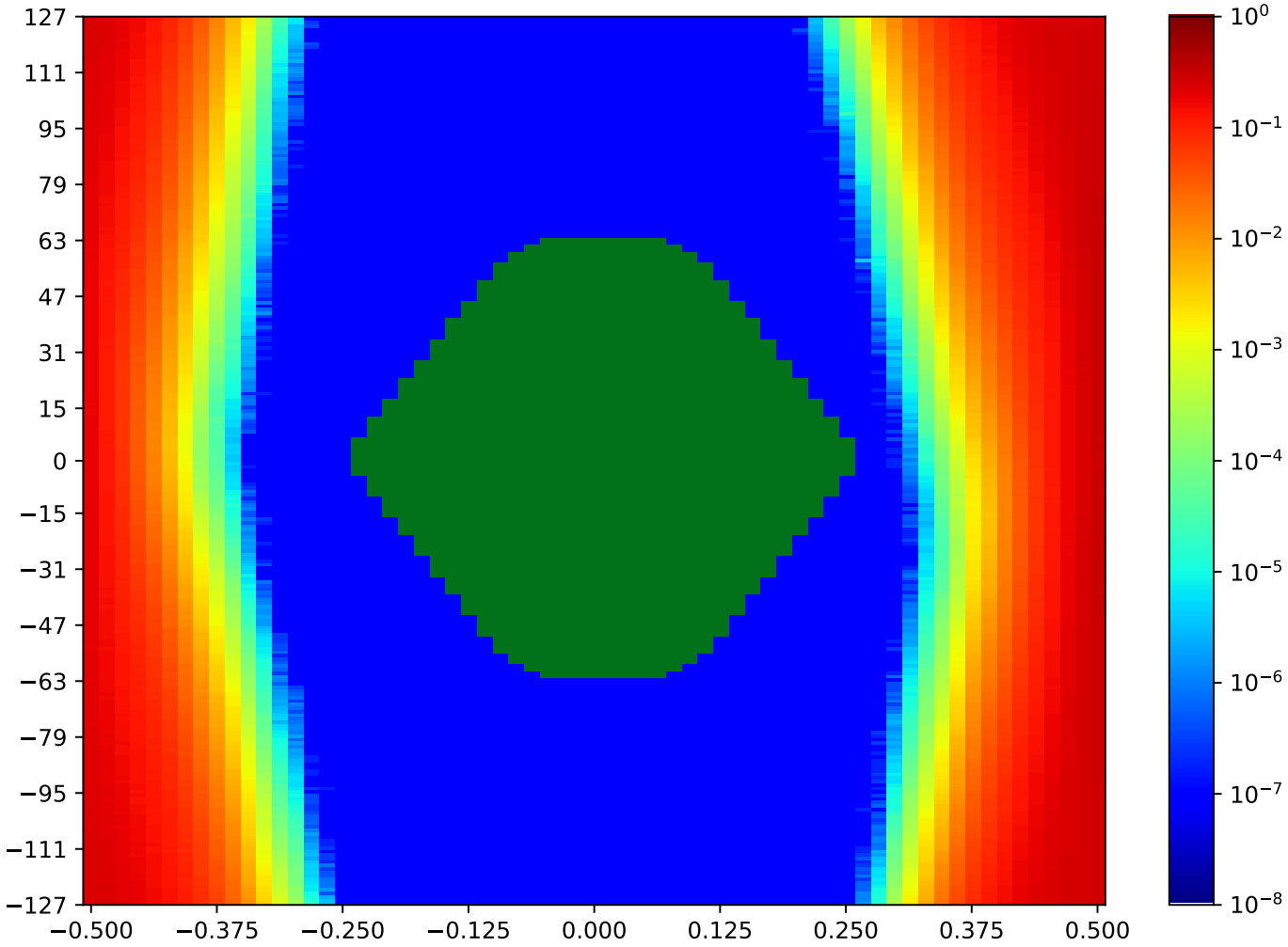


Figure 4.238: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.18.12 MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Table 4.221: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:57:50		2018-Sep-27 15:58:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9660	43	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

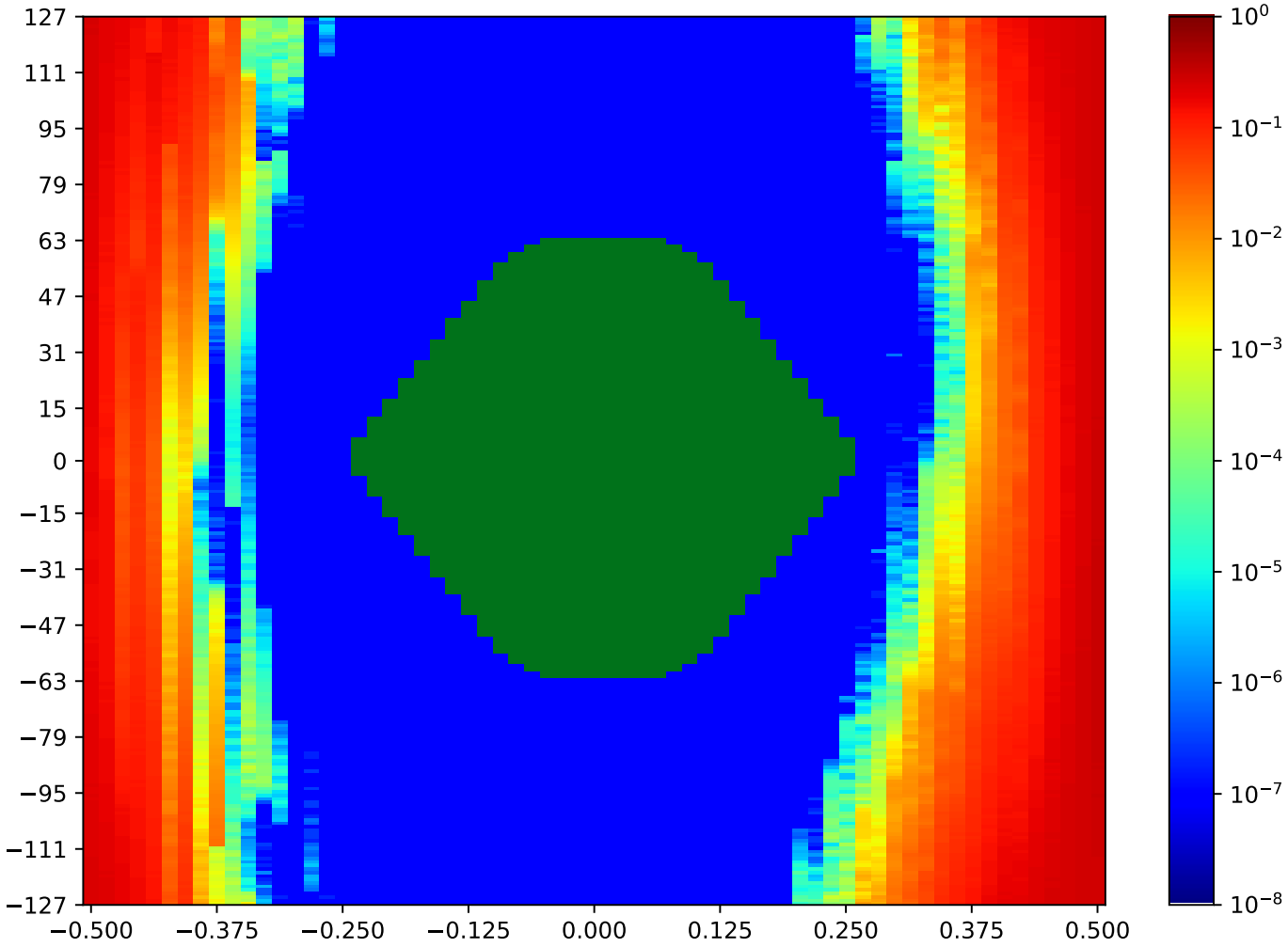


Figure 4.239: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19 MSP_A TX1 MSP_C RX12 Minipod Loopback

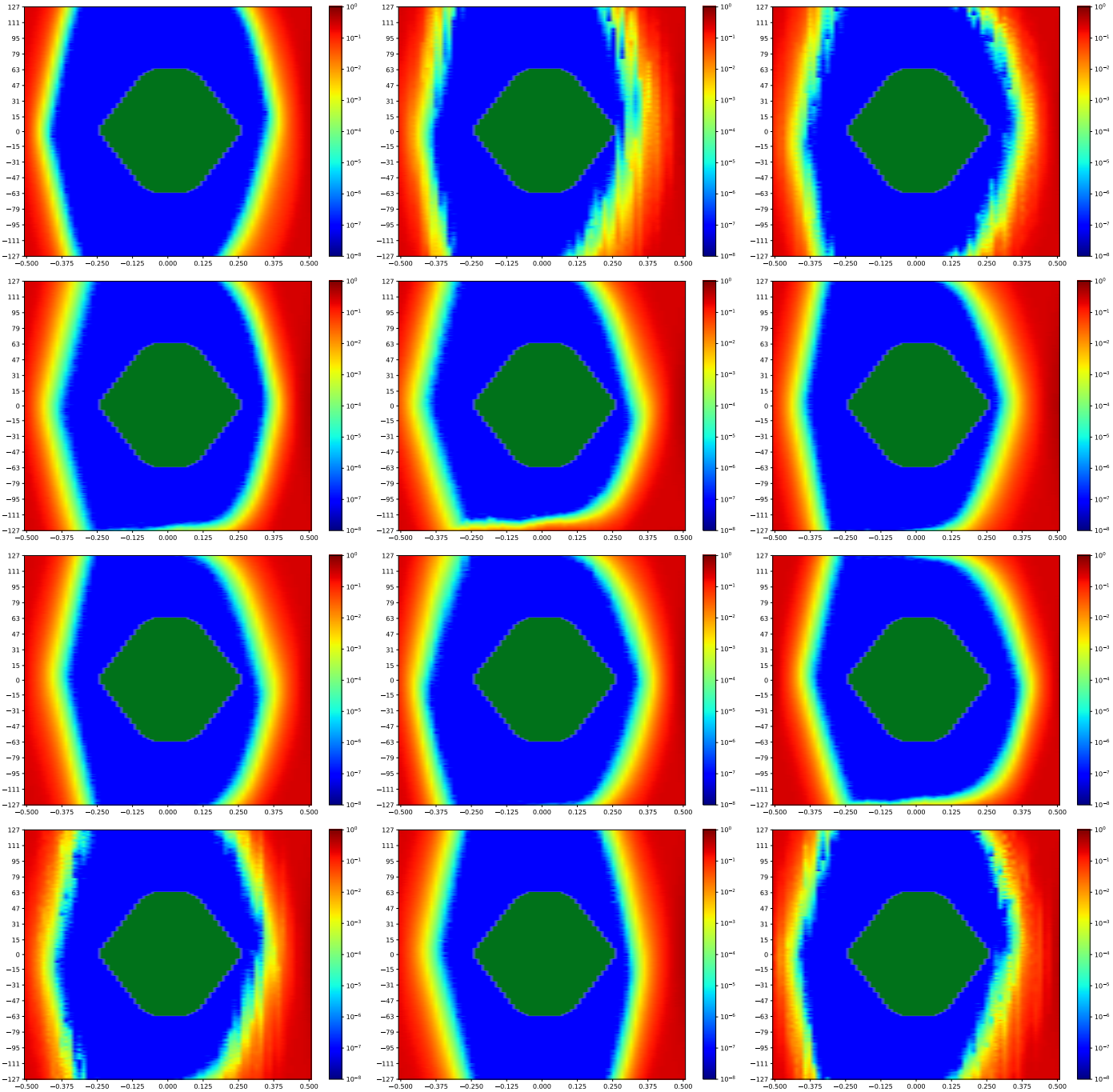


Figure 4.240: MSP_A TX1 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.253.

4.19.1 MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Table 4.222: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:23:29		2018-Sep-27 15:23:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10244	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

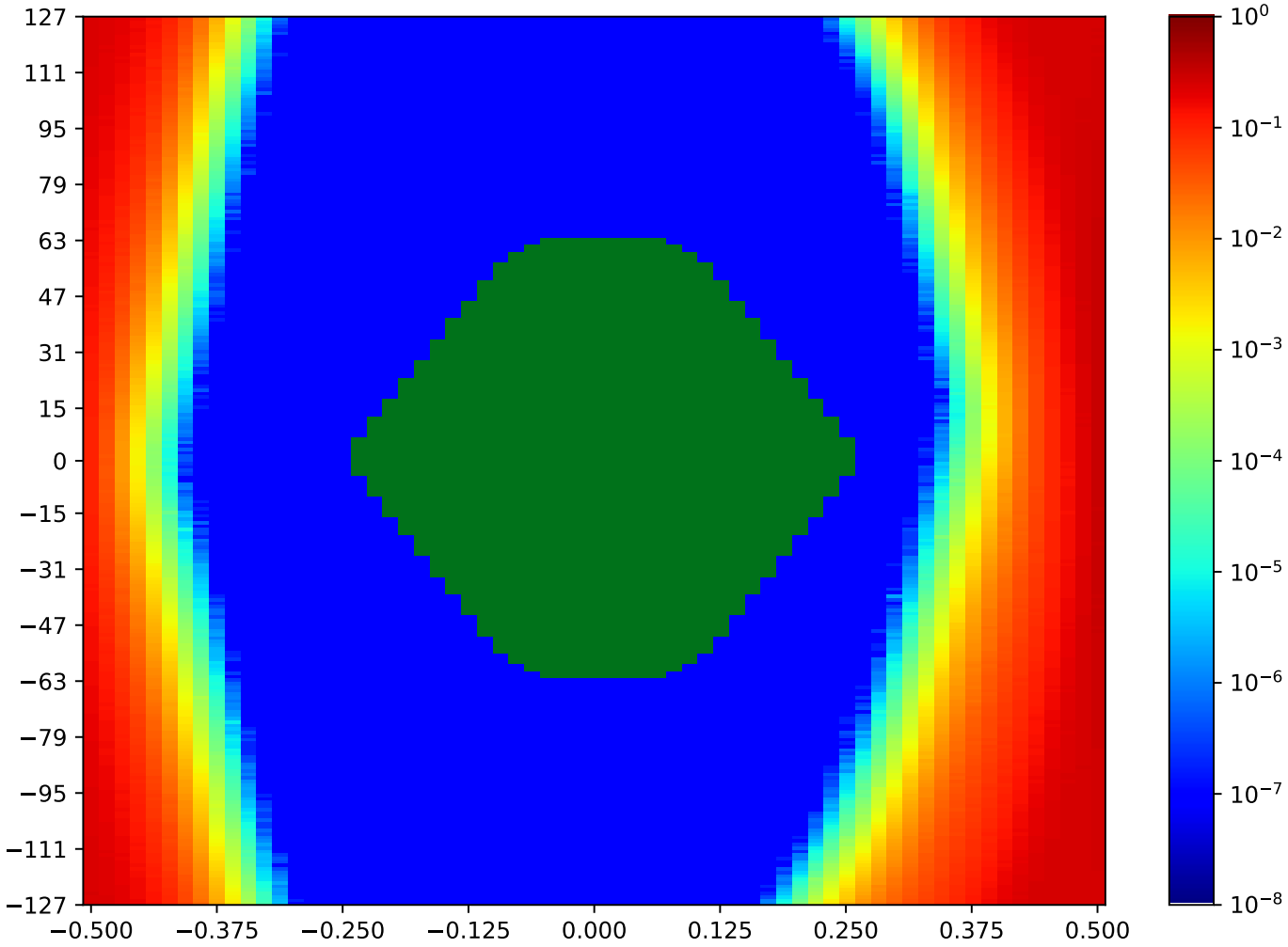


Figure 4.241: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.2 MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Table 4.223: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:24:10		2018-Sep-27 15:24:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8915	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

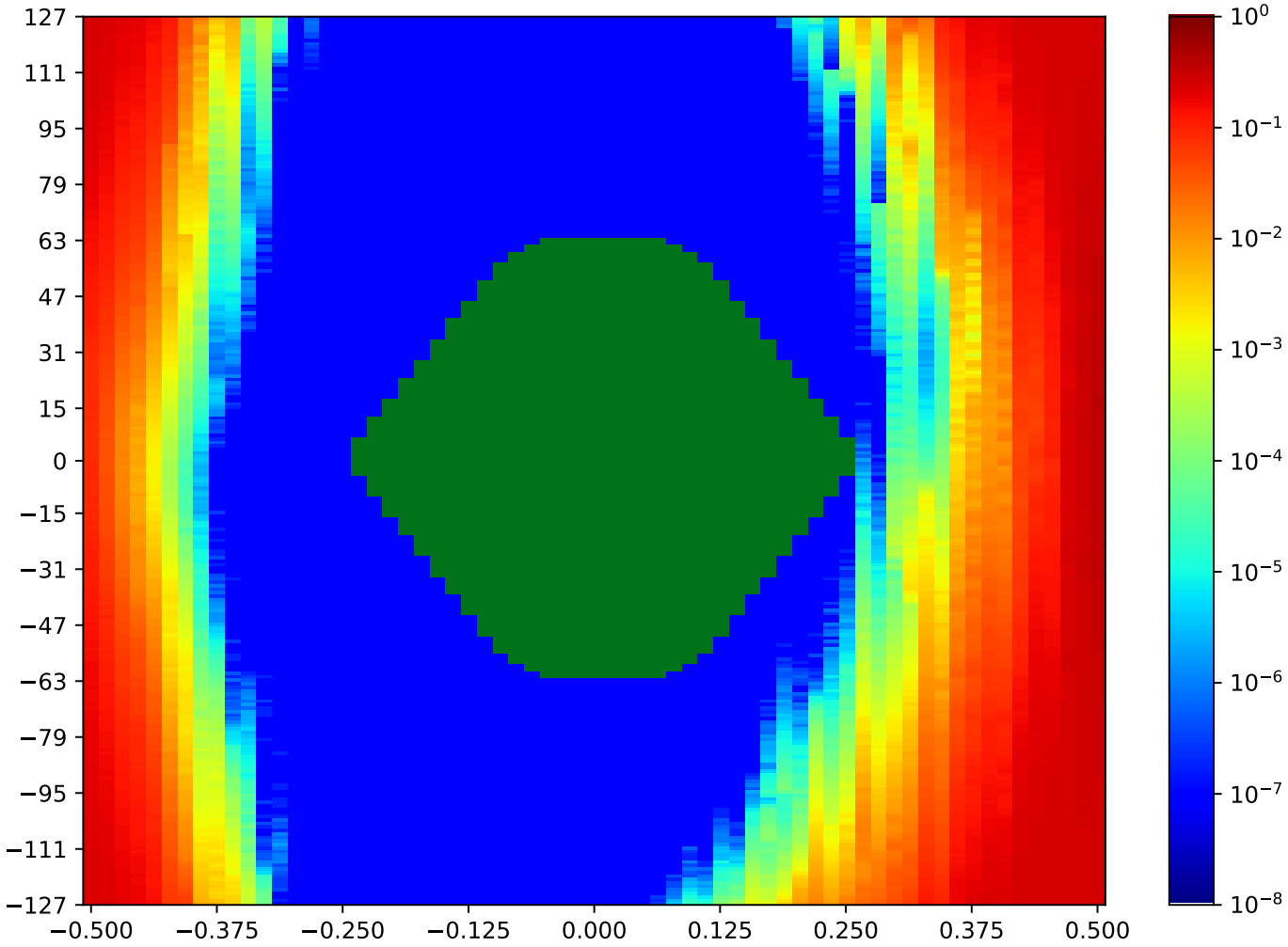


Figure 4.242: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.3 MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Table 4.224: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:24:30		2018-Sep-27 15:24:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9255	43	64.62%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

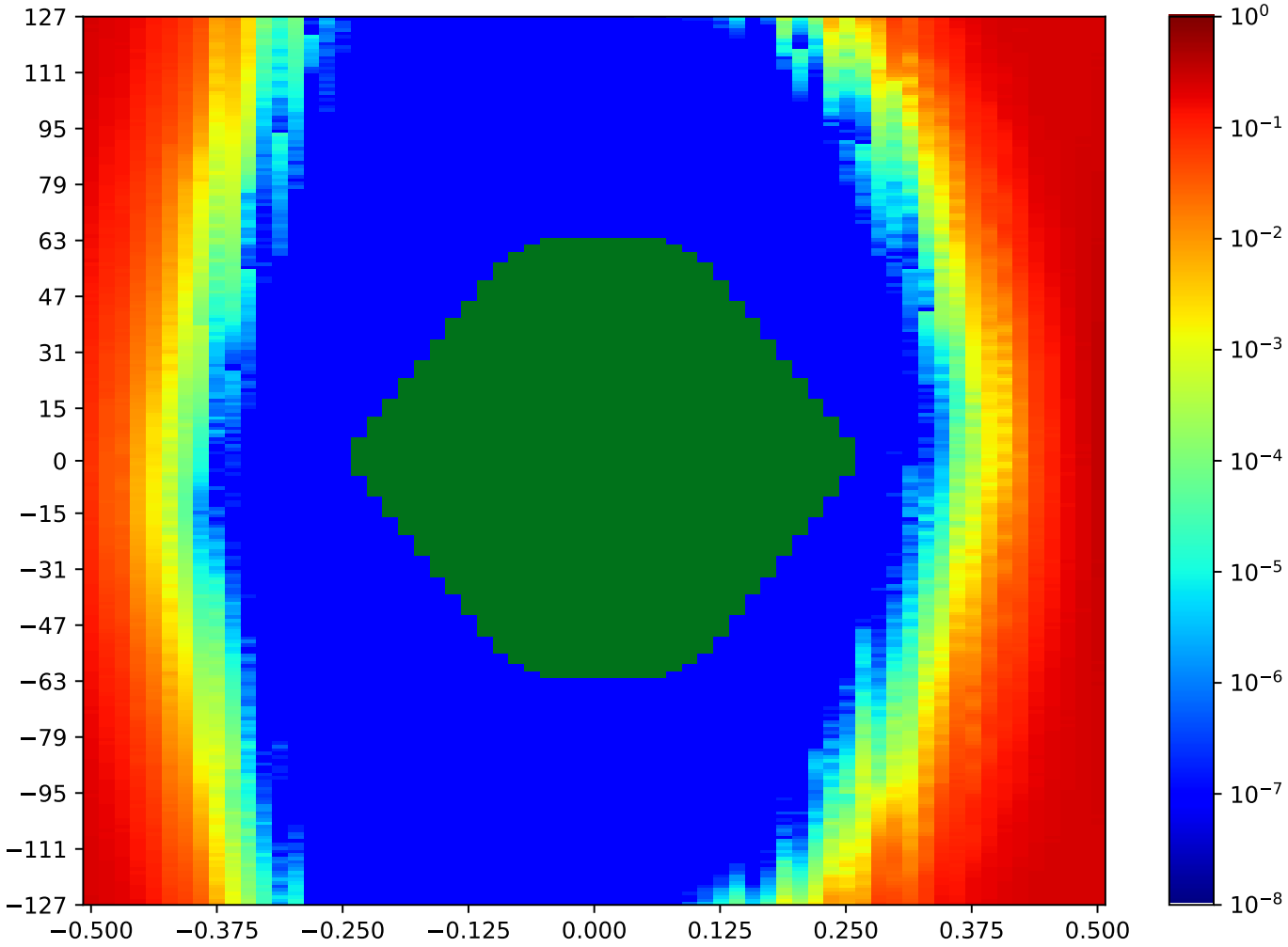


Figure 4.243: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.4 MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Table 4.225: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:22:48		2018-Sep-27 15:23:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9079	44	67.69%	246	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

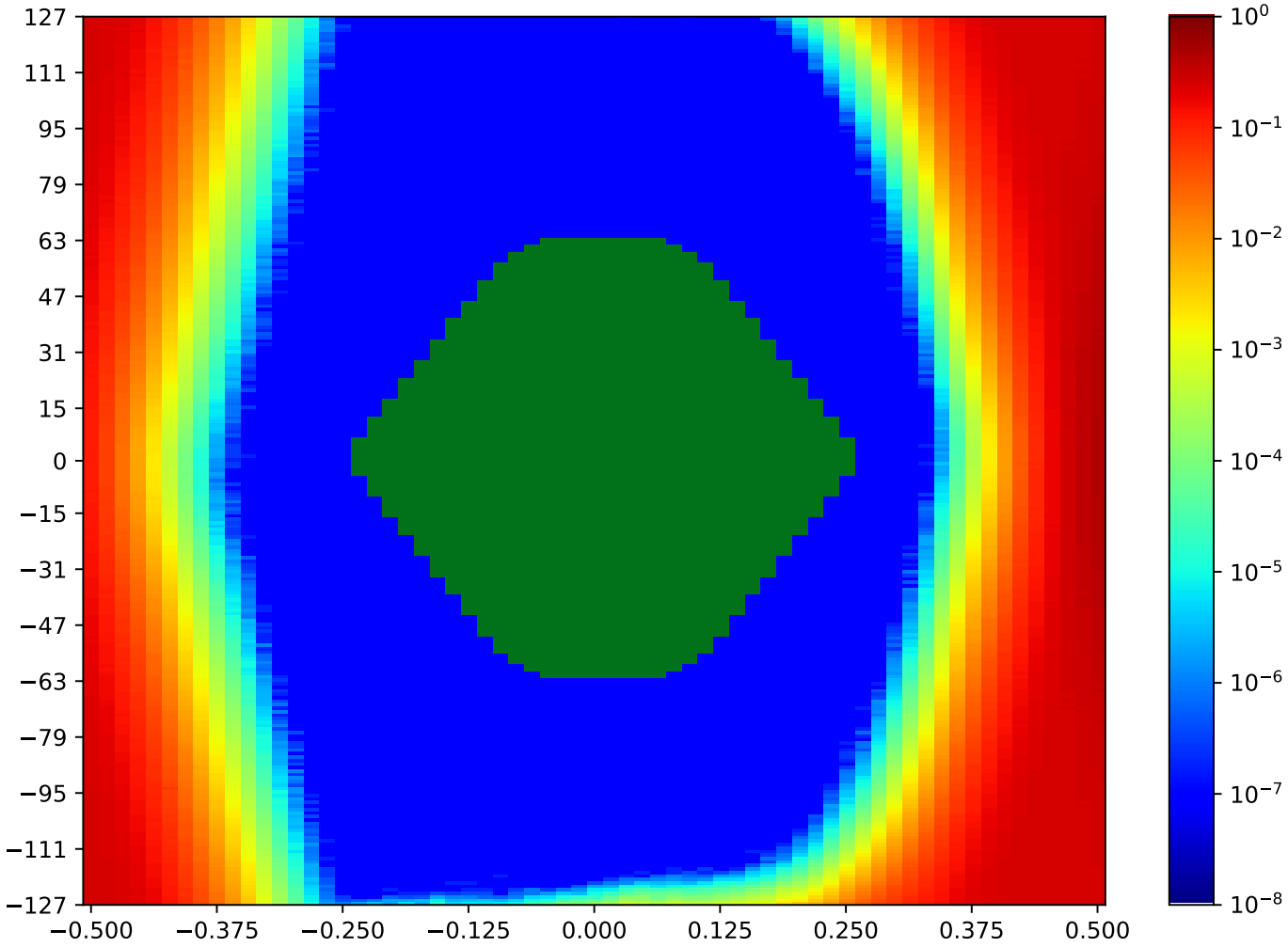


Figure 4.244: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.5 MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Table 4.226: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:25:31		2018-Sep-27 15:25:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8343	41	63.08%	237	92.94%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

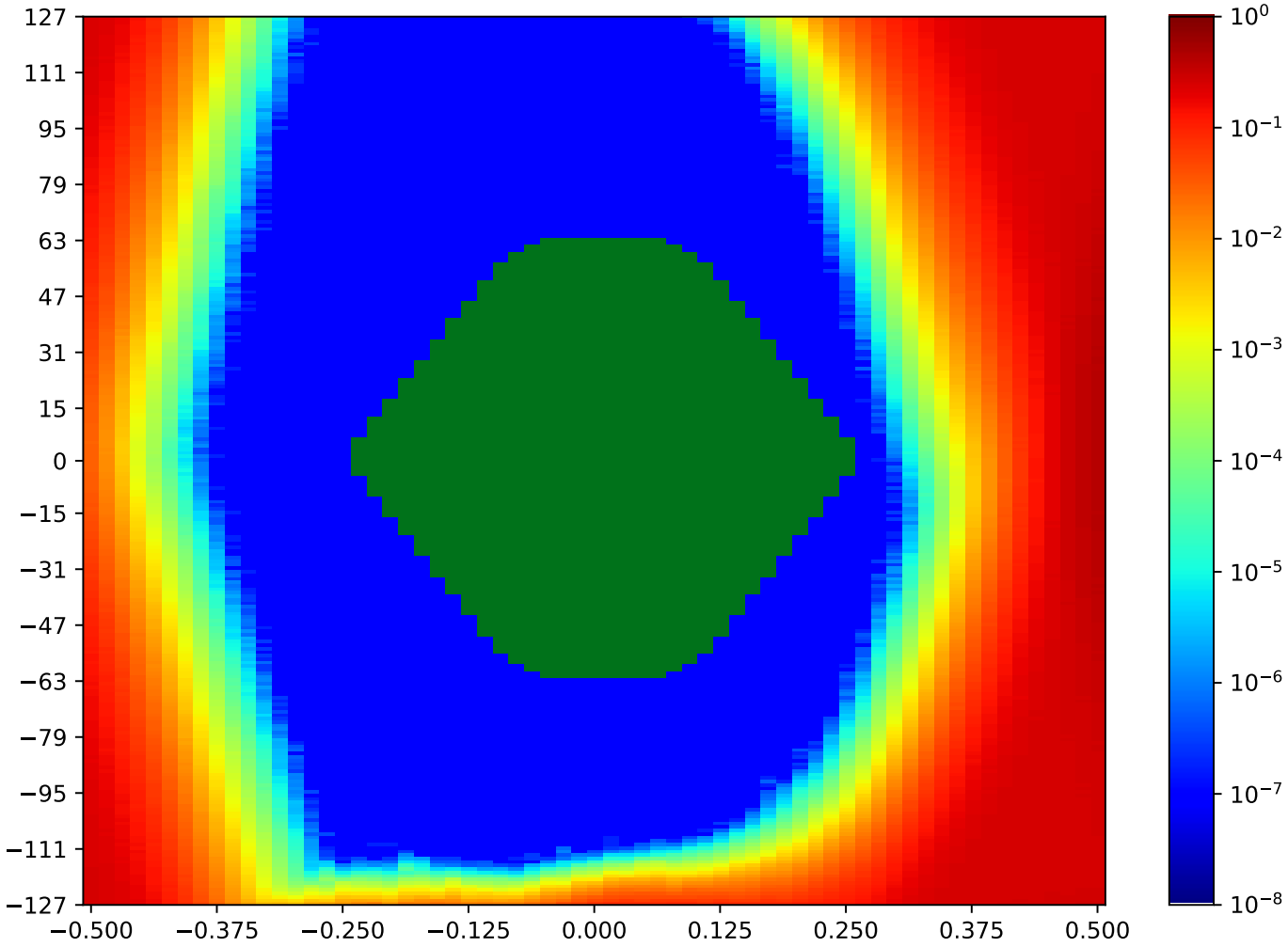


Figure 4.245: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.6 MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Table 4.227: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:22:28		2018-Sep-27 15:22:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8608	41	63.08%	252	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

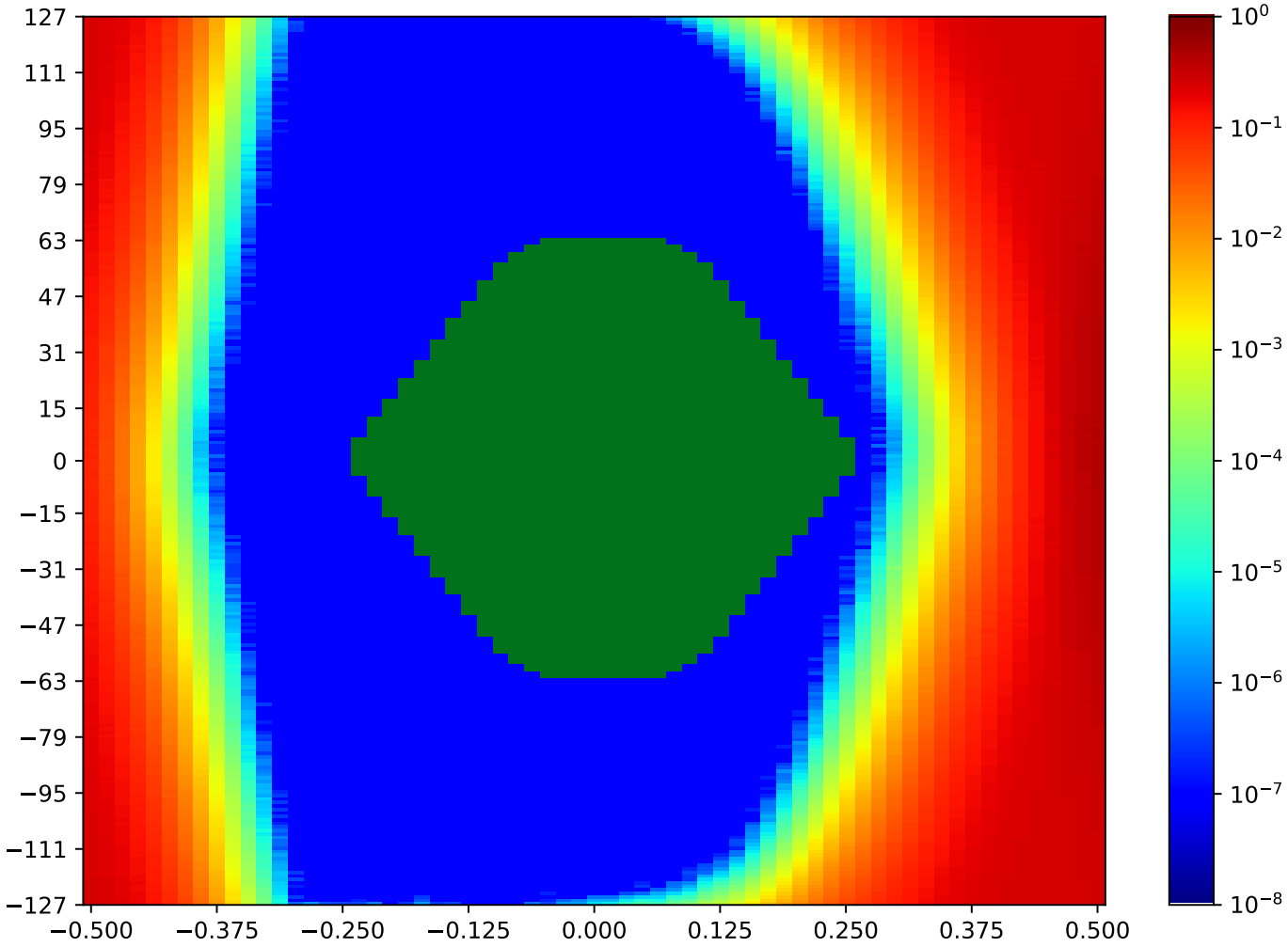


Figure 4.246: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.7 MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Table 4.228: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:26:12		2018-Sep-27 15:26:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8452	41	63.08%	255	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

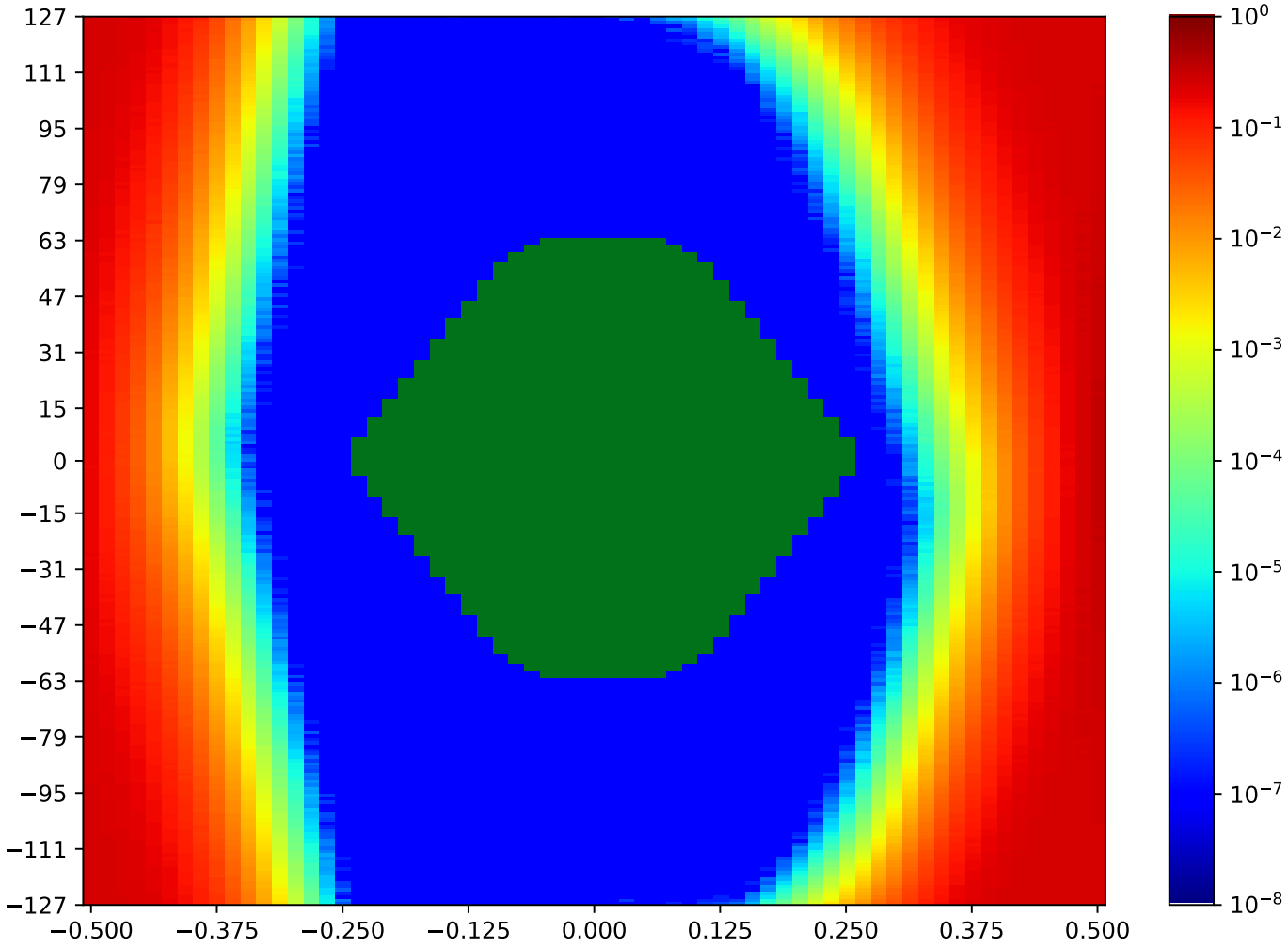


Figure 4.247: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.8 MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Table 4.229: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:23:09		2018-Sep-27 15:23:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9216	44	67.69%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

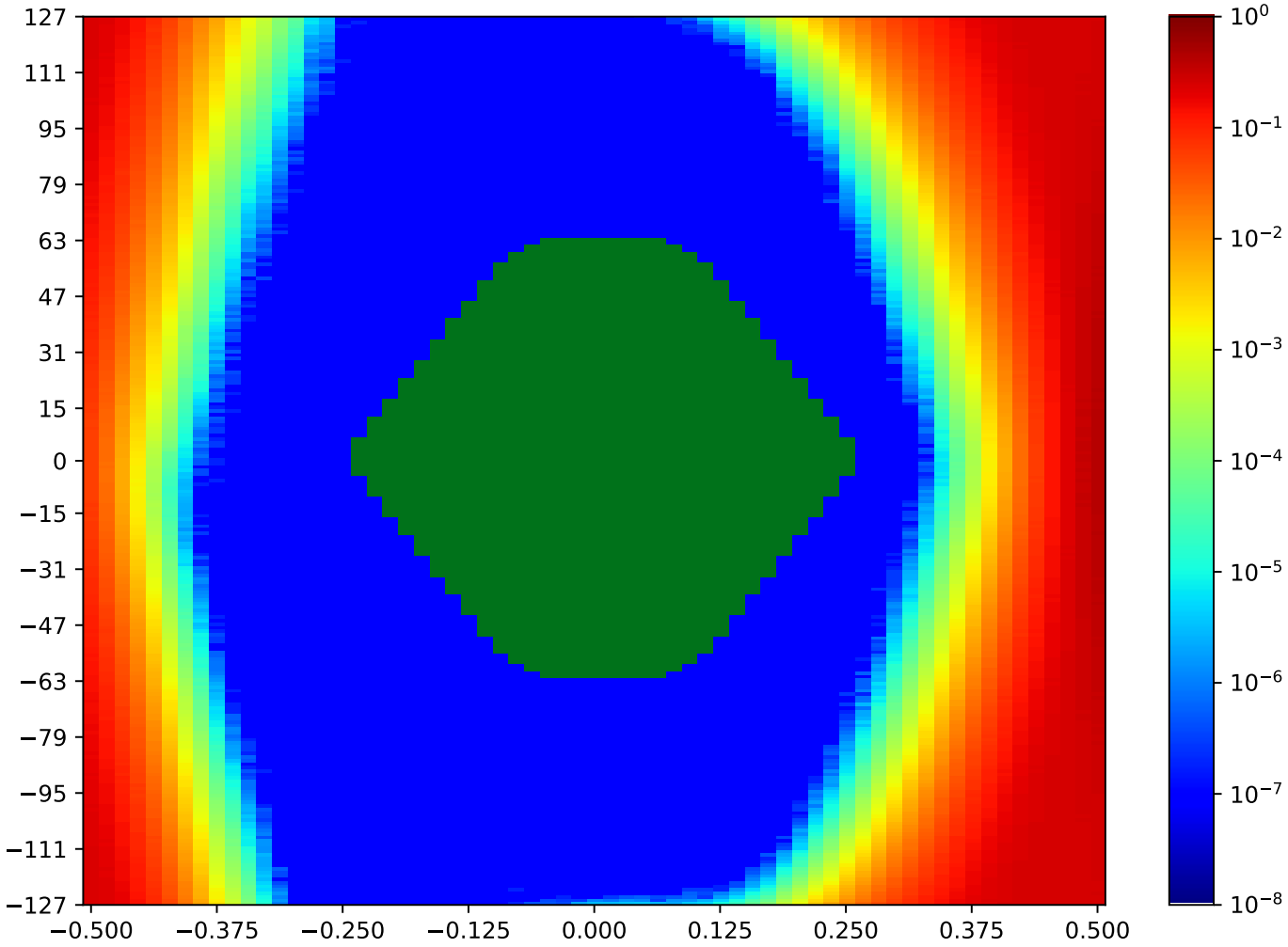


Figure 4.248: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.9 MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Table 4.230: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:25:52		2018-Sep-27 15:26:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8483	43	66.15%	239	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

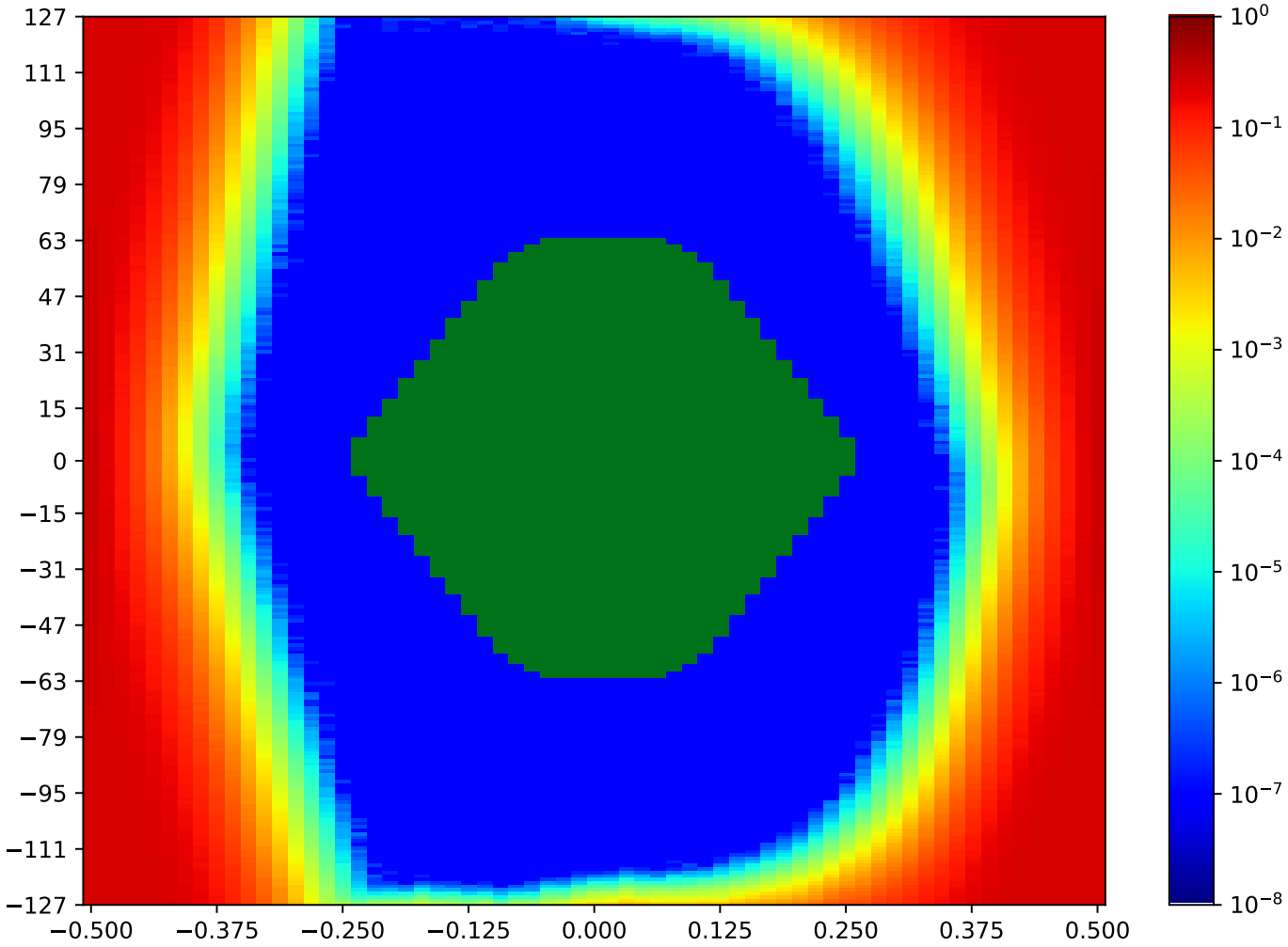


Figure 4.249: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.10 MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Table 4.231: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:23:50		2018-Sep-27 15:24:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9024	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

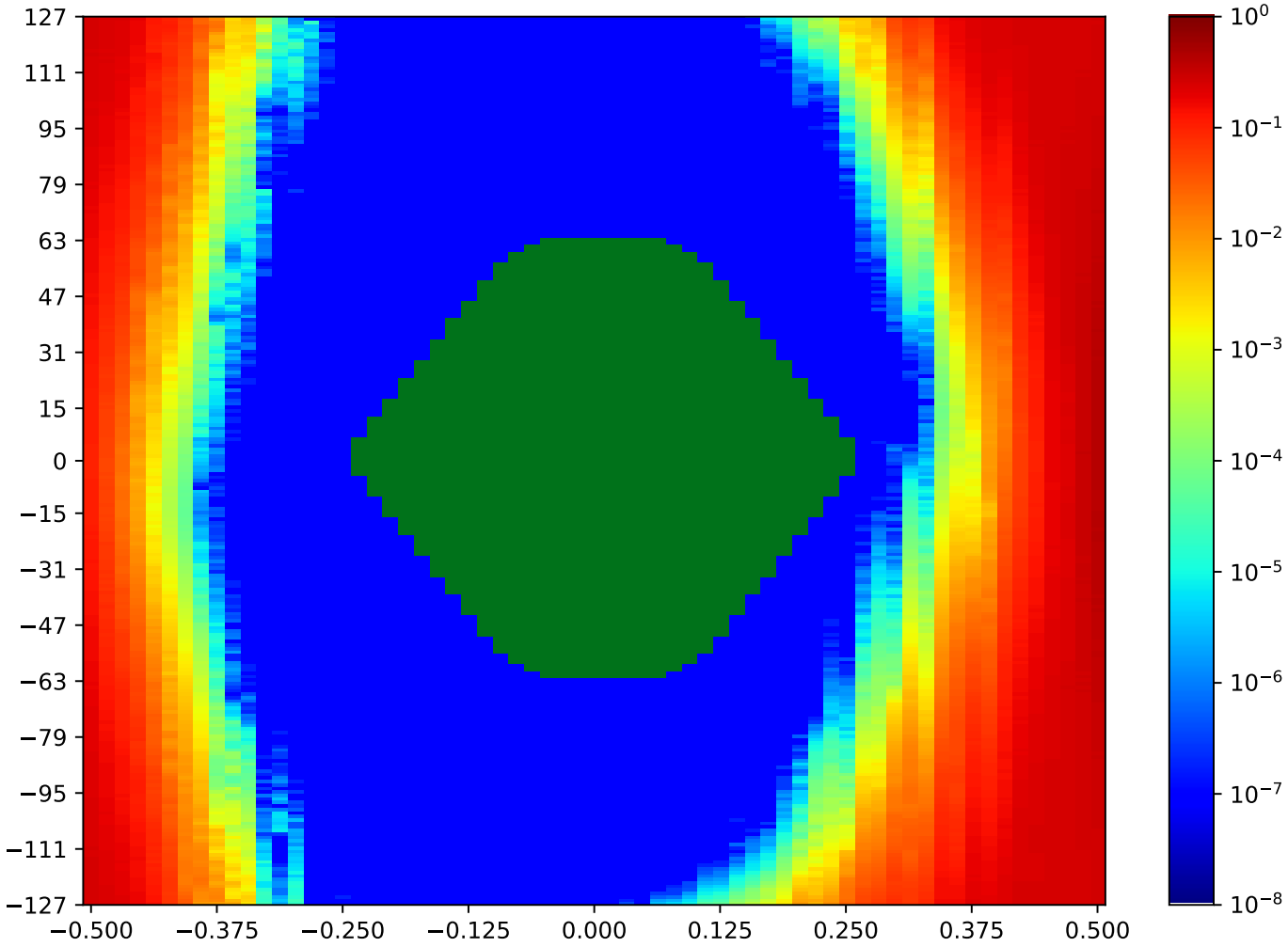


Figure 4.250: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.11 MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Table 4.232: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:25:11		2018-Sep-27 15:25:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8855	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

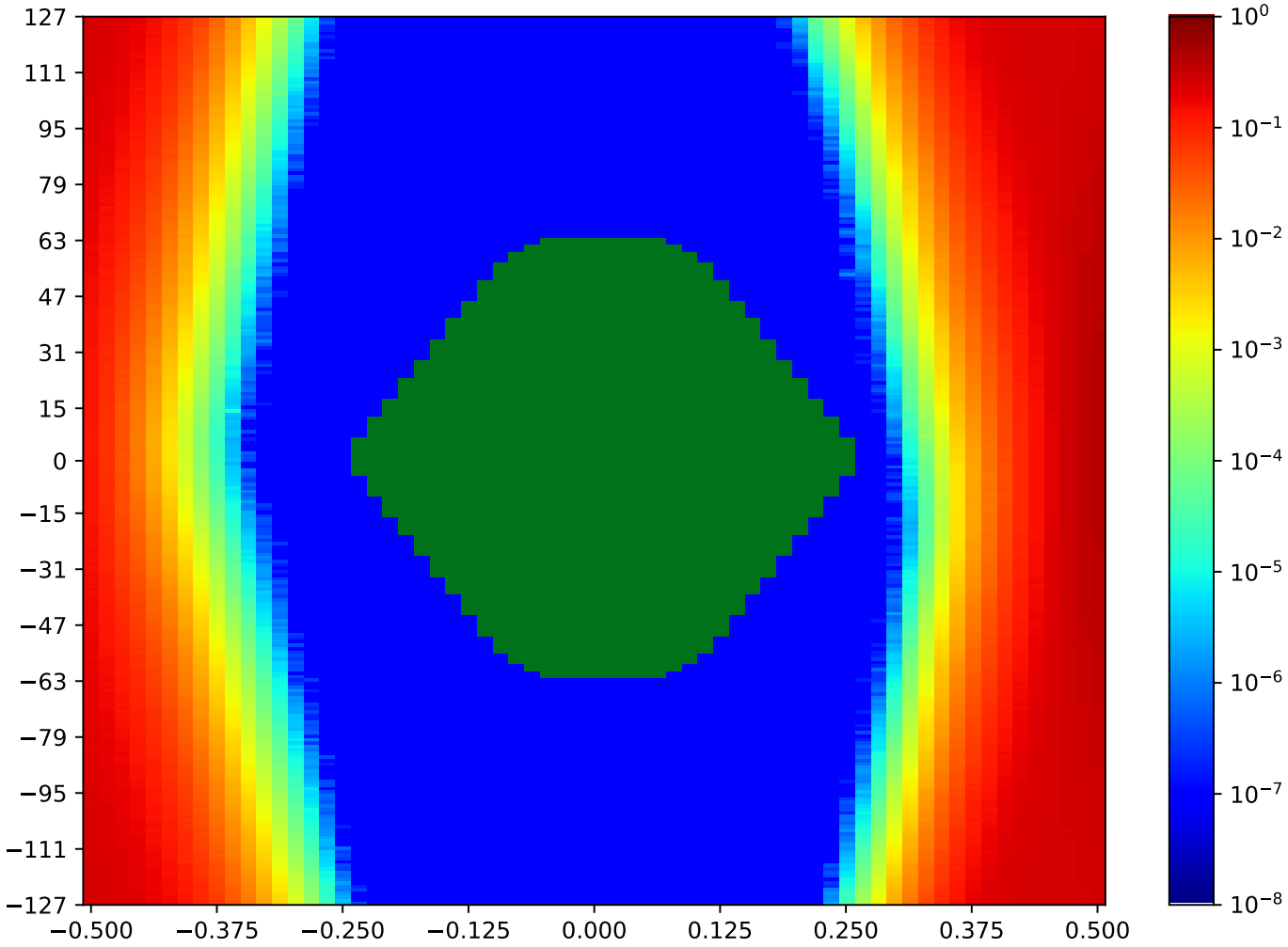


Figure 4.251: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.19.12 MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Table 4.233: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:24:51		2018-Sep-27 15:25:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9552	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

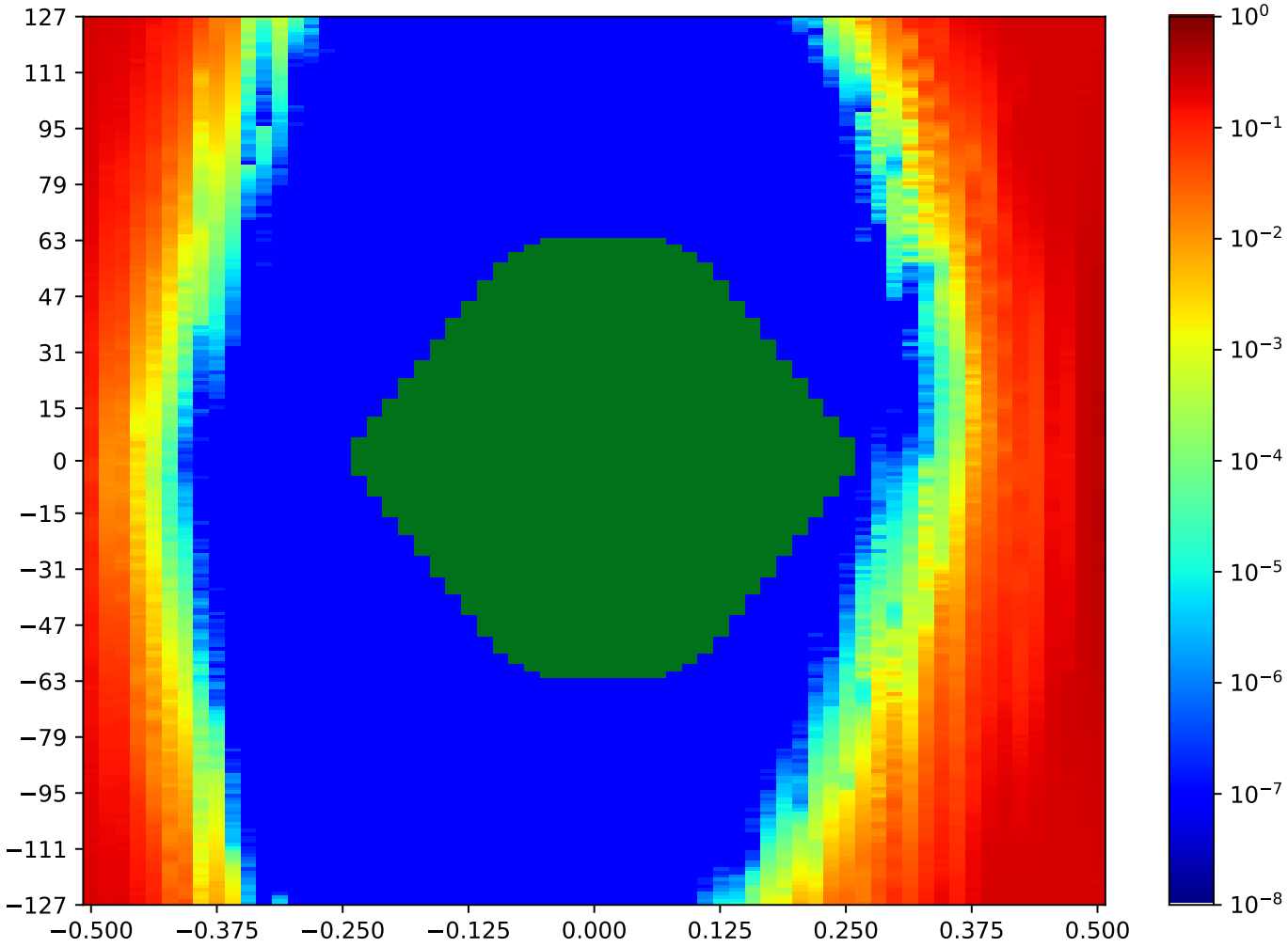


Figure 4.252: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20 MSP_A TX2 MSP_C RX13 Minipod Loopback

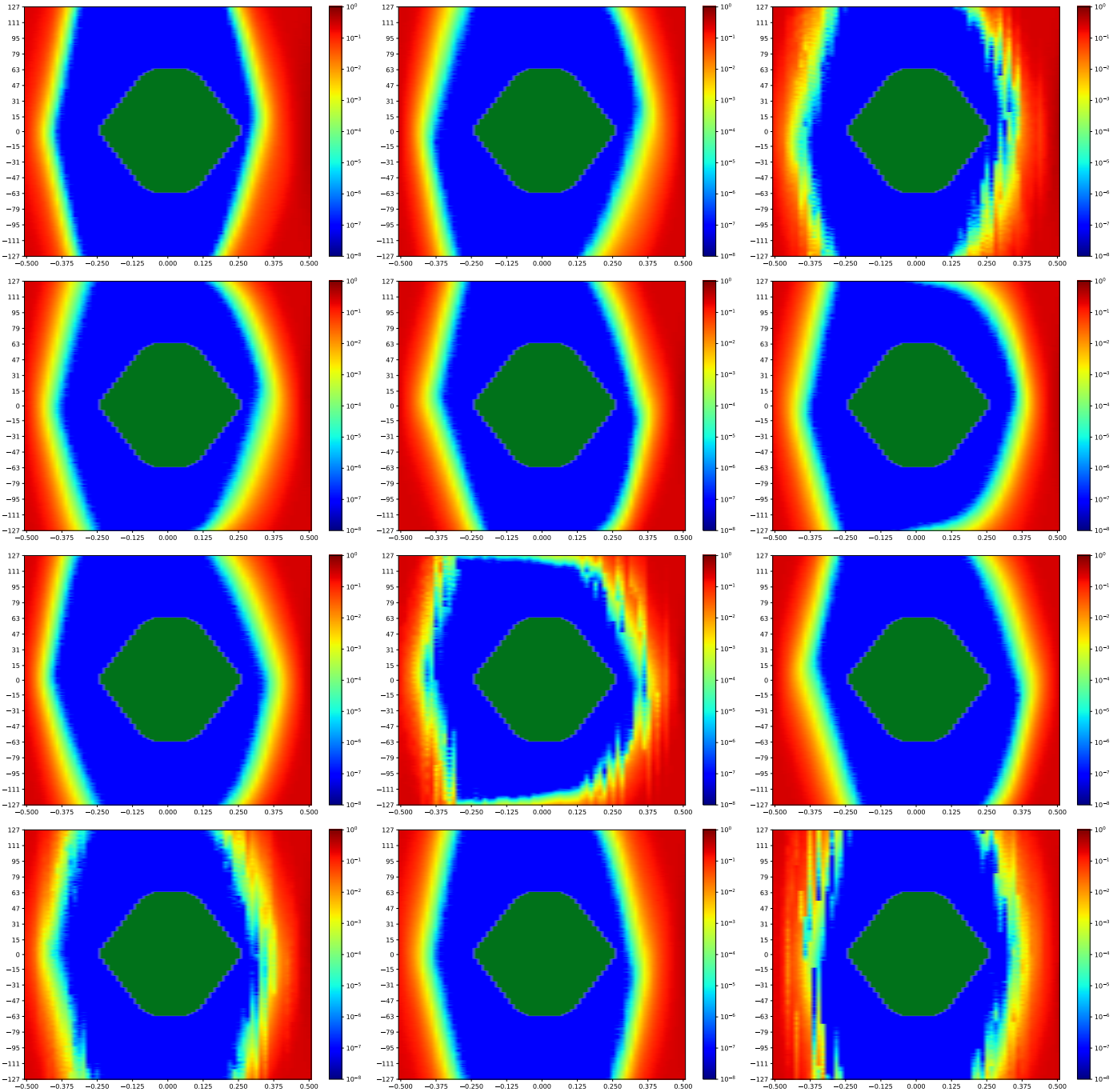


Figure 4.253: MSP_A TX2 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.266.

4.20.1 MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Table 4.234: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:27:33		2018-Sep-27 15:27:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9351	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

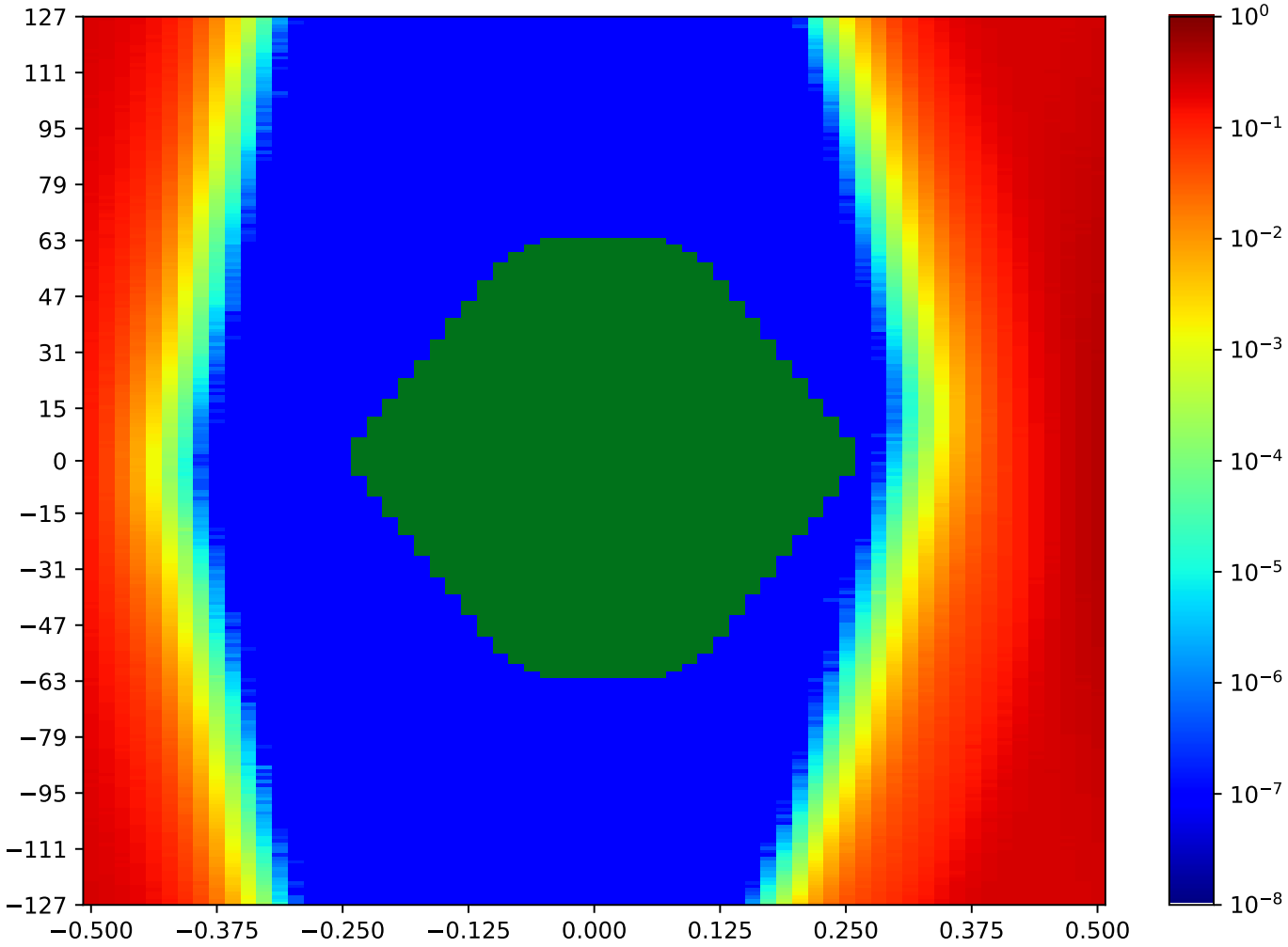


Figure 4.254: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.2 MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Table 4.235: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:26:52		2018-Sep-27 15:27:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9206	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

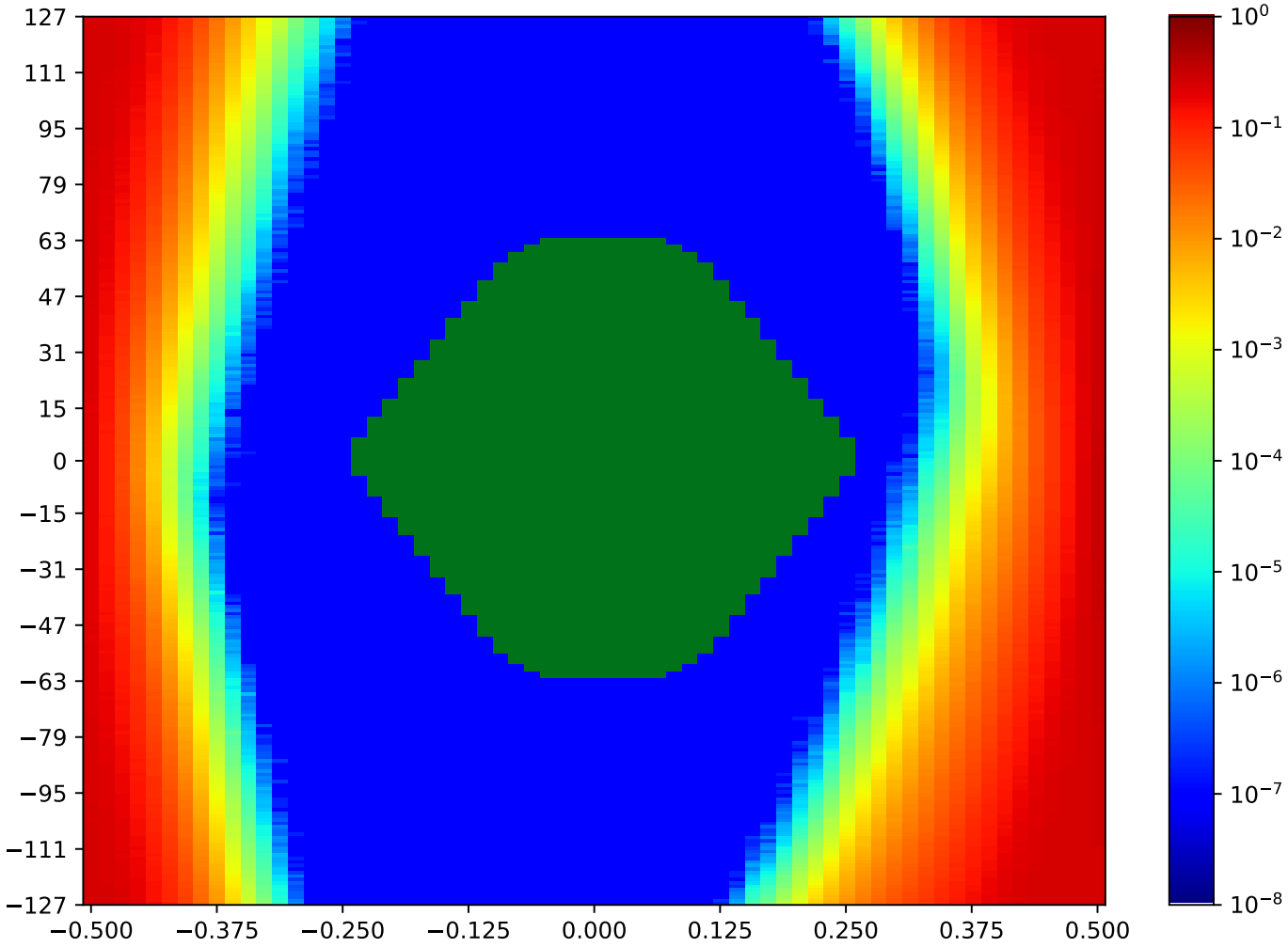


Figure 4.255: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.3 MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Table 4.236: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:28:38		2018-Sep-27 15:28:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8846	42	64.62%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

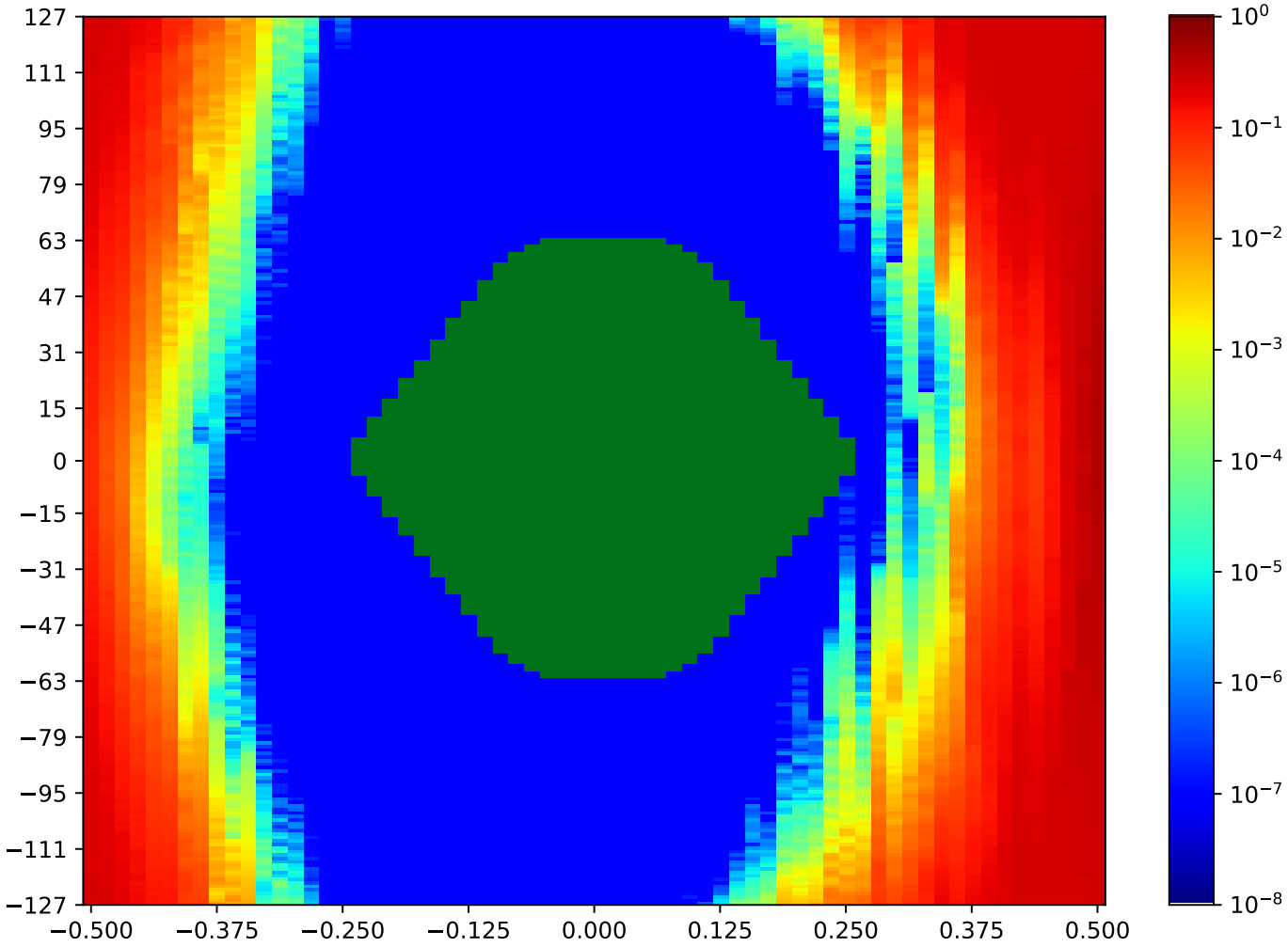


Figure 4.256: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.4 MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Table 4.237: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:26:32		2018-Sep-27 15:26:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8676	40	61.54%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

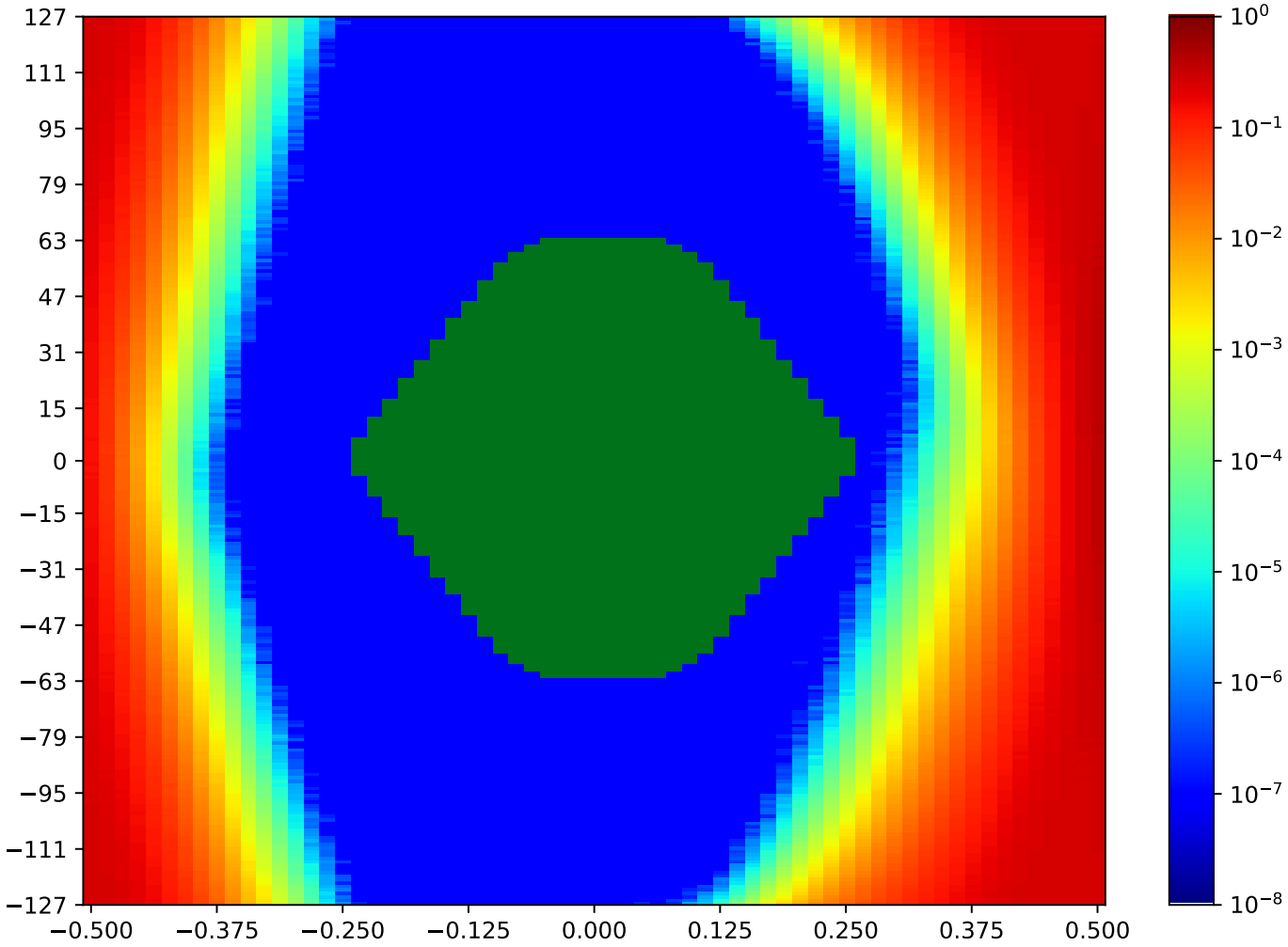


Figure 4.257: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.5 MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Table 4.238: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:29:39		2018-Sep-27 15:30:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8660	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

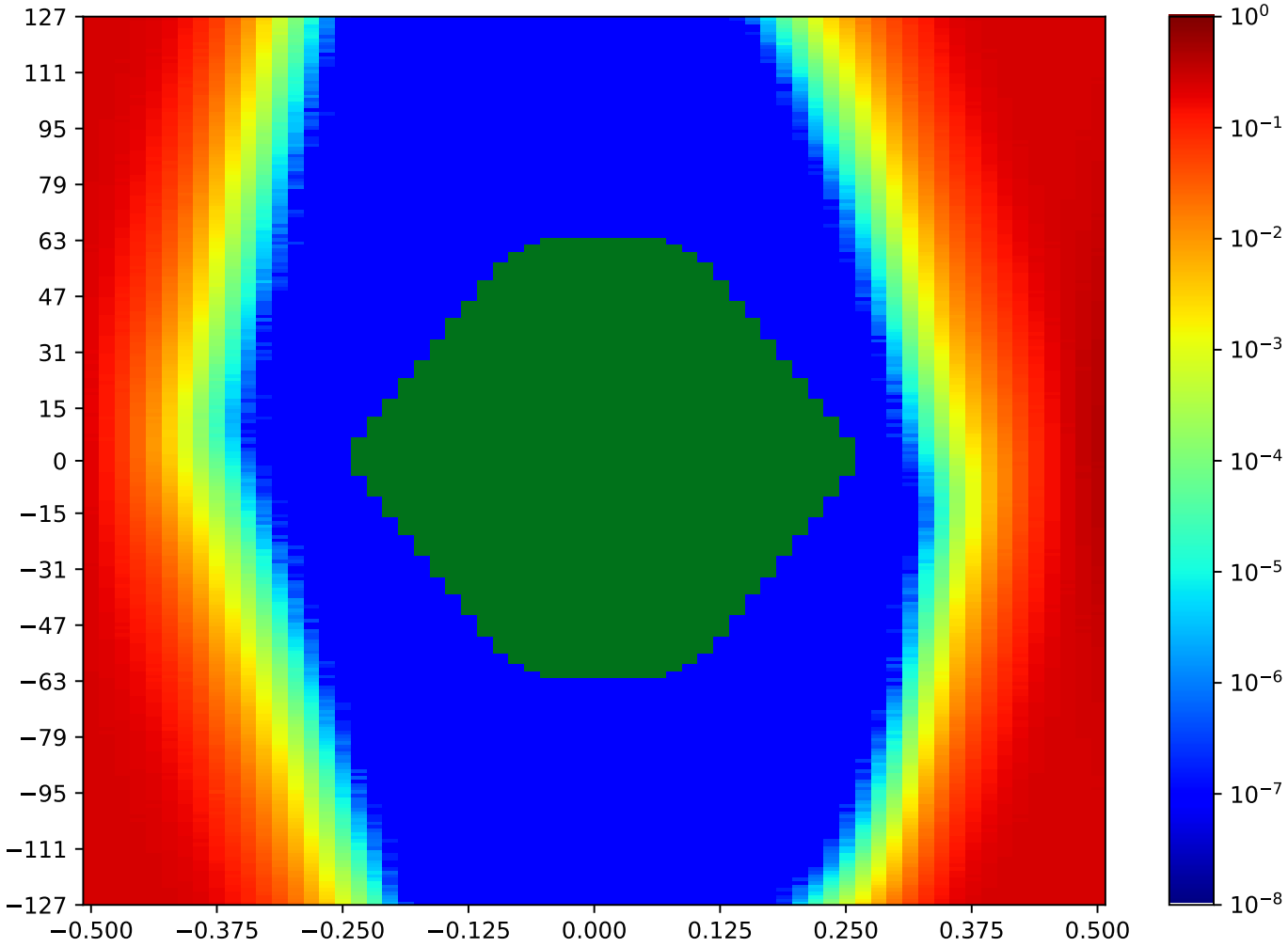


Figure 4.258: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.6 MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Table 4.239: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:27:12		2018-Sep-27 15:27:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8866	43	66.15%	243	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

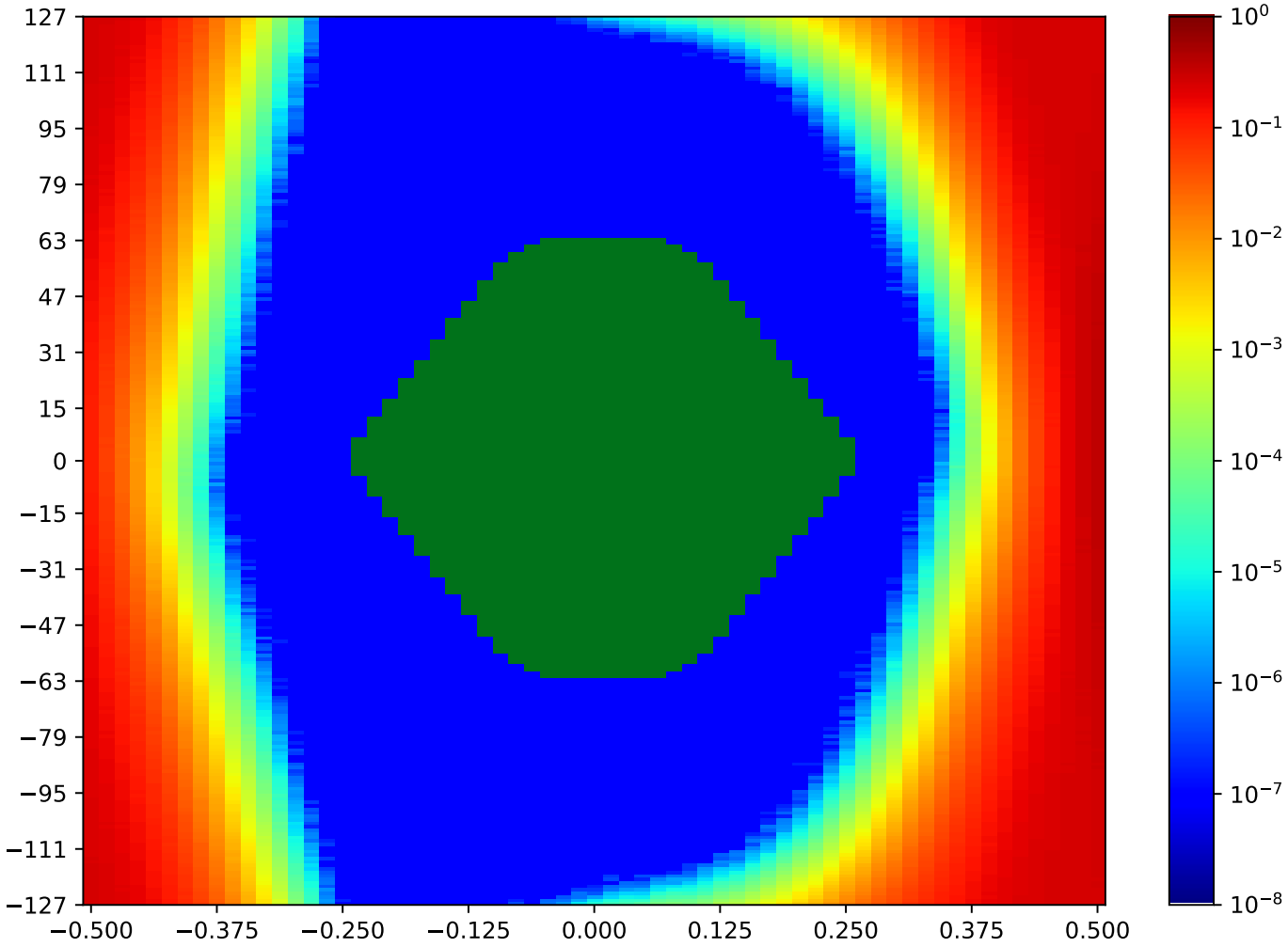


Figure 4.259: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.7 MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Table 4.240: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:30:20		2018-Sep-27 15:30:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9455	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

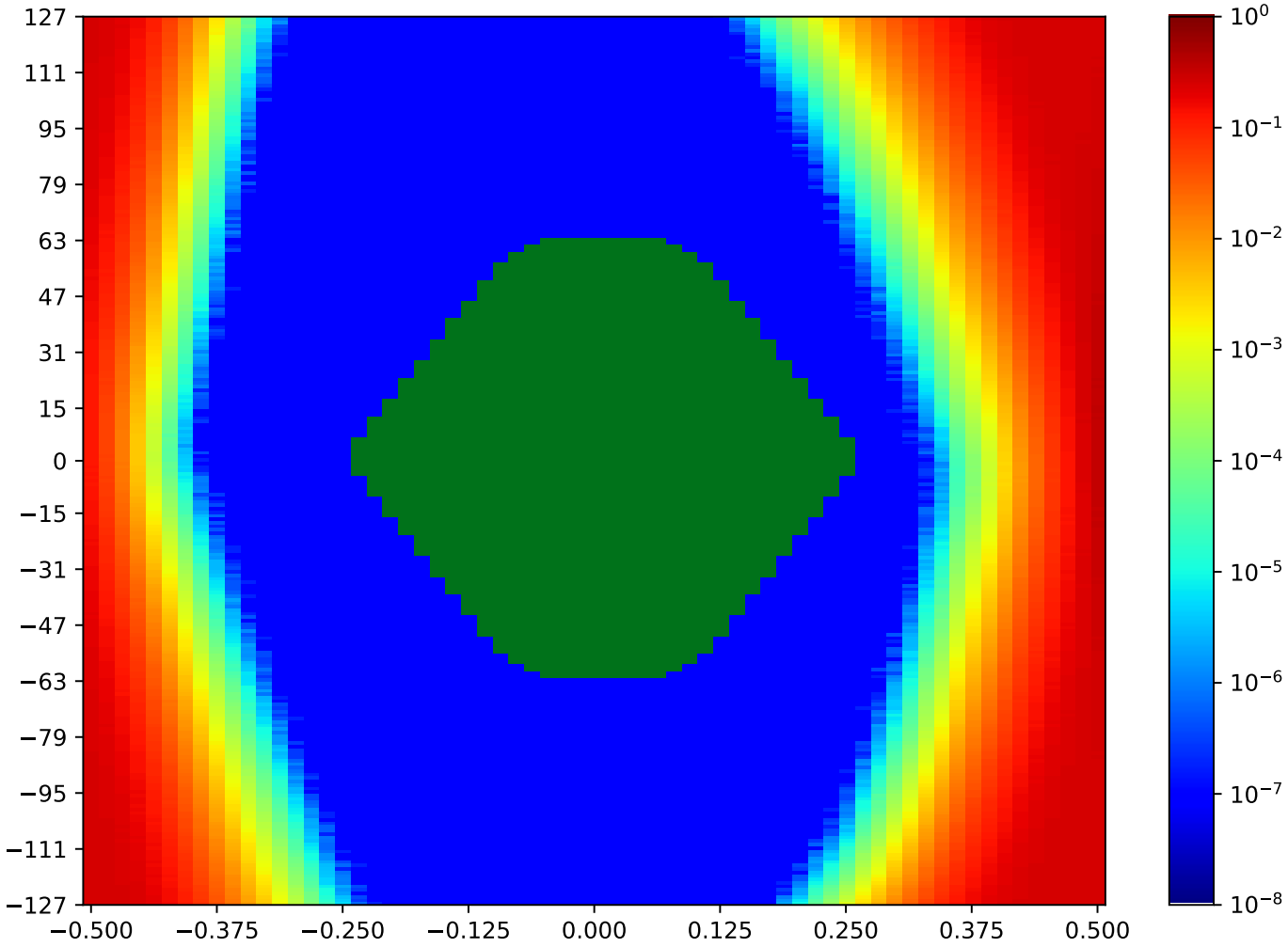


Figure 4.260: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.8 MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Table 4.241: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:27:57		2018-Sep-27 15:28:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8364	42	64.62%	230	90.20%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

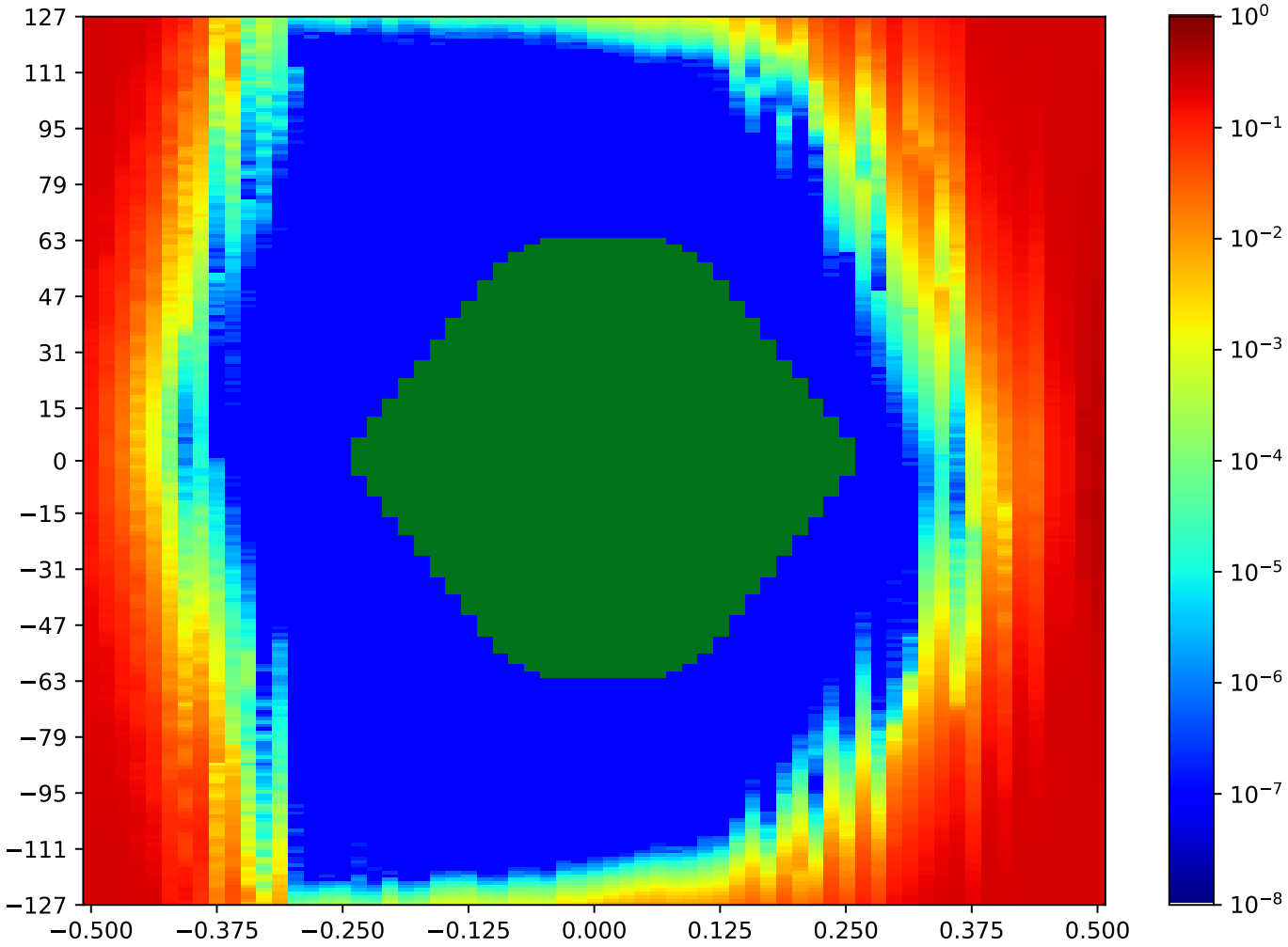


Figure 4.261: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.9 MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Table 4.242: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:30:00		2018-Sep-27 15:30:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9051	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

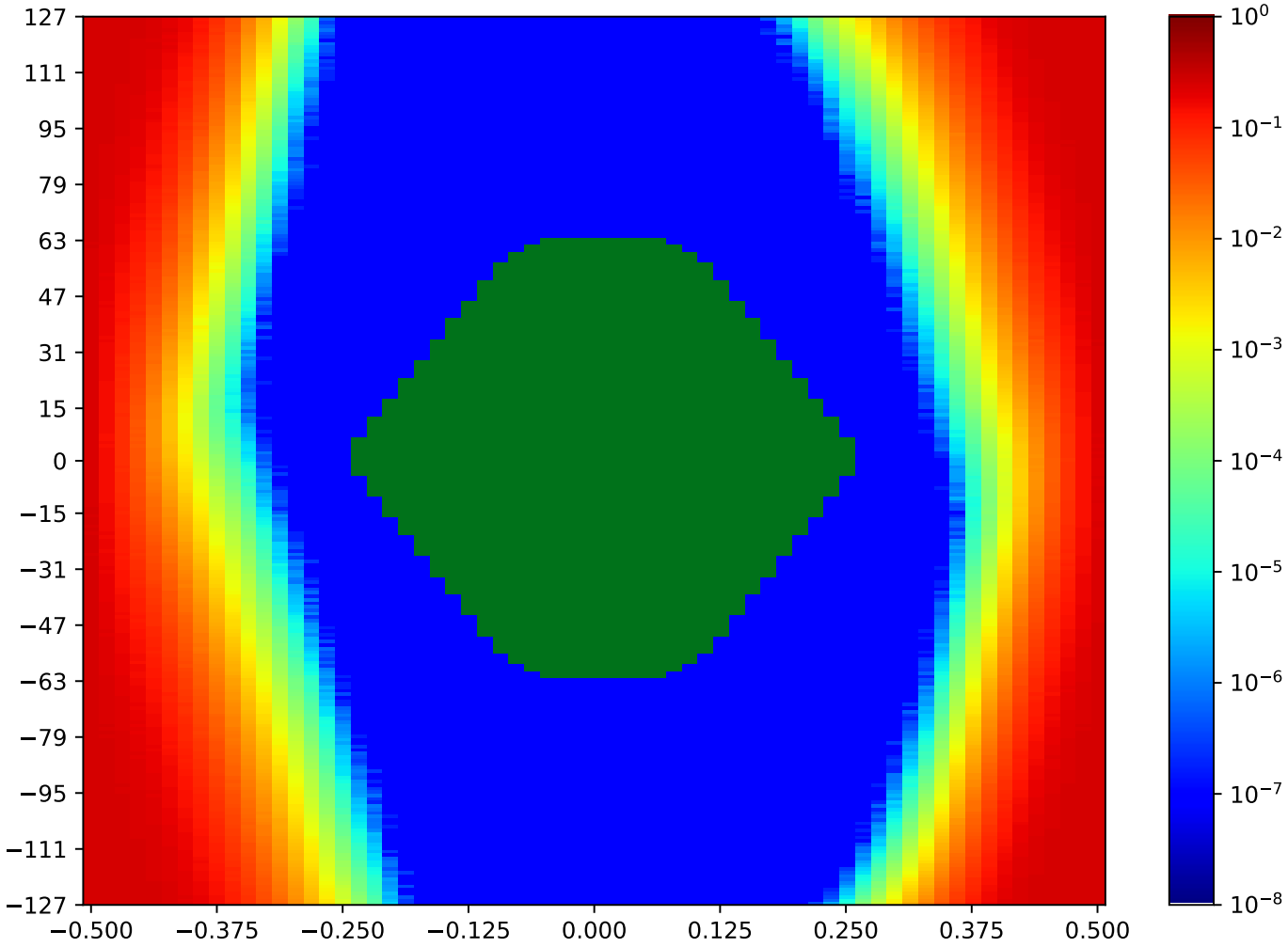


Figure 4.262: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.10 MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Table 4.243: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:28:17		2018-Sep-27 15:28:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8994	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

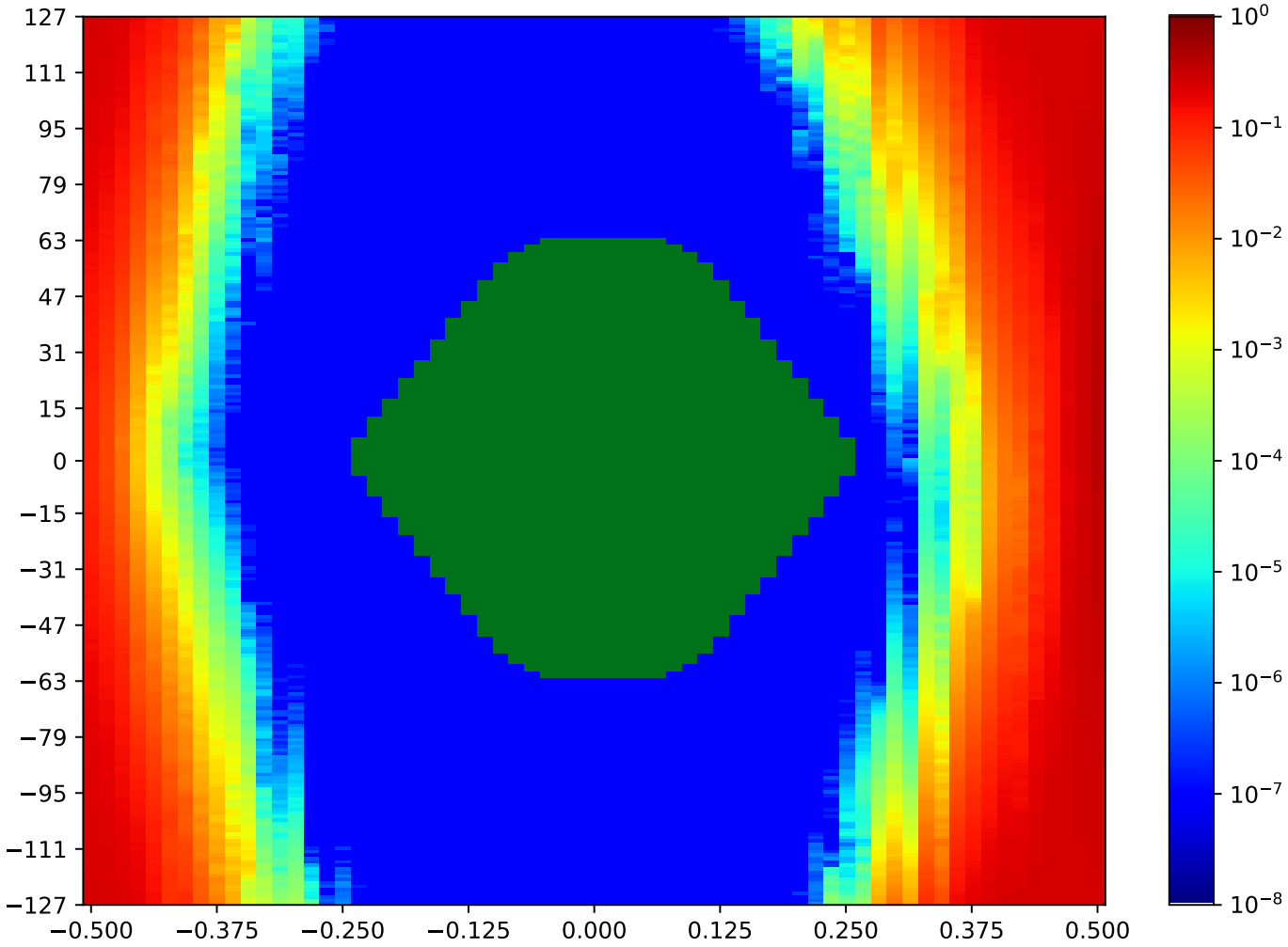


Figure 4.263: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.11 MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Table 4.244: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:29:19		2018-Sep-27 15:29:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9244	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

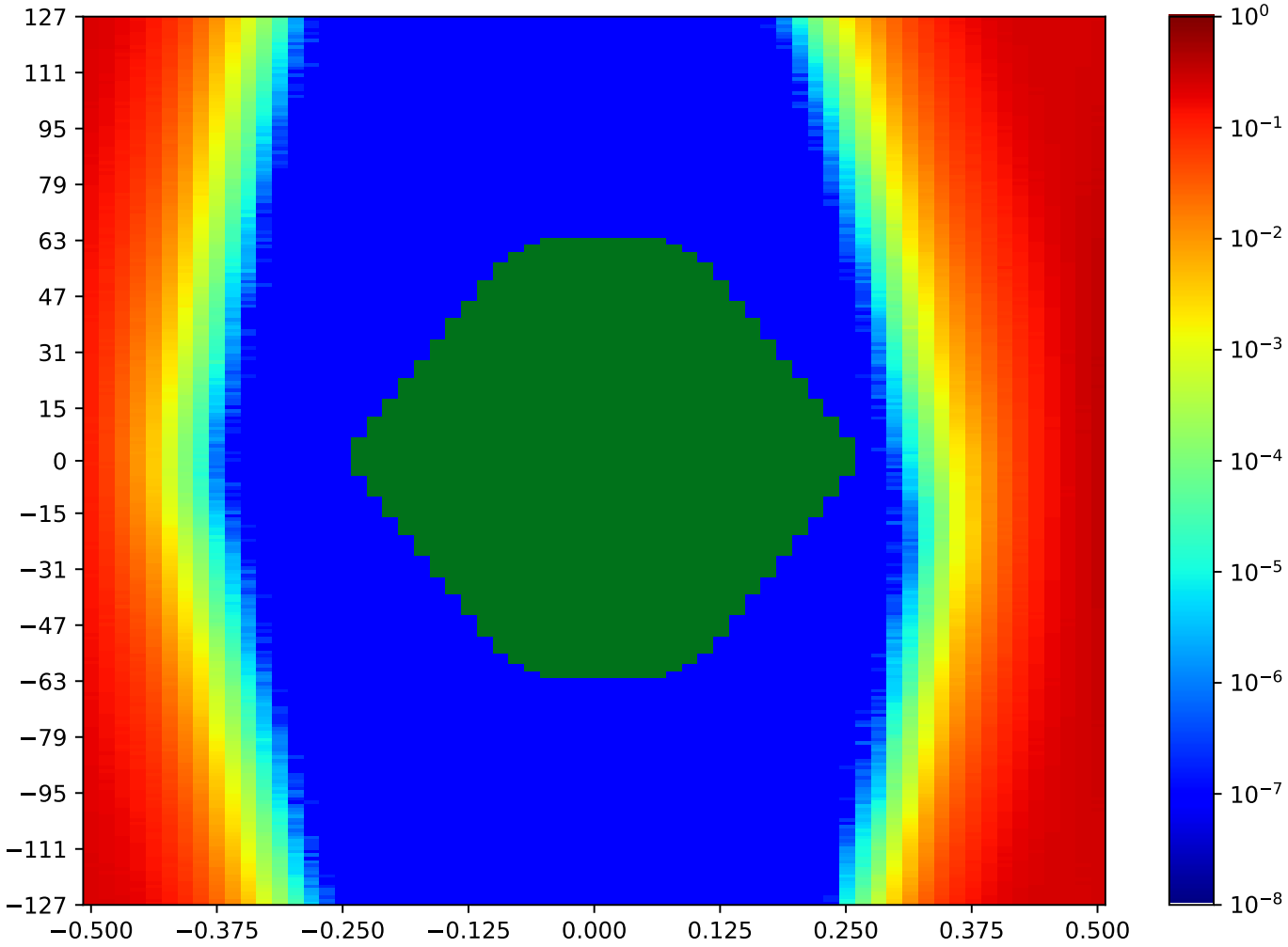


Figure 4.264: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.20.12 MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Table 4.245: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:28:58		2018-Sep-27 15:29:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9173	41	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

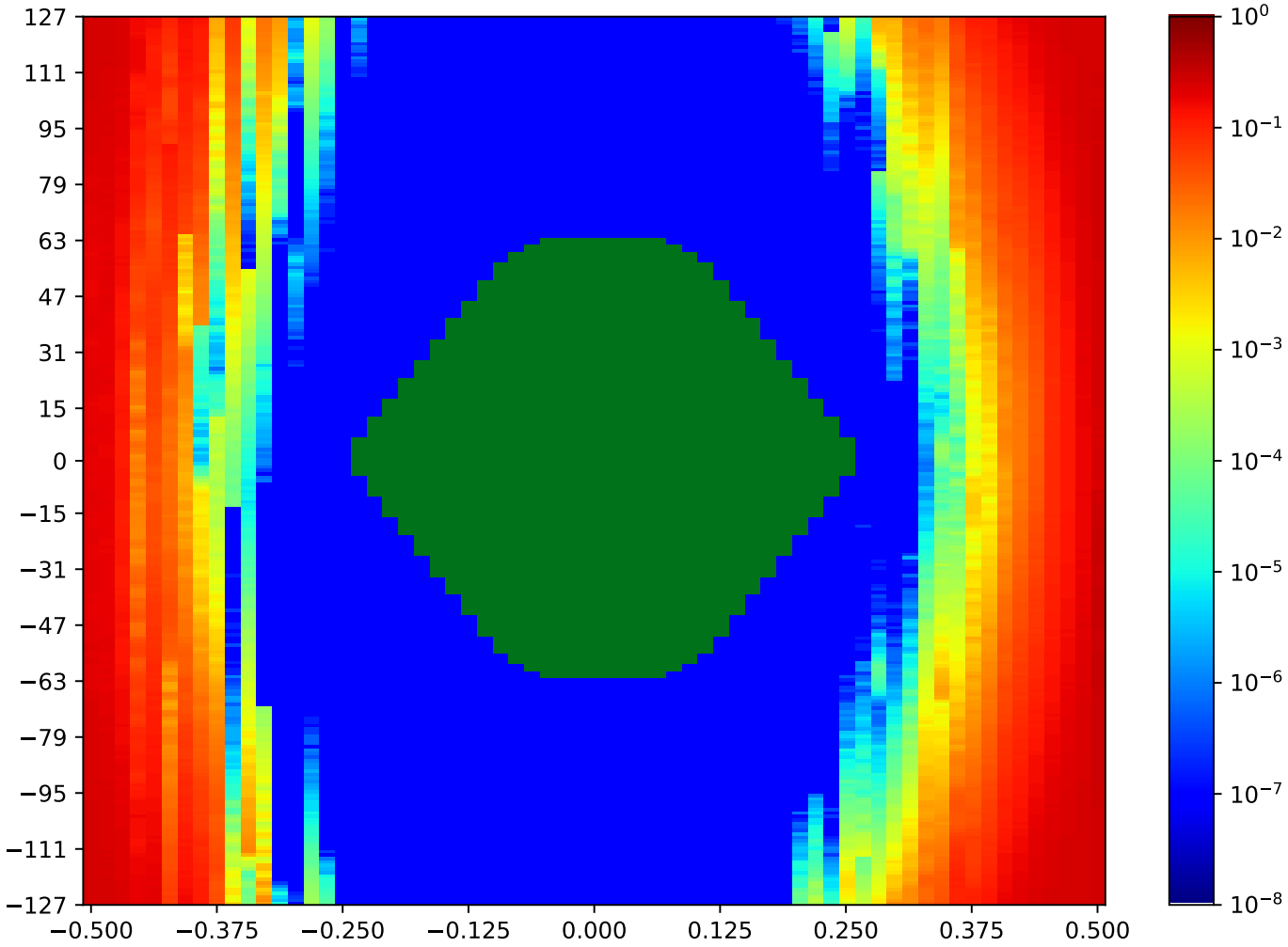


Figure 4.265: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21 MSP_C TX3 MSP_A RX3 Minipod Loopback

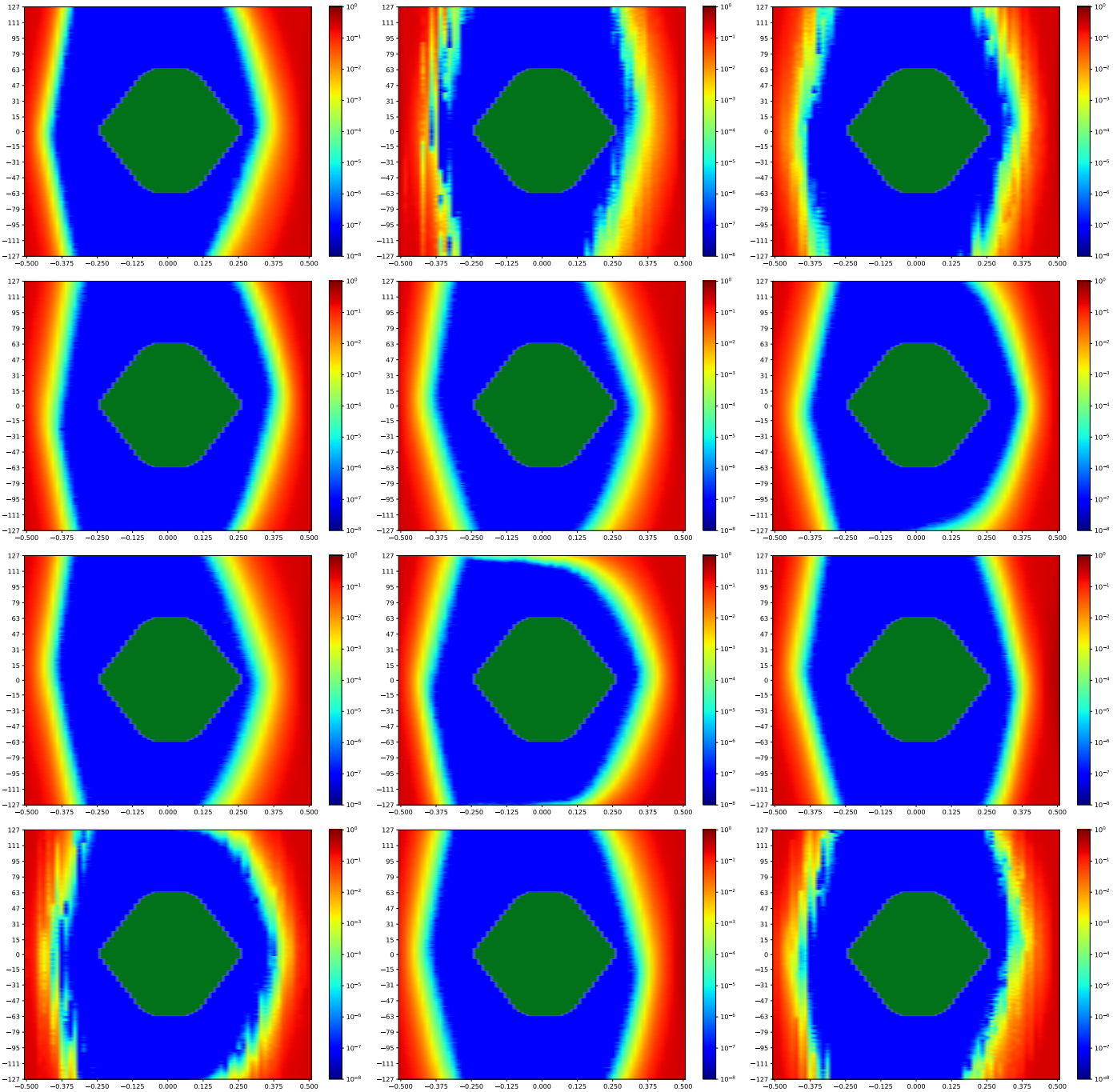


Figure 4.266: MSP_C TX3 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 4.279.

4.21.1 MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Table 4.246: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:31:41		2018-Sep-27 15:32:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9610	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

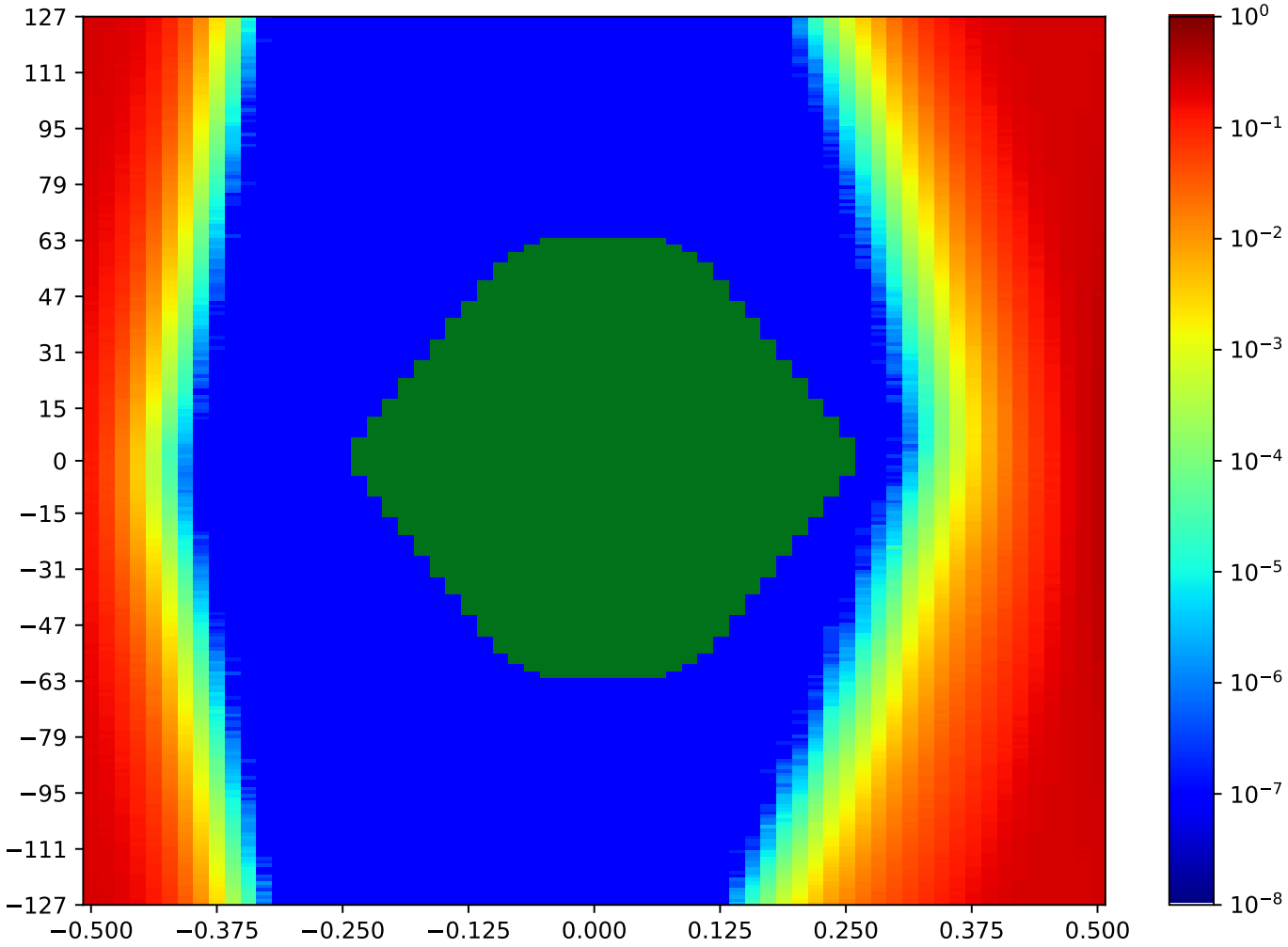


Figure 4.267: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.2 MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Table 4.247: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:32:22		2018-Sep-27 15:32:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8940	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

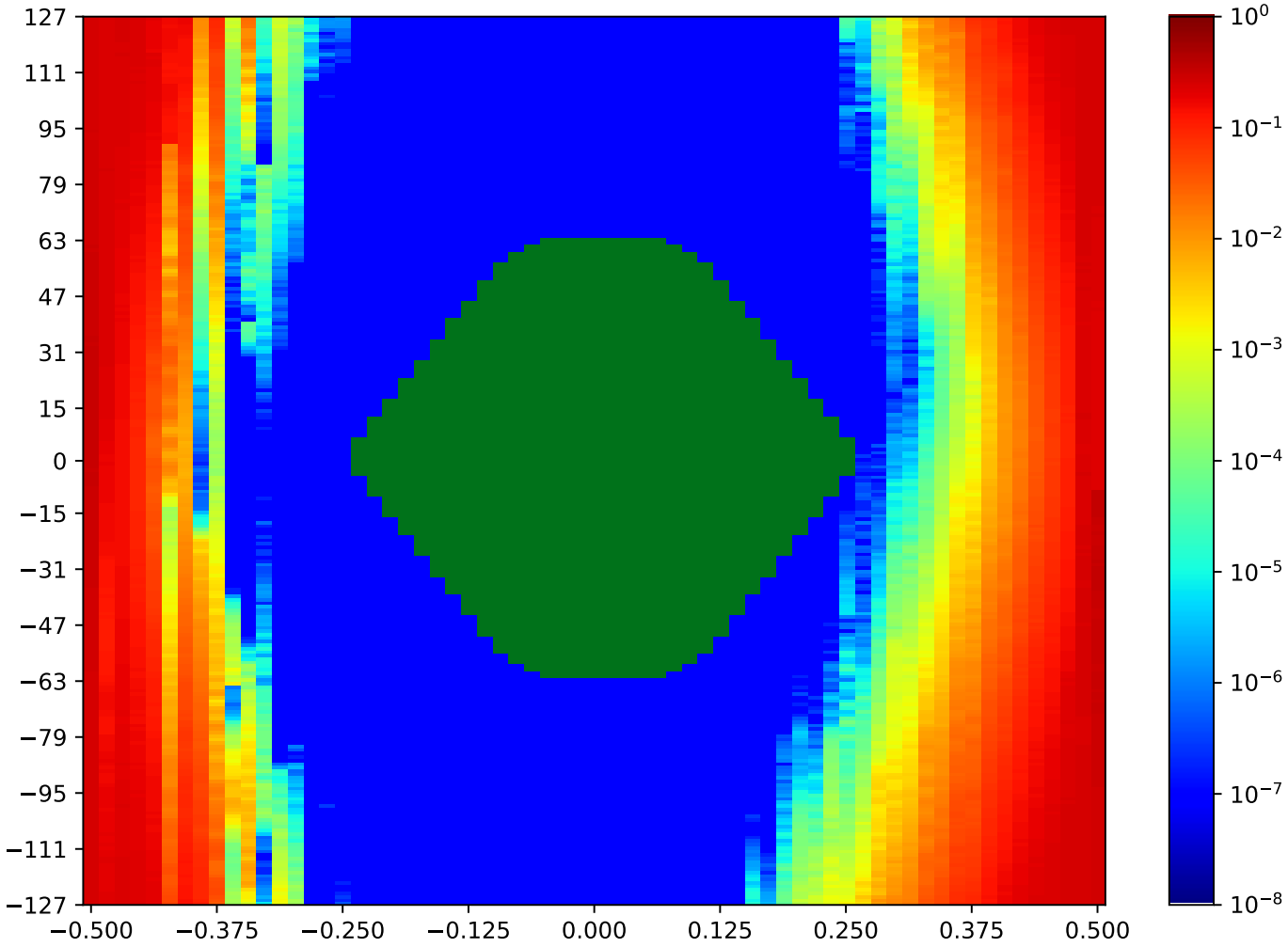


Figure 4.268: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.3 MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Table 4.248: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:32:43		2018-Sep-27 15:33:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9453	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

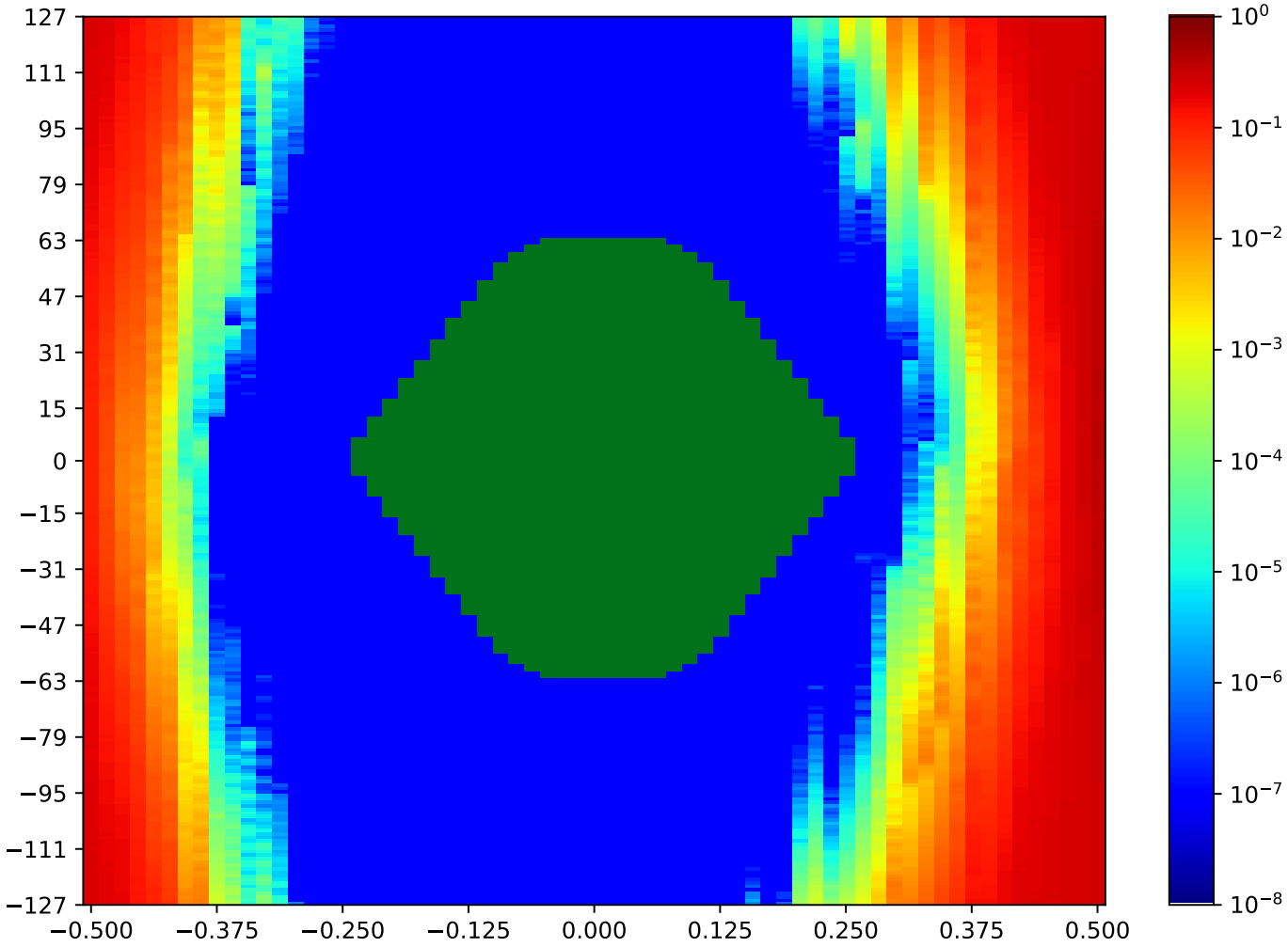


Figure 4.269: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.4 MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Table 4.249: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:31:01		2018-Sep-27 15:31:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10030	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

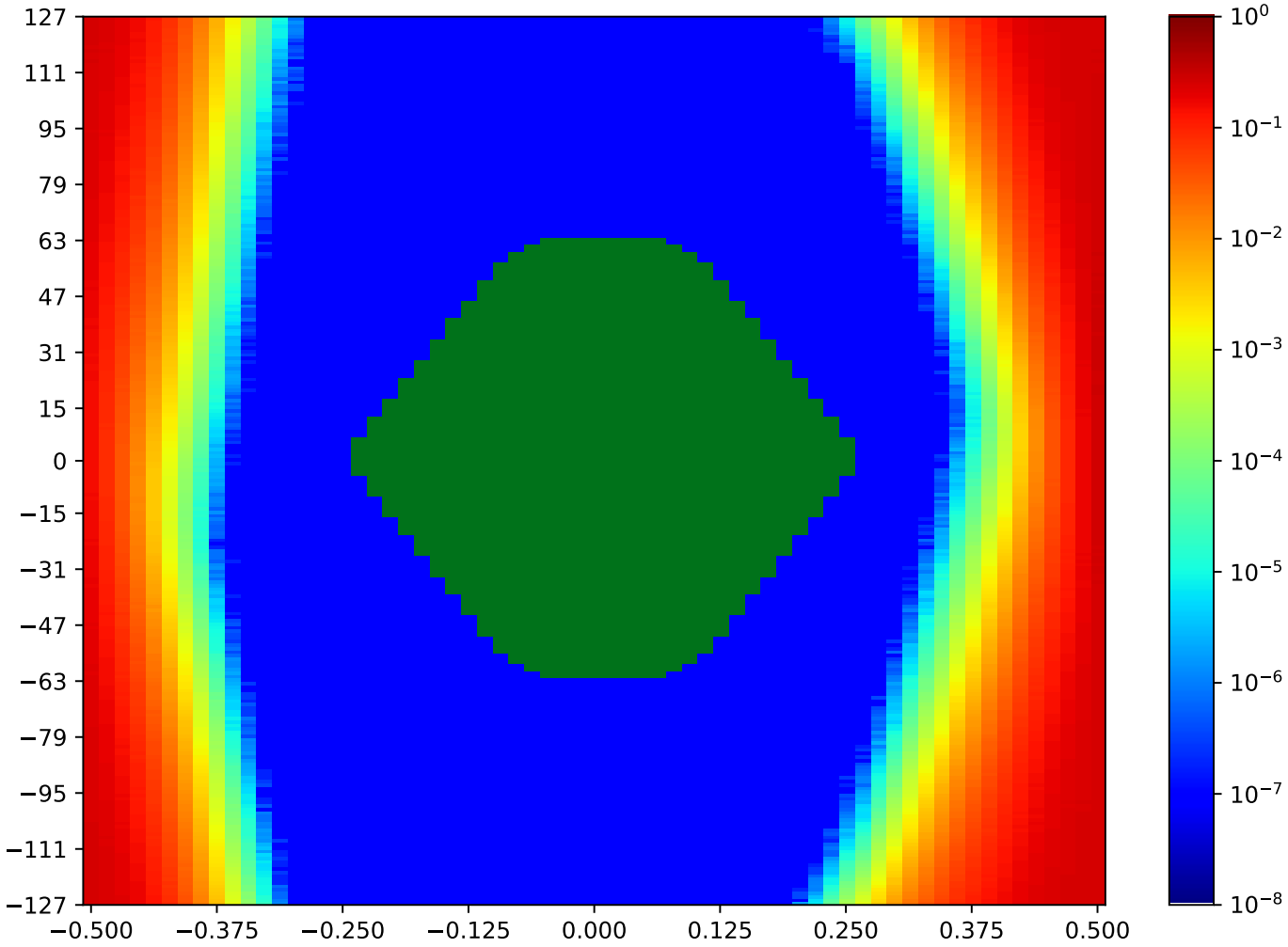


Figure 4.270: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.5 MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Table 4.250: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:33:44		2018-Sep-27 15:34:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8495	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

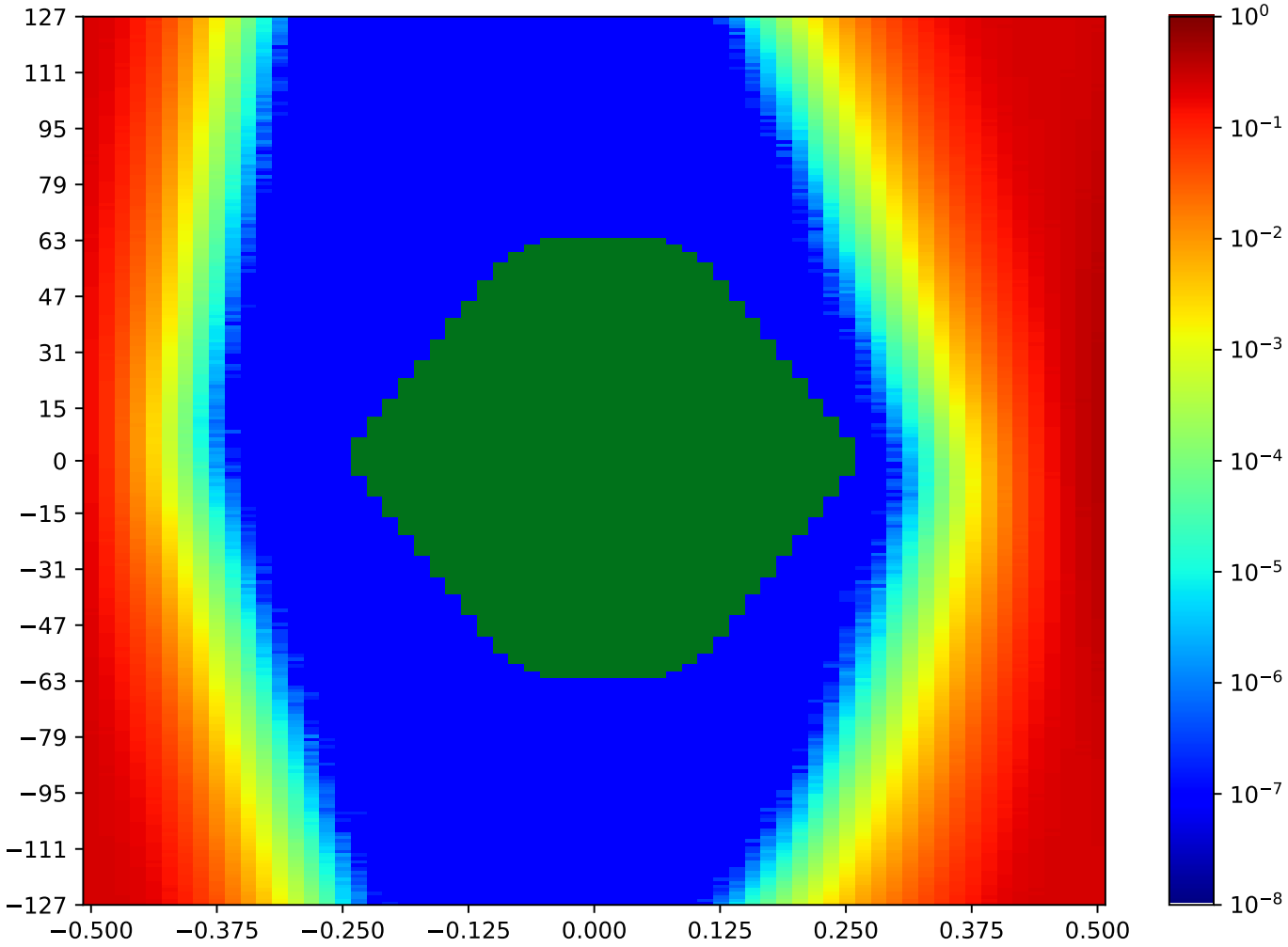


Figure 4.271: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.6 MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Table 4.251: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:30:41		2018-Sep-27 15:31:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9208	45	69.23%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

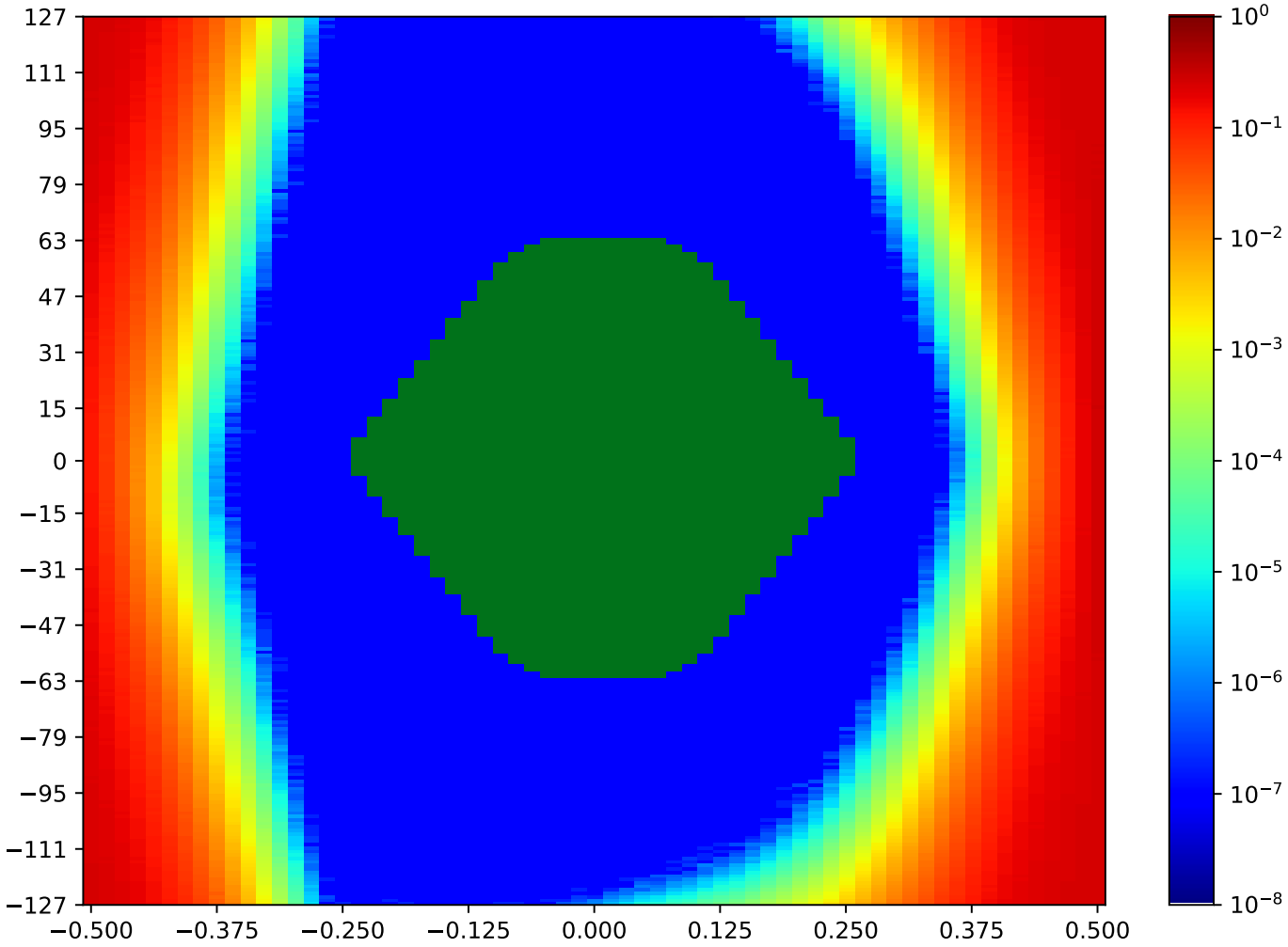


Figure 4.272: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.7 MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Table 4.252: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:34:26		2018-Sep-27 15:34:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8850	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

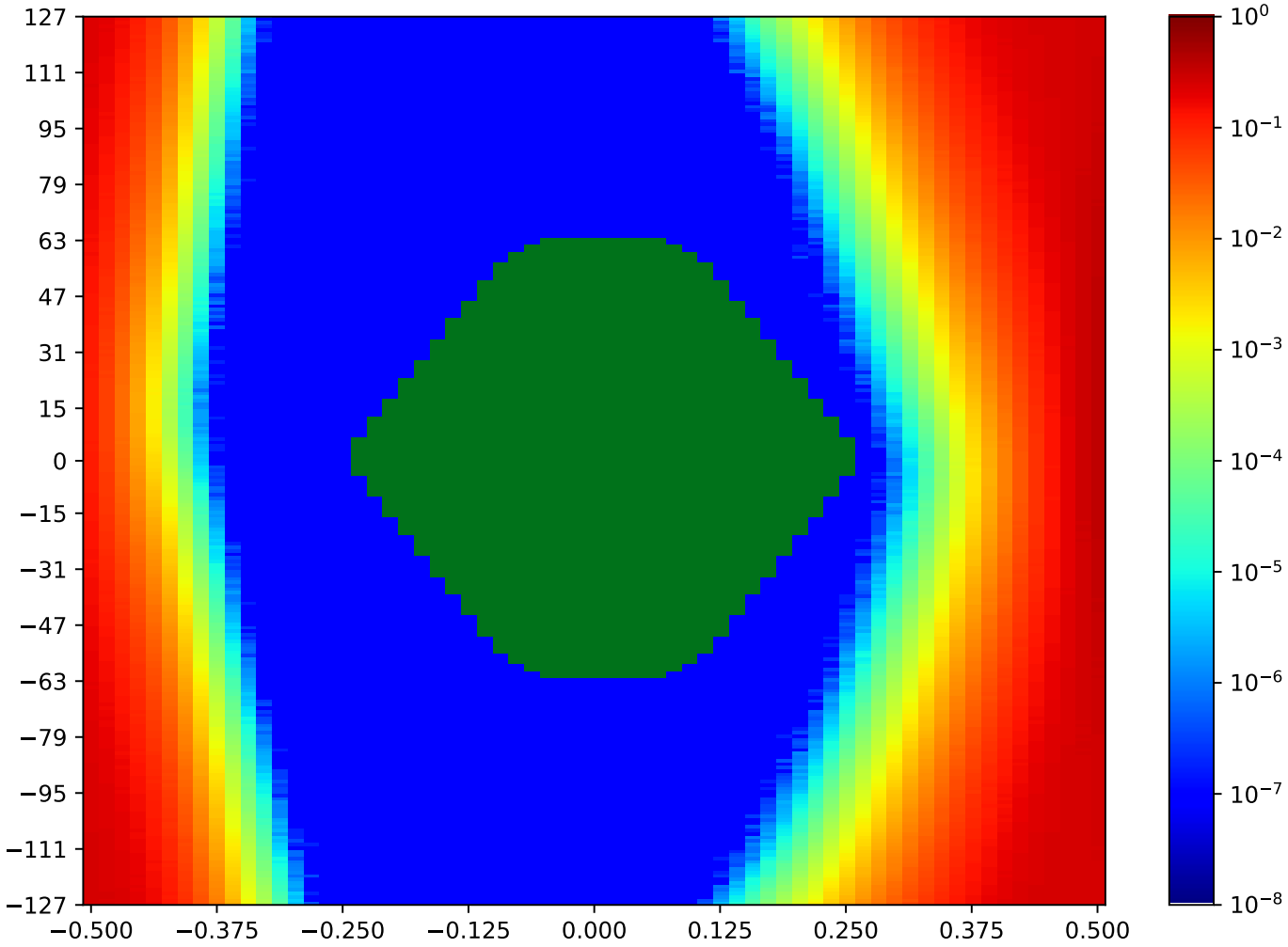


Figure 4.273: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.8 MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Table 4.253: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:31:21		2018-Sep-27 15:31:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8582	43	66.15%	235	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

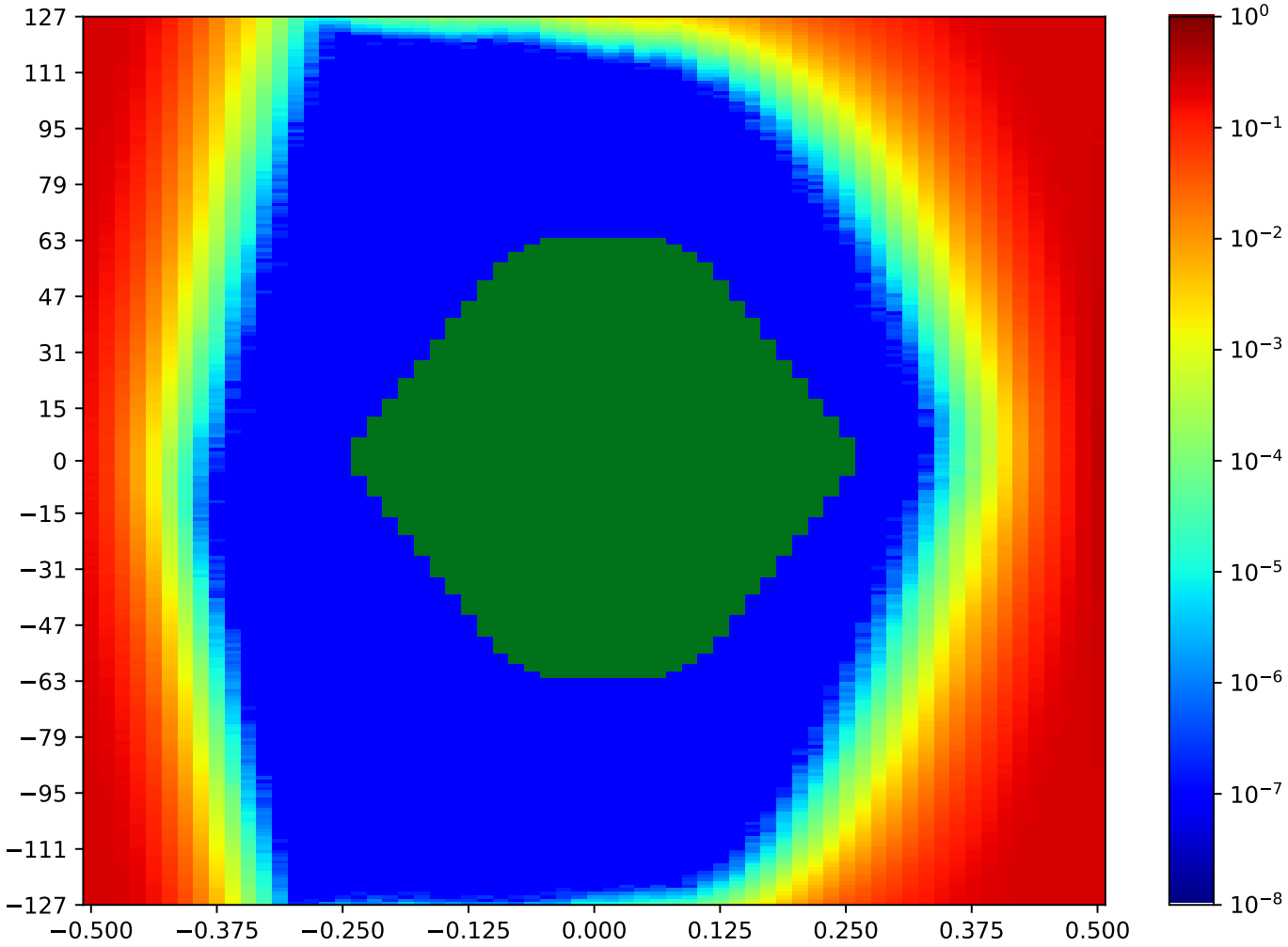


Figure 4.274: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.9 MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Table 4.254: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:34:05		2018-Sep-27 15:34:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9739	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

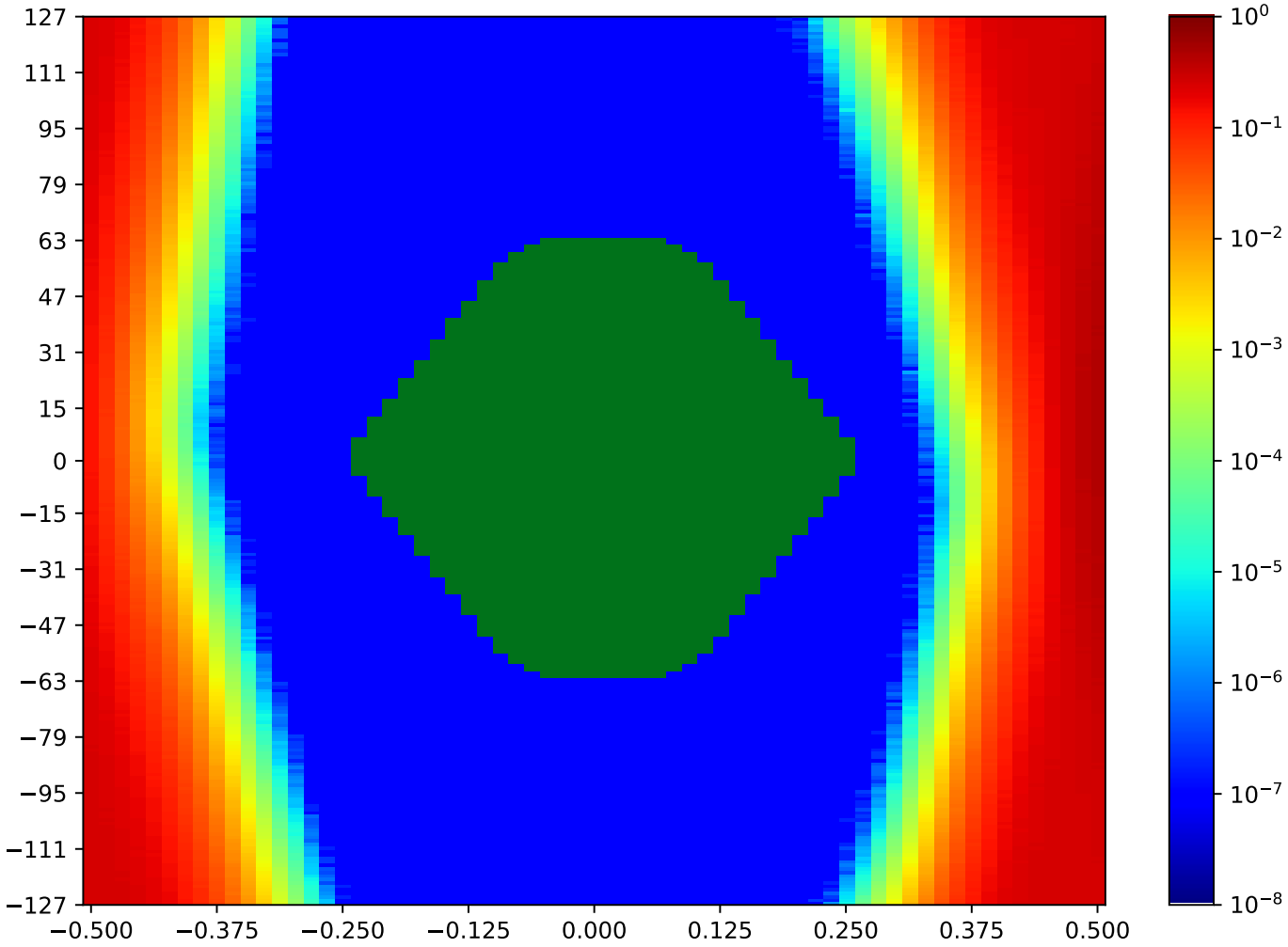


Figure 4.275: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.10 MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Table 4.255: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:32:02		2018-Sep-27 15:32:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9600	47	70.77%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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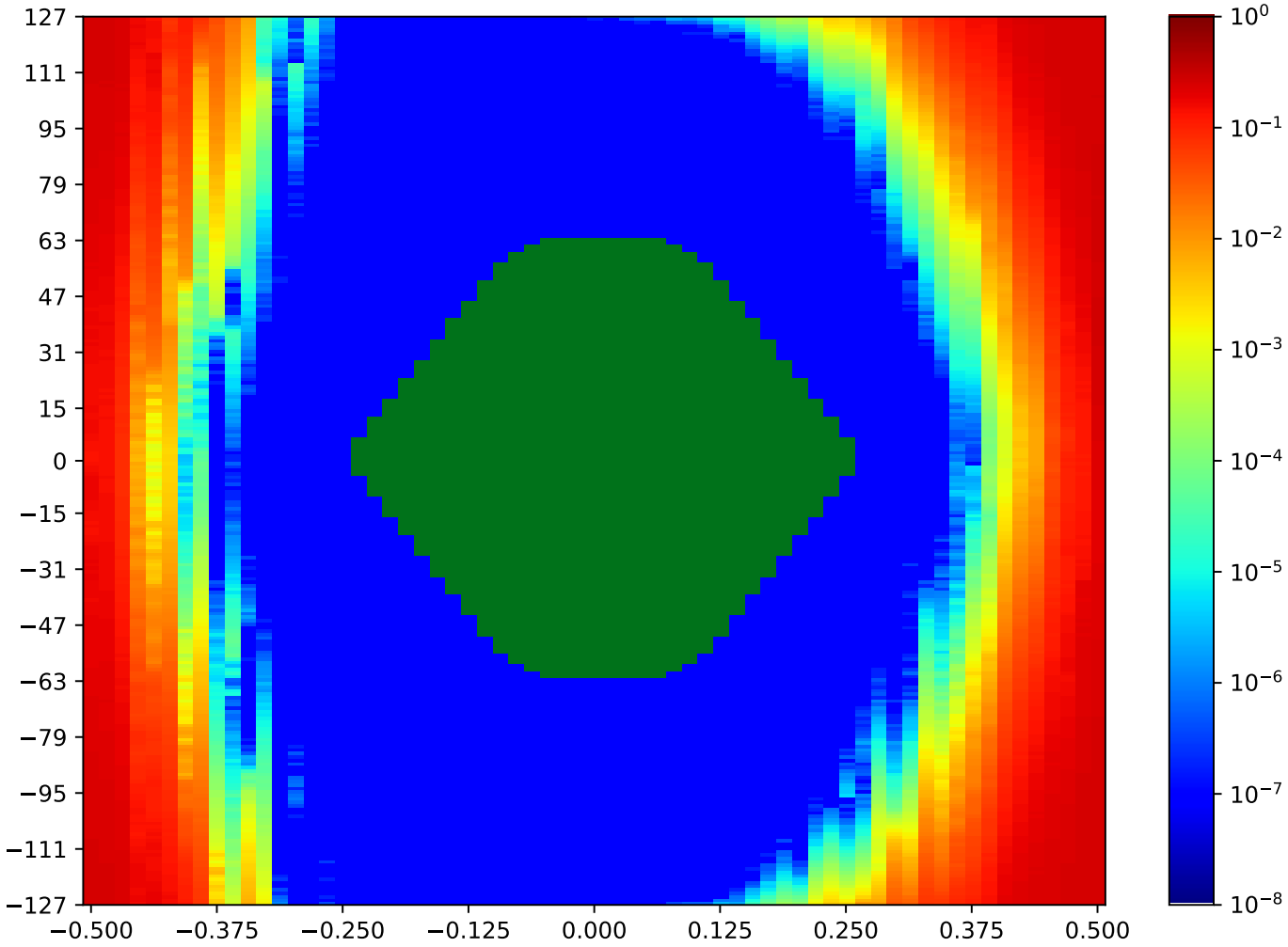


Figure 4.276: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.11 MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Table 4.256: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:33:24		2018-Sep-27 15:33:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9688	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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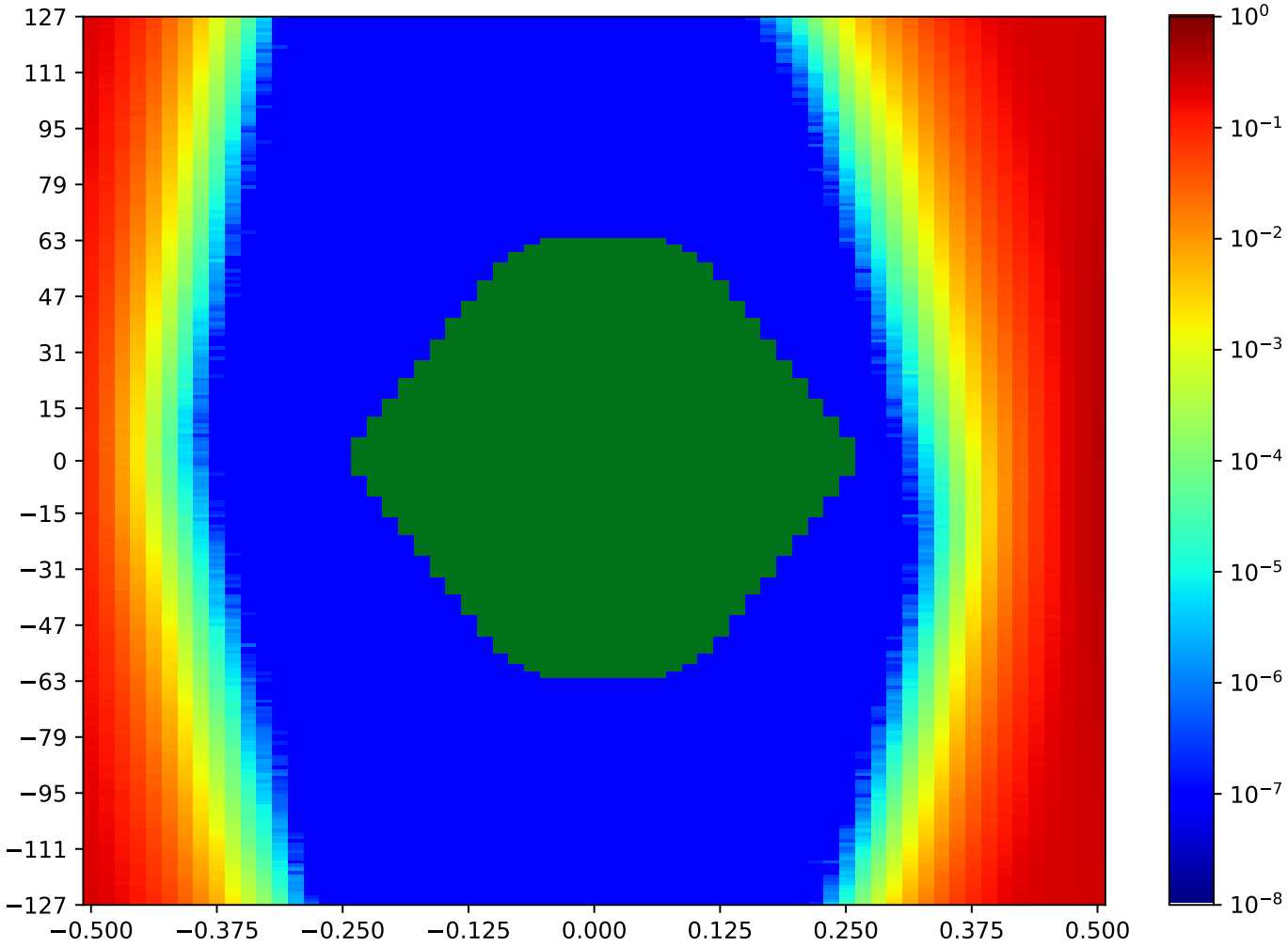


Figure 4.277: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.21.12 MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Table 4.257: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:33:03		2018-Sep-27 15:33:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9702	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

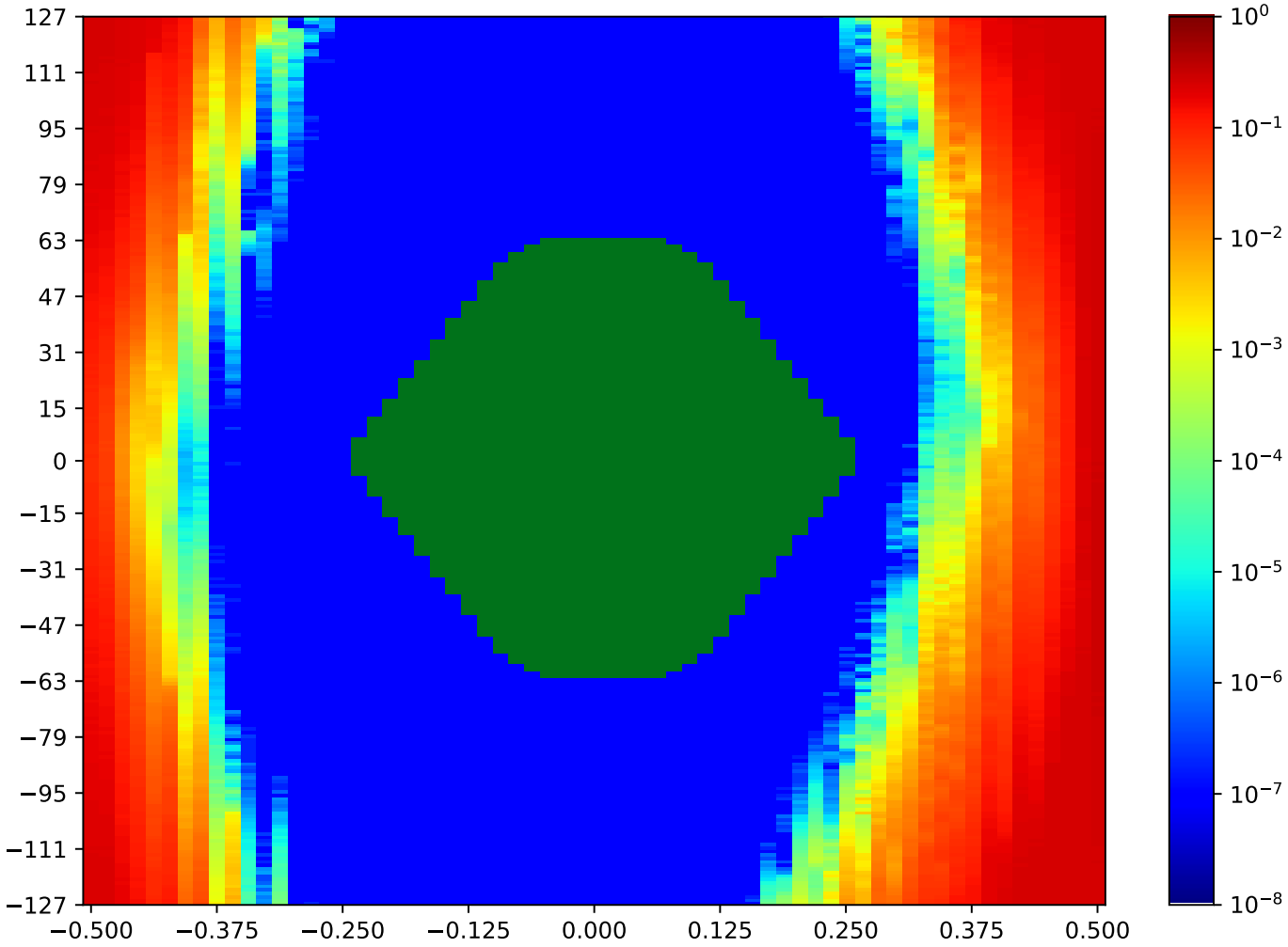


Figure 4.278: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22 MSP_C TX4 MSP_A RX4 Minipod Loopback

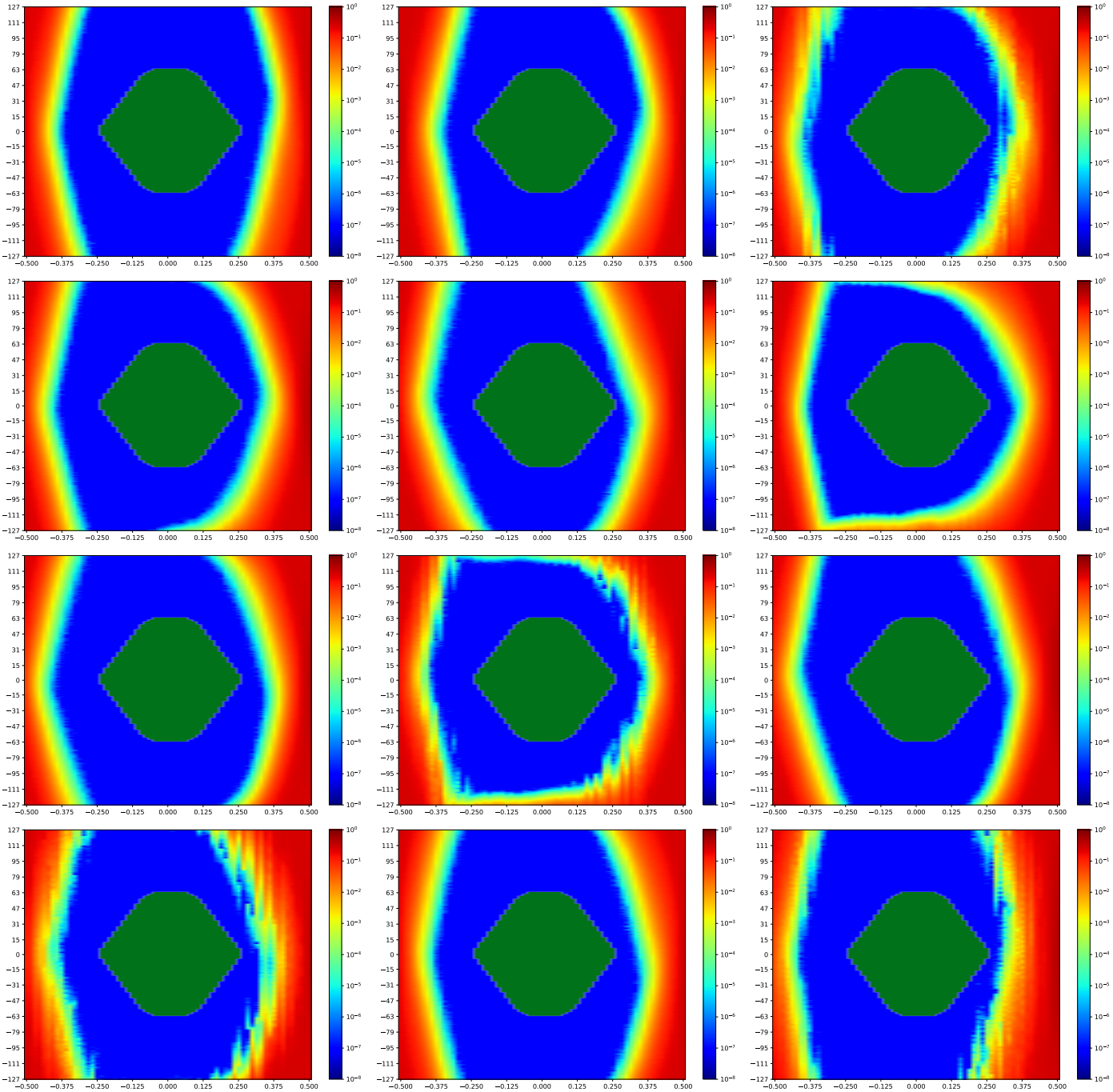


Figure 4.279: MSP_C TX4 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.
Next summary Figure 5.1.

4.22.1 MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Table 4.258: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:35:48		2018-Sep-27 15:36:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9885	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

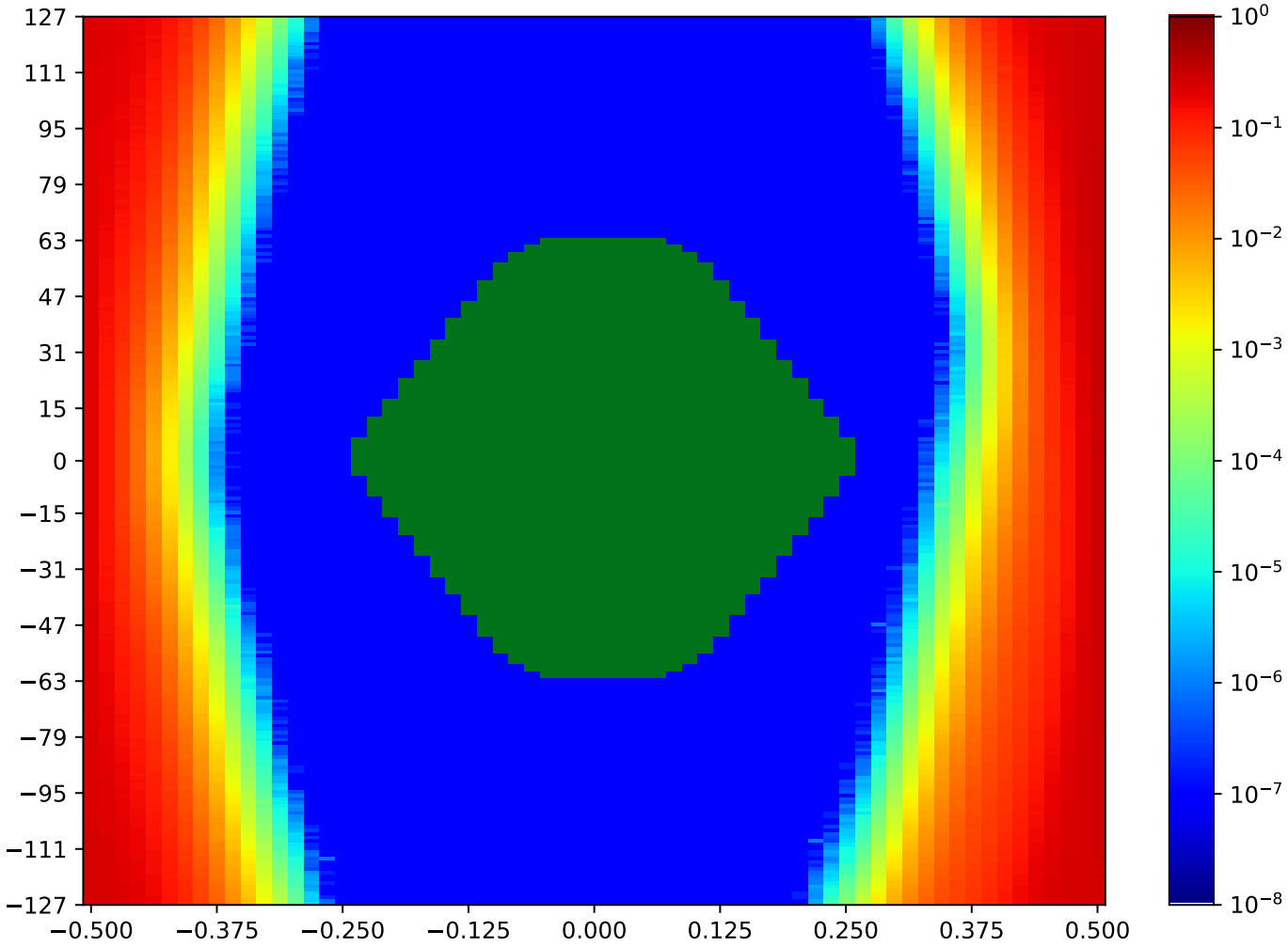


Figure 4.280: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.2 MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Table 4.259: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:35:07		2018-Sep-27 15:35:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8818	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

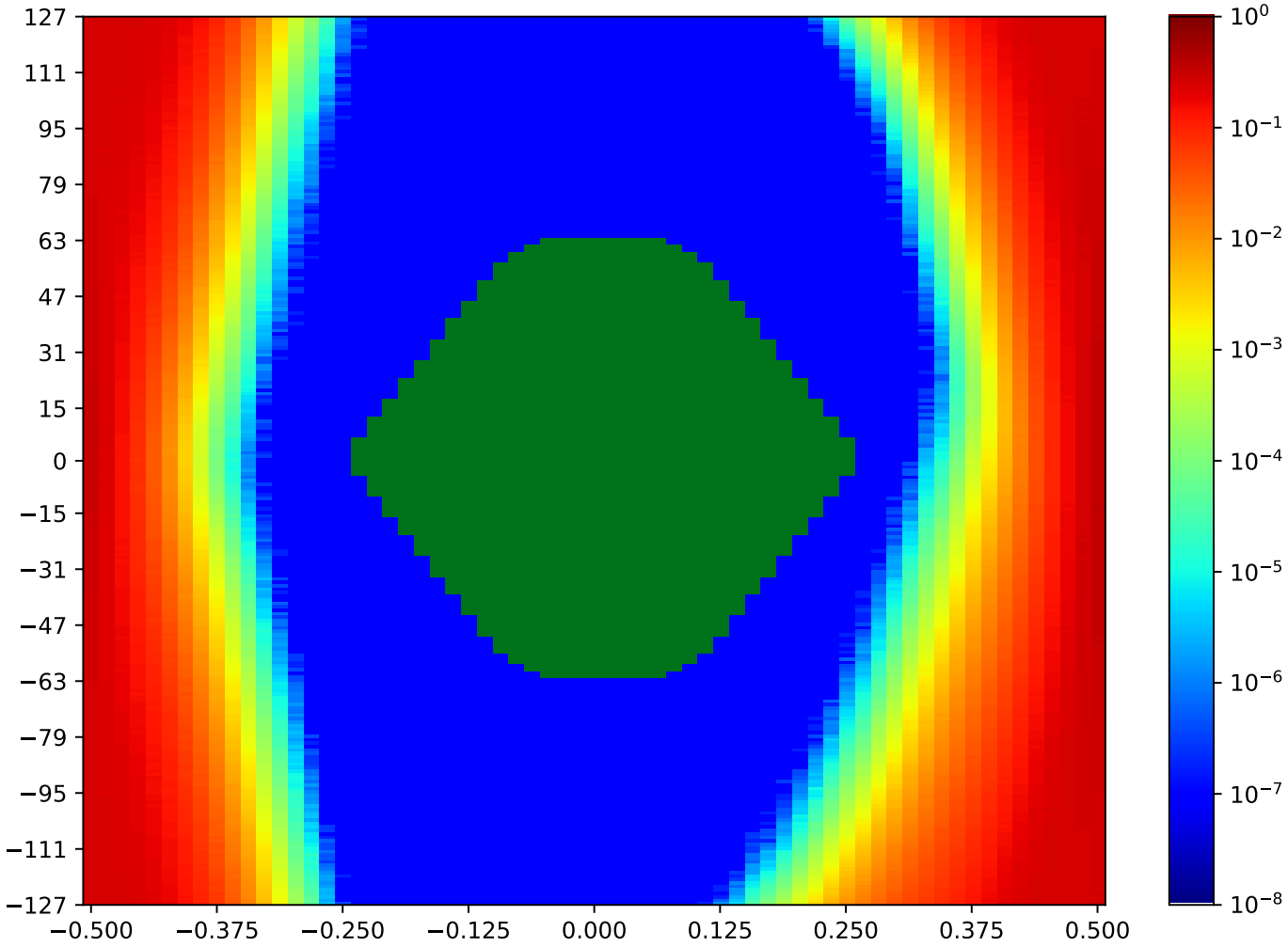


Figure 4.281: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.3 MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Table 4.260: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:36:49		2018-Sep-27 15:37:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8839	40	61.54%	251	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

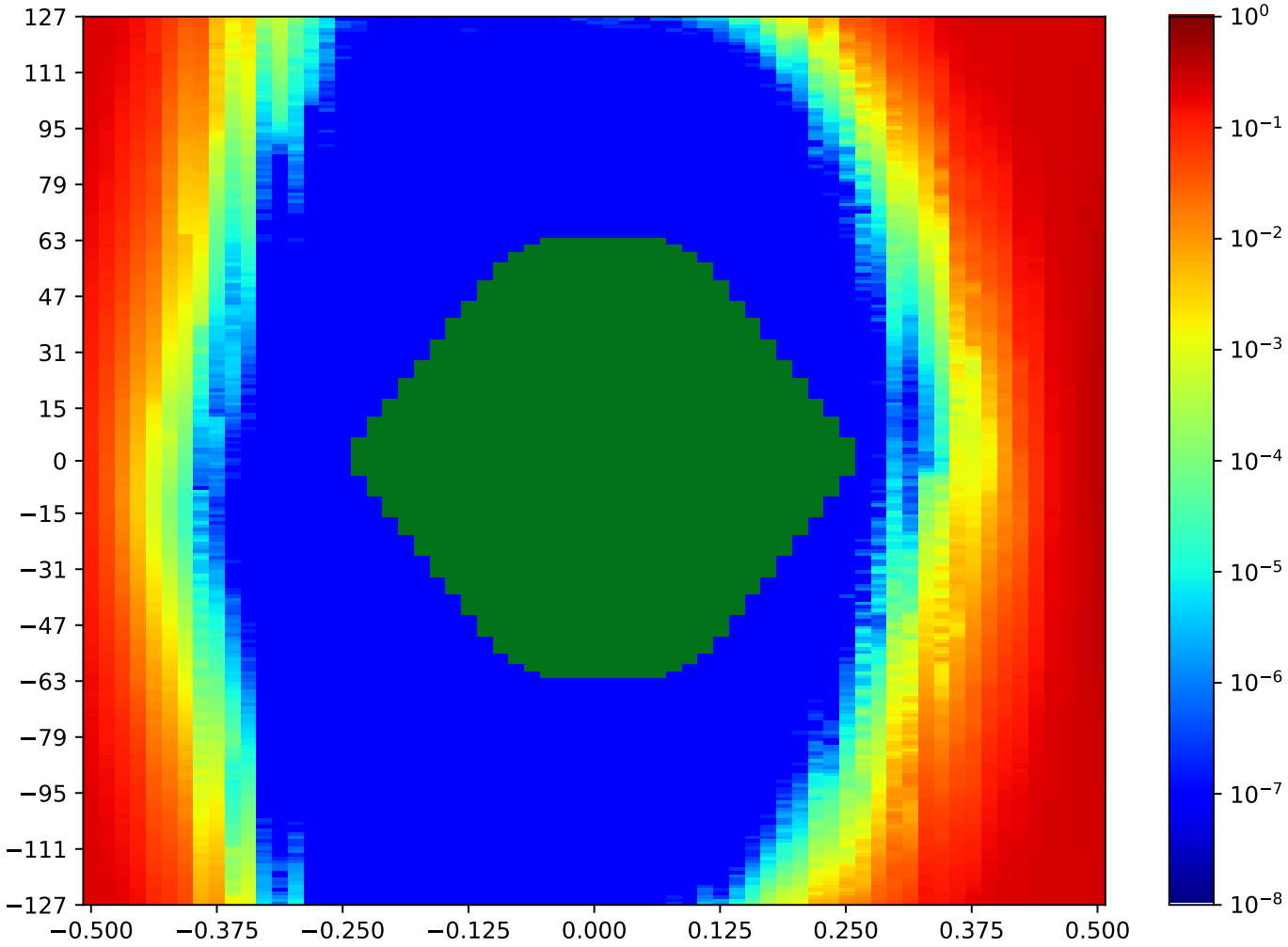


Figure 4.282: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.4 MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Table 4.261: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:34:47		2018-Sep-27 15:35:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8899	43	66.15%	247	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

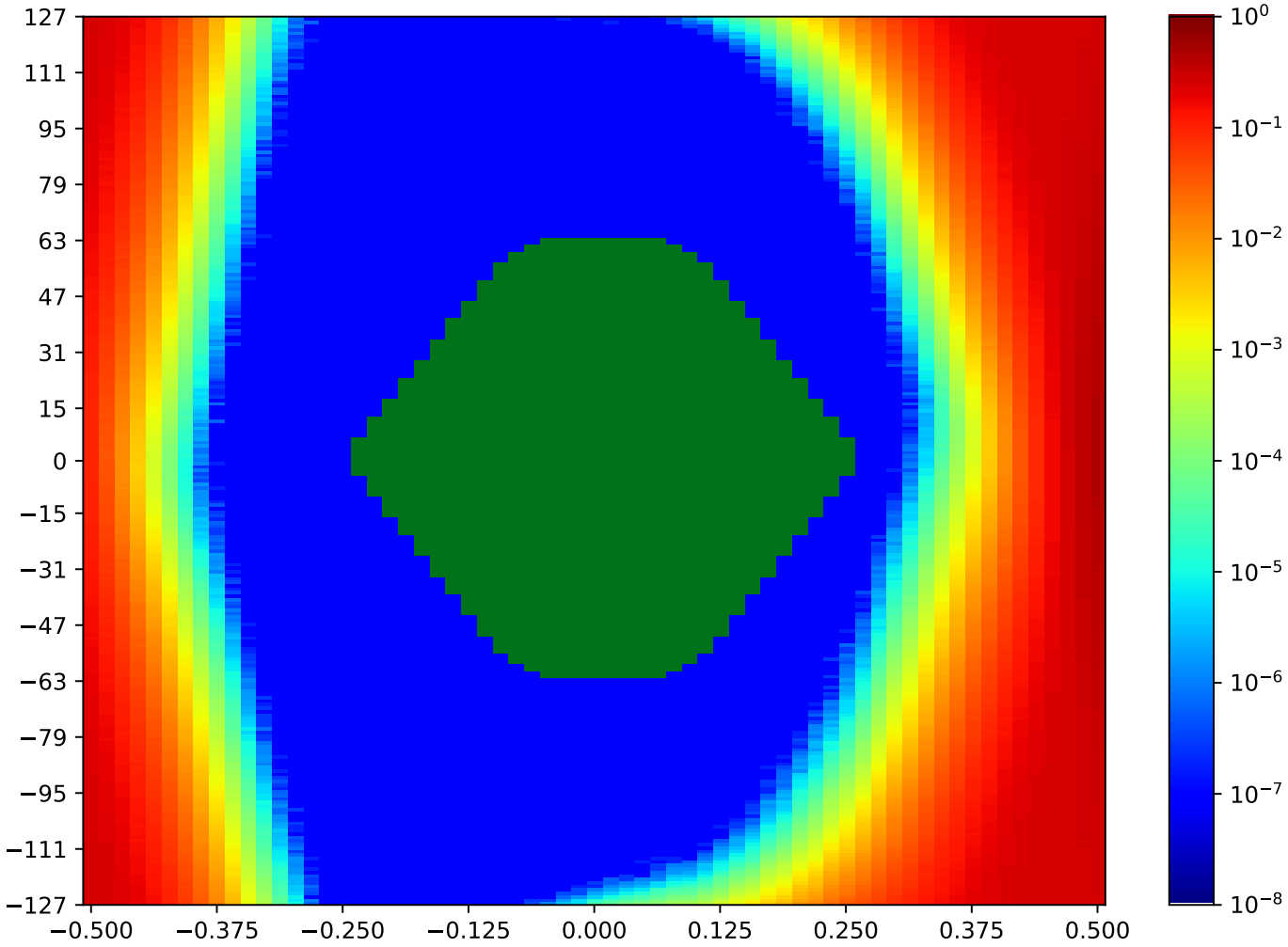


Figure 4.283: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.5 MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Table 4.262: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:37:50		2018-Sep-27 15:38:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8215	40	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

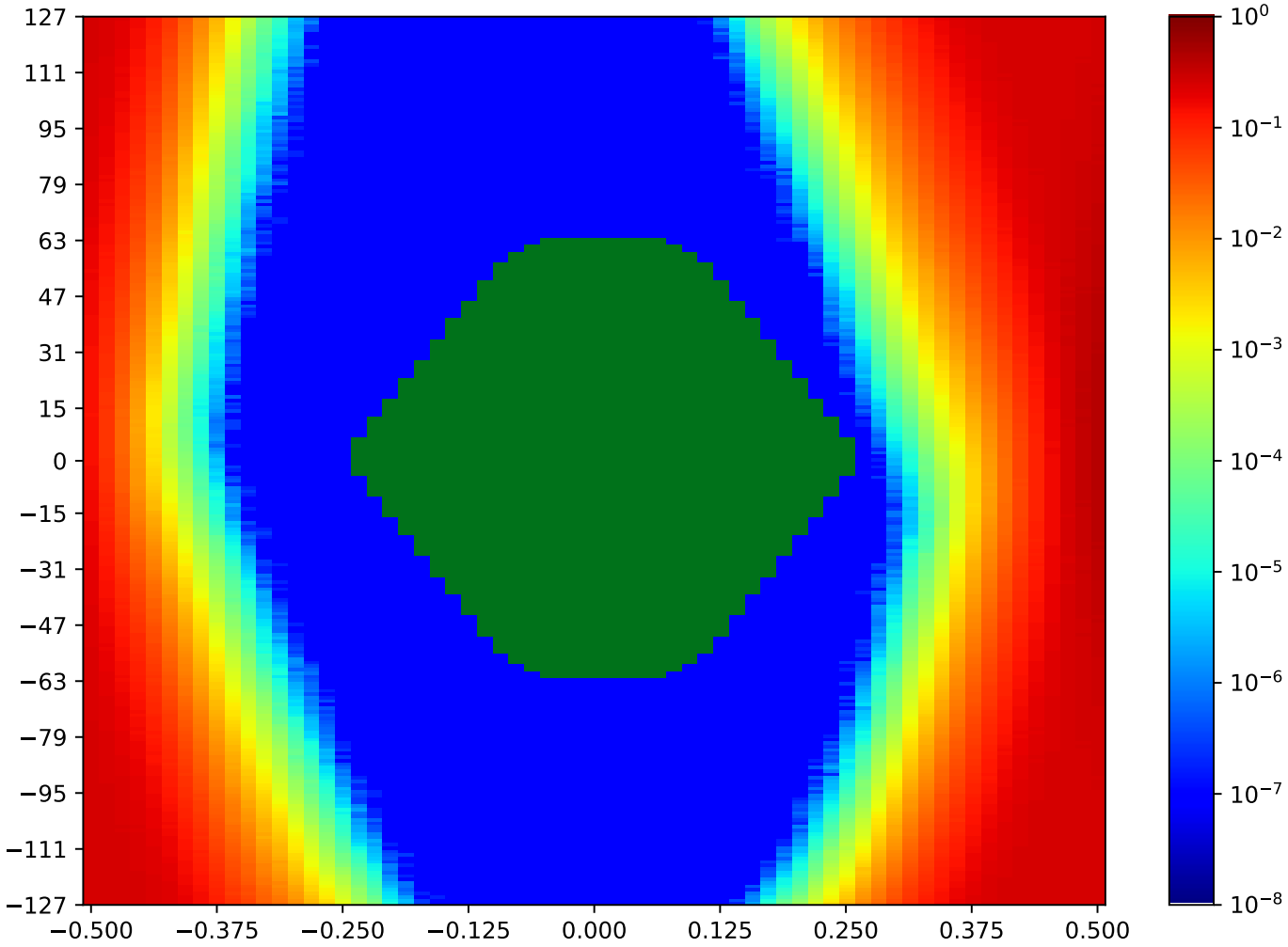


Figure 4.284: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.6 MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Table 4.263: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:35:27		2018-Sep-27 15:35:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7947	44	67.69%	218	85.49%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

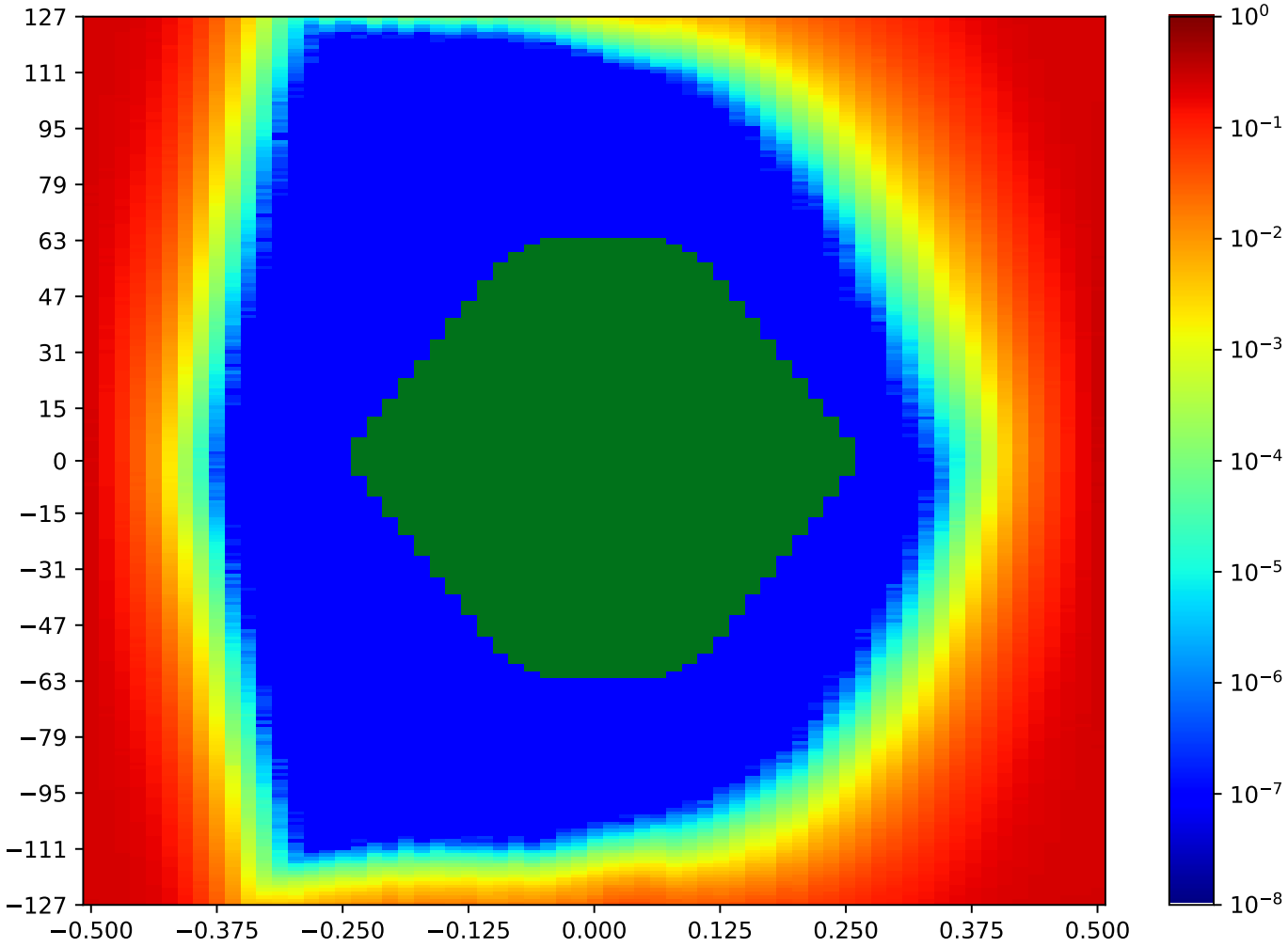


Figure 4.285: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.7 MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Table 4.264: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:38:35		2018-Sep-27 15:38:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9563	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

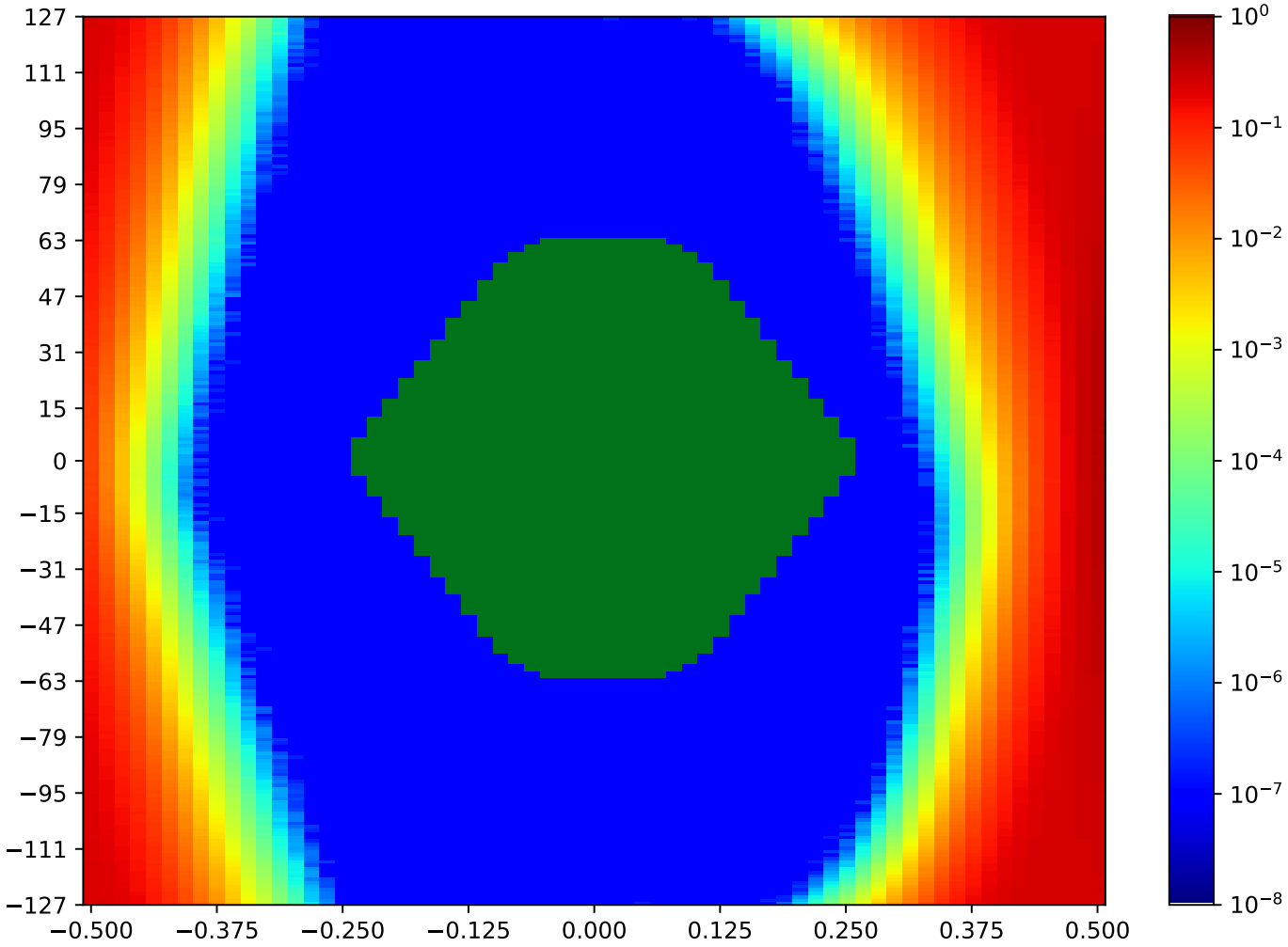


Figure 4.286: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.8 MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Table 4.265: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:36:08		2018-Sep-27 15:36:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8466	47	72.31%	226	88.63%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

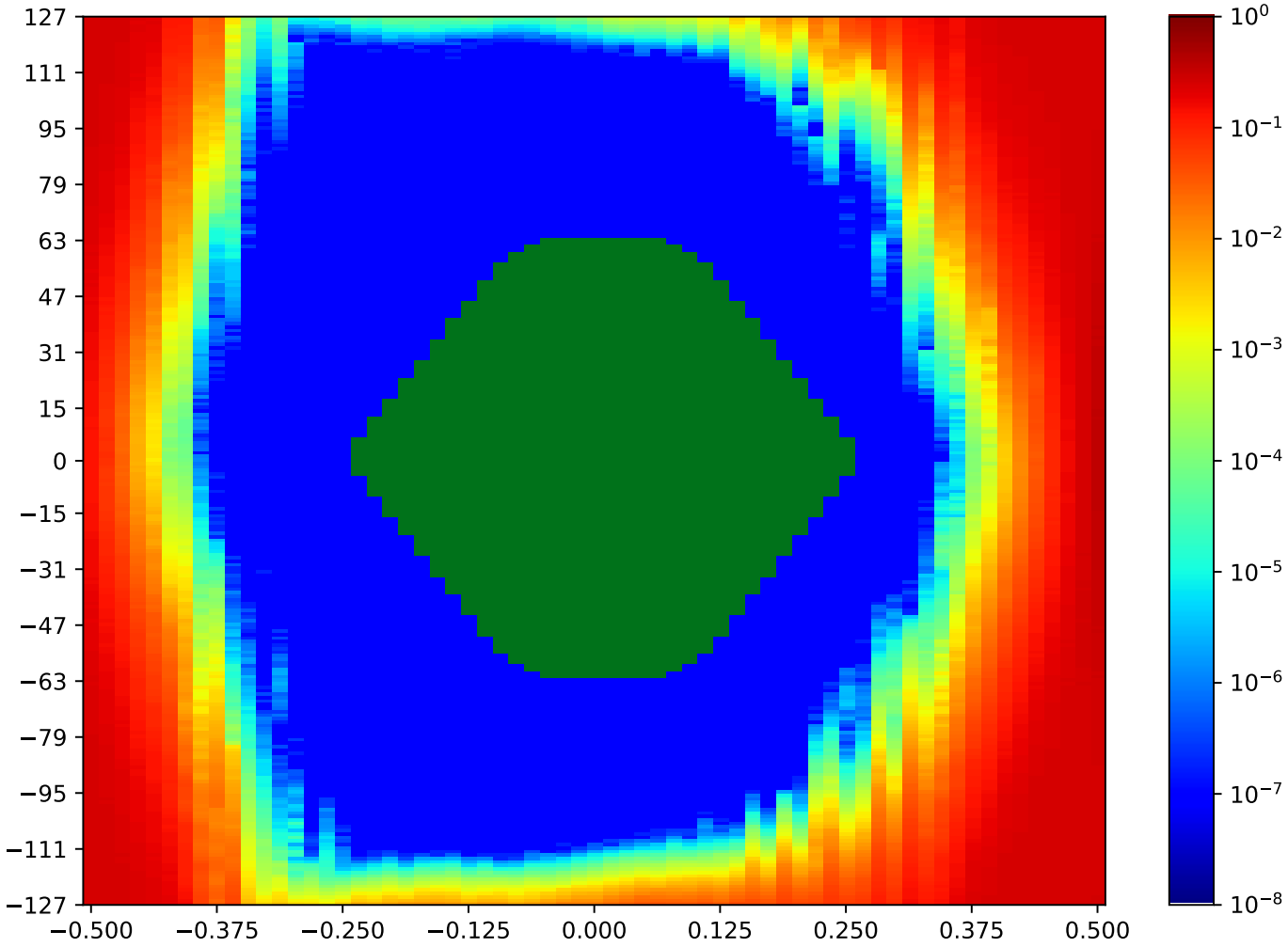


Figure 4.287: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.9 MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Table 4.266: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:38:15		2018-Sep-27 15:38:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9231	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

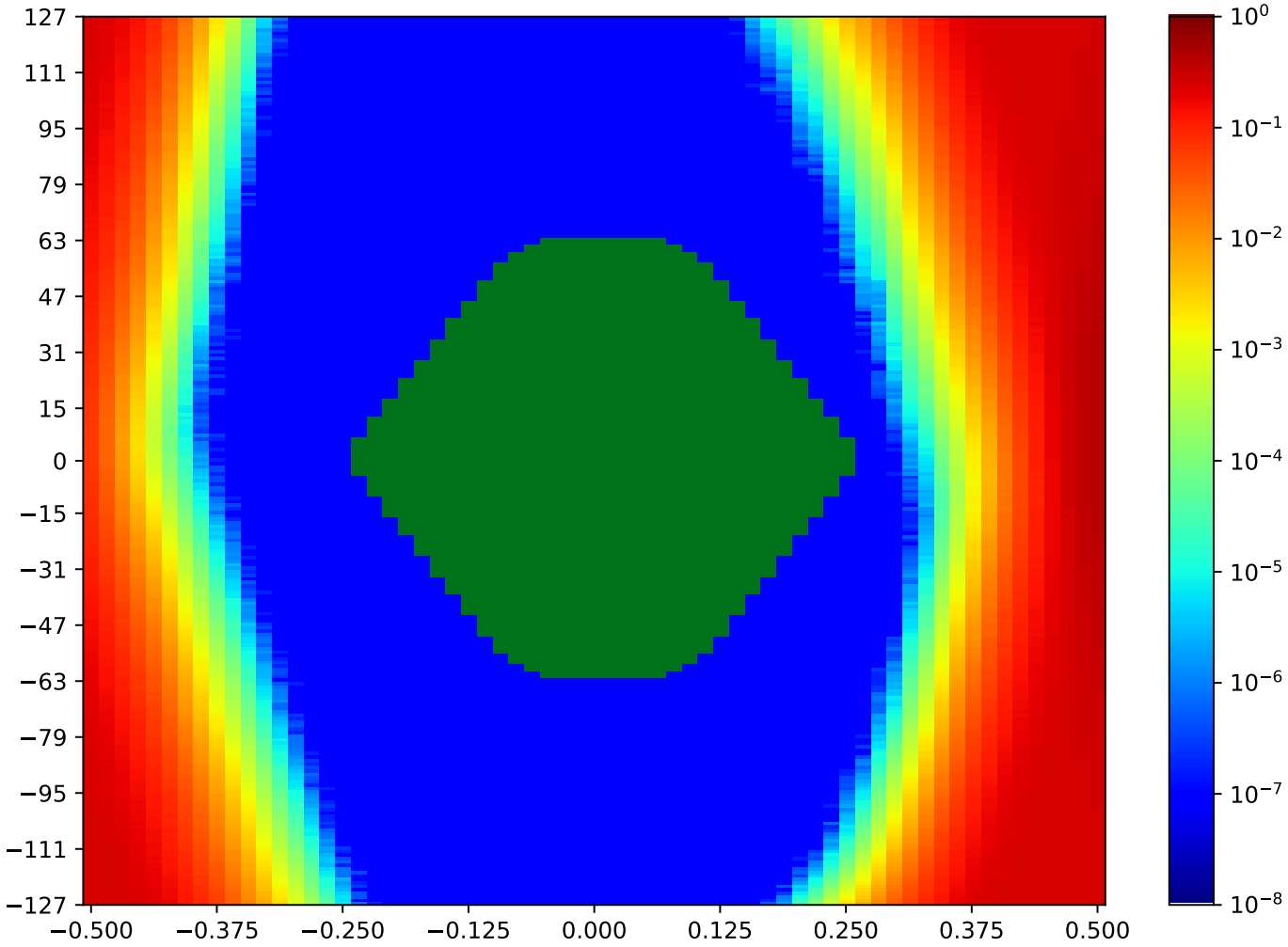


Figure 4.288: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.10 MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Table 4.267: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:36:29		2018-Sep-27 15:36:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9022	44	67.69%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

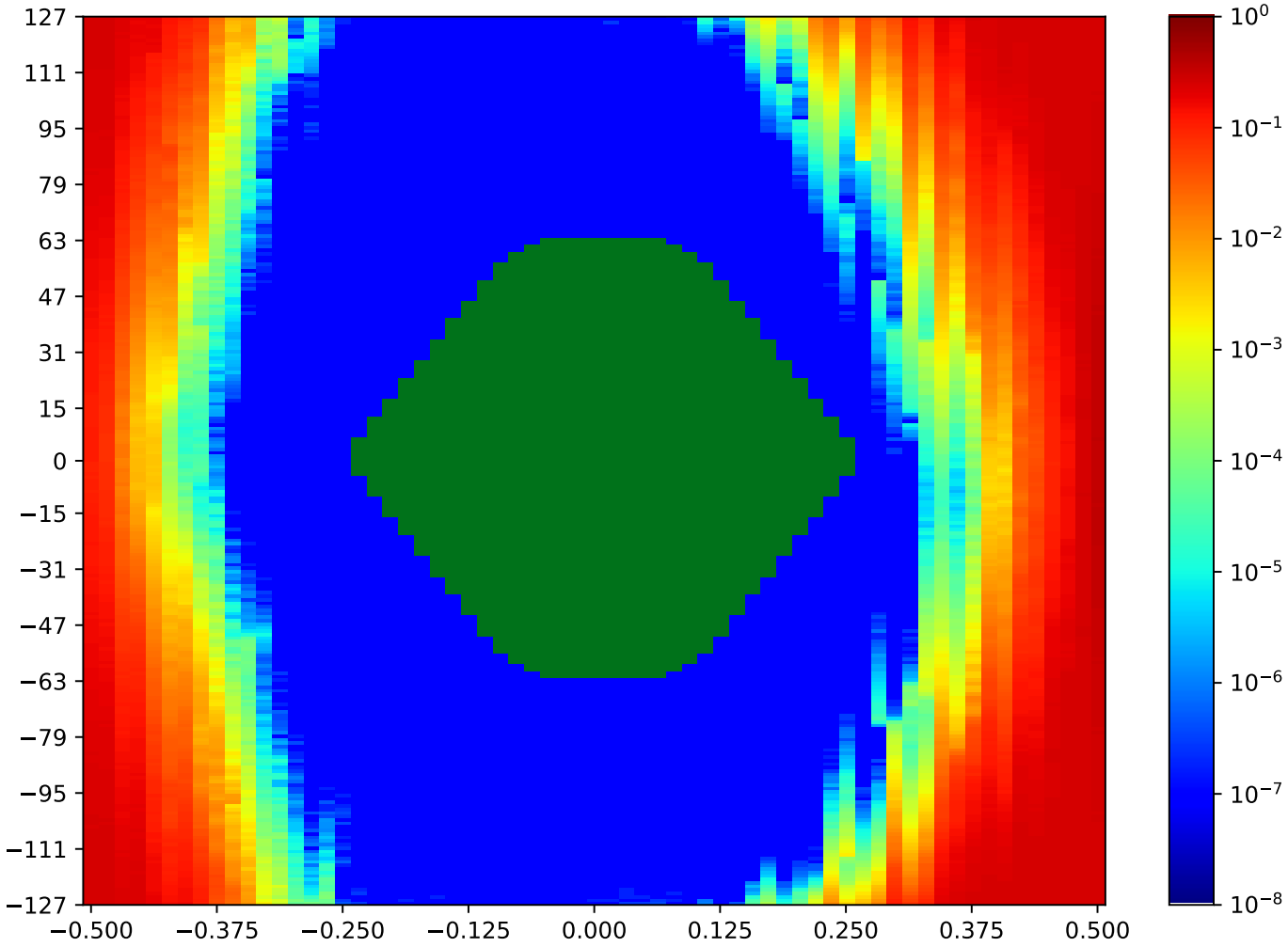


Figure 4.289: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.11 MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Table 4.268: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:37:30		2018-Sep-27 15:37:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9613	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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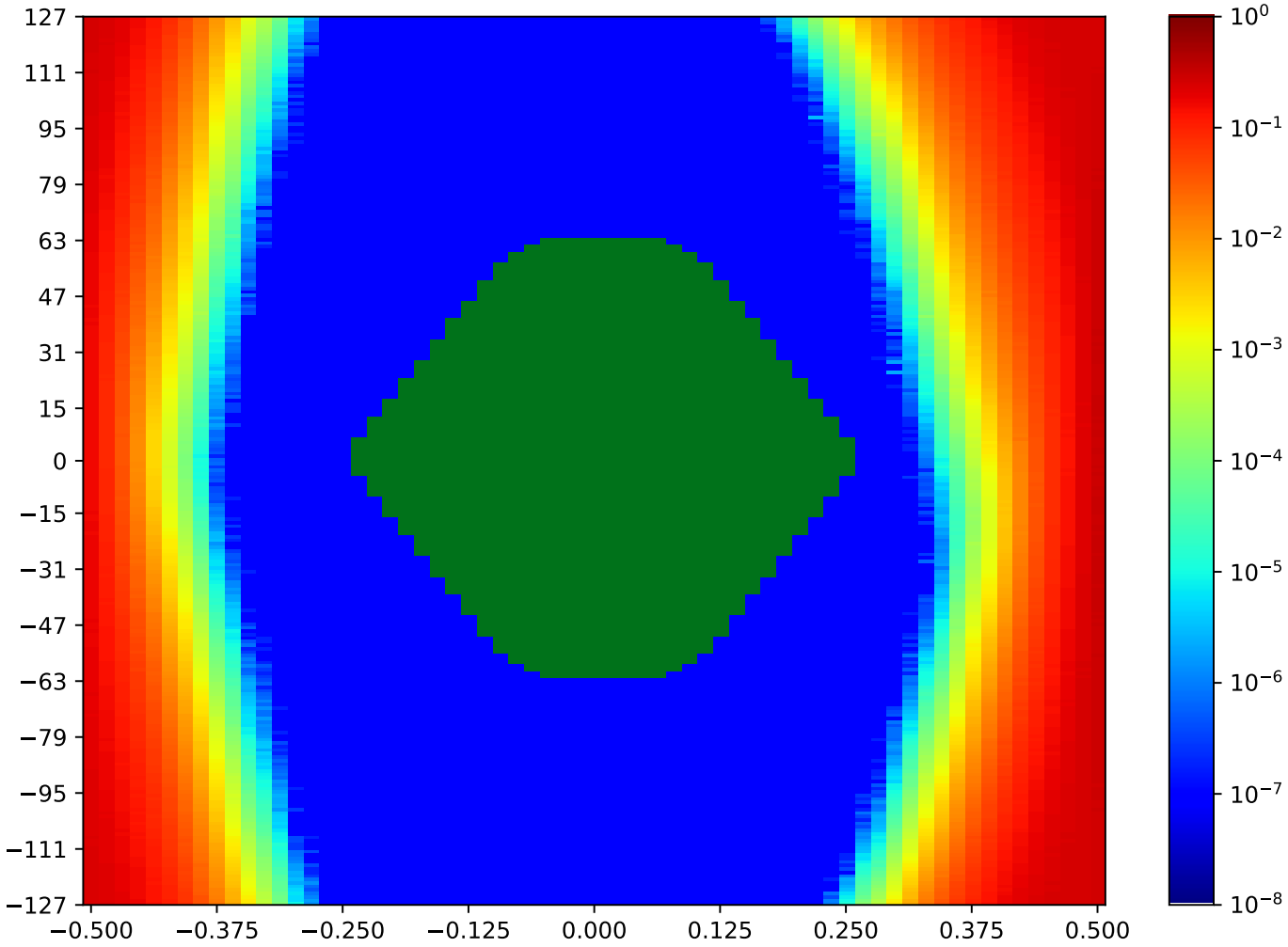


Figure 4.290: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

4.22.12 MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Table 4.269: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:37:09		2018-Sep-27 15:37:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9763	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

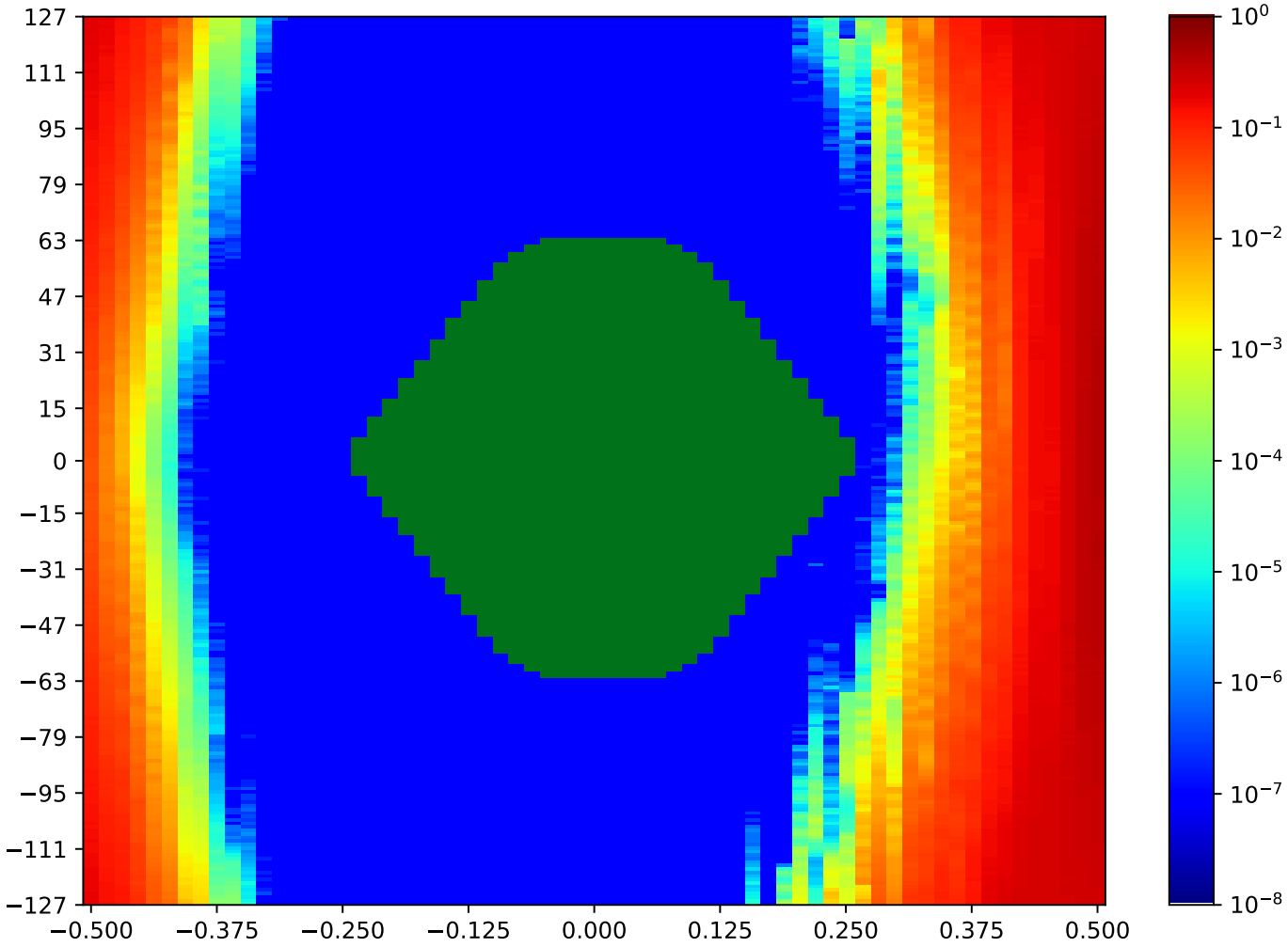


Figure 4.291: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-6.4, V3-6.4, V3-12.8.

Chapter 5

MUCTPI V3 6.4 Gbps

5.1 MSP_A TX1 MSP_C RX15 Minipod Loopback

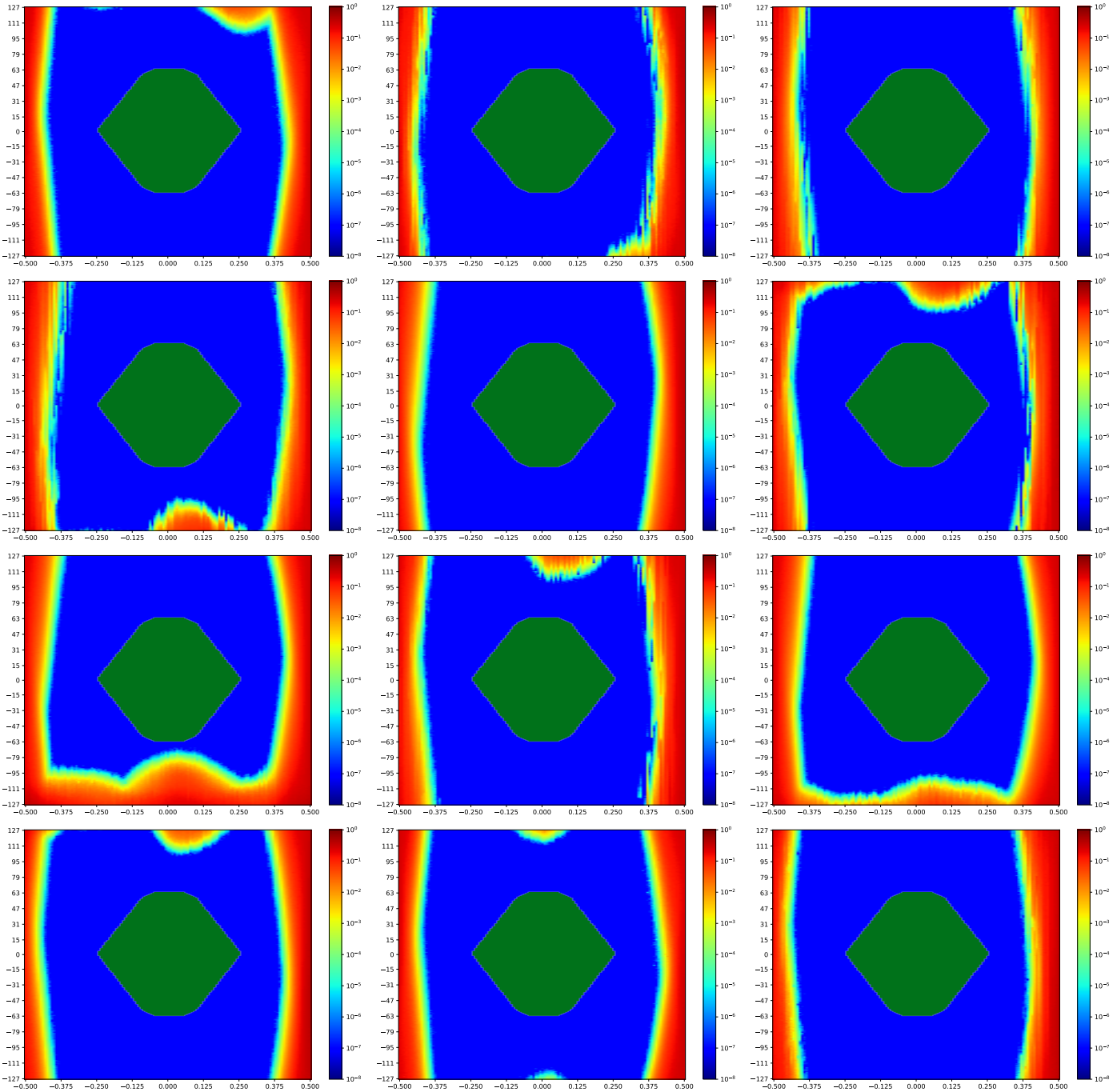


Figure 5.1: MSP_A TX1 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.14.

5.1.1 MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Table 5.1: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:28:42		2019-Nov-26 10:30:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23981	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

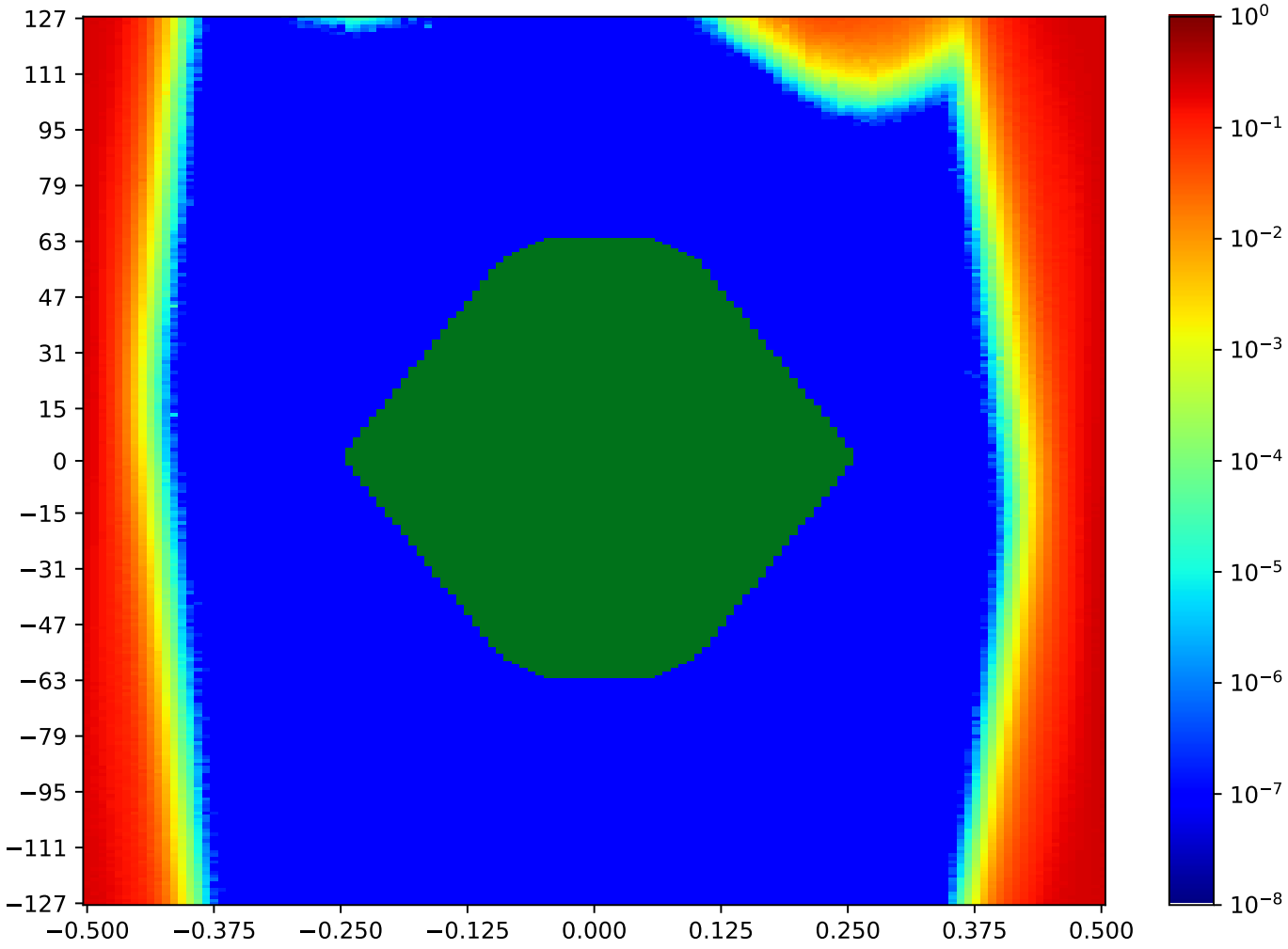


Figure 5.2: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.2 MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Table 5.2: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:31:10		2019-Nov-26 10:32:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24511	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

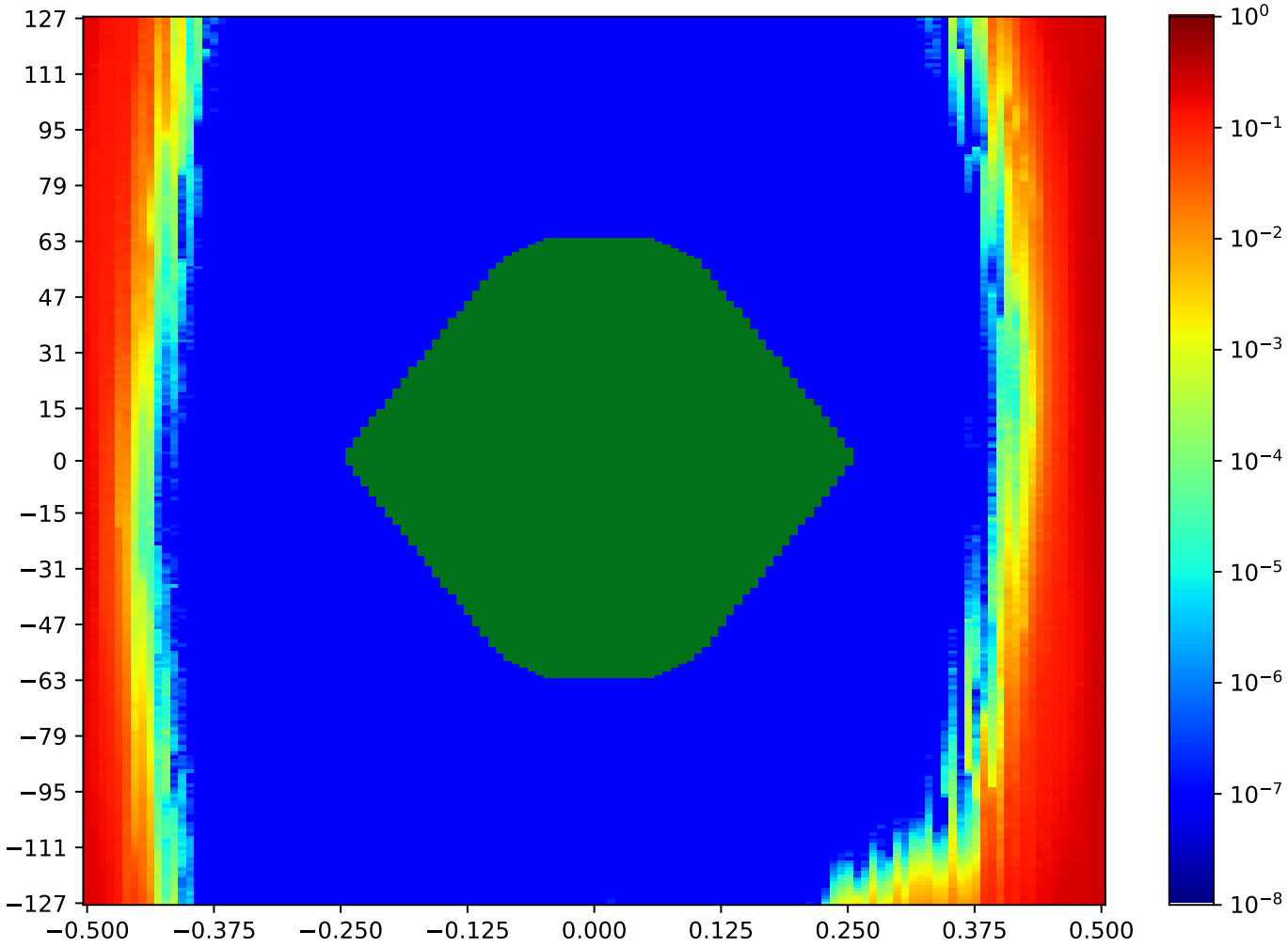


Figure 5.3: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.3 MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Table 5.3: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:32:32		2019-Nov-26 10:33:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24001	100	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

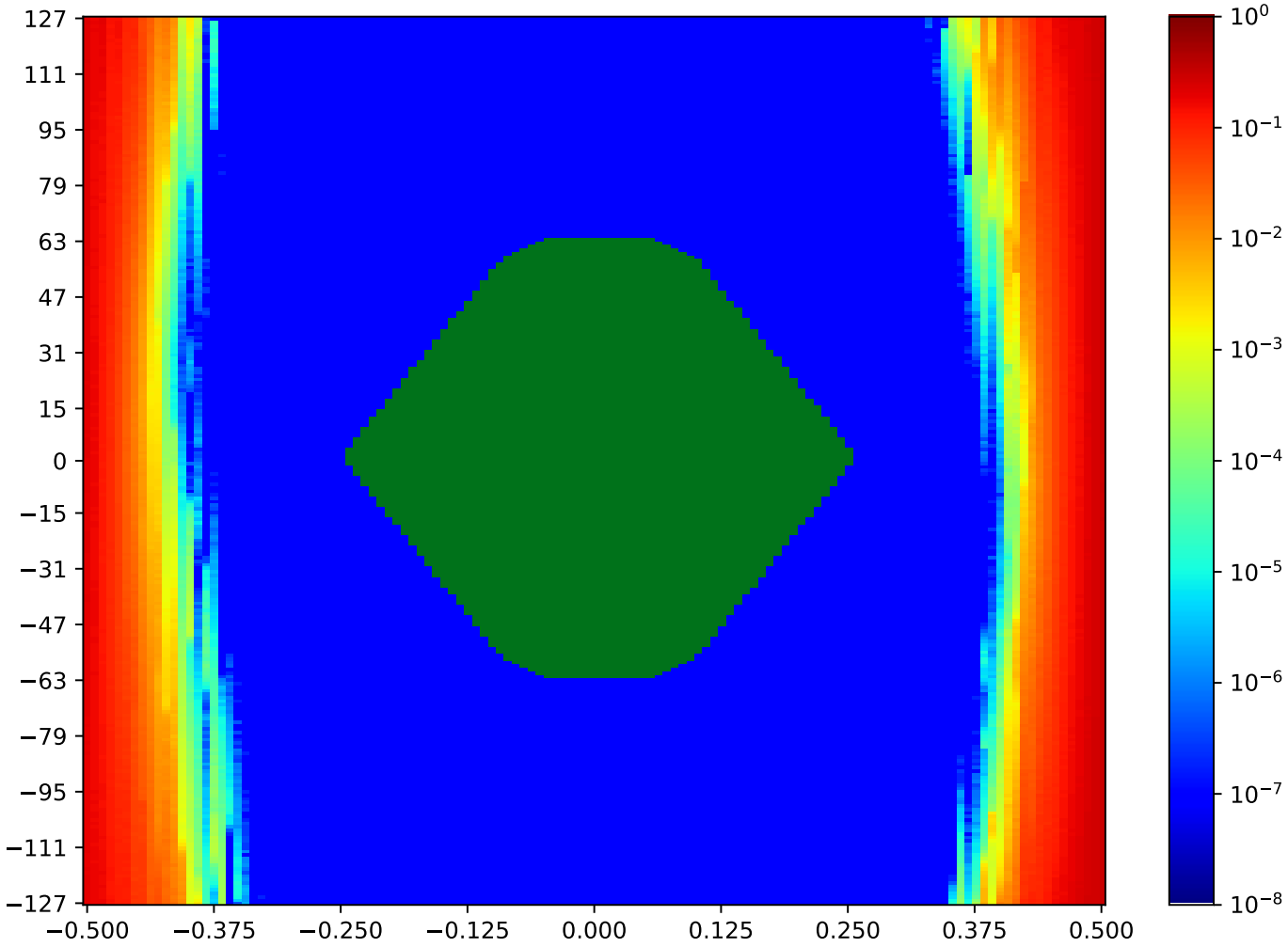


Figure 5.4: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.4 MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Table 5.4: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:26:27		2019-Nov-26 10:27:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22994	99	75.19%	224	87.84%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

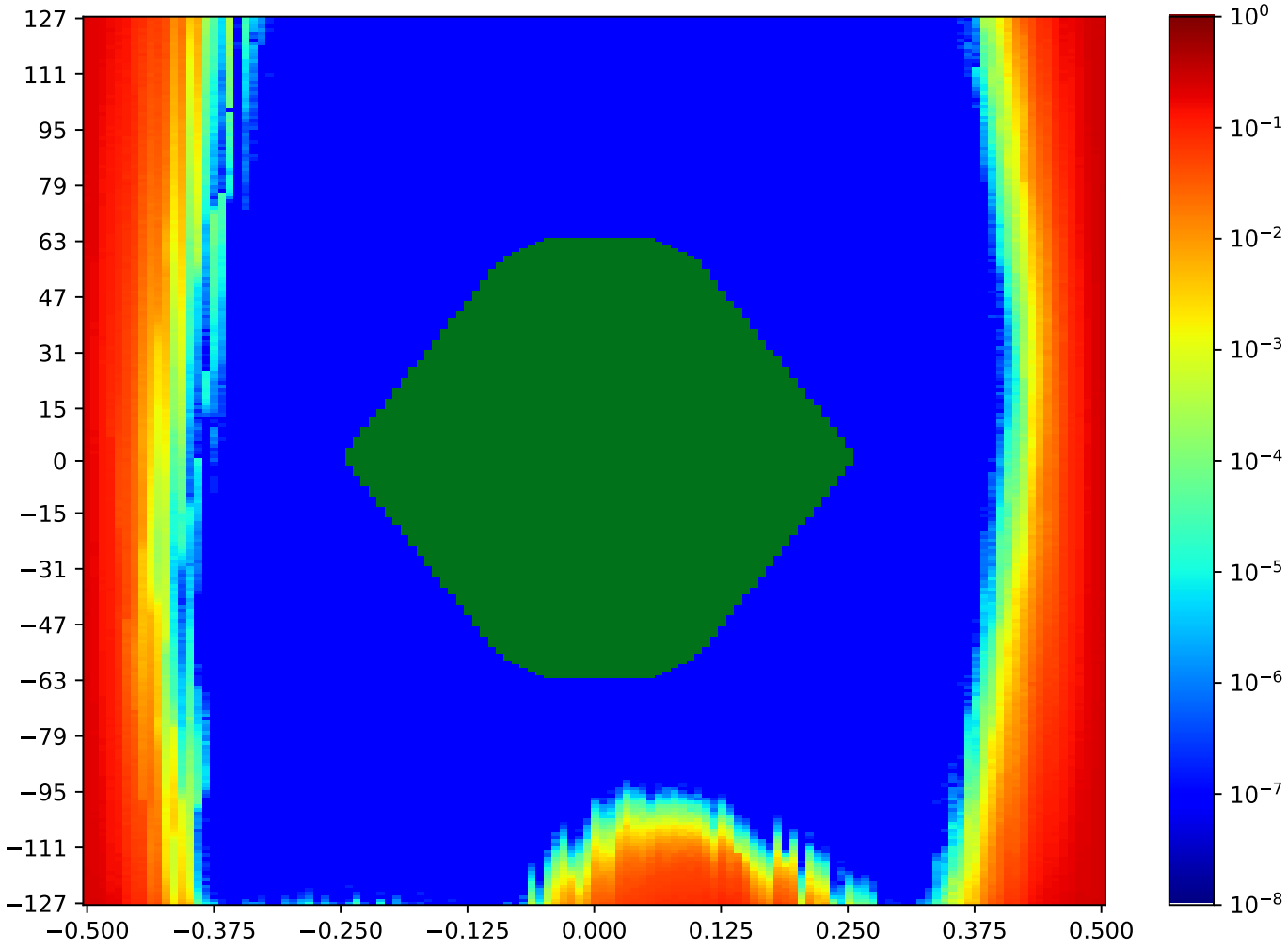


Figure 5.5: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.5 MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Table 5.5: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:36:21		2019-Nov-26 10:37:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24507	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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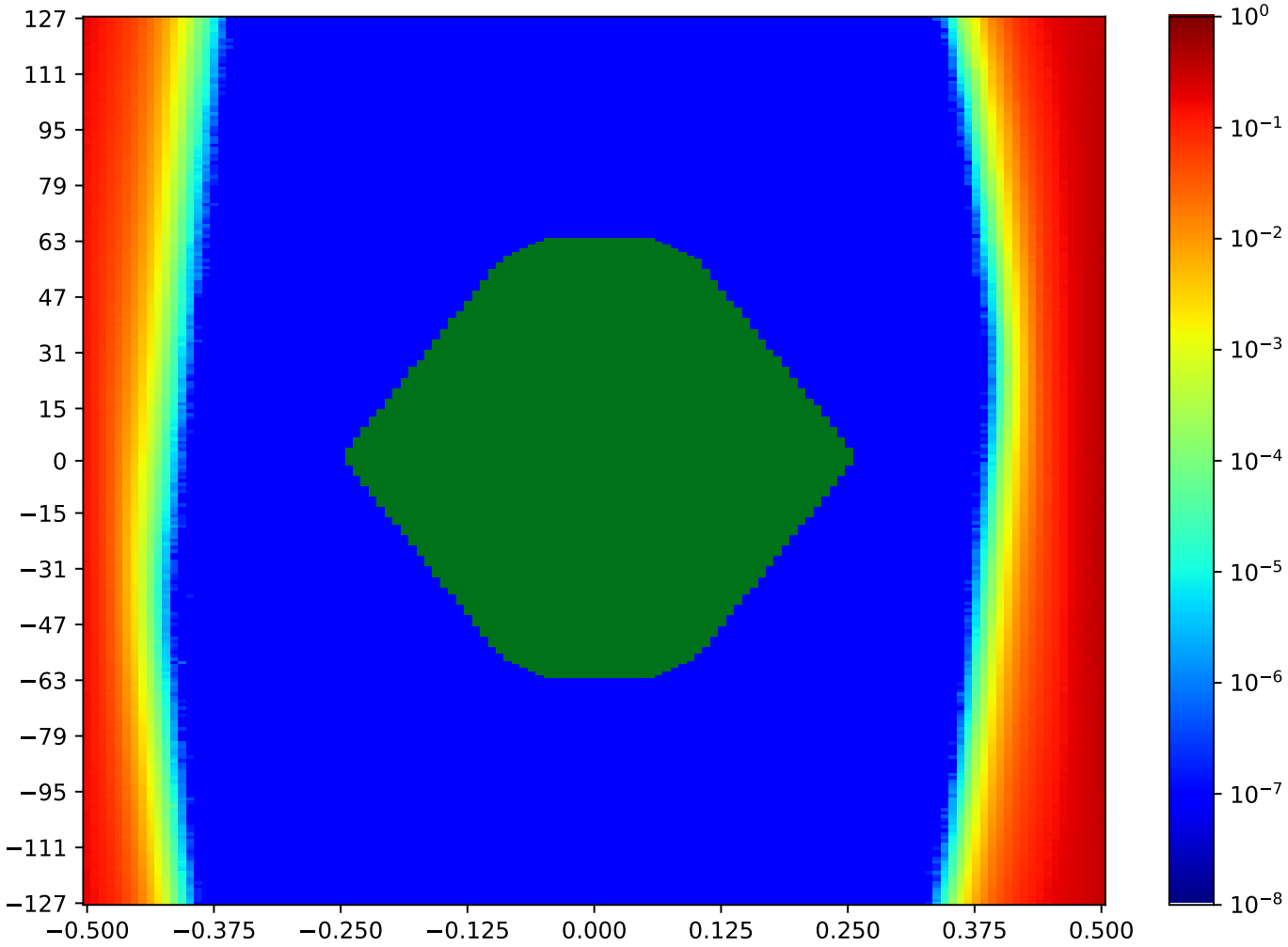


Figure 5.6: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.6 MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Table 5.6: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:25:20		2019-Nov-26 10:26:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22931	102	78.29%	226	88.24%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

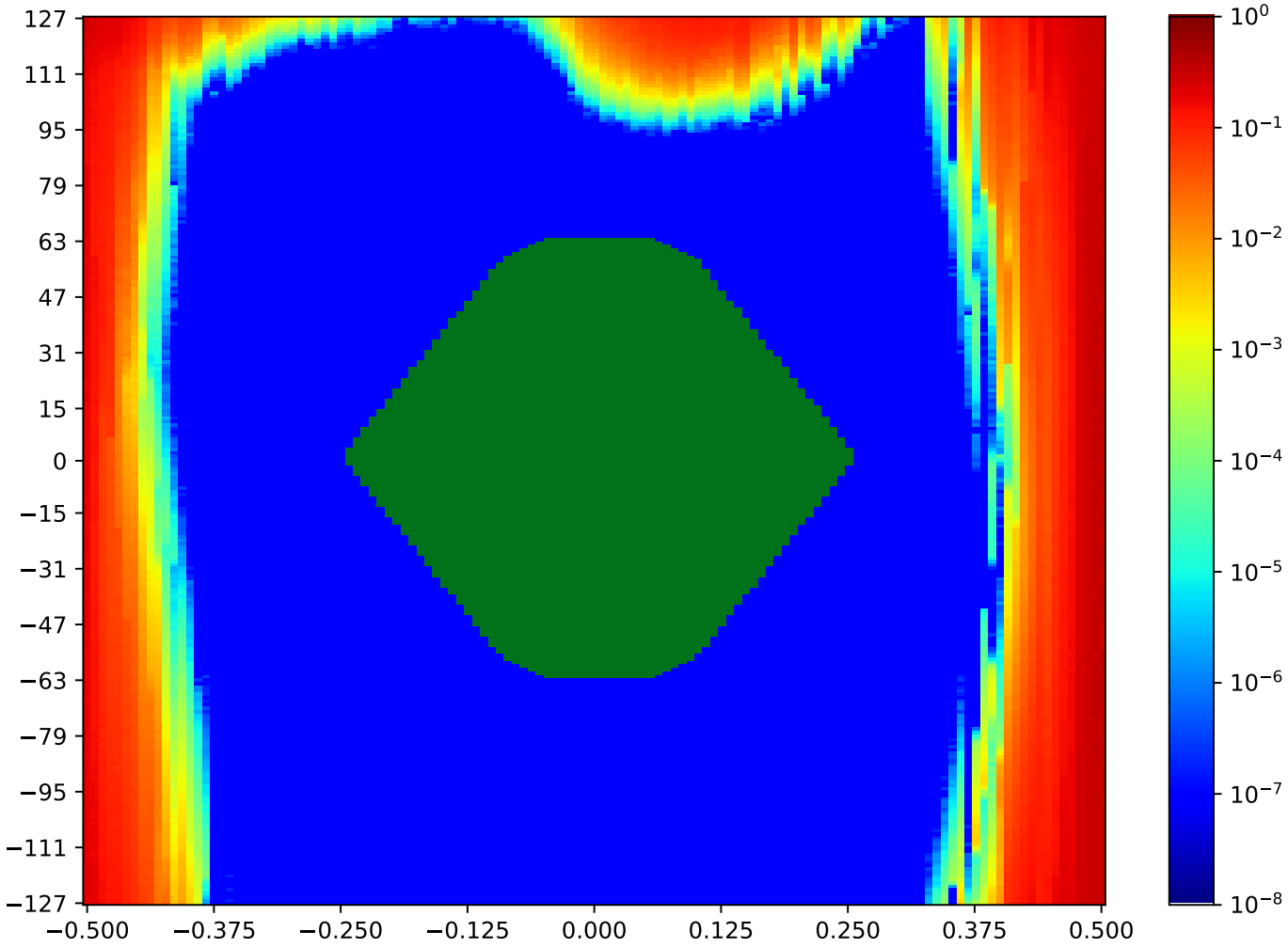


Figure 5.7: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.7 MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Table 5.7: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:38:35		2019-Nov-26 10:39:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	20430	101	78.29%	197	76.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

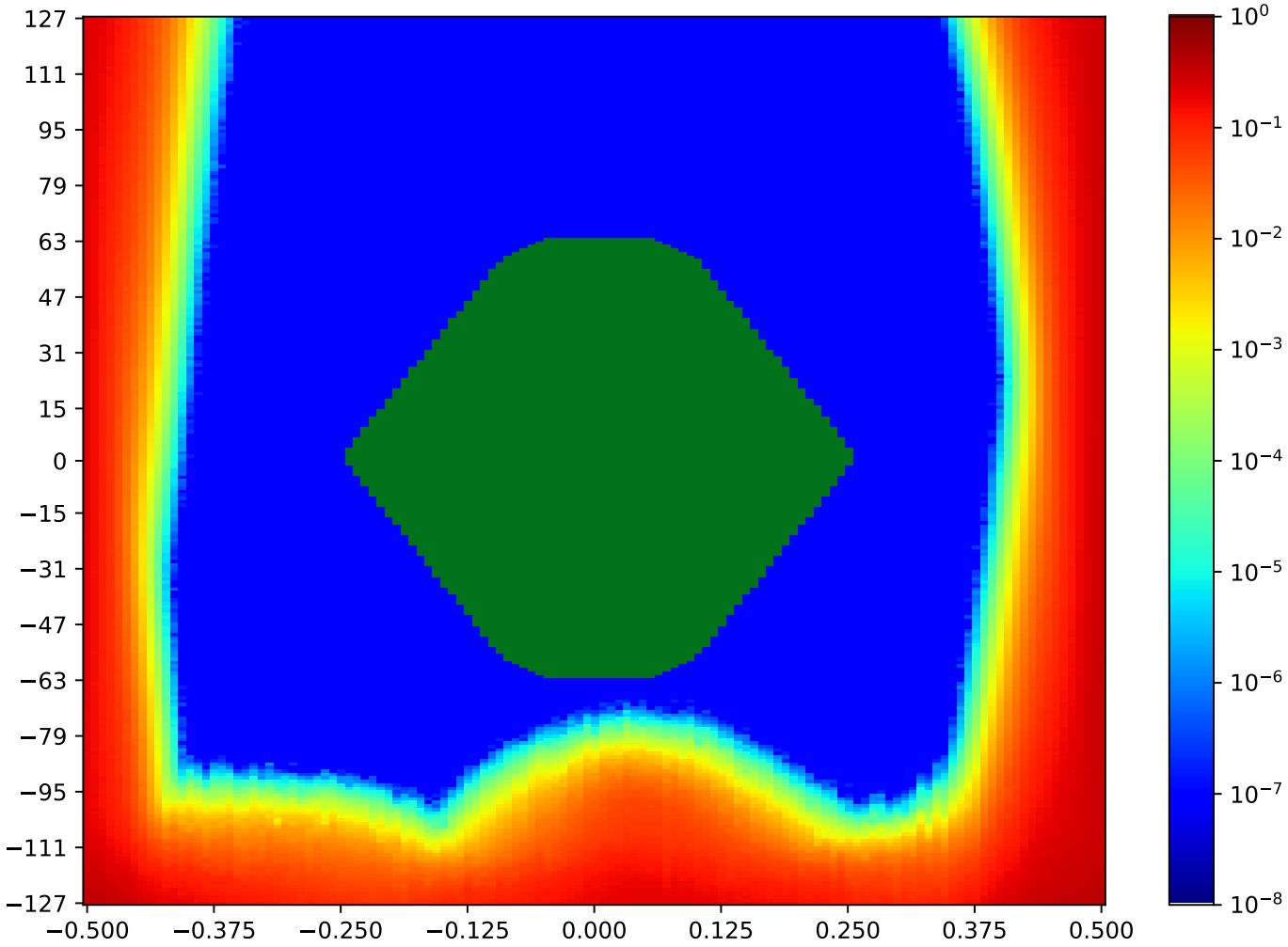


Figure 5.8: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.8 MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Table 5.8: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:27:35		2019-Nov-26 10:28:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23490	97	75.19%	235	91.76%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

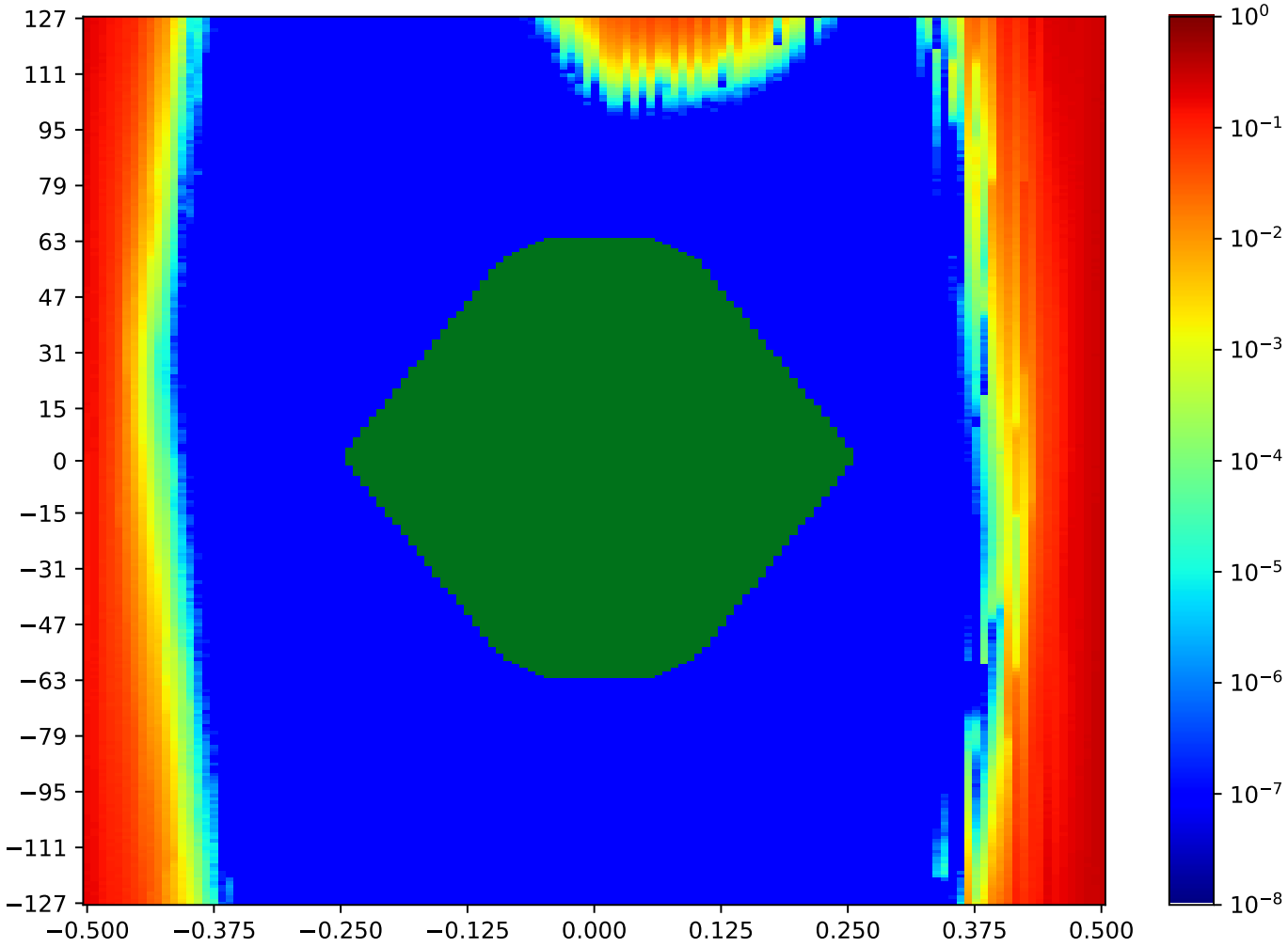


Figure 5.9: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.9 MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Table 5.9: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:37:28		2019-Nov-26 10:38:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22212	99	76.74%	226	88.63%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

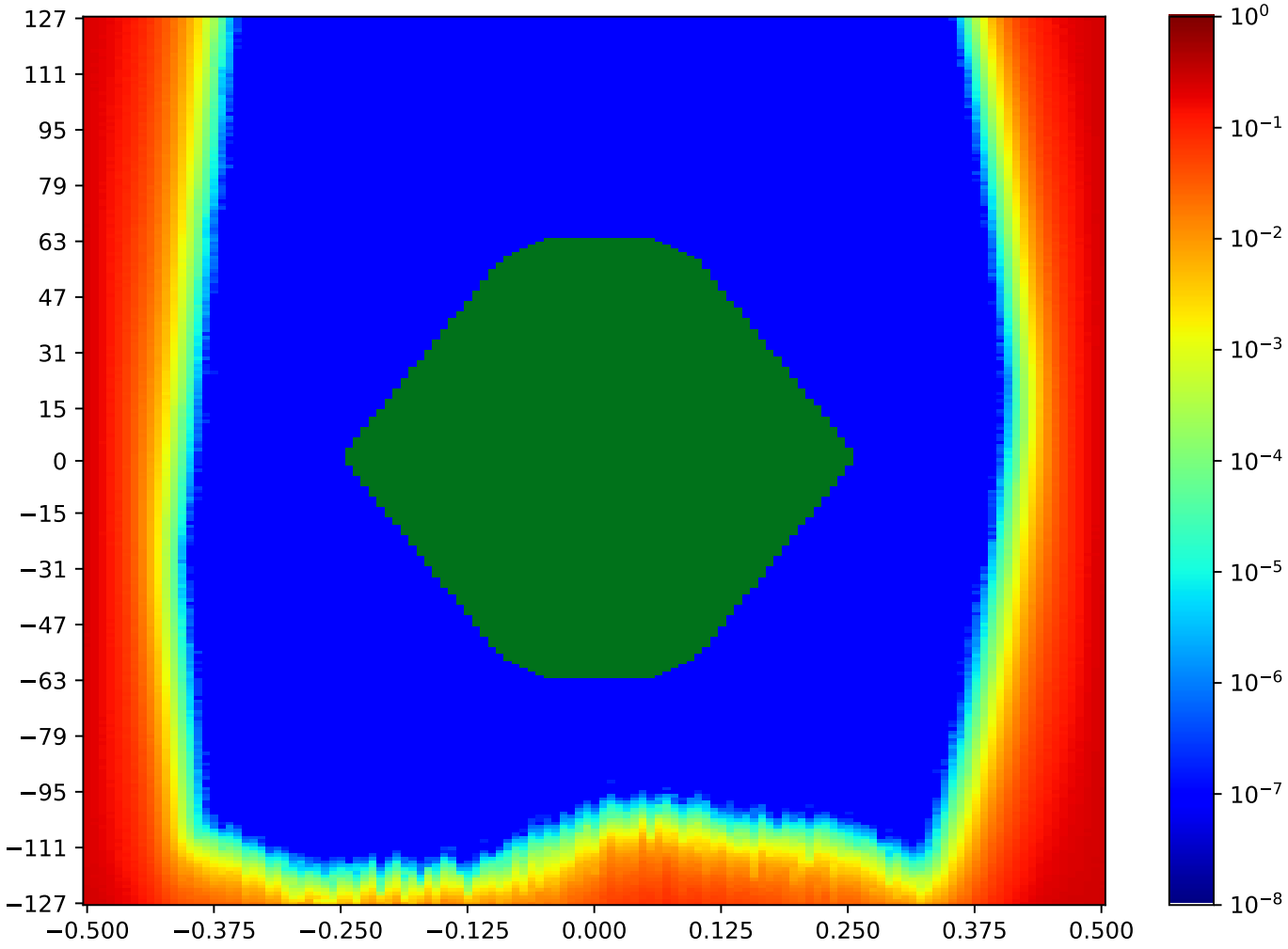


Figure 5.10: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.10 MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Table 5.10: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:30:02		2019-Nov-26 10:31:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24441	102	79.07%	231	90.59%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

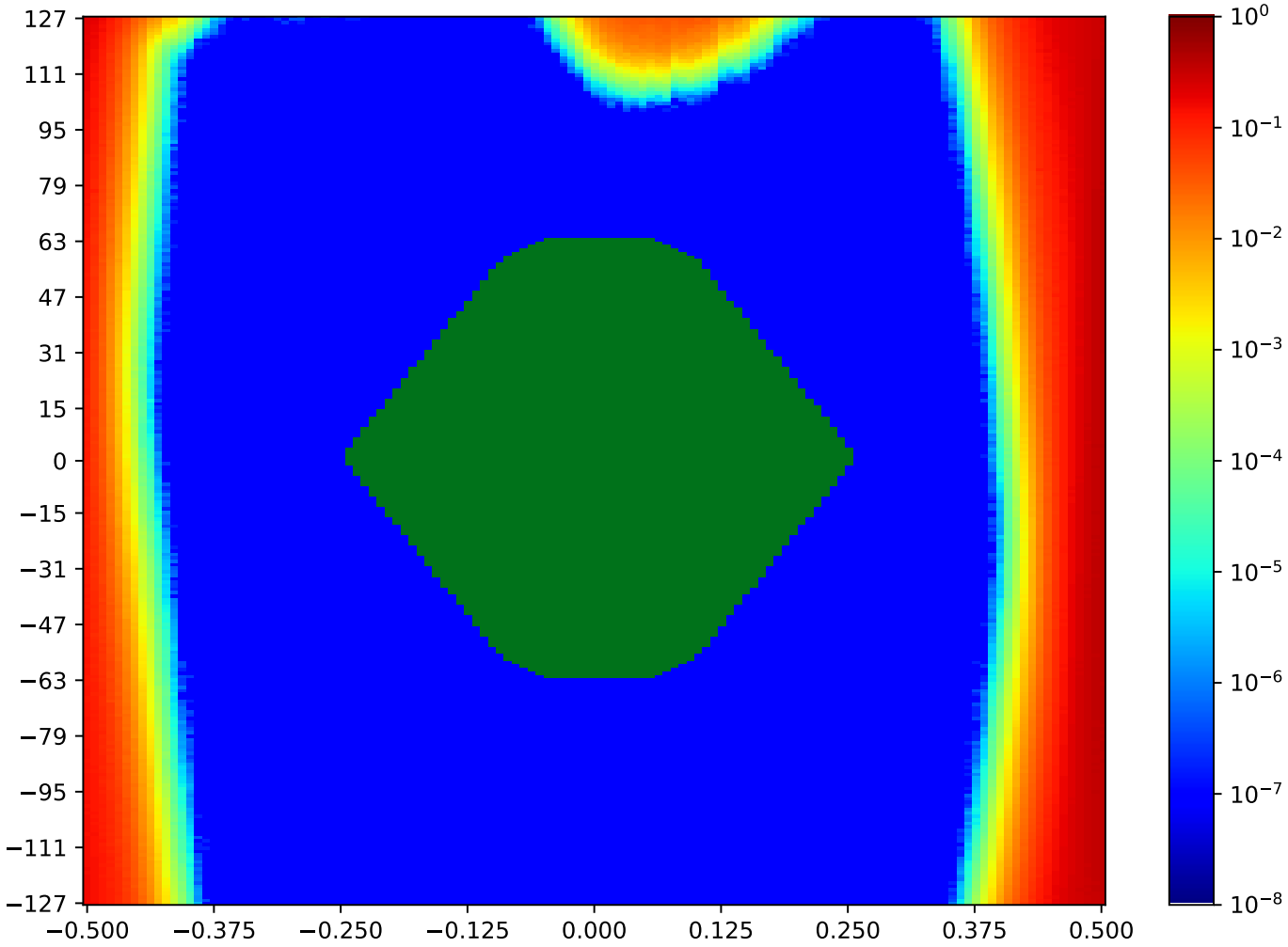


Figure 5.11: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.11 MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Table 5.11: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:35:04		2019-Nov-26 10:36:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24403	103	79.07%	230	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

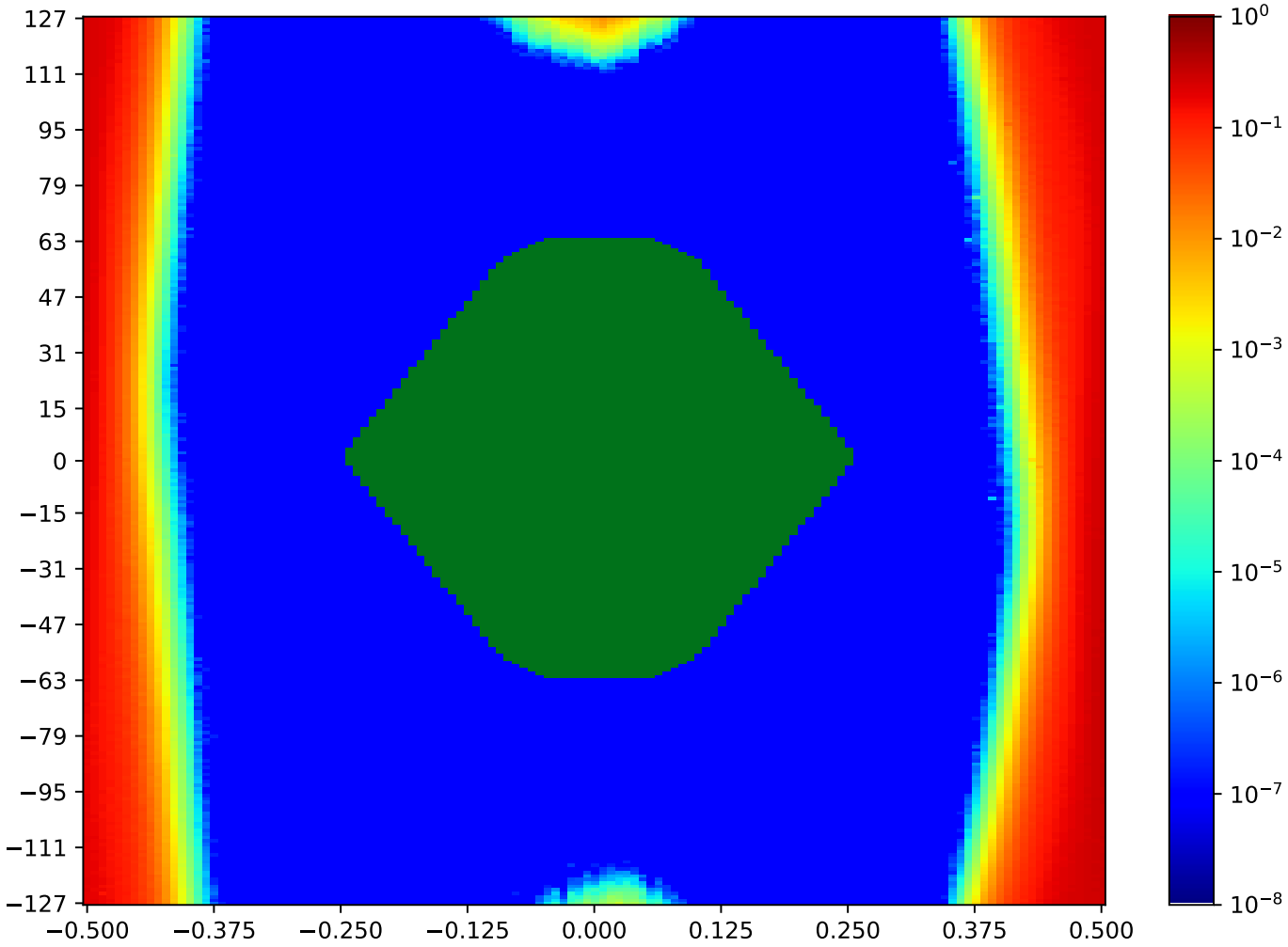


Figure 5.12: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.1.12 MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Table 5.12: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:33:39		2019-Nov-26 10:35:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24929	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

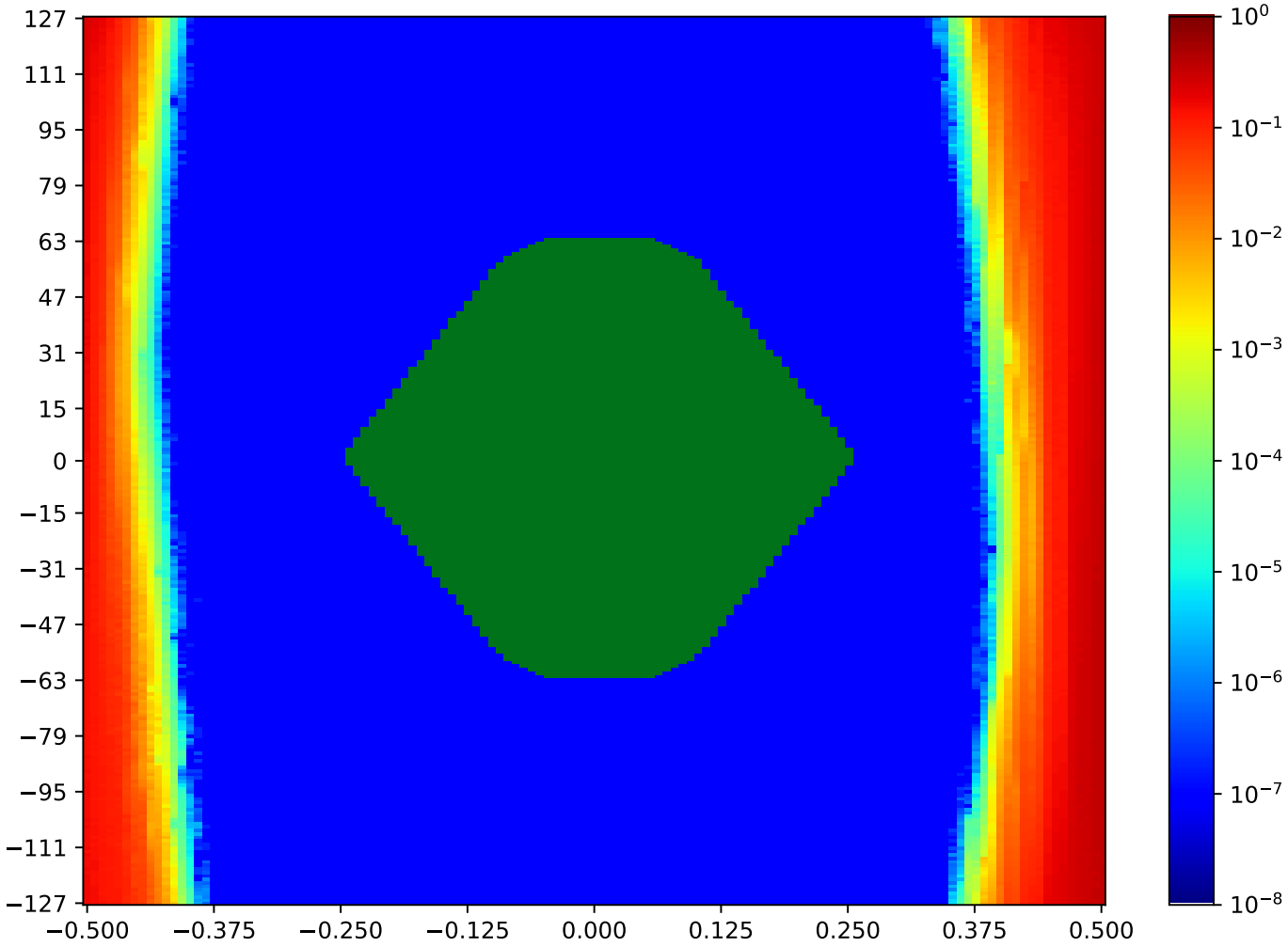


Figure 5.13: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2 MSP_A TX2 MSP_C RX16 Minipod Loopback

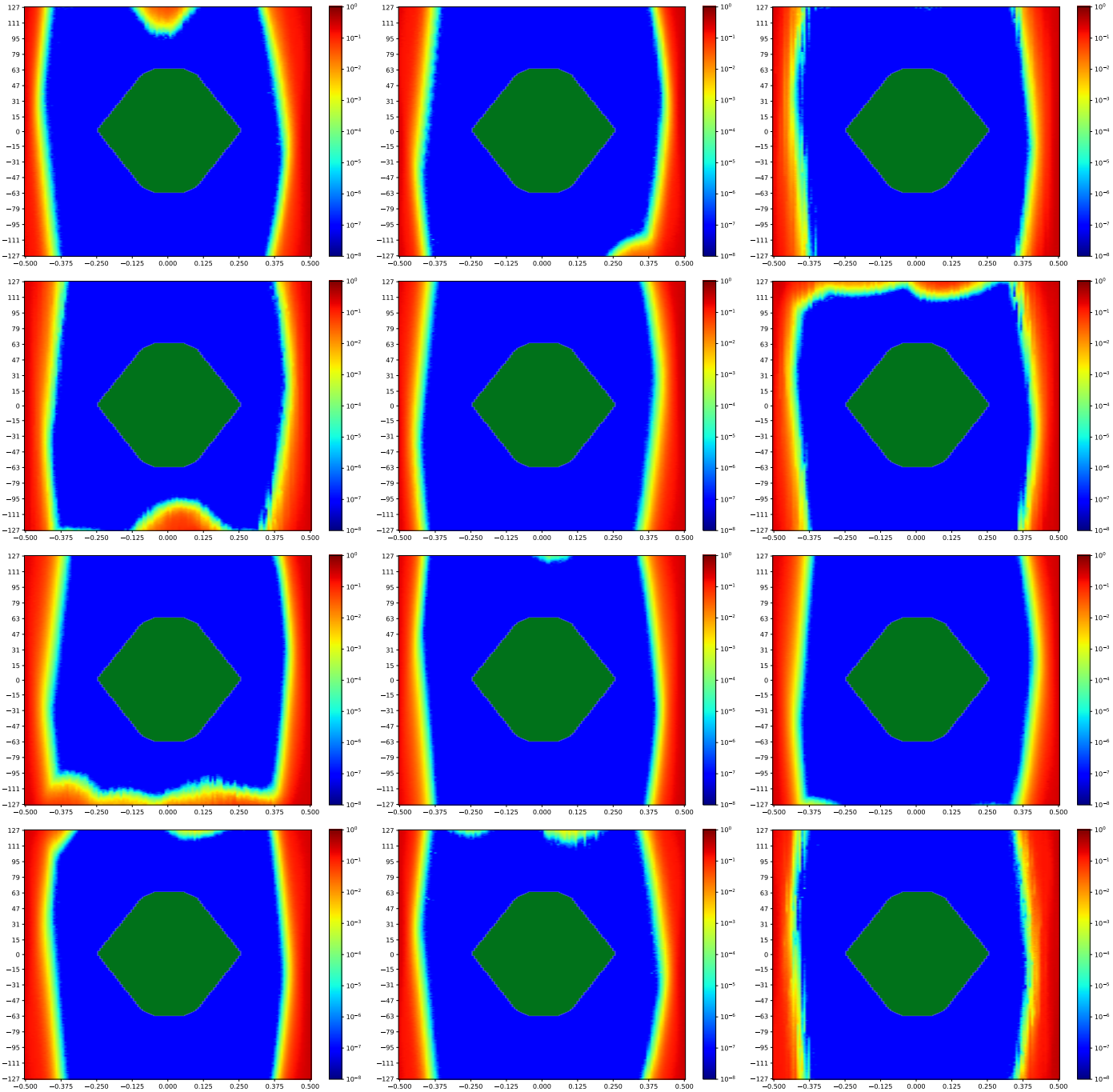


Figure 5.14: MSP_A TX2 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.27.

5.2.1 MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Table 5.13: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:43:39		2019-Nov-26 10:44:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23879	101	78.29%	224	86.67%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

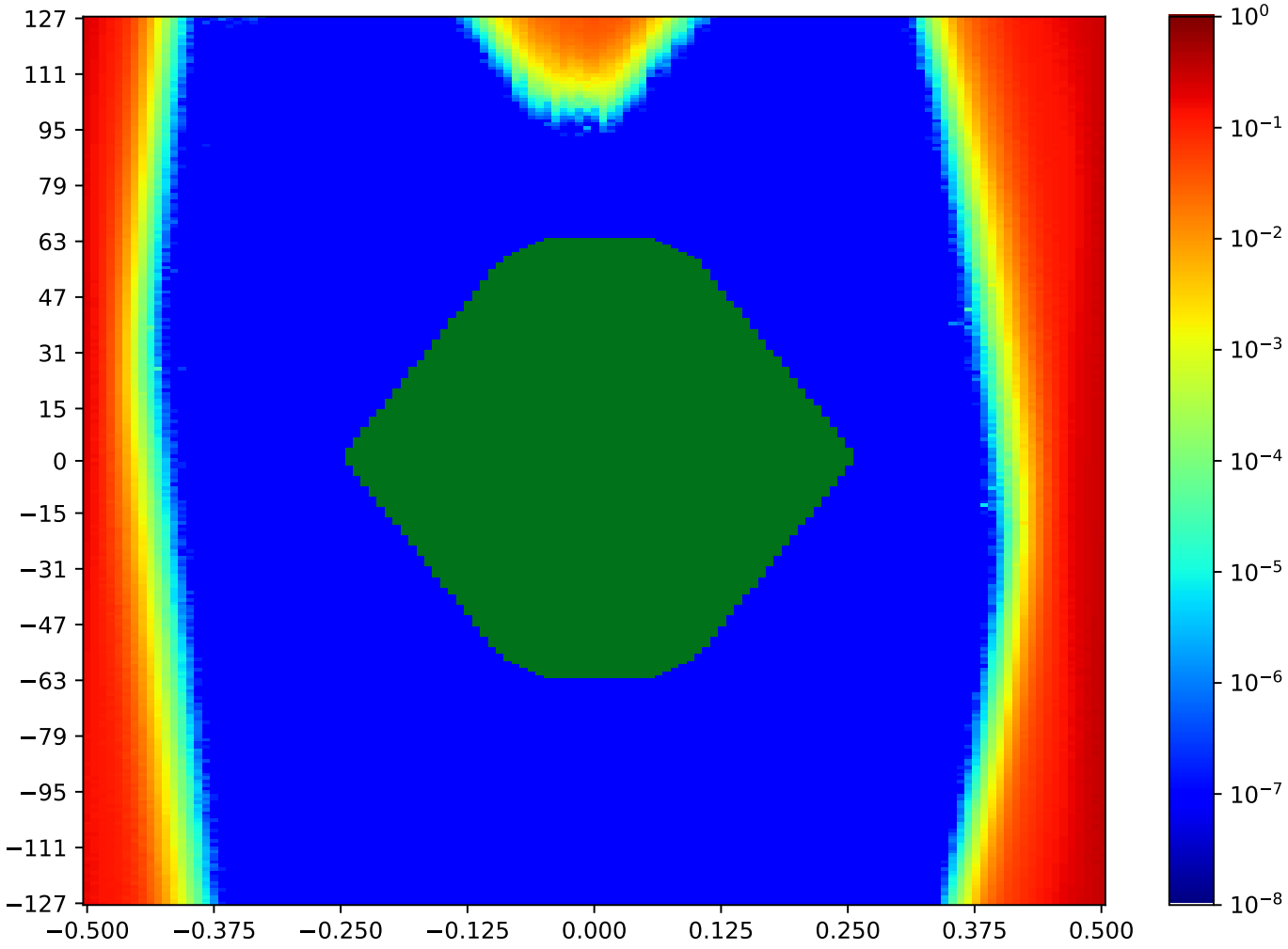


Figure 5.15: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.2 MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Table 5.14: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:41:03		2019-Nov-26 10:42:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24525	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

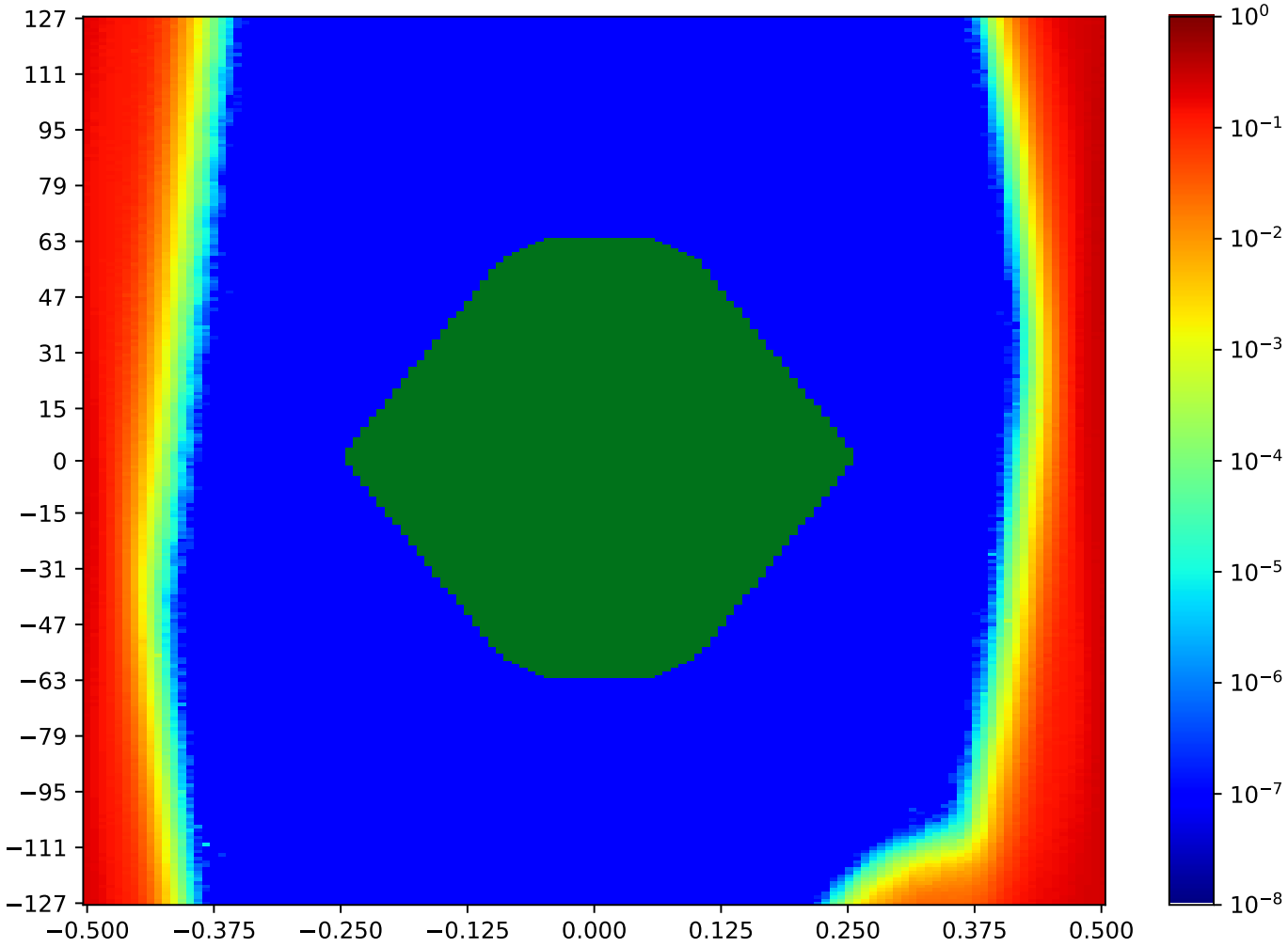


Figure 5.16: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.3 MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Table 5.15: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:47:14		2019-Nov-26 10:48:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24136	97	75.19%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

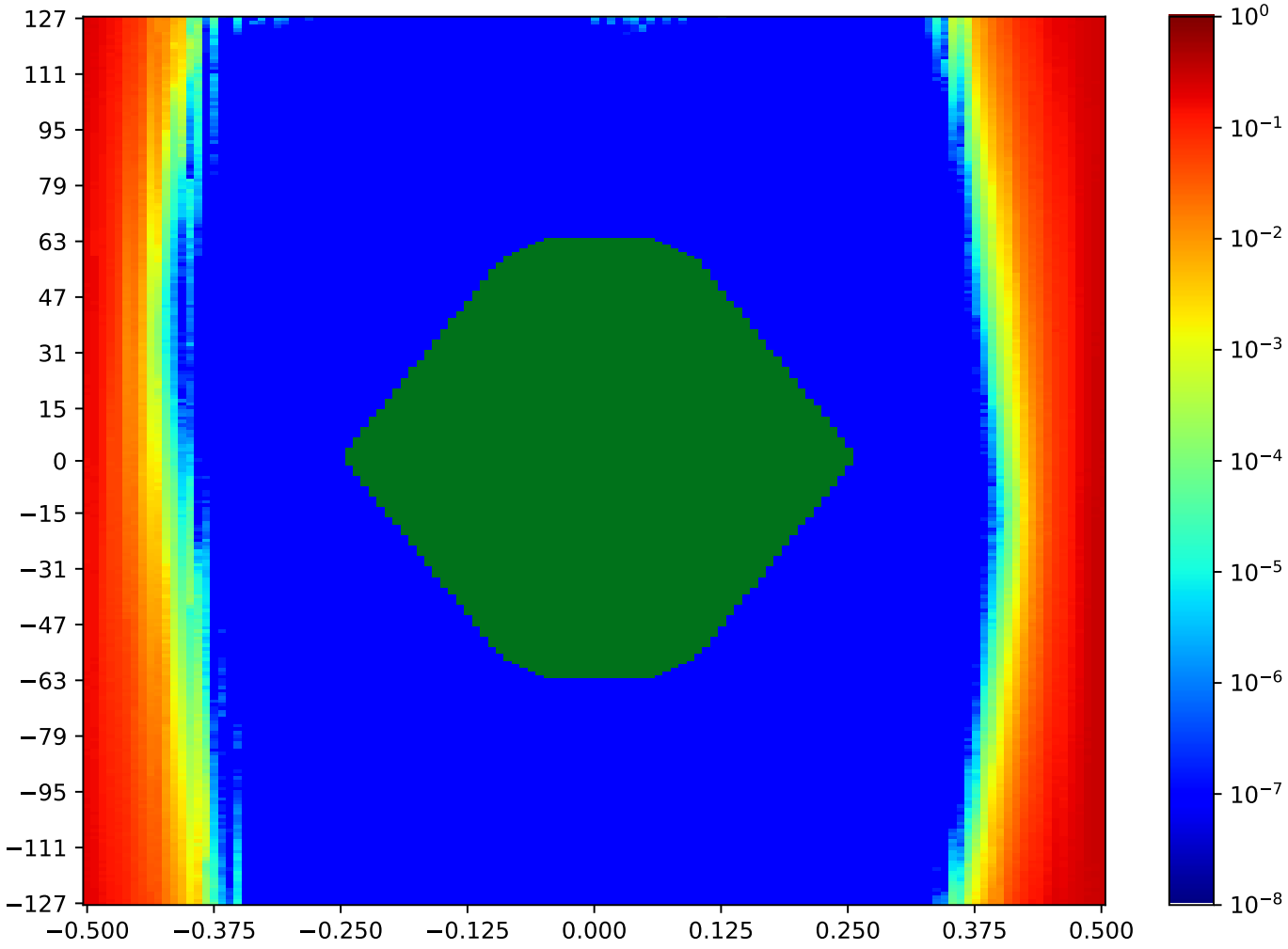


Figure 5.17: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.4 MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Table 5.16: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:39:43		2019-Nov-26 10:41:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23037	99	76.74%	221	86.67%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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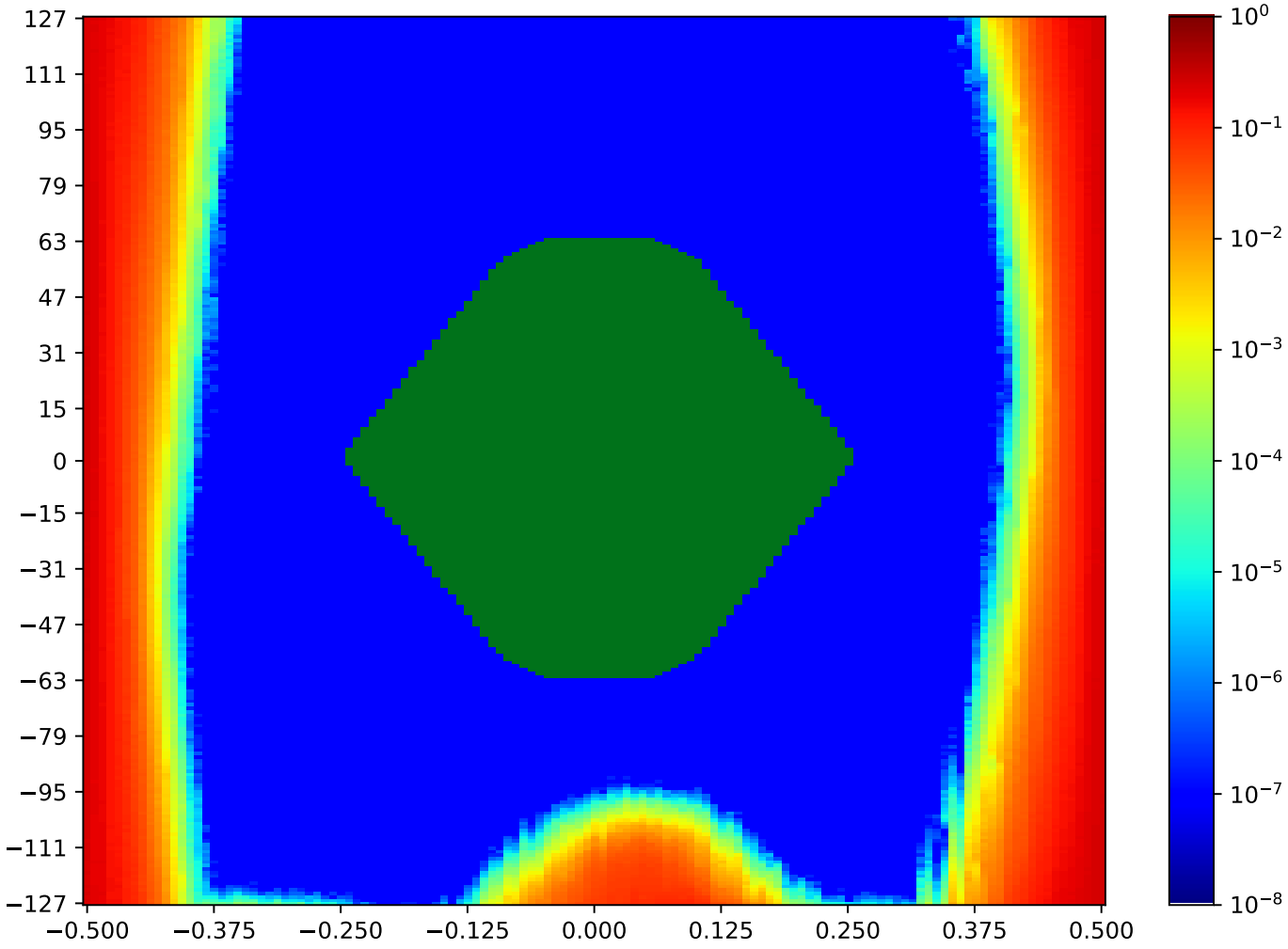


Figure 5.18: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.5 MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Table 5.17: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:50:55		2019-Nov-26 10:52:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24359	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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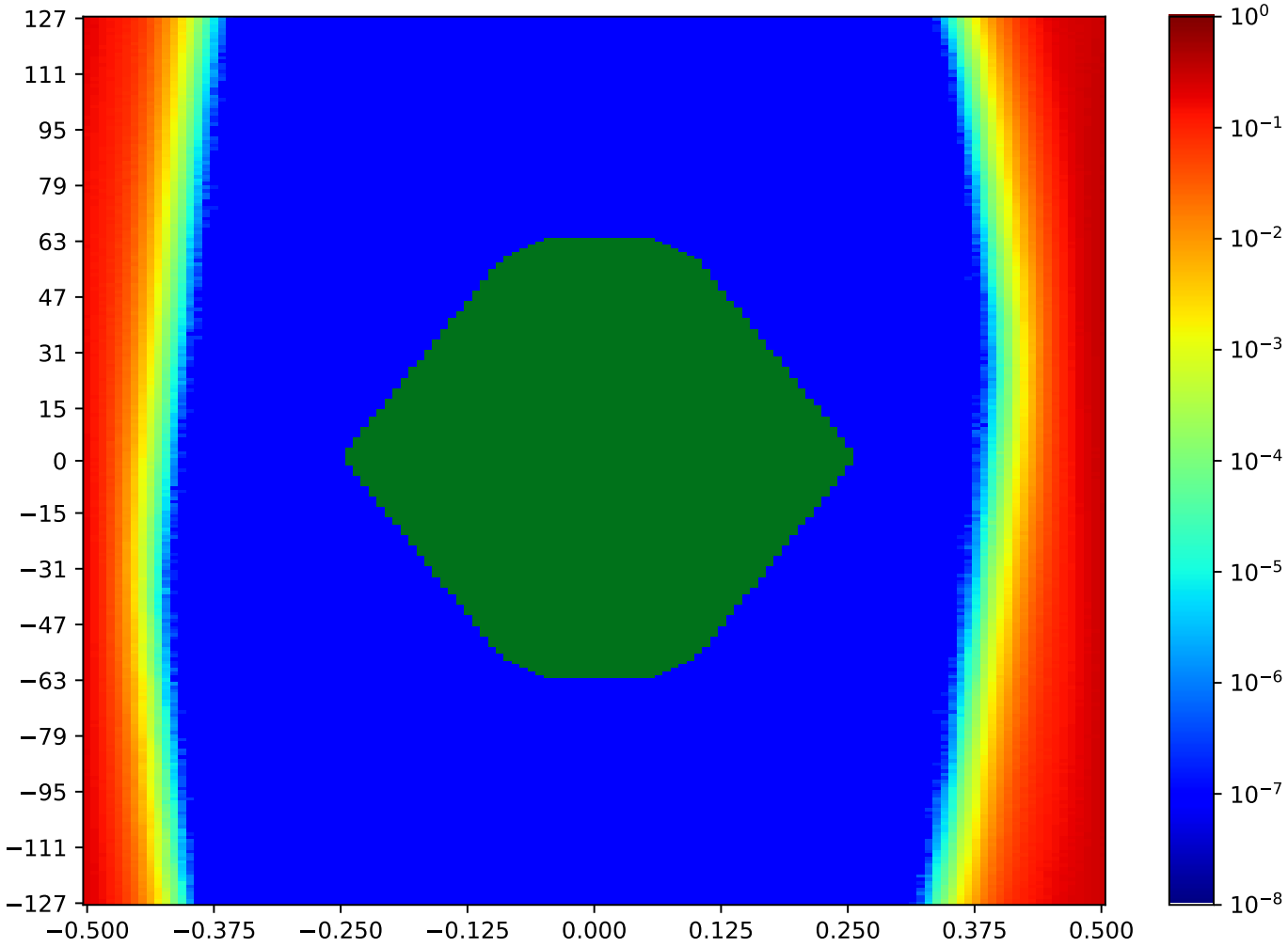


Figure 5.19: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.6 MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Table 5.18: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:42:27		2019-Nov-26 10:43:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22925	101	78.29%	234	91.76%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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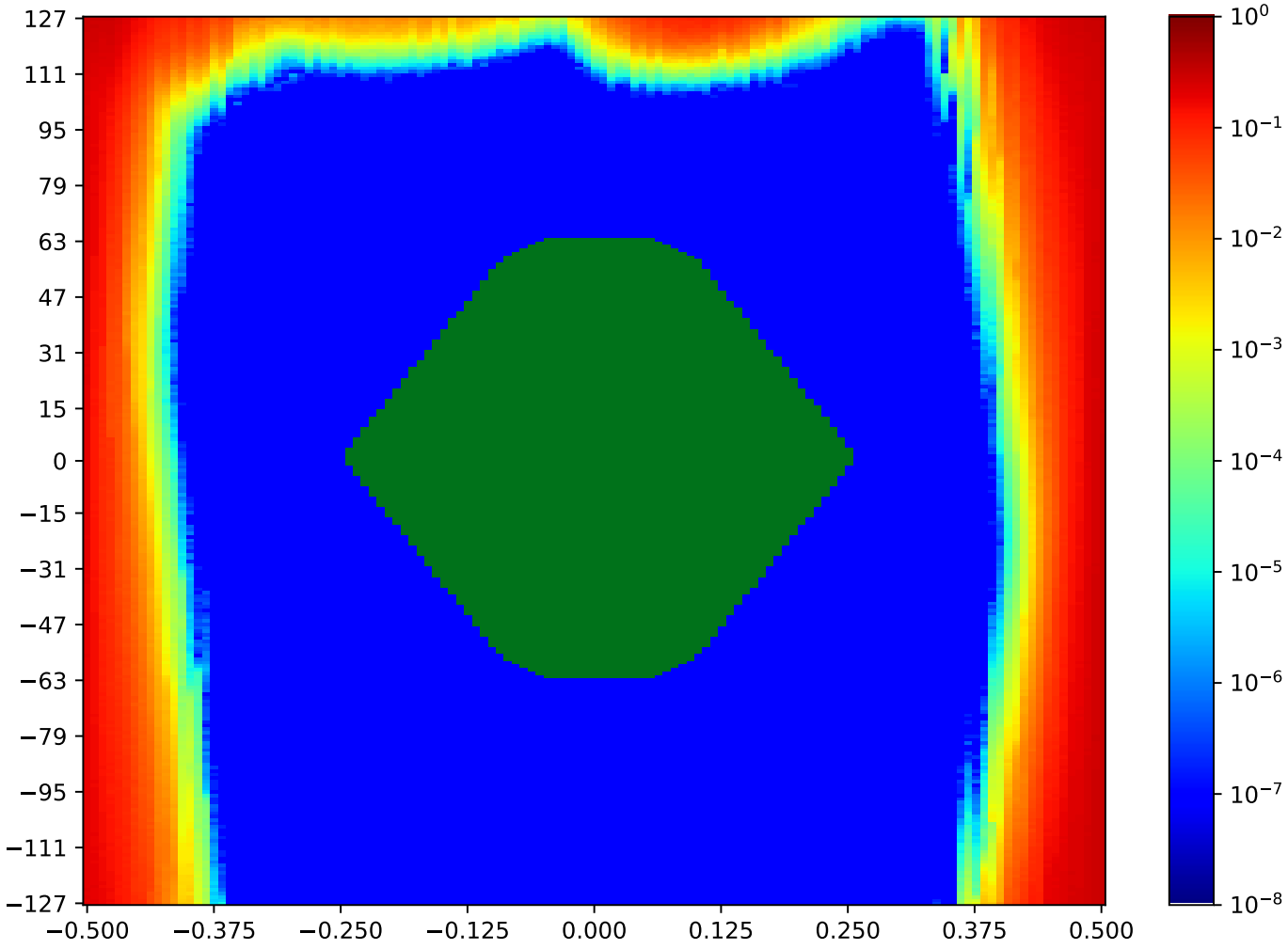


Figure 5.20: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.7 MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Table 5.19: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:53:10		2019-Nov-26 10:54:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22256	99	76.74%	235	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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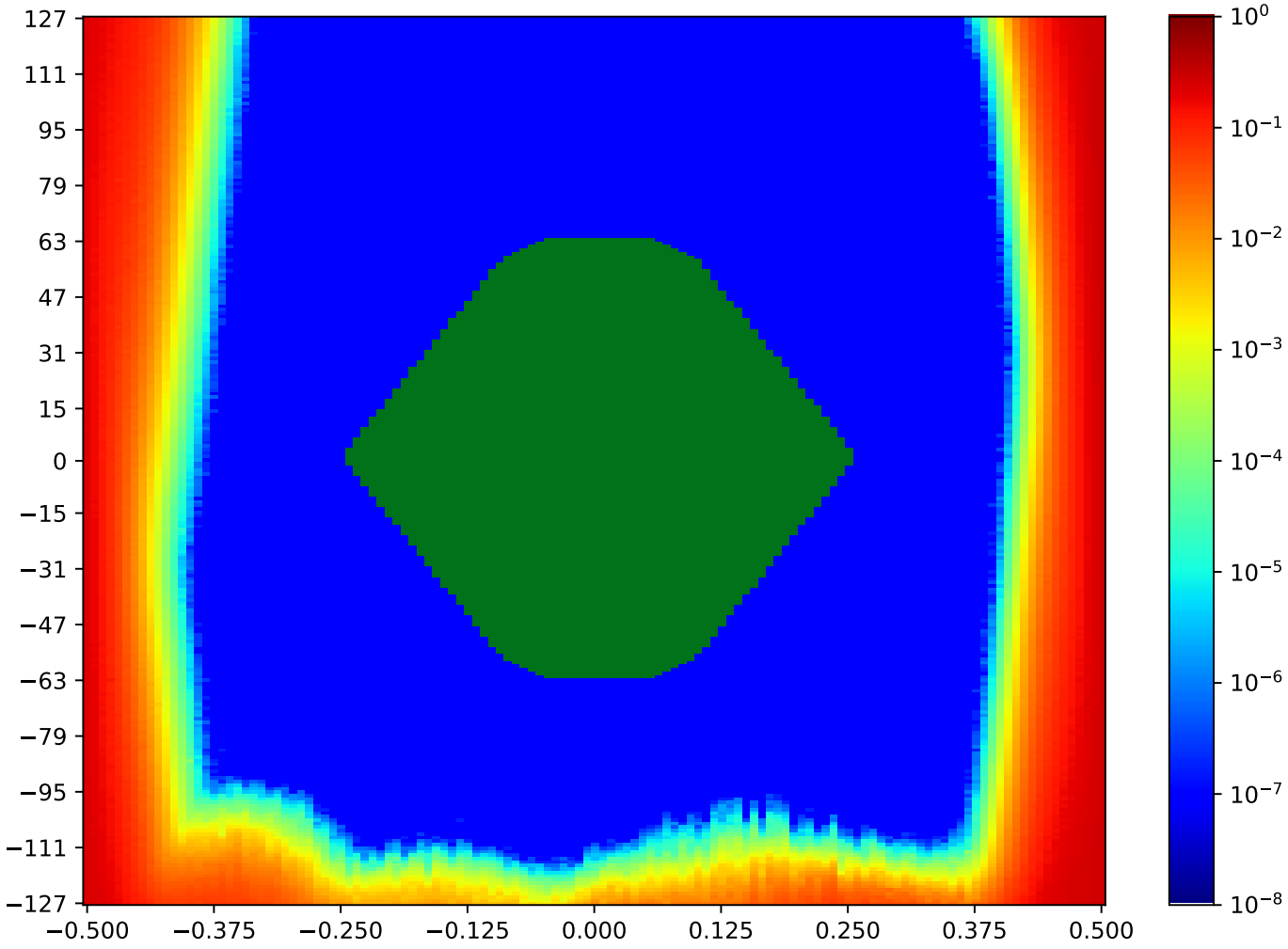


Figure 5.21: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.8 MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Table 5.20: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:45:00		2019-Nov-26 10:46:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24518	100	77.52%	246	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

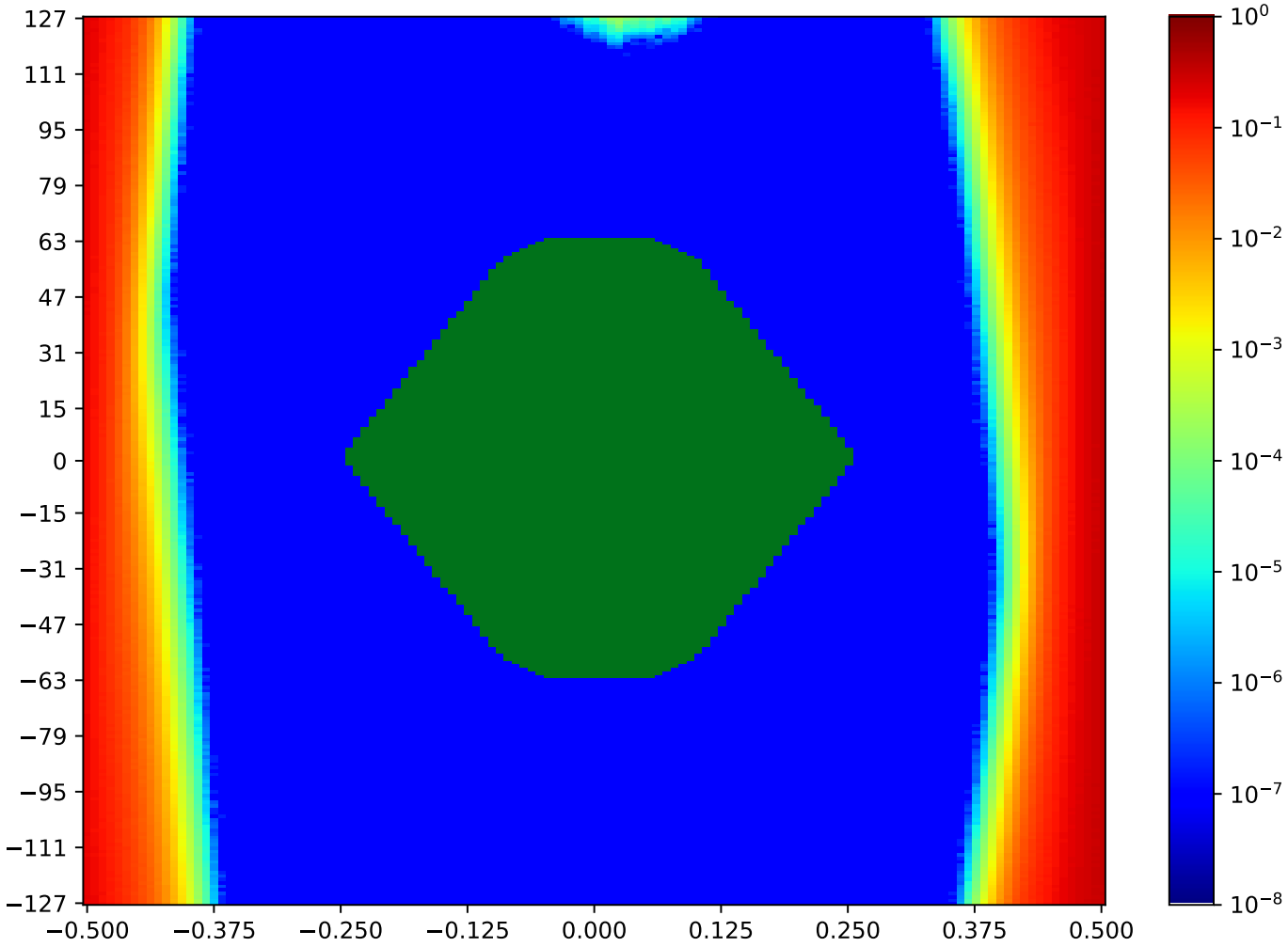


Figure 5.22: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.9 MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Table 5.21: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:52:03		2019-Nov-26 10:53:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24099	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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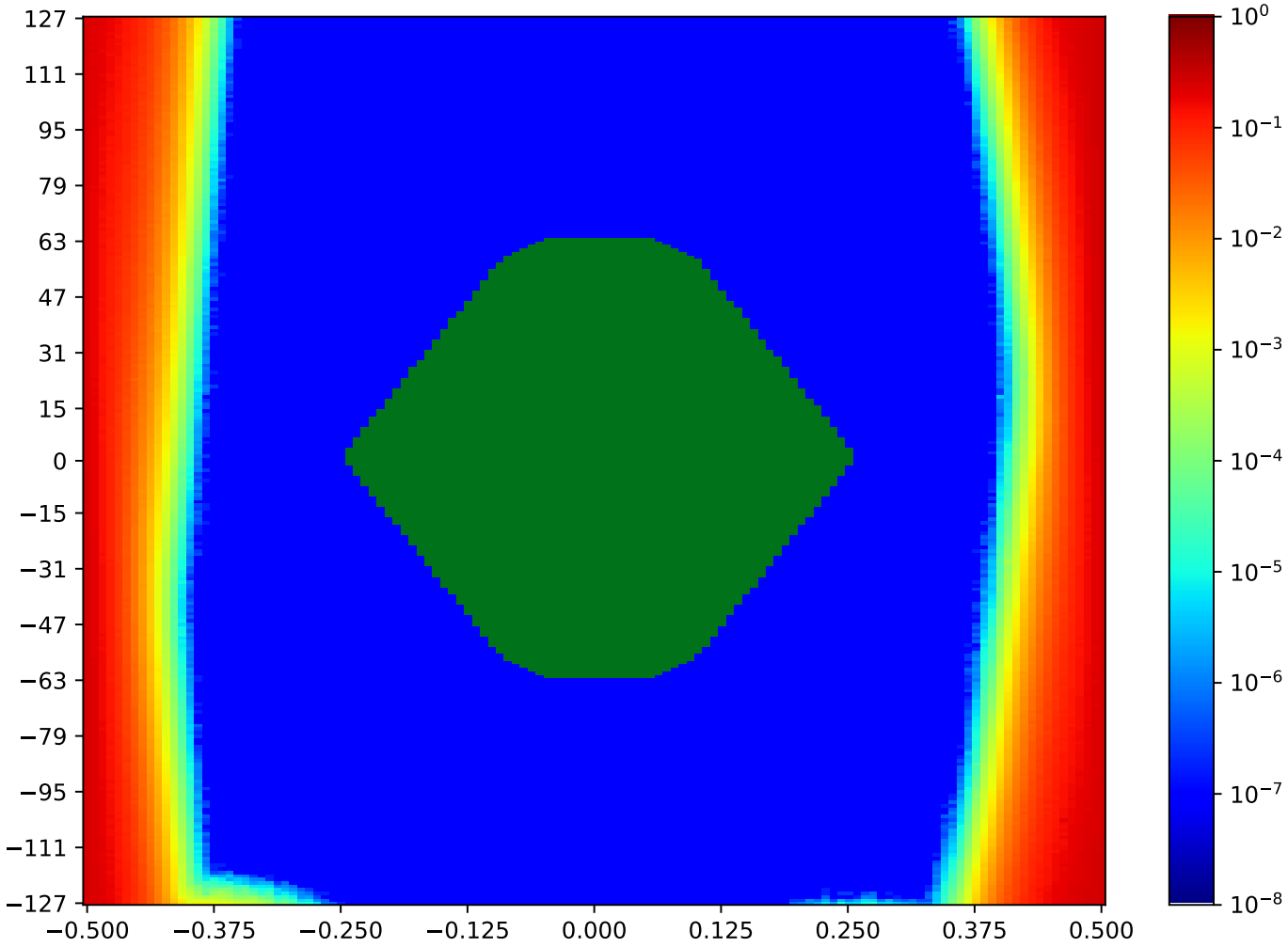


Figure 5.23: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.10 MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Table 5.22: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:46:07		2019-Nov-26 10:47:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23942	97	75.19%	251	97.65%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

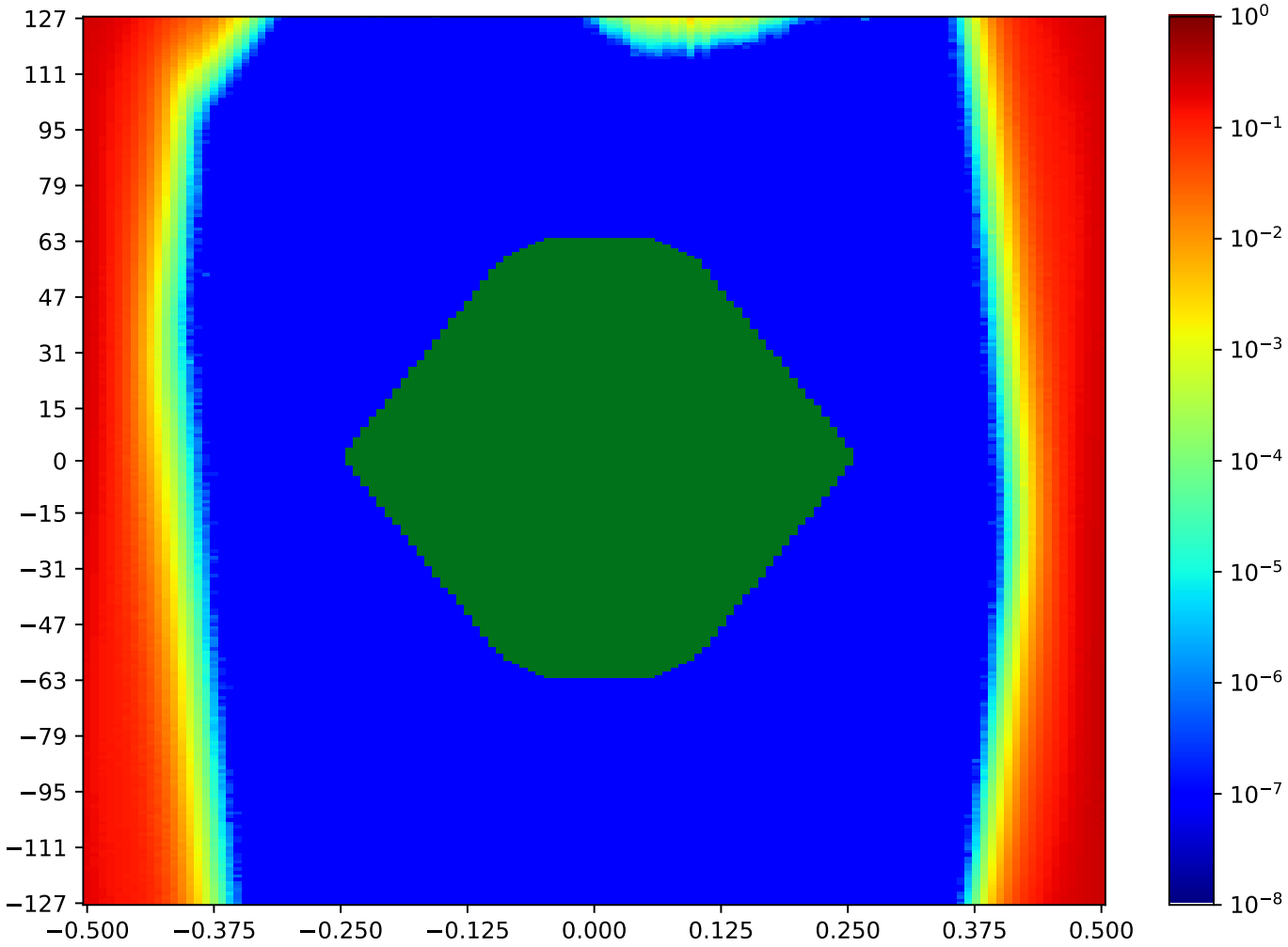


Figure 5.24: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.11 MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Table 5.23: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:49:45		2019-Nov-26 10:50:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23893	101	78.29%	251	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

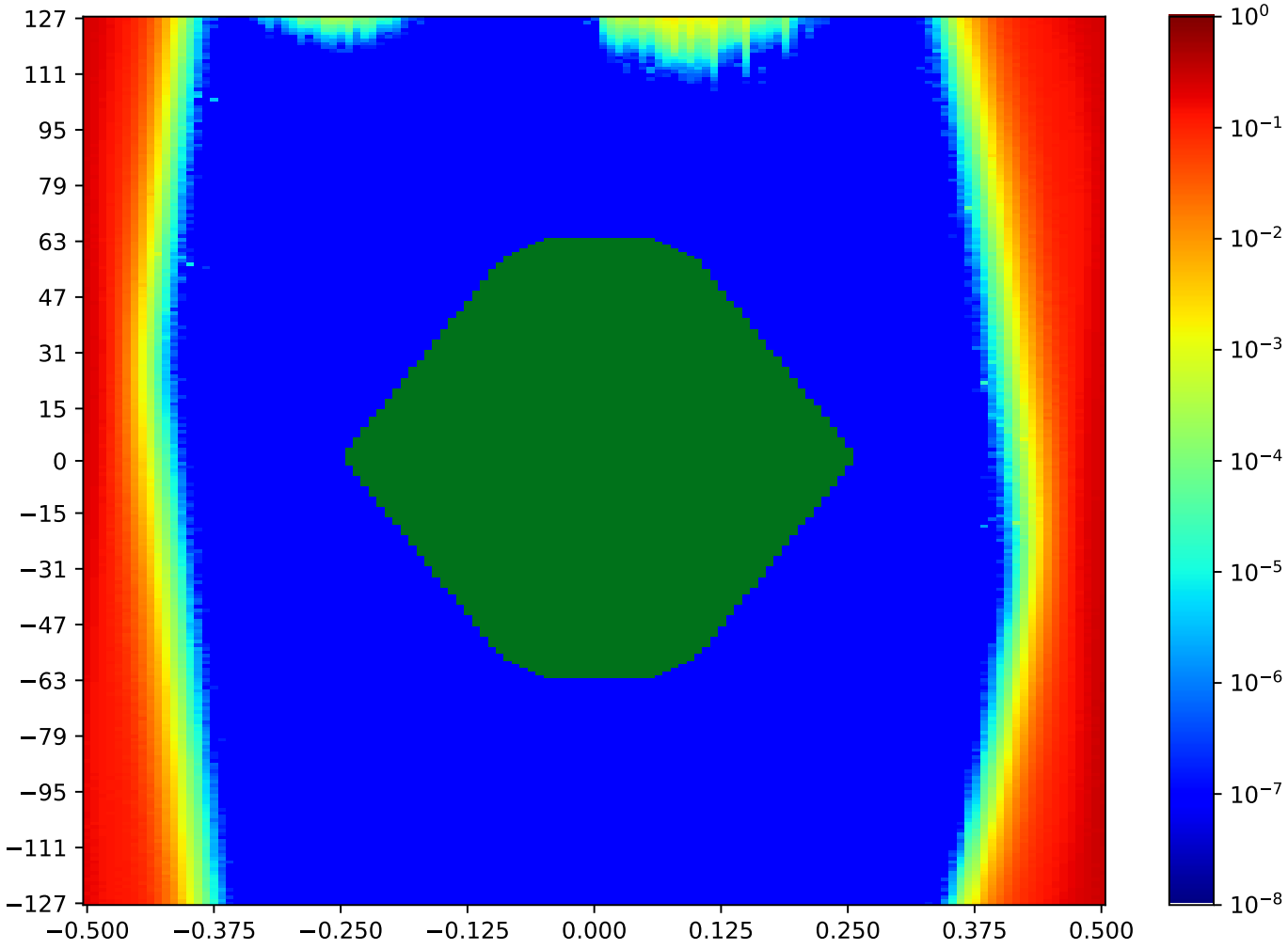


Figure 5.25: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.2.12 MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Table 5.24: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:48:22		2019-Nov-26 10:49:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24151	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

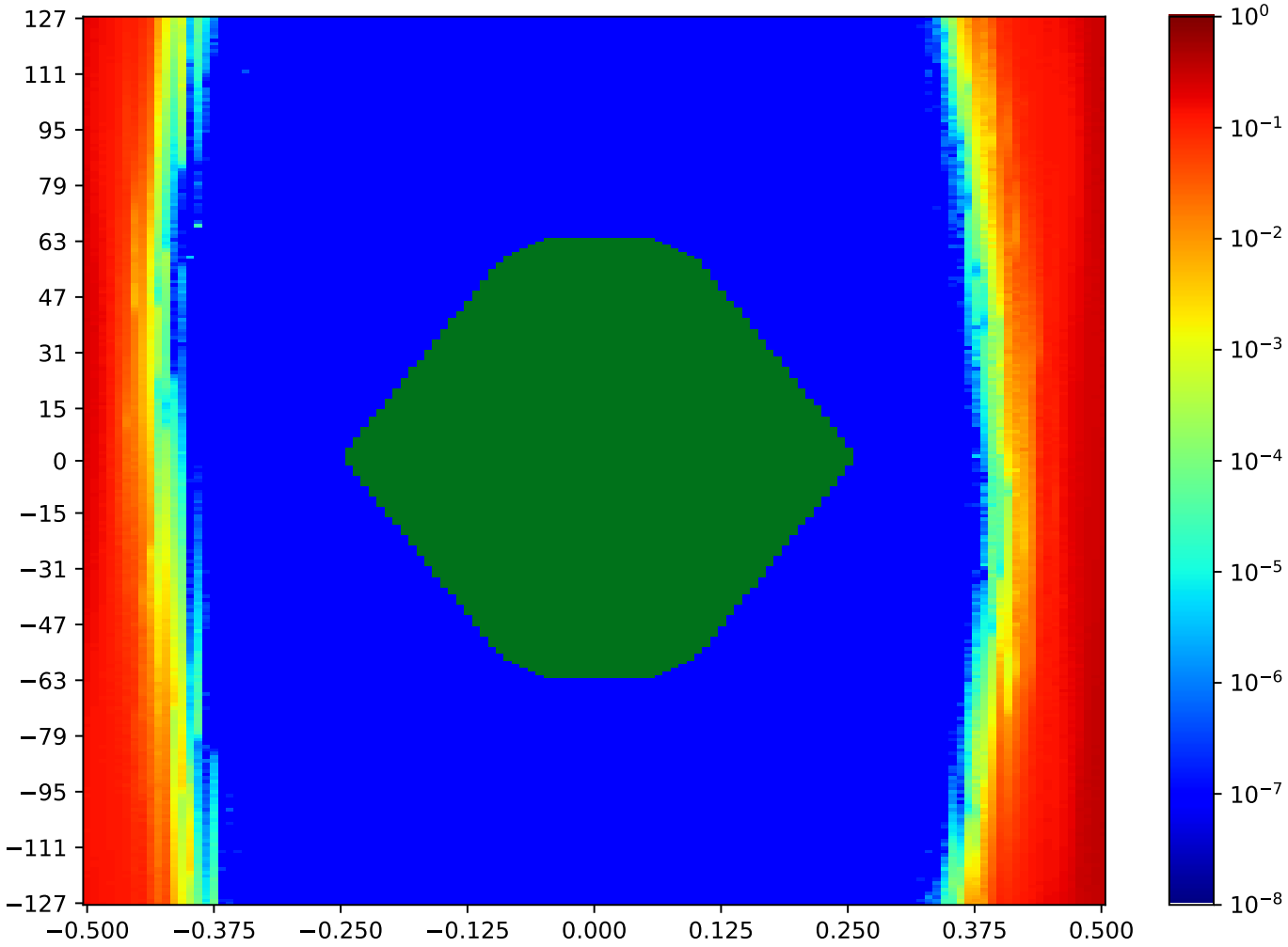


Figure 5.26: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3 MSP_C TX3 MSP_A RX6 Minipod Loopback

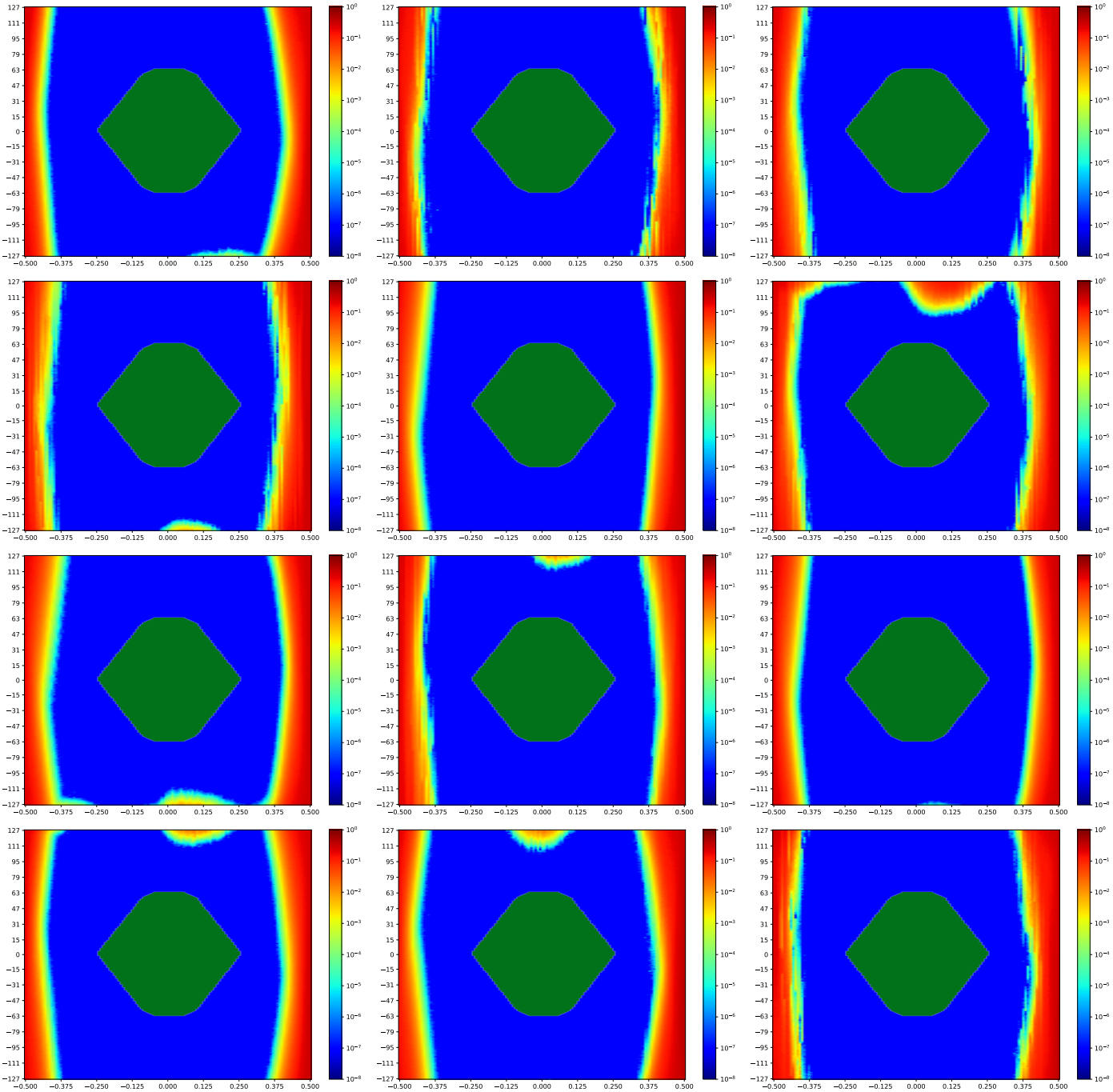


Figure 5.27: MSP_C TX3 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.40.

5.3.1 MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Table 5.25: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:57:49		2019-Nov-26 10:58:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24509	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

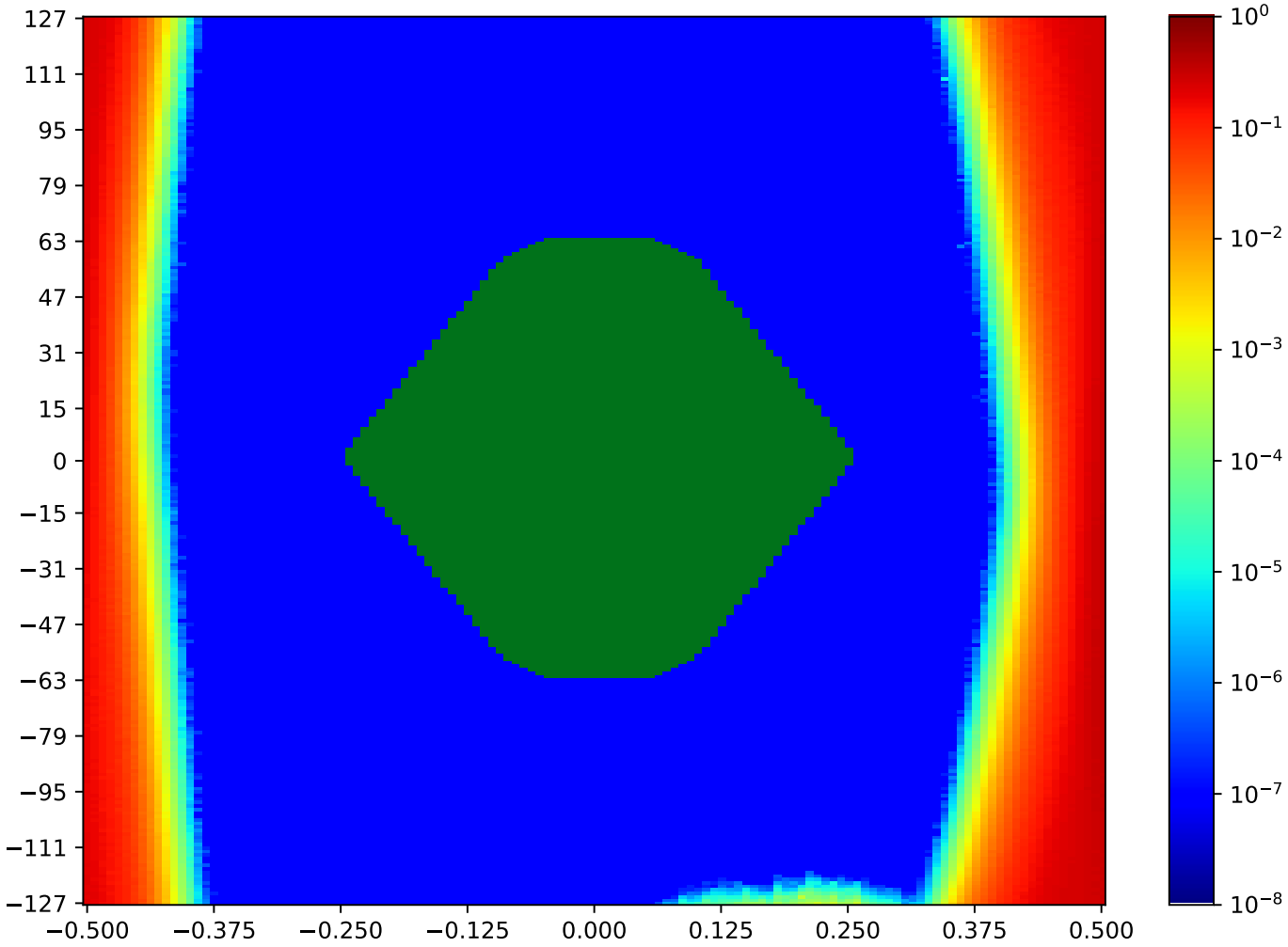


Figure 5.28: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.2 MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Table 5.26: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:00:04		2019-Nov-26 11:01:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24780	102	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

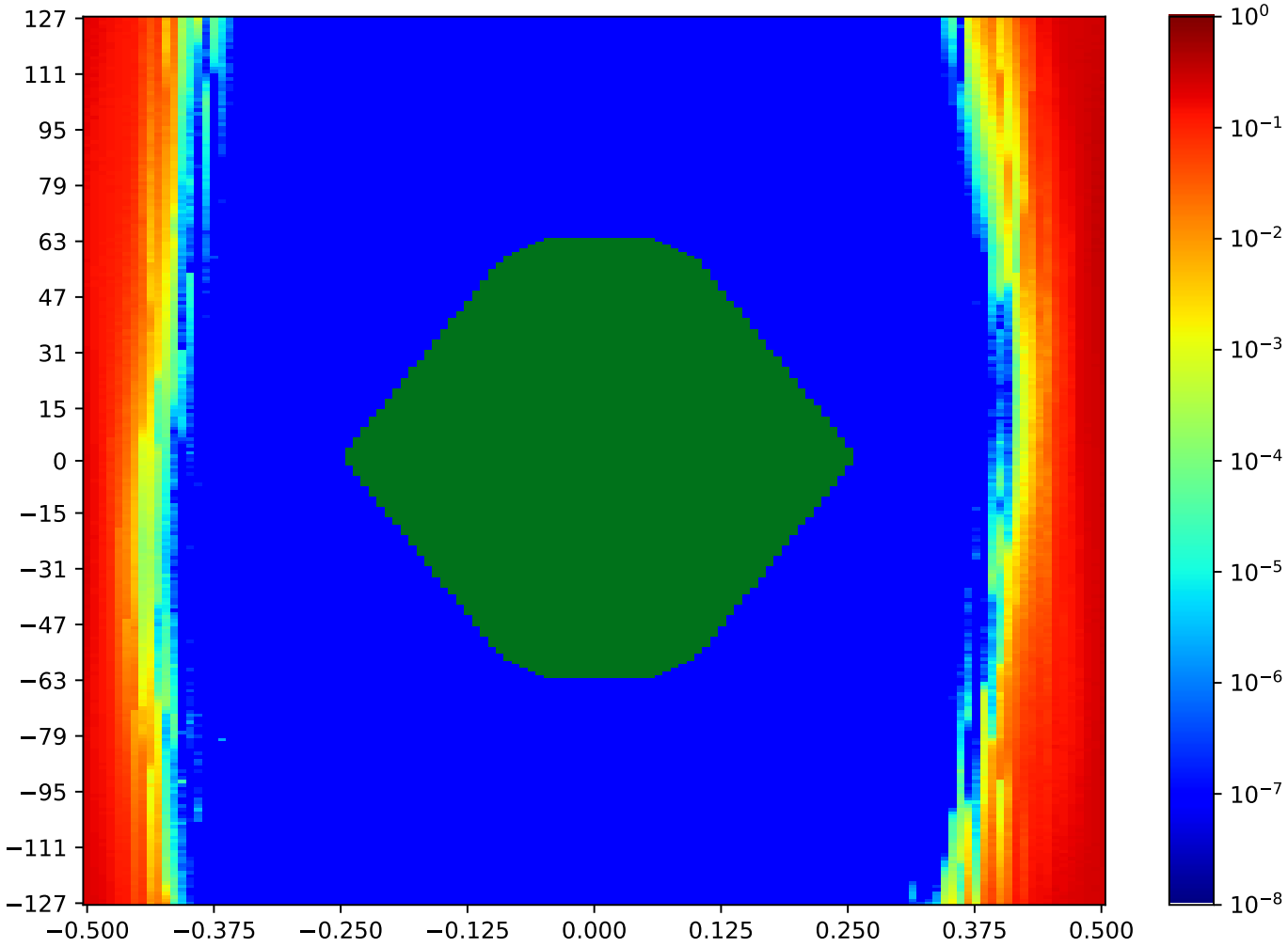


Figure 5.29: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.3 MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Table 5.27: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:01:12		2019-Nov-26 11:02:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24017	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

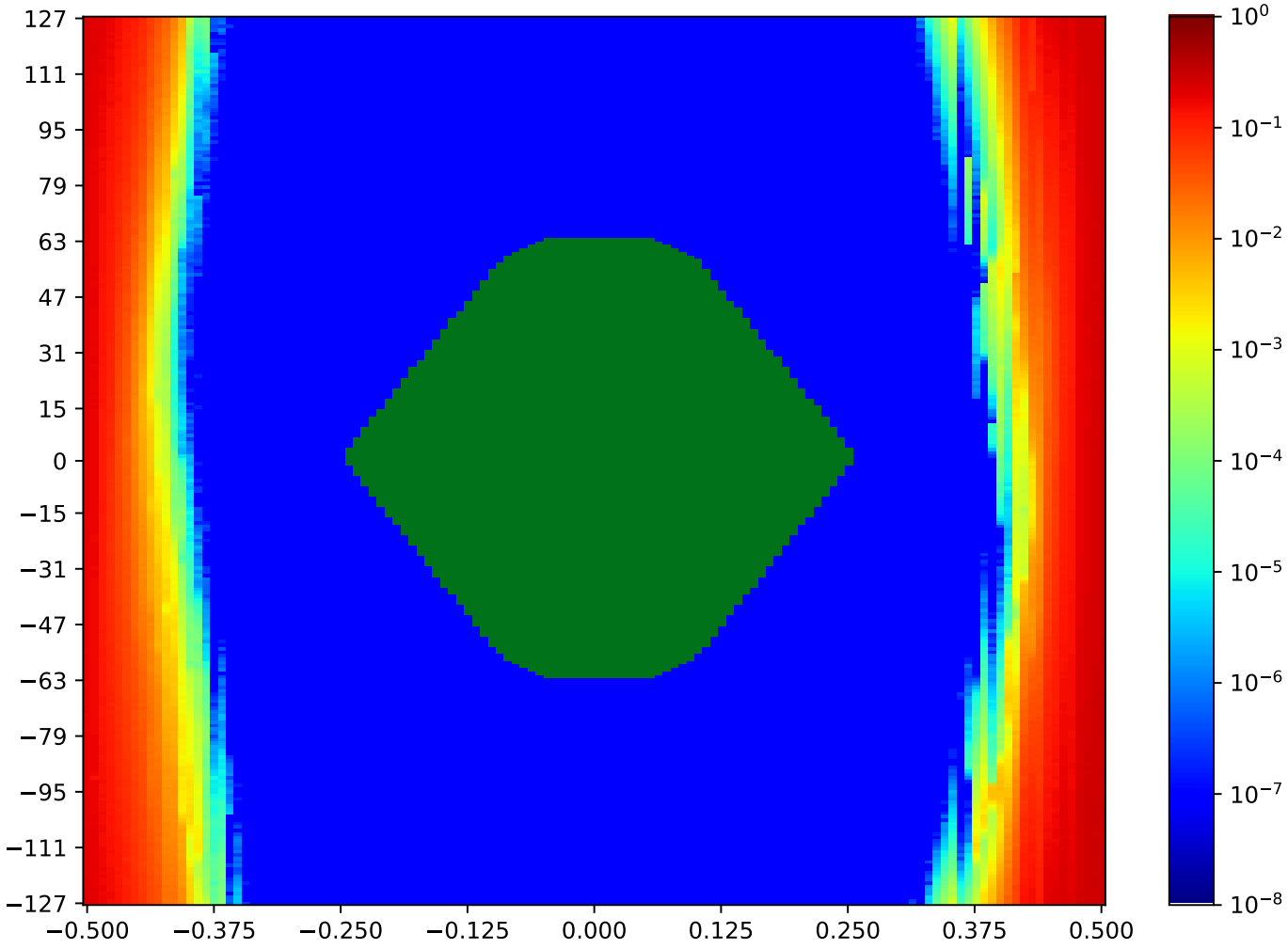


Figure 5.30: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.4 MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Table 5.28: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:55:34		2019-Nov-26 10:56:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23565	97	75.19%	246	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

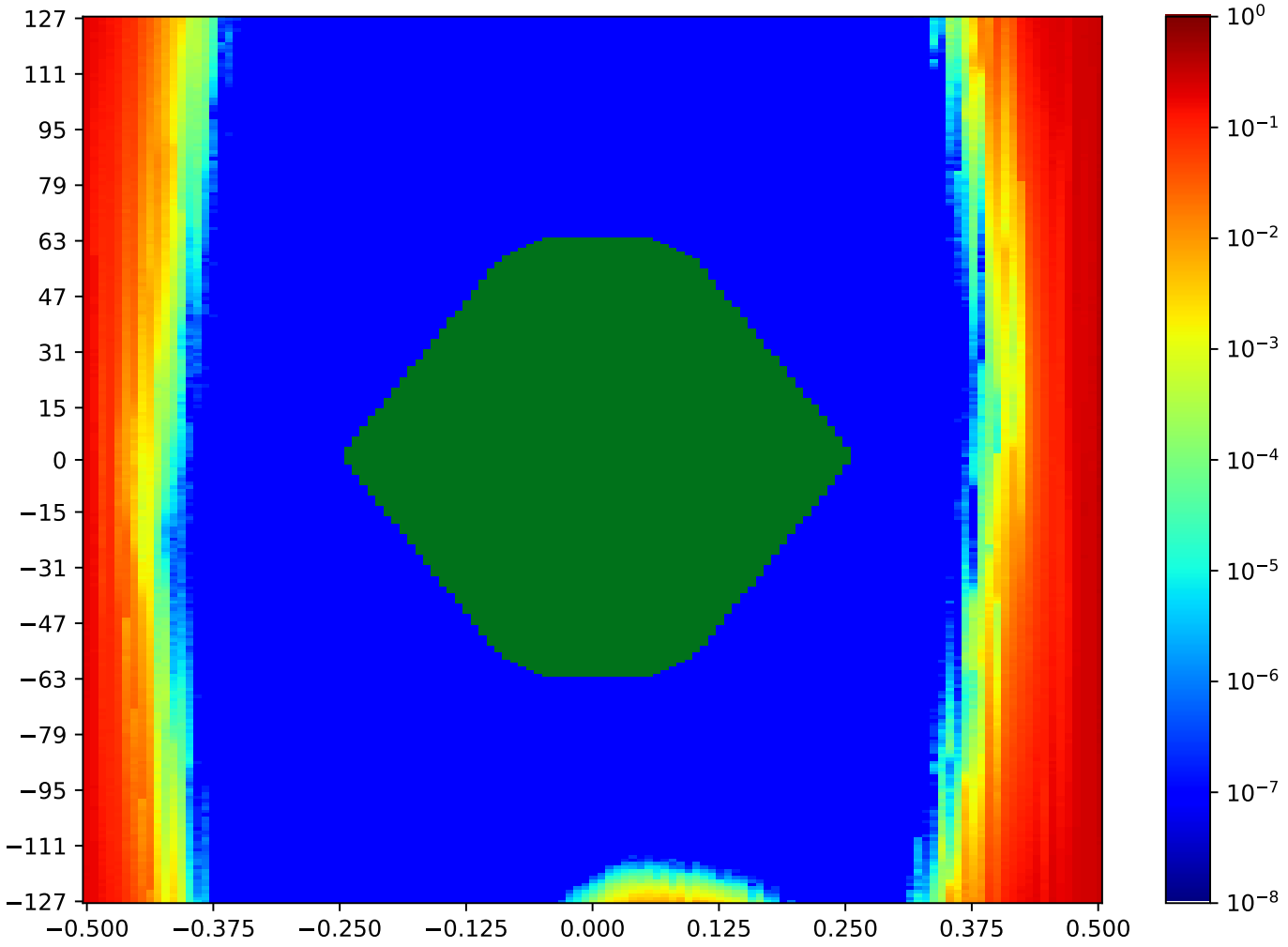


Figure 5.31: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.5 MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Table 5.29: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:04:34		2019-Nov-26 11:05:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24474	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

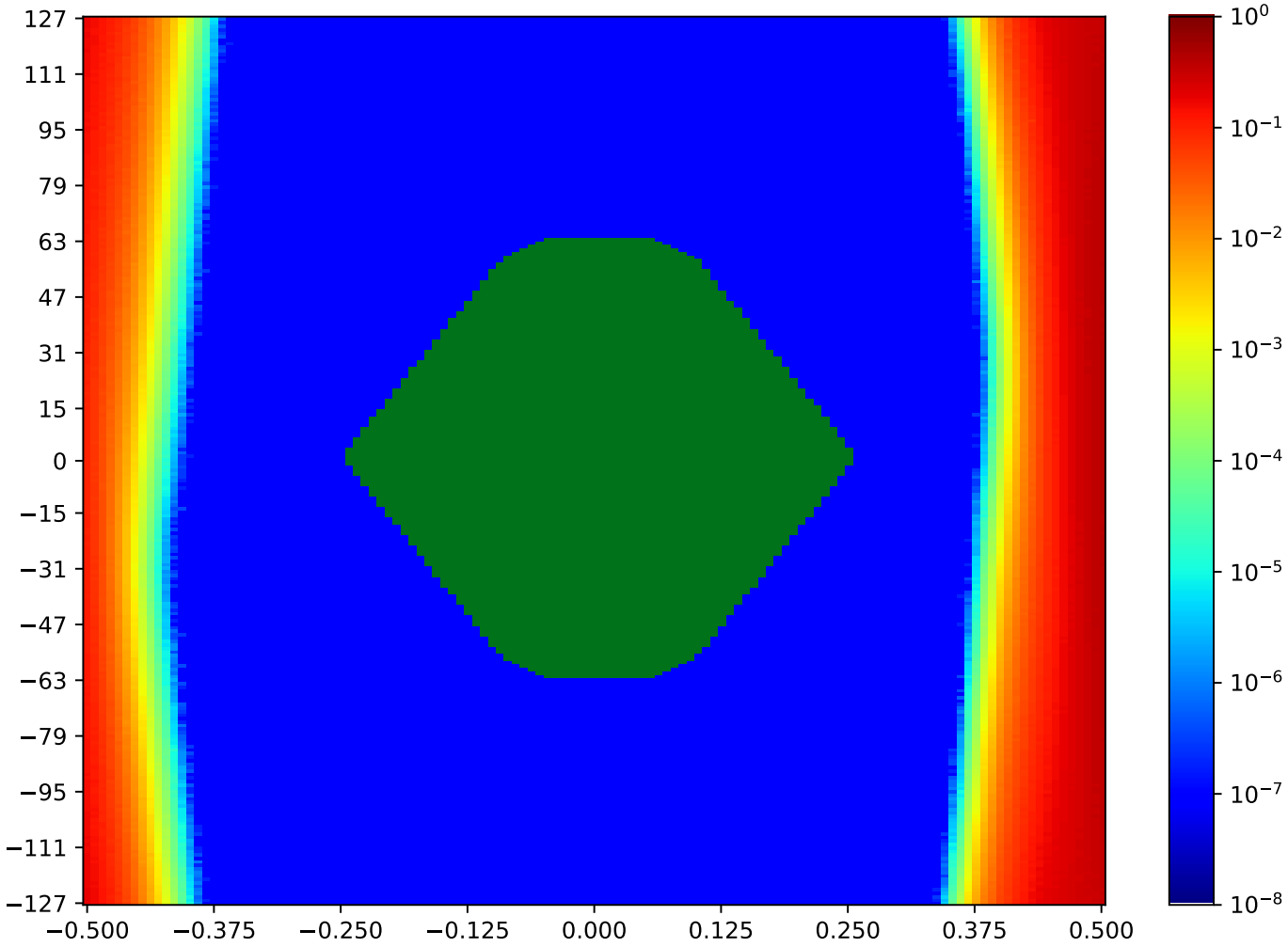


Figure 5.32: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.6 MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Table 5.30: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:54:18		2019-Nov-26 10:55:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22680	99	76.74%	223	87.45%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

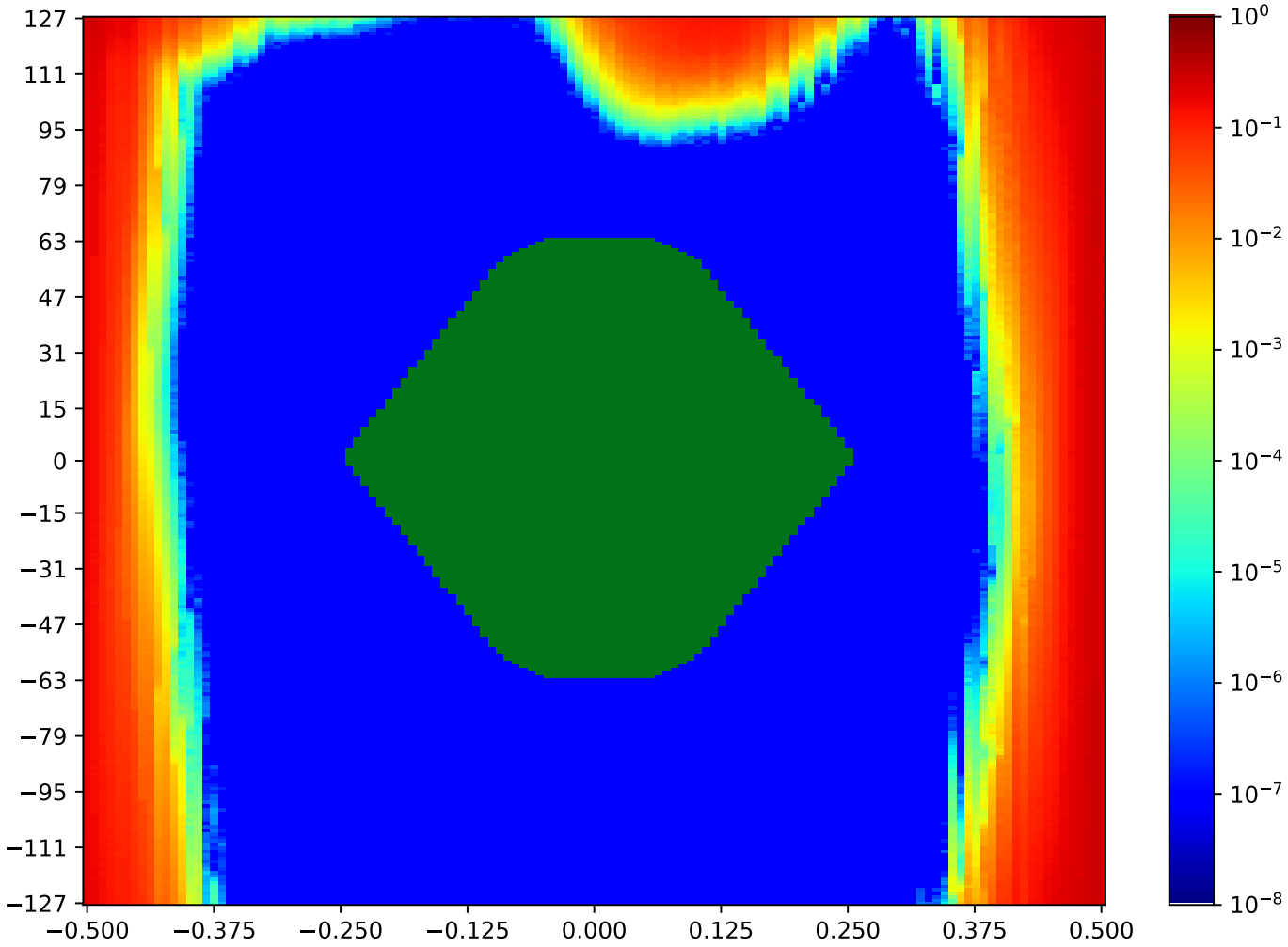


Figure 5.33: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.7 MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Table 5.31: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:06:57		2019-Nov-26 11:08:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23471	99	76.74%	238	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

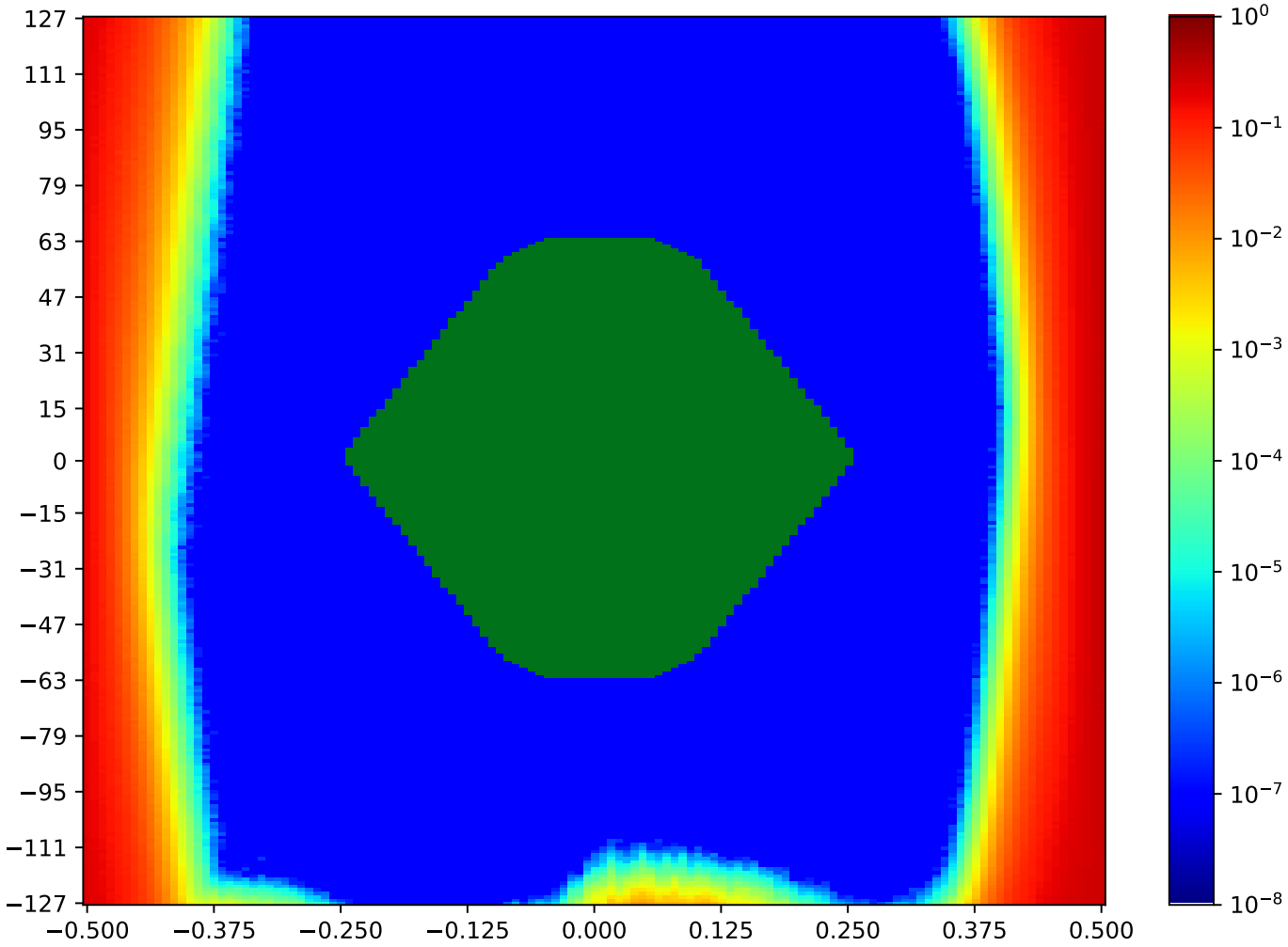


Figure 5.34: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.8 MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Table 5.32: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:56:42		2019-Nov-26 10:57:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24129	99	76.74%	243	94.12%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

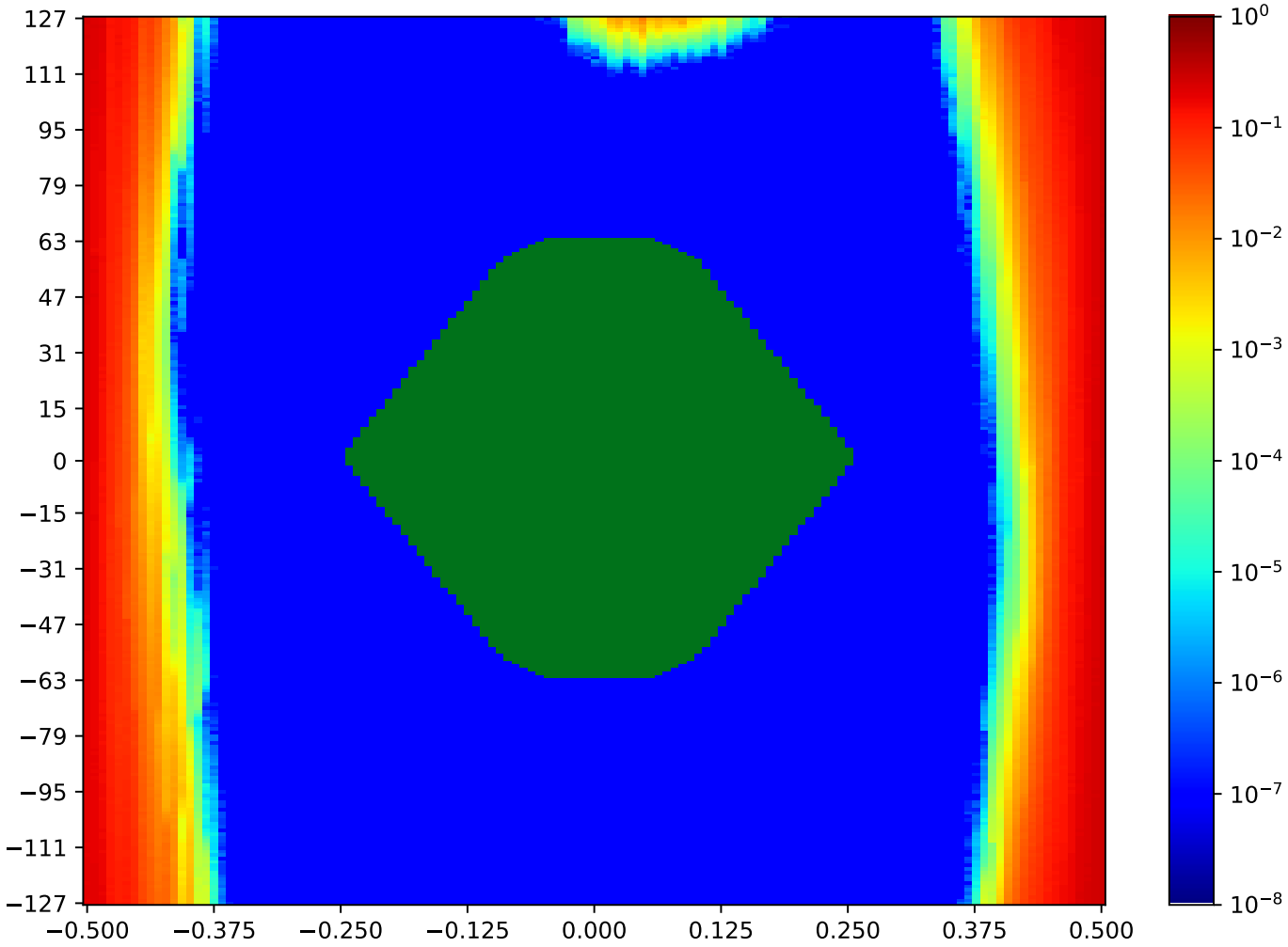


Figure 5.35: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.9 MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Table 5.33: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:05:41		2019-Nov-26 11:06:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24584	100	77.52%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

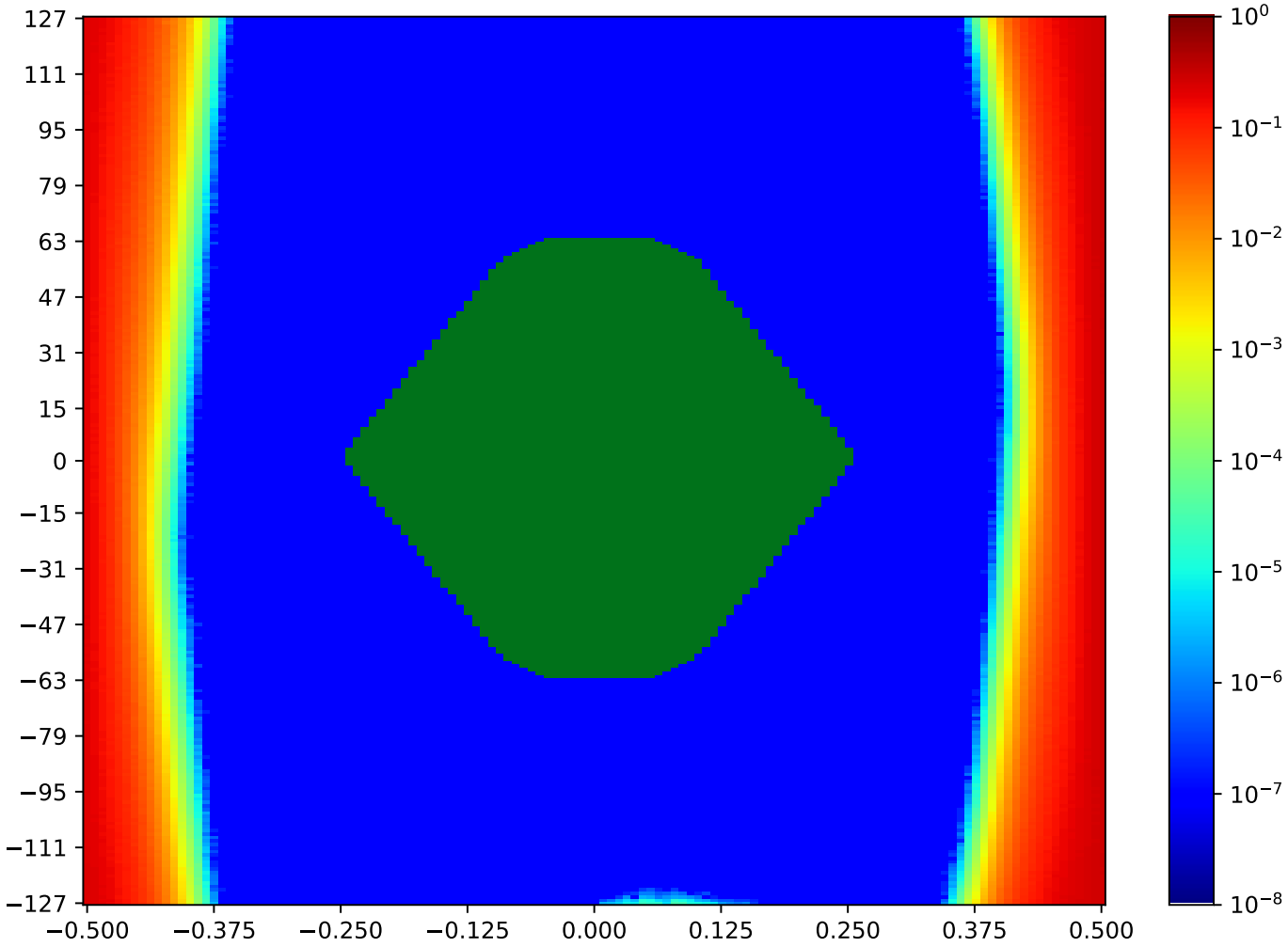


Figure 5.36: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.10 MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Table 5.34: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 10:58:57		2019-Nov-26 11:00:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24108	100	77.52%	242	94.51%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

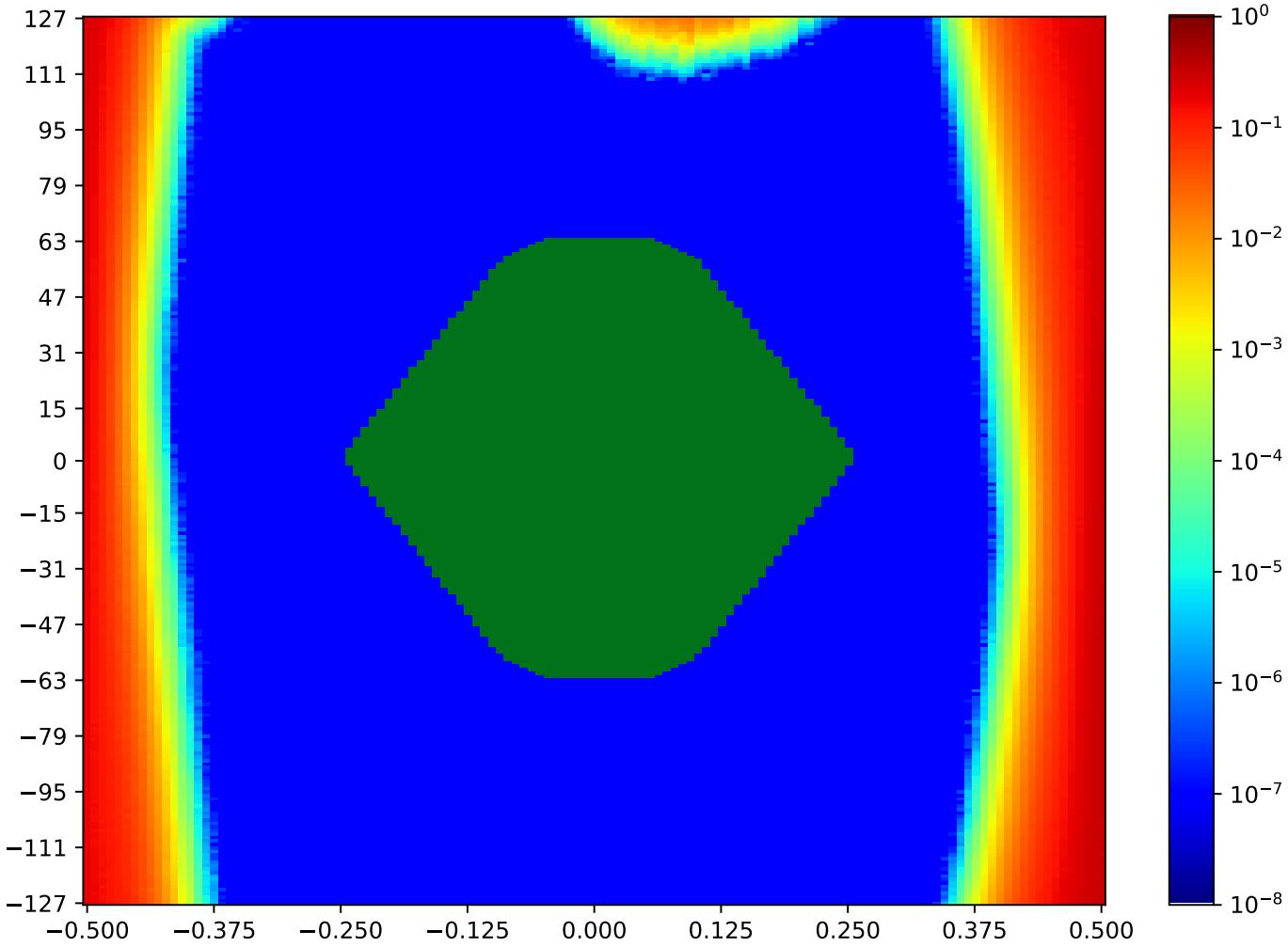


Figure 5.37: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.11 MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Table 5.35: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:03:26		2019-Nov-26 11:04:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23719	100	77.52%	229	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

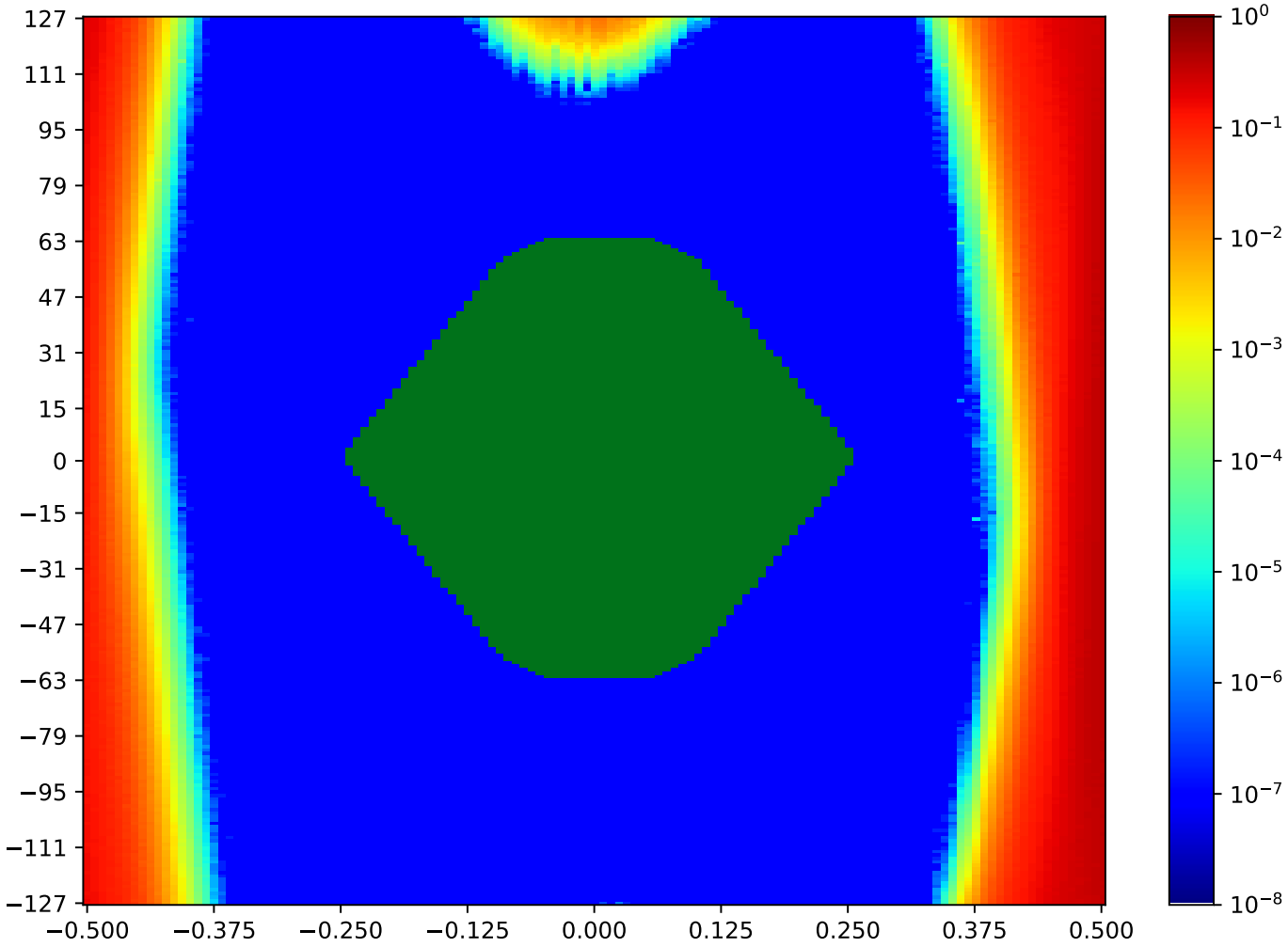


Figure 5.38: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.3.12 MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Table 5.36: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:02:19		2019-Nov-26 11:03:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24474	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

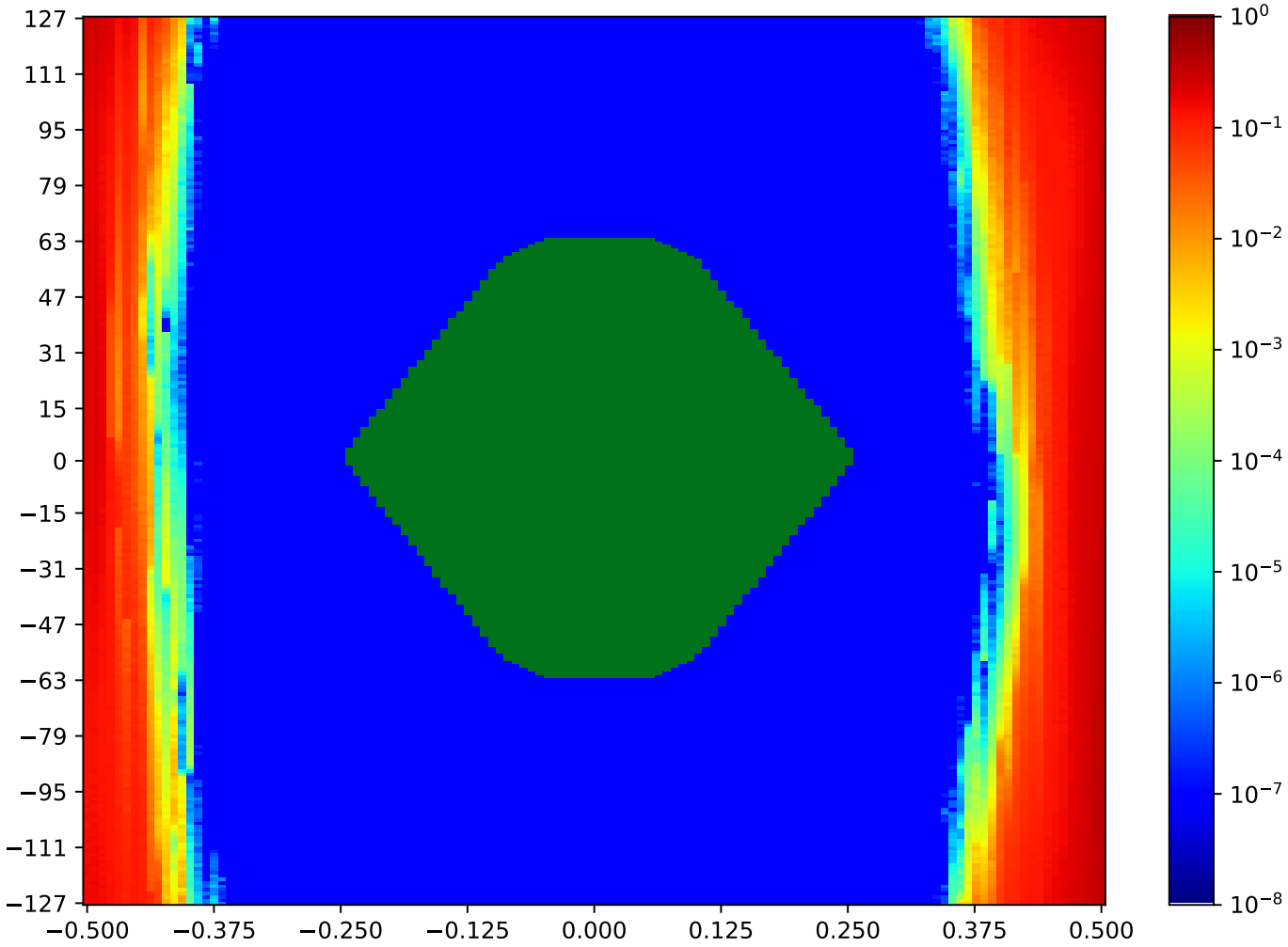


Figure 5.39: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4 MSP_C TX4 MSP_A RX7 Minipod Loopback

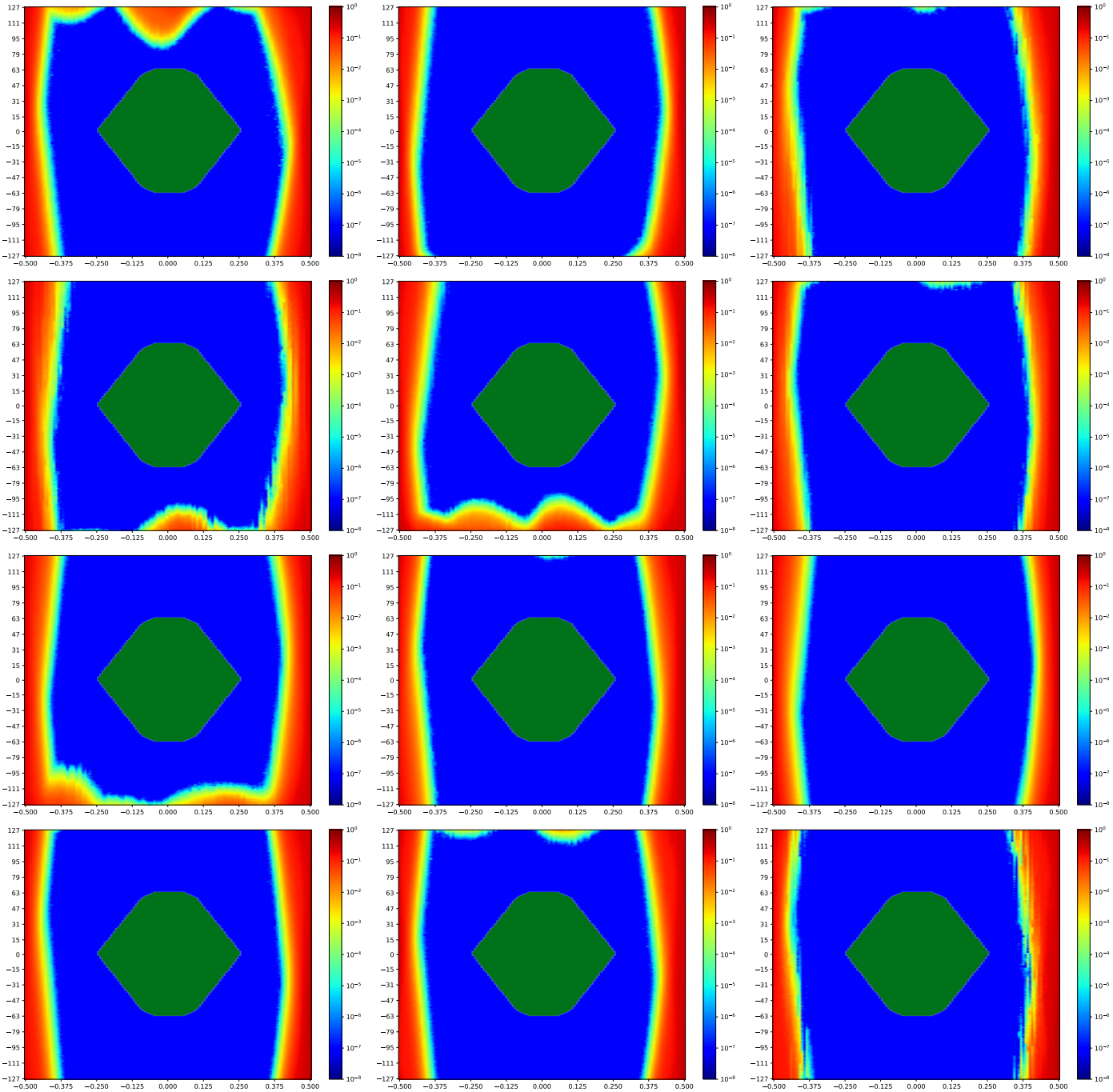


Figure 5.40: MSP_C TX4 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.53.

5.4.1 MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Table 5.37: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:11:46		2019-Nov-26 11:12:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22464	102	79.07%	208	81.57%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

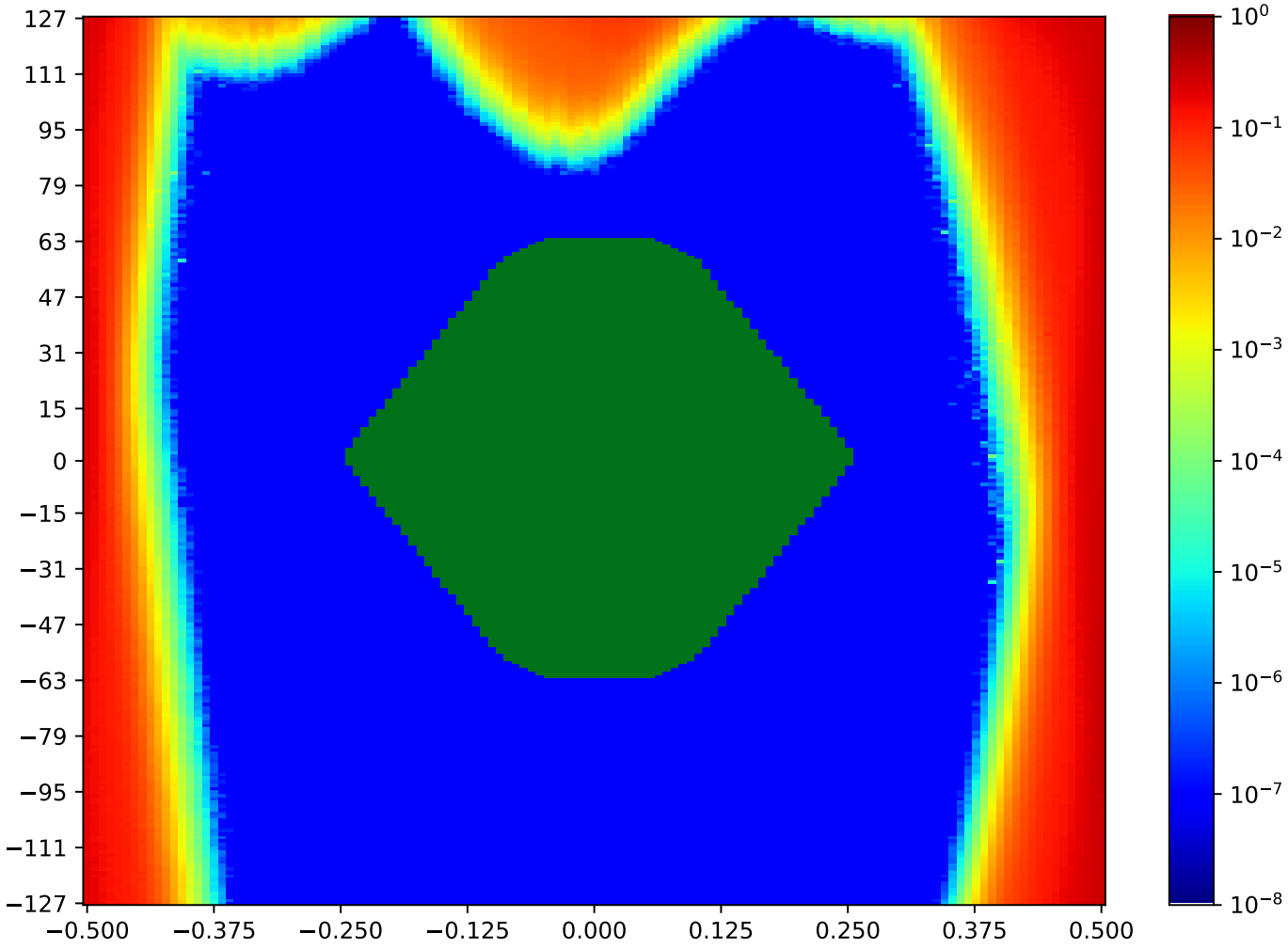


Figure 5.41: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.2 MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Table 5.38: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:09:11		2019-Nov-26 11:10:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25050	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

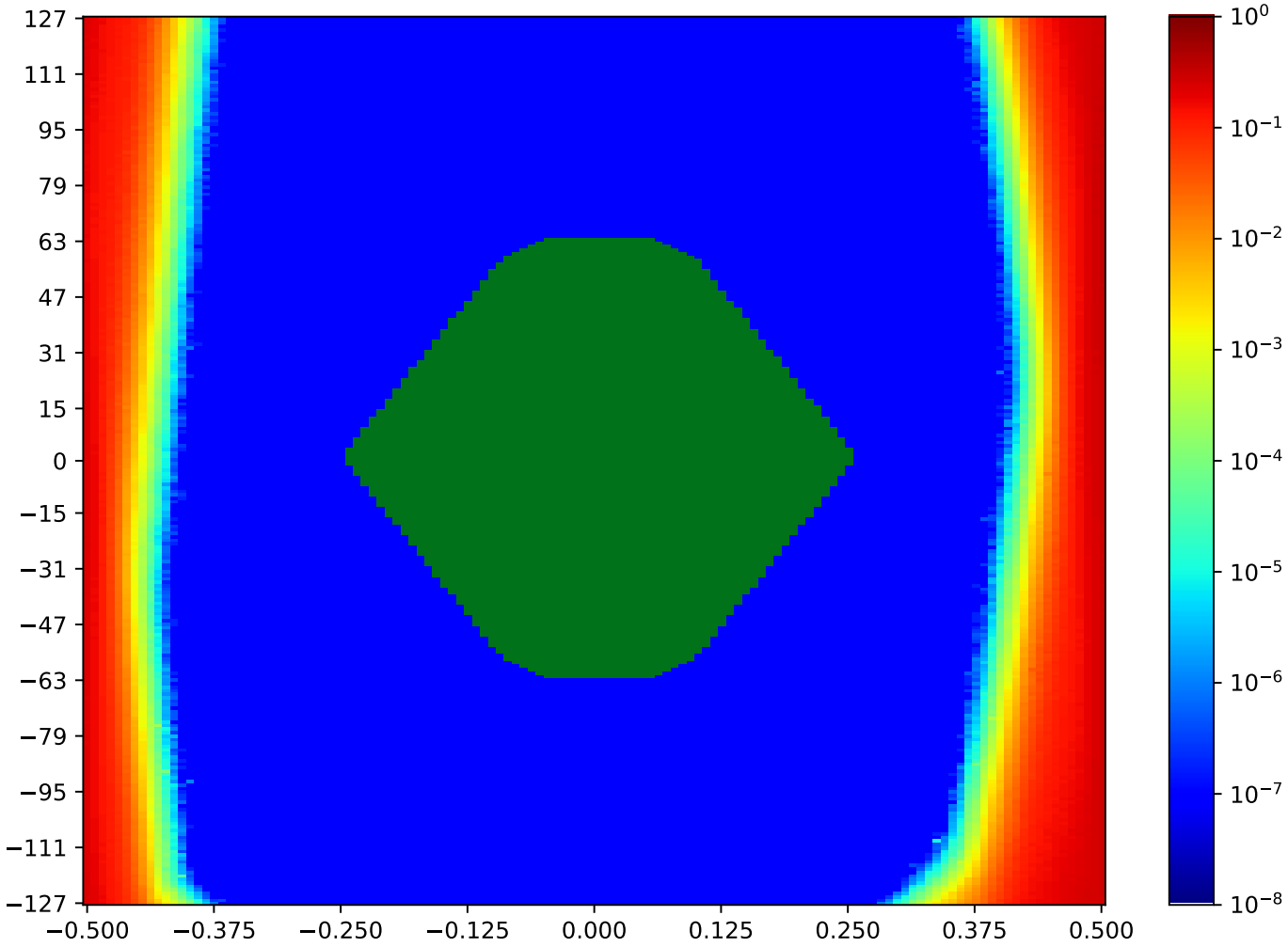


Figure 5.42: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.3 MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Table 5.39: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:15:08		2019-Nov-26 11:16:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23839	96	74.42%	247	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

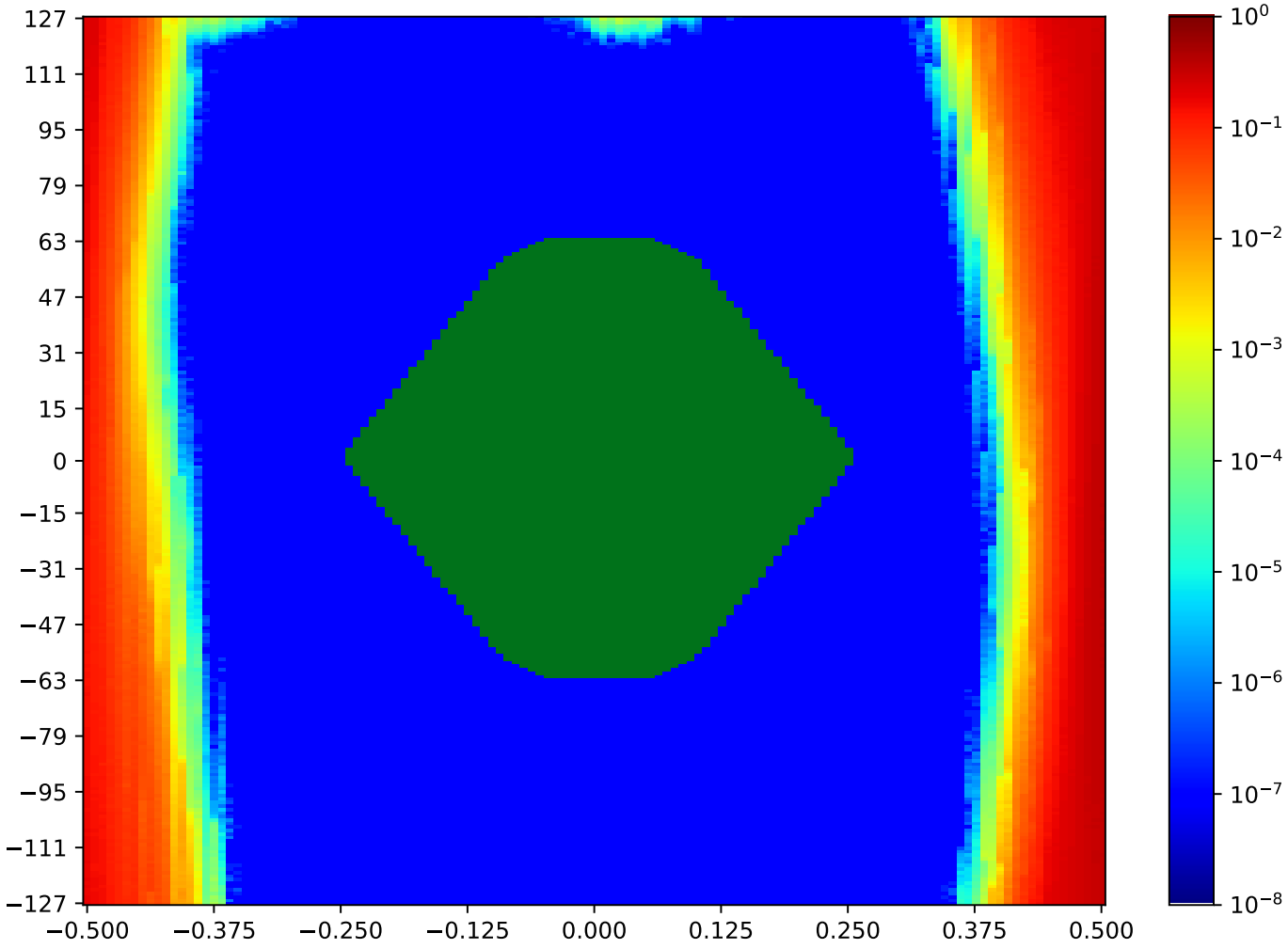


Figure 5.43: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.4 MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Table 5.40: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:08:04		2019-Nov-26 11:09:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22809	97	75.19%	227	89.02%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

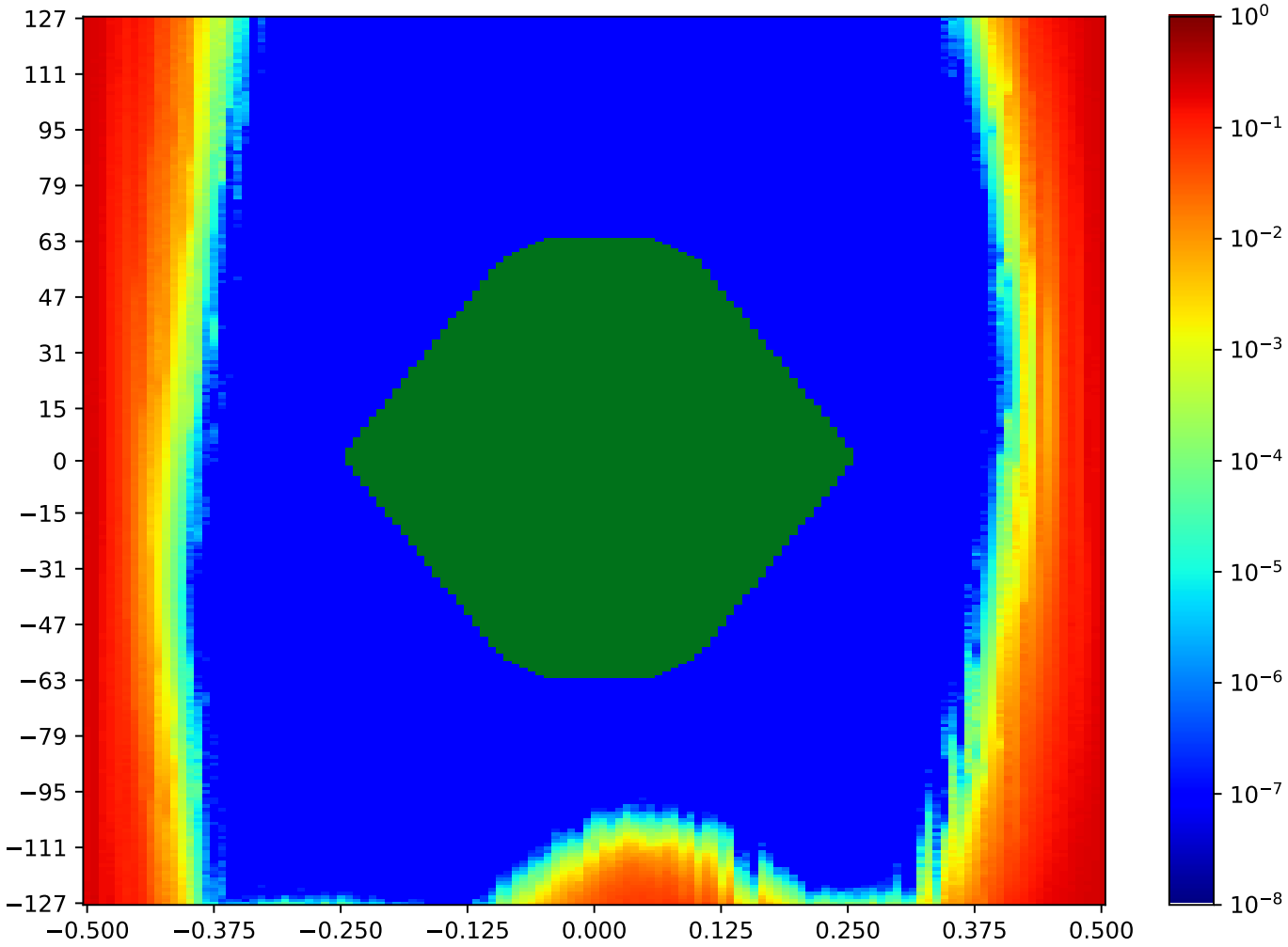


Figure 5.44: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.5 MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Table 5.41: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:18:57		2019-Nov-26 11:20:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21633	98	75.97%	220	86.27%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

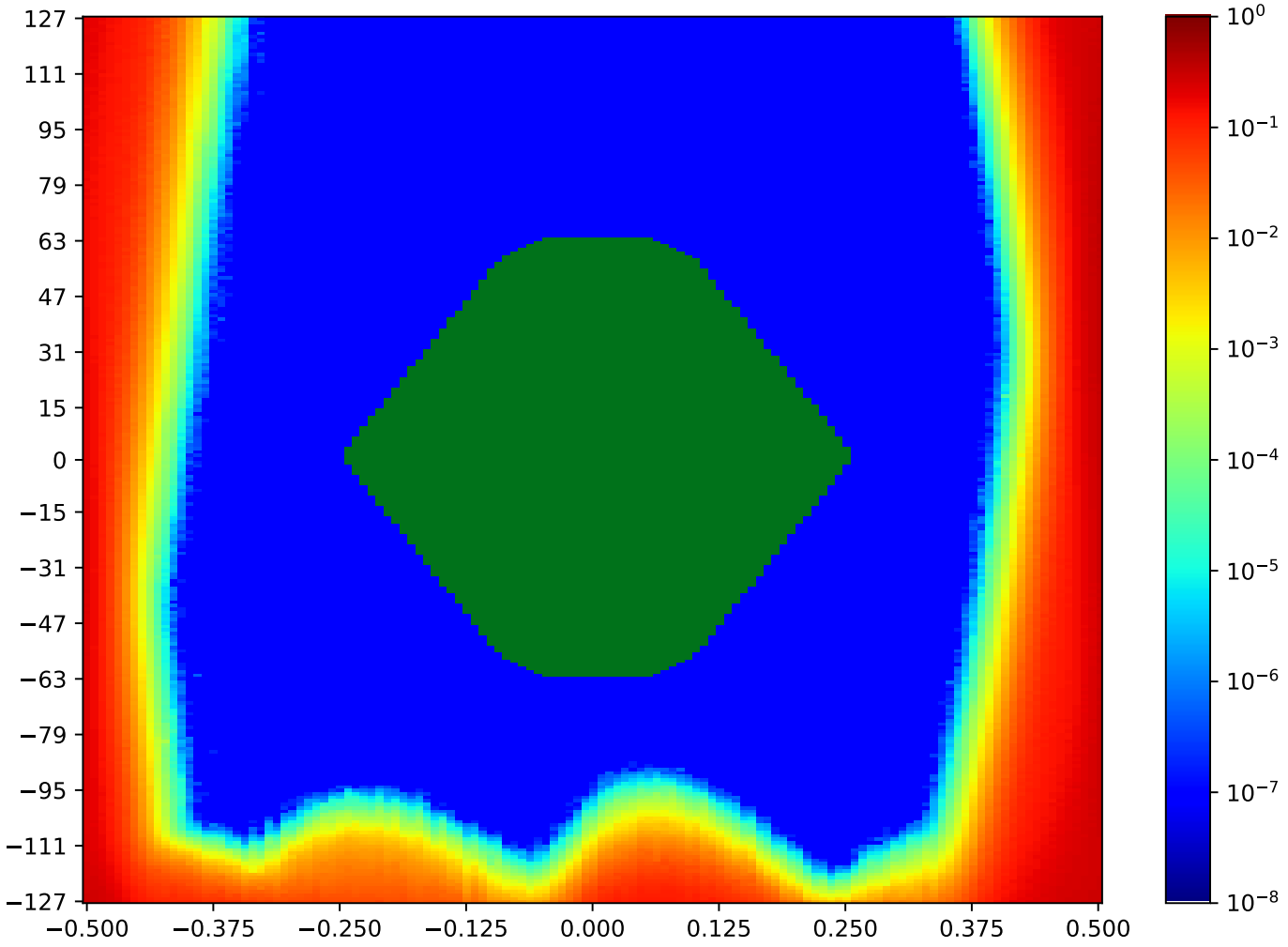


Figure 5.45: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.6 MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Table 5.42: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:10:38		2019-Nov-26 11:11:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24246	100	77.52%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

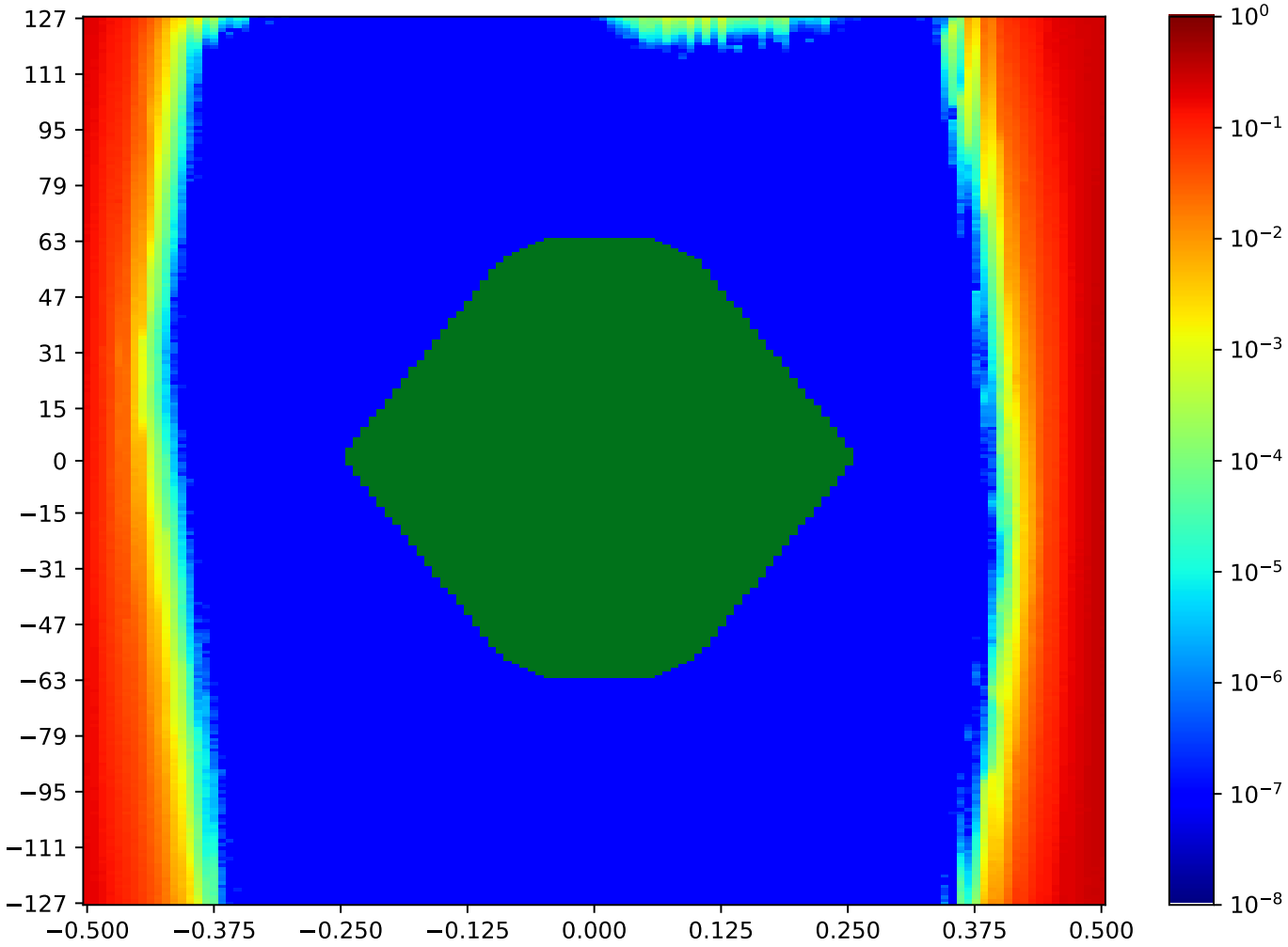


Figure 5.46: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.7 MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Table 5.43: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:21:12		2019-Nov-26 11:22:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22224	100	77.52%	244	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

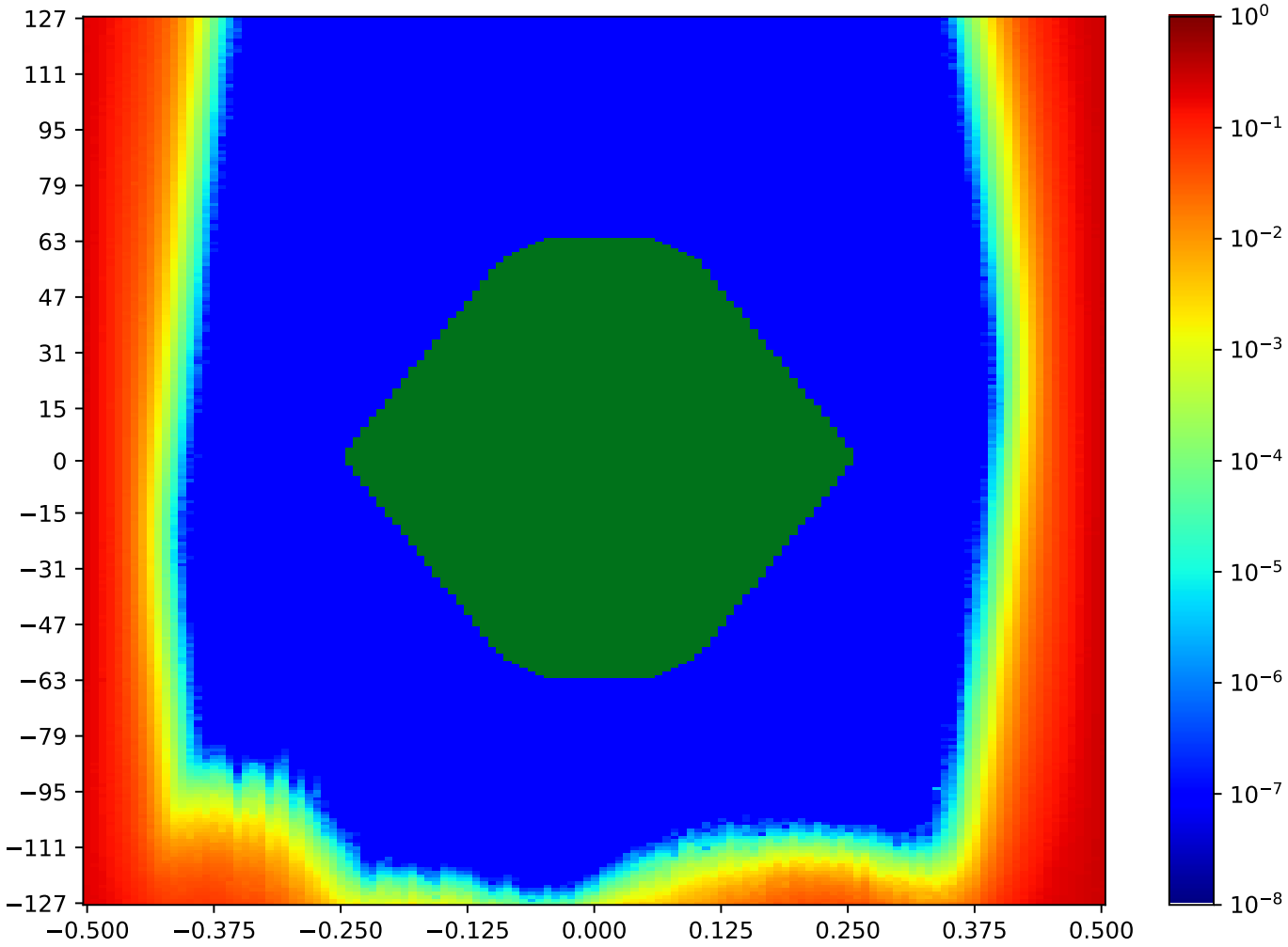


Figure 5.47: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.8 MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Table 5.44: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:12:53		2019-Nov-26 11:14:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24239	99	76.74%	249	97.65%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

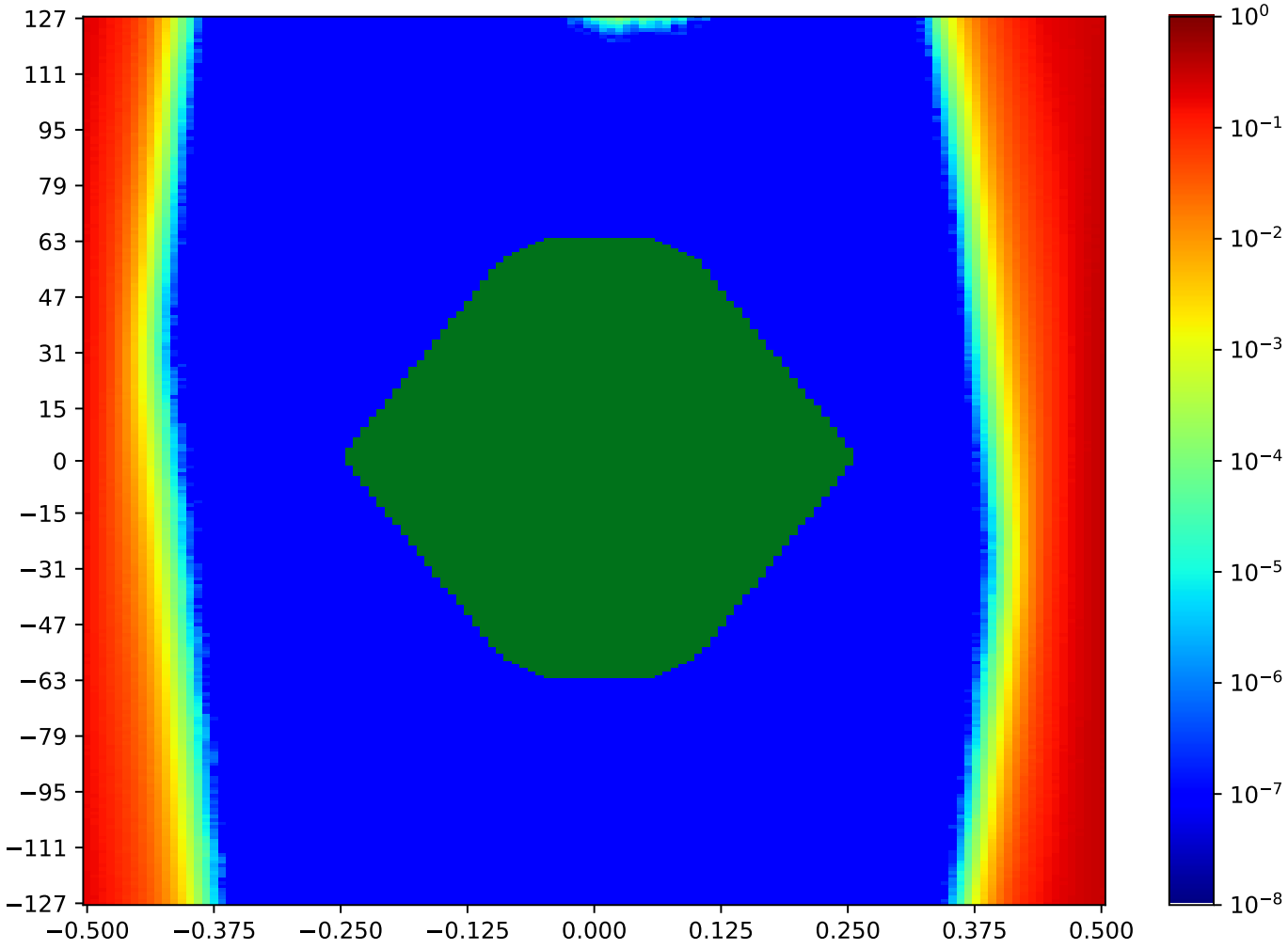


Figure 5.48: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.9 MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Table 5.45: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:20:05		2019-Nov-26 11:21:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24482	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

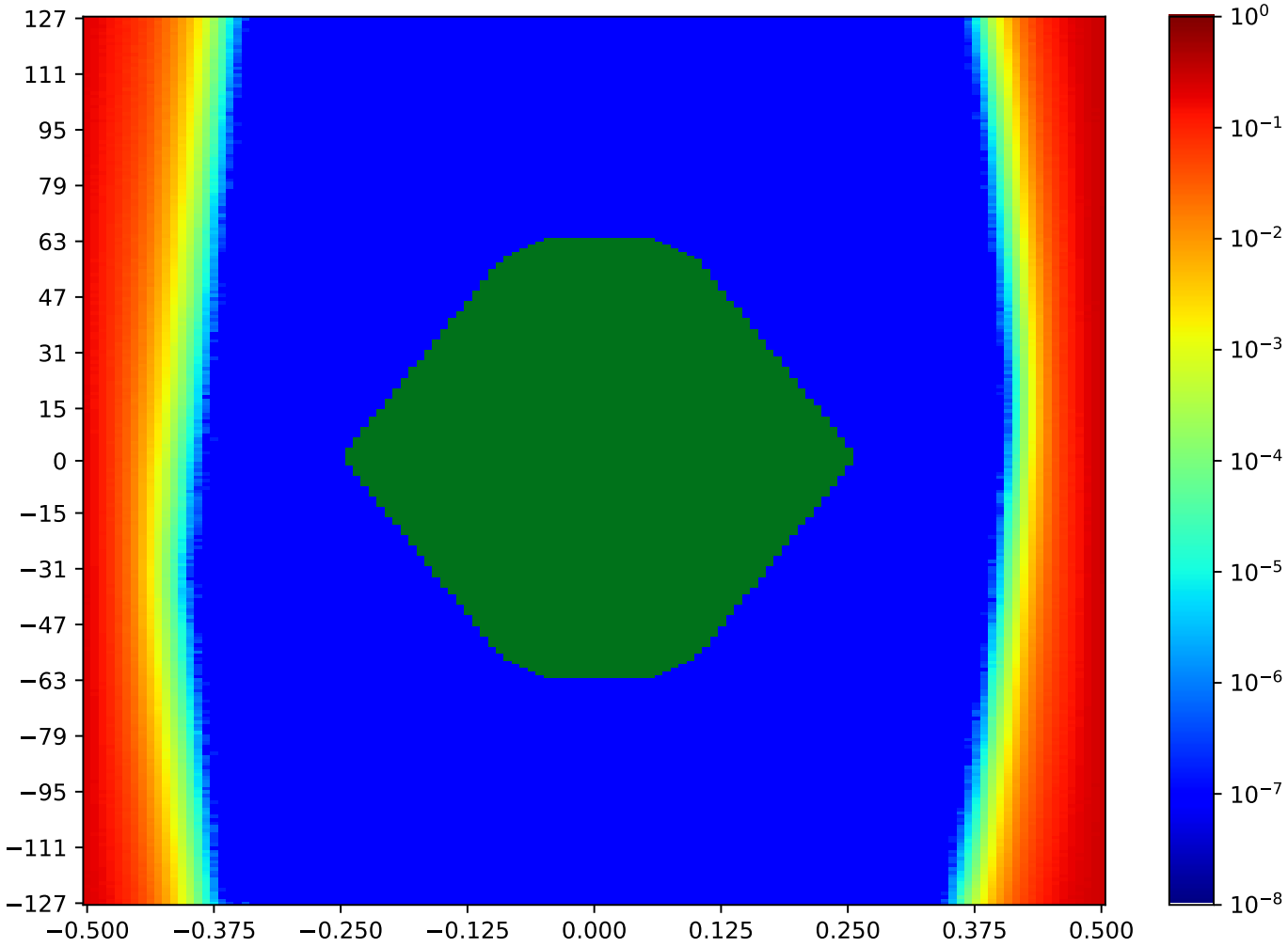


Figure 5.49: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.10 MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Table 5.46: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:14:01		2019-Nov-26 11:15:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24620	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

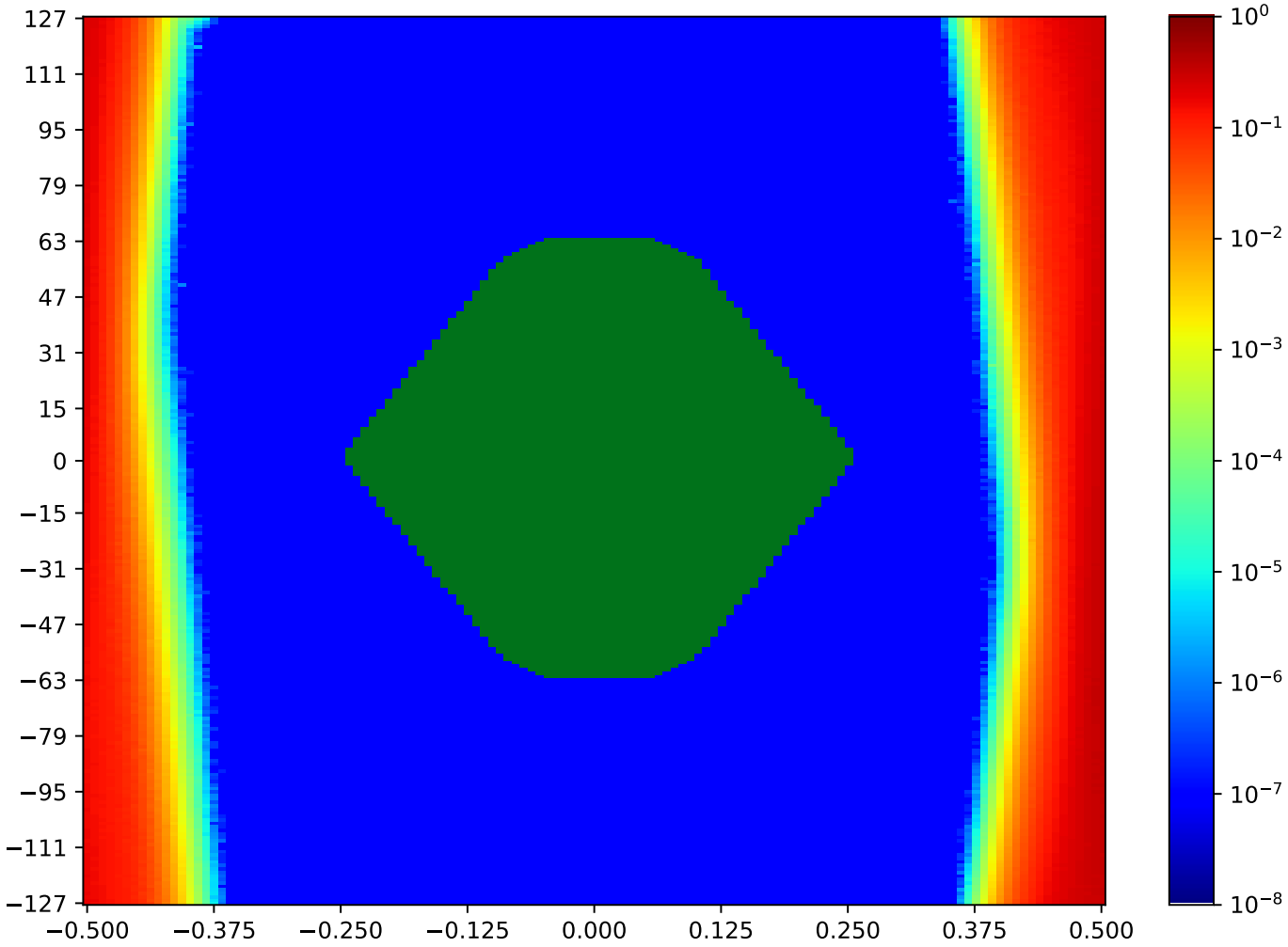


Figure 5.50: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.11 MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Table 5.47: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:17:39		2019-Nov-26 11:18:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23573	99	76.74%	245	95.29%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

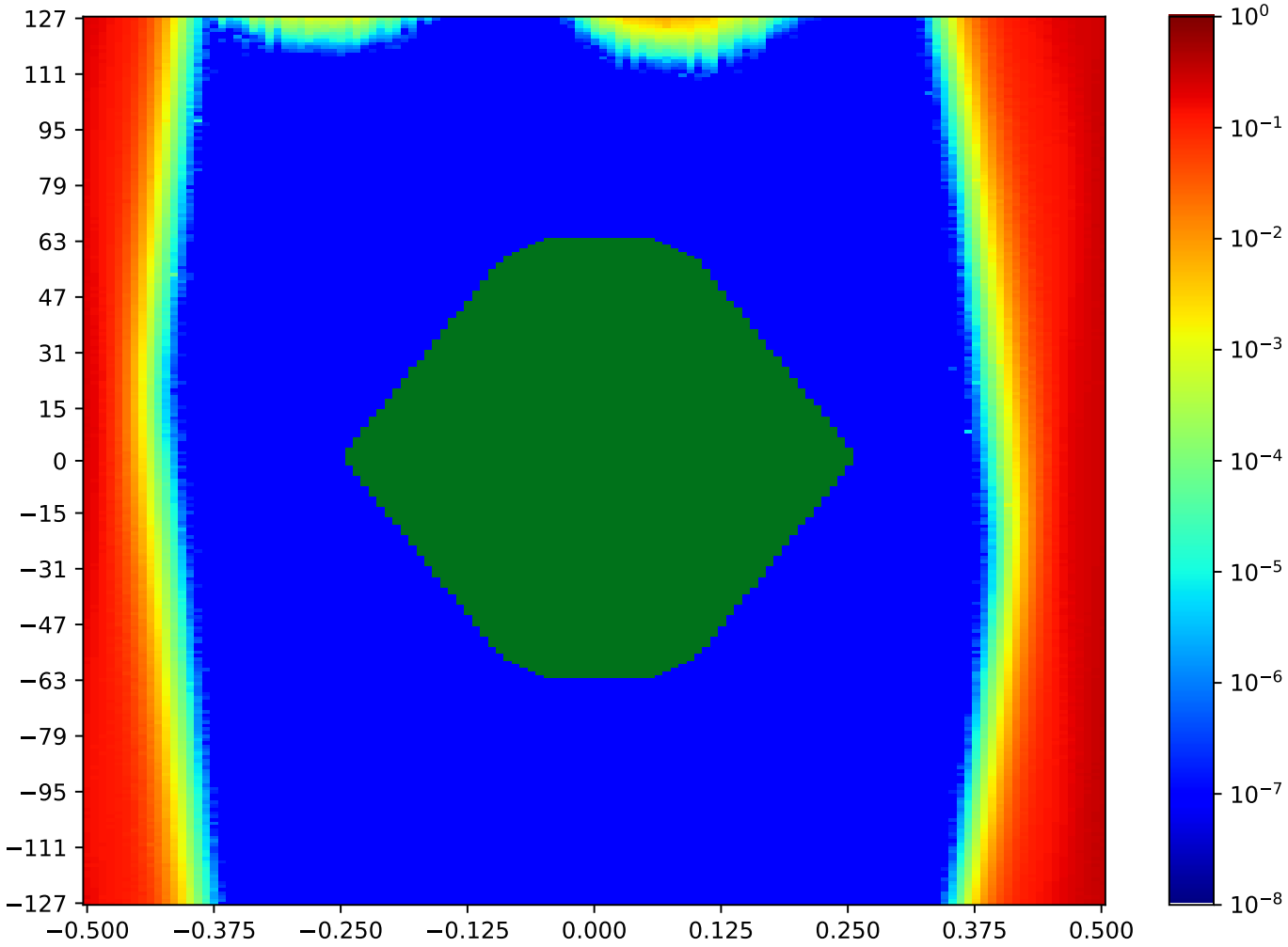


Figure 5.51: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.4.12 MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Table 5.48: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 11:16:16		2019-Nov-26 11:17:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24383	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

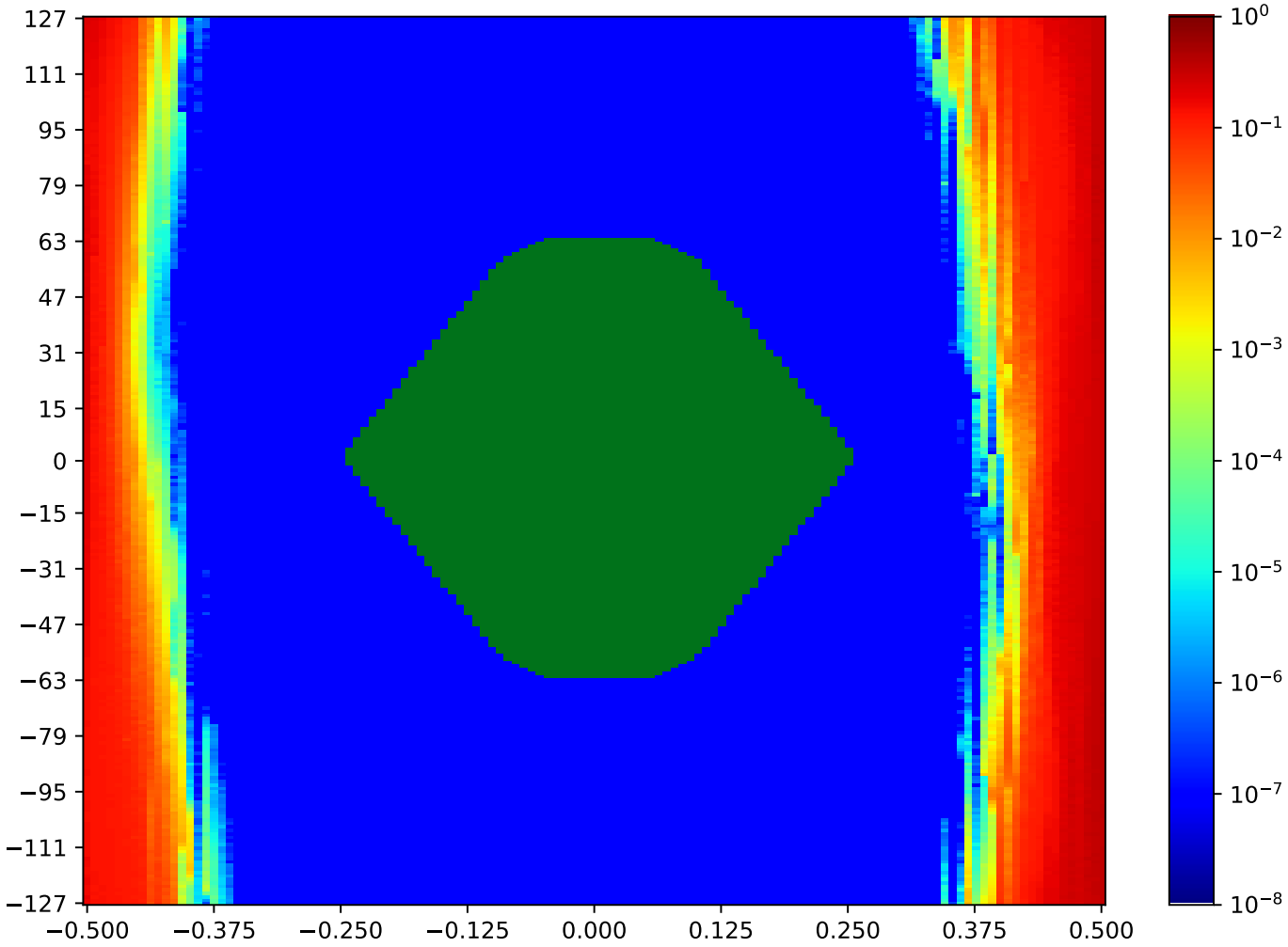


Figure 5.52: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.62.

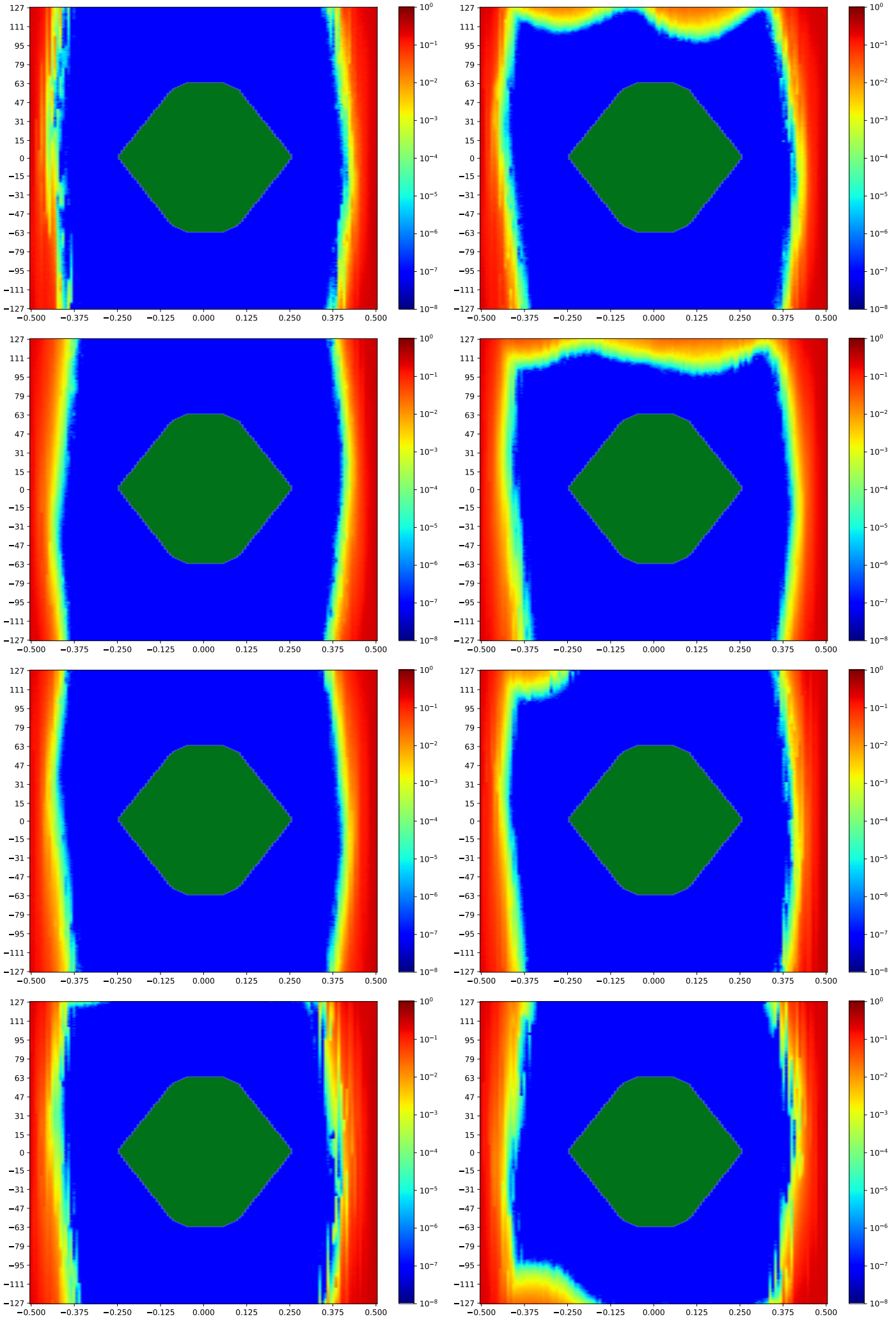


Figure 5.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

5.5.1 TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Table 5.49: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:31:12		2019-Nov-25 21:32:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25101	105	81.40%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

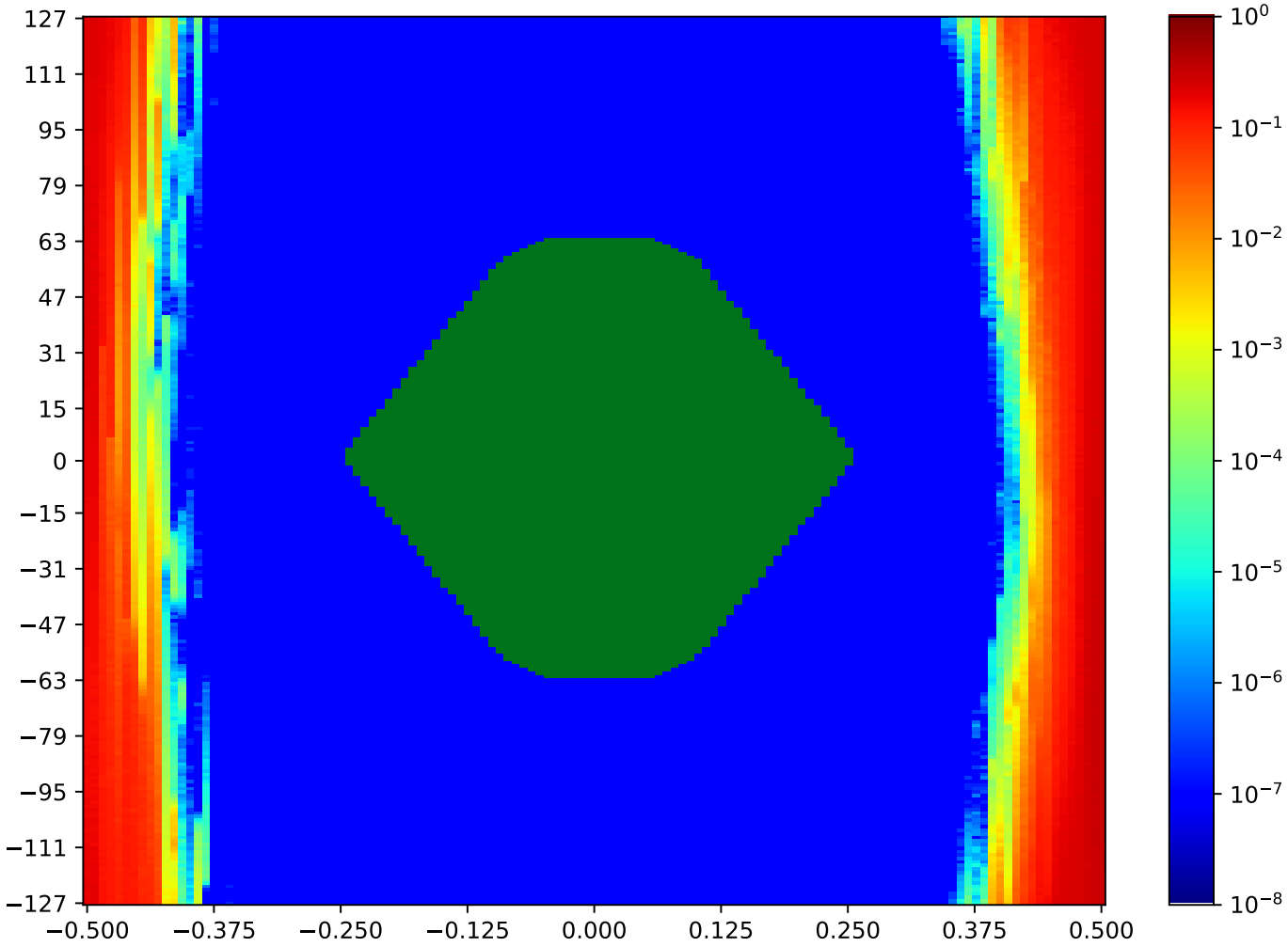


Figure 5.54: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.2 TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Table 5.50: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:28:57		2019-Nov-25 21:30:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22777	102	79.07%	236	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

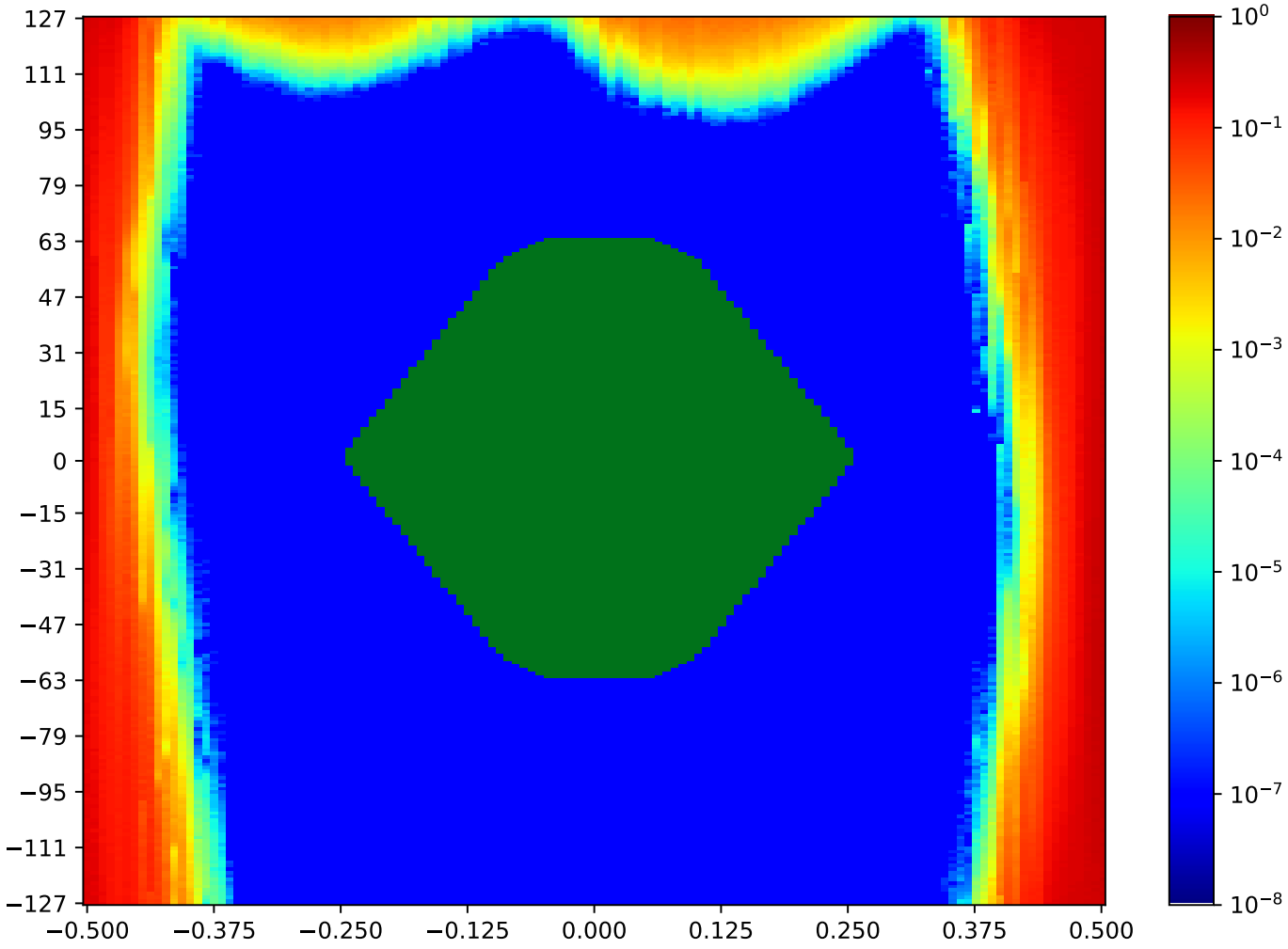


Figure 5.55: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.3 TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Table 5.51: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:33:41		2019-Nov-25 21:35:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24679	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

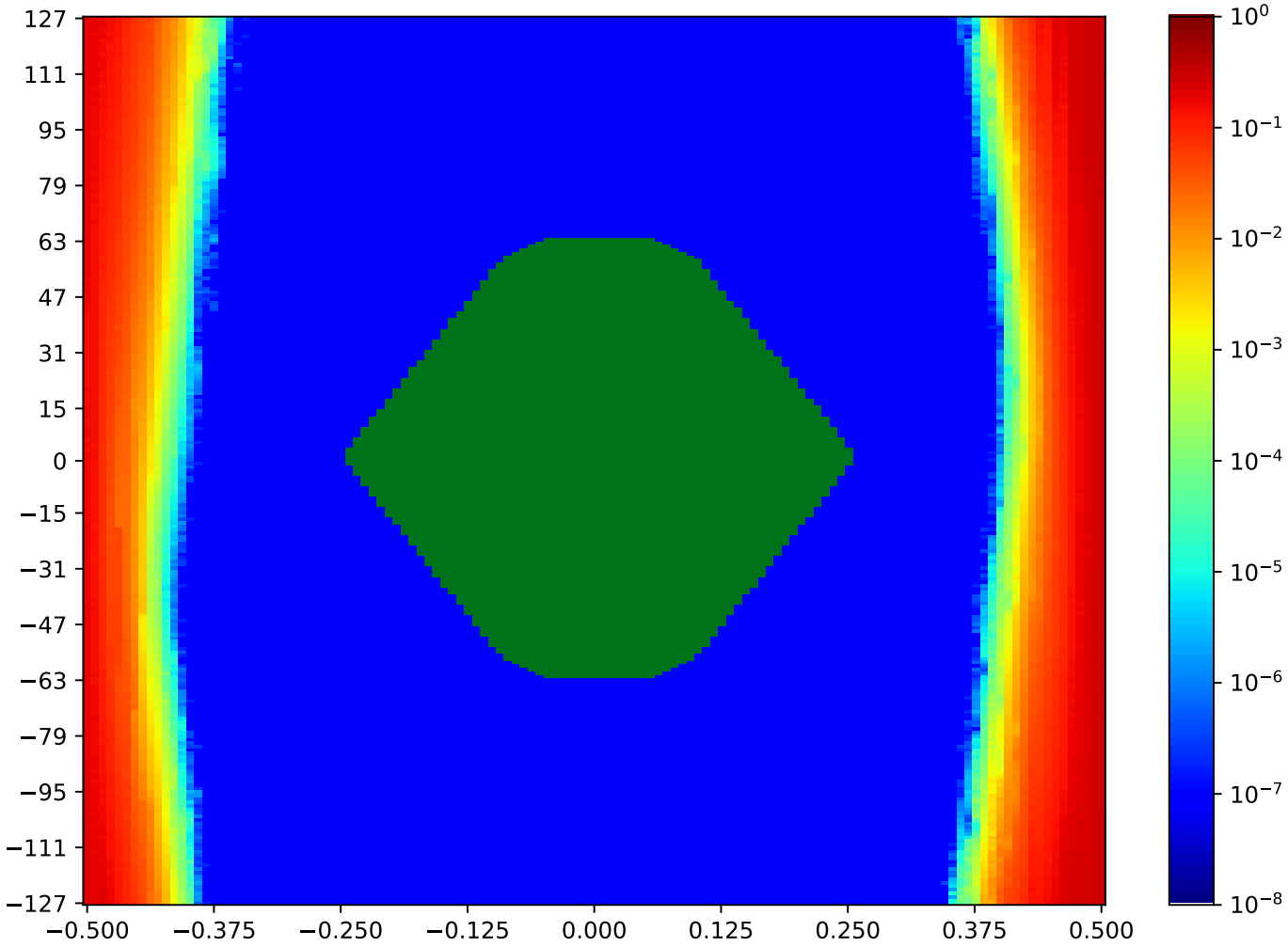


Figure 5.56: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.4 TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Table 5.52: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:30:04		2019-Nov-25 21:31:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21869	99	76.74%	229	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

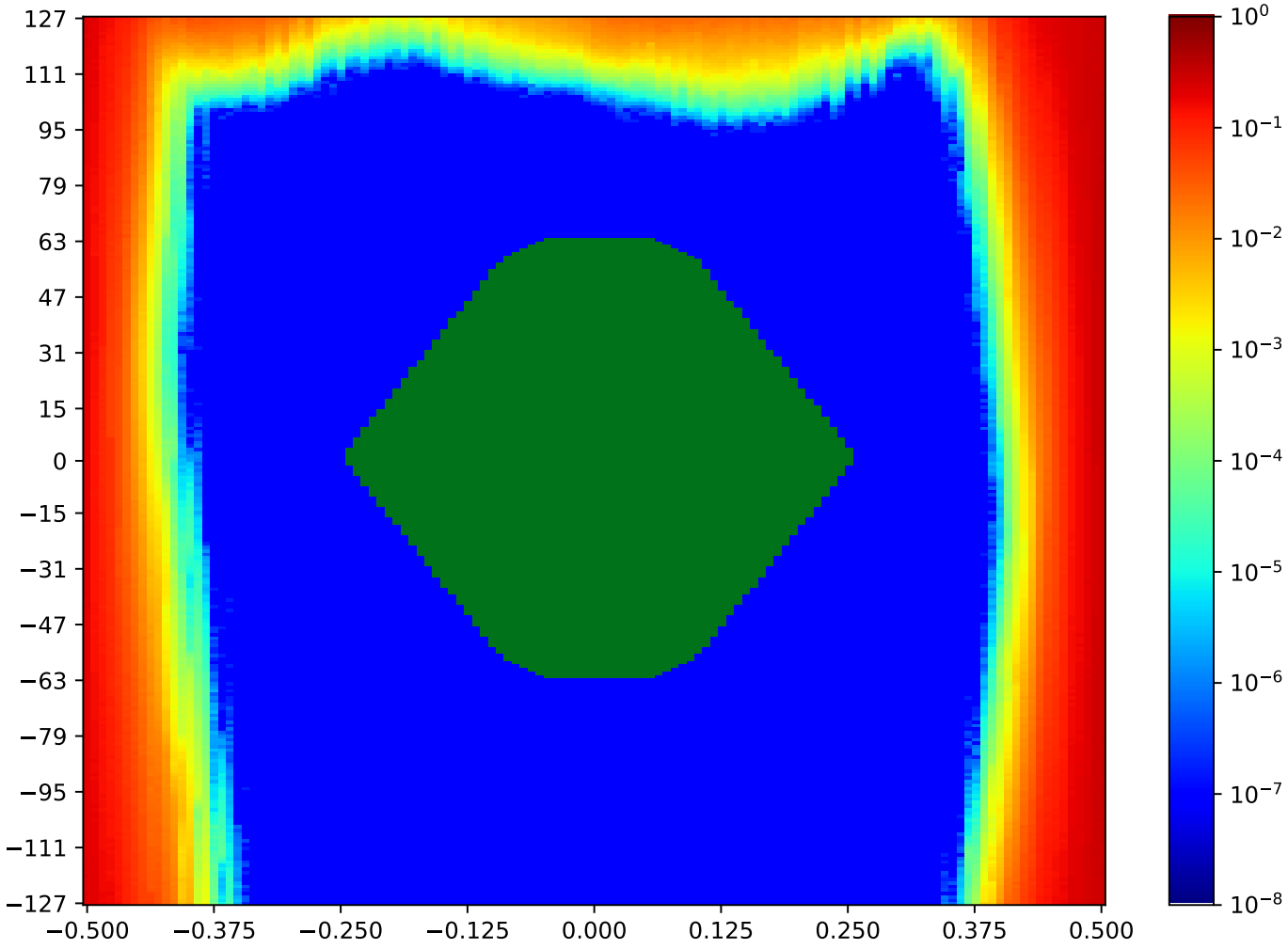


Figure 5.57: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.5 TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Table 5.53: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:36:08		2019-Nov-25 21:37:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24644	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

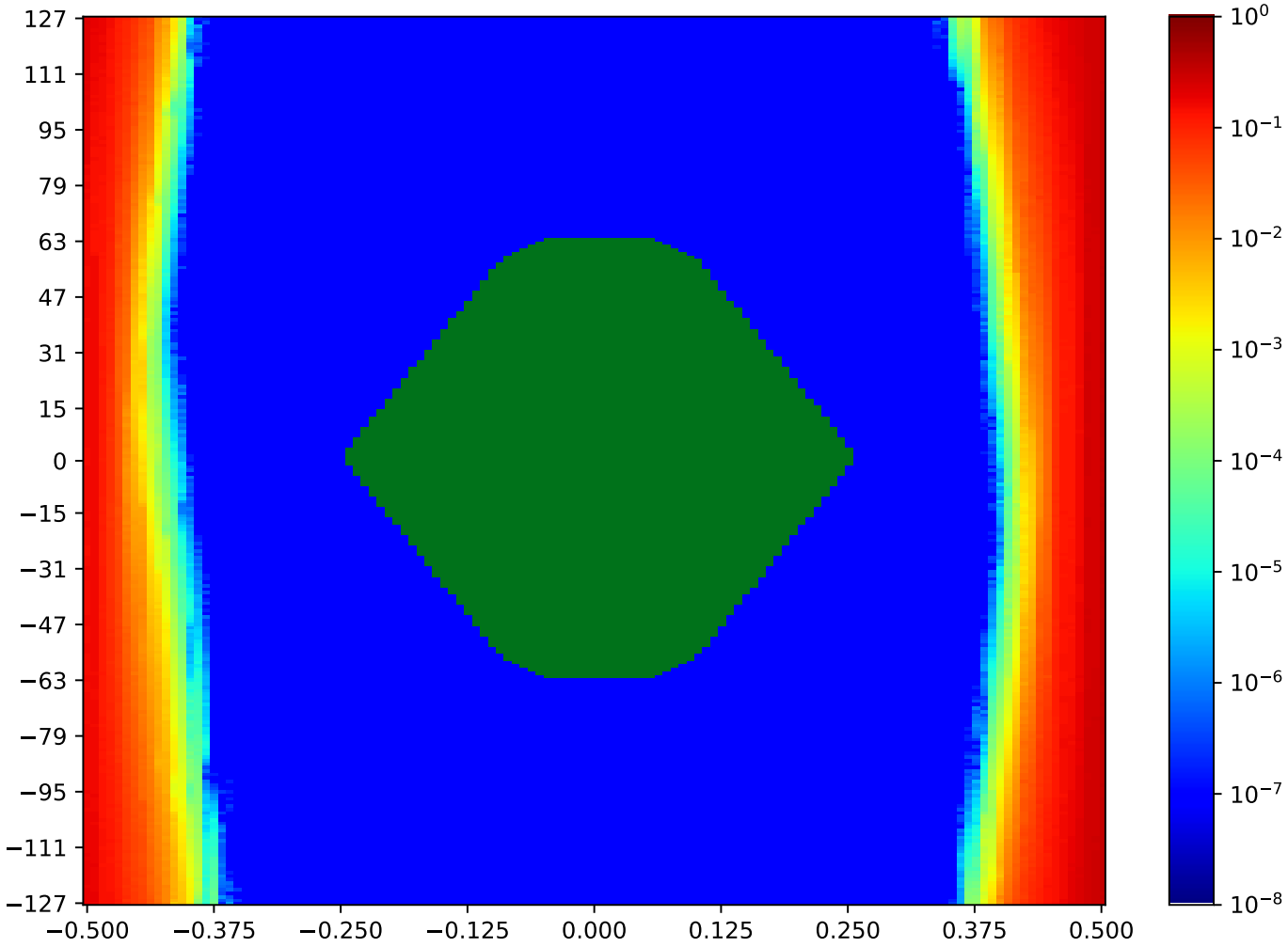


Figure 5.58: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.6 TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Table 5.54: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:27:49		2019-Nov-25 21:28:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24256	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

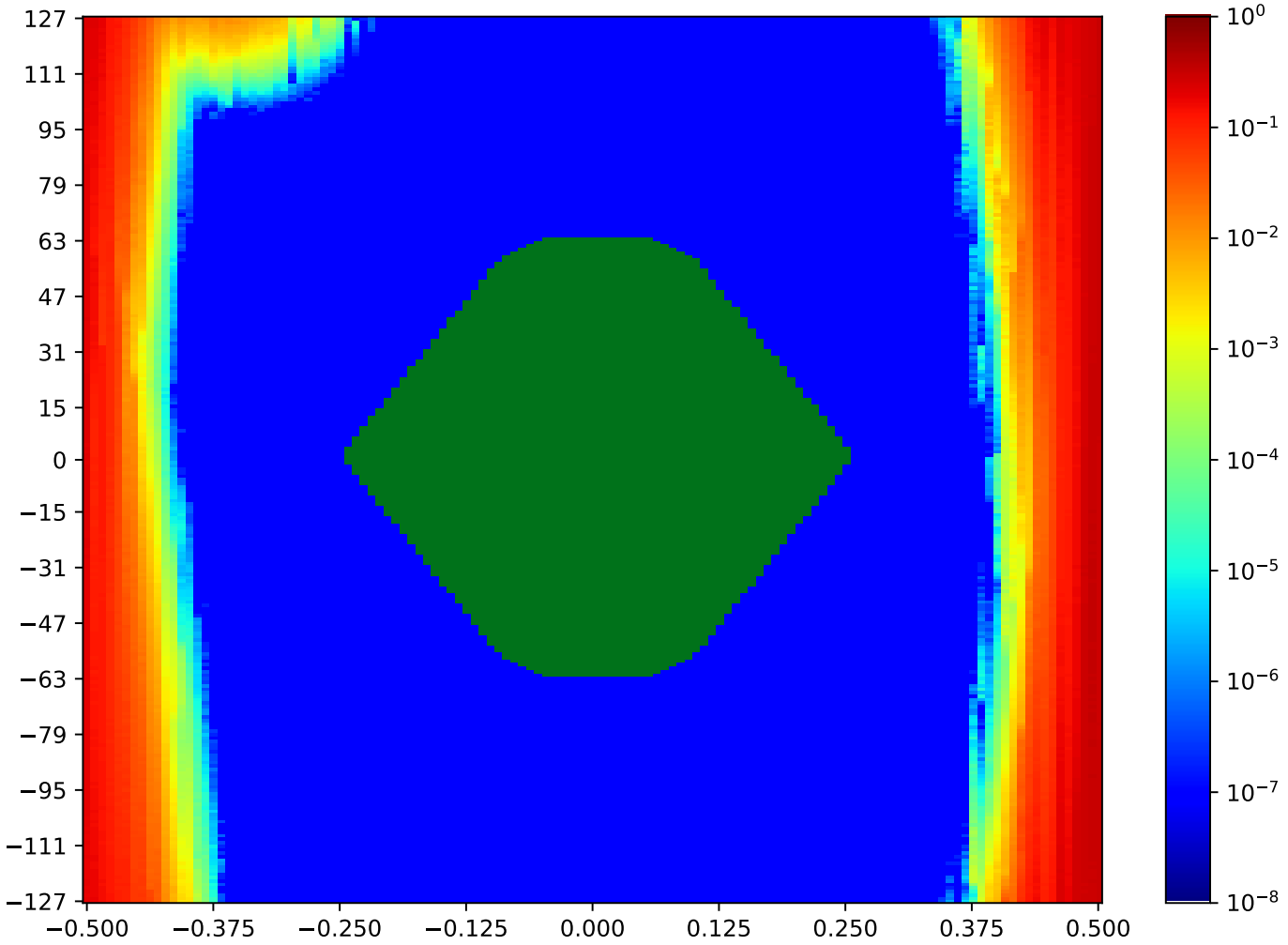


Figure 5.59: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.7 TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Table 5.55: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:32:19		2019-Nov-25 21:33:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23694	95	73.64%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

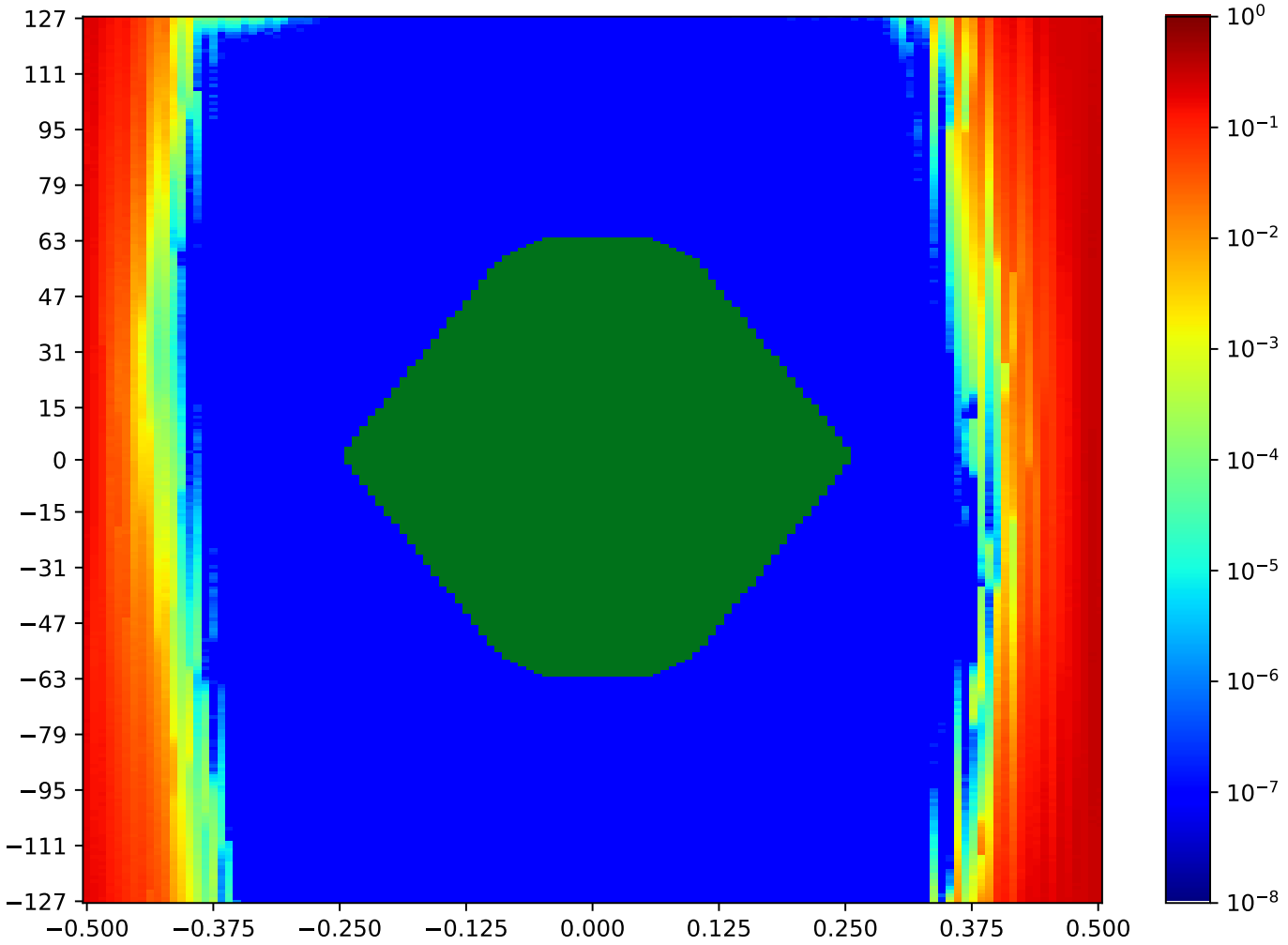


Figure 5.60: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.5.8 TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Table 5.56: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-25 21:35:01		2019-Nov-25 21:36:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23276	101	77.52%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

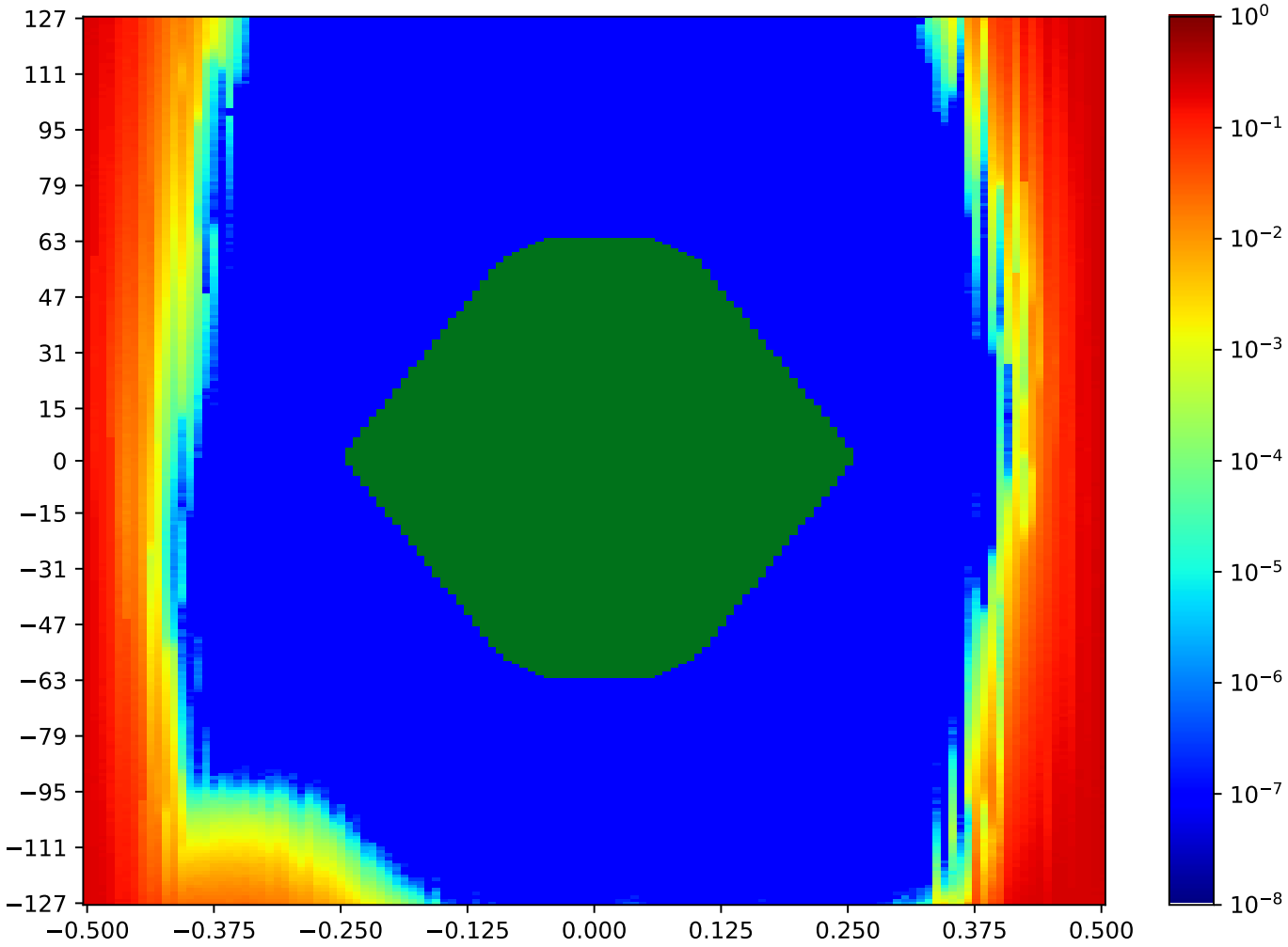


Figure 5.61: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.6 TRP J1 QSFP Loopback

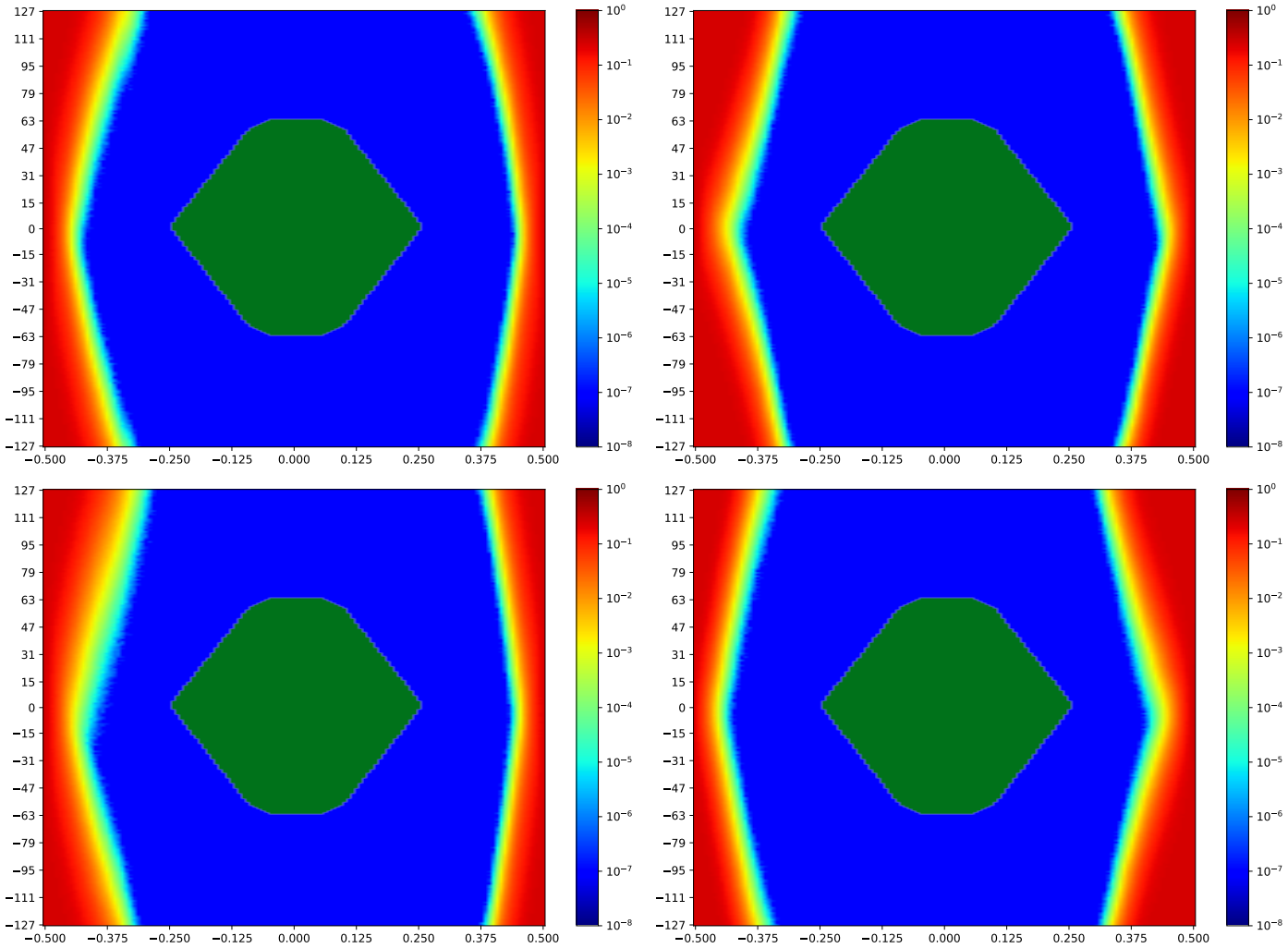


Figure 5.62: TRP J1 QSFP Loopback

A cross-reference to Figure 5.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.67.

5.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 5.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 11:55:46		2019-Nov-26 11:56:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24818	107	82.95%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

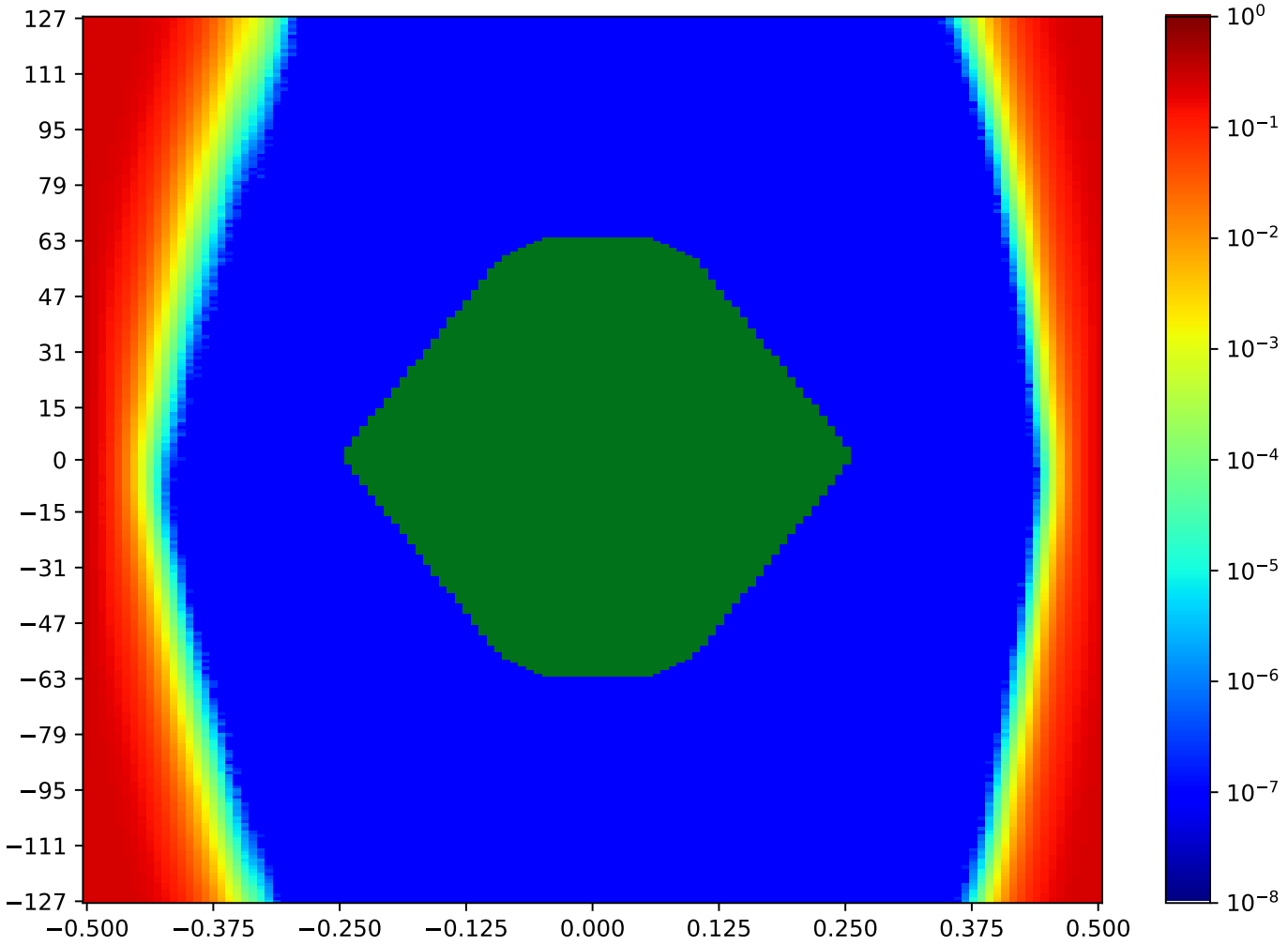


Figure 5.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 5.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 11:56:52		2019-Nov-26 11:57:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23453	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

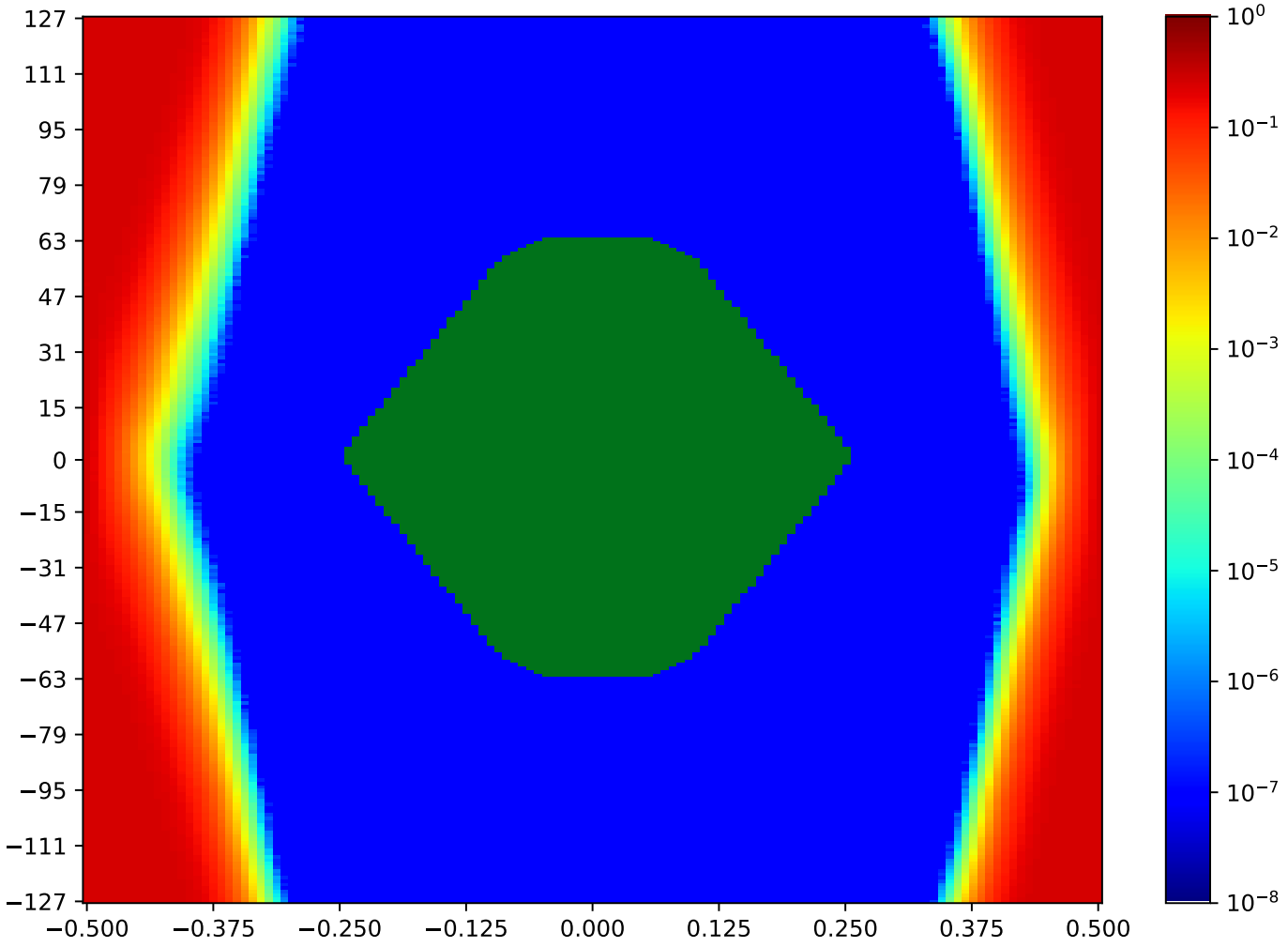


Figure 5.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 5.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 11:57:56		2019-Nov-26 11:59:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24040	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

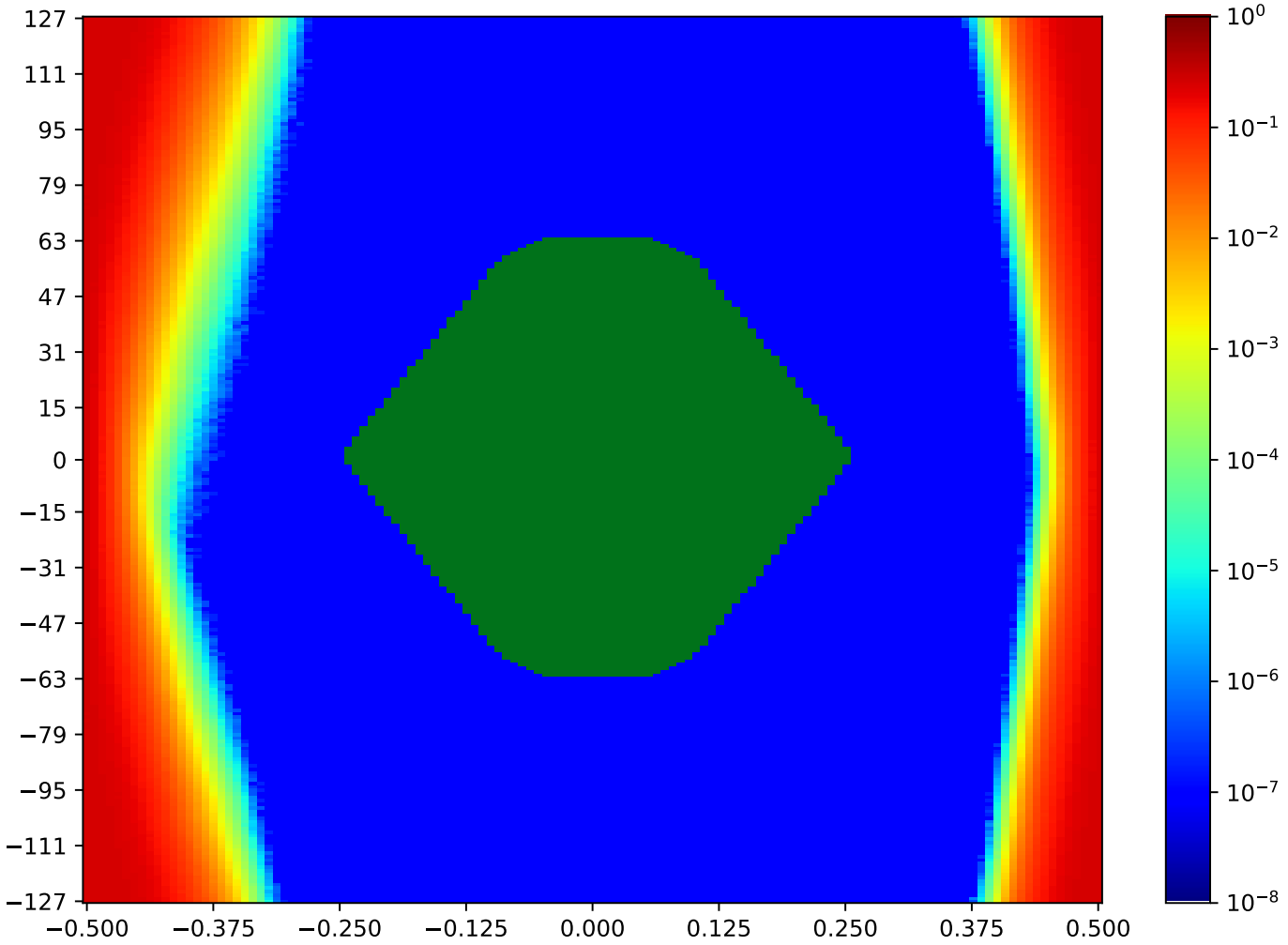


Figure 5.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 5.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 11:59:01		2019-Nov-26 12:00:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23586	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

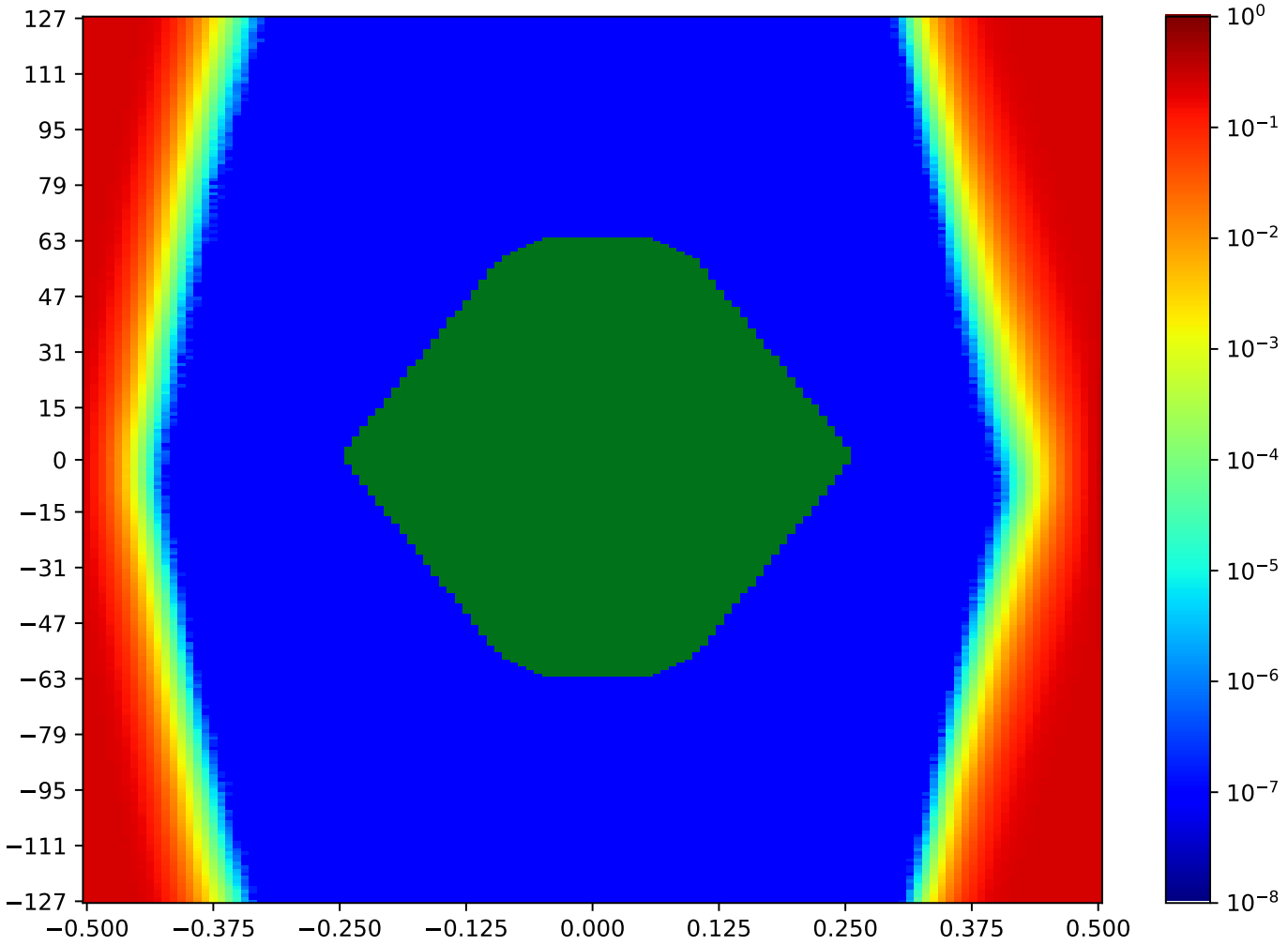


Figure 5.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.7 TRP J3 SFP Loopback

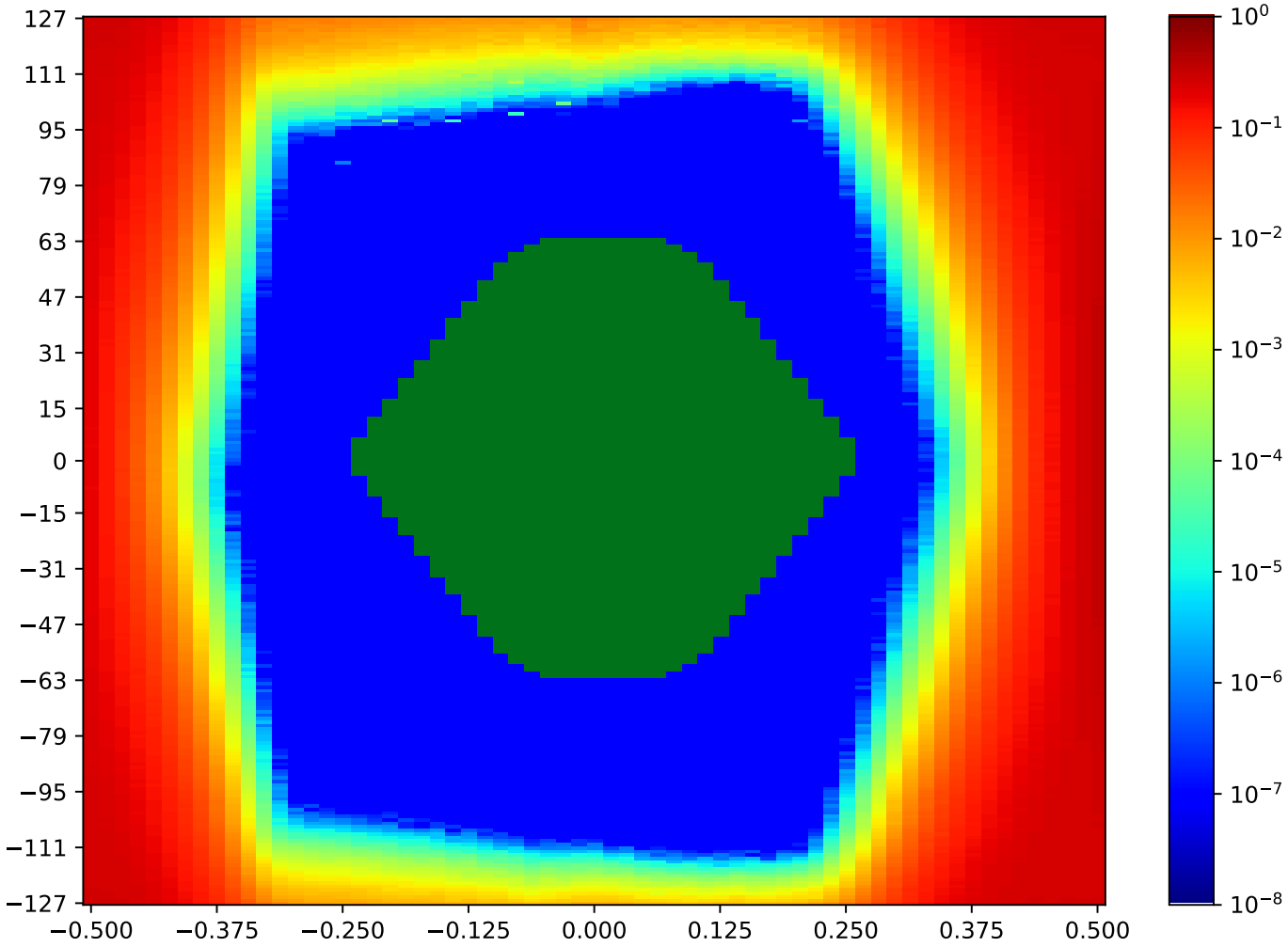


Figure 5.67: TRP J3 SFP Loopback

A cross-reference to Figure 5.67. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.69.

5.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 5.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 12:00:07		2019-Nov-26 12:00:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7908	43	66.15%	209	81.57%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

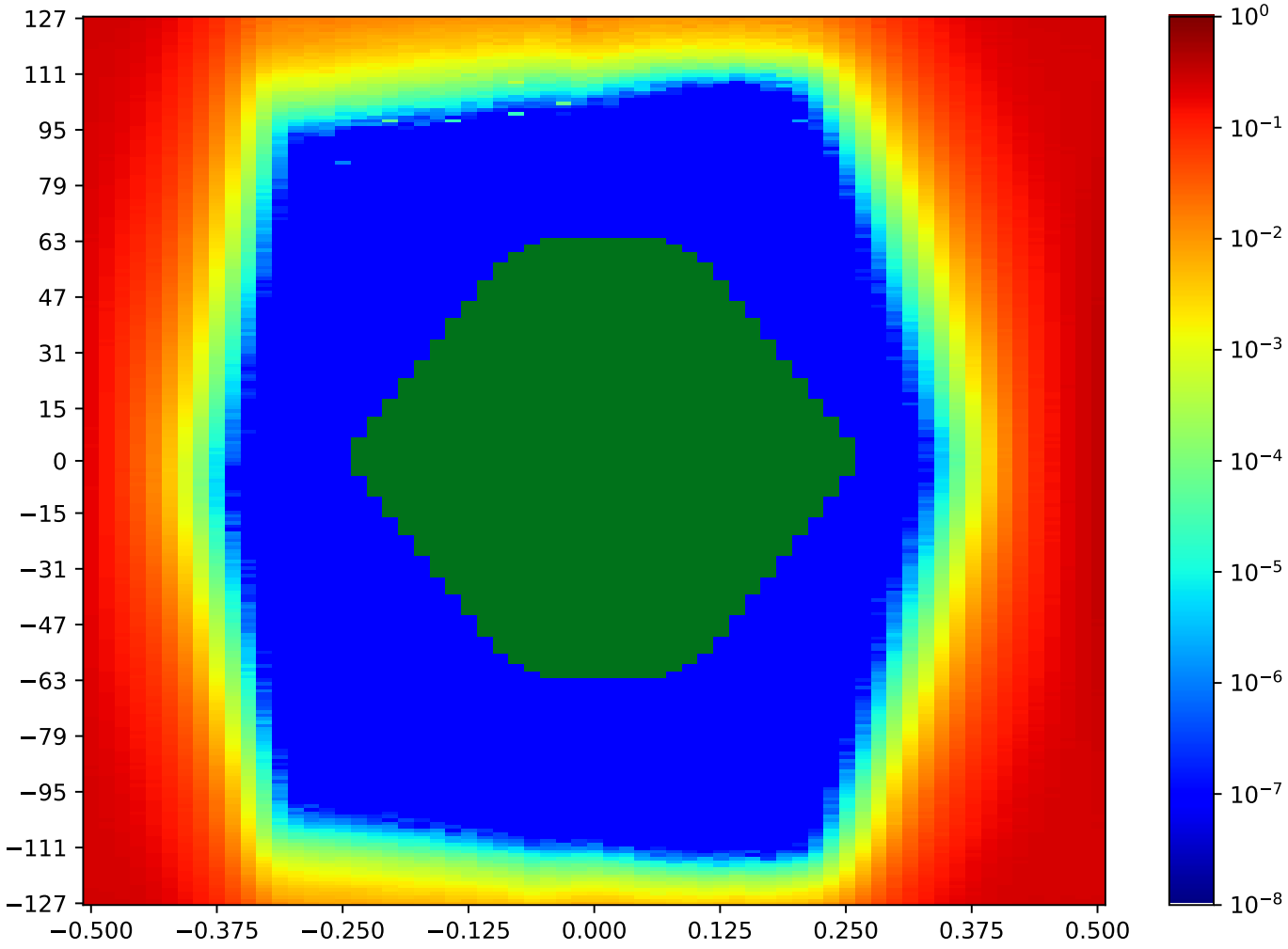


Figure 5.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 5.67. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8 MSP_A TRP On board links

A cross-reference to Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.98.

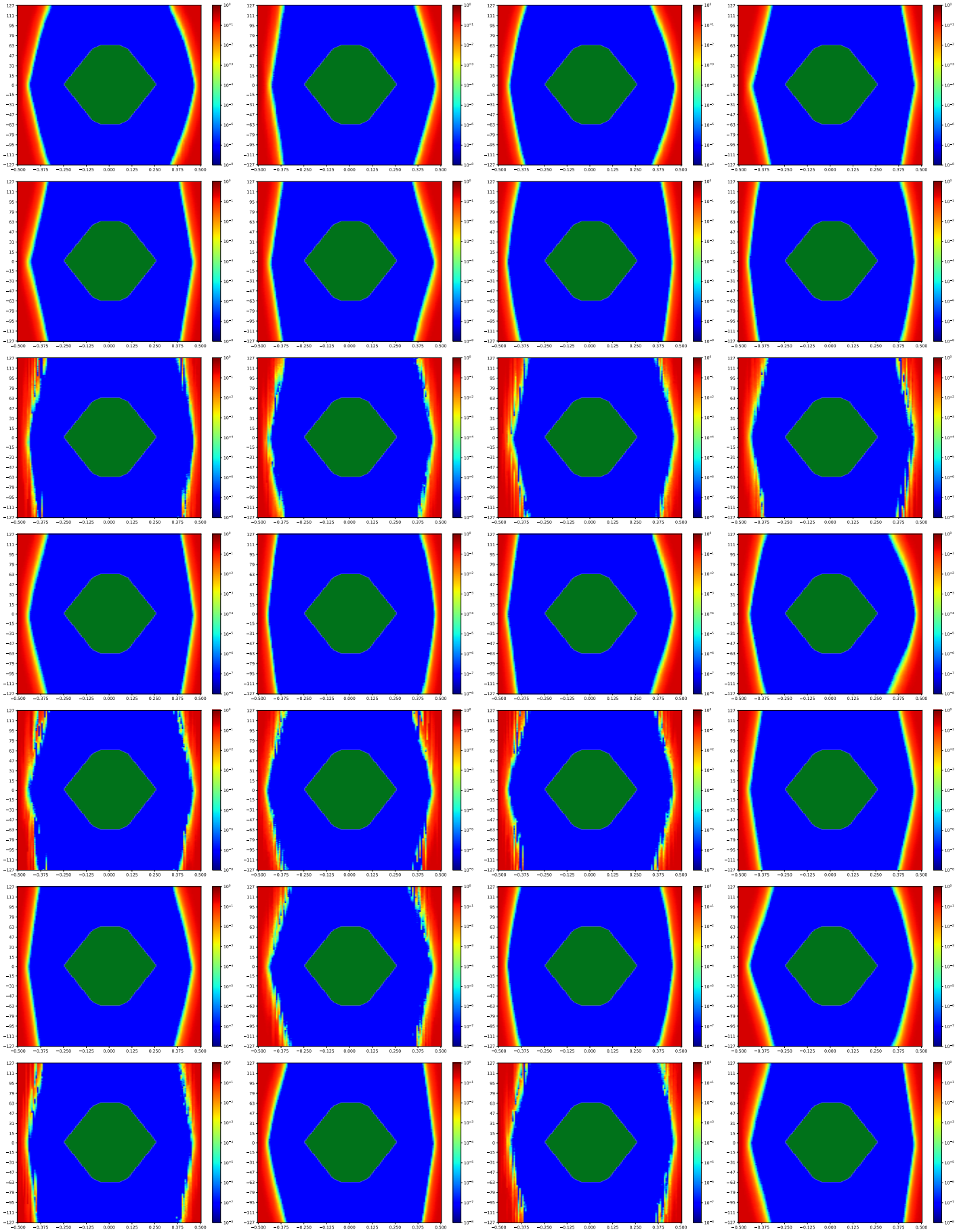


Figure 5.69: MSP_A TRP On board links

5.8.1 MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Table 5.62: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:37:15		2019-Nov-25 21:38:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25383	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

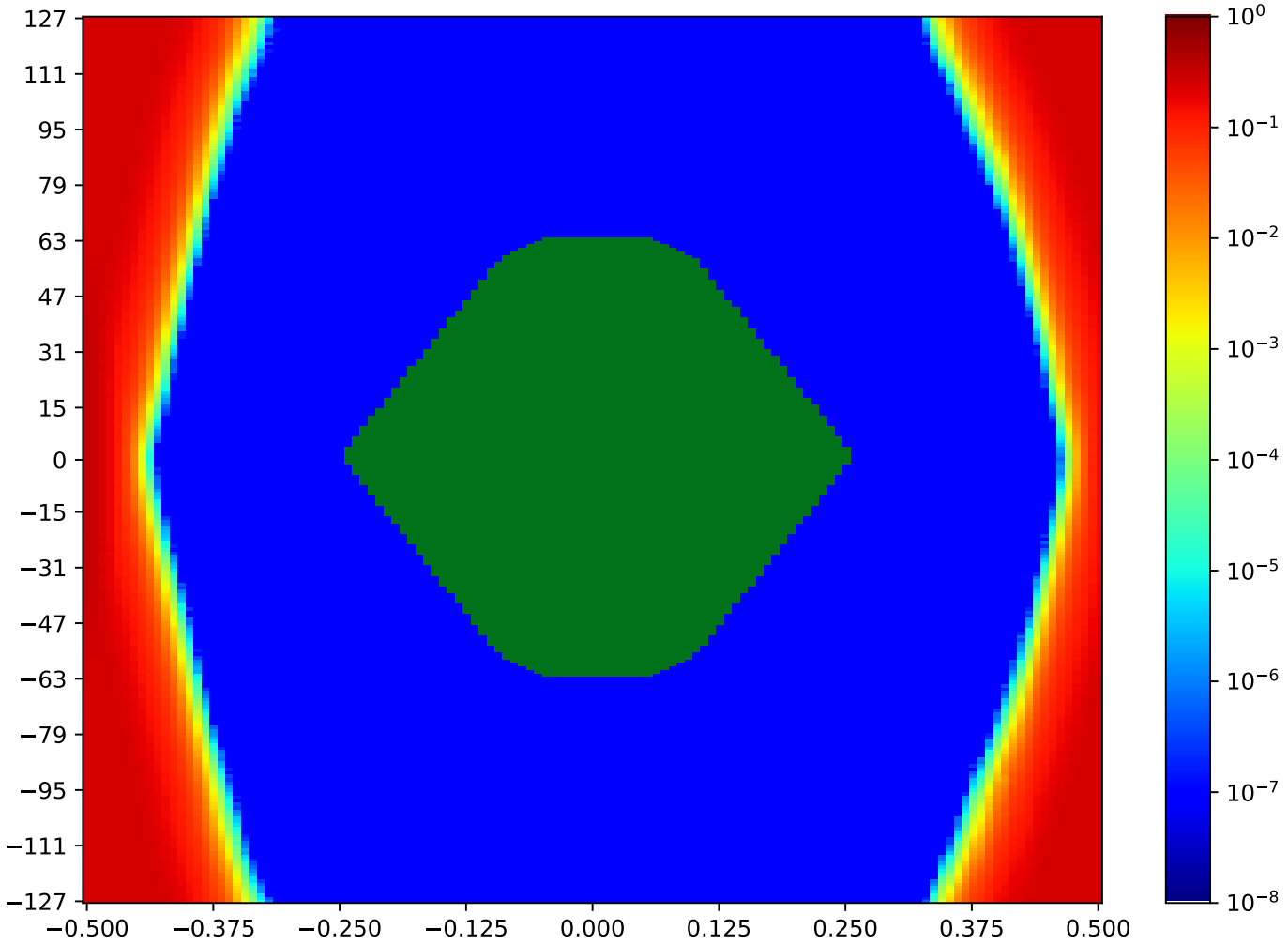


Figure 5.70: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.2 MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Table 5.63: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:38:20		2019-Nov-25 21:39:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25758	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

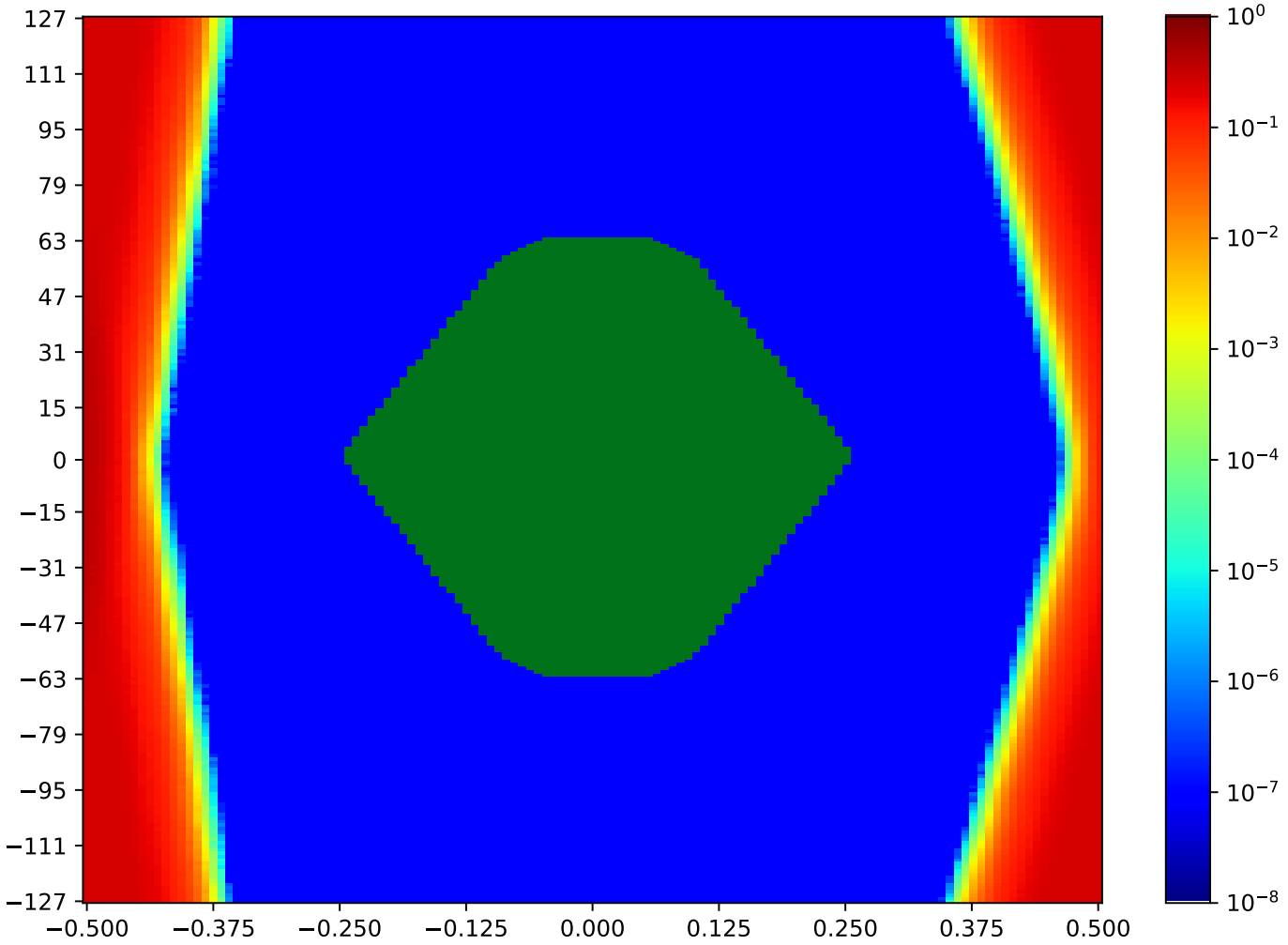


Figure 5.71: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.3 MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Table 5.64: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:39:25		2019-Nov-25 21:40:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25877	114	88.37%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

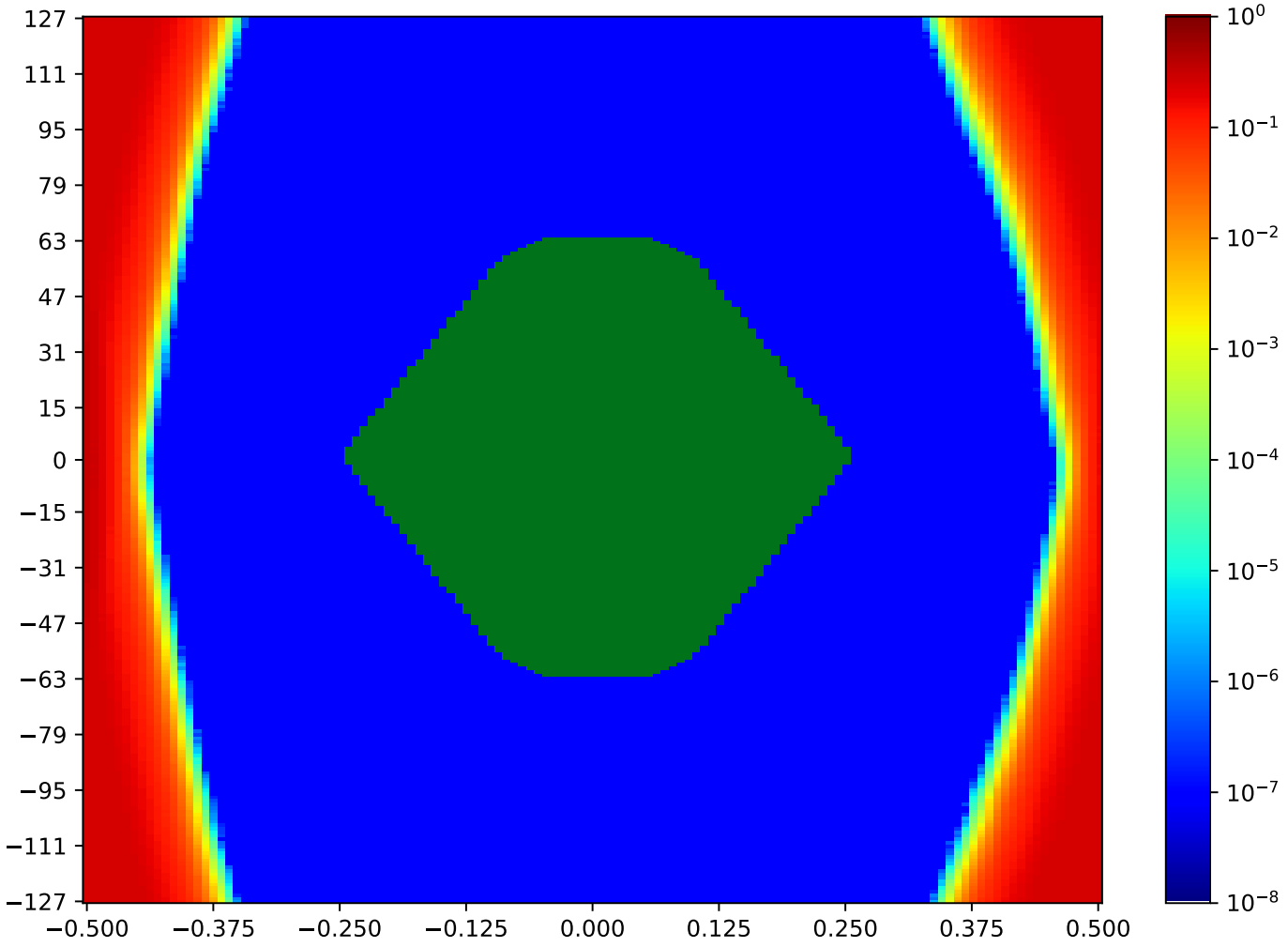


Figure 5.72: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.4 MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Table 5.65: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:40:32		2019-Nov-25 21:41:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25448	111	86.05%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

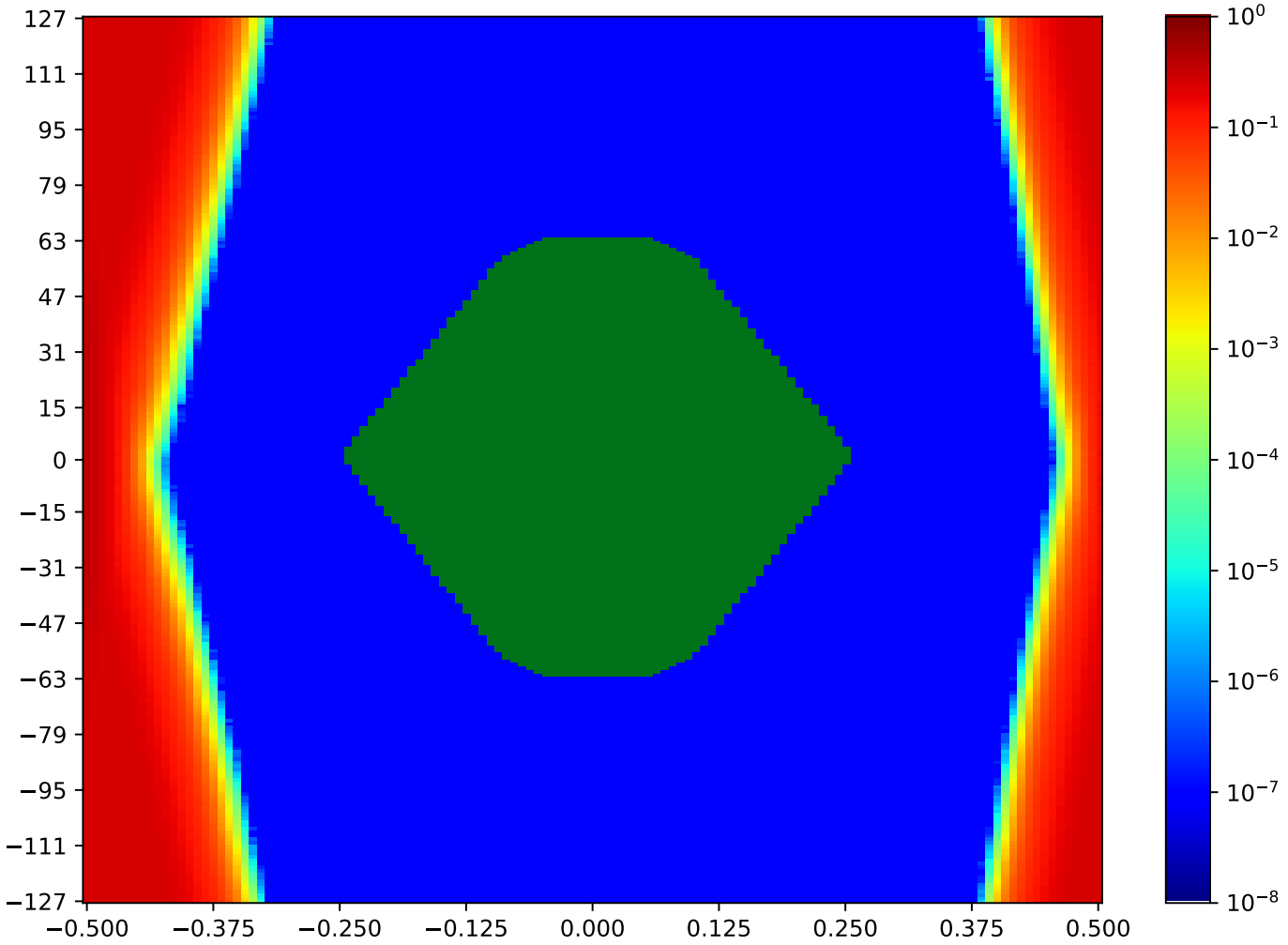


Figure 5.73: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.5 MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Table 5.66: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:41:37		2019-Nov-25 21:42:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25669	111	86.05%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

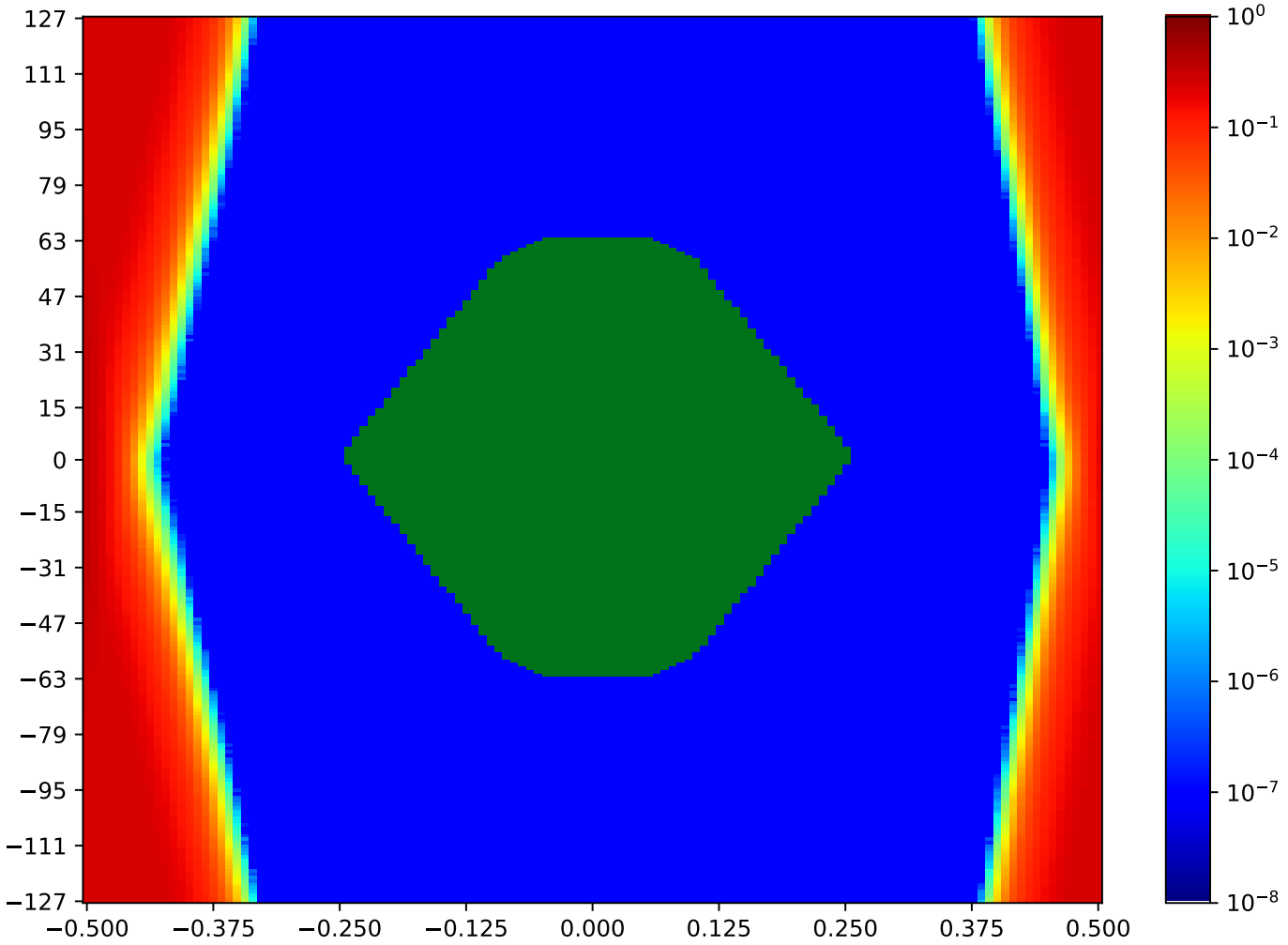


Figure 5.74: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.6 MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Table 5.67: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:42:42		2019-Nov-25 21:43:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25591	111	86.05%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

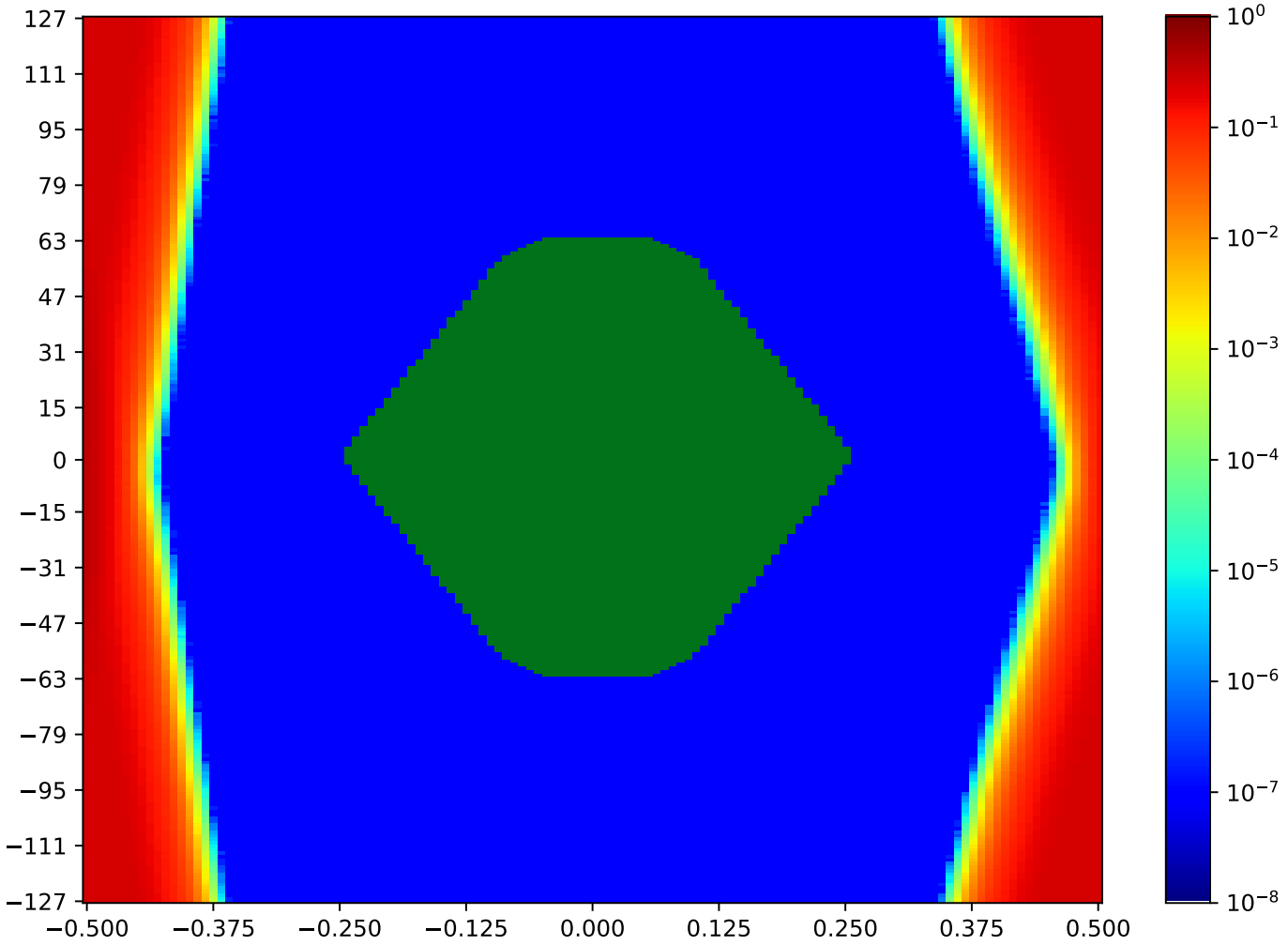


Figure 5.75: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.7 MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Table 5.68: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:43:48		2019-Nov-25 21:44:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	27037	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

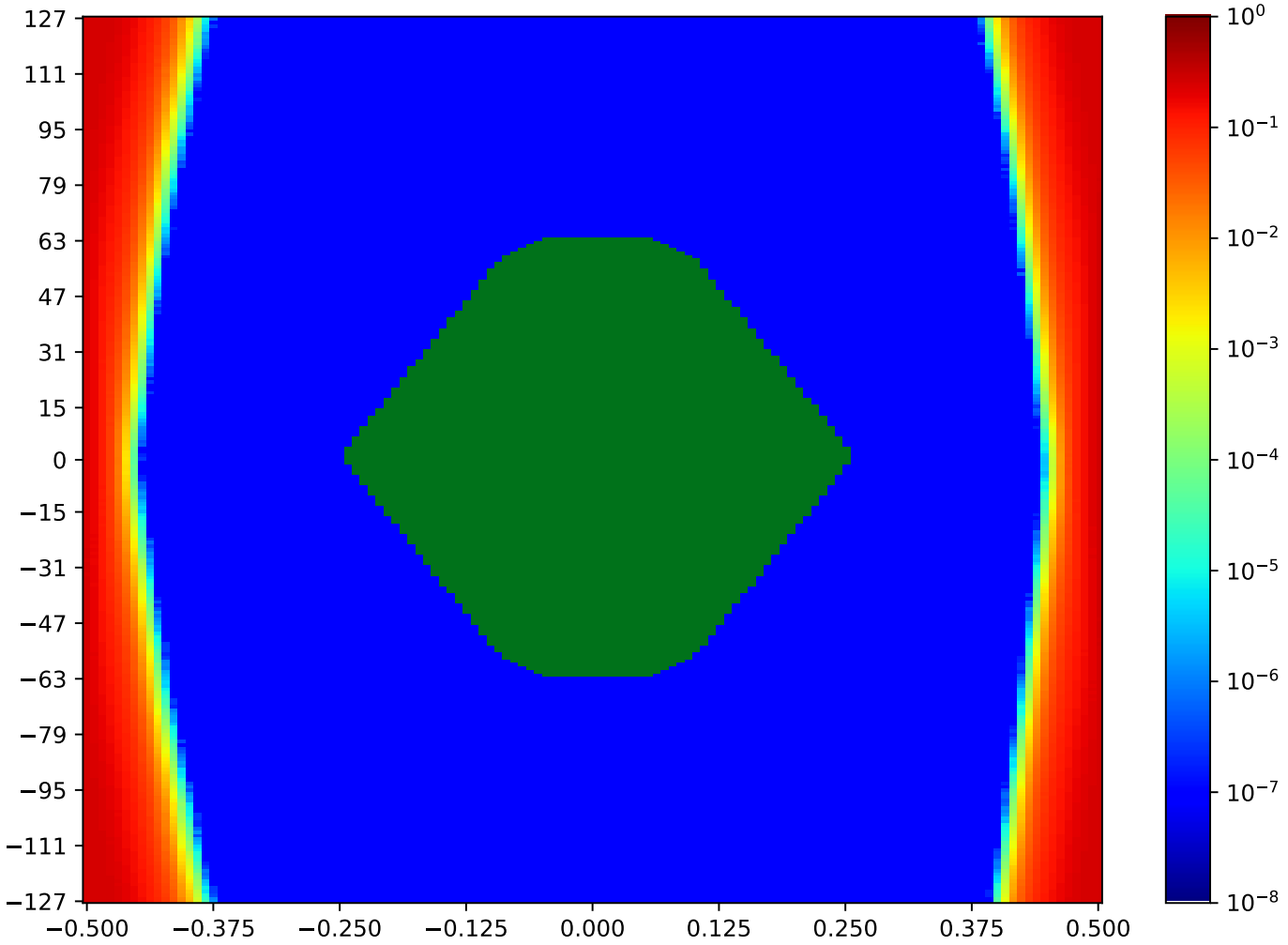


Figure 5.76: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.8 MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Table 5.69: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:44:55		2019-Nov-25 21:46:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	27080	114	88.37%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

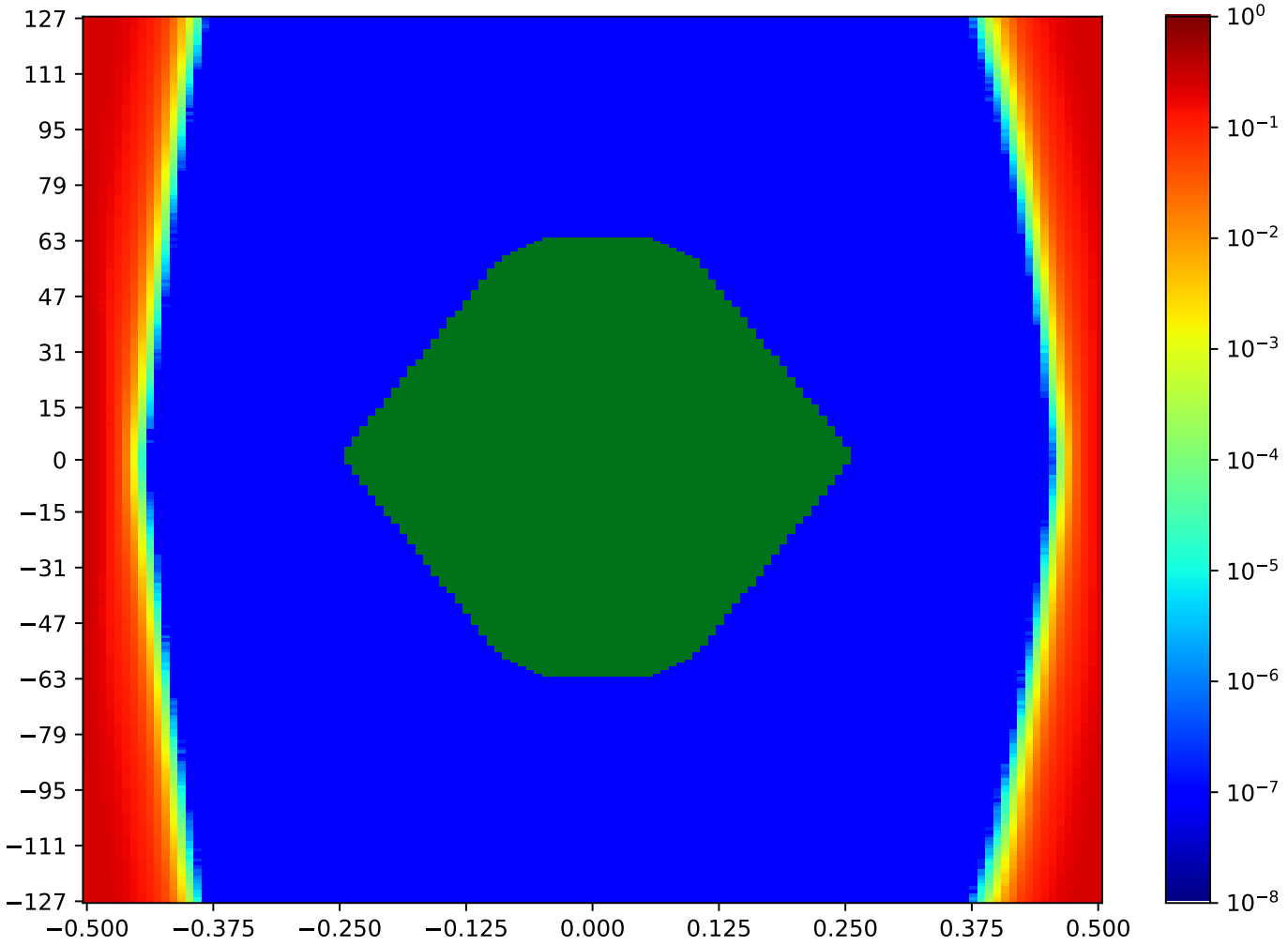


Figure 5.77: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.9 MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Table 5.70: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:46:02		2019-Nov-25 21:47:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26719	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

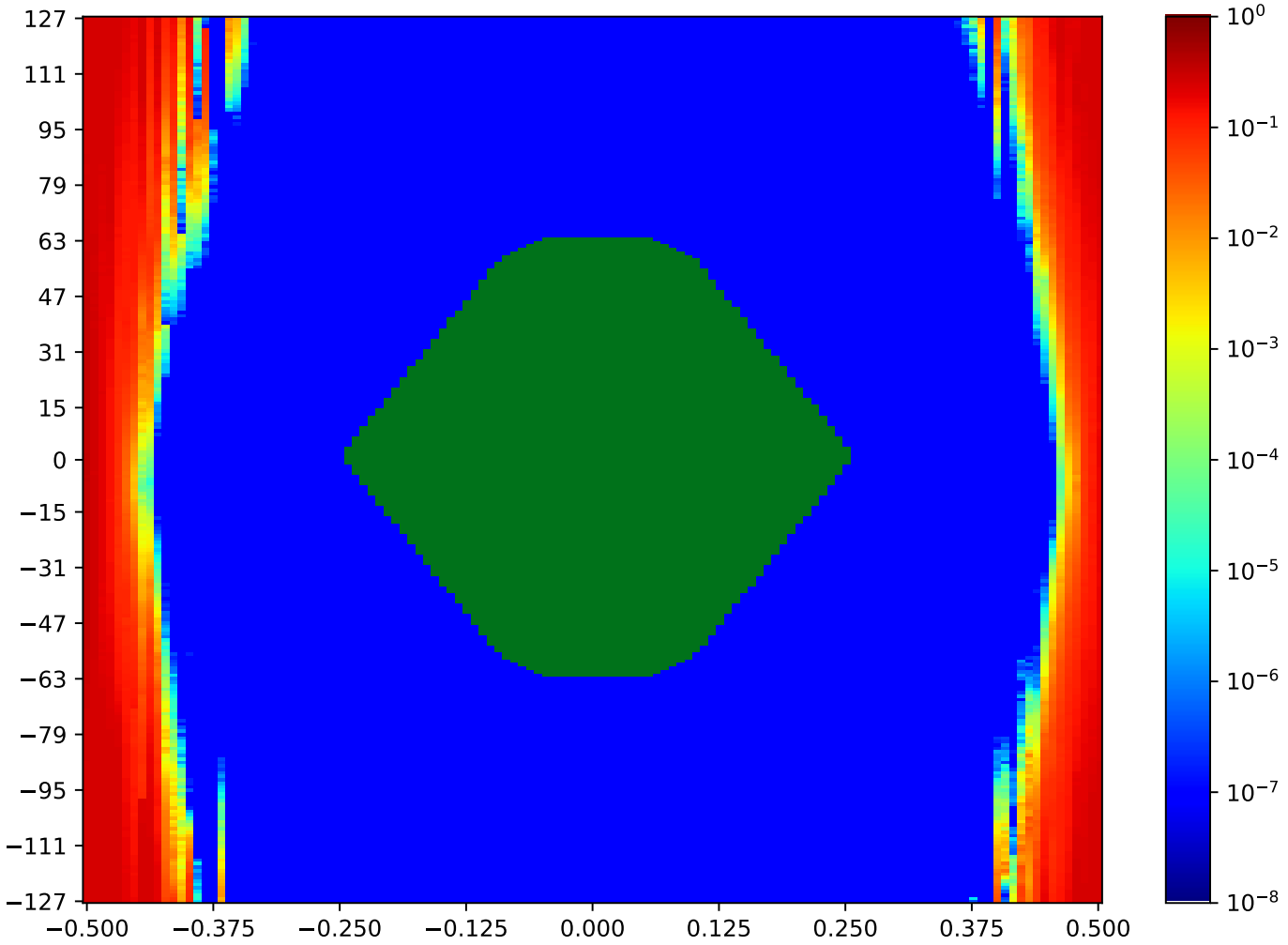


Figure 5.78: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.10 MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Table 5.71: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:47:09		2019-Nov-25 21:48:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25921	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

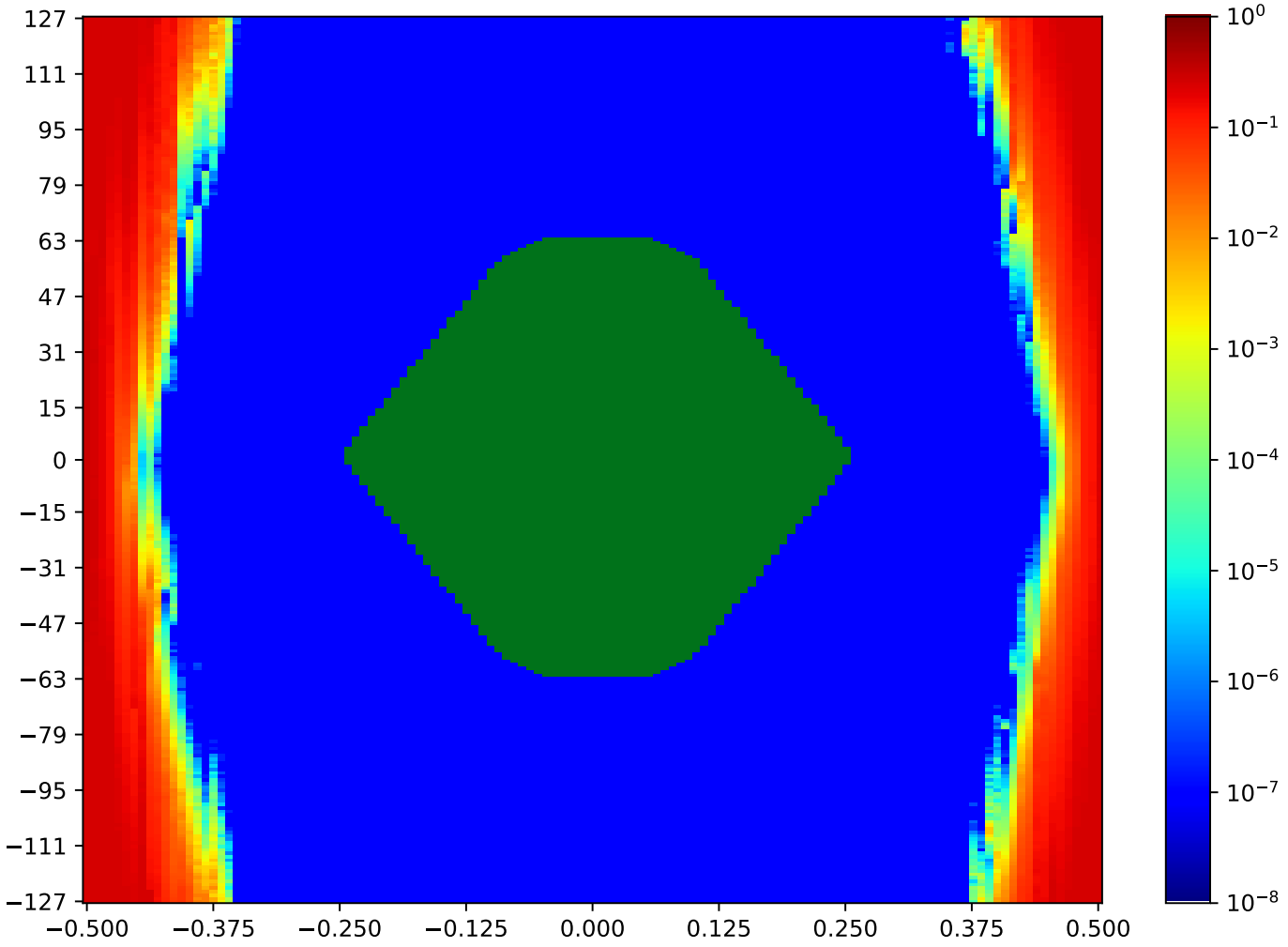


Figure 5.79: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.11 MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Table 5.72: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:48:15		2019-Nov-25 21:49:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25495	110	85.27%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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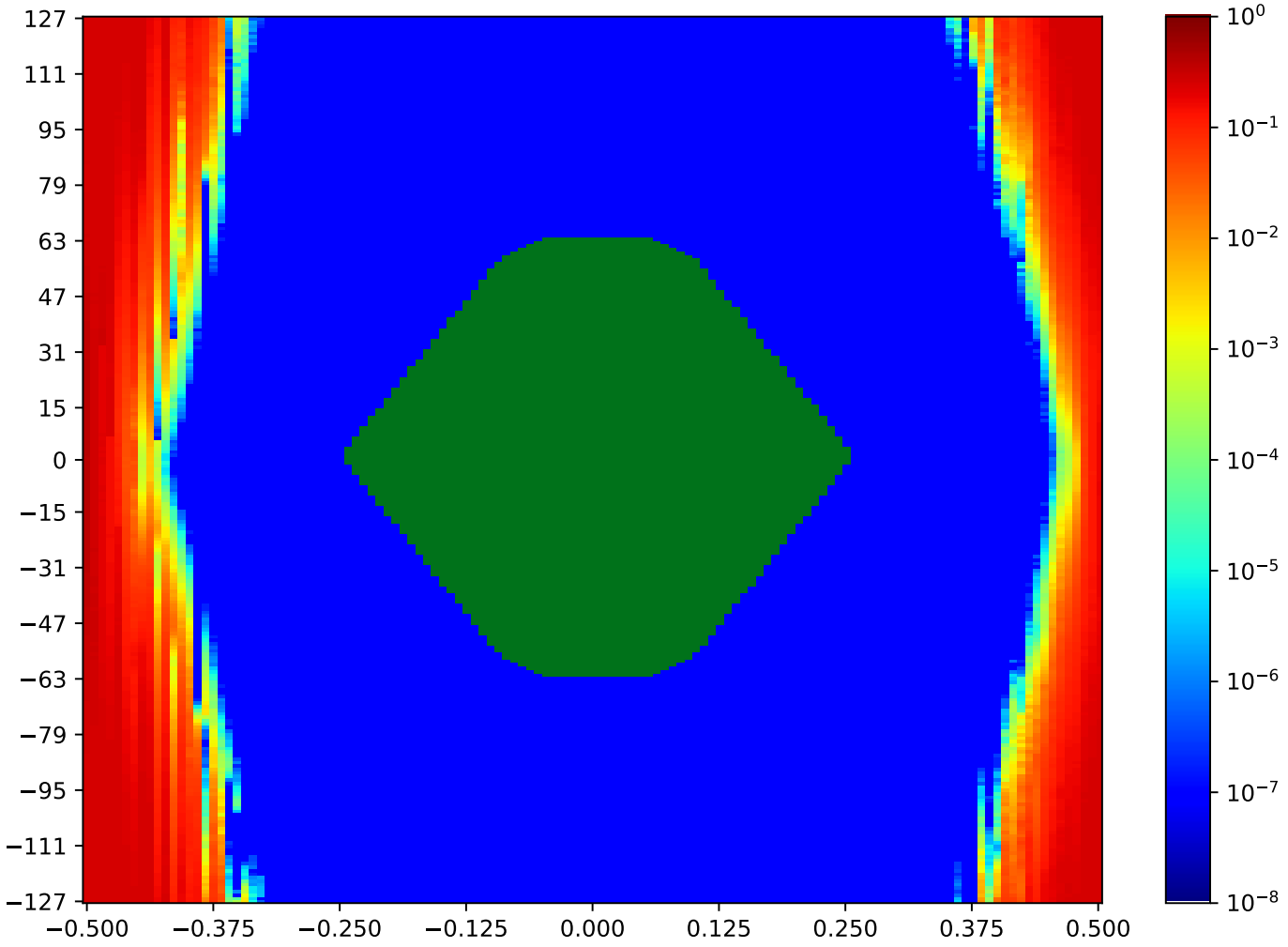


Figure 5.80: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.12 MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Table 5.73: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:49:21		2019-Nov-25 21:50:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25716	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

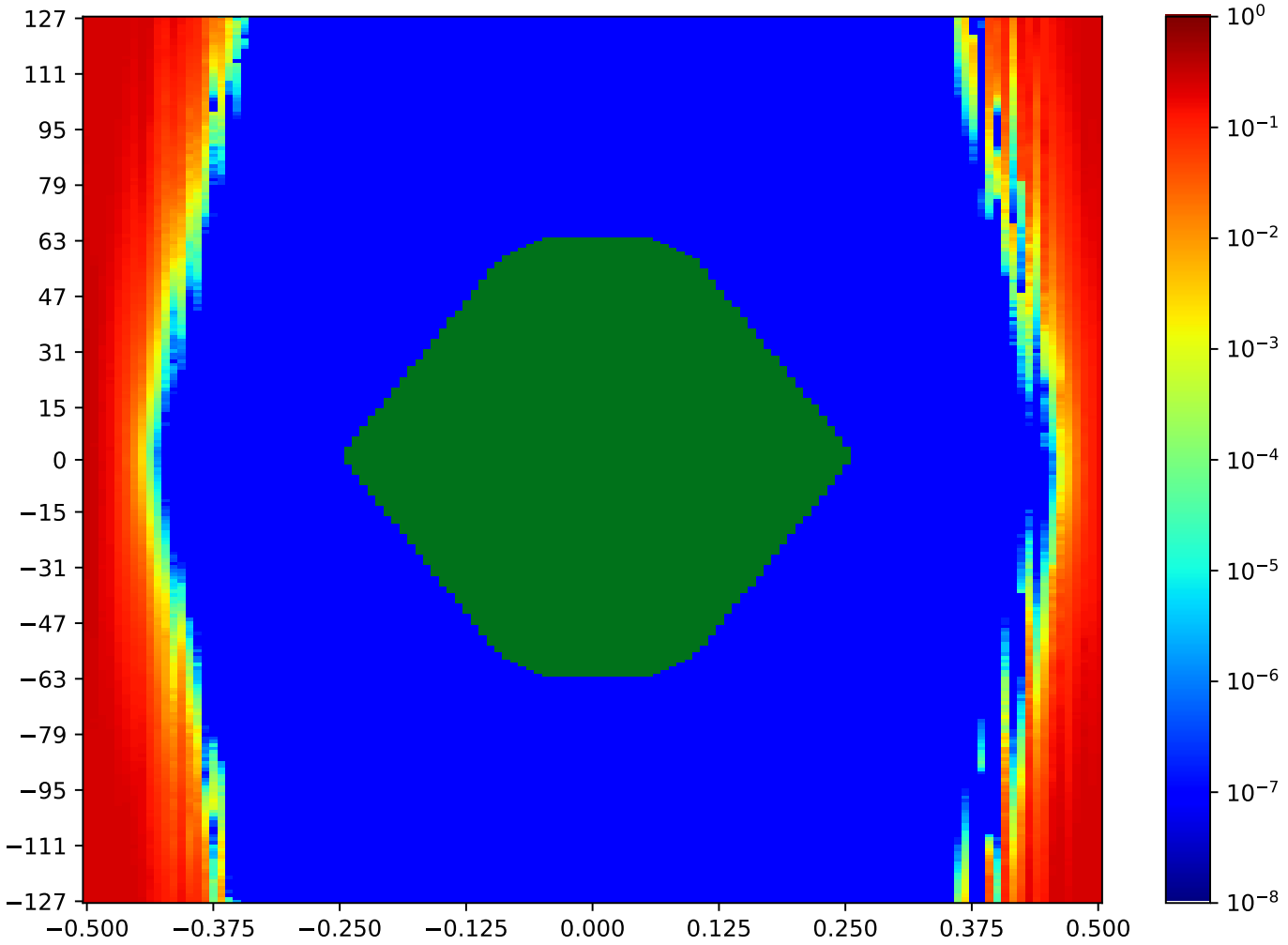


Figure 5.81: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.13 MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Table 5.74: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:50:27		2019-Nov-25 21:51:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26144	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

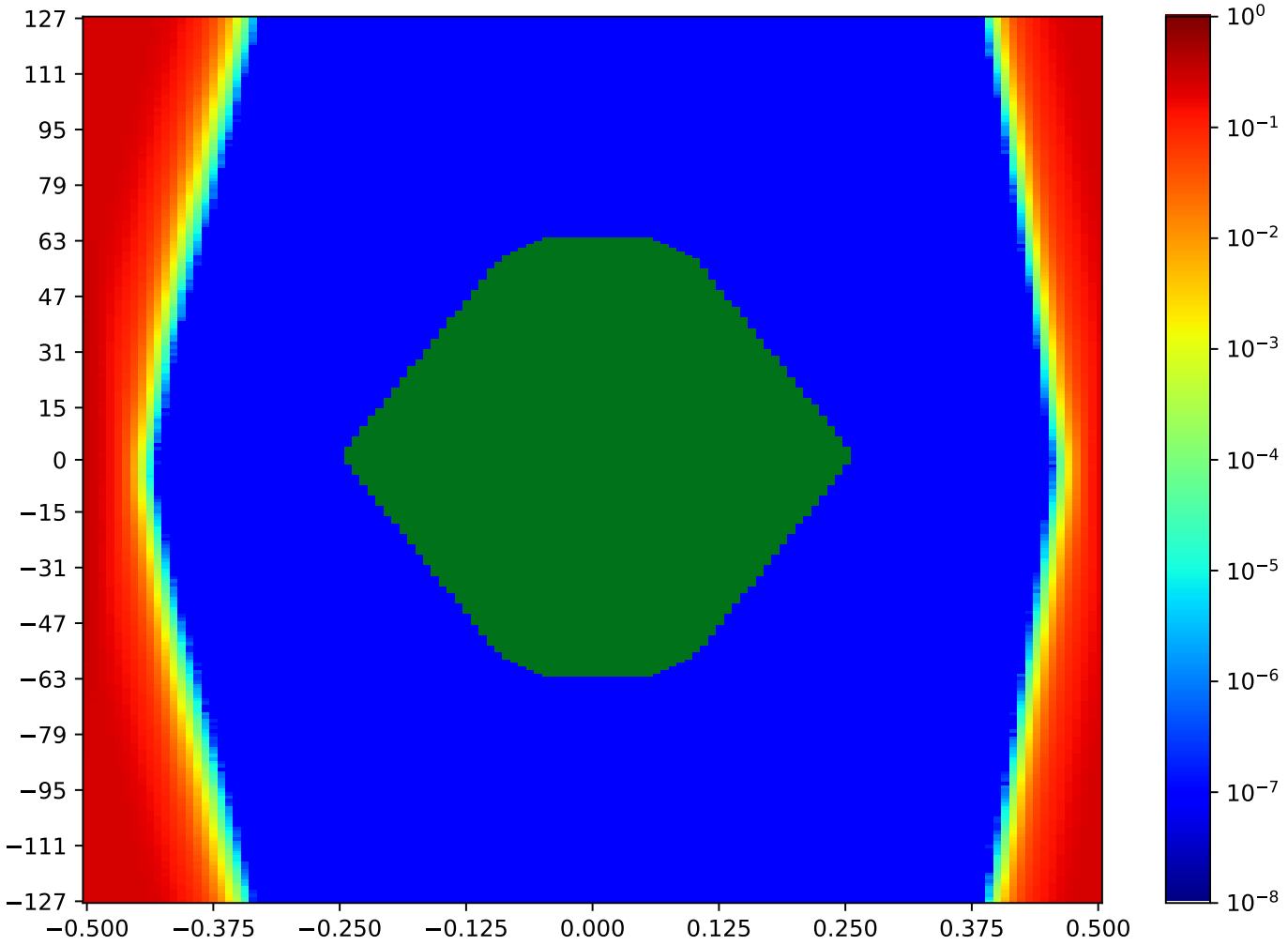


Figure 5.82: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.14 MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Table 5.75: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:51:34		2019-Nov-25 21:52:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	27446	115	89.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

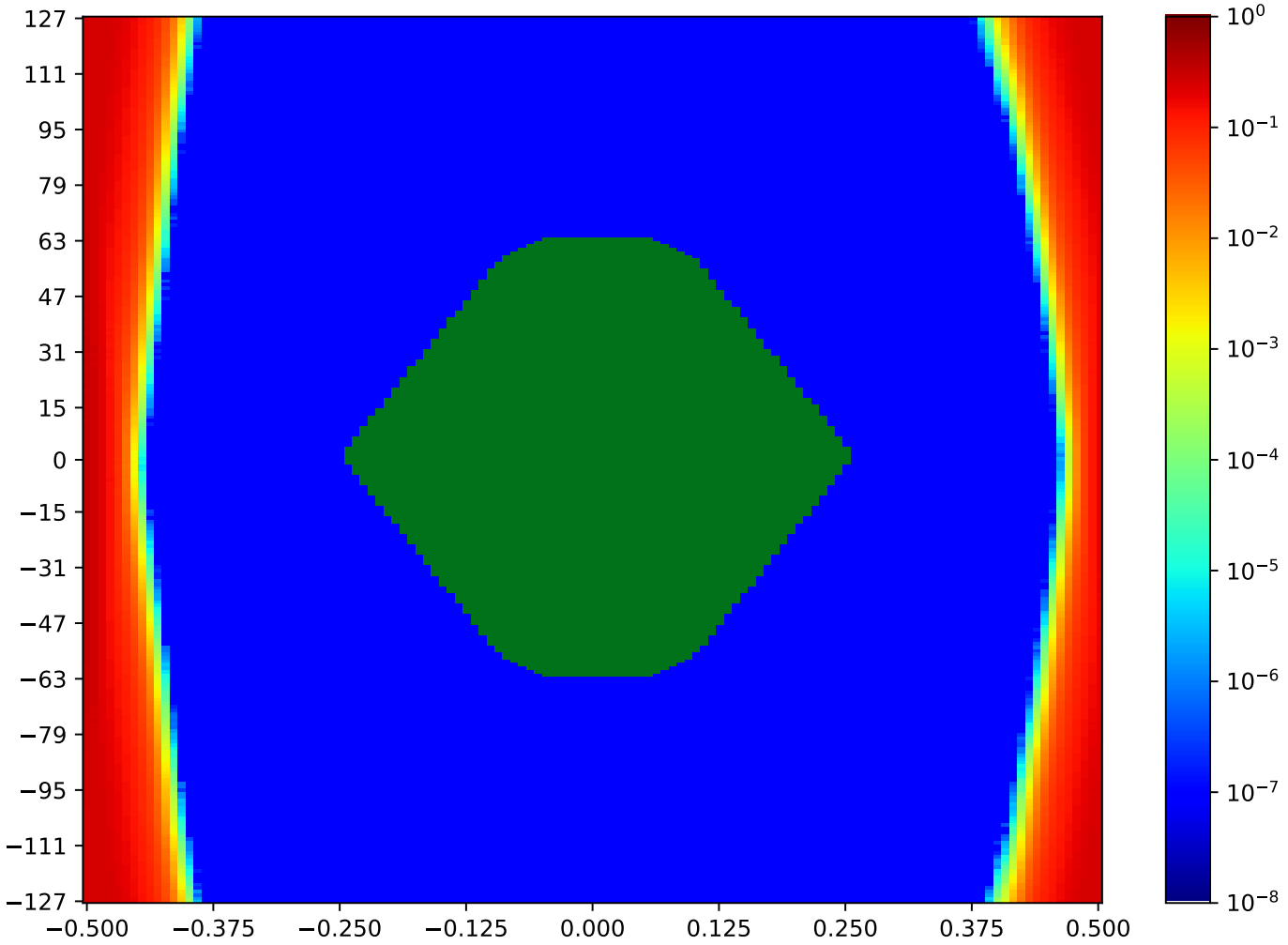


Figure 5.83: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.15 MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Table 5.76: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:52:41		2019-Nov-25 21:53:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26232	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

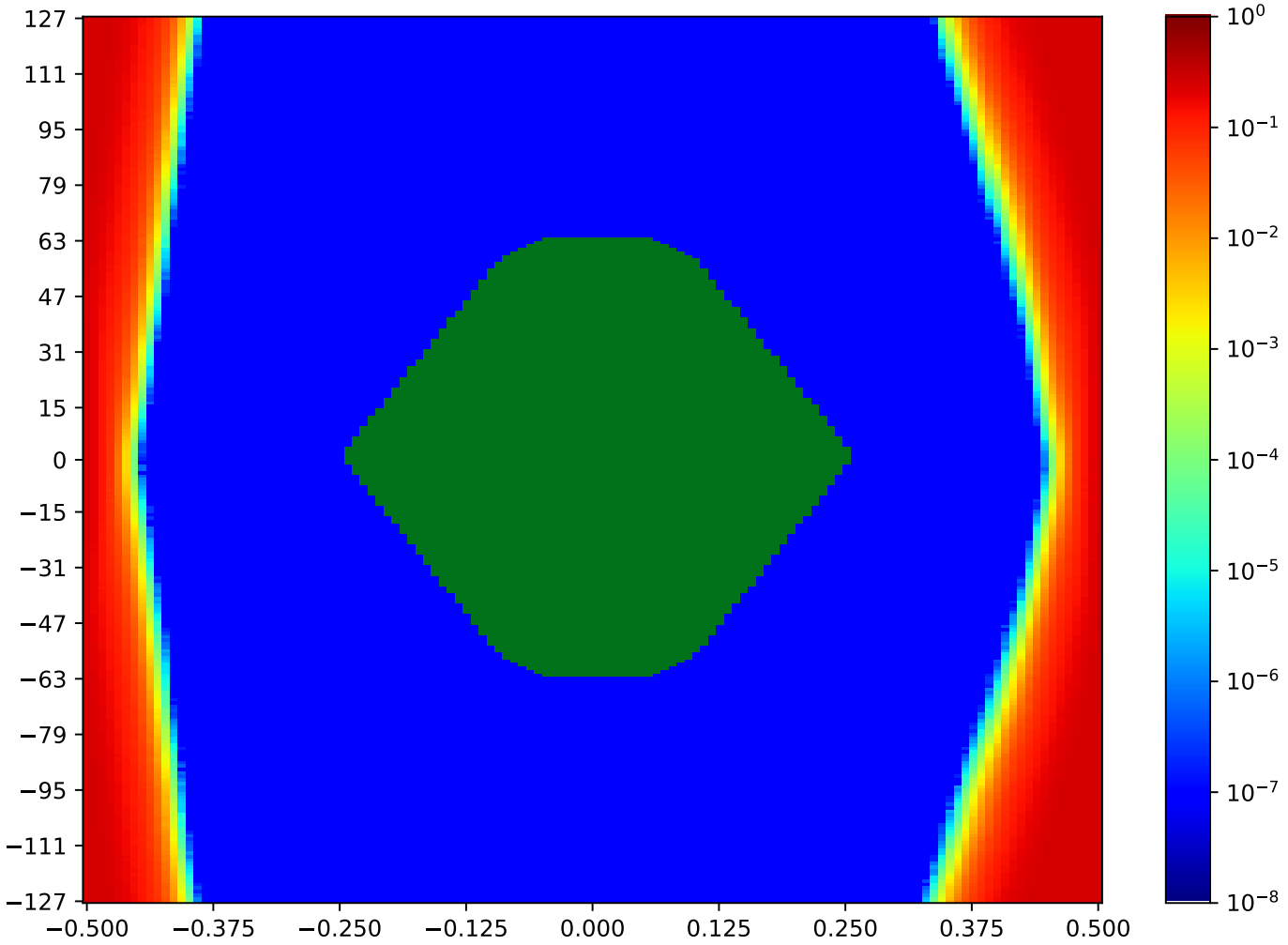


Figure 5.84: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.16 MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Table 5.77: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:53:47		2019-Nov-25 21:54:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25595	114	88.37%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

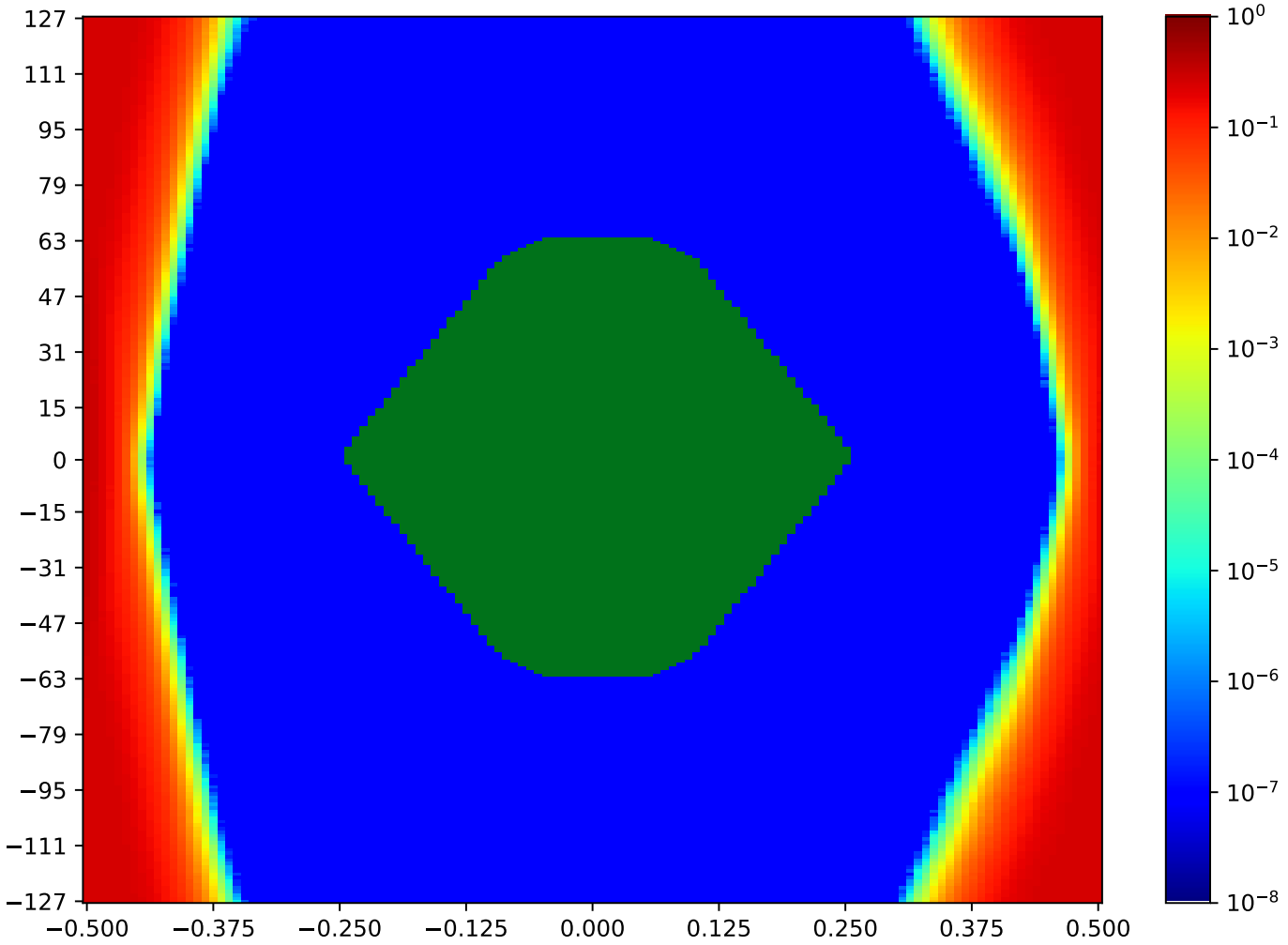


Figure 5.85: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.17 MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Table 5.78: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:54:53		2019-Nov-25 21:55:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26176	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

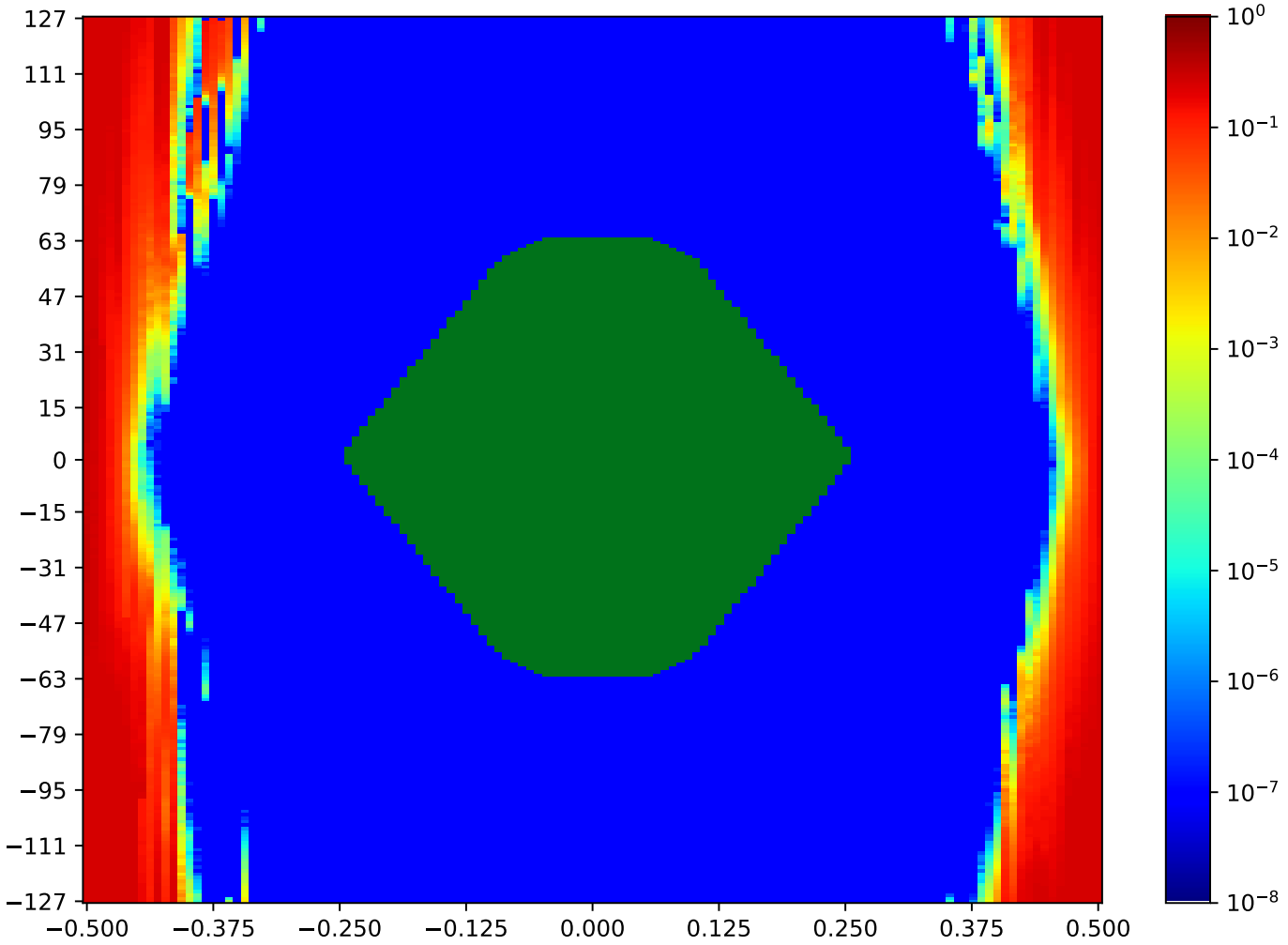


Figure 5.86: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.18 MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Table 5.79: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:55:58		2019-Nov-25 21:57:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25894	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

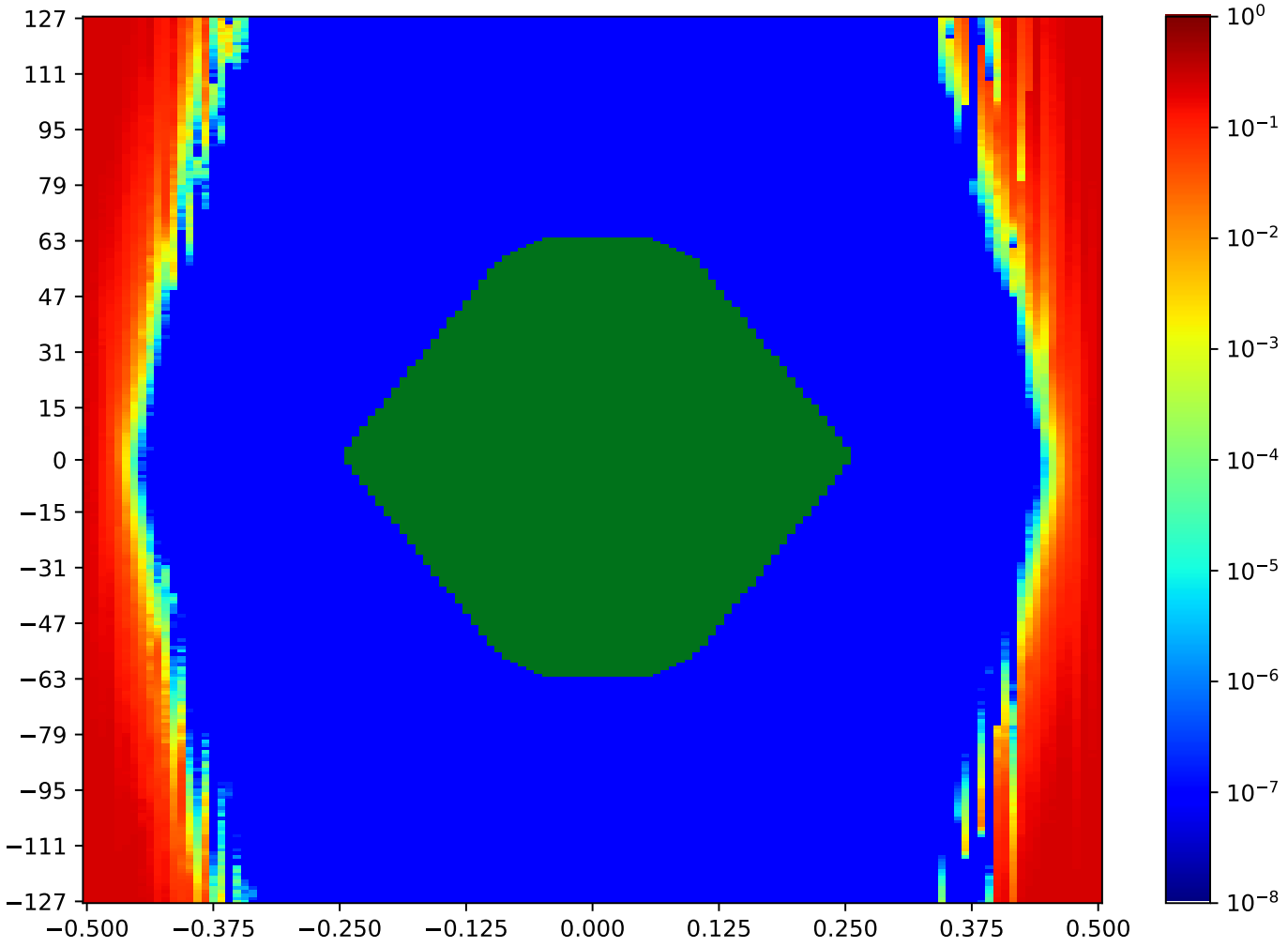


Figure 5.87: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.19 MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Table 5.80: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:57:05		2019-Nov-25 21:58:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25867	114	88.37%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

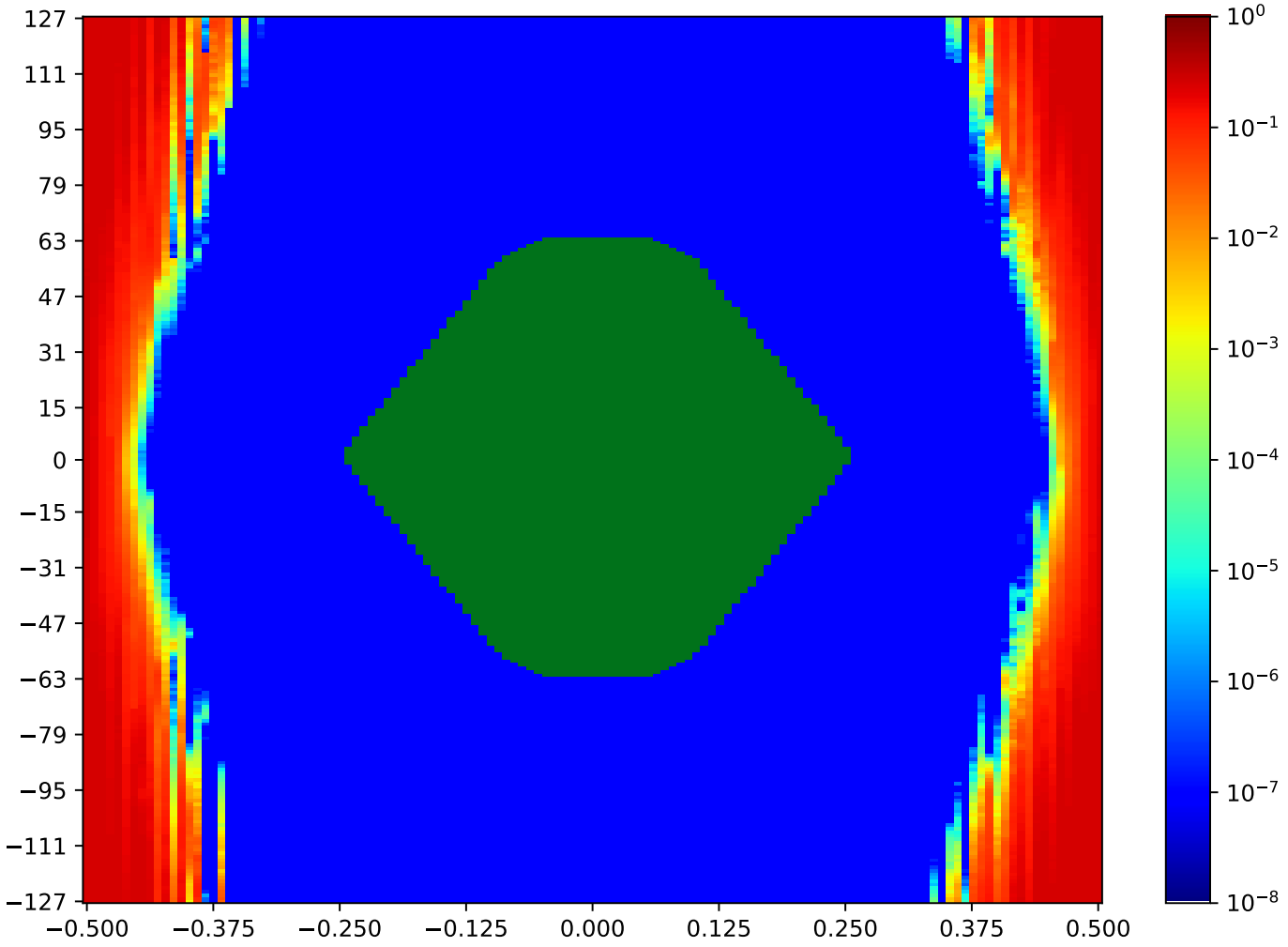


Figure 5.88: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.20 MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Table 5.81: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:58:11		2019-Nov-25 21:59:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26290	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

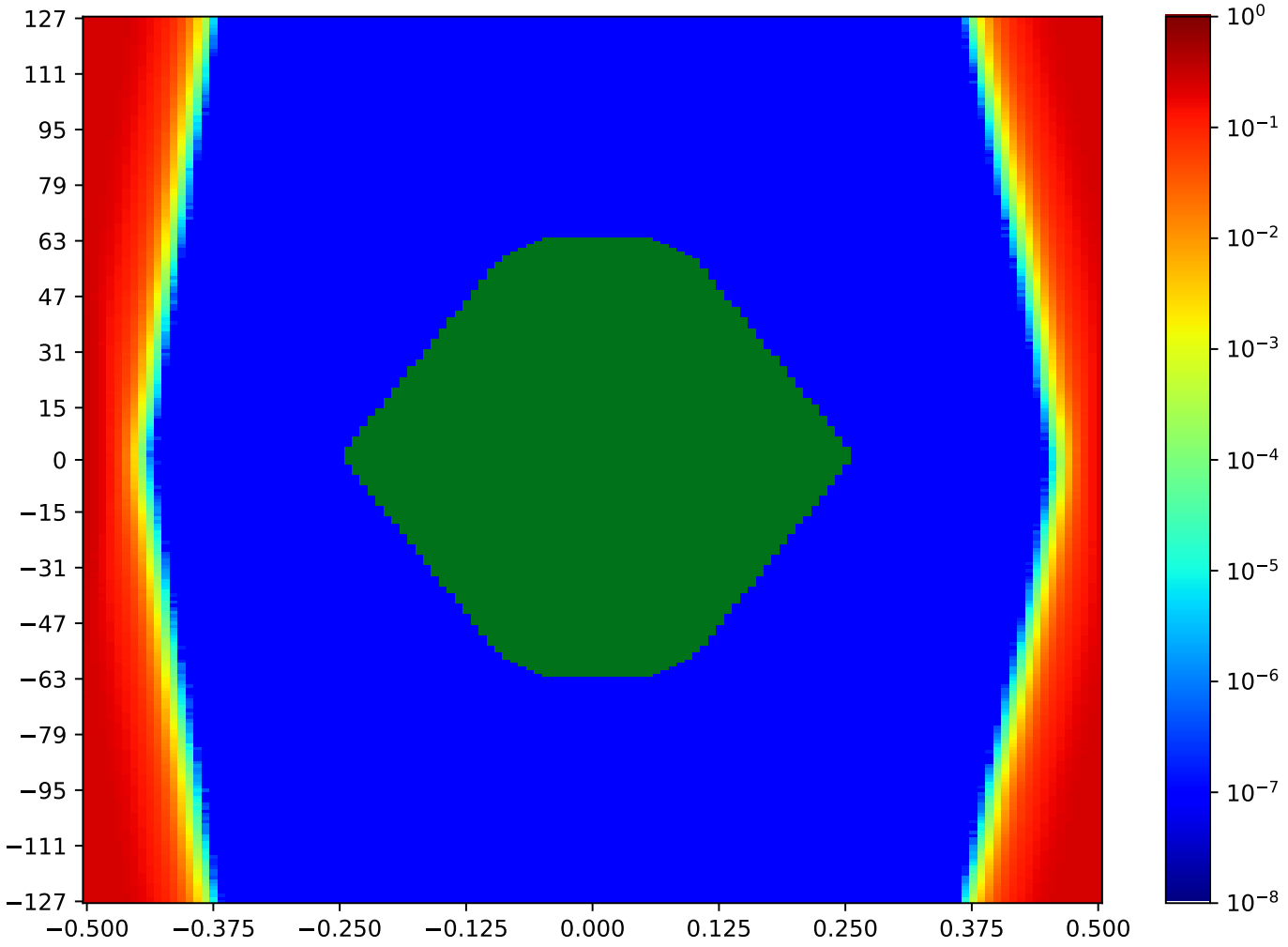


Figure 5.89: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.21 MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Table 5.82: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 21:59:17		2019-Nov-25 22:00:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26152	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

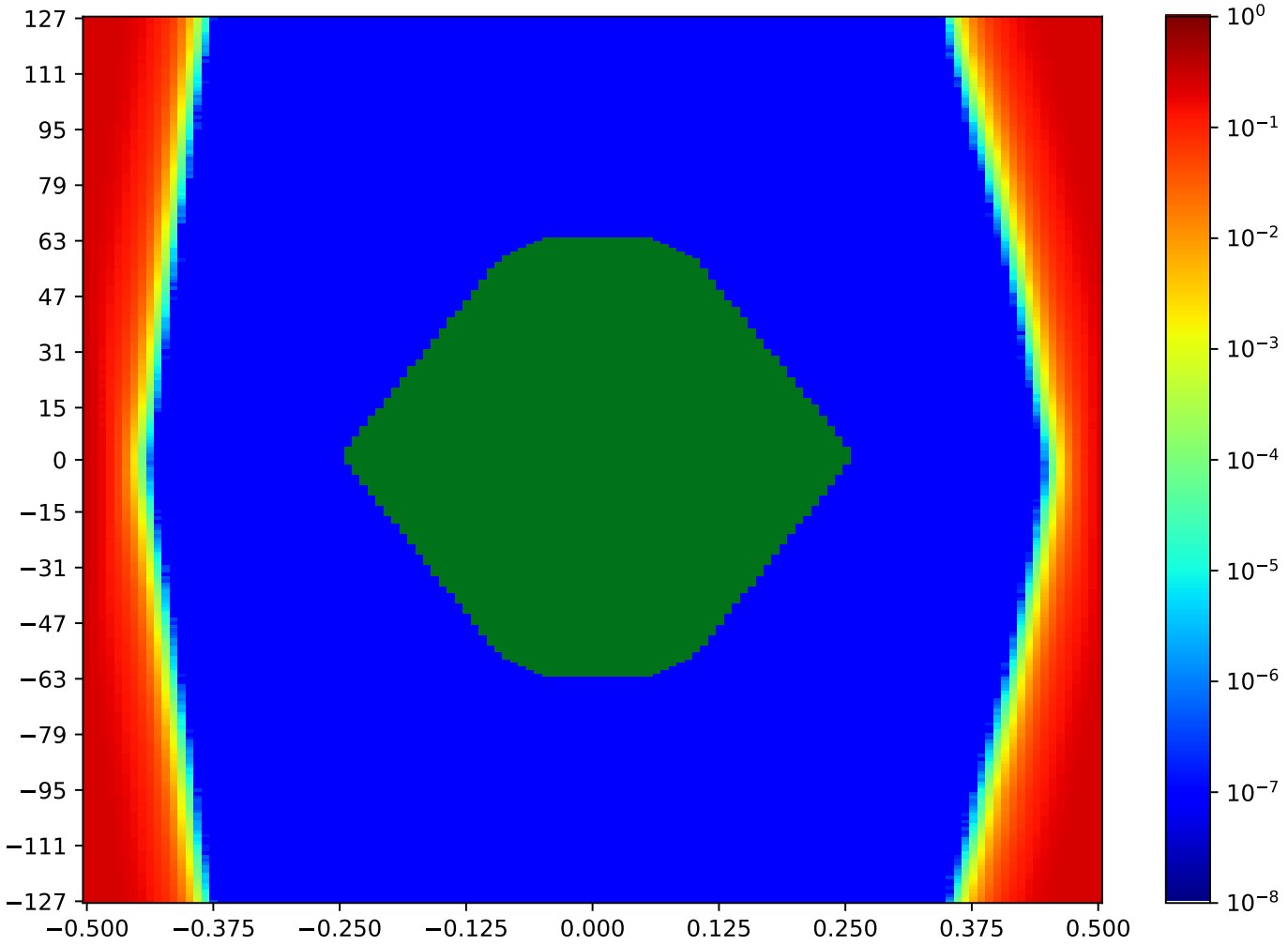


Figure 5.90: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.22 MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Table 5.83: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:00:24		2019-Nov-25 22:01:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24992	113	87.60%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

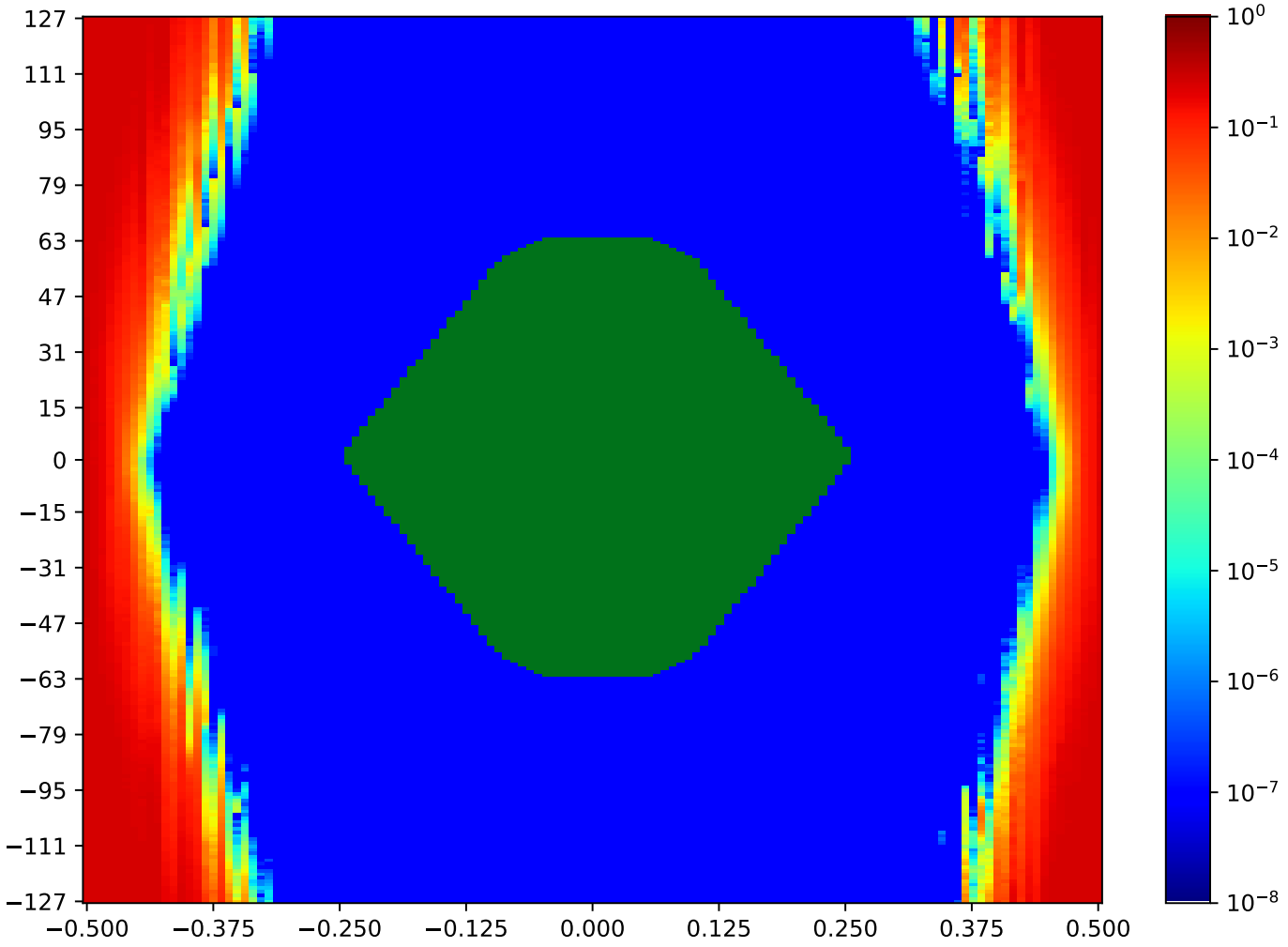


Figure 5.91: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.23 MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Table 5.84: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:01:30		2019-Nov-25 22:02:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26965	114	88.37%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

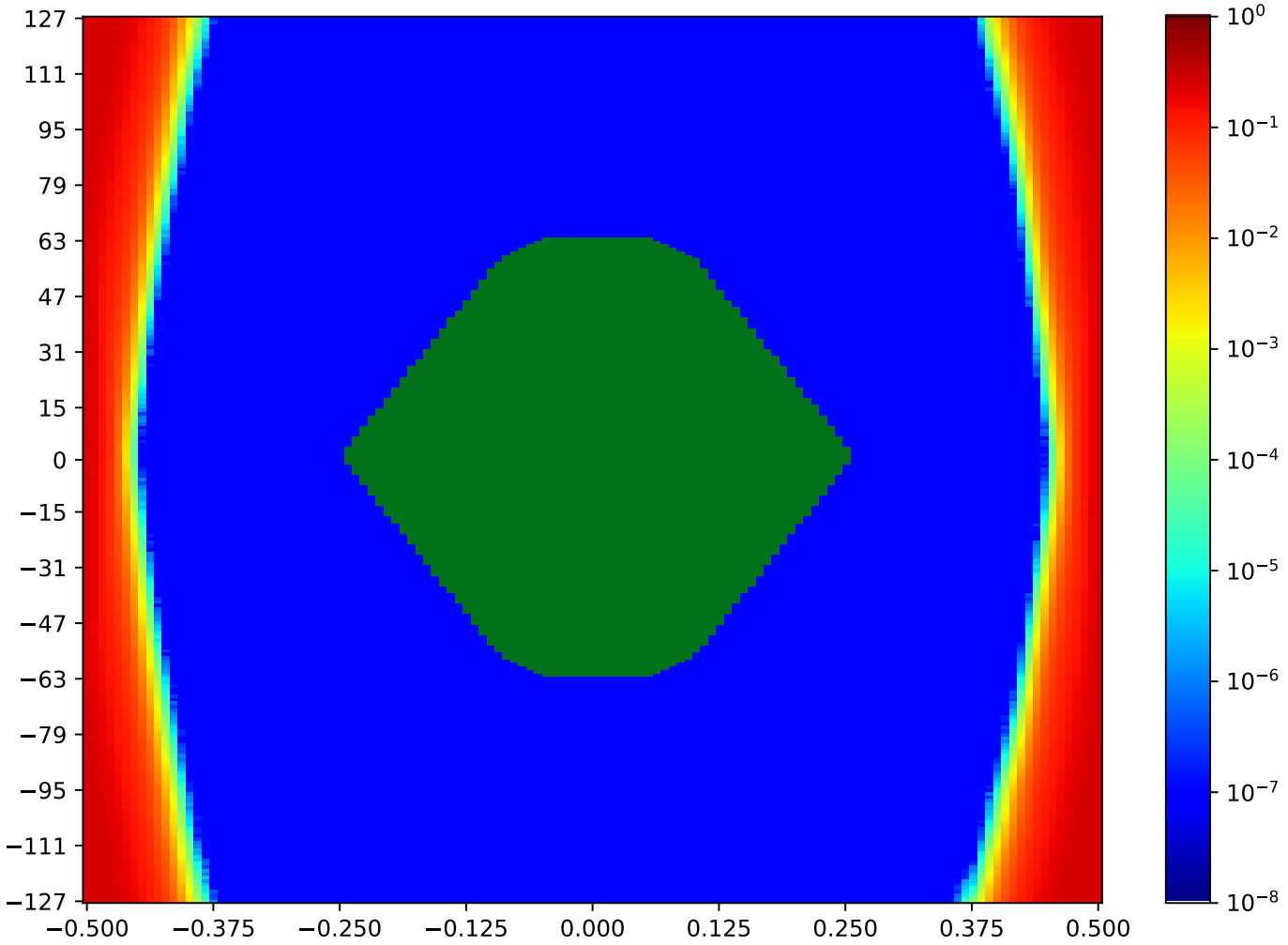


Figure 5.92: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.24 MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Table 5.85: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:02:37		2019-Nov-25 22:03:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24754	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

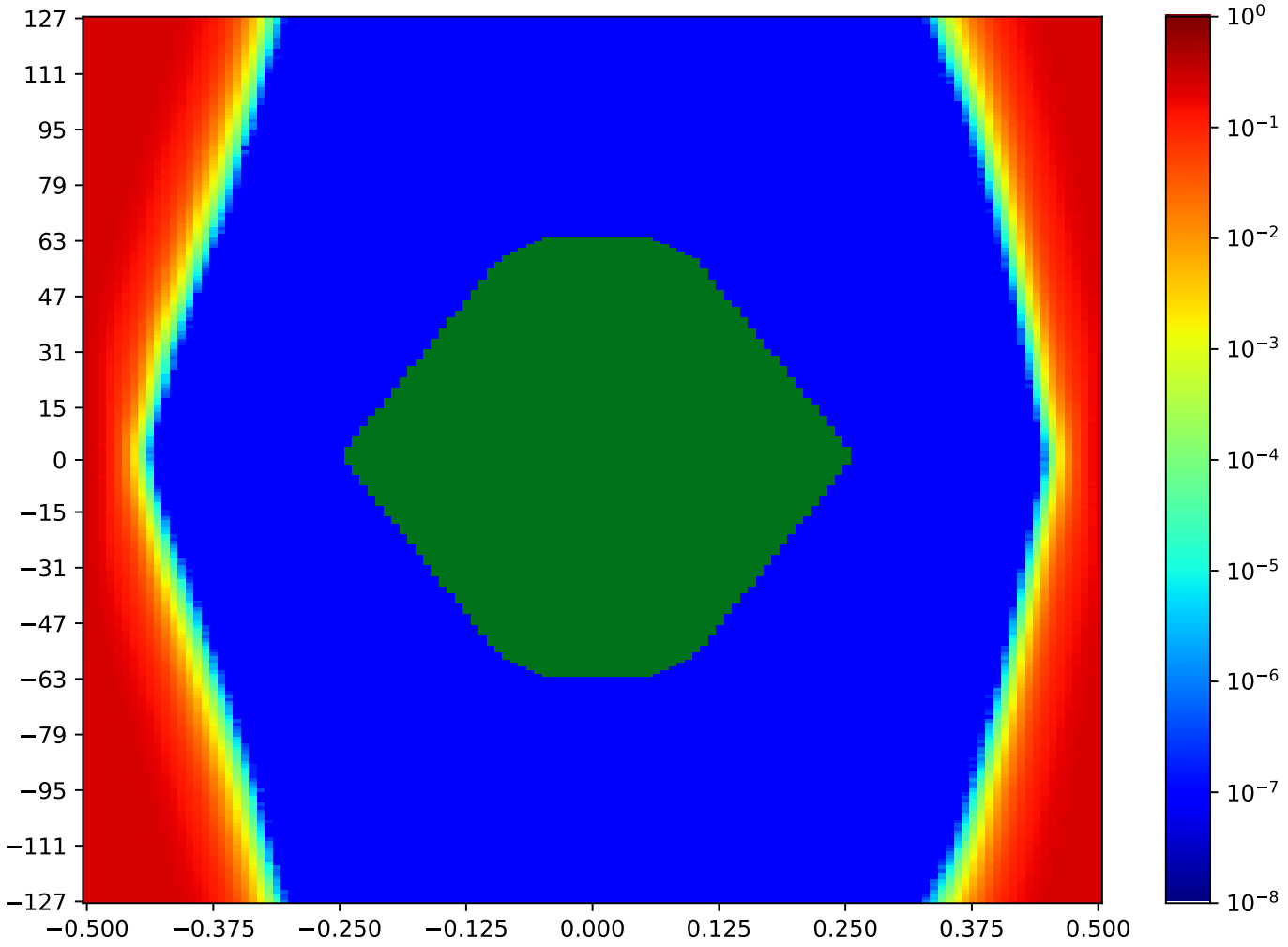


Figure 5.93: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.25 MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Table 5.86: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:03:42		2019-Nov-25 22:04:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26513	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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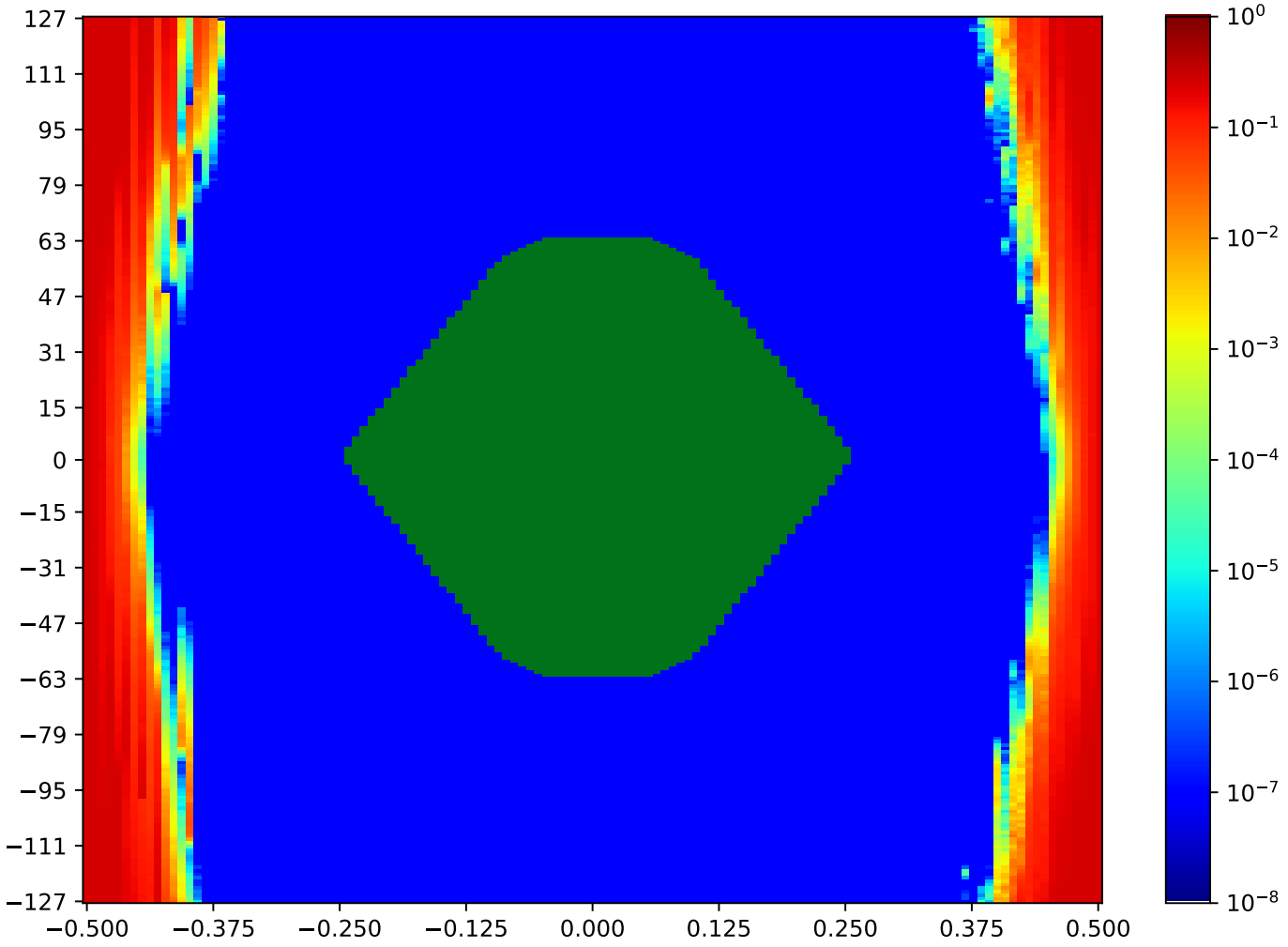


Figure 5.94: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.26 MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Table 5.87: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:04:49		2019-Nov-25 22:05:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	26503	114	88.37%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

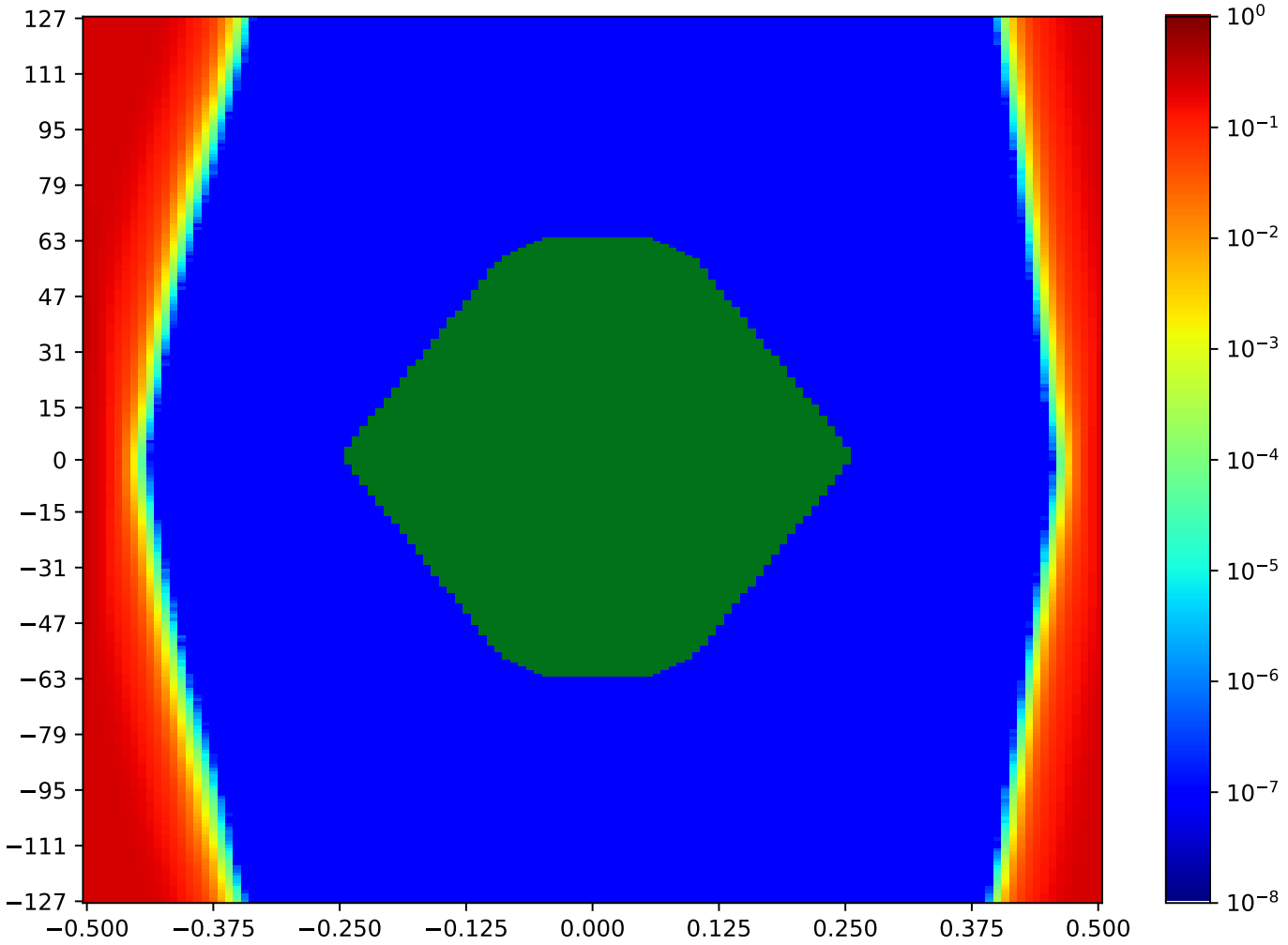


Figure 5.95: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.27 MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Table 5.88: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:05:56		2019-Nov-25 22:07:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25937	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

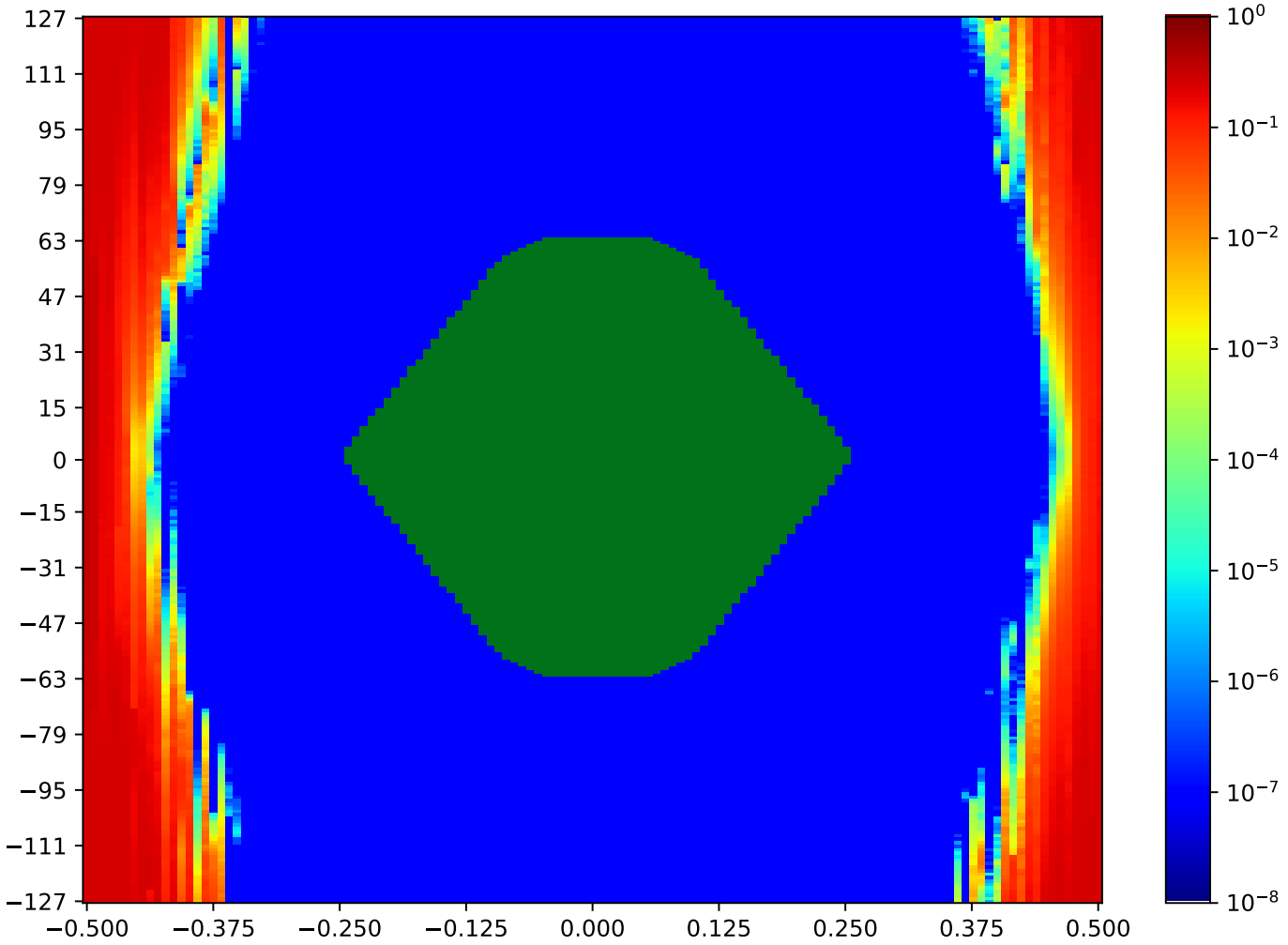


Figure 5.96: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.8.28 MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Table 5.89: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-25 22:07:03		2019-Nov-25 22:08:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25914	112	86.82%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

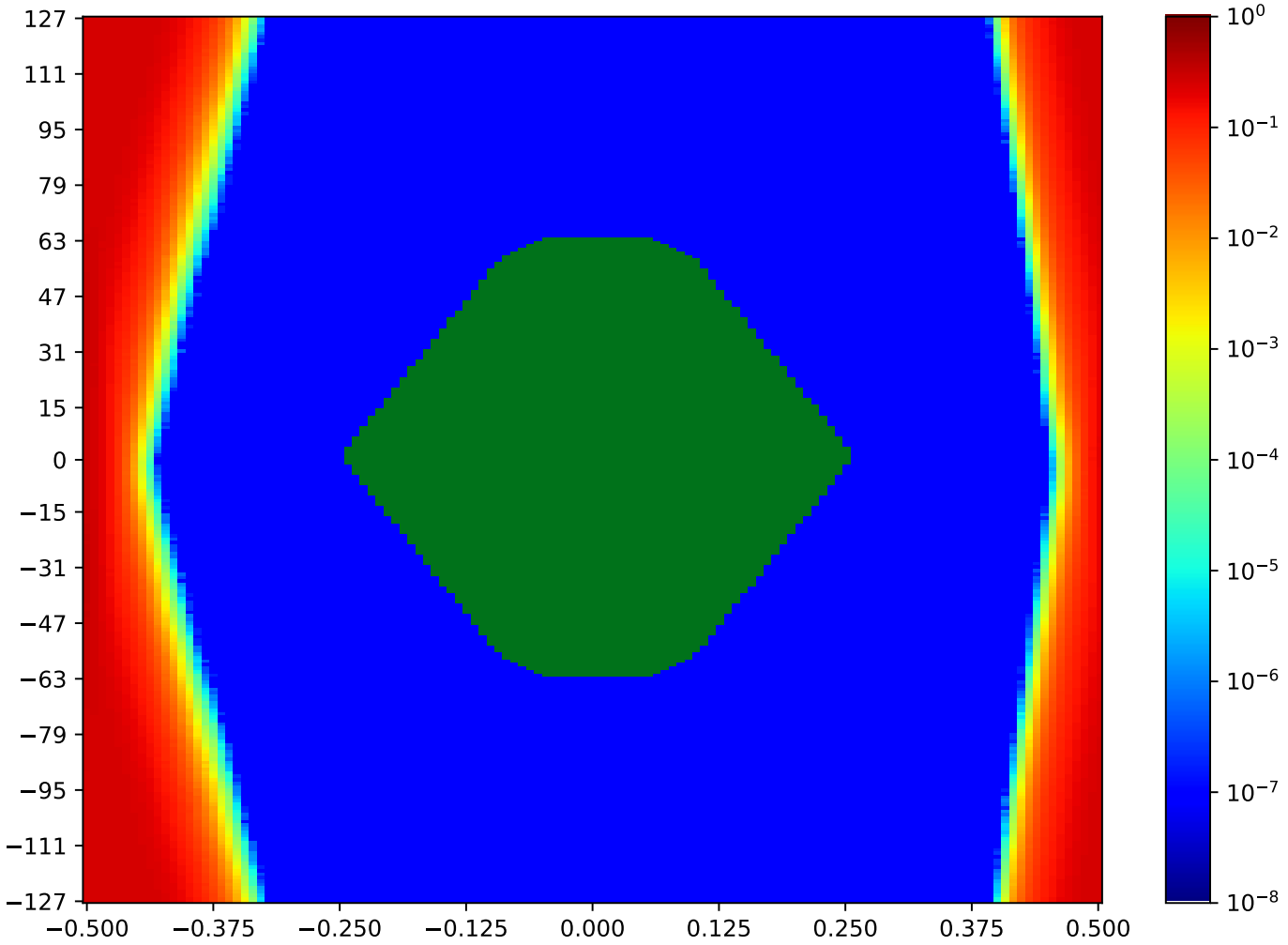


Figure 5.97: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9 MSP_C TRP On board links

A cross-reference to Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.127.

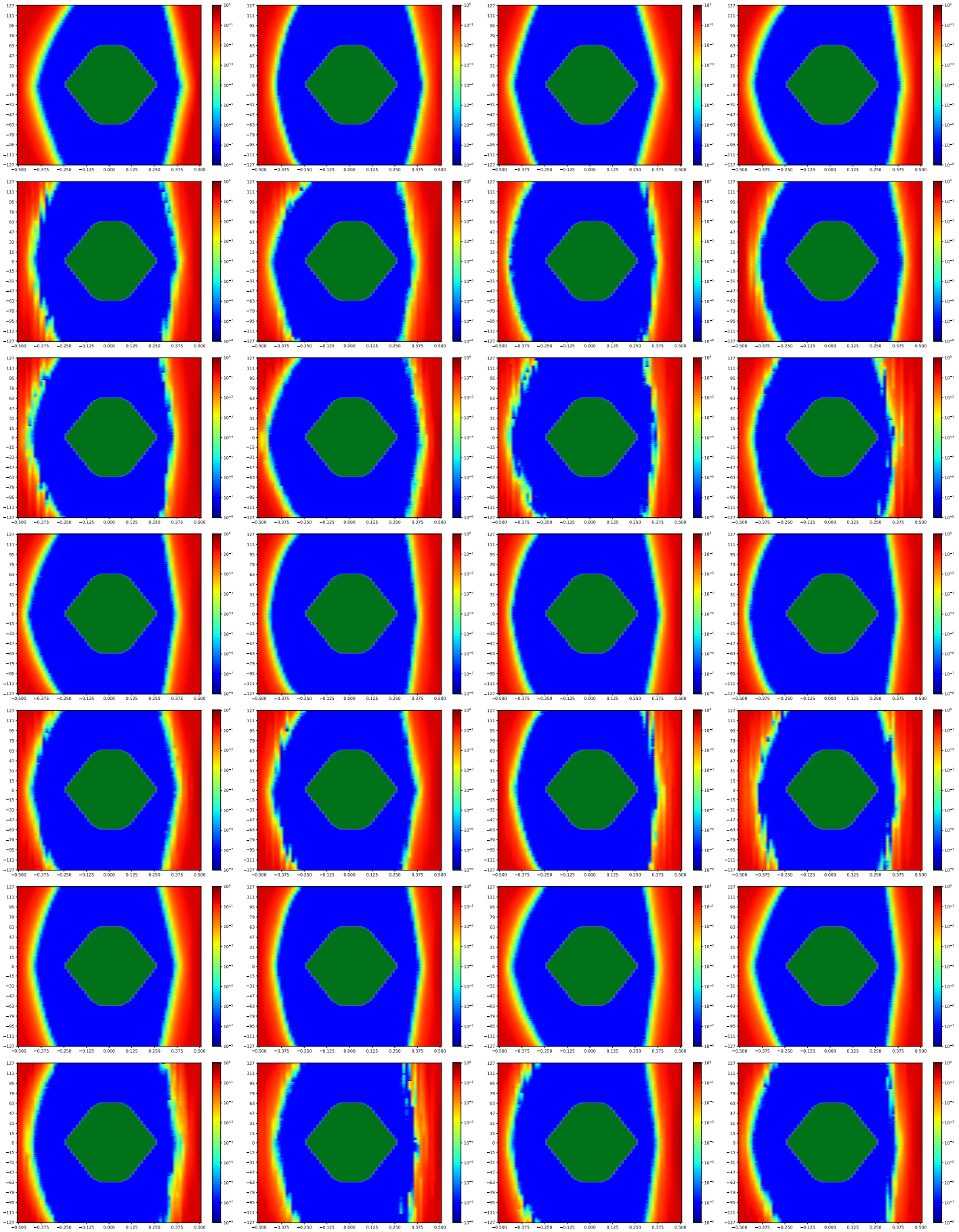


Figure 5.98: MSP_C TRP On board links

5.9.1 MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Table 5.90: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:08:09		2019-Nov-25 22:08:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10547	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

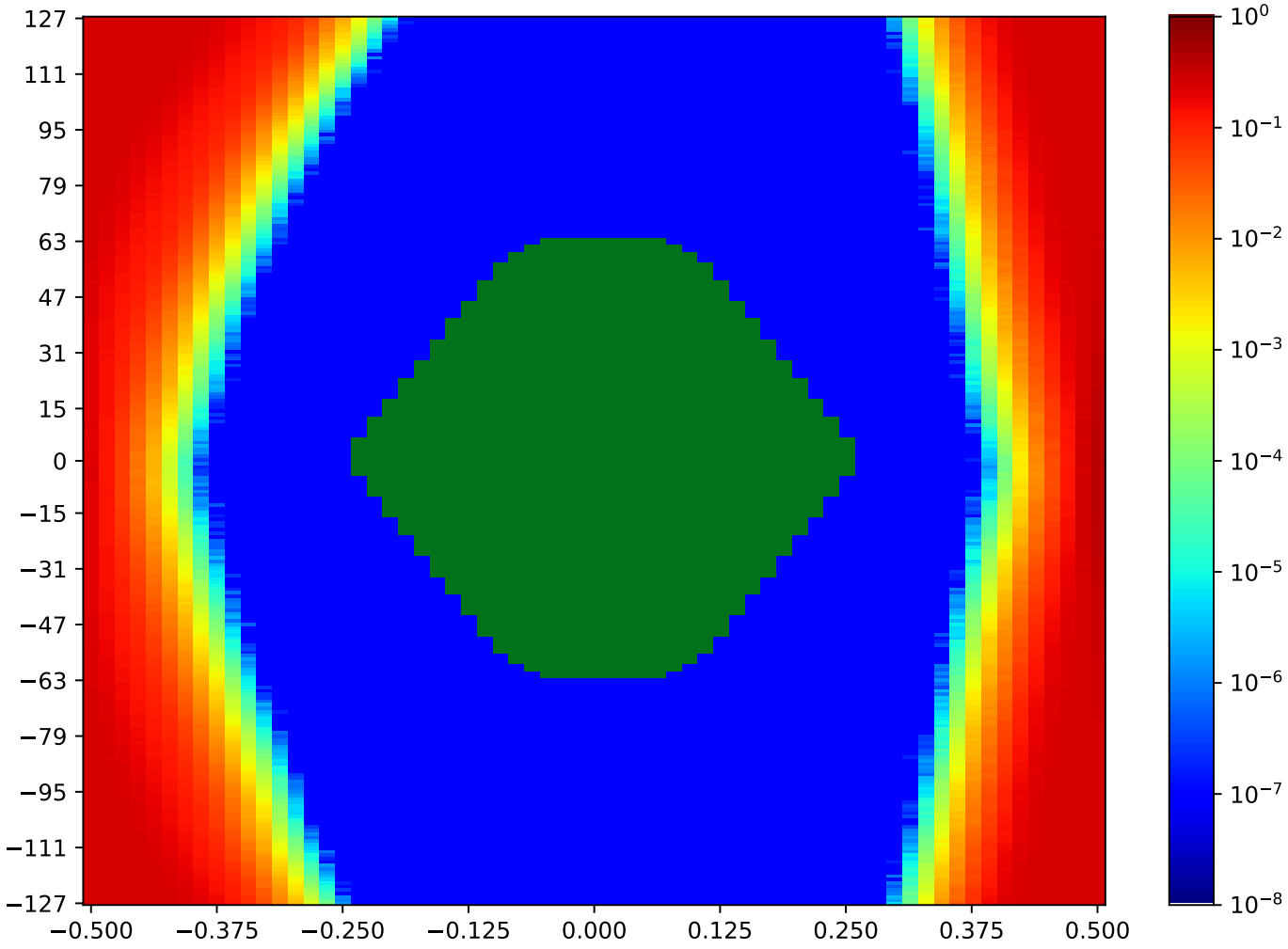


Figure 5.99: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.2 MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Table 5.91: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:08:42		2019-Nov-25 22:09:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11322	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

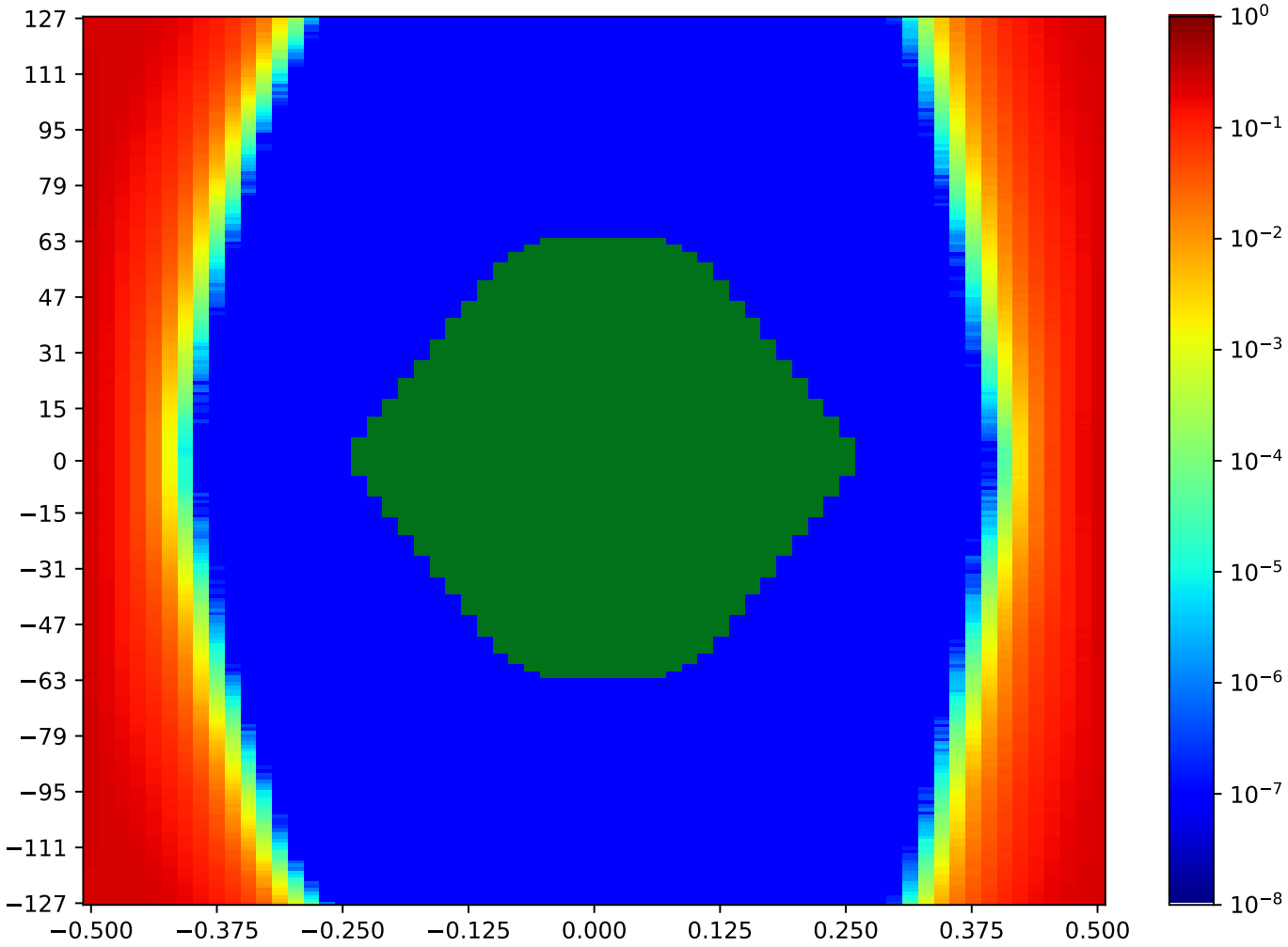


Figure 5.100: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.3 MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Table 5.92: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:09:15		2019-Nov-25 22:09:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10593	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

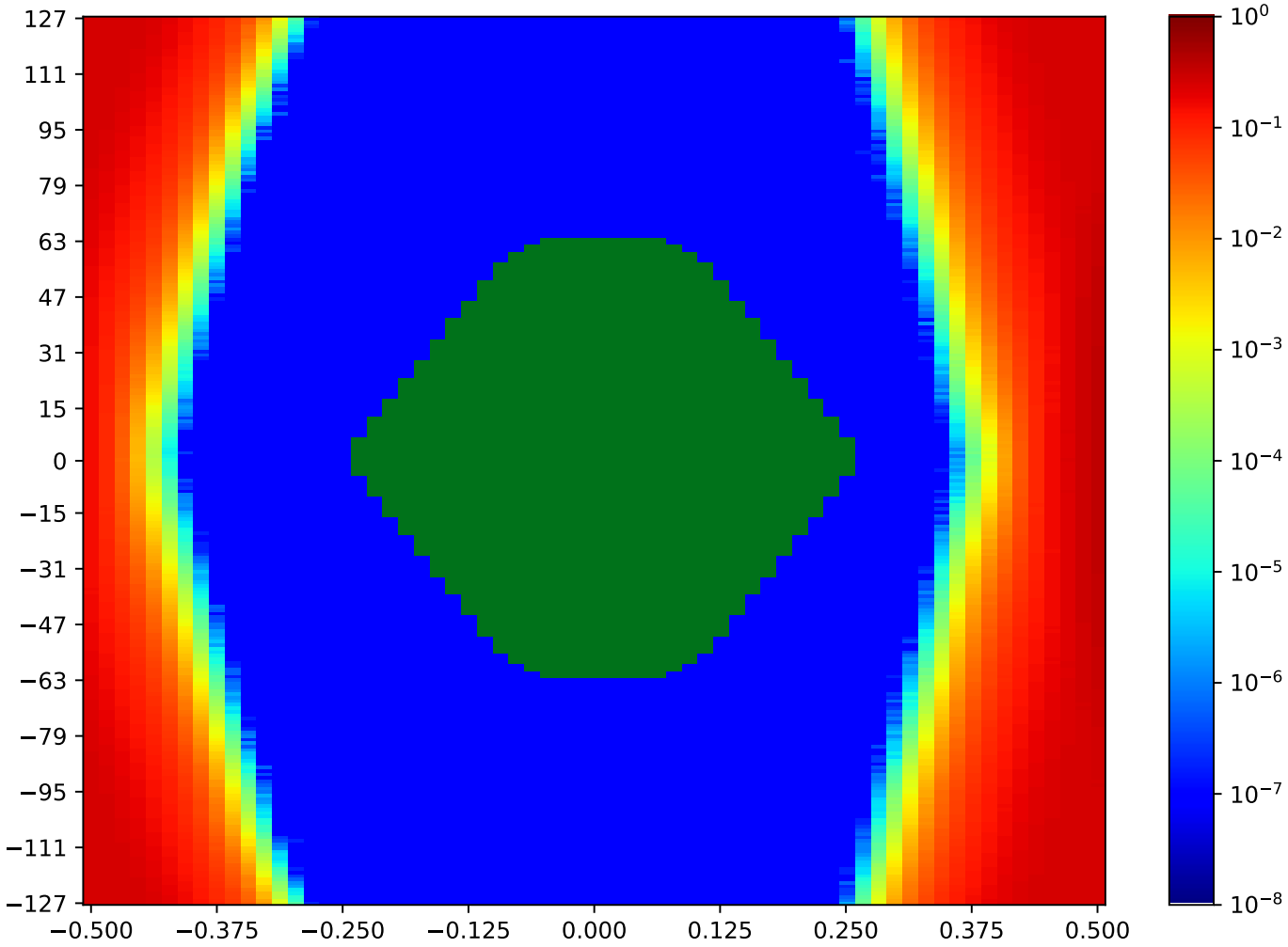


Figure 5.101: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.4 MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Table 5.93: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:09:47		2019-Nov-25 22:10:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11127	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

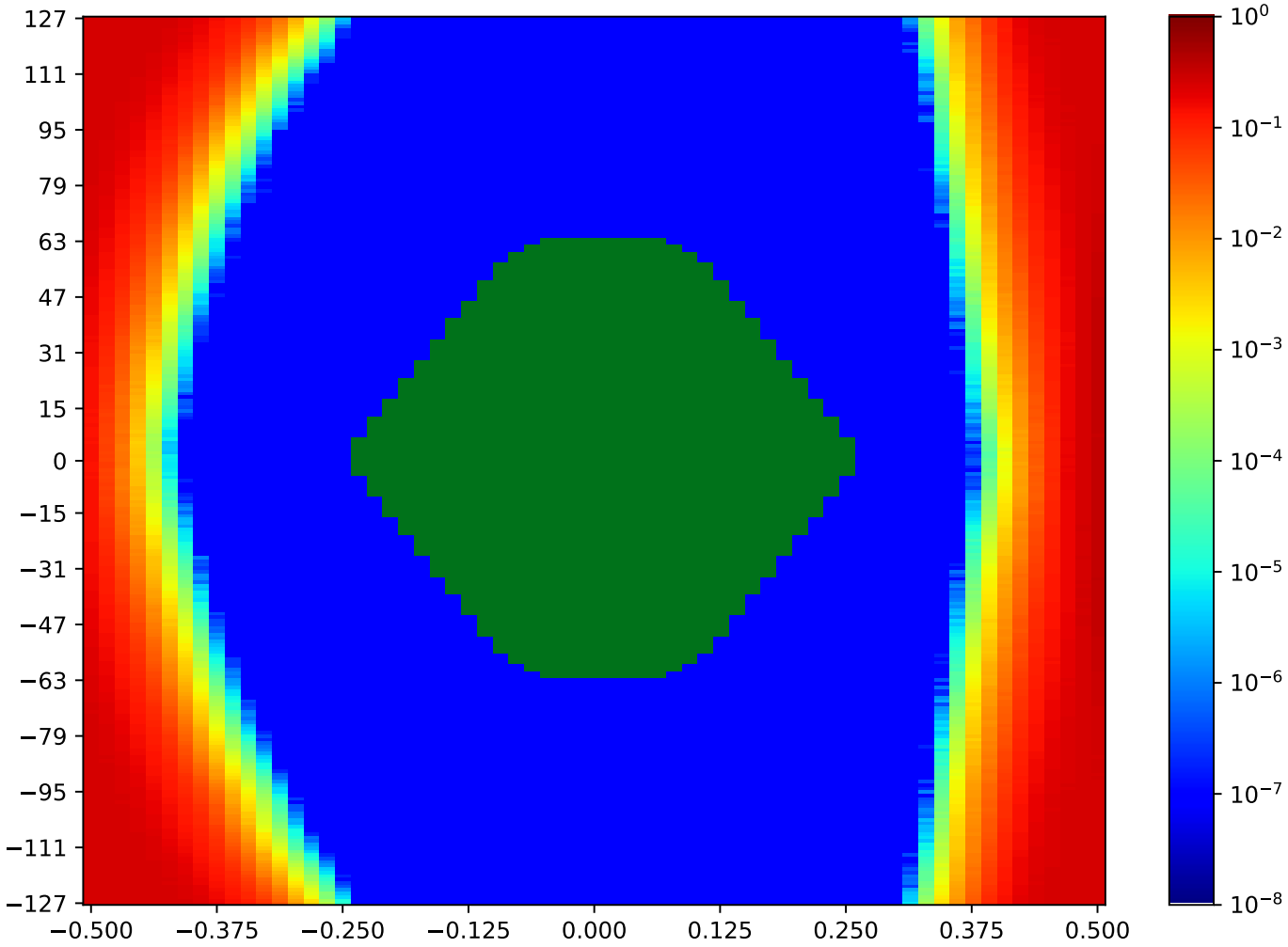


Figure 5.102: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.5 MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Table 5.94: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:10:21		2019-Nov-25 22:10:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10864	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

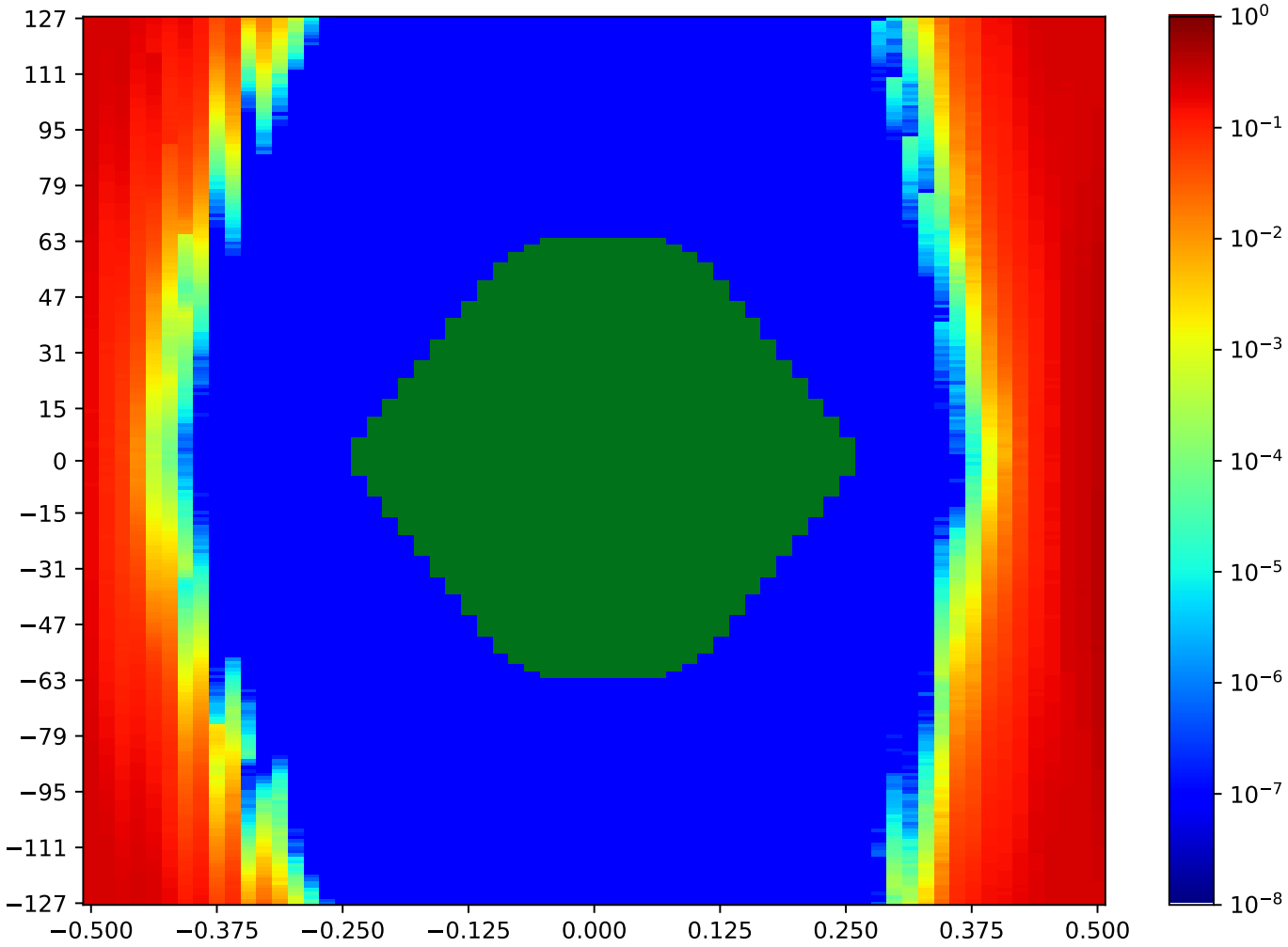


Figure 5.103: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.6 MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Table 5.95: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:10:53		2019-Nov-25 22:11:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10576	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

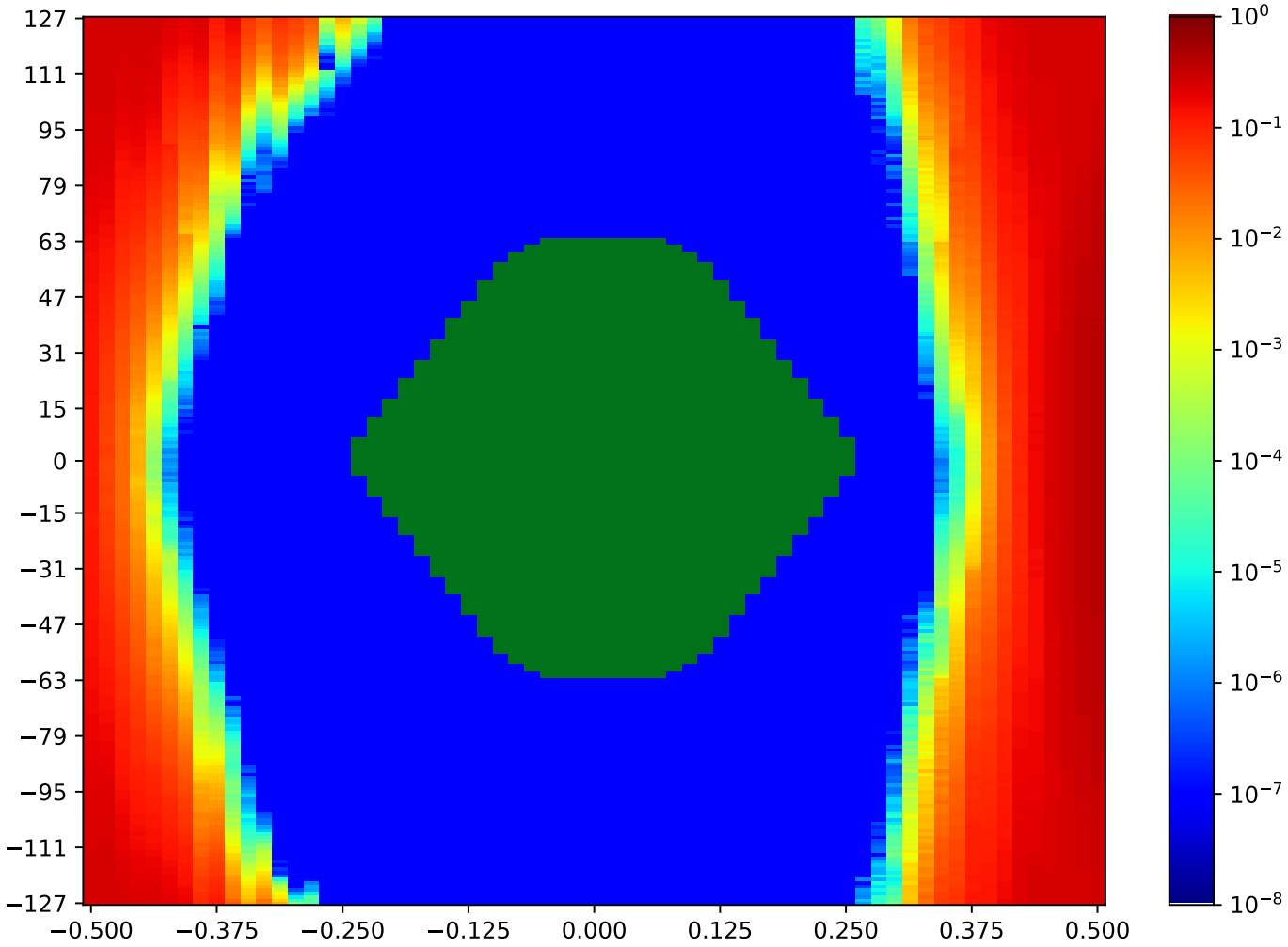


Figure 5.104: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.7 MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Table 5.96: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:11:26		2019-Nov-25 22:11:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11417	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

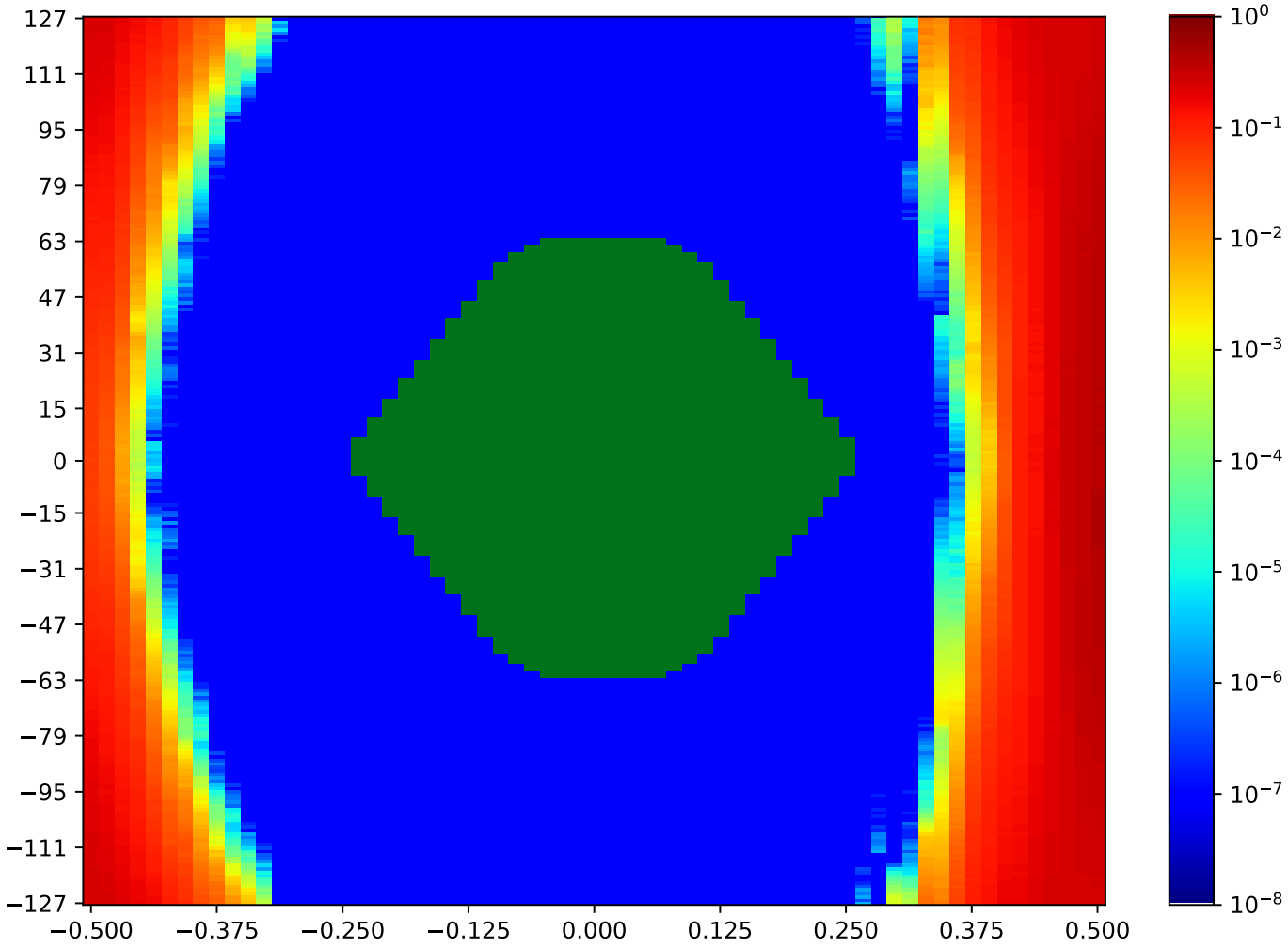


Figure 5.105: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.8 MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Table 5.97: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:11:59		2019-Nov-25 22:12:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11136	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

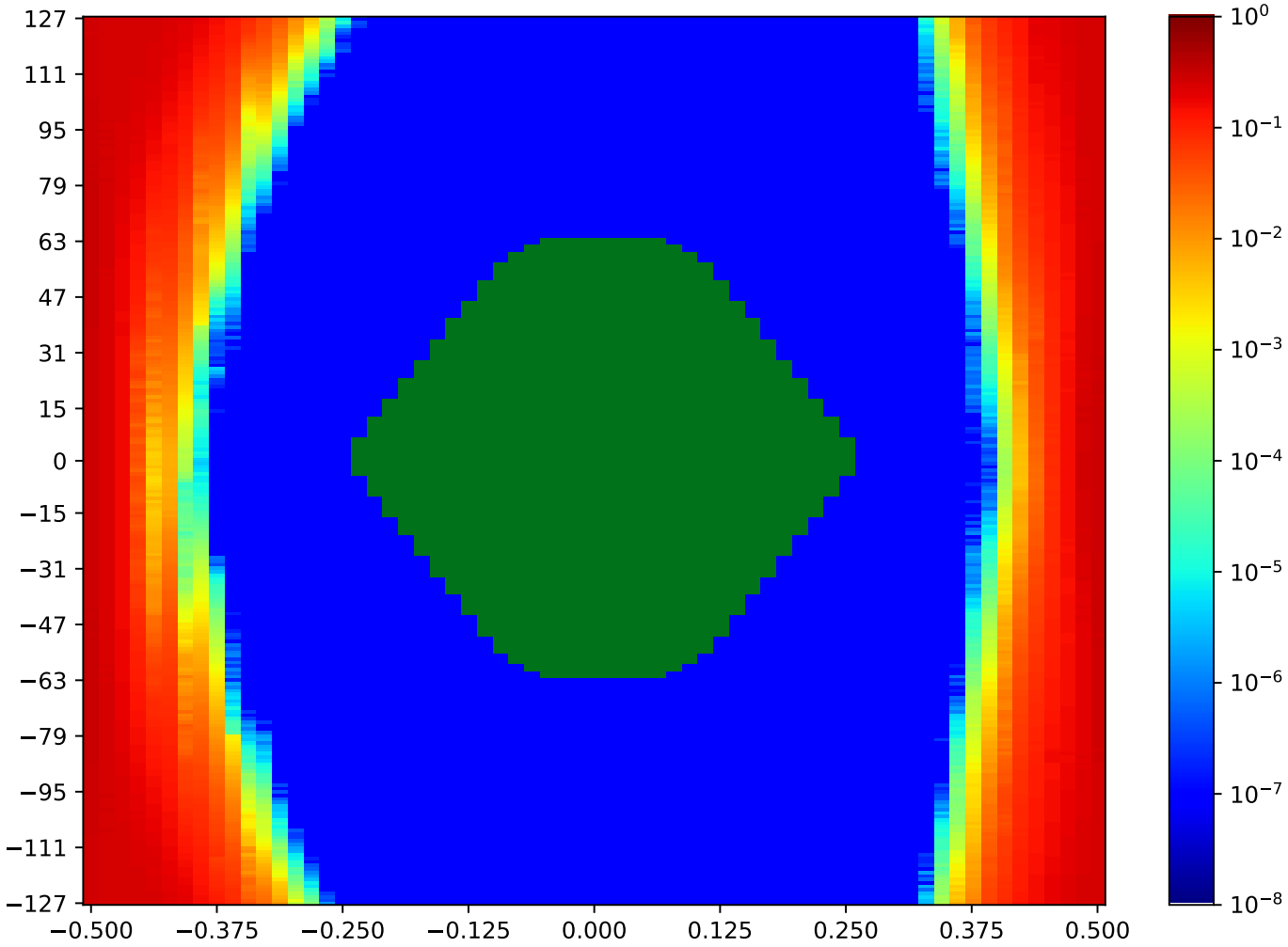


Figure 5.106: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.9 MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Table 5.98: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:12:32		2019-Nov-25 22:13:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10804	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

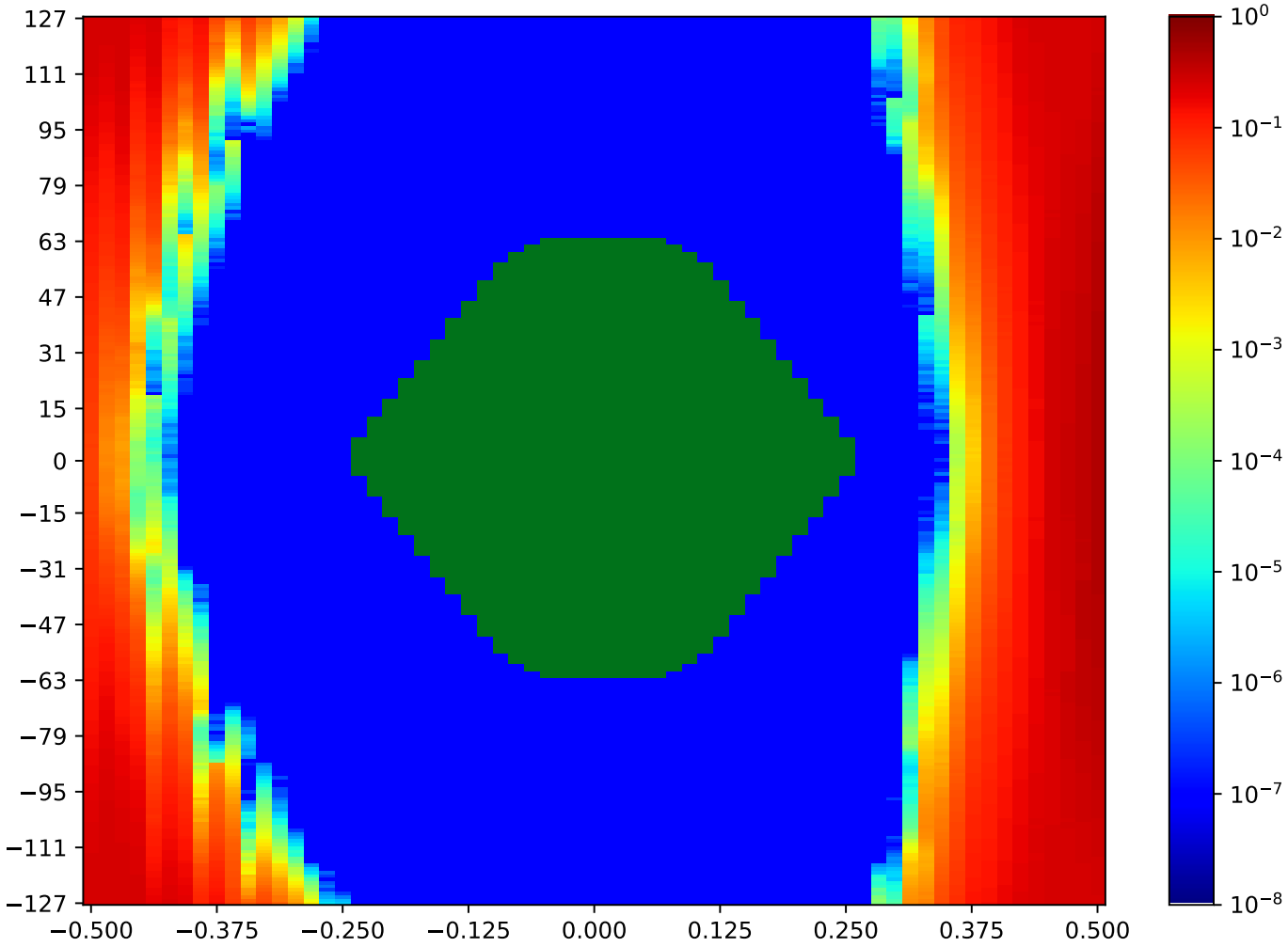


Figure 5.107: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.10 MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Table 5.99: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:13:05		2019-Nov-25 22:13:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11525	52	80.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

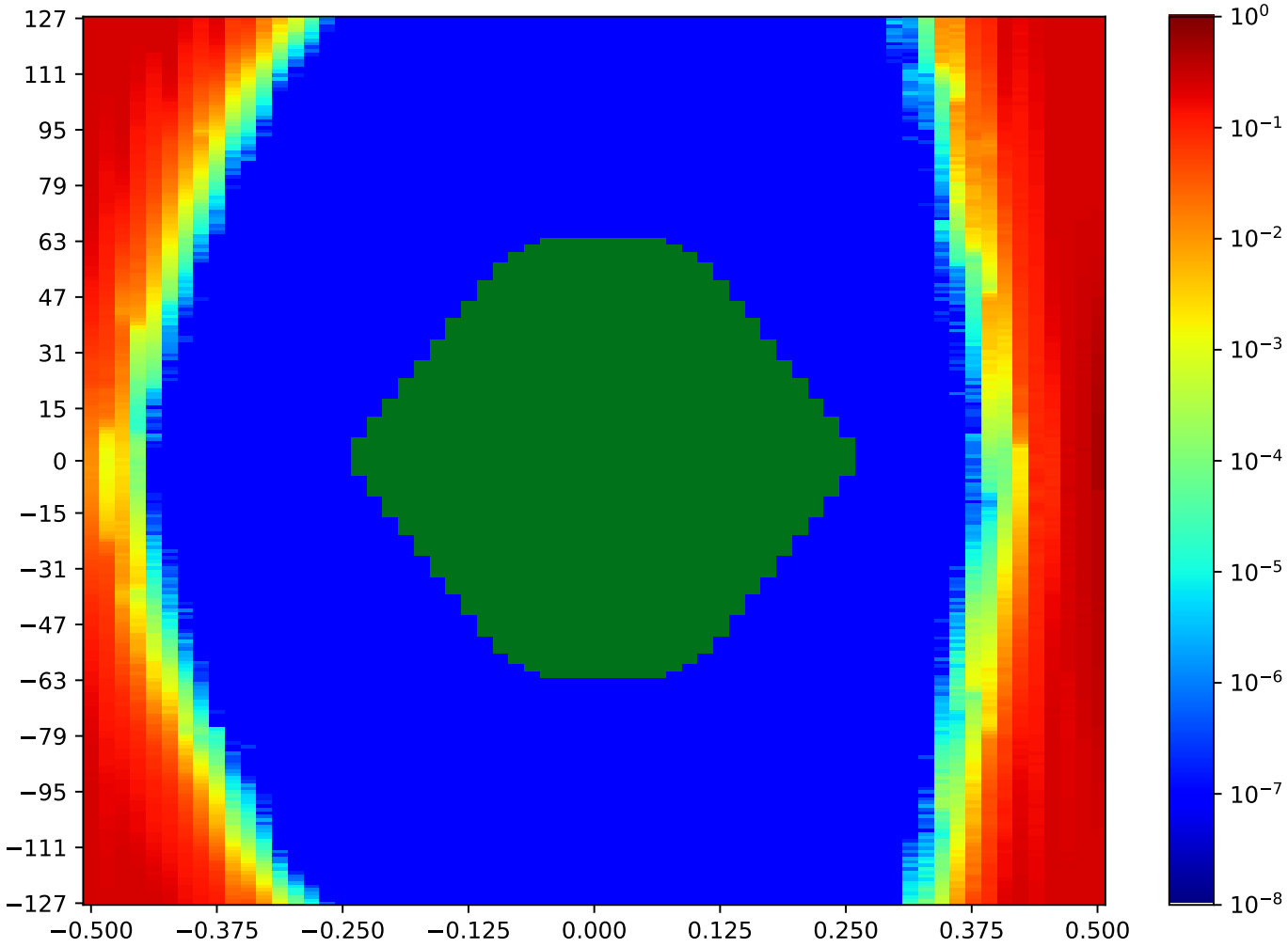


Figure 5.108: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.11 MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Table 5.100: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:13:38		2019-Nov-25 22:14:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11072	51	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

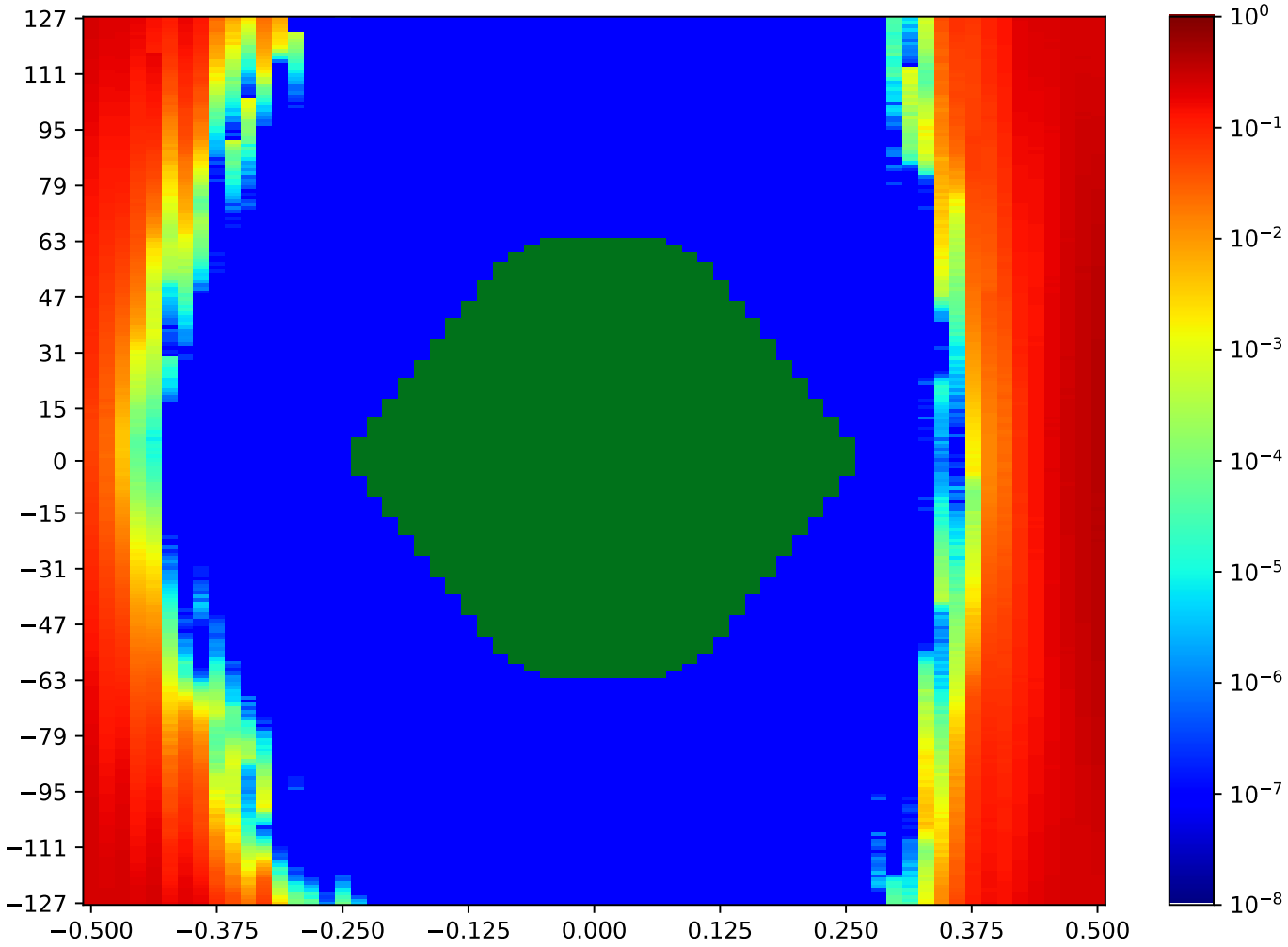


Figure 5.109: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.12 MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Table 5.101: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:14:11		2019-Nov-25 22:14:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10756	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

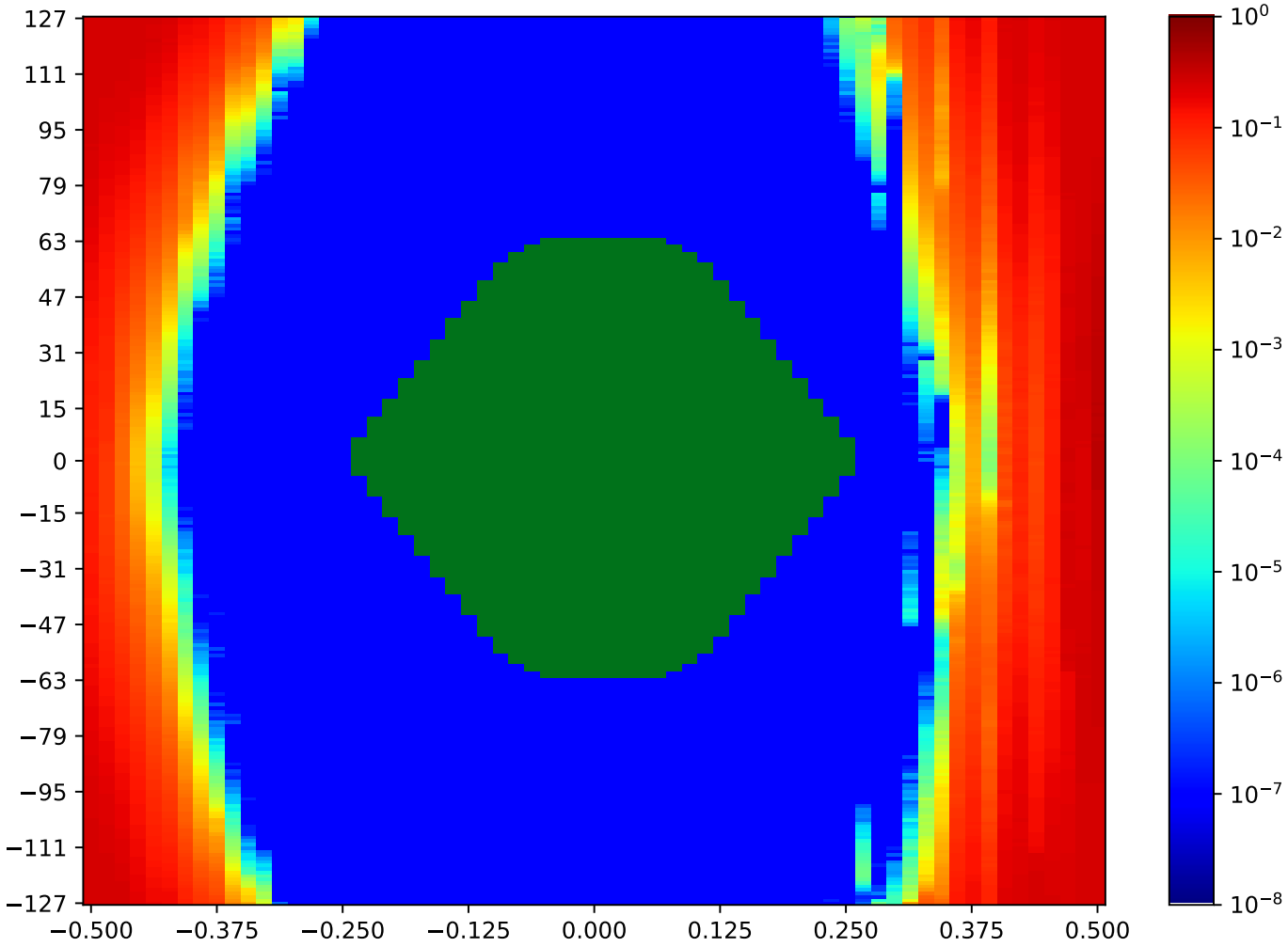


Figure 5.110: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.13 MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Table 5.102: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:14:43		2019-Nov-25 22:15:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11104	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

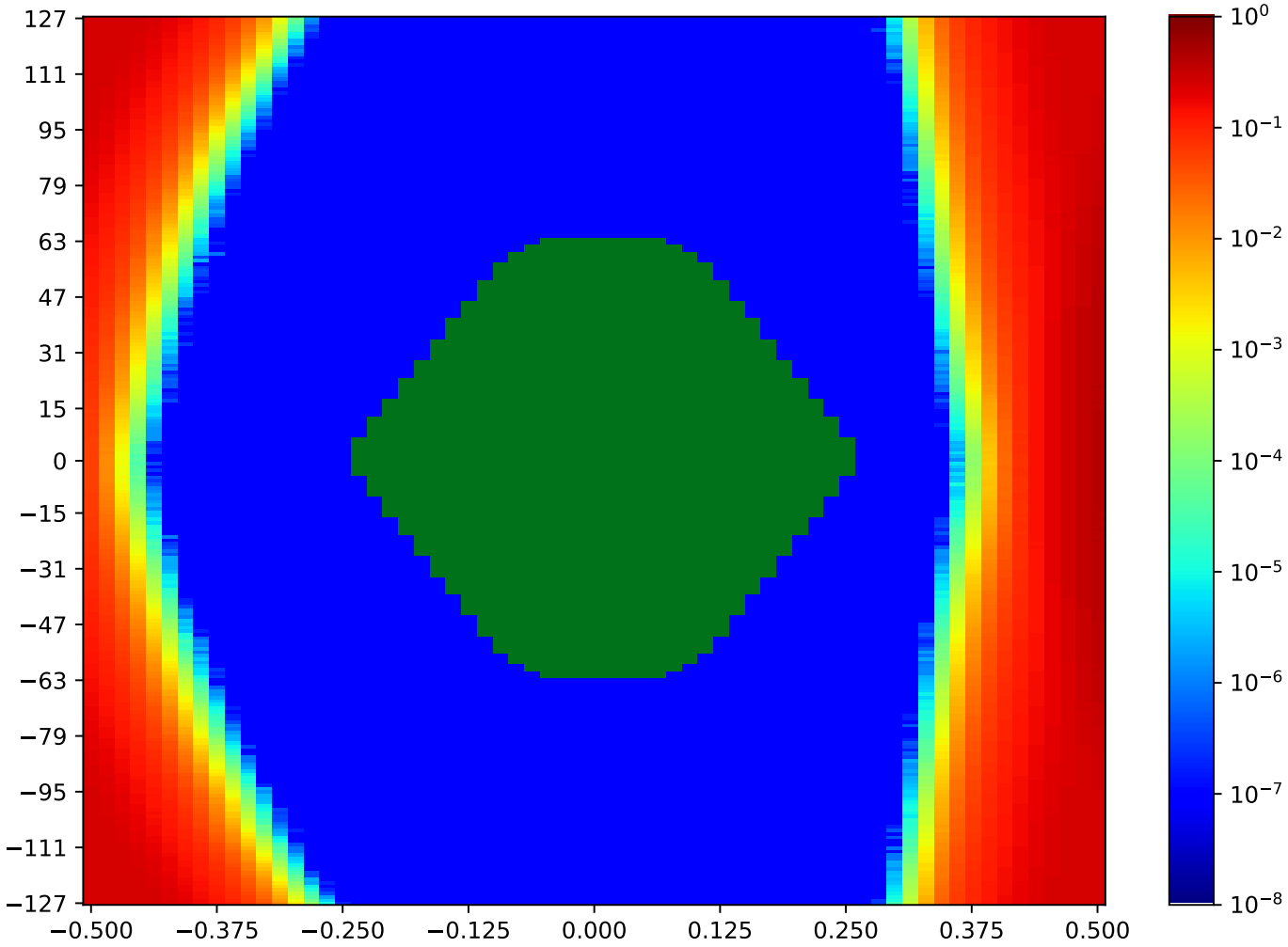


Figure 5.111: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.14 MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Table 5.103: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:15:16		2019-Nov-25 22:15:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11549	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

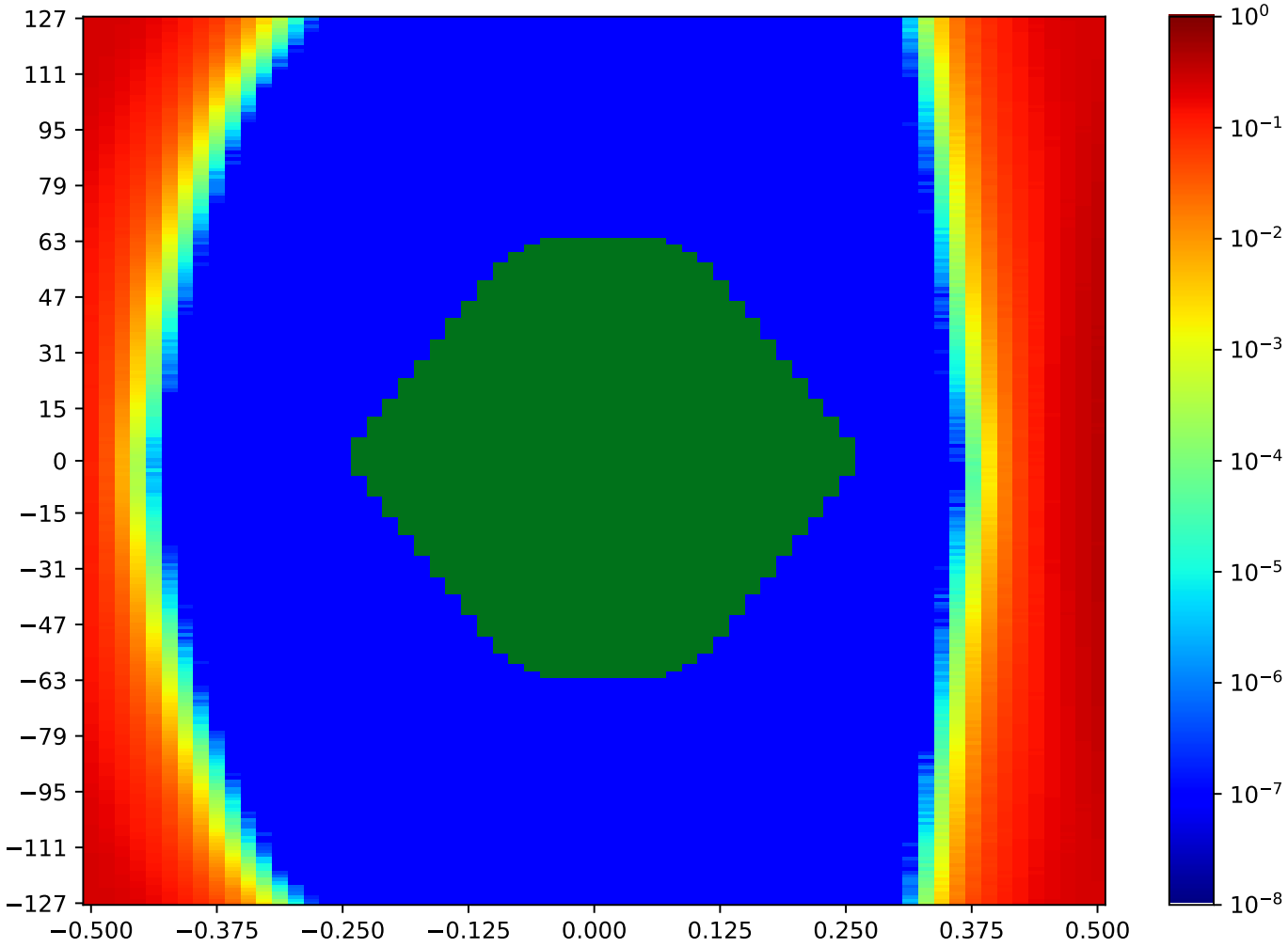


Figure 5.112: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.15 MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Table 5.104: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:15:49		2019-Nov-25 22:16:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11423	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

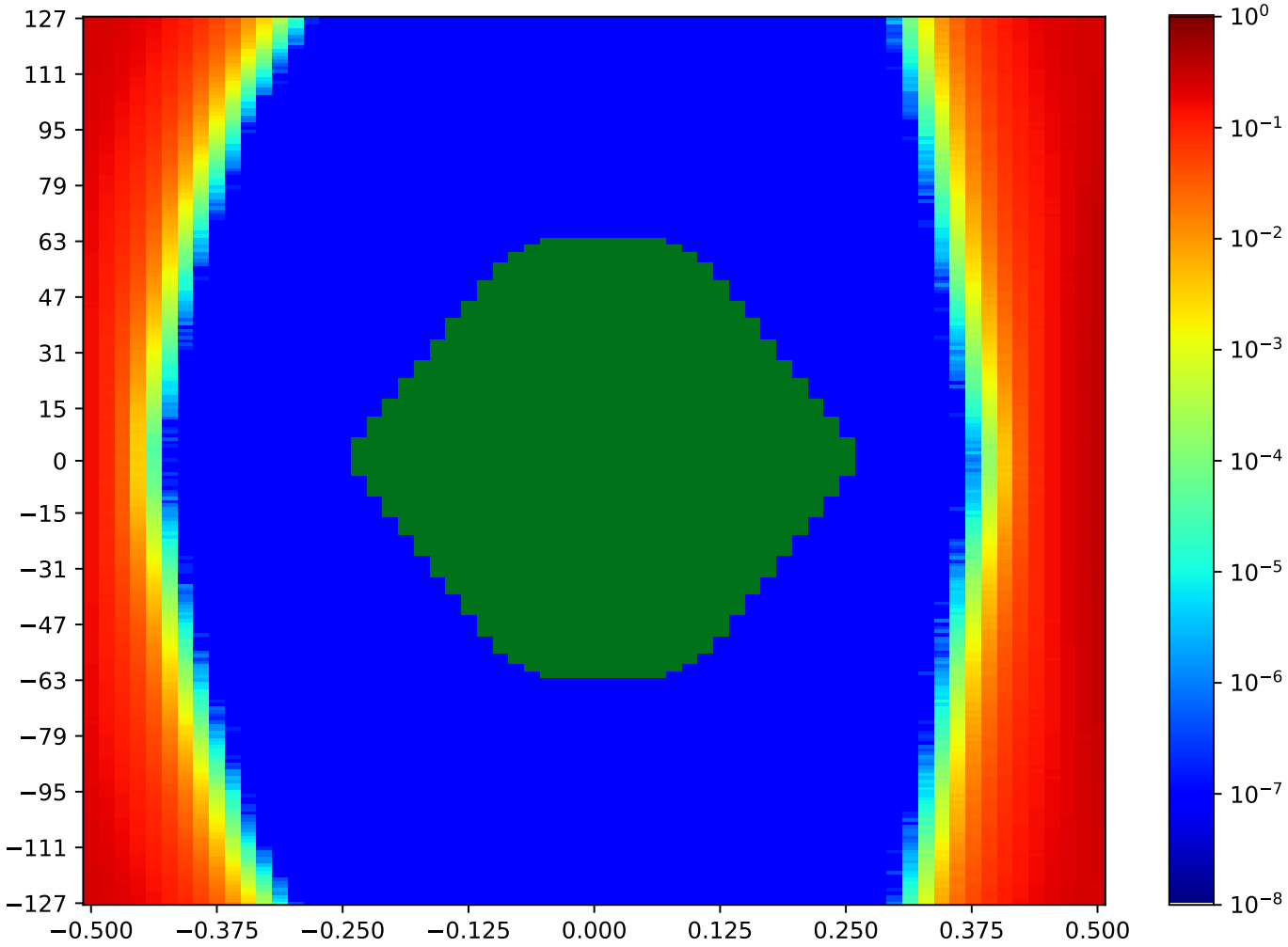


Figure 5.113: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.16 MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Table 5.105: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:16:22		2019-Nov-25 22:16:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11571	51	78.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

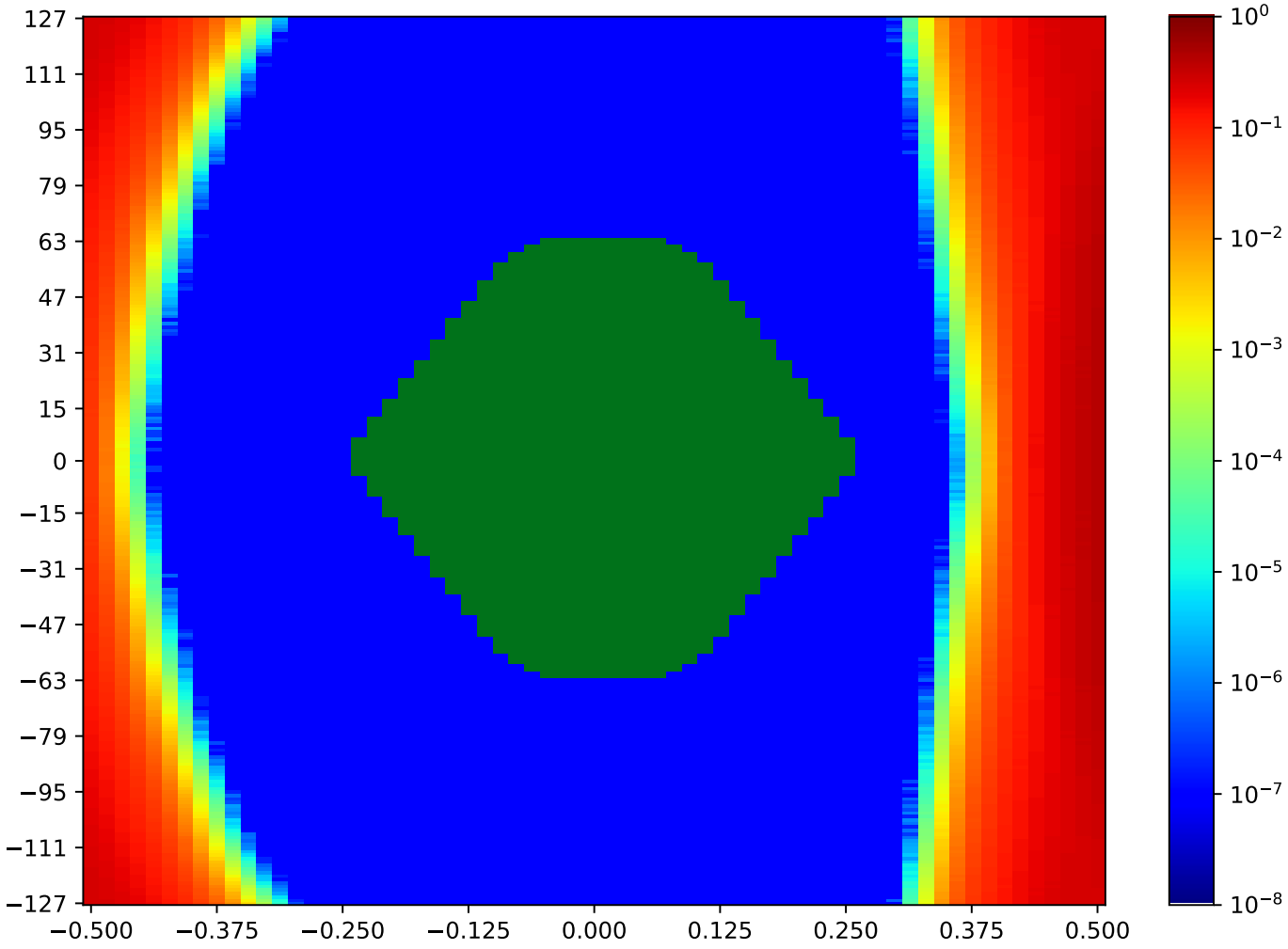


Figure 5.114: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.17 MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Table 5.106: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:16:54		2019-Nov-25 22:17:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10902	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

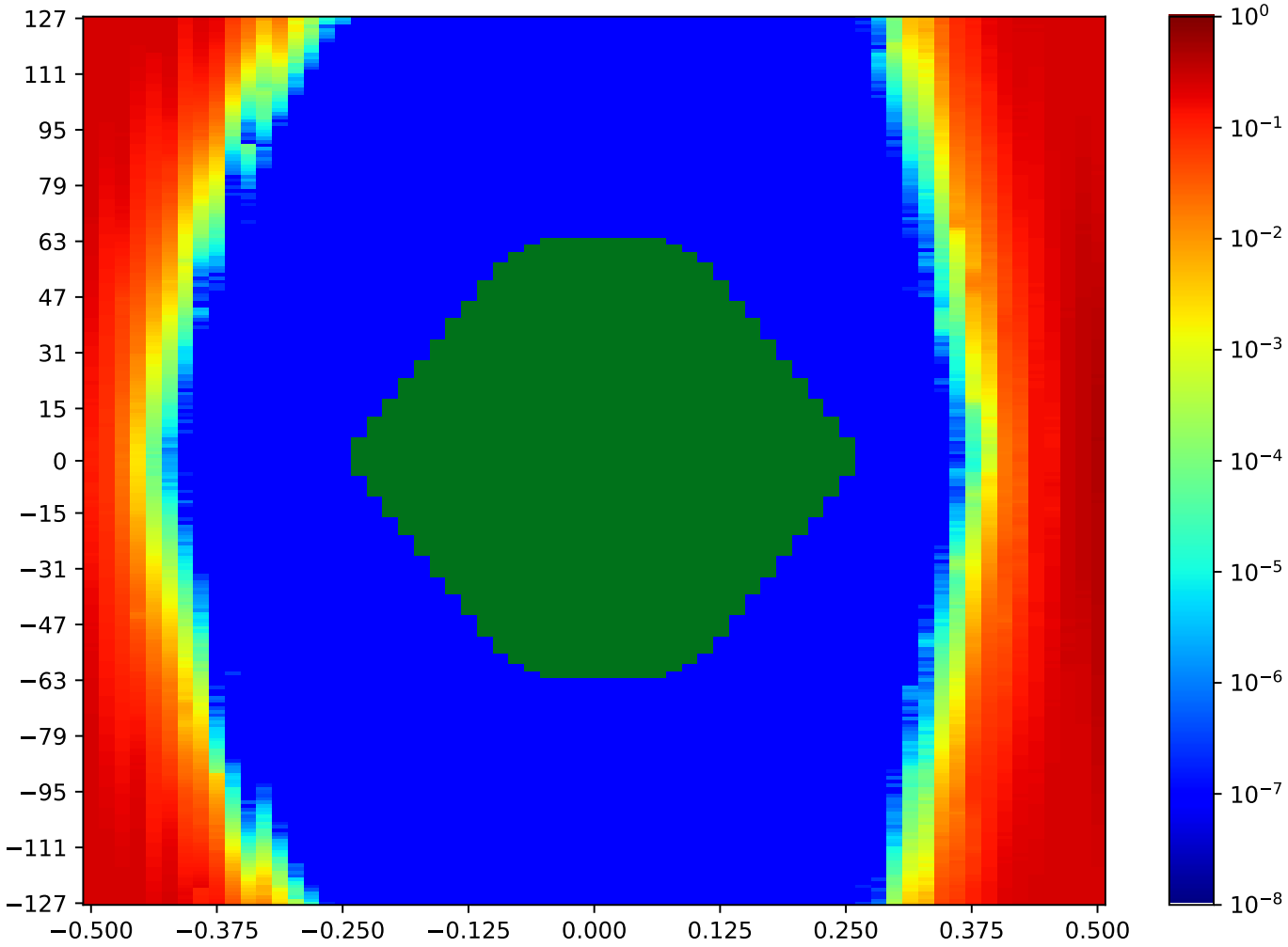


Figure 5.115: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.18 MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Table 5.107: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:17:27		2019-Nov-25 22:17:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10807	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

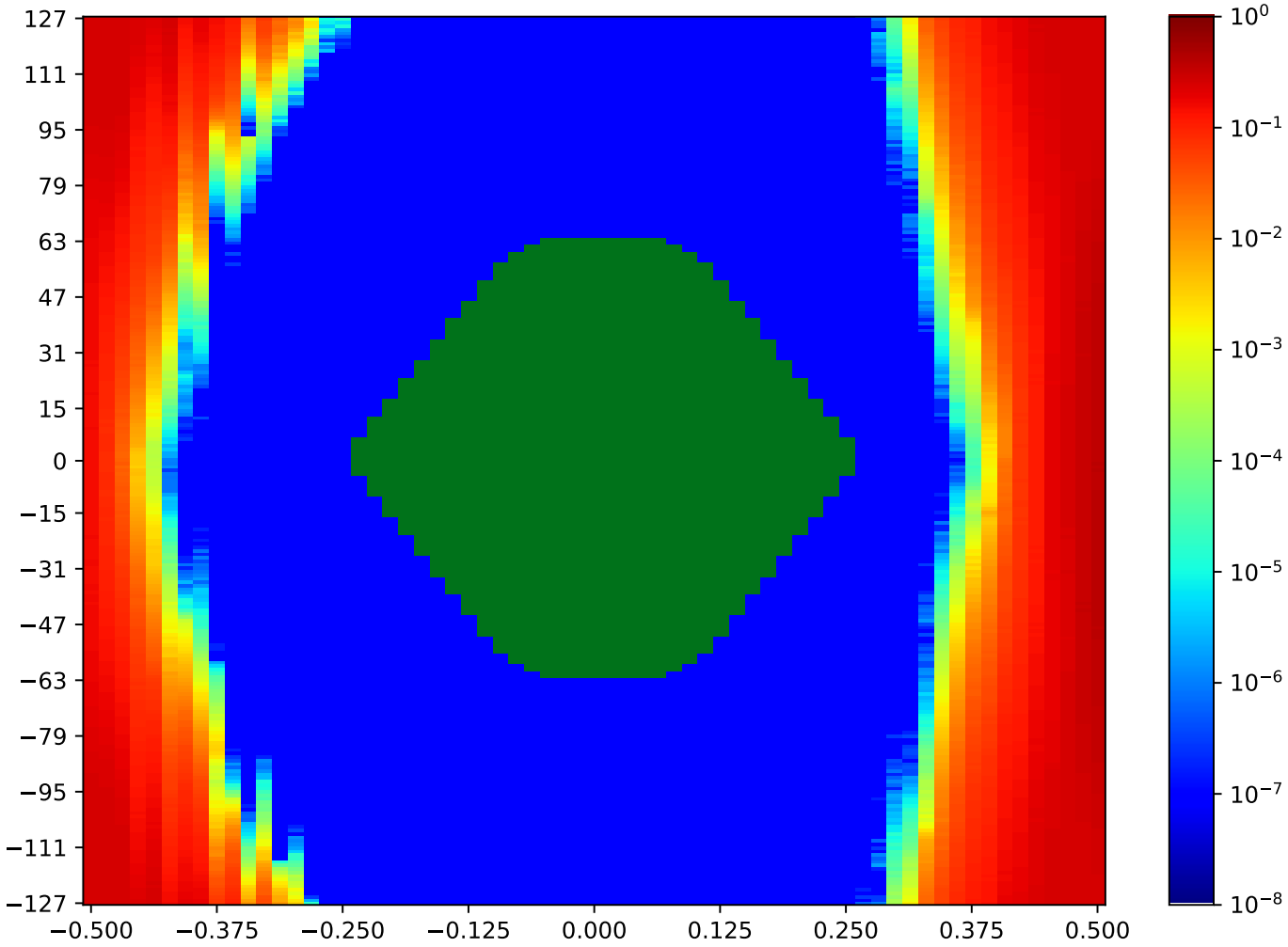


Figure 5.116: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.19 MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Table 5.108: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:17:59		2019-Nov-25 22:18:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11056	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

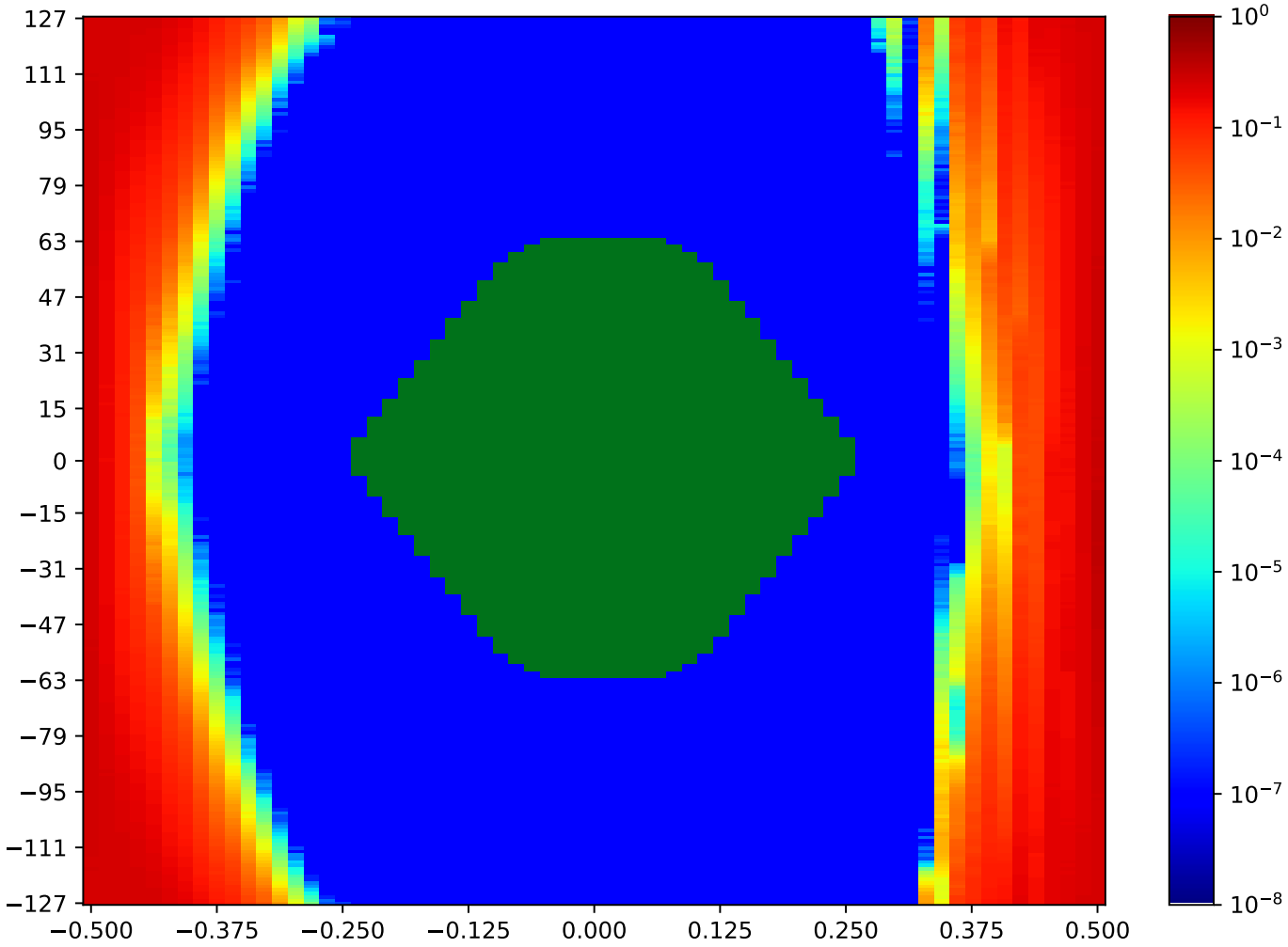


Figure 5.117: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.20 MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Table 5.109: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:18:32		2019-Nov-25 22:19:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10516	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

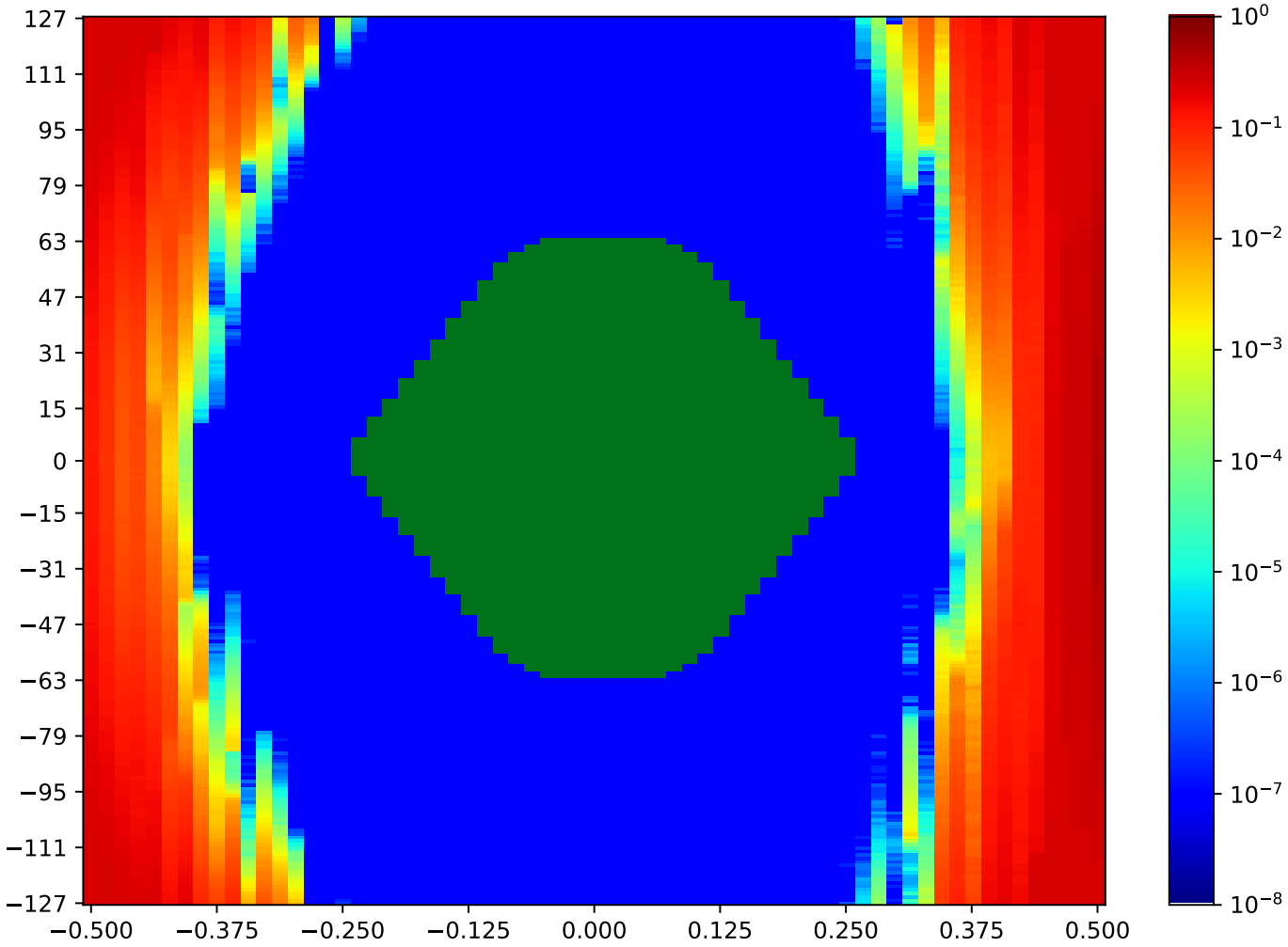


Figure 5.118: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.21 MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Table 5.110: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:19:04		2019-Nov-25 22:19:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10637	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

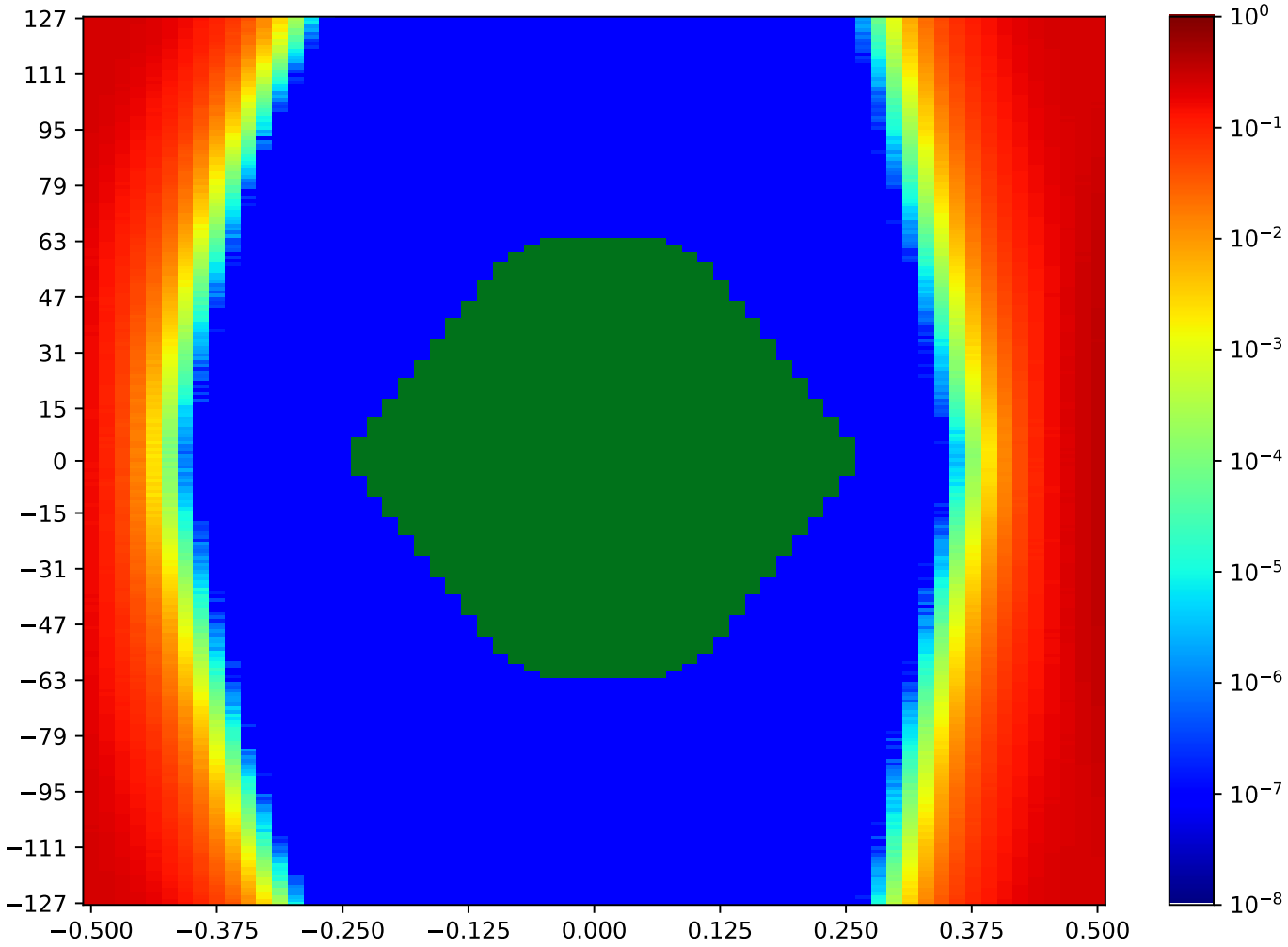


Figure 5.119: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.22 MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Table 5.111: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:19:36		2019-Nov-25 22:20:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11255	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

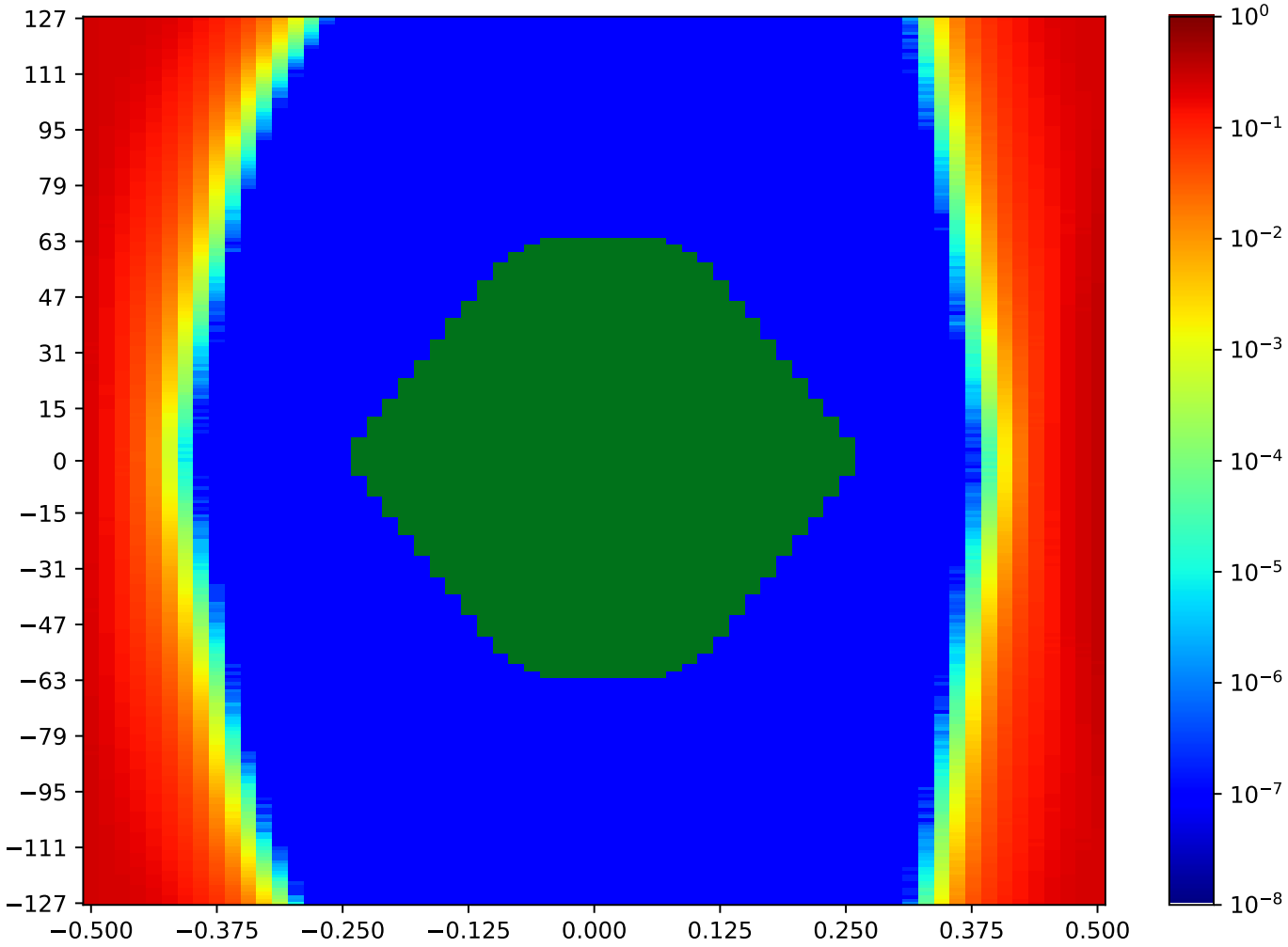


Figure 5.120: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.23 MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Table 5.112: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:20:09		2019-Nov-25 22:20:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10699	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

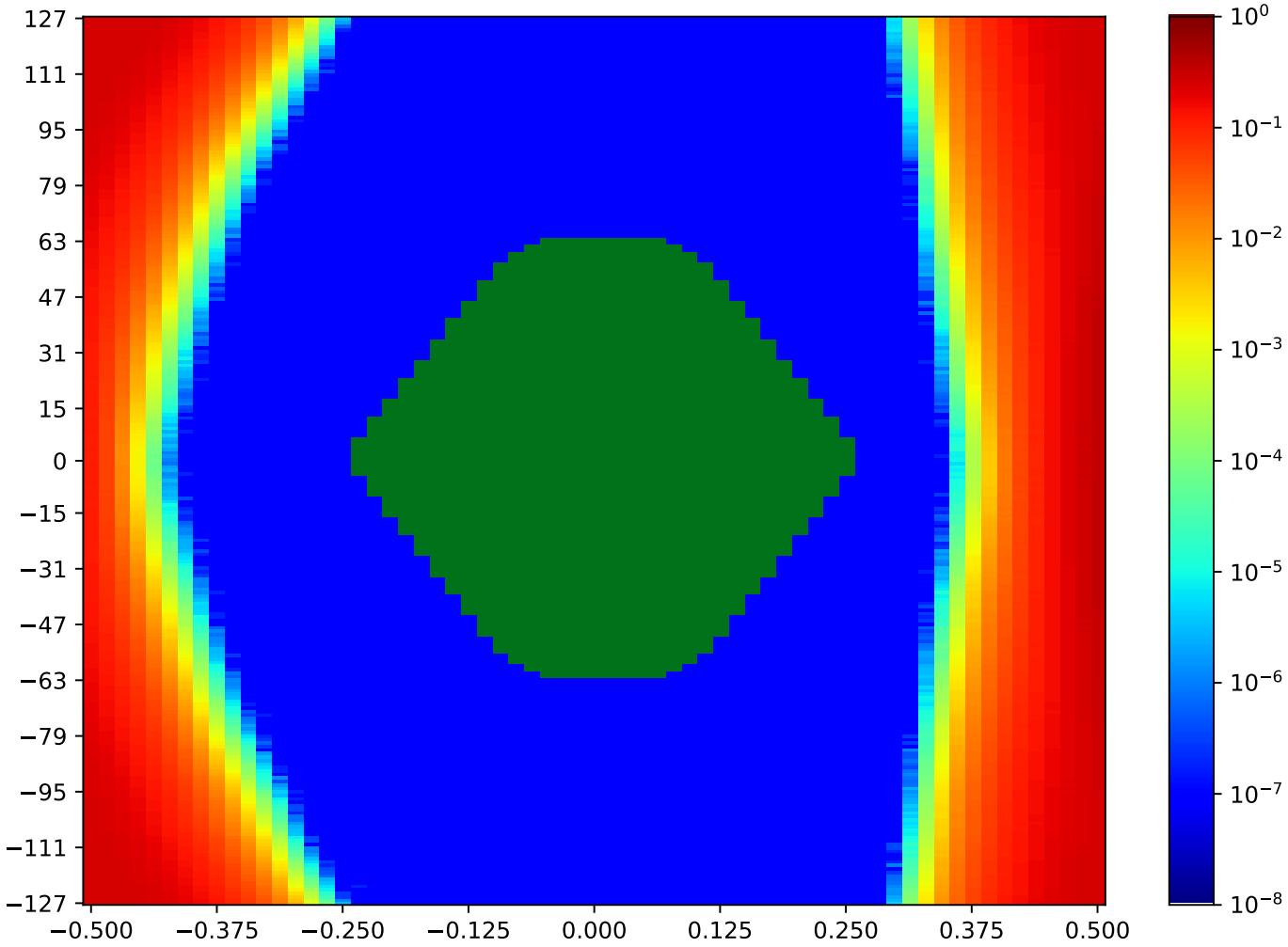


Figure 5.121: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.24 MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Table 5.113: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:20:42		2019-Nov-25 22:21:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10770	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

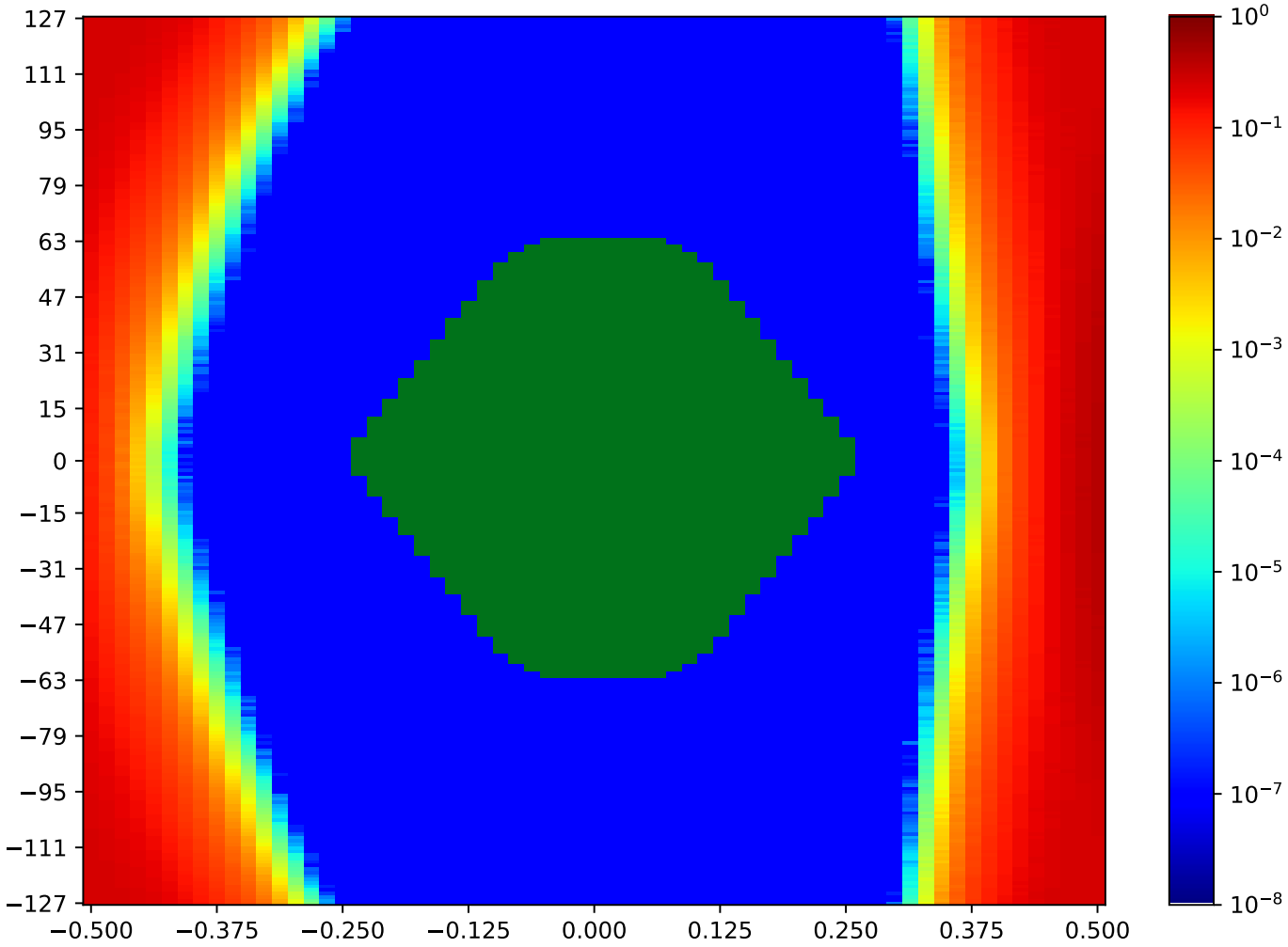


Figure 5.122: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.25 MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Table 5.114: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:21:15		2019-Nov-25 22:21:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11130	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

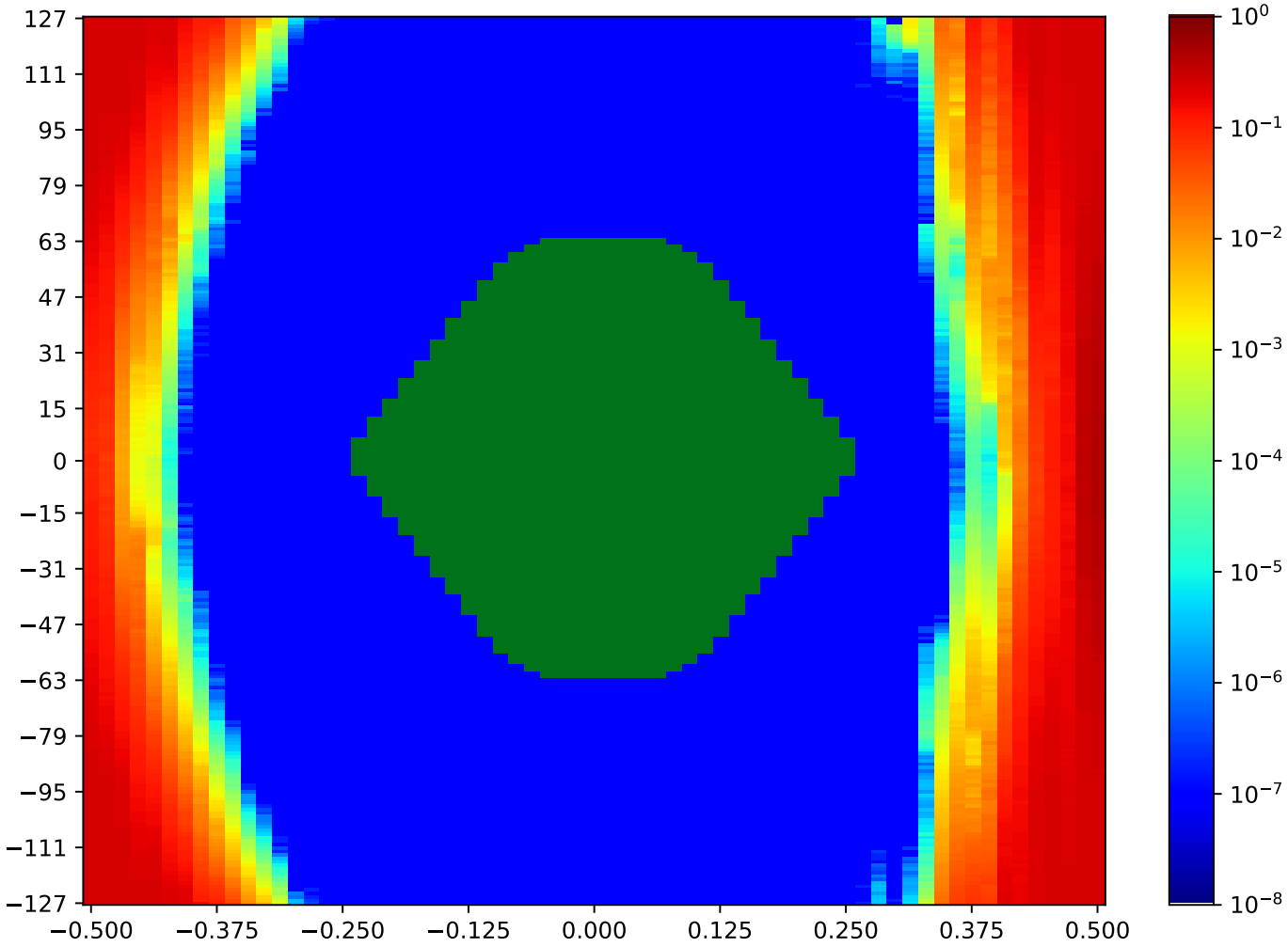


Figure 5.123: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.26 MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Table 5.115: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:21:48		2019-Nov-25 22:22:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10866	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

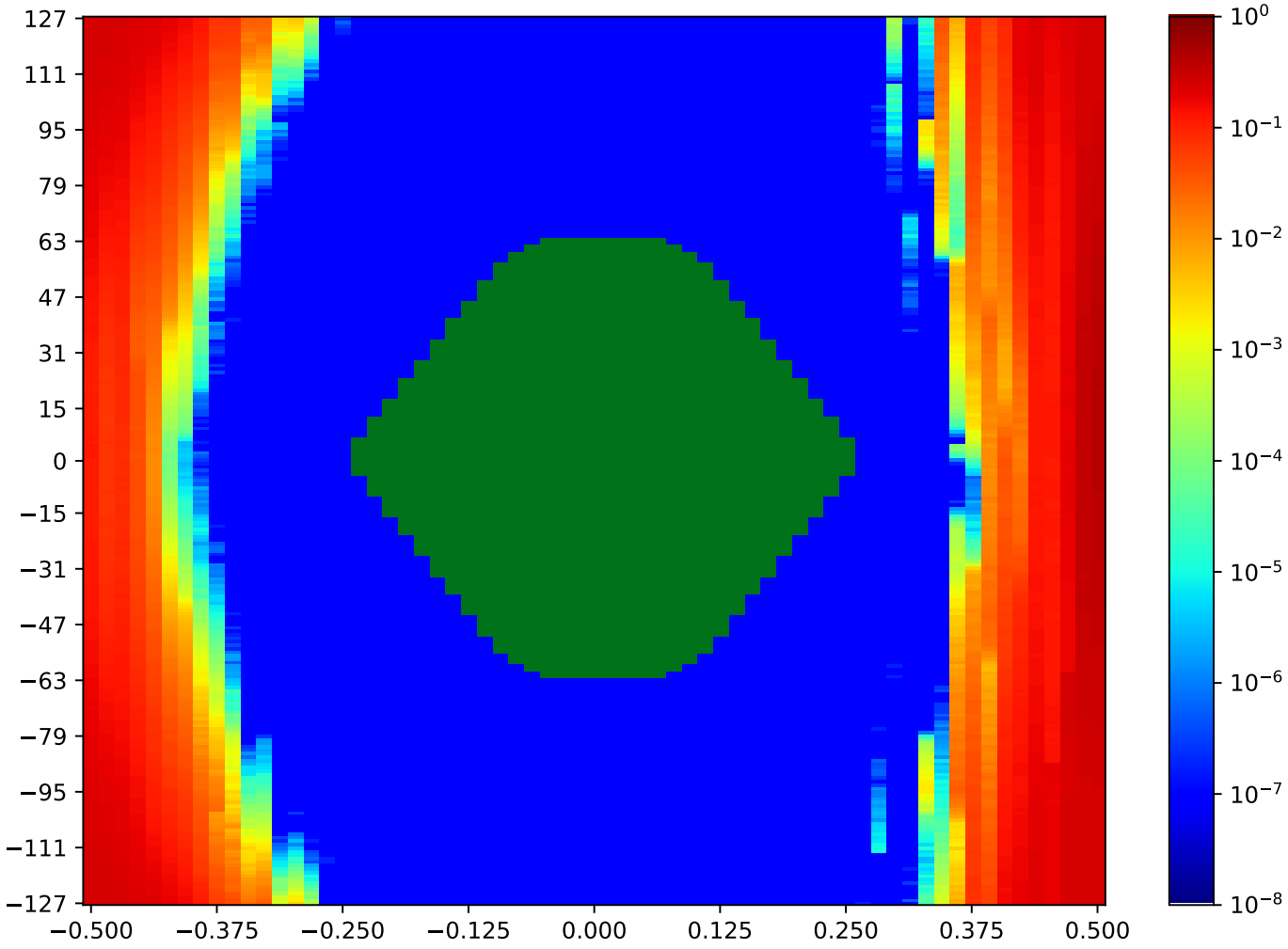


Figure 5.124: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.27 MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Table 5.116: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:22:20		2019-Nov-25 22:22:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11268	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

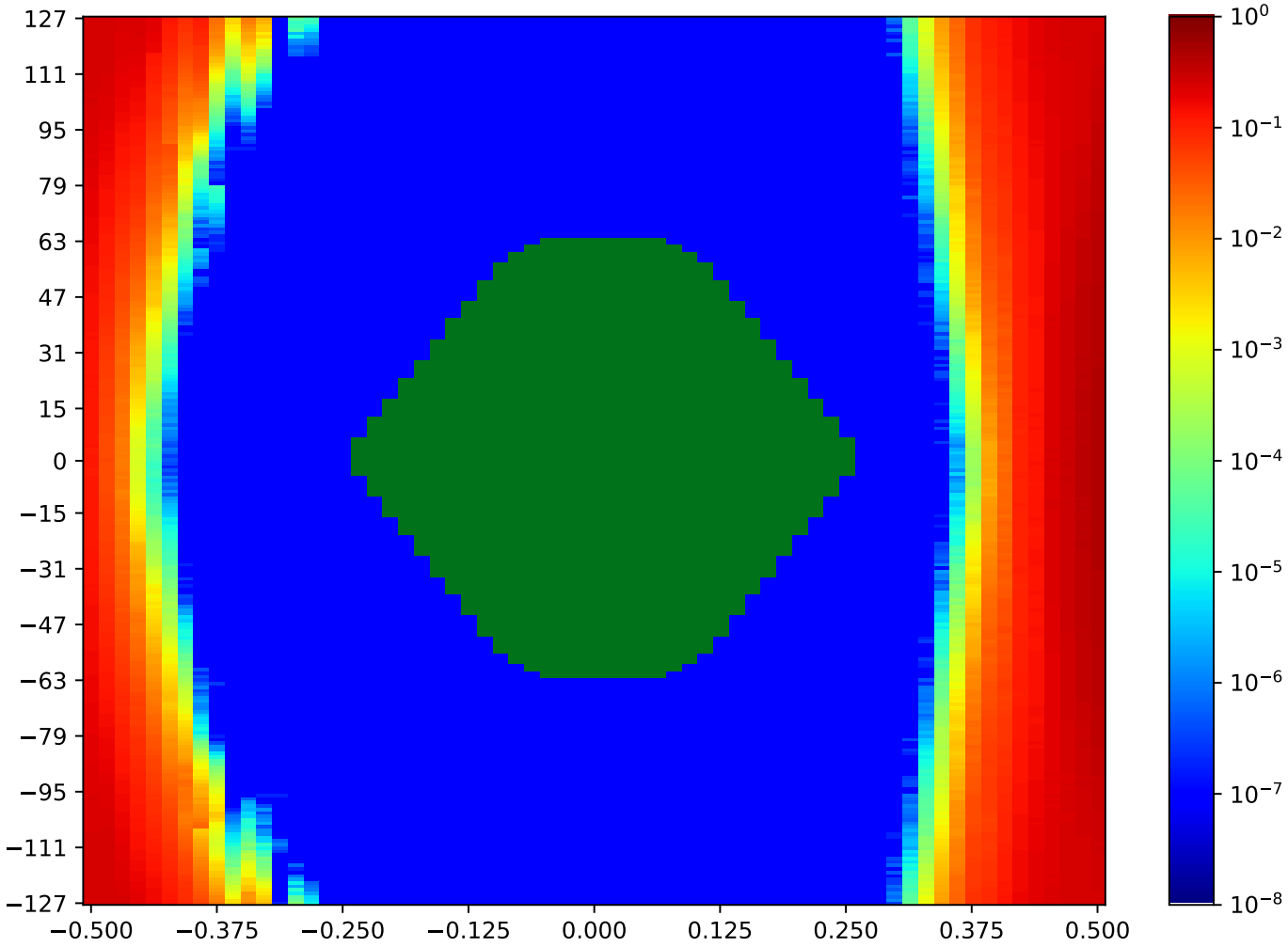


Figure 5.125: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.9.28 MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Table 5.117: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-25 22:22:53		2019-Nov-25 22:23:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	11170	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

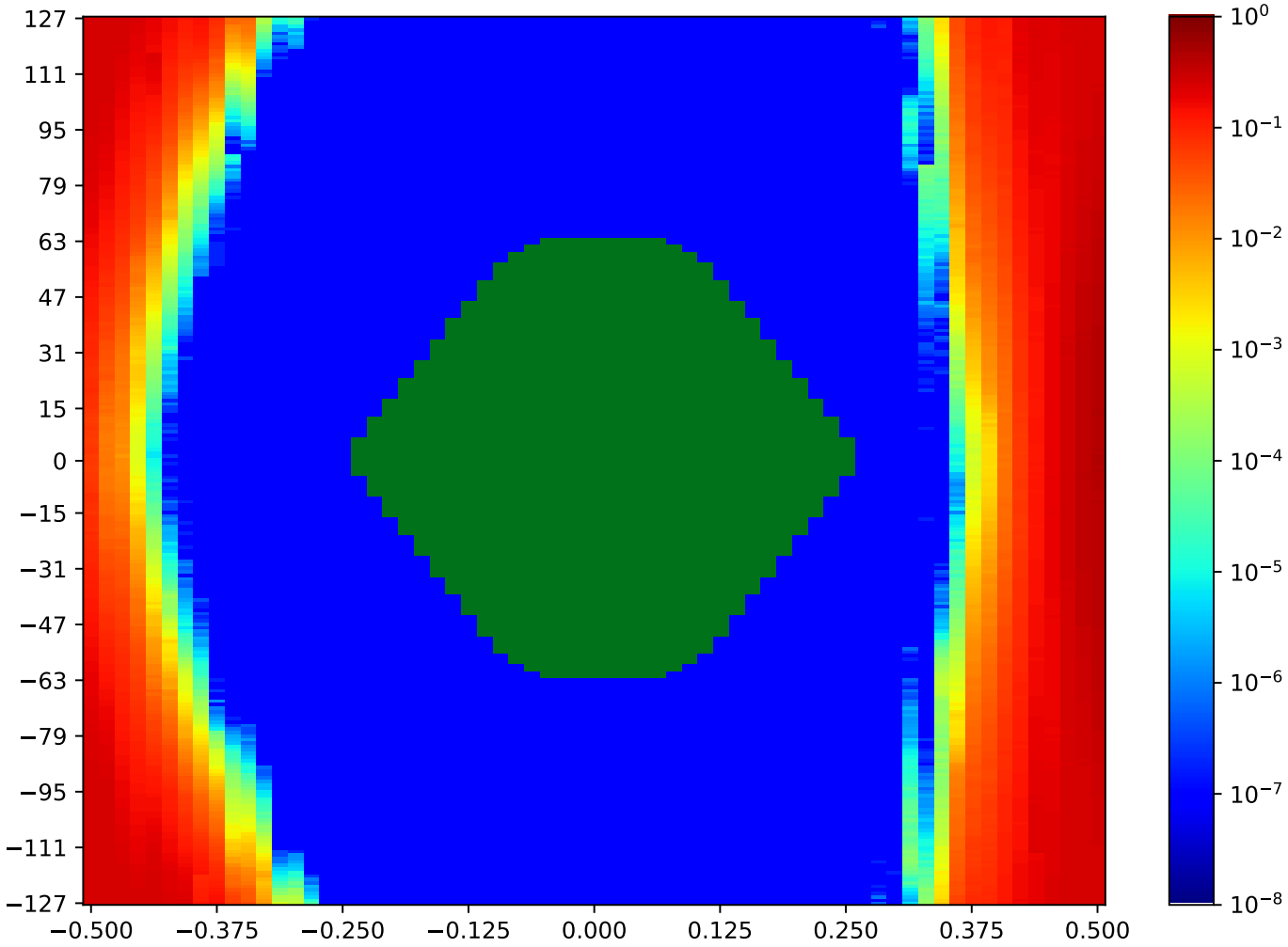


Figure 5.126: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10 MSP_A TX1 MSP_C RX17 Minipod Loopback

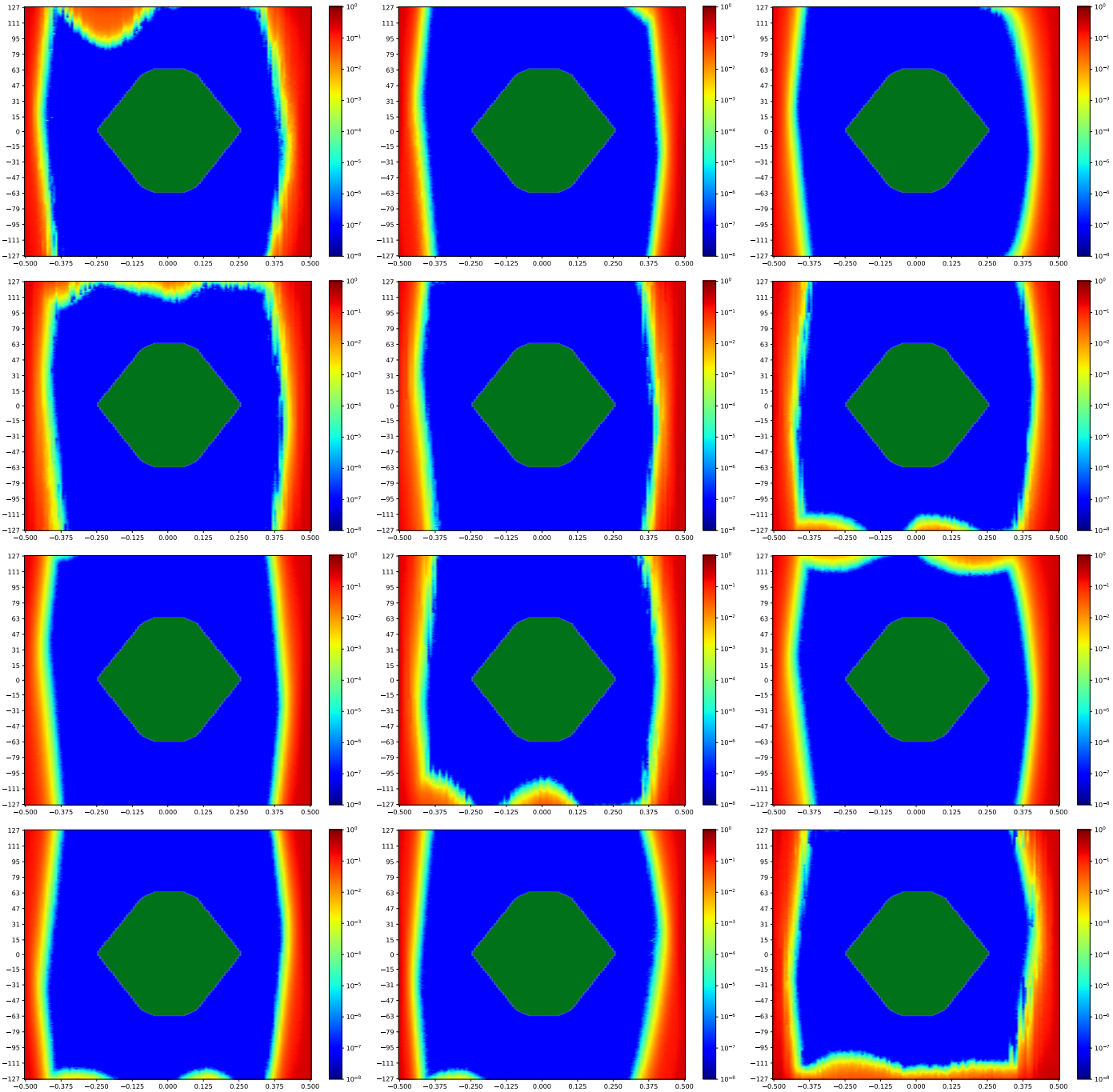


Figure 5.127: MSP_A TX1 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.140.

5.10.1 MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Table 5.118: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:24:07		2019-Nov-26 12:25:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23205	102	79.07%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

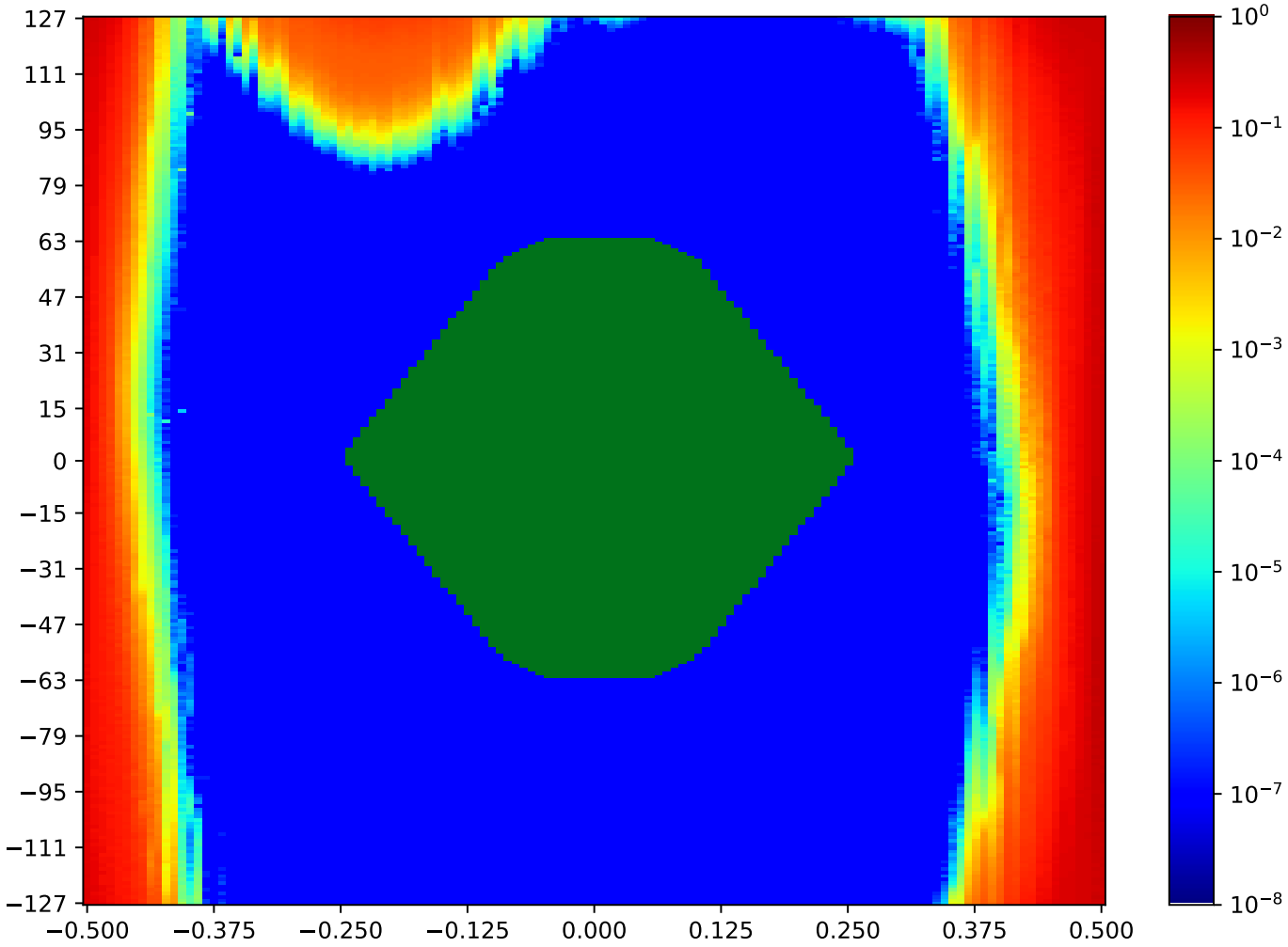


Figure 5.128: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.2 MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Table 5.119: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:26:28		2019-Nov-26 12:27:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24820	101	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

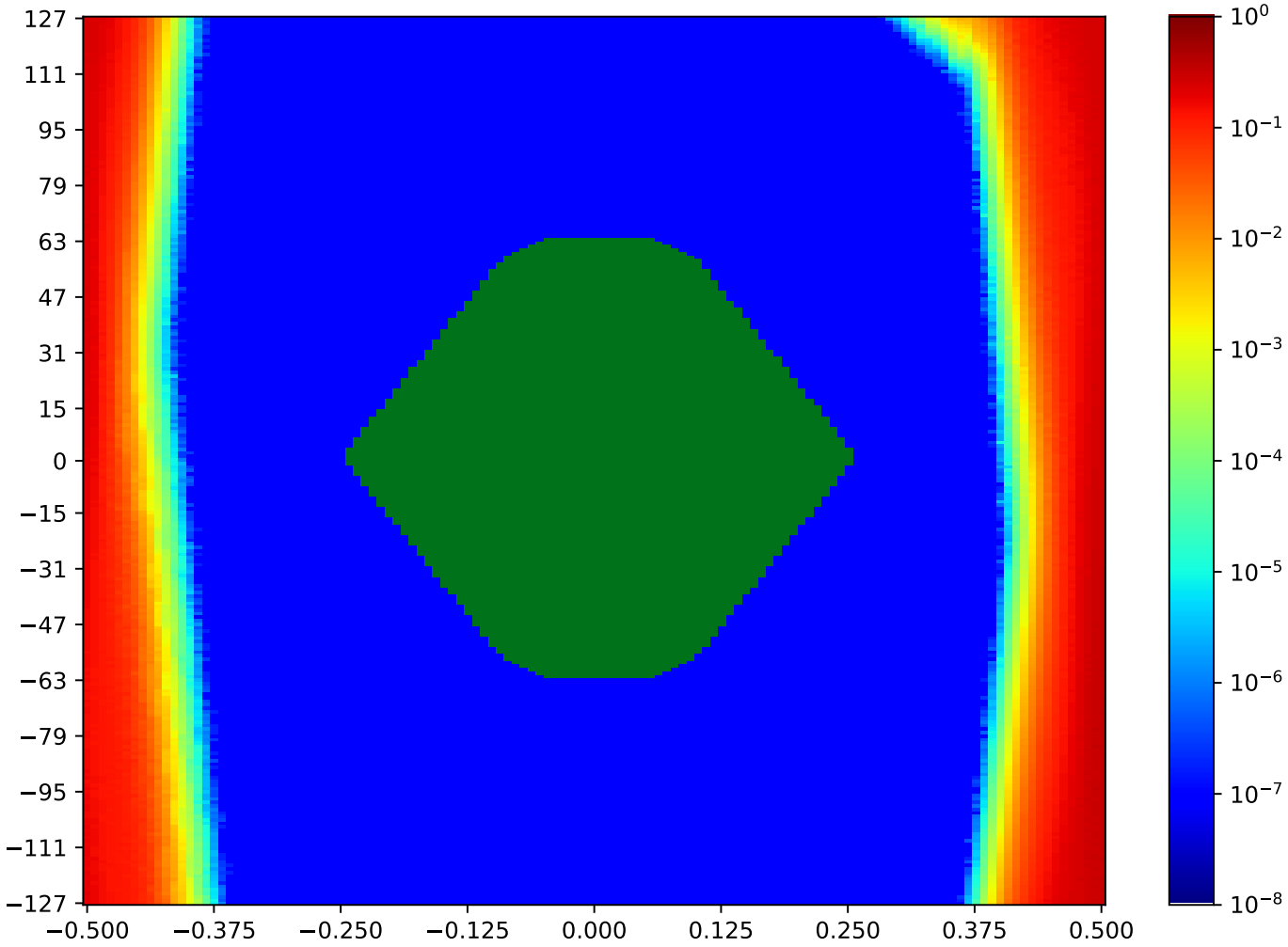


Figure 5.129: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.3 MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Table 5.120: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:27:36		2019-Nov-26 12:28:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24050	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

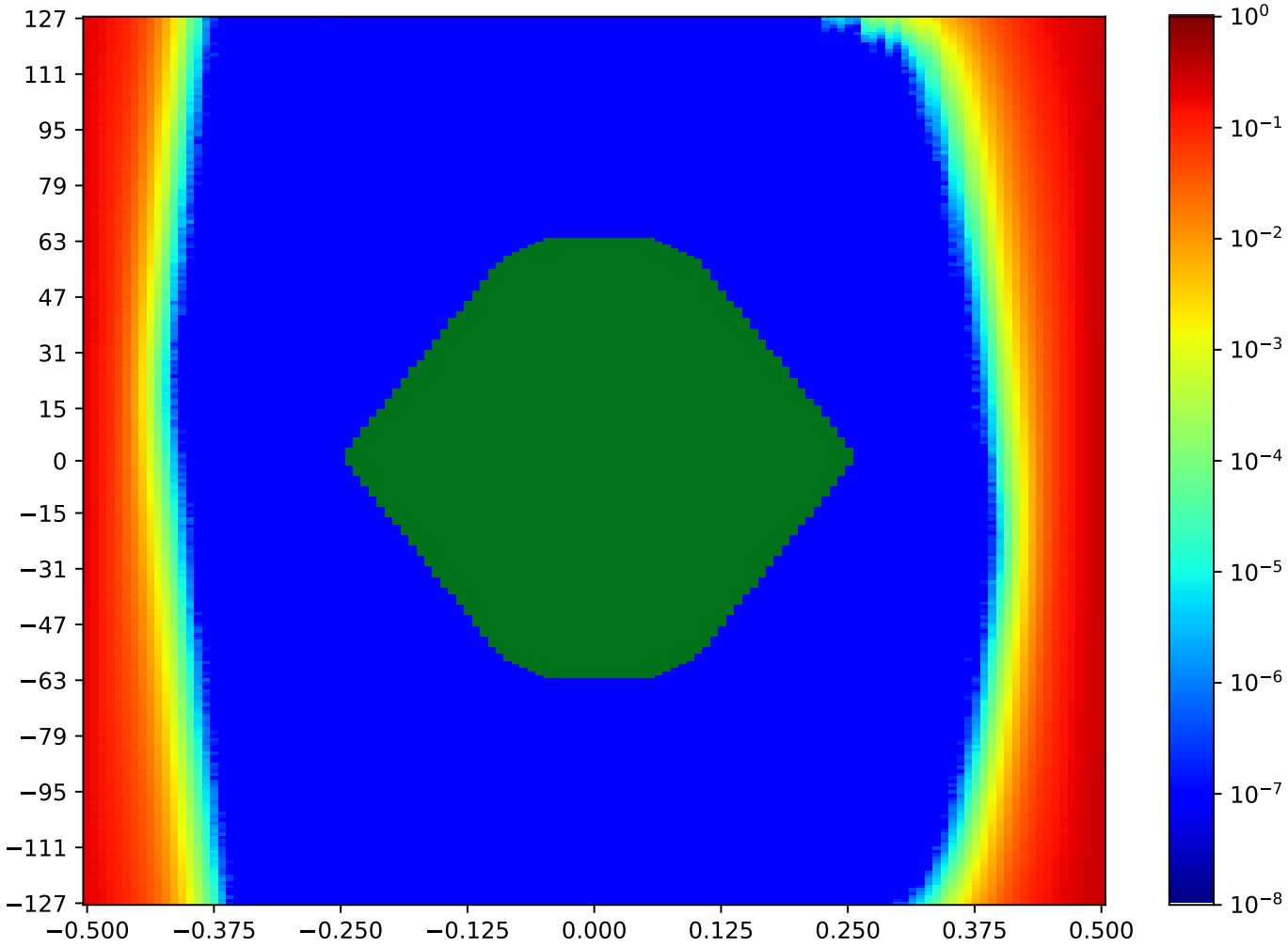


Figure 5.130: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.4 MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Table 5.121: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:21:47		2019-Nov-26 12:22:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22846	98	75.97%	232	90.98%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

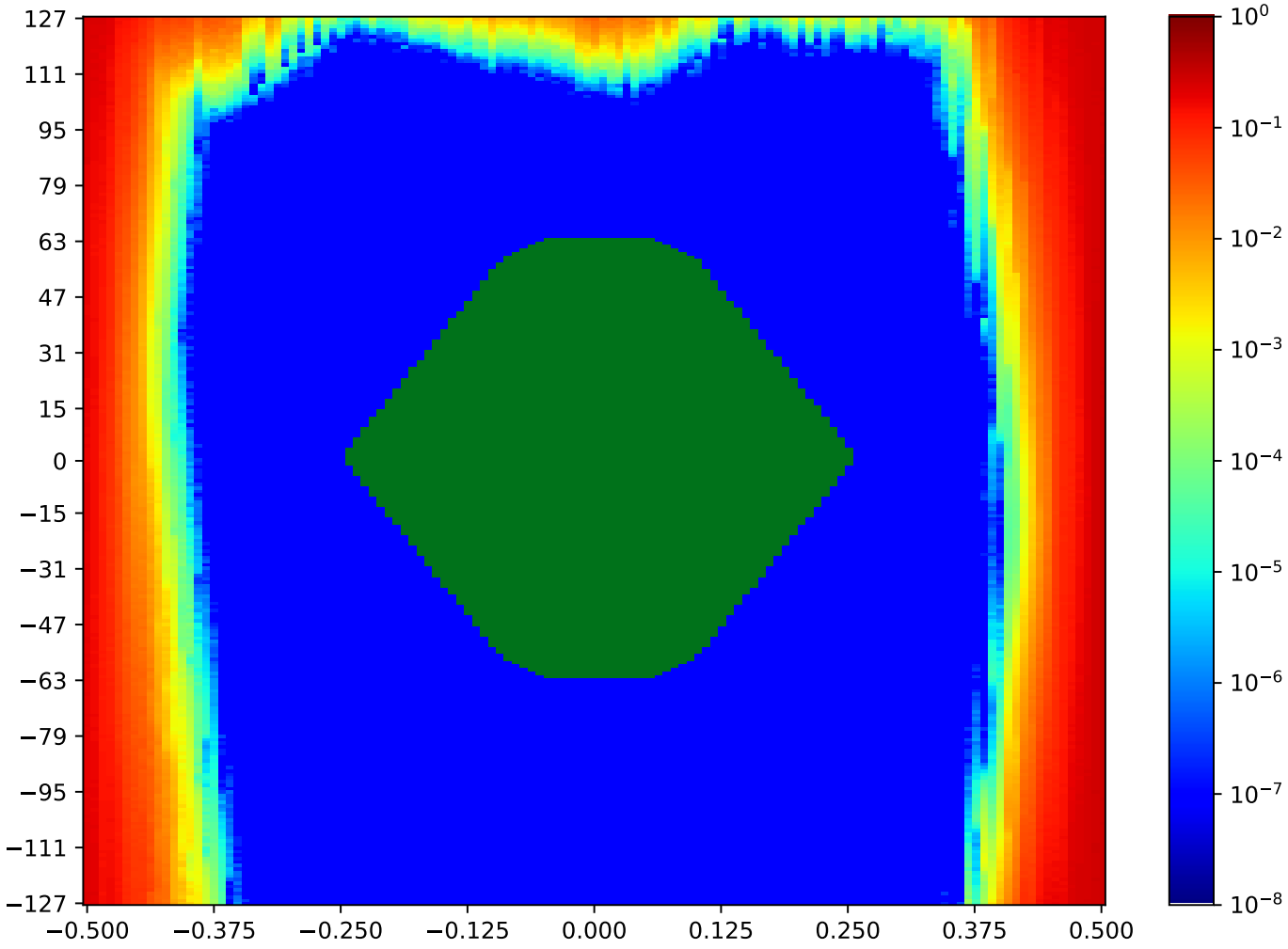


Figure 5.131: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.5 MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Table 5.122: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:31:12		2019-Nov-26 12:32:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24321	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

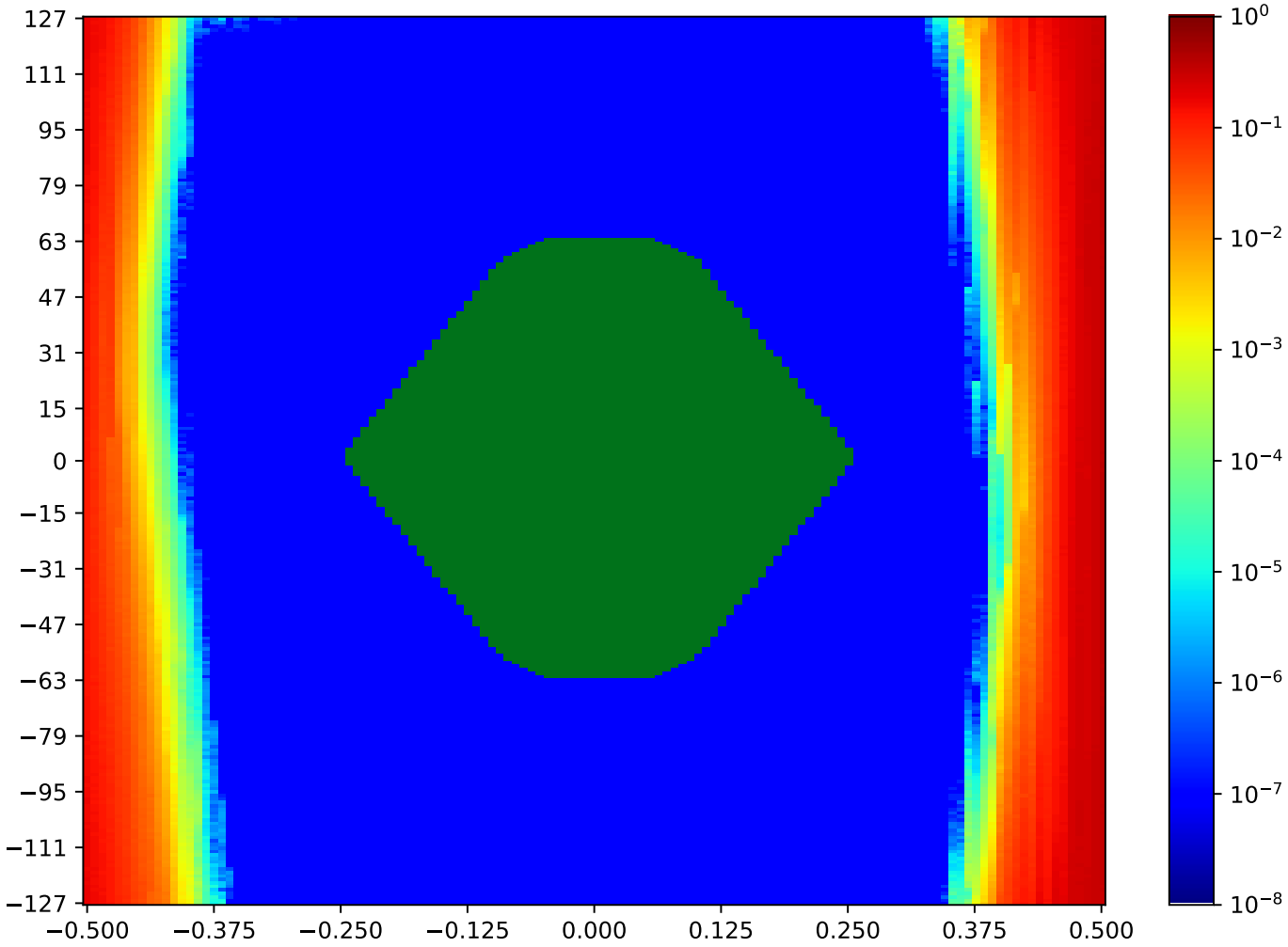


Figure 5.132: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.6 MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Table 5.123: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:20:40		2019-Nov-26 12:21:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23785	103	79.84%	238	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

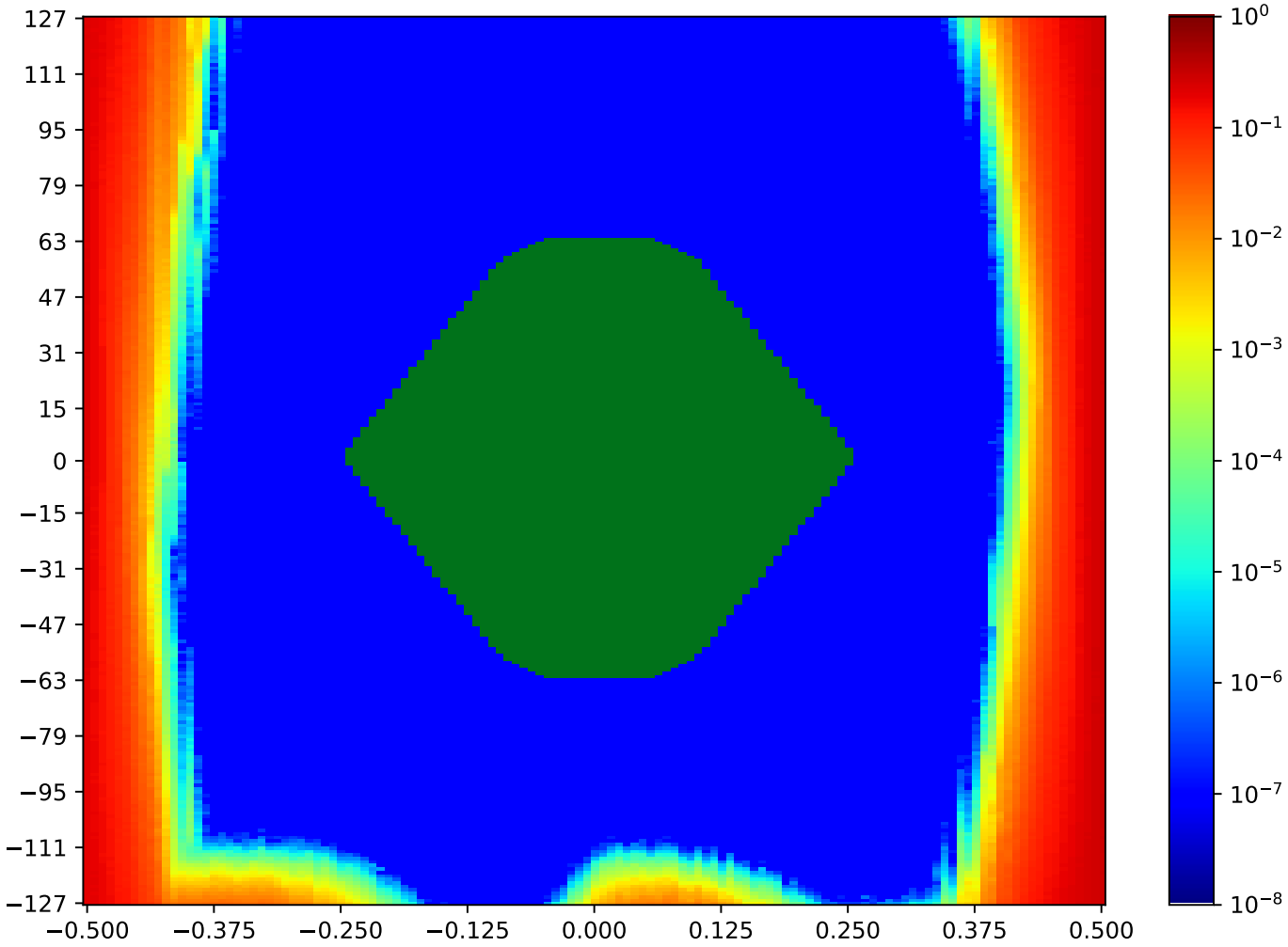


Figure 5.133: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.7 MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Table 5.124: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:33:28		2019-Nov-26 12:34:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24250	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

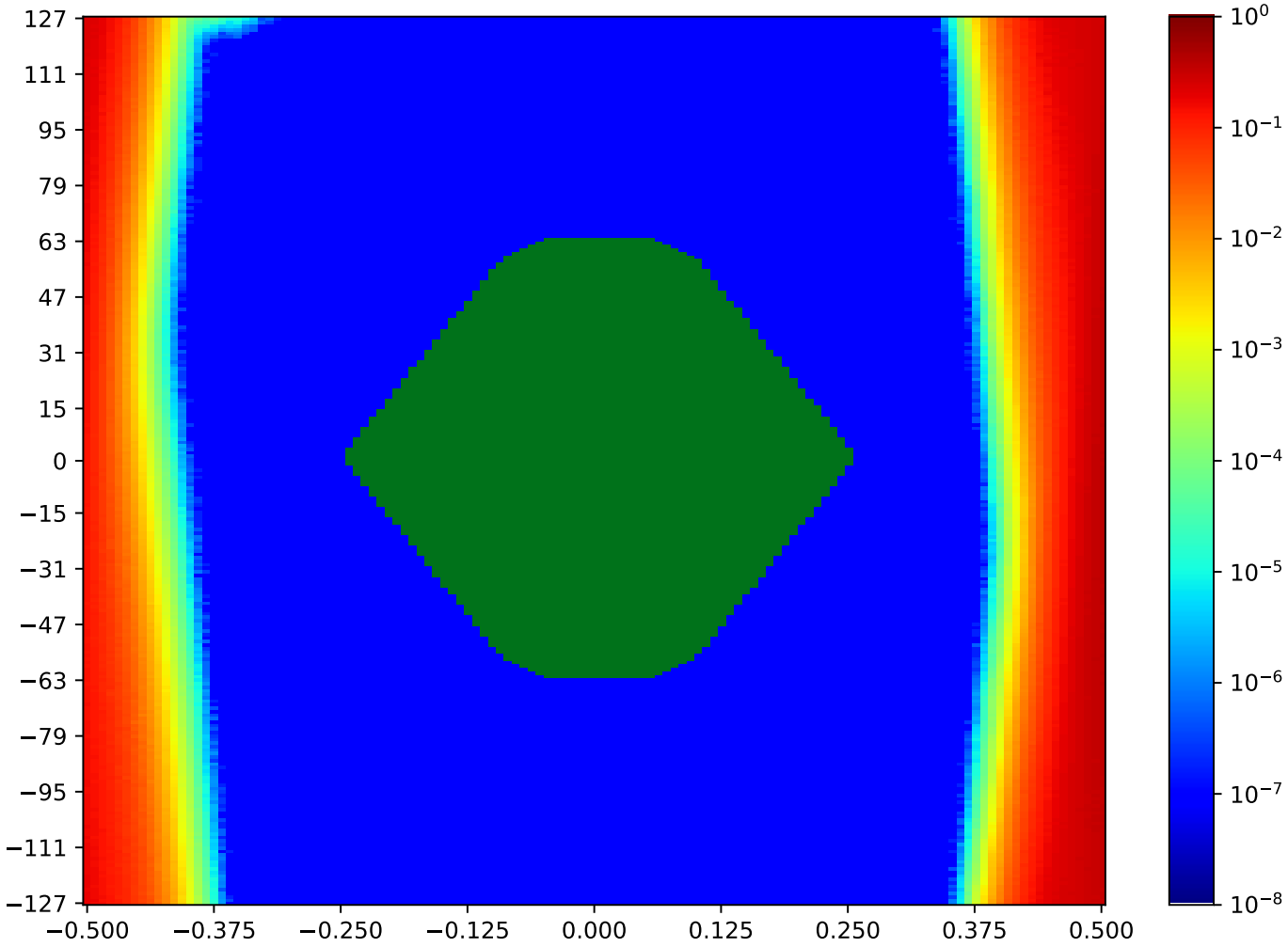


Figure 5.134: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.8 MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Table 5.125: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:22:56		2019-Nov-26 12:24:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23012	100	77.52%	224	87.45%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

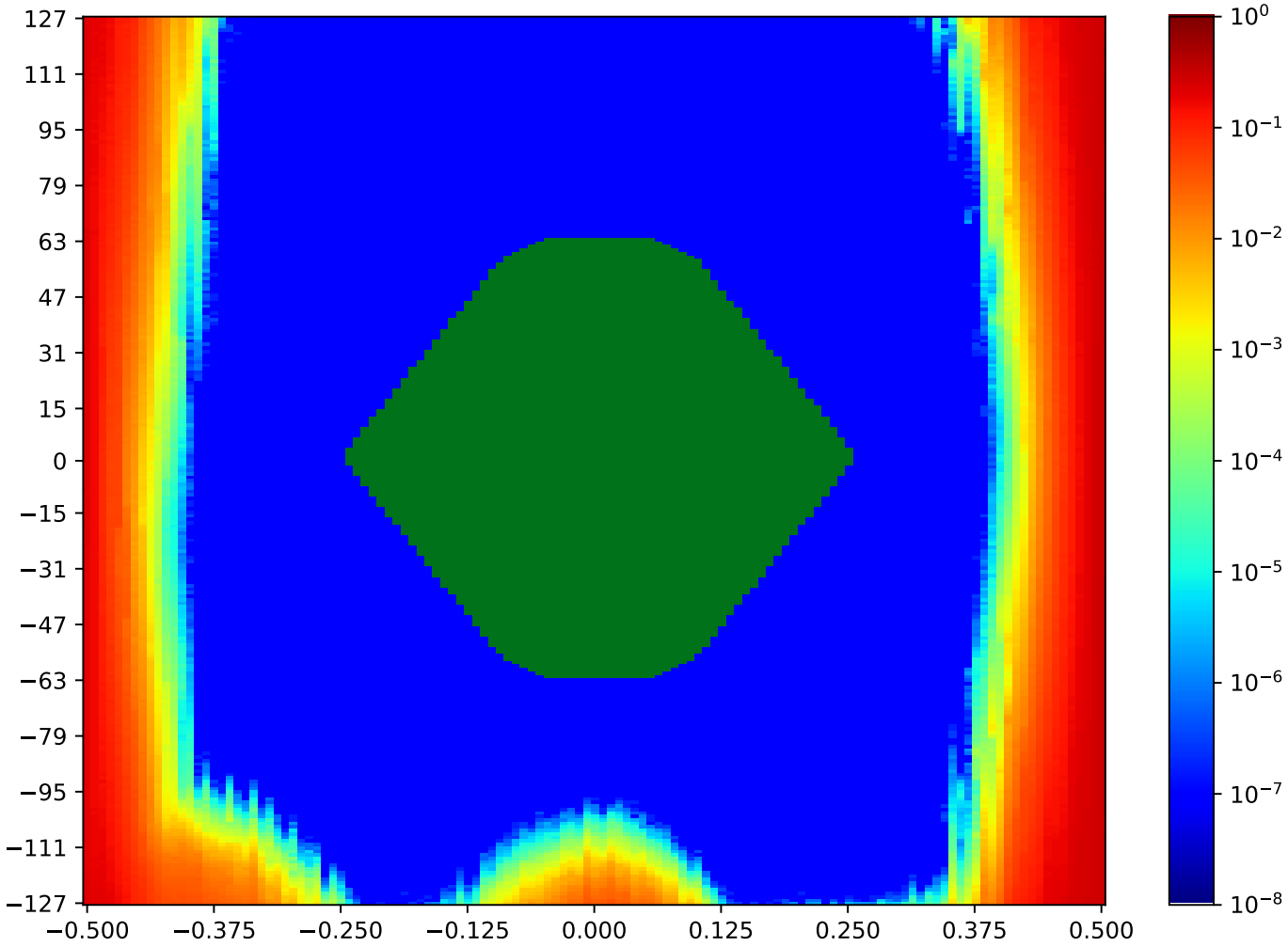


Figure 5.135: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.9 MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Table 5.126: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:32:20		2019-Nov-26 12:33:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22694	99	76.74%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

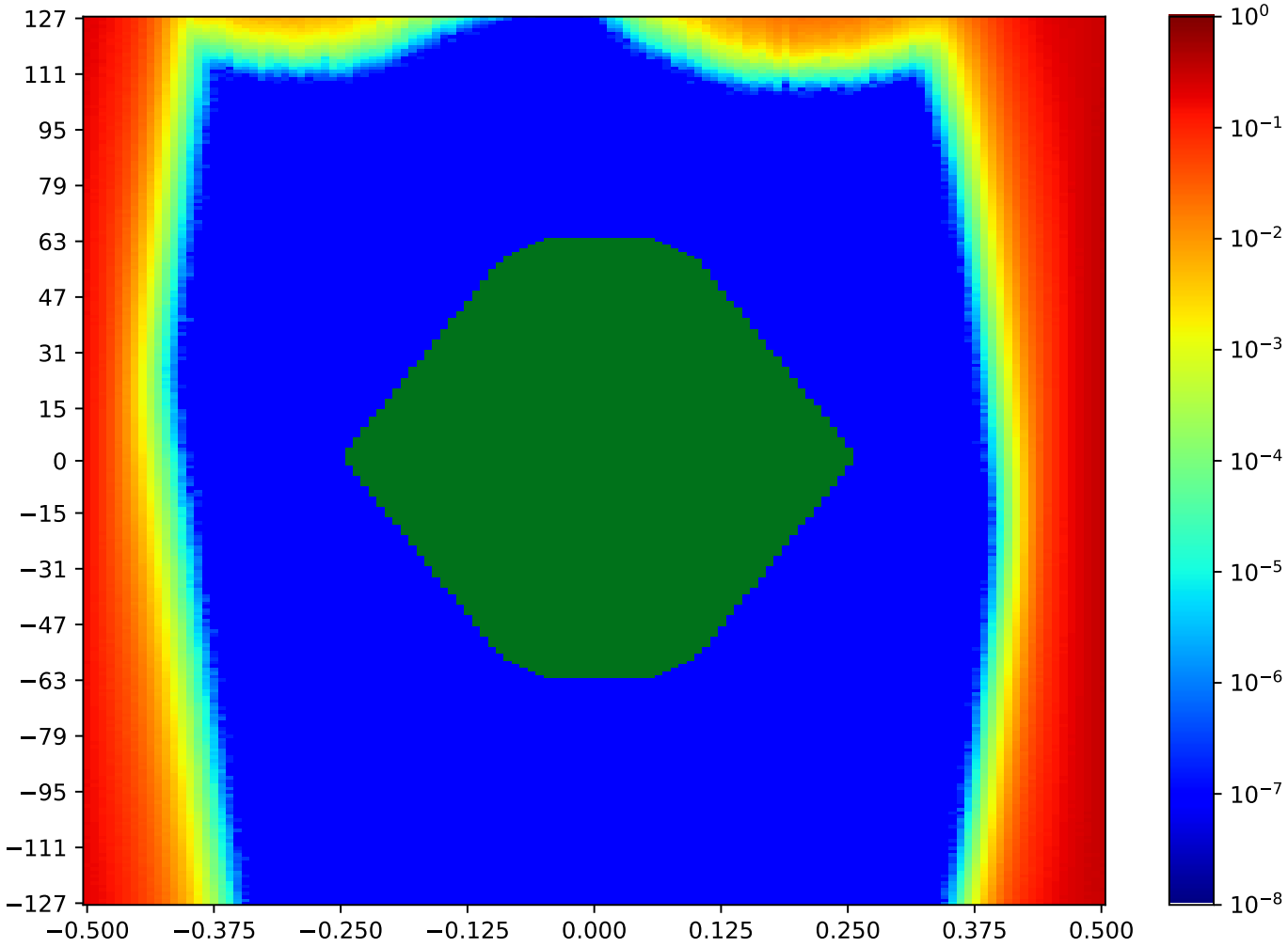


Figure 5.136: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.10 MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Table 5.127: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:25:21		2019-Nov-26 12:26:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24191	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

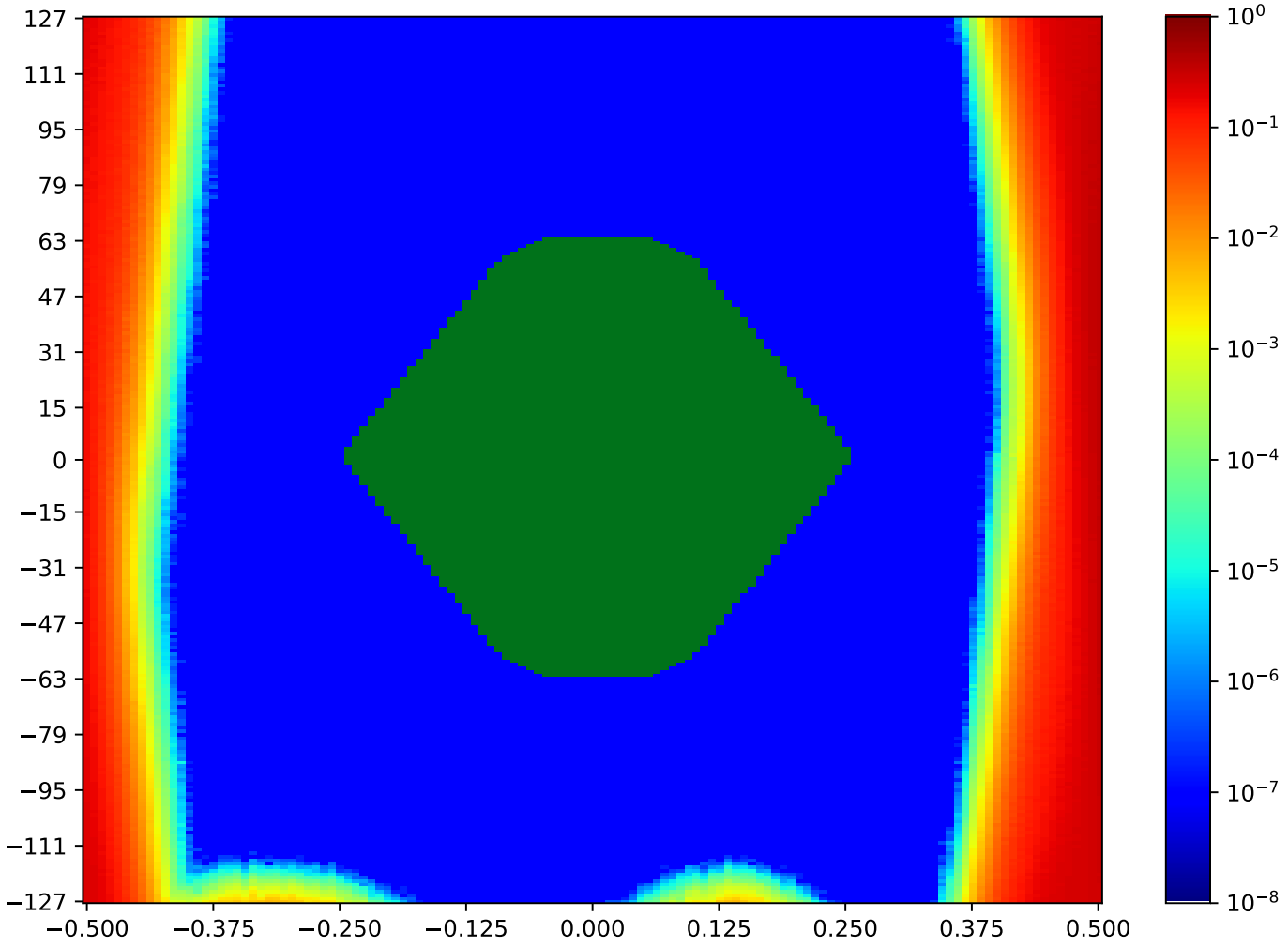


Figure 5.137: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.11 MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Table 5.128: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:29:51		2019-Nov-26 12:31:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24432	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

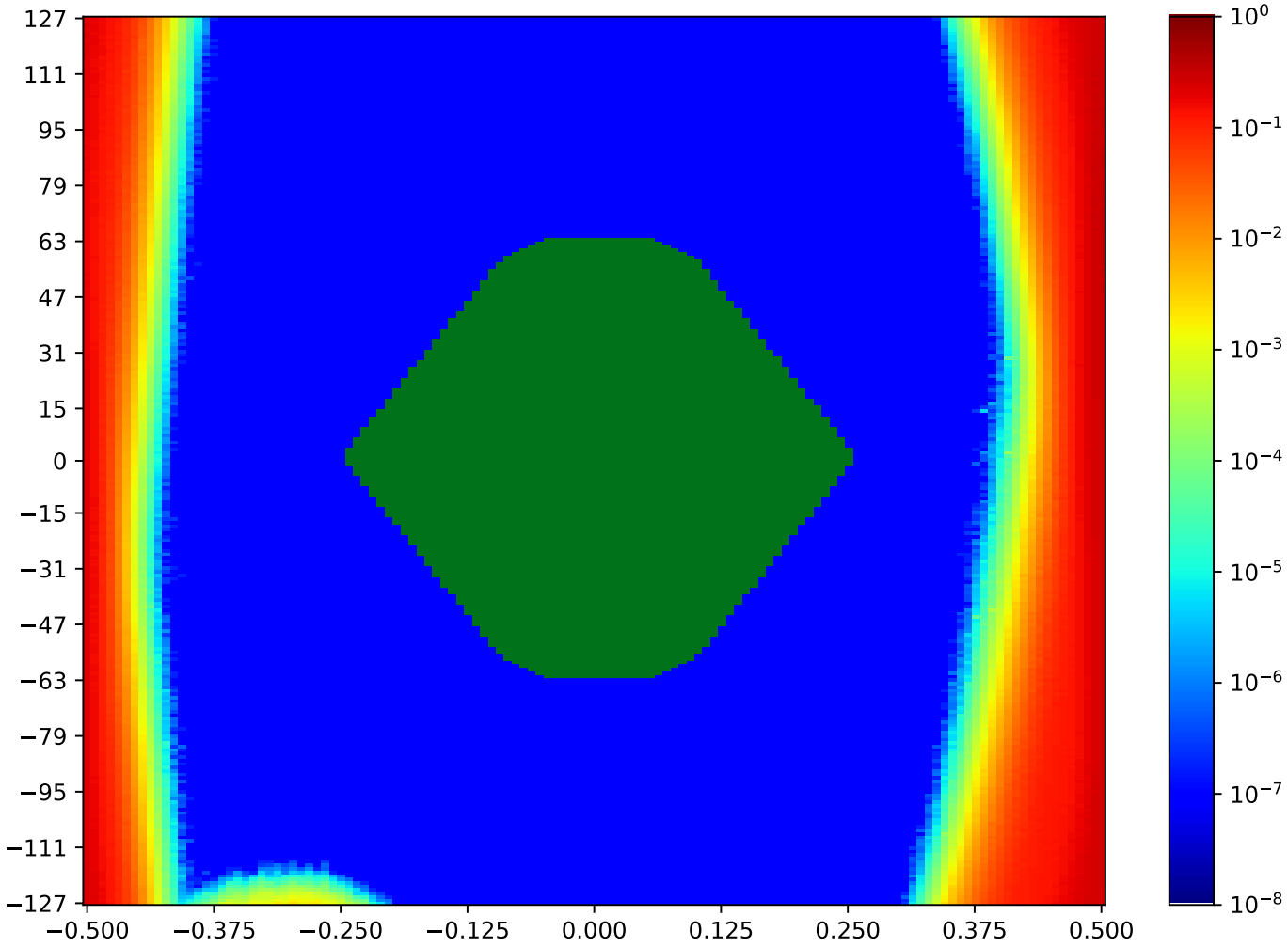


Figure 5.138: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.10.12 MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Table 5.129: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:28:43		2019-Nov-26 12:29:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22236	99	76.74%	239	93.73%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

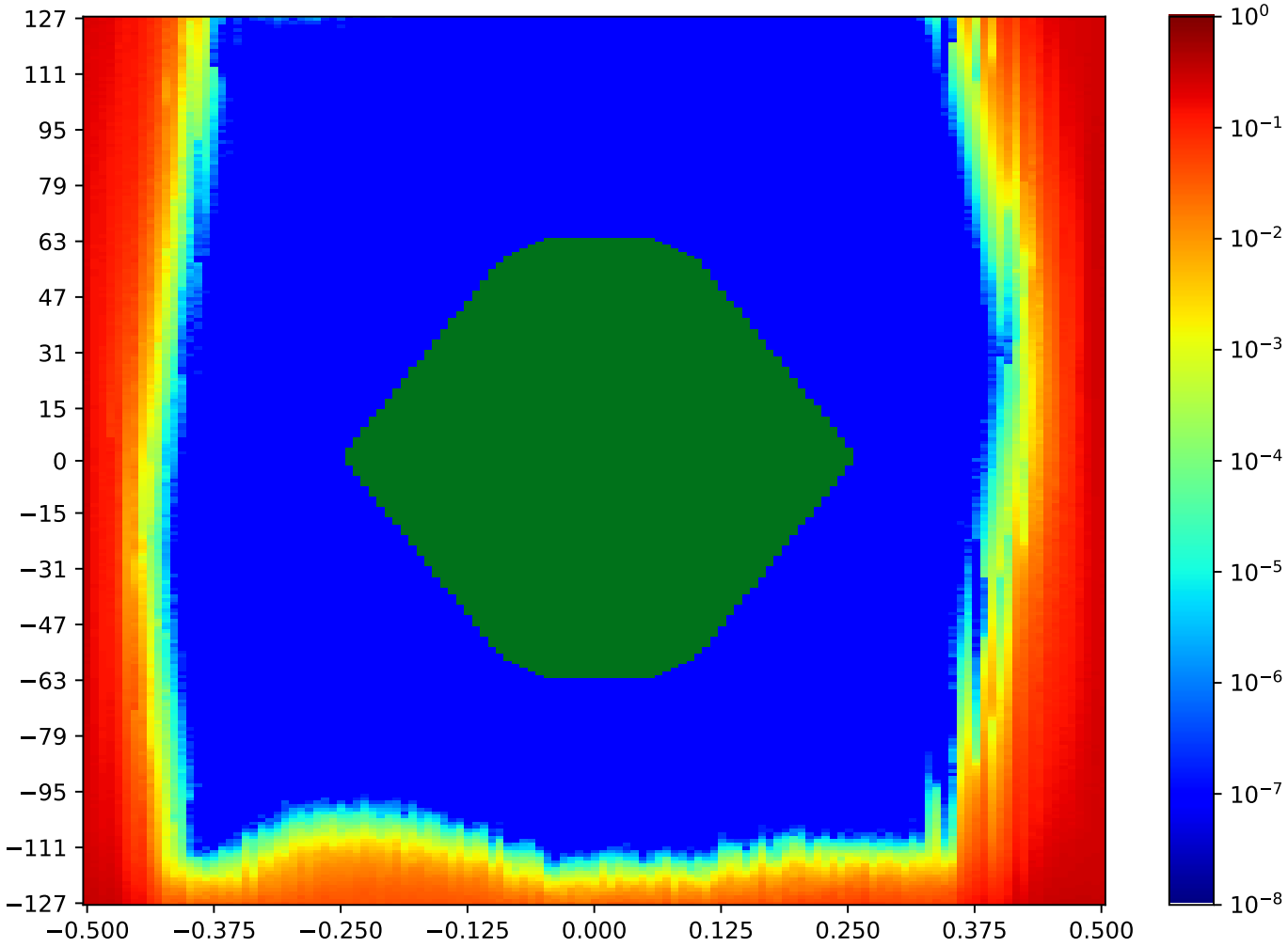


Figure 5.139: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11 MSP_A TX2 MSP_C RX18 Minipod Loopback

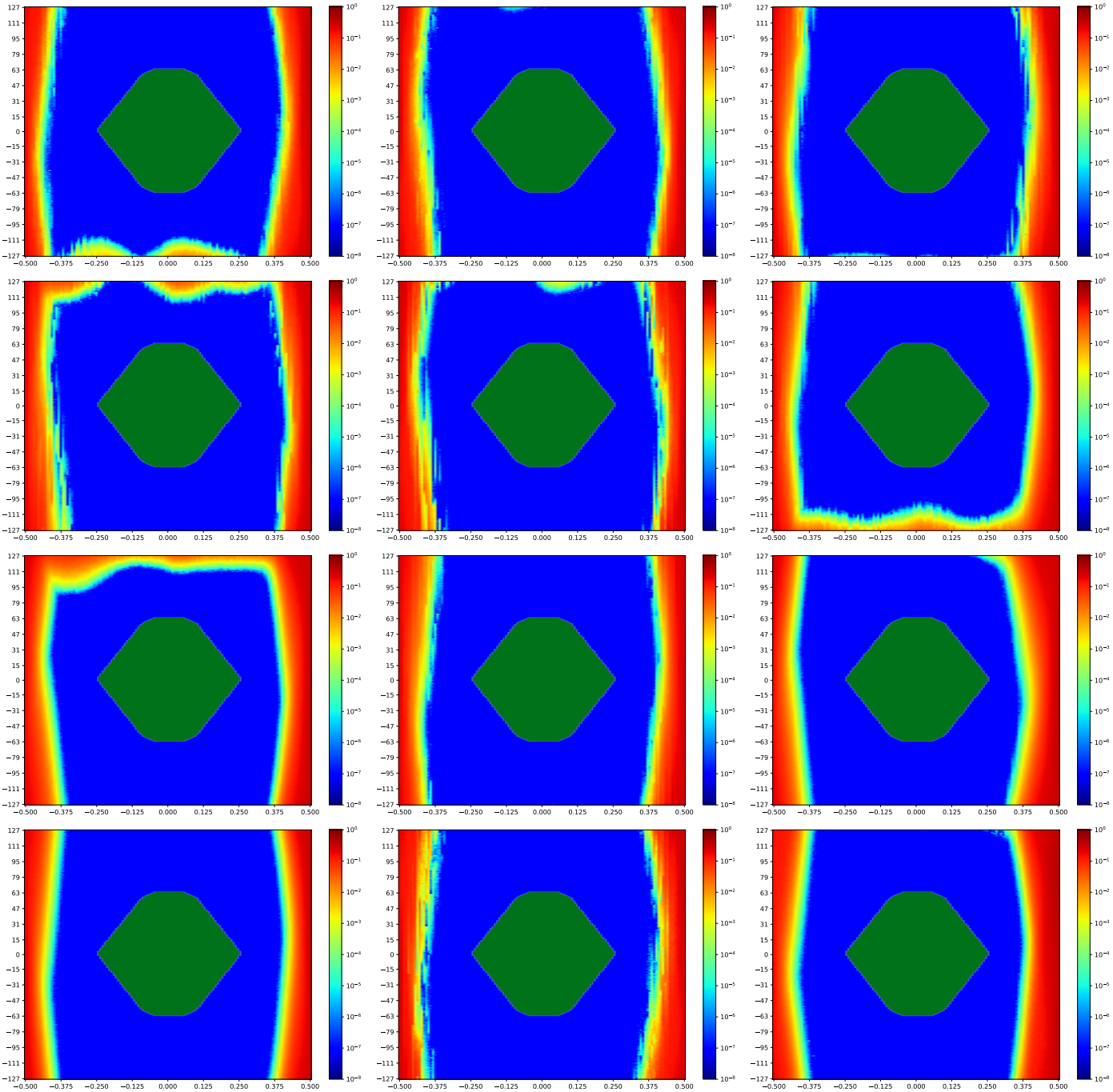


Figure 5.140: MSP_A TX2 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.153.

5.11.1 MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Table 5.130: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:38:12		2019-Nov-26 12:39:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23310	101	78.29%	236	92.55%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

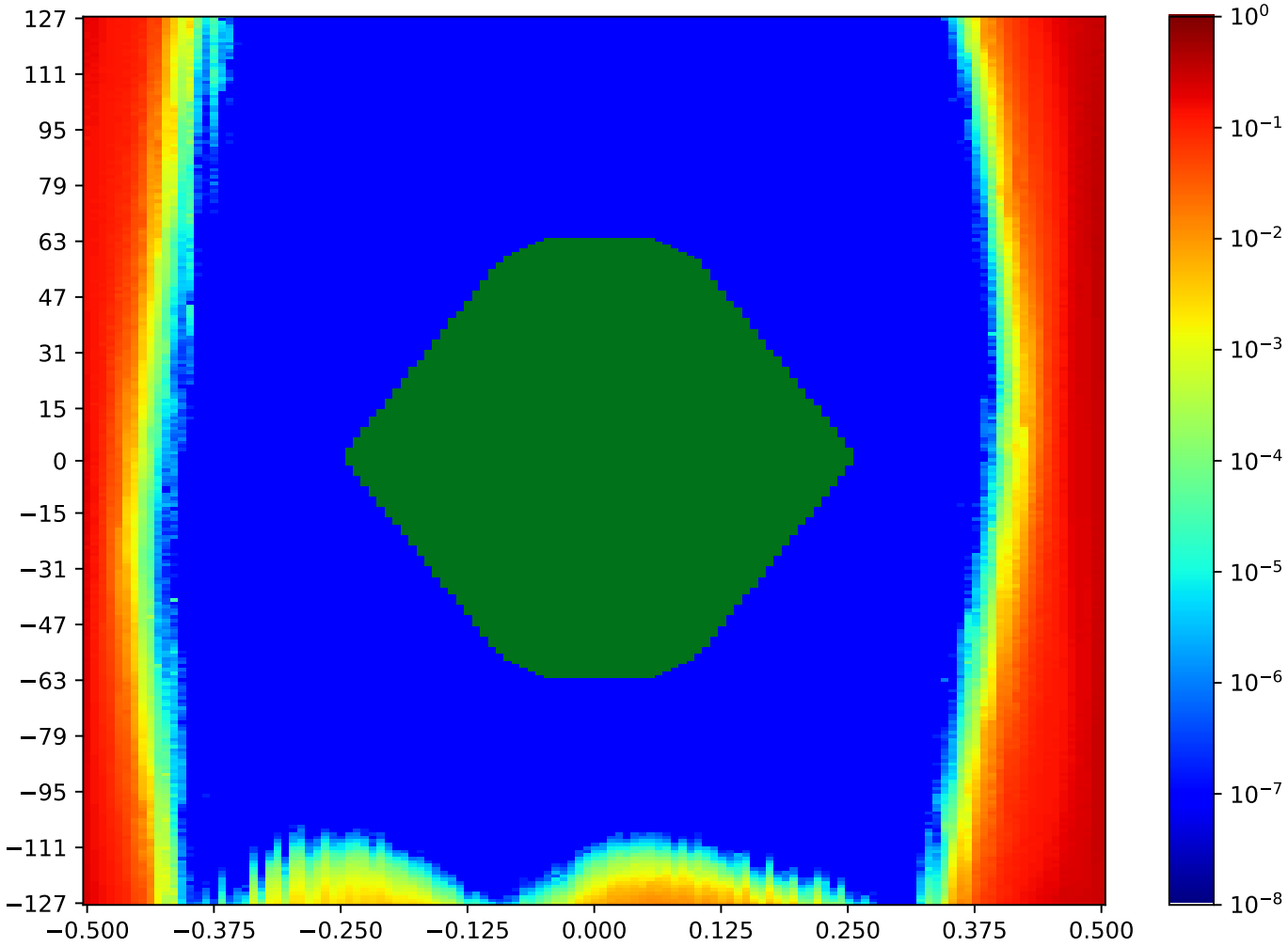


Figure 5.141: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.2 MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Table 5.131: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:35:57		2019-Nov-26 12:37:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24276	99	76.74%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

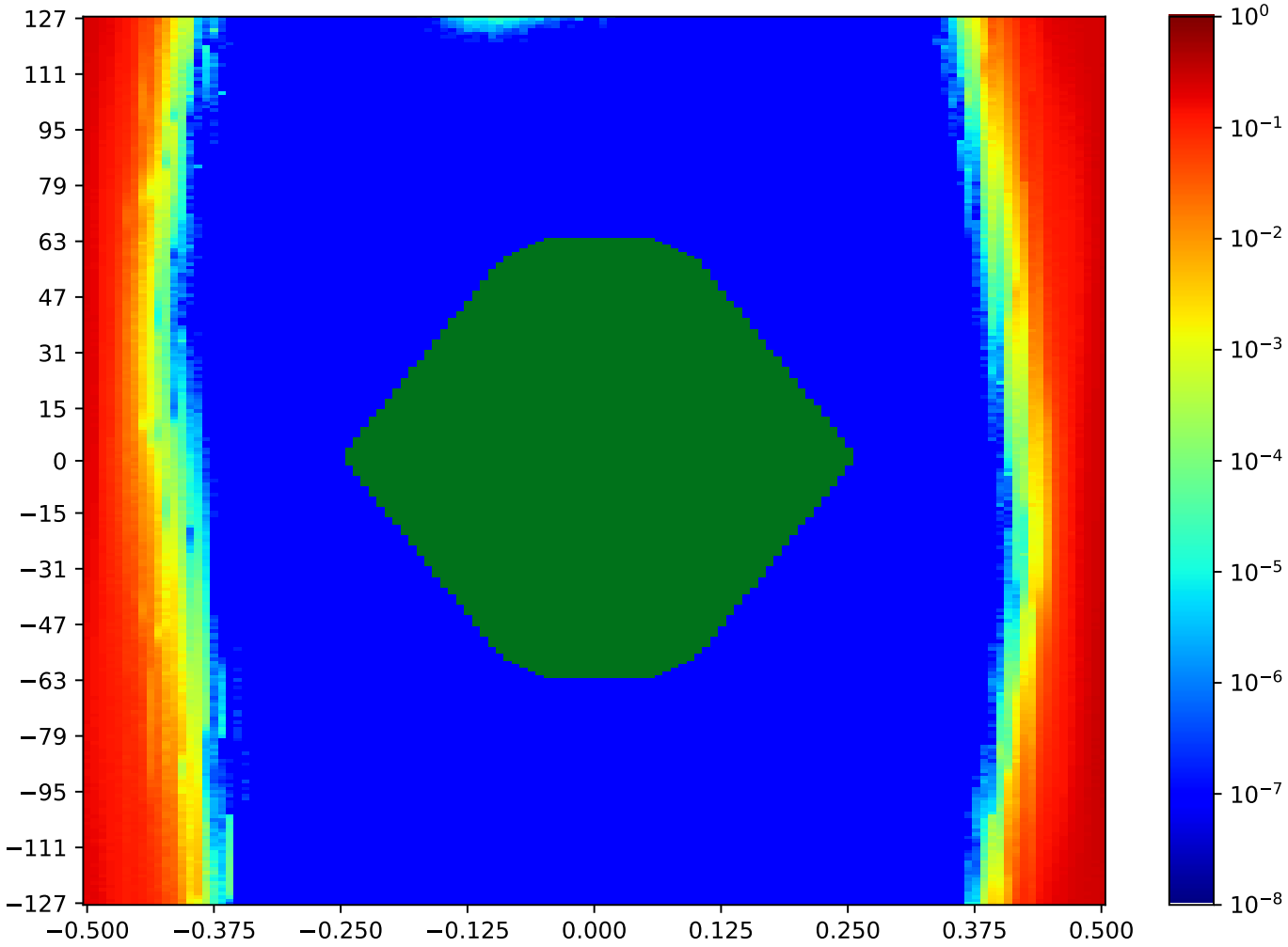


Figure 5.142: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.3 MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Table 5.132: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:41:35		2019-Nov-26 12:42:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23844	99	76.74%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

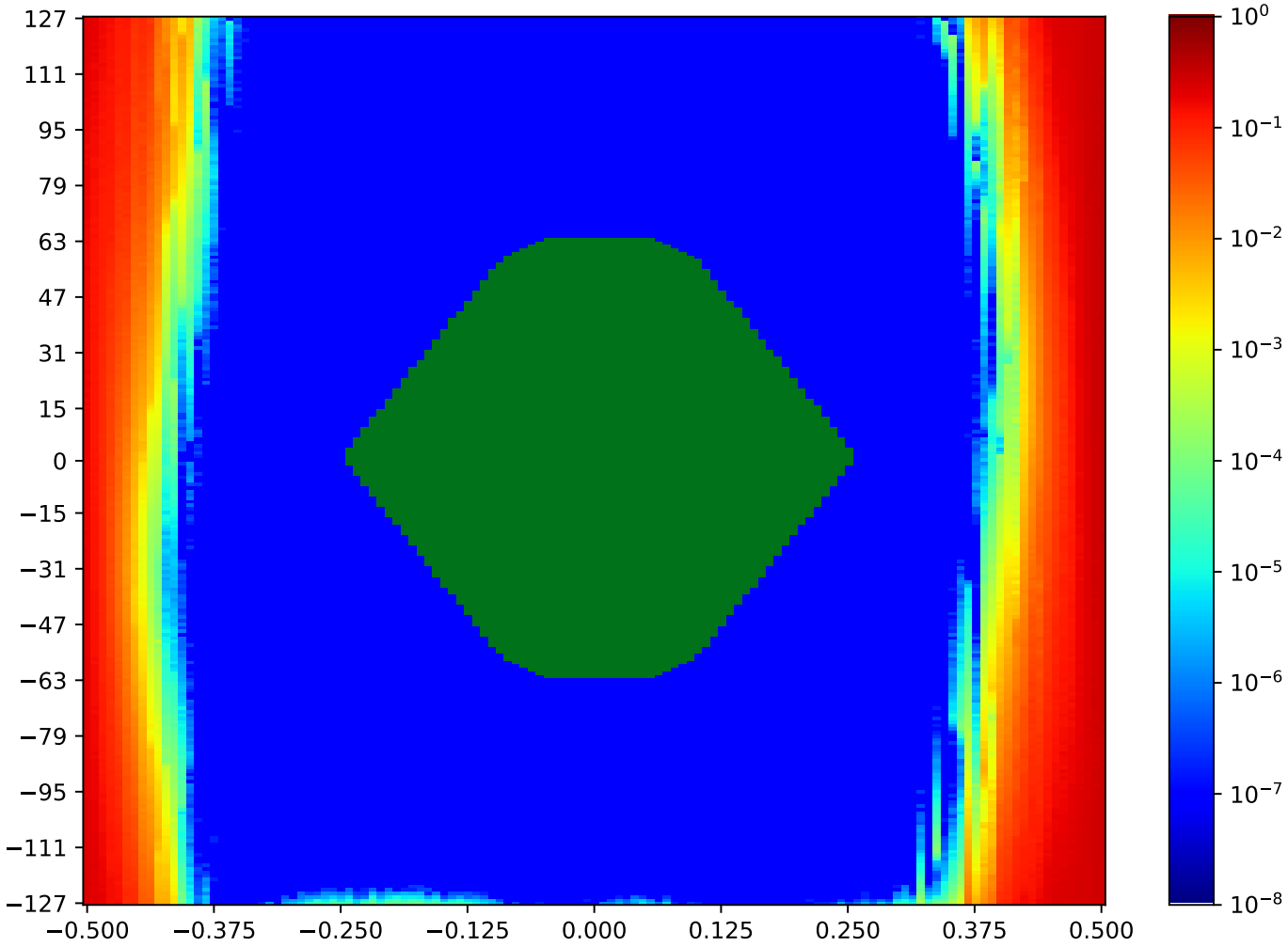


Figure 5.143: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.4 MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Table 5.133: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:34:35		2019-Nov-26 12:35:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22887	101	76.74%	232	90.98%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

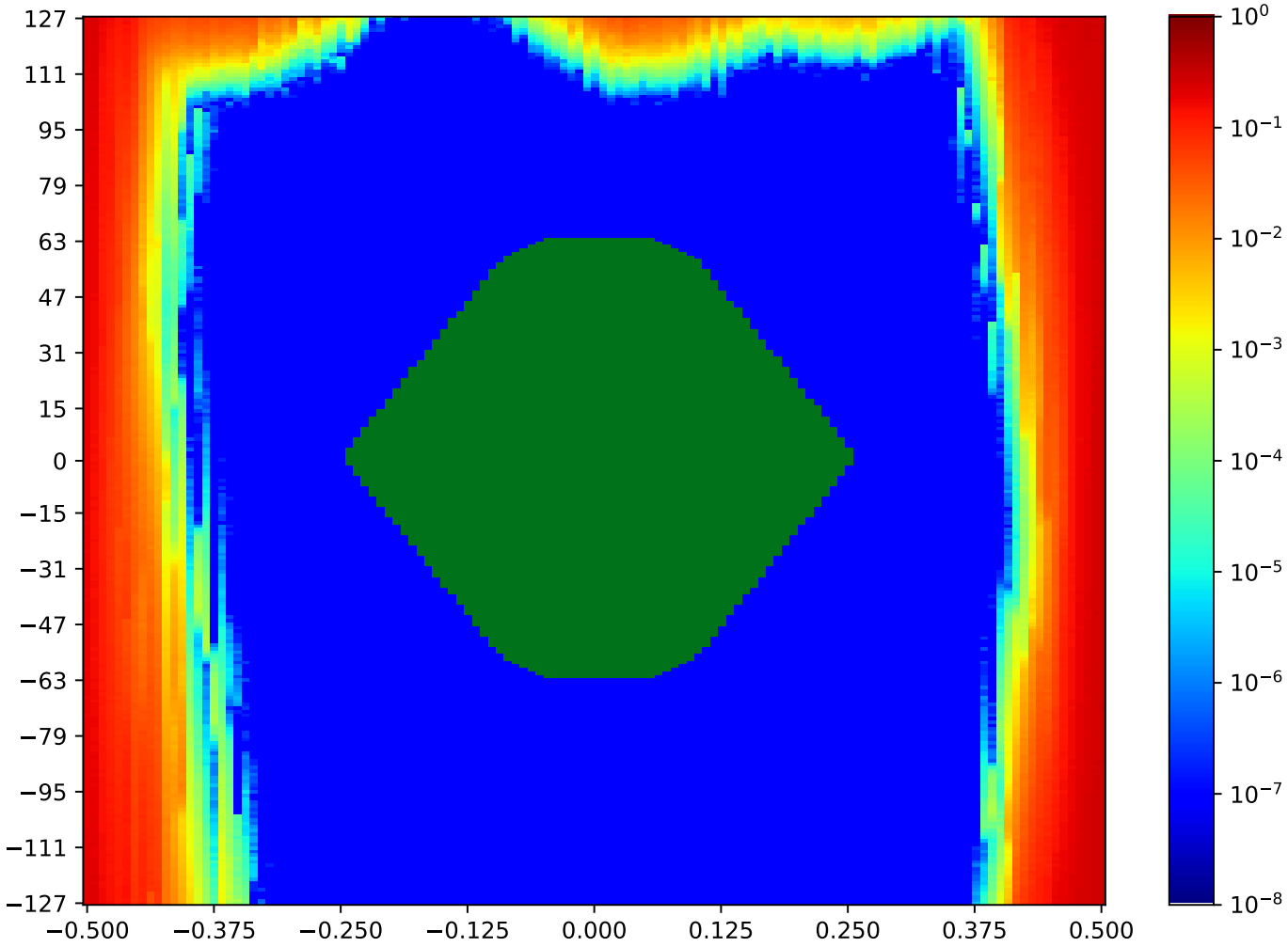


Figure 5.144: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.5 MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Table 5.134: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:44:57		2019-Nov-26 12:46:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24087	98	75.97%	244	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

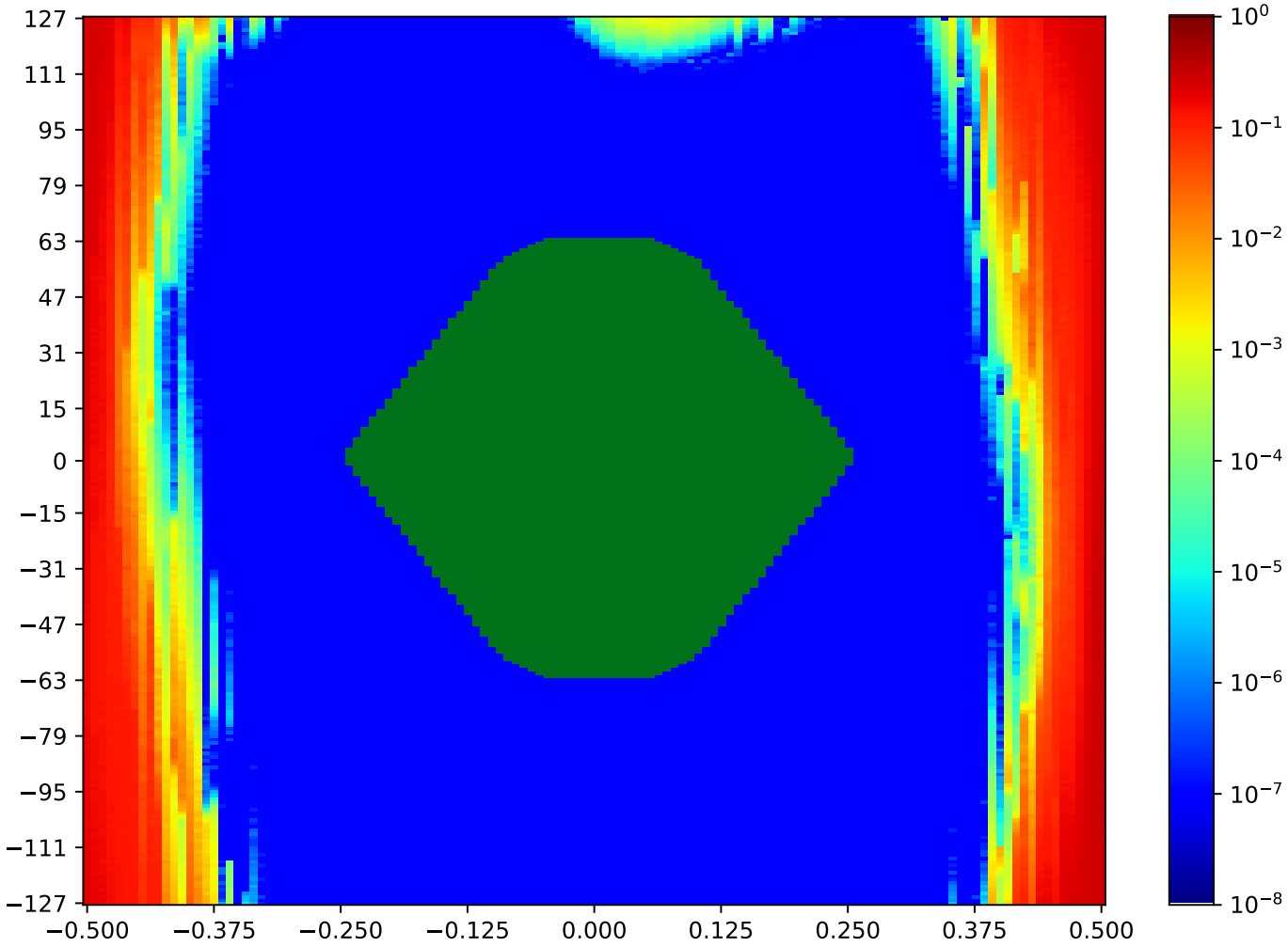


Figure 5.145: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.6 MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Table 5.135: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:37:05		2019-Nov-26 12:38:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22215	100	77.52%	227	89.02%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

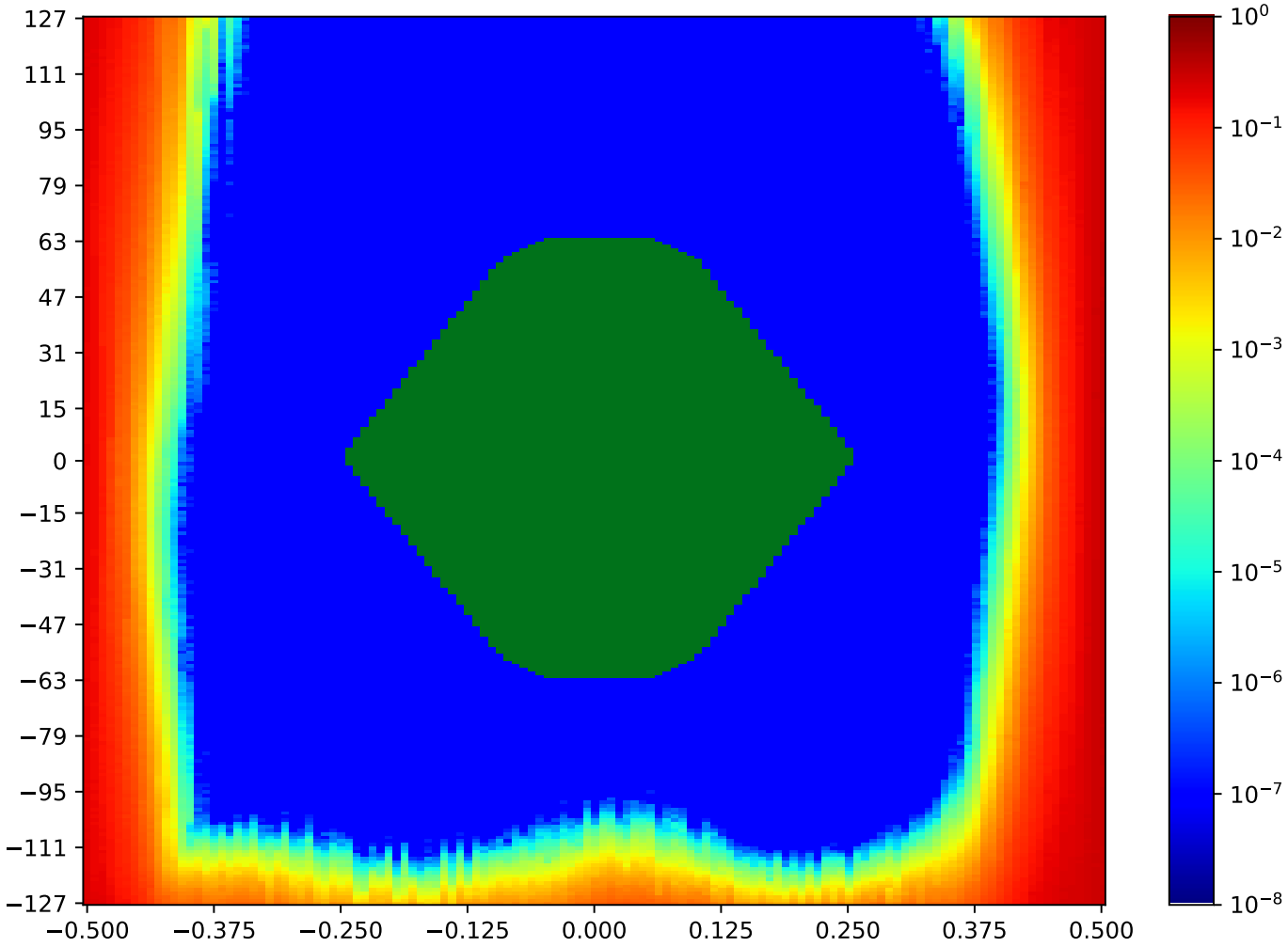


Figure 5.146: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.7 MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Table 5.136: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:47:13		2019-Nov-26 12:48:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22062	98	75.97%	235	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

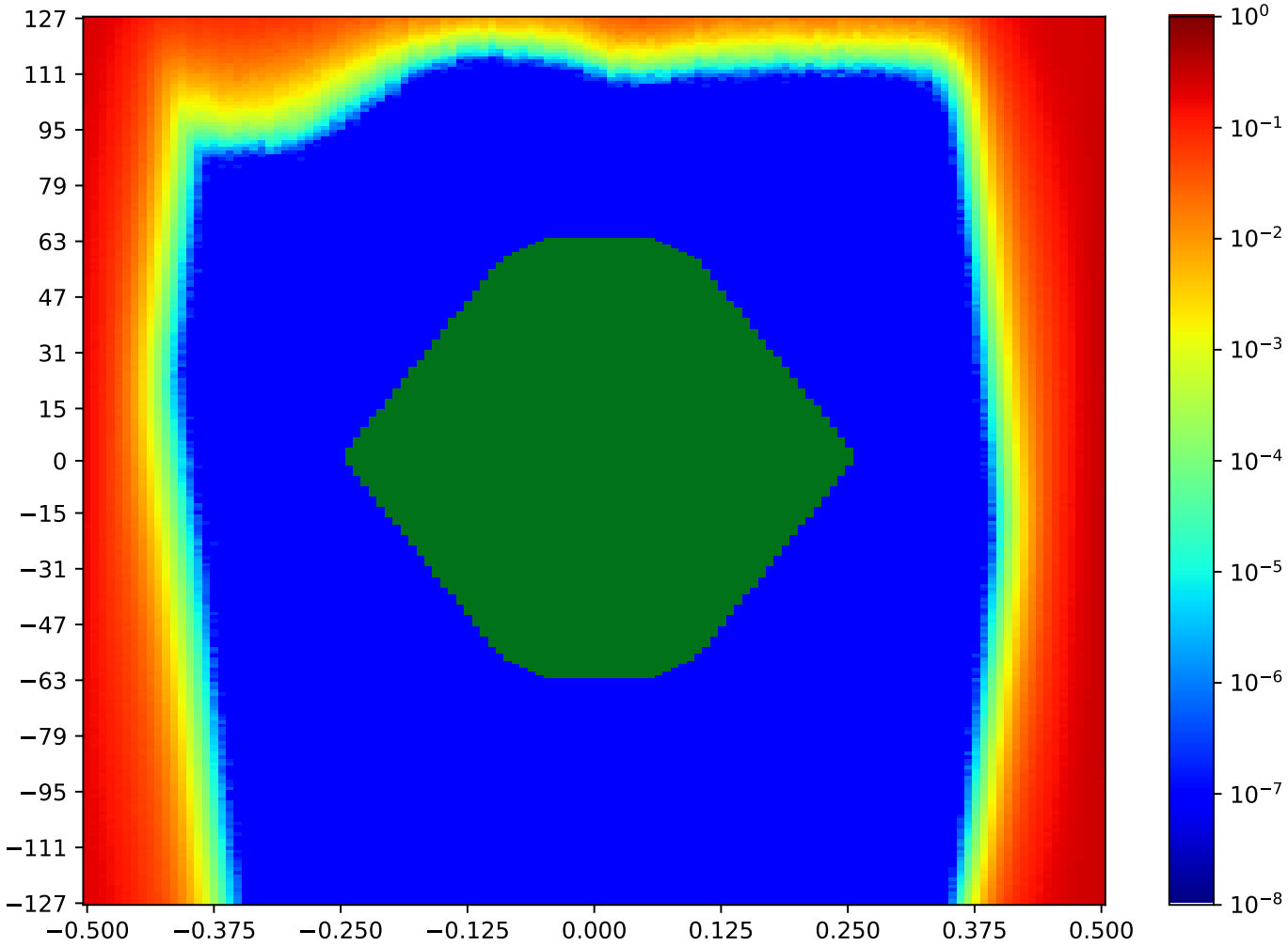


Figure 5.147: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.8 MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Table 5.137: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:39:20		2019-Nov-26 12:40:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24290	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

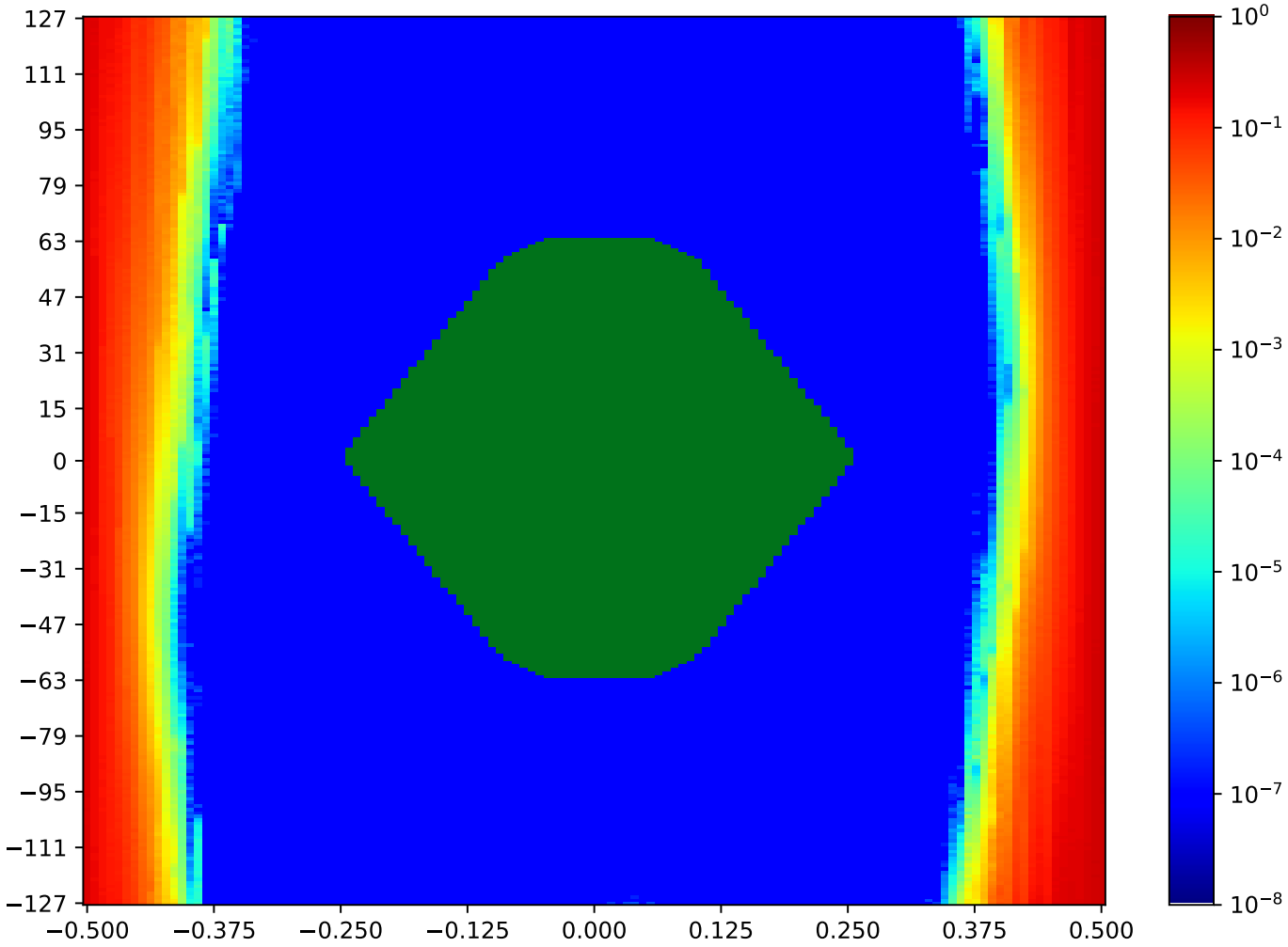


Figure 5.148: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.9 MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Table 5.138: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:46:05		2019-Nov-26 12:47:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22923	95	73.64%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

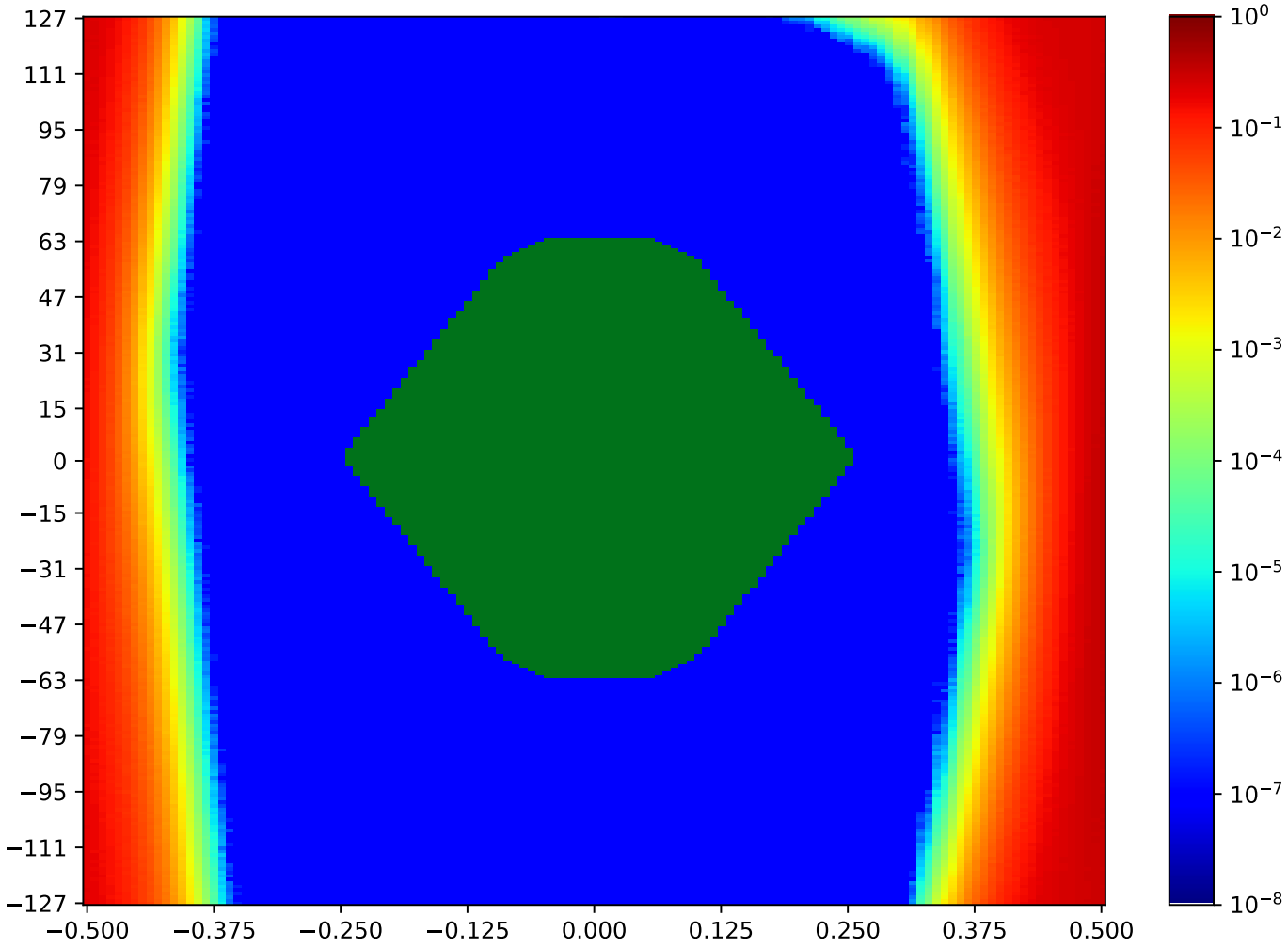


Figure 5.149: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.10 MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Table 5.139: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:40:28		2019-Nov-26 12:41:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24491	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

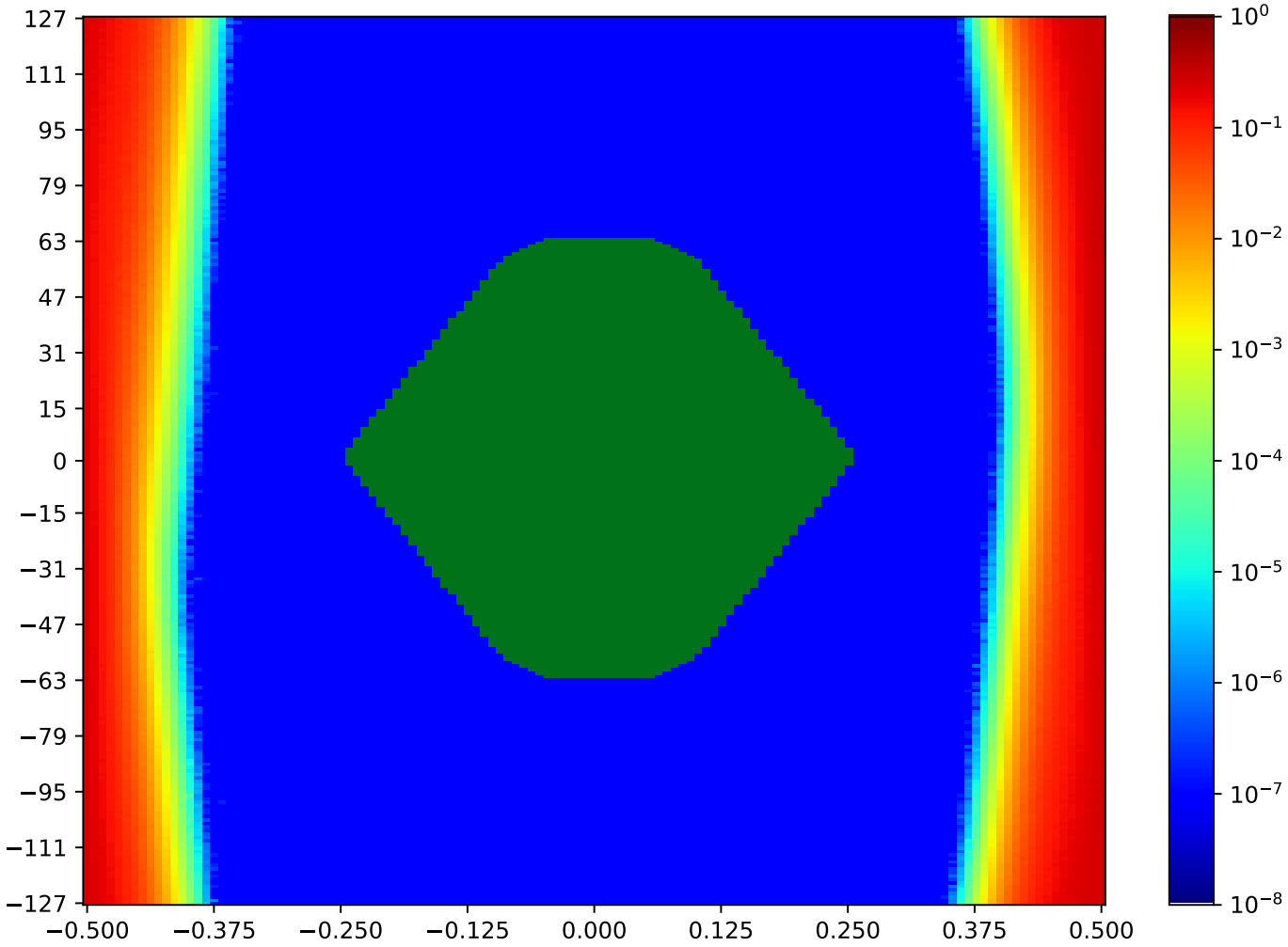


Figure 5.150: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.11 MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Table 5.140: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:43:50		2019-Nov-26 12:44:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23992	98	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

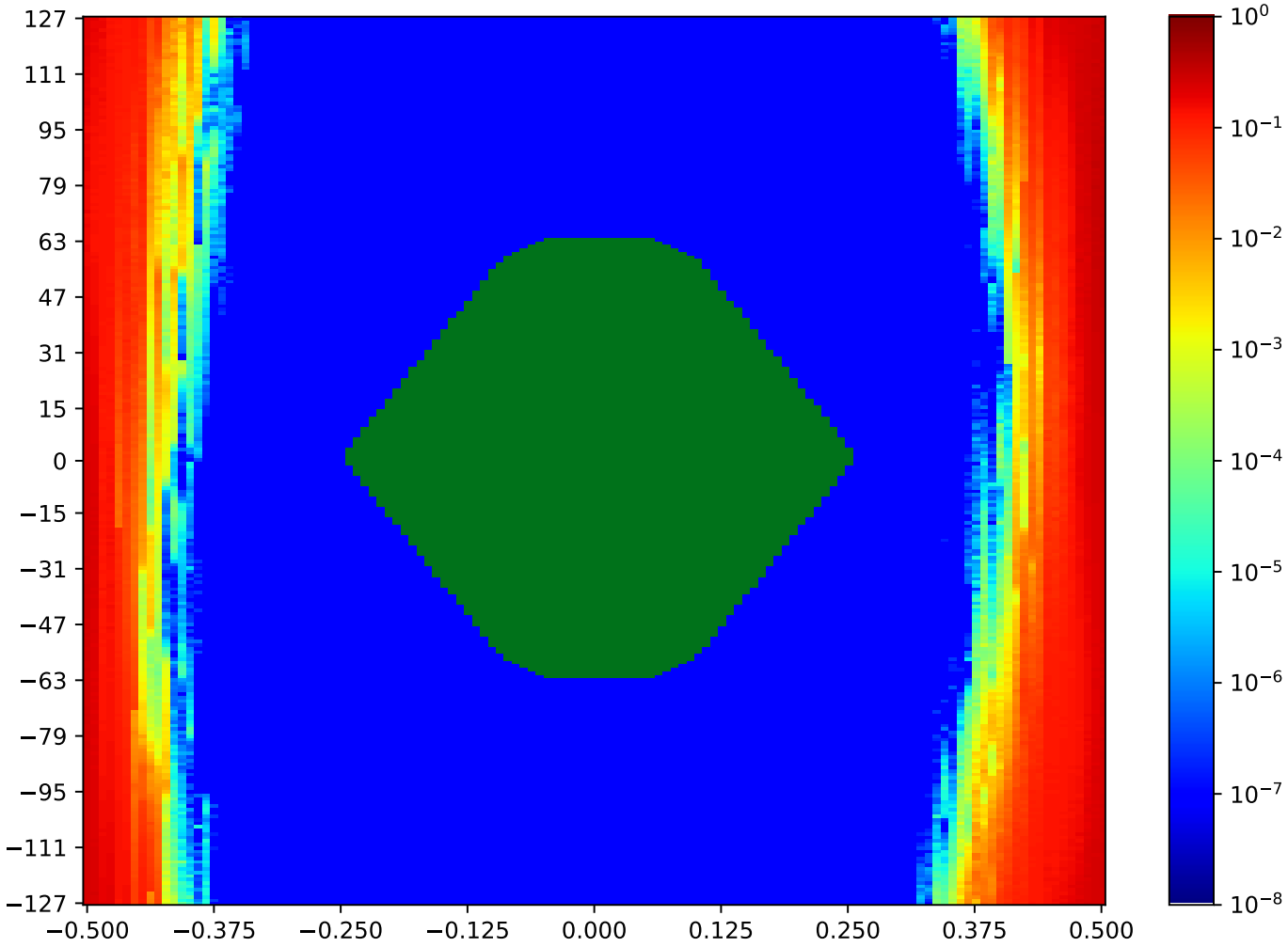


Figure 5.151: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.11.12 MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Table 5.141: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:42:43		2019-Nov-26 12:43:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23298	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

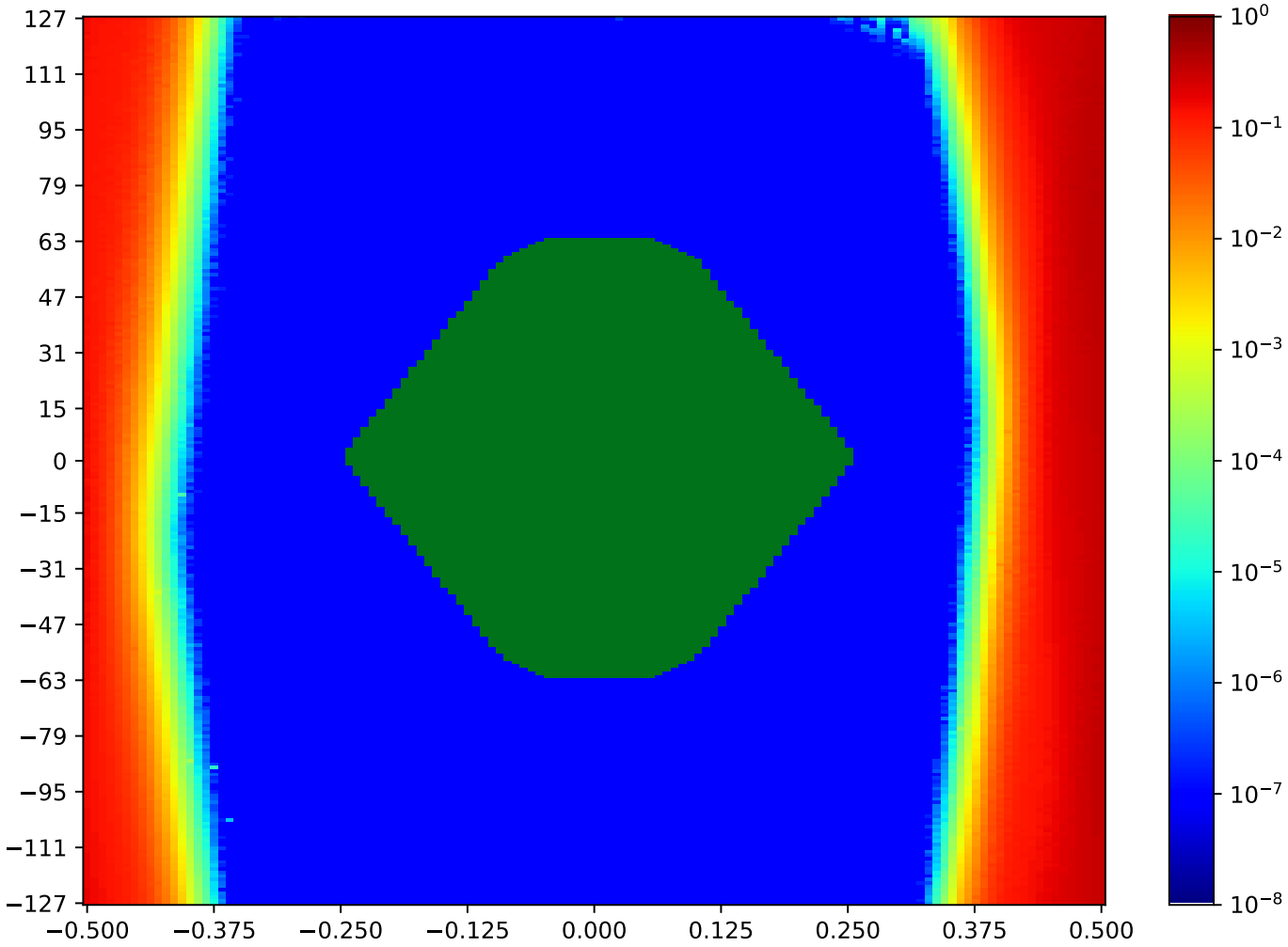


Figure 5.152: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12 MSP_C TX3 MSP_A RX8 Minipod Loopback

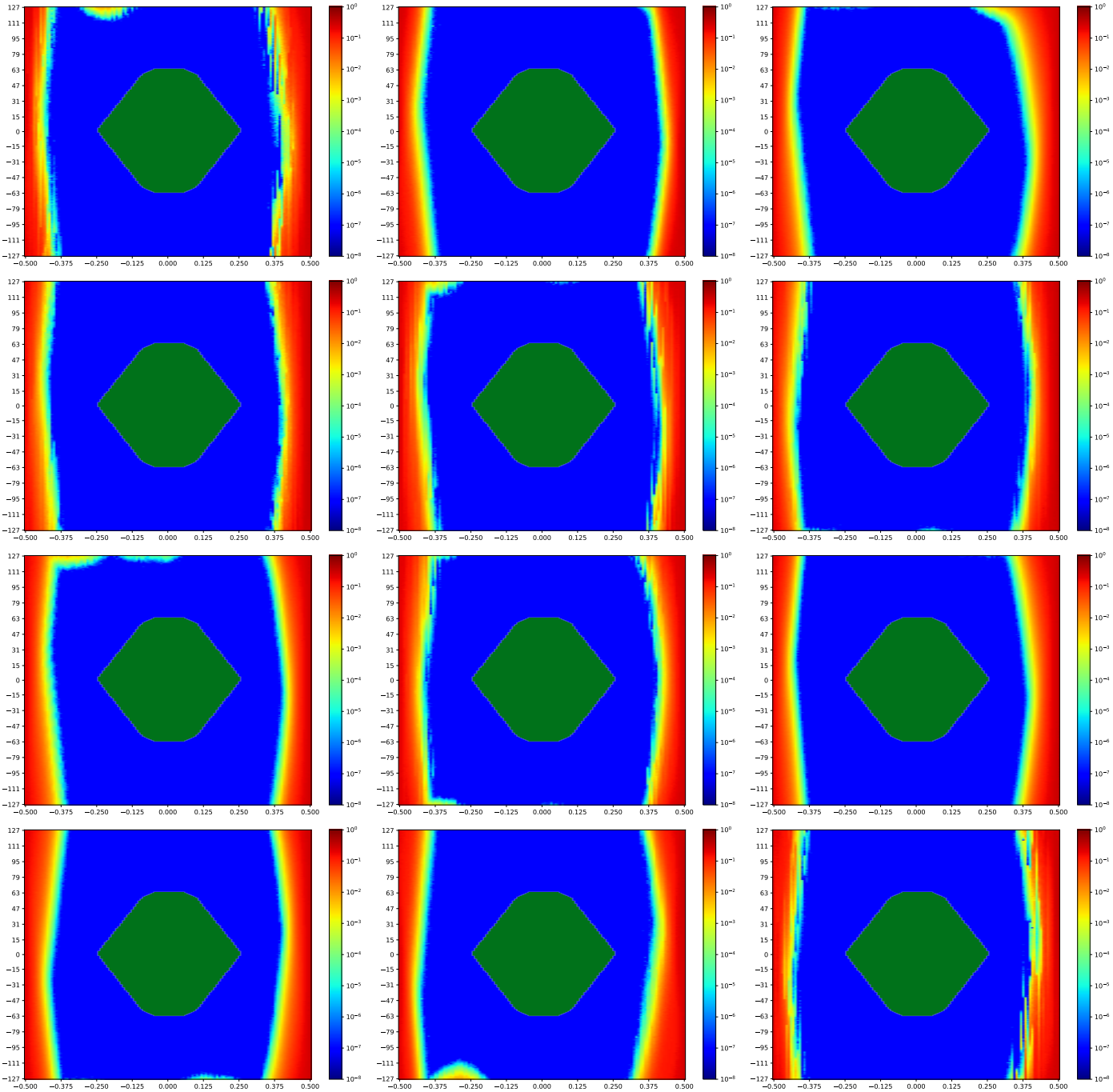


Figure 5.153: MSP_C TX3 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.166.

5.12.1 MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Table 5.142: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:52:06		2019-Nov-26 12:53:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24181	104	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

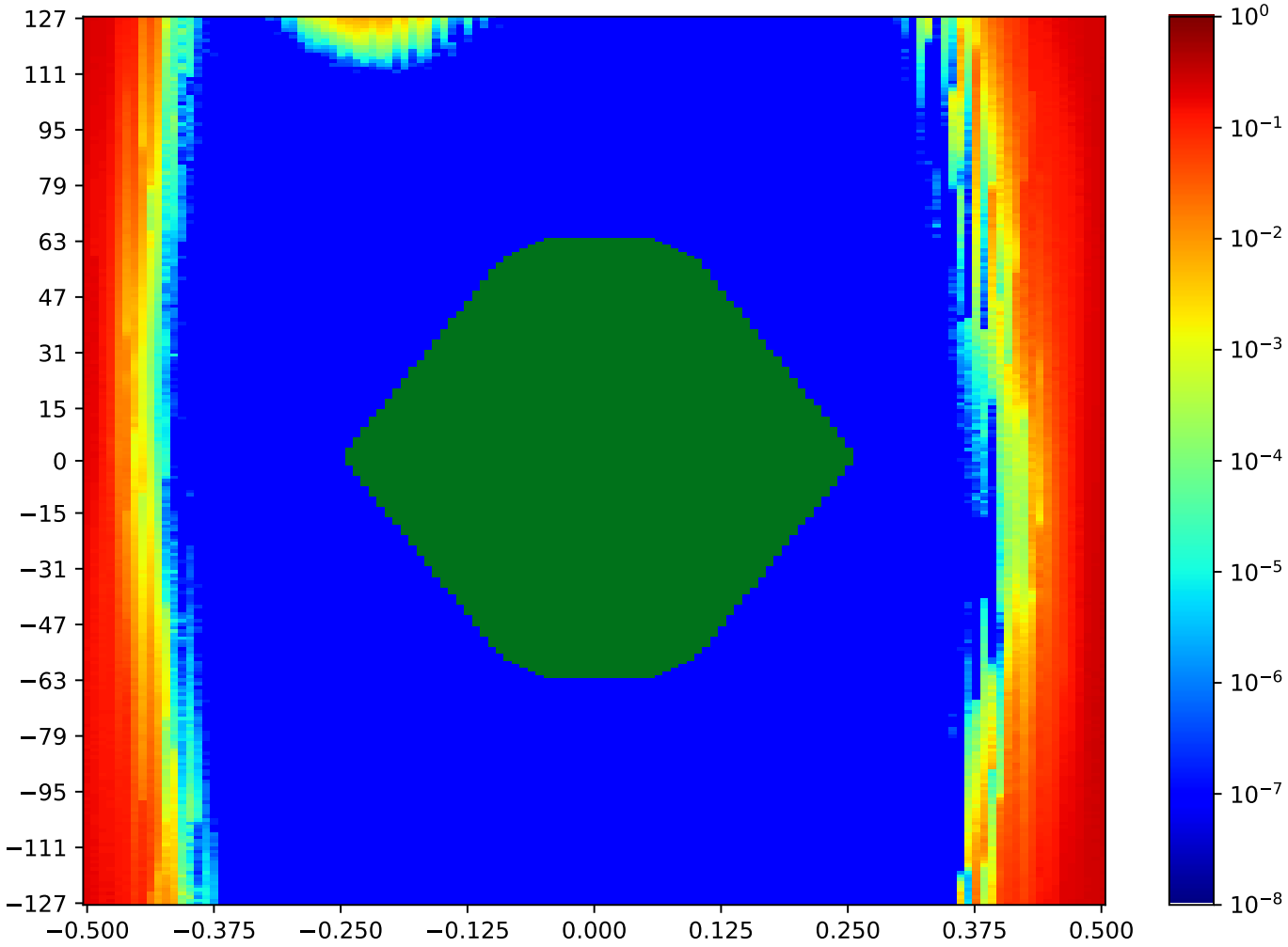


Figure 5.154: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.2 MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Table 5.143: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:54:21		2019-Nov-26 12:55:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25015	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

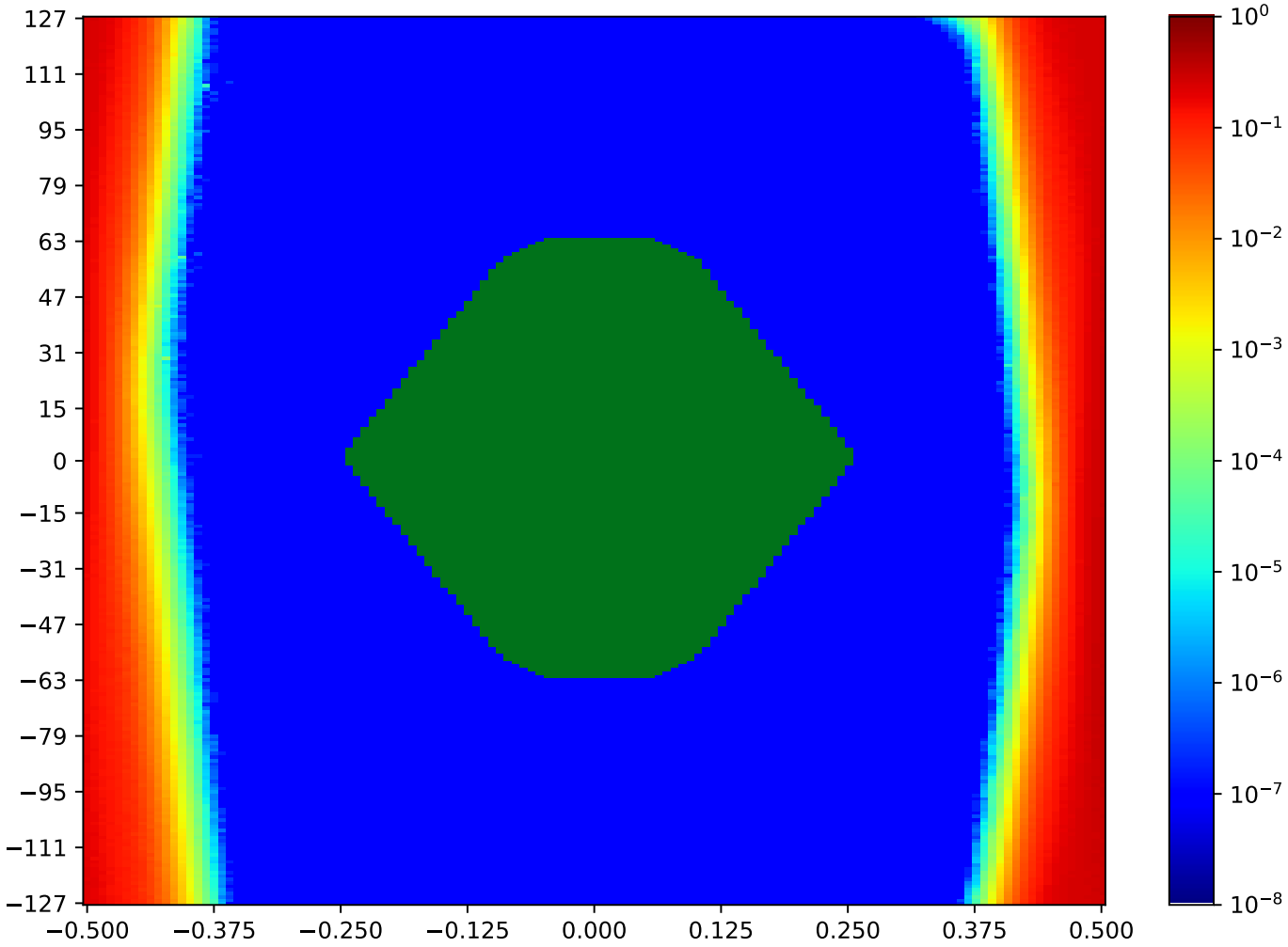


Figure 5.155: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.3 MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Table 5.144: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:55:28		2019-Nov-26 12:56:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23358	98	75.97%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

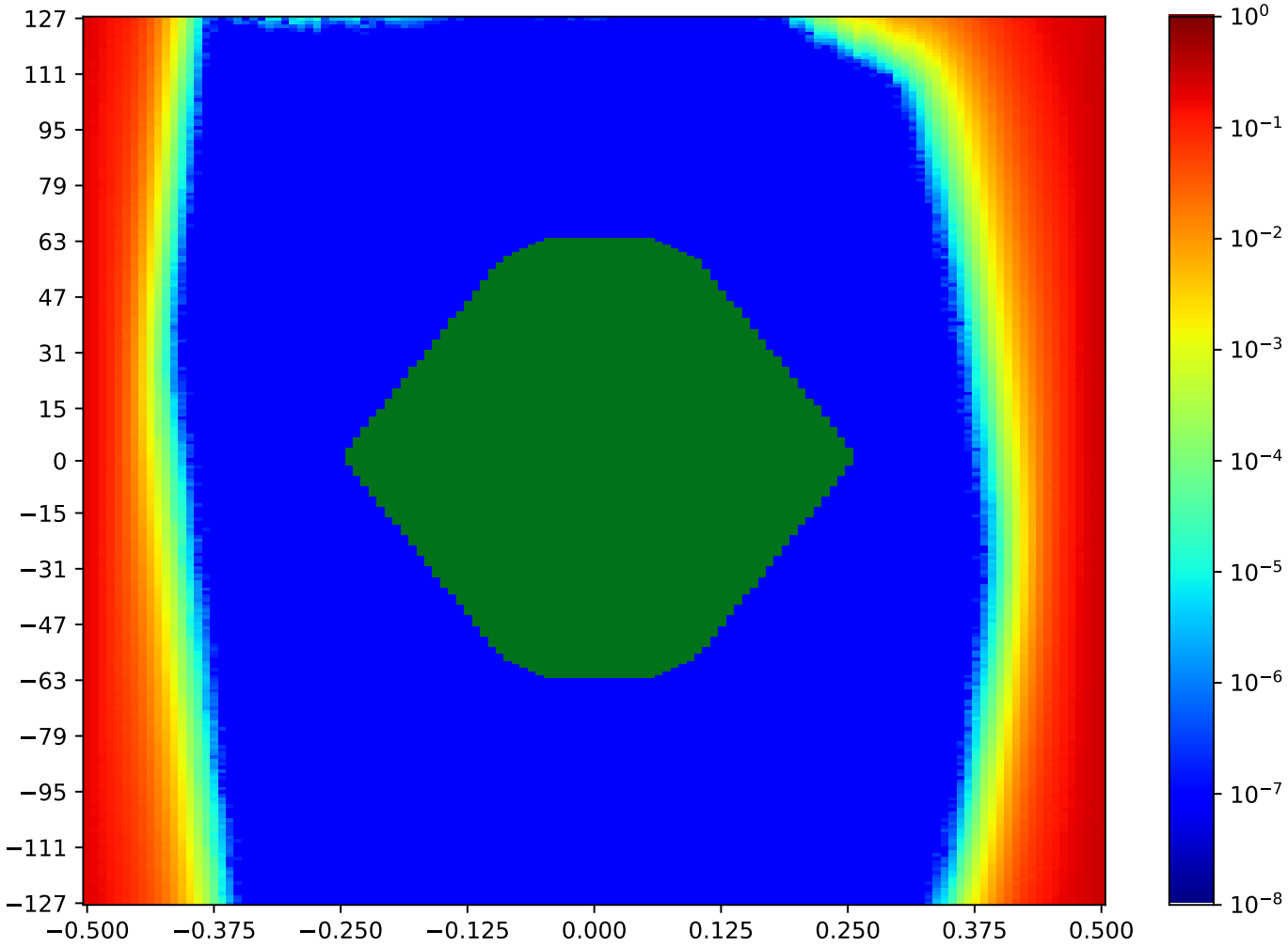


Figure 5.156: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.4 MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Table 5.145: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:49:44		2019-Nov-26 12:50:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24803	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

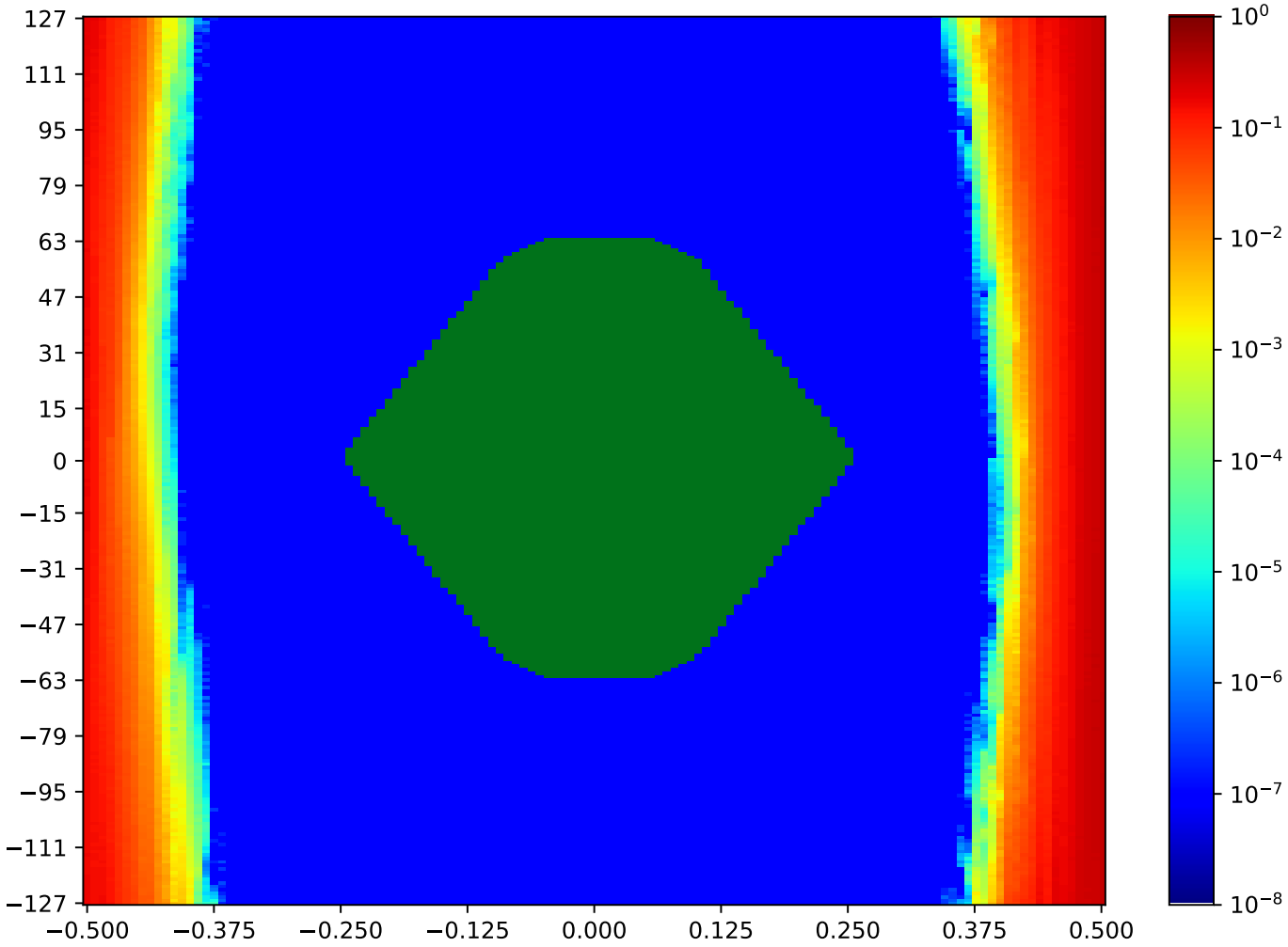


Figure 5.157: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.5 MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Table 5.146: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:59:05		2019-Nov-26 13:00:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24266	99	76.74%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

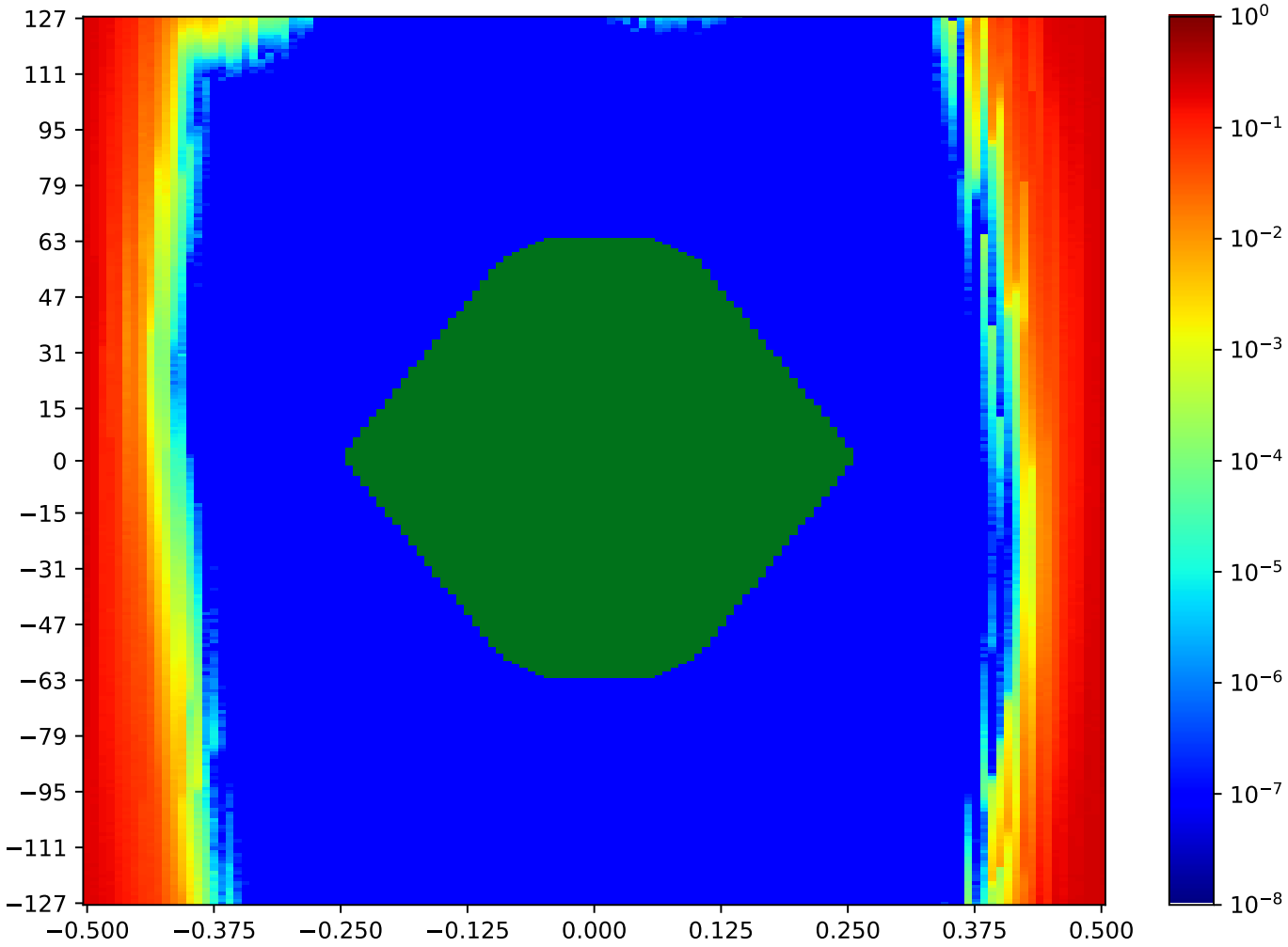


Figure 5.158: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.6 MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Table 5.147: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:48:20		2019-Nov-26 12:49:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24317	100	77.52%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

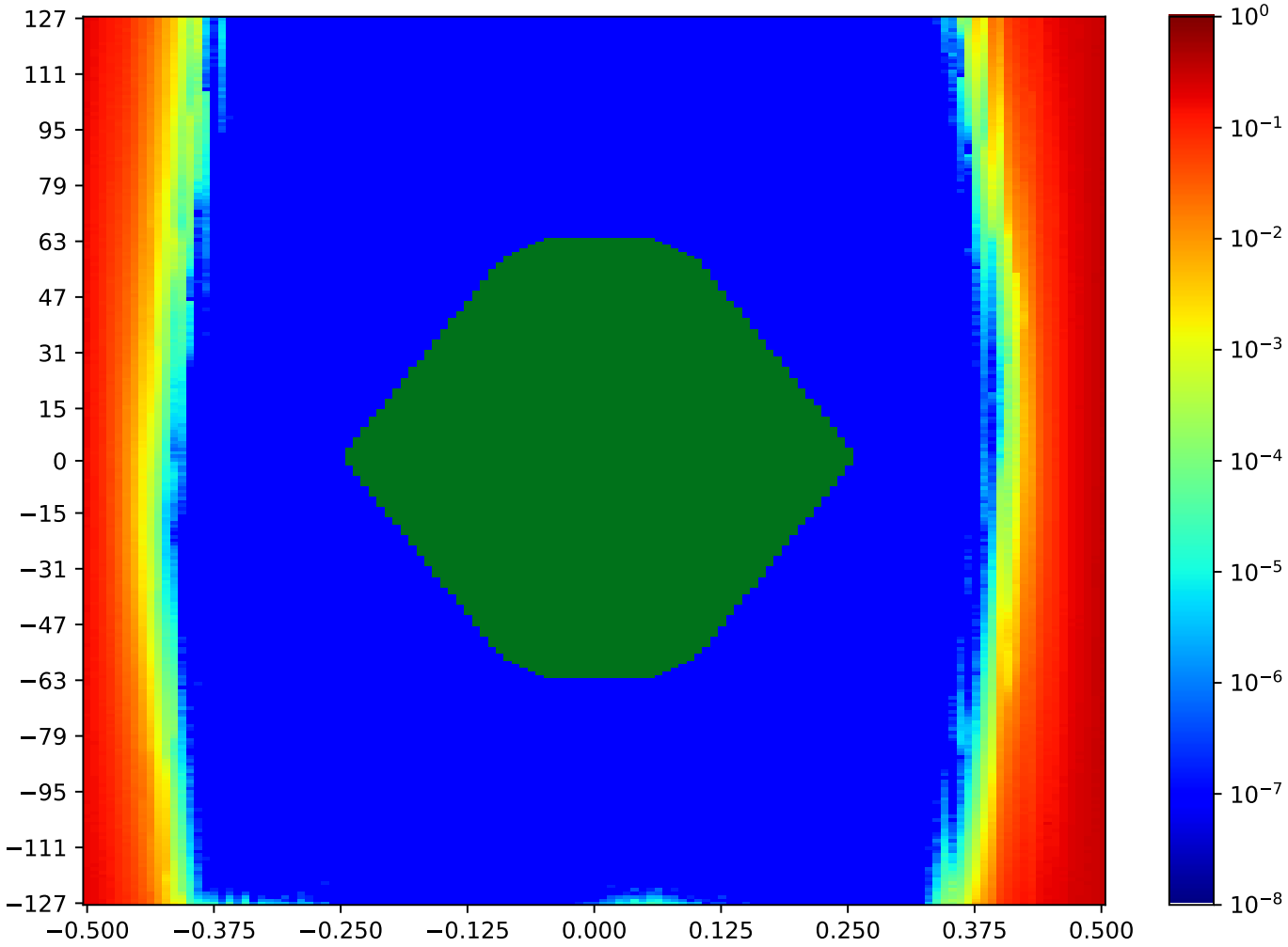


Figure 5.159: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.7 MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Table 5.148: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:01:20		2019-Nov-26 13:02:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23706	99	76.74%	244	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

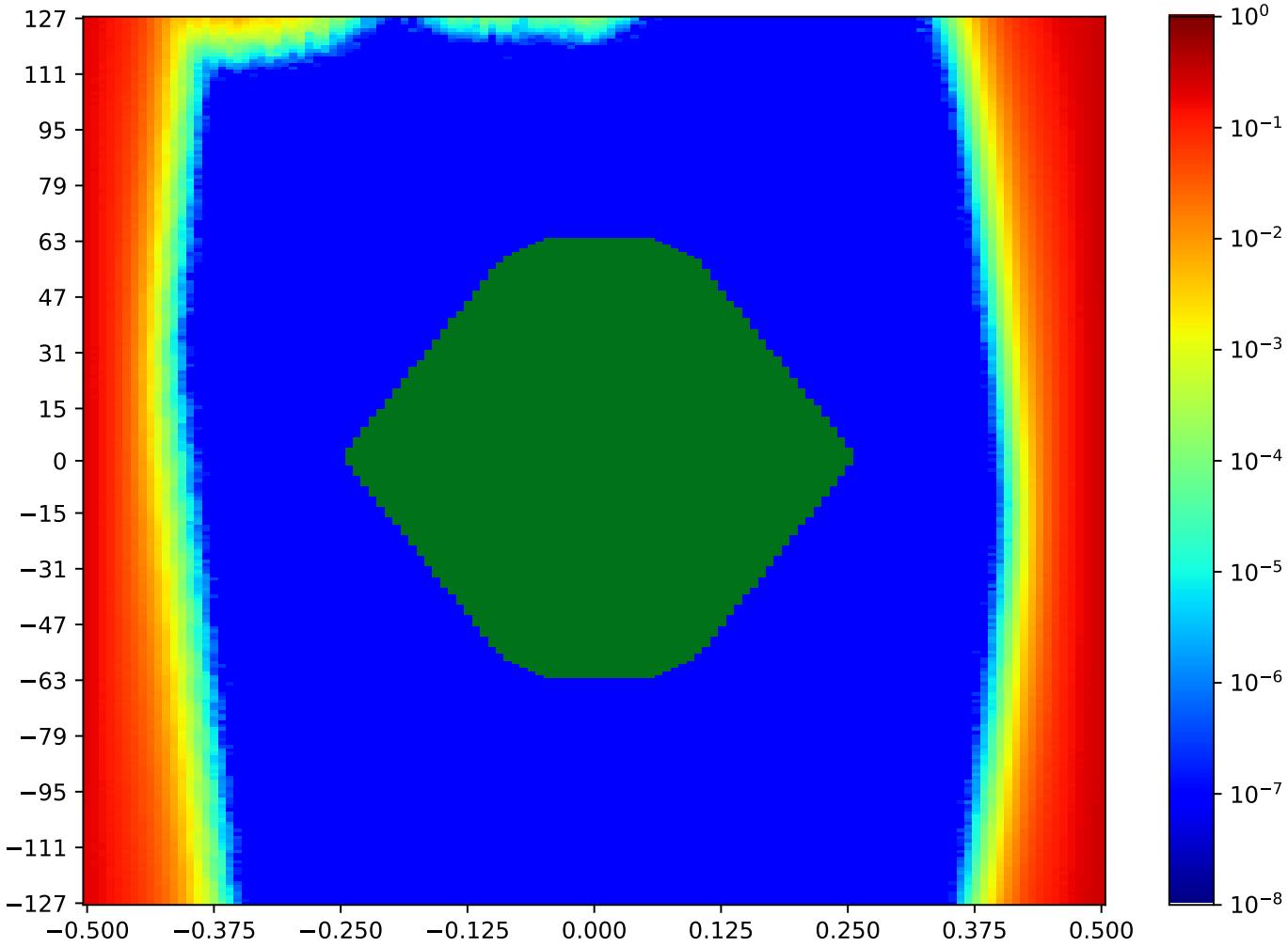


Figure 5.160: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.8 MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Table 5.149: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:50:58		2019-Nov-26 12:52:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24193	100	77.52%	250	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

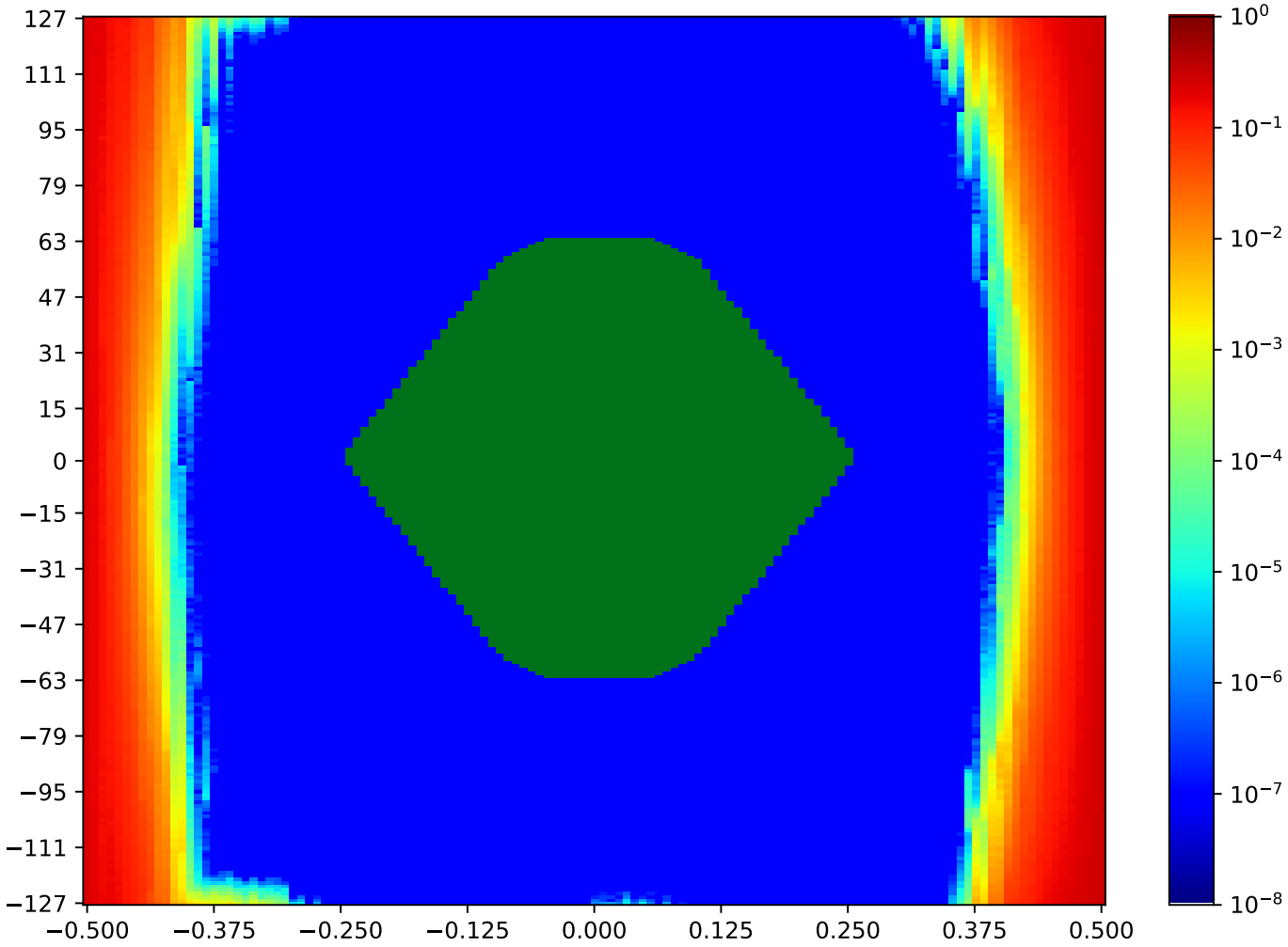


Figure 5.161: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.9 MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Table 5.150: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:00:13		2019-Nov-26 13:01:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24253	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

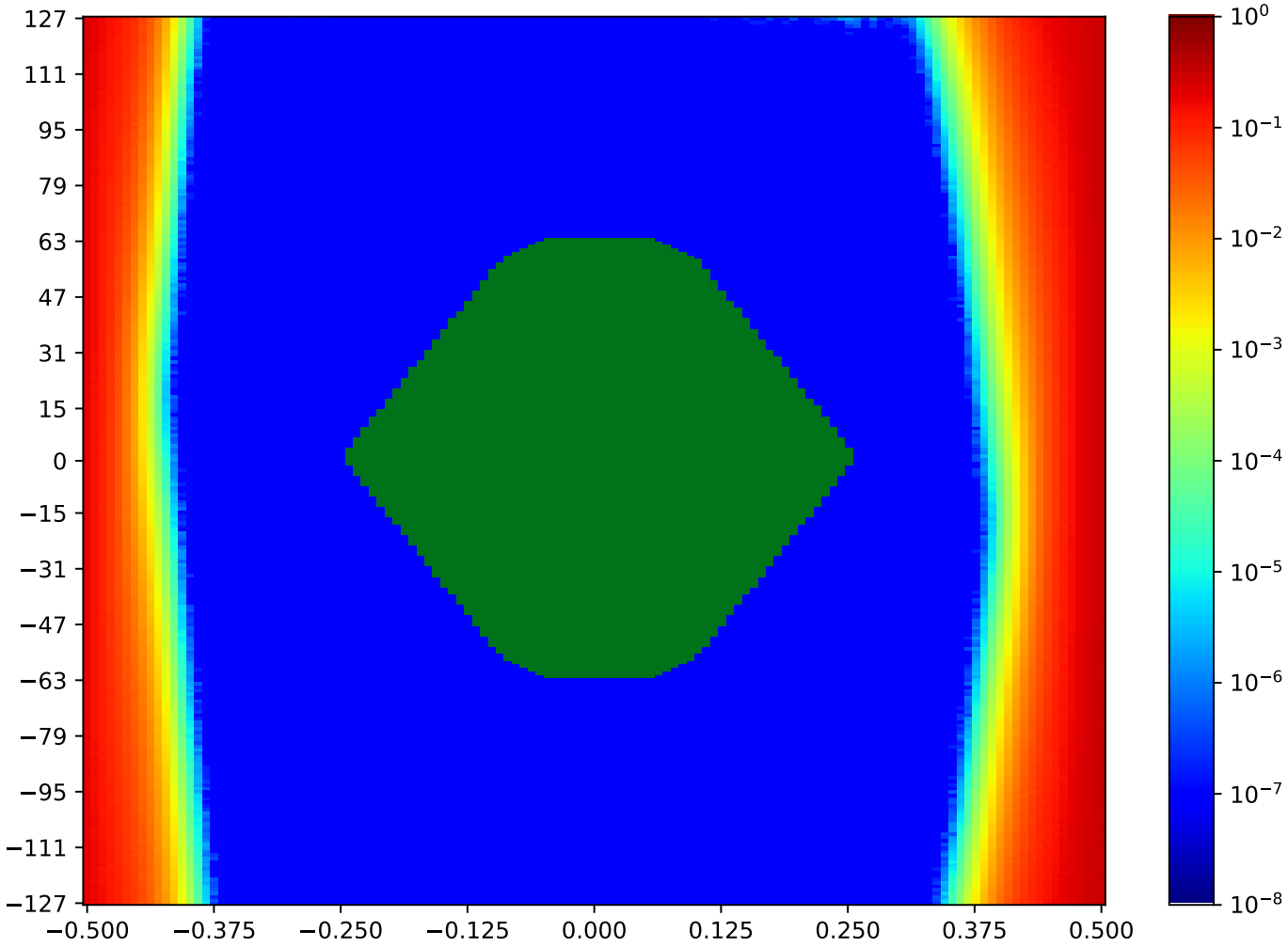


Figure 5.162: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.10 MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Table 5.151: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:53:14		2019-Nov-26 12:54:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23946	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

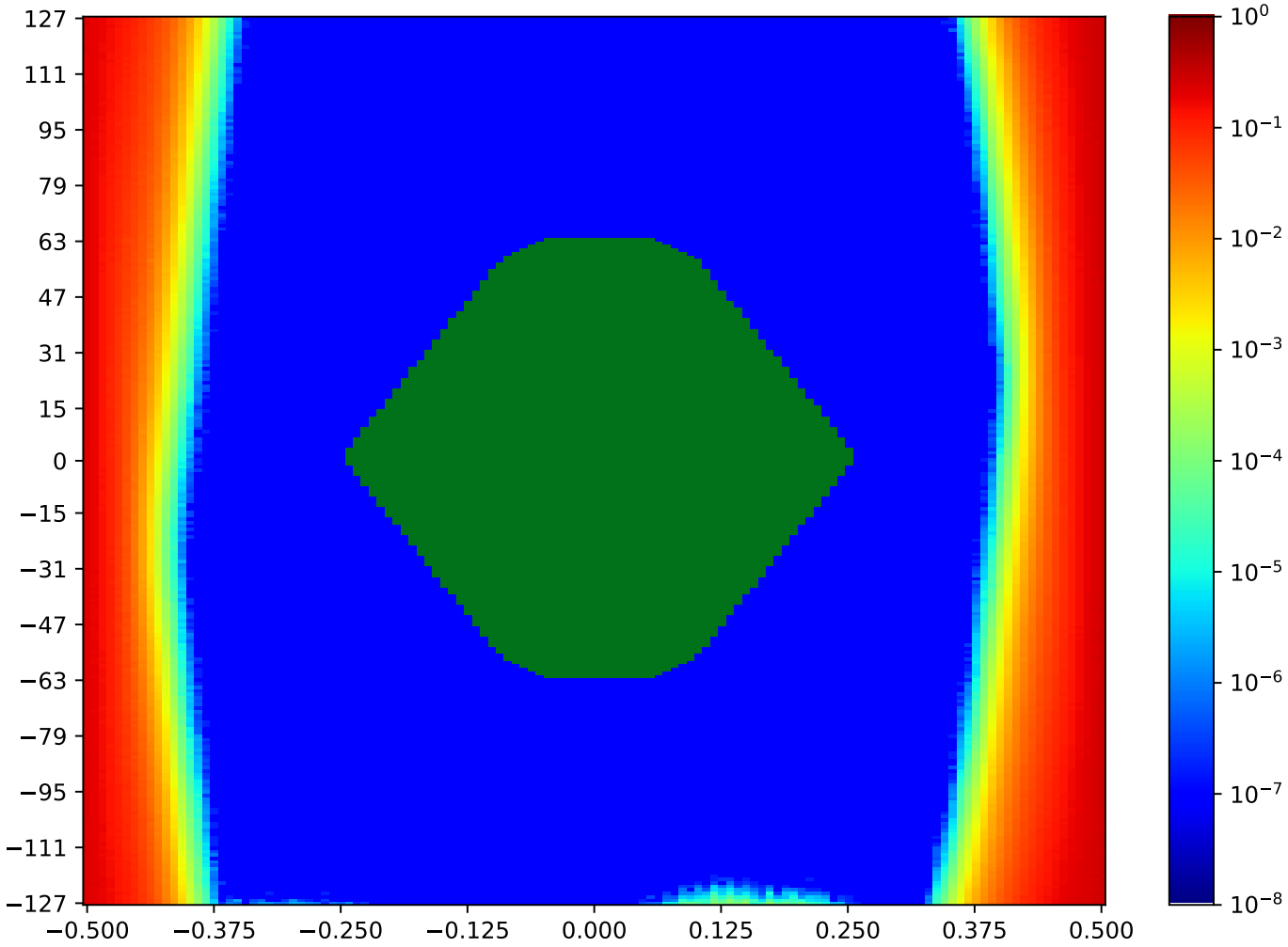


Figure 5.163: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.11 MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Table 5.152: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:57:45		2019-Nov-26 12:59:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23790	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

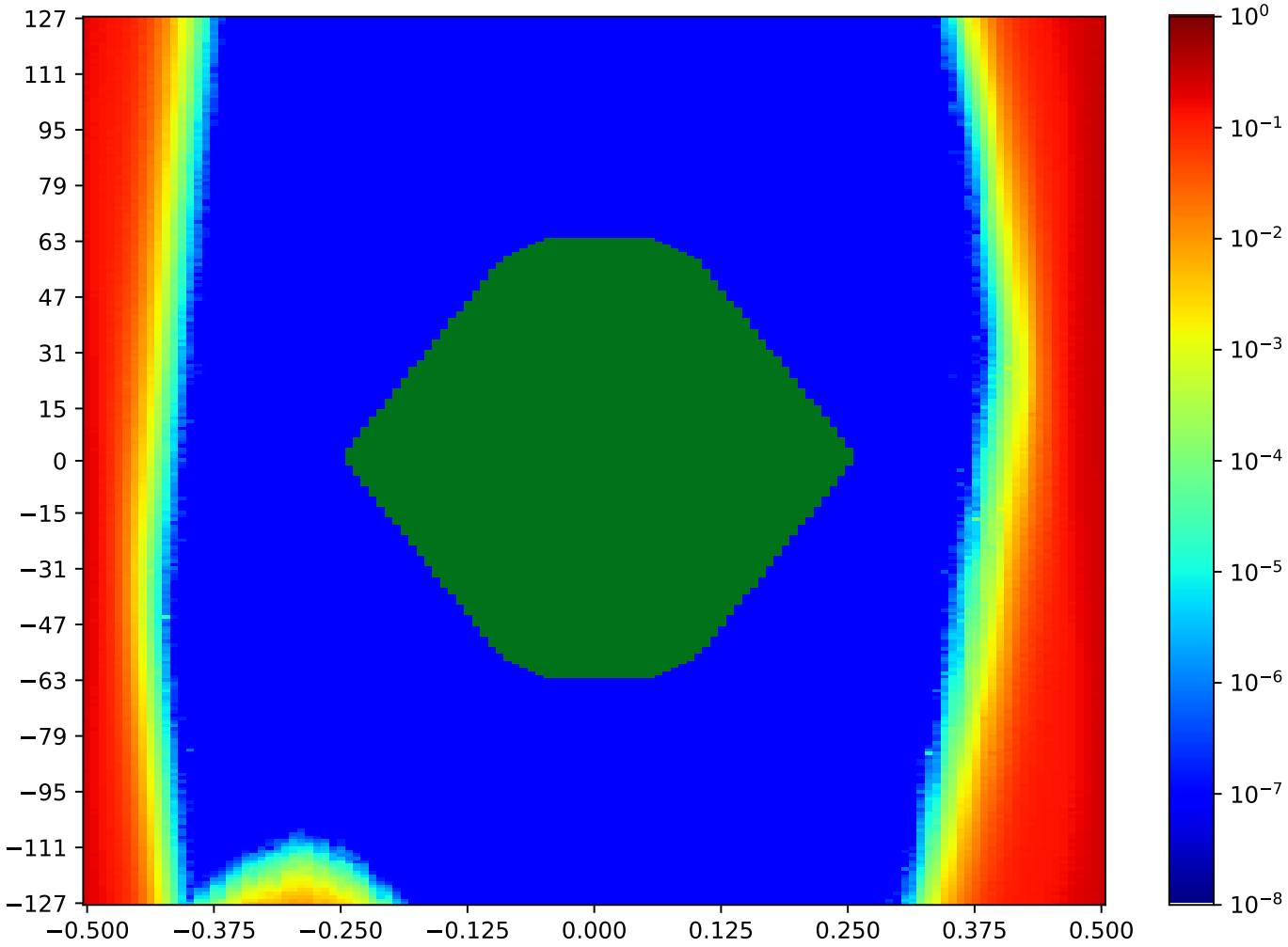


Figure 5.164: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.12.12 MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Table 5.153: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 12:56:36		2019-Nov-26 12:57:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24900	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

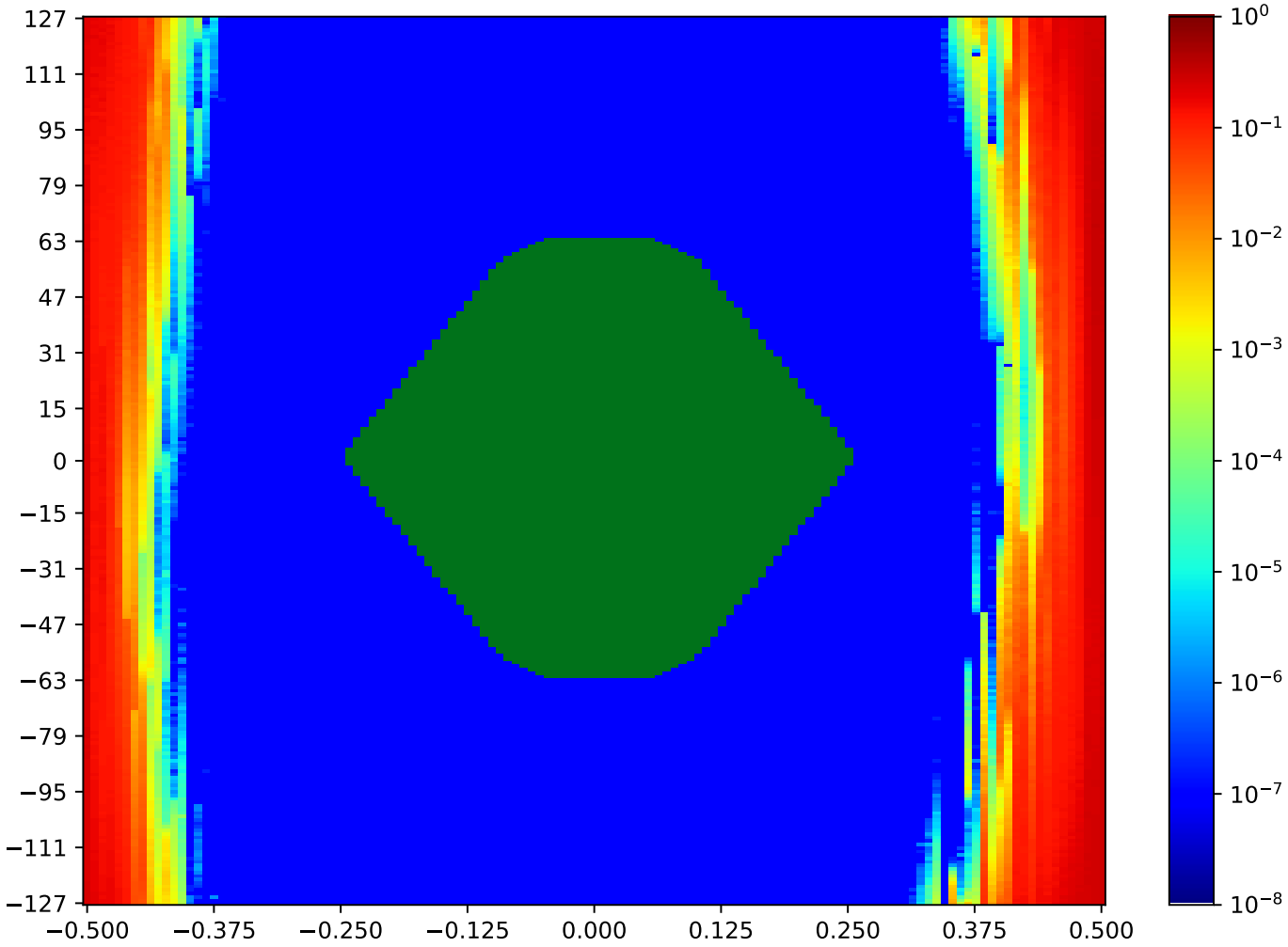


Figure 5.165: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13 MSP_C TX4 MSP_A RX9 Minipod Loopback

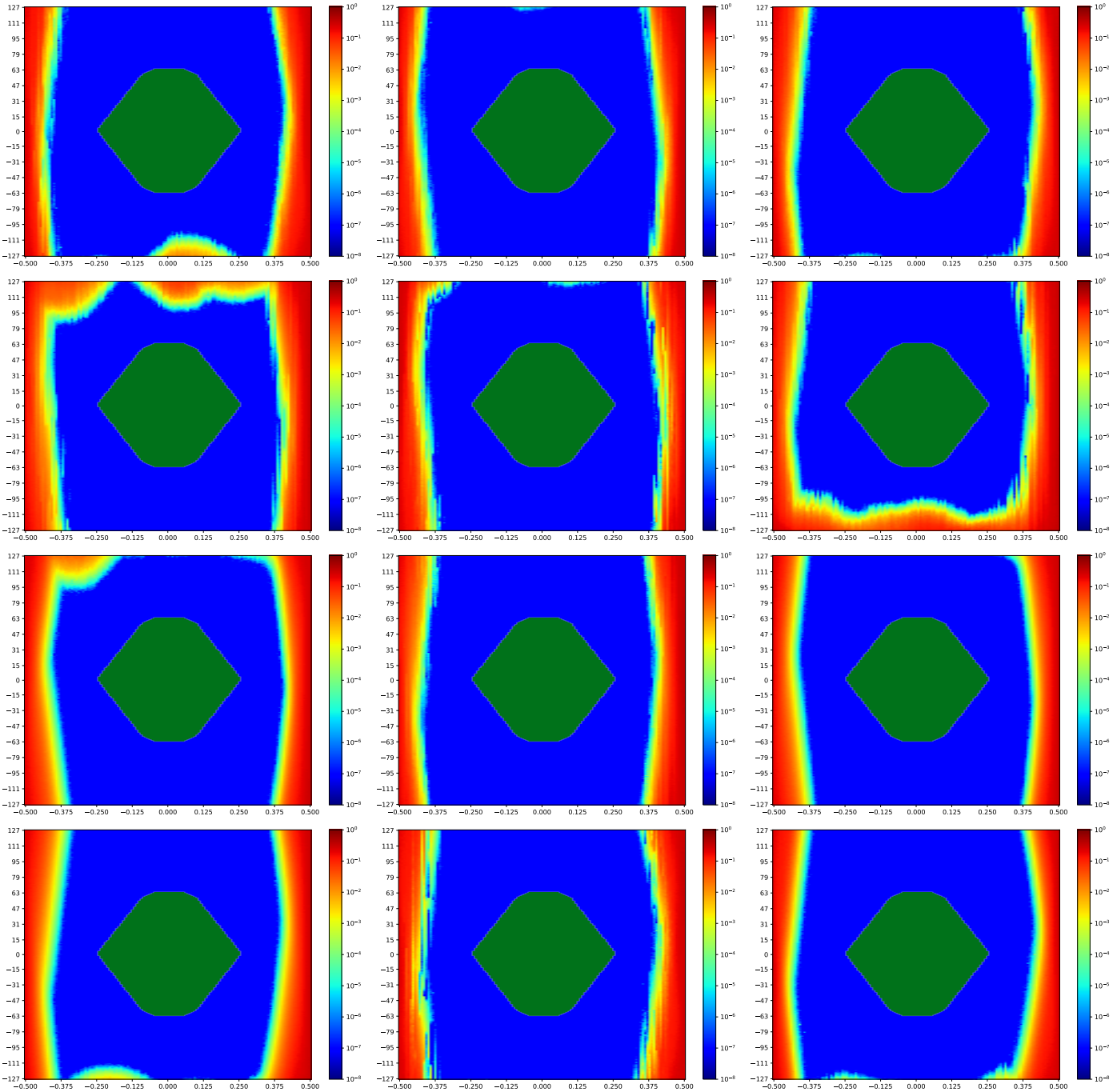


Figure 5.166: MSP_C TX4 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.179.

5.13.1 MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Table 5.154: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:05:57		2019-Nov-26 13:07:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23904	100	77.52%	233	90.59%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

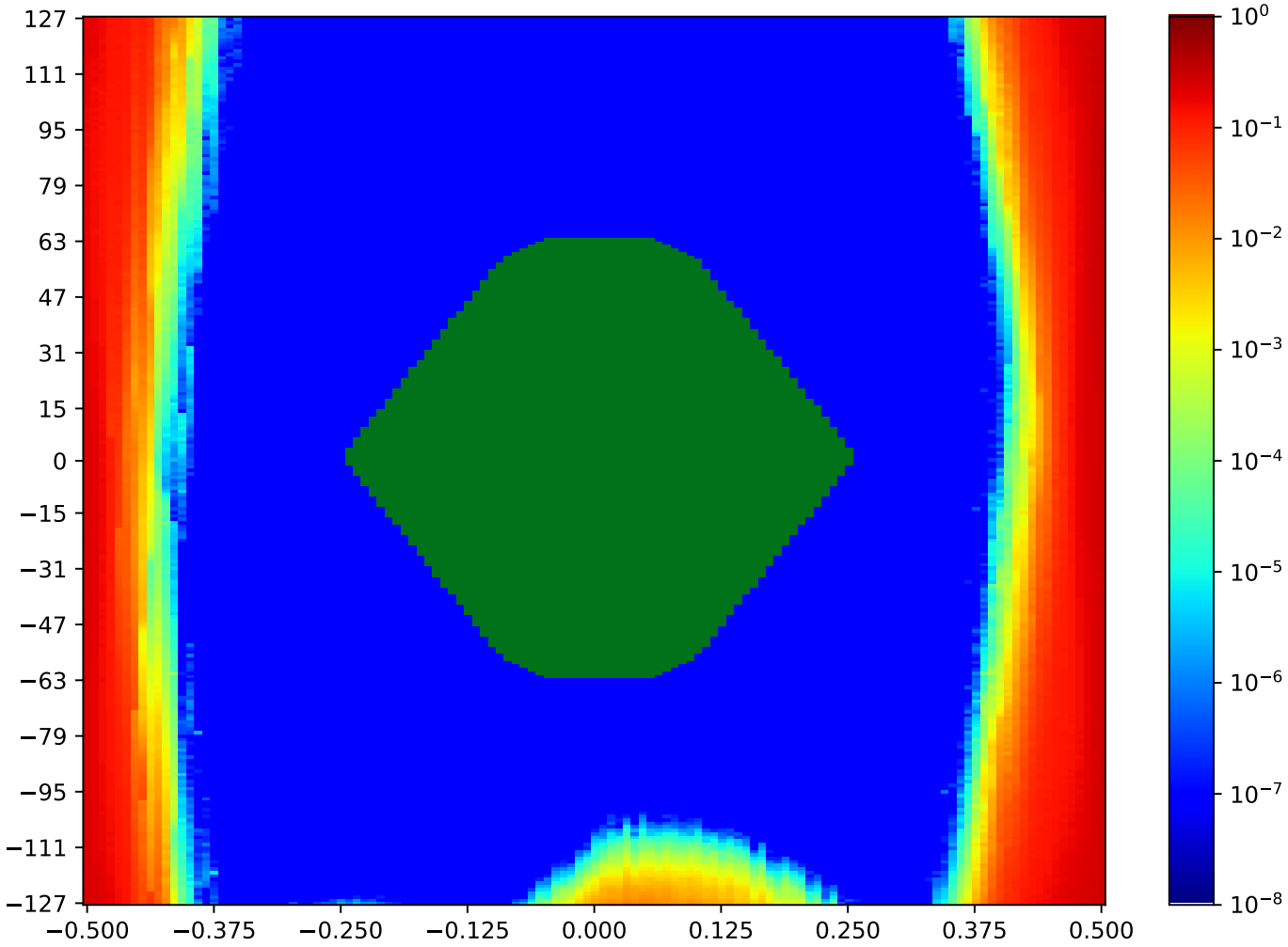


Figure 5.167: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.2 MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Table 5.155: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:03:42		2019-Nov-26 13:04:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24750	101	78.29%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

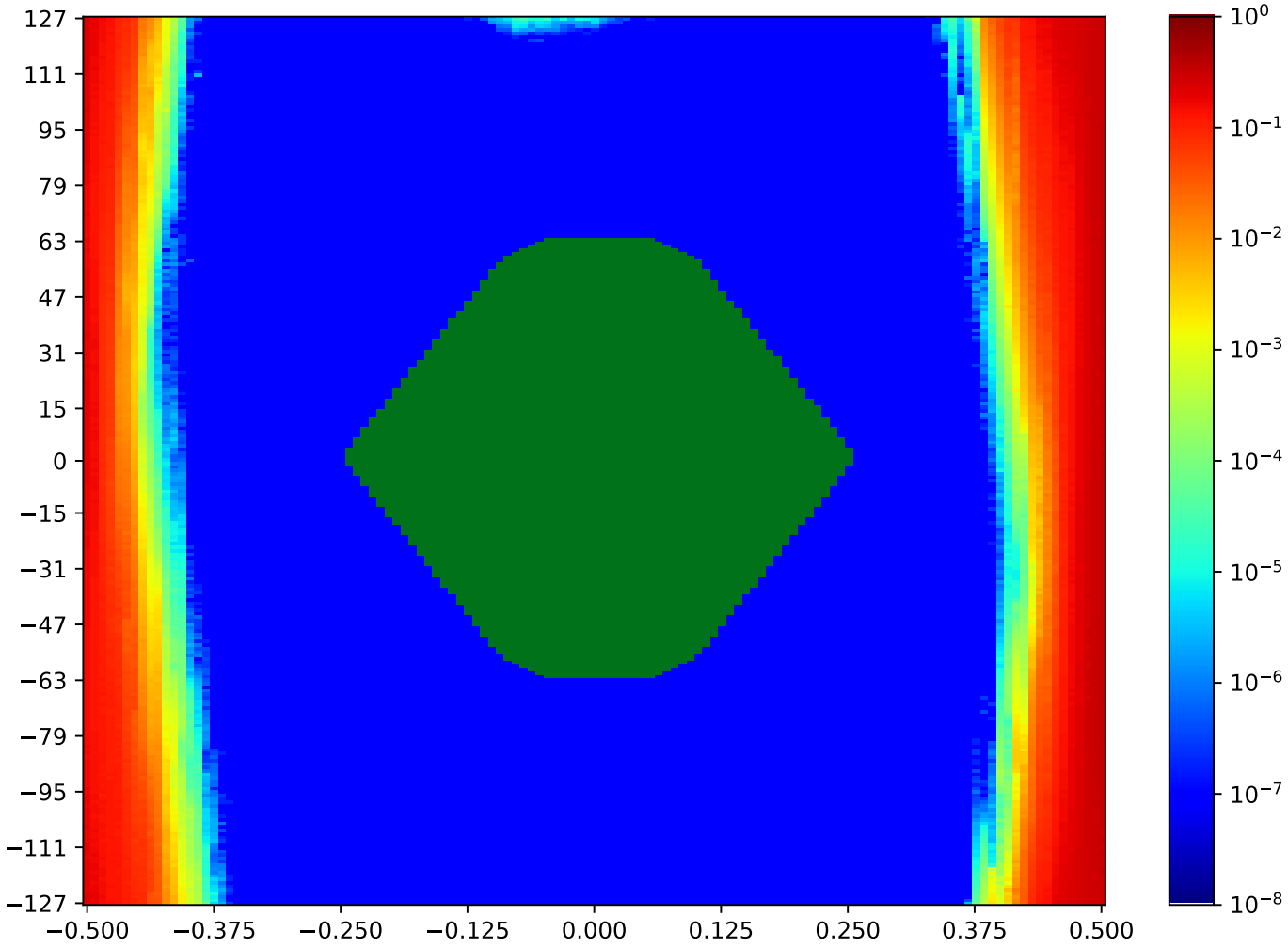


Figure 5.168: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.3 MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Table 5.156: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:09:54		2019-Nov-26 13:11:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24749	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

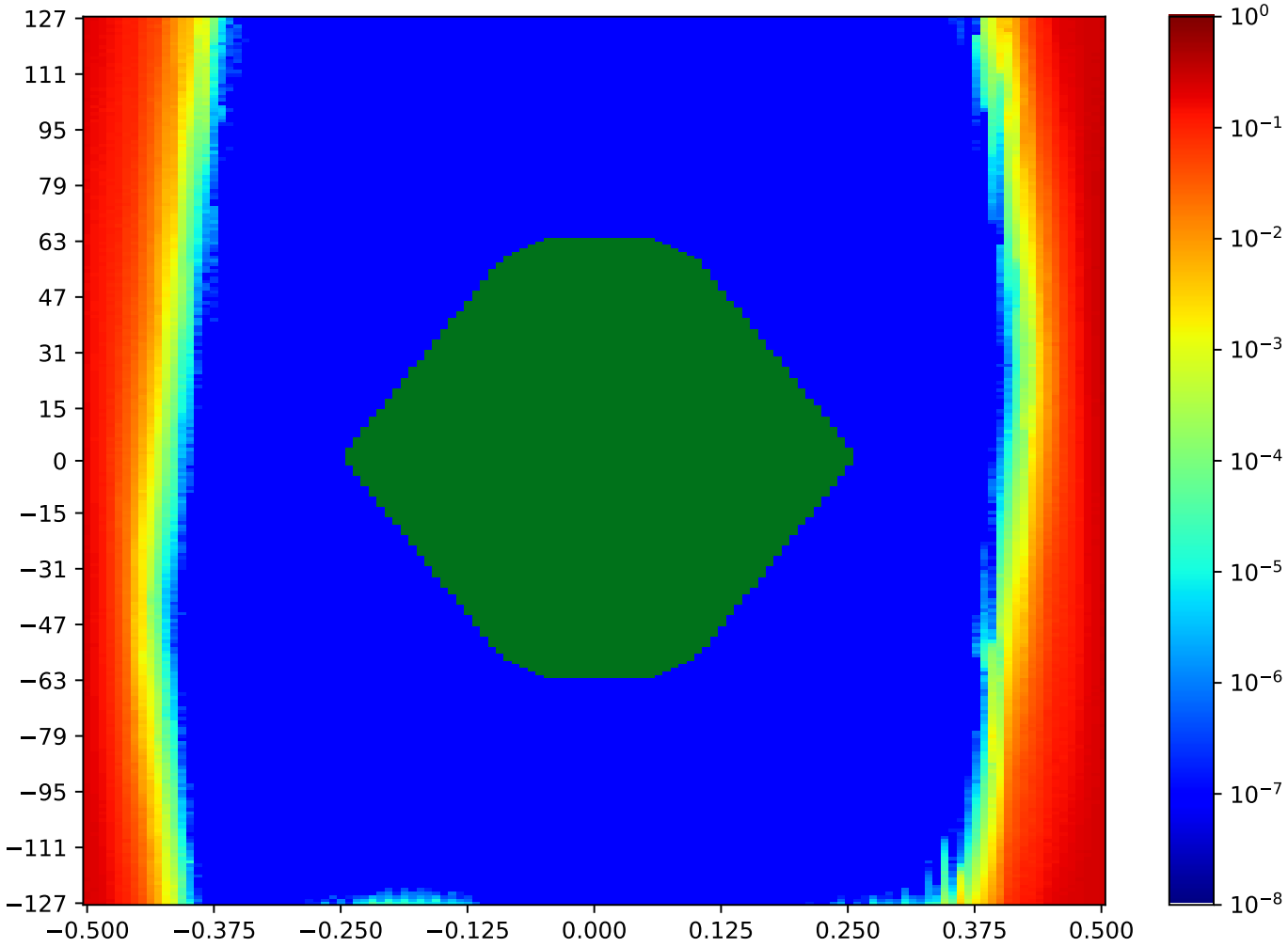


Figure 5.169: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.4 MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Table 5.157: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:02:27		2019-Nov-26 13:03:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21589	98	75.97%	222	86.67%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

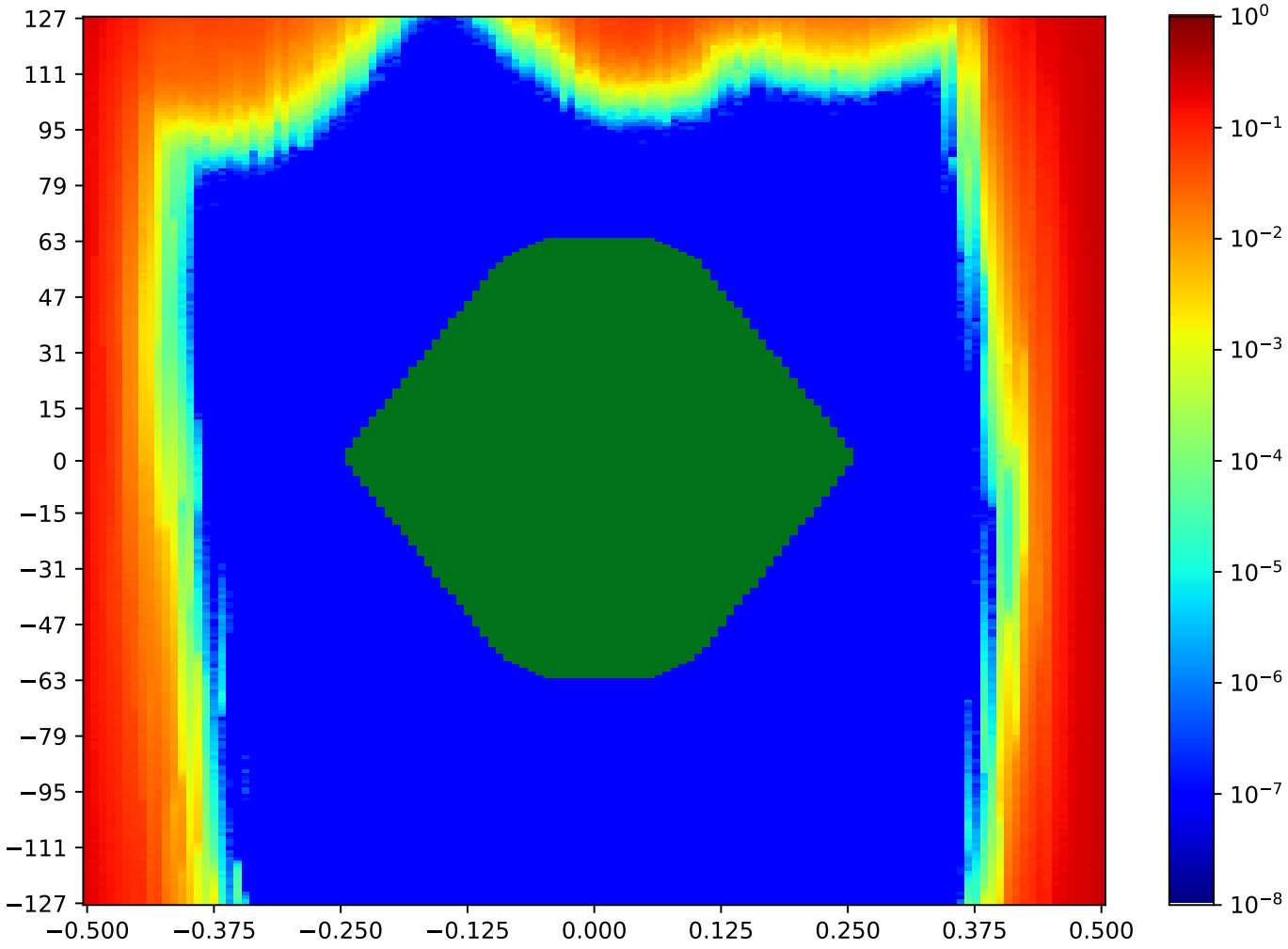


Figure 5.170: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.5 MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Table 5.158: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:13:18		2019-Nov-26 13:14:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24357	101	77.52%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

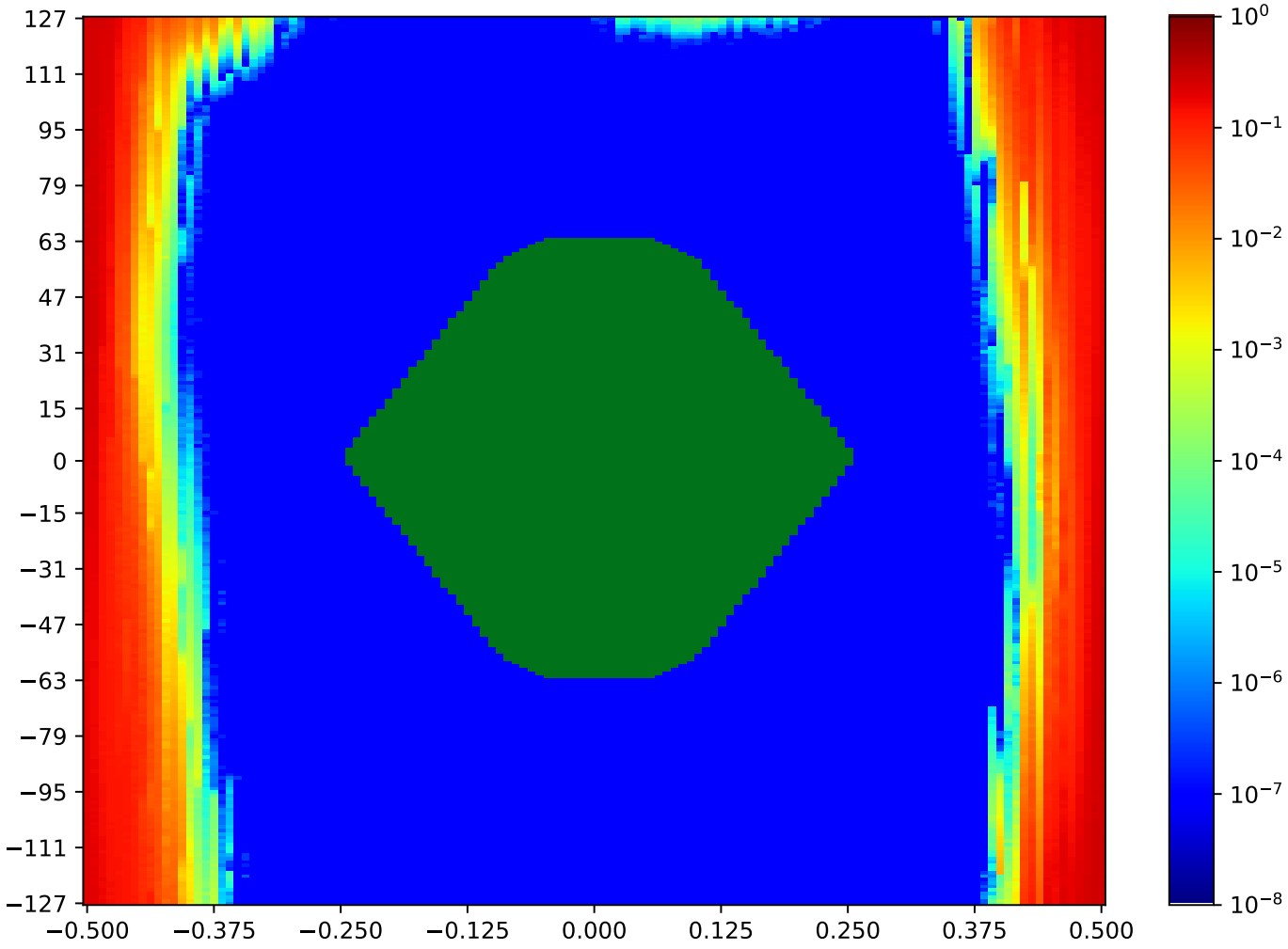


Figure 5.171: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.6 MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Table 5.159: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:04:50		2019-Nov-26 13:05:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21456	100	77.52%	220	86.27%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

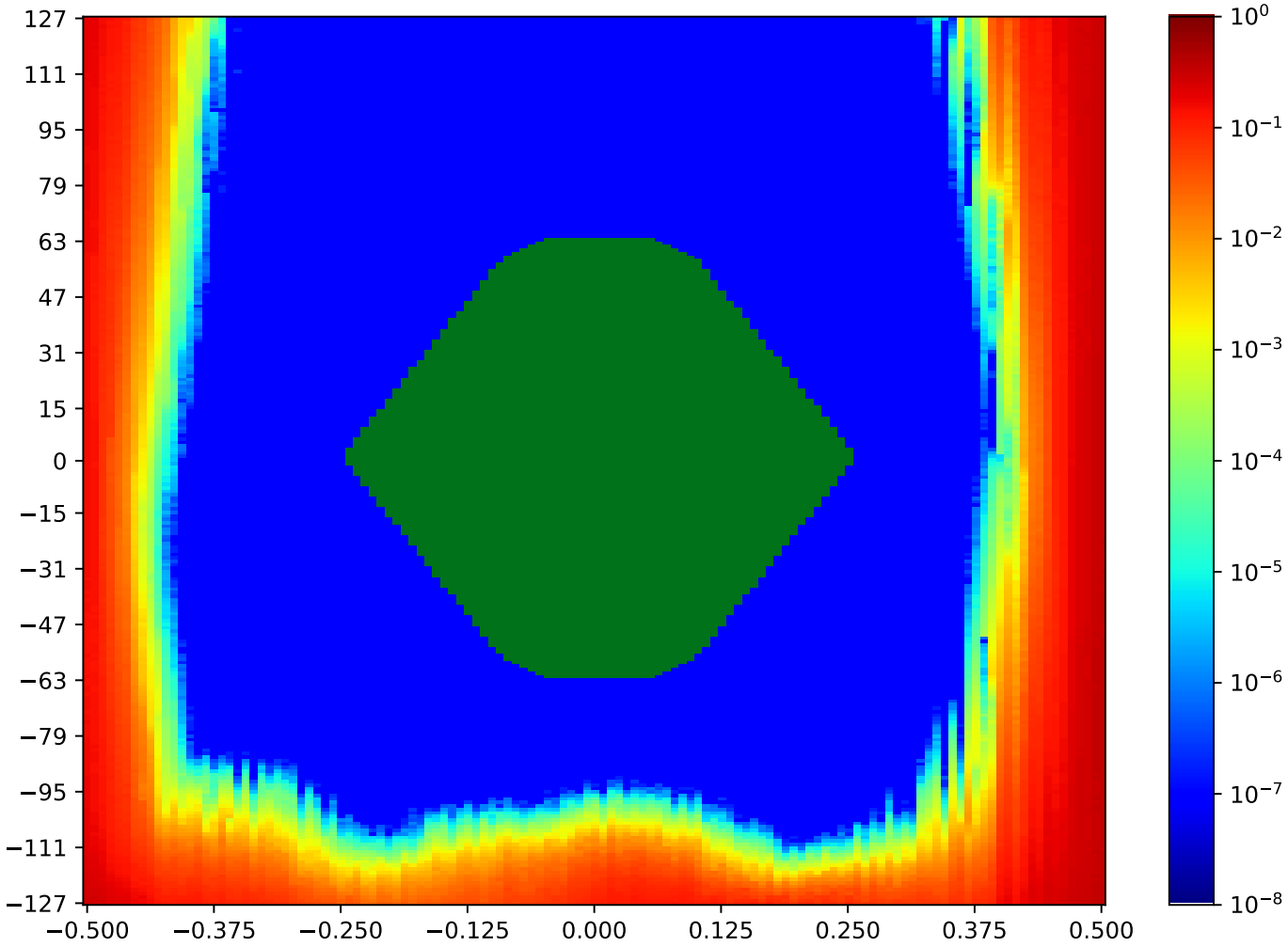


Figure 5.172: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.7 MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Table 5.160: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:15:34		2019-Nov-26 13:16:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23053	99	76.74%	251	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

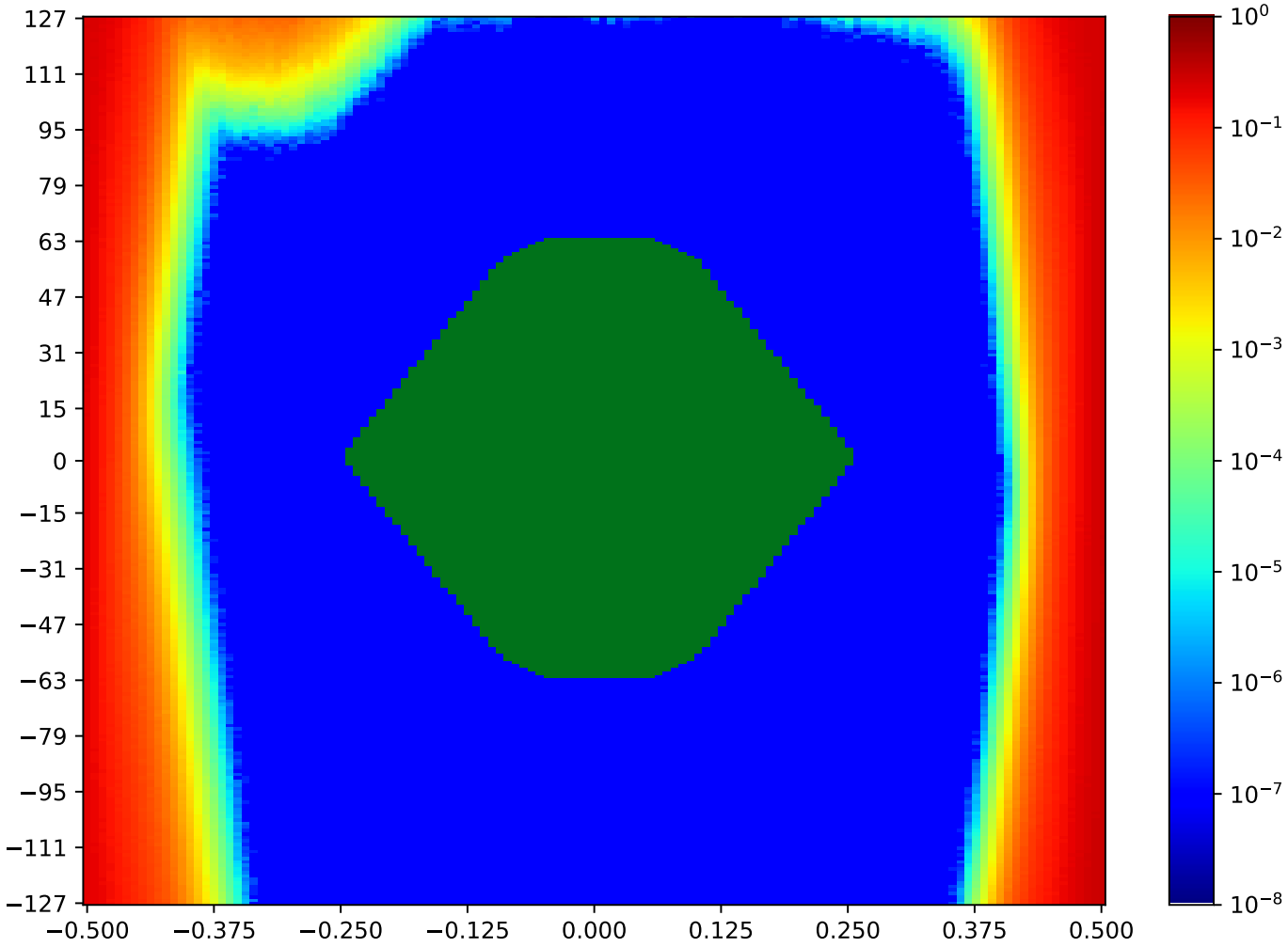


Figure 5.173: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.8 MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Table 5.161: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:07:05		2019-Nov-26 13:08:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24493	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

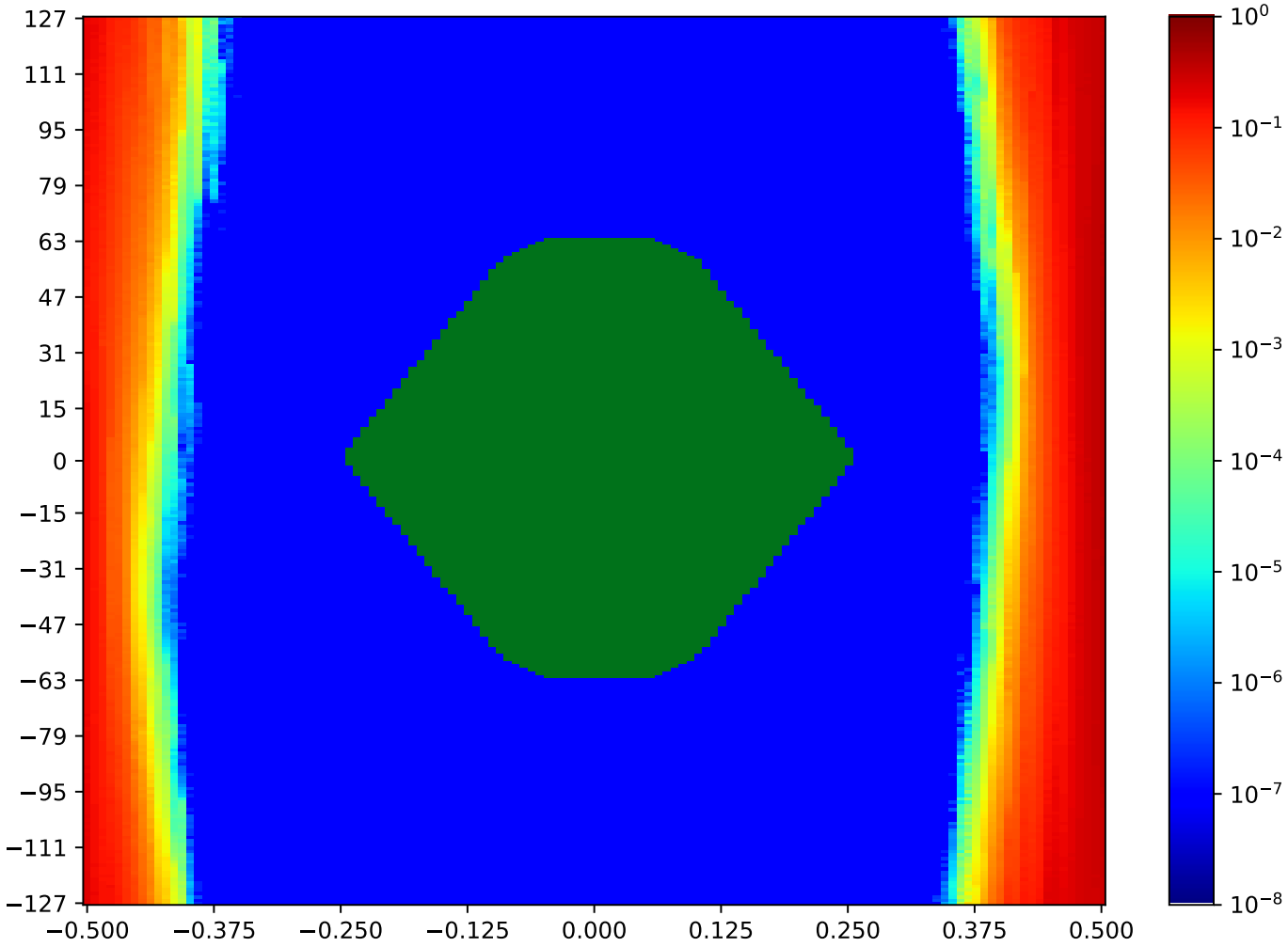


Figure 5.174: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.9 MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Table 5.162: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:14:26		2019-Nov-26 13:15:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24458	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

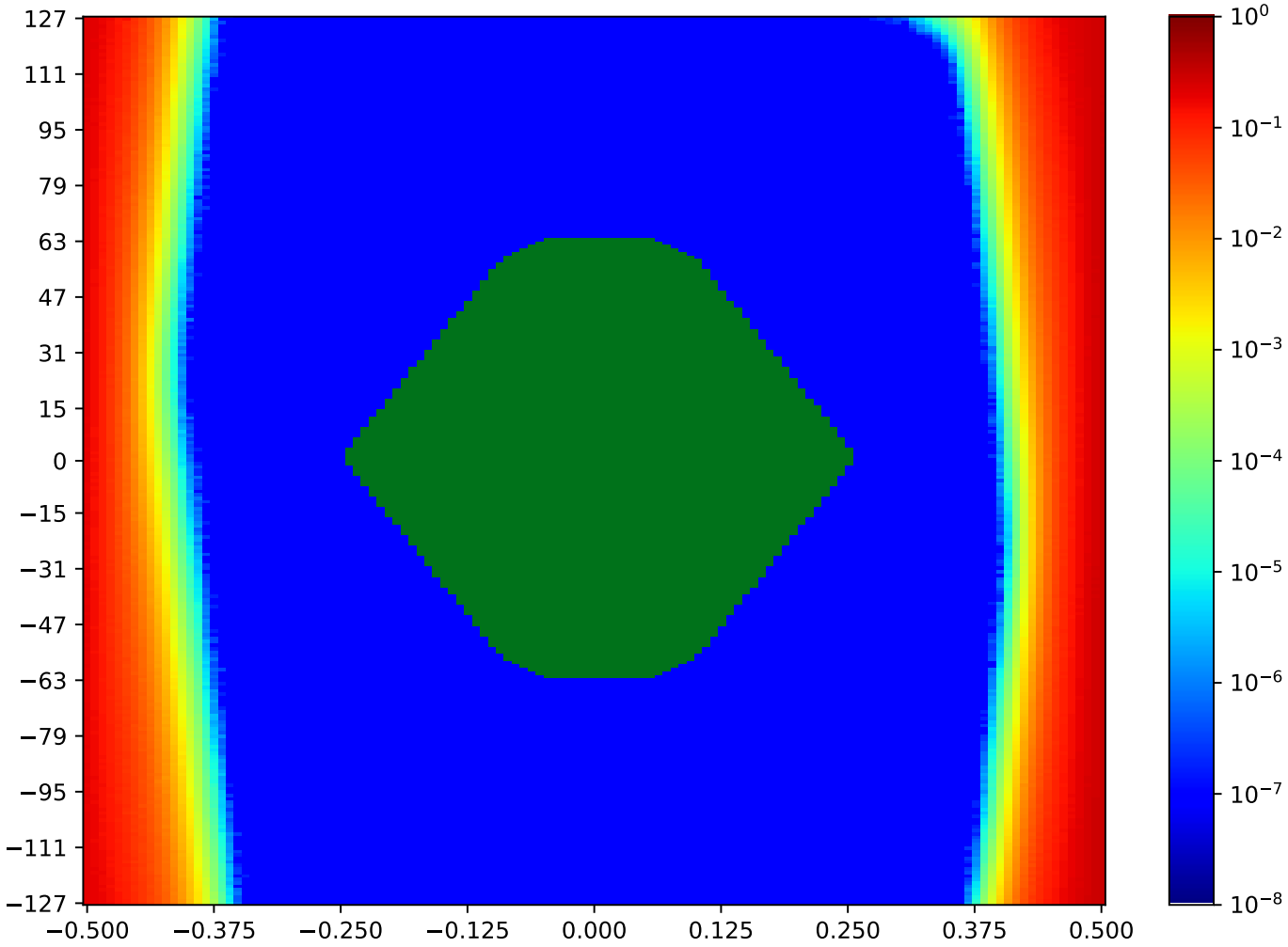


Figure 5.175: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.10 MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Table 5.163: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:08:30		2019-Nov-26 13:09:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23024	95	73.64%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

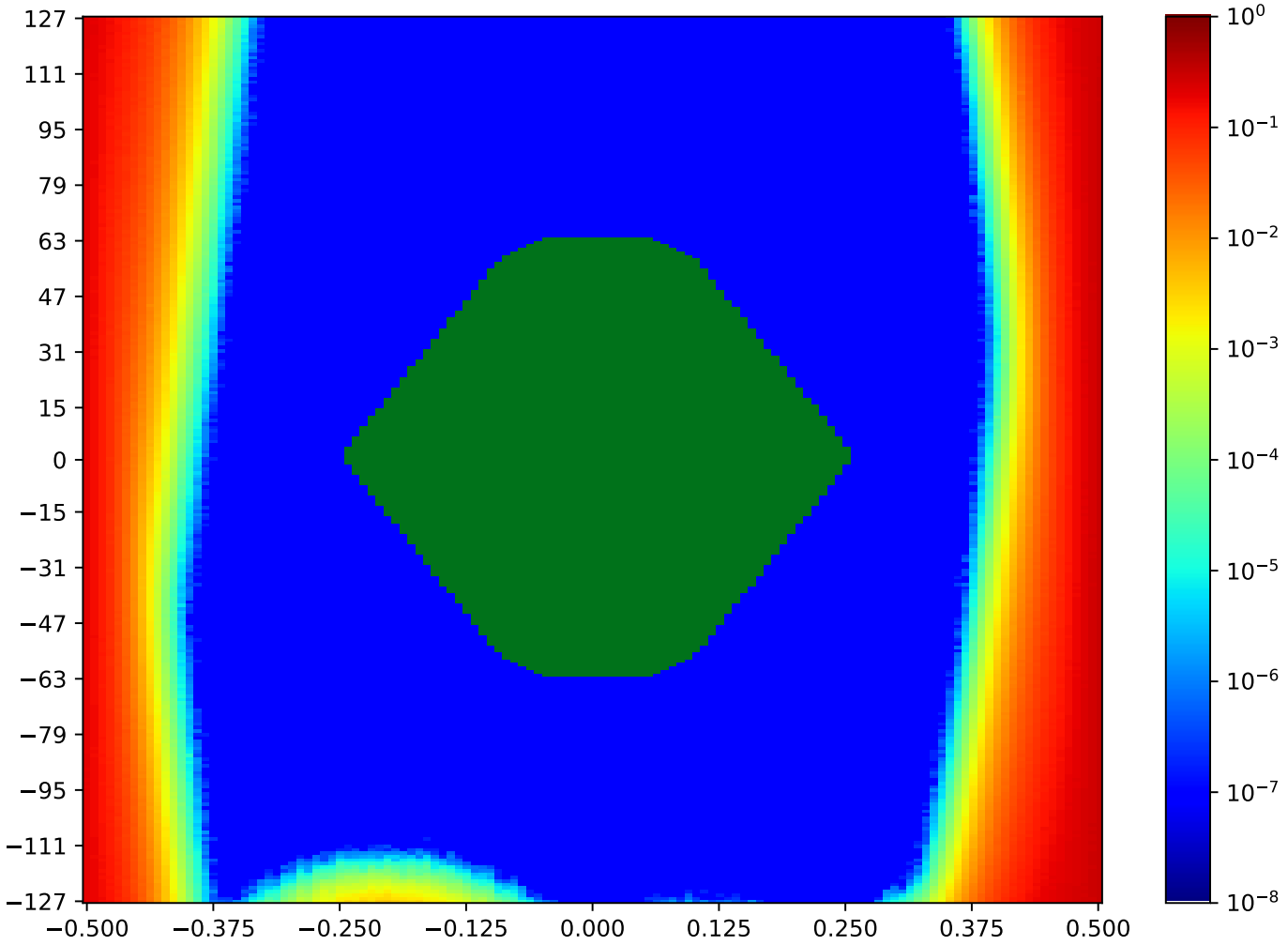


Figure 5.176: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.11 MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Table 5.164: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:12:10		2019-Nov-26 13:13:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24042	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

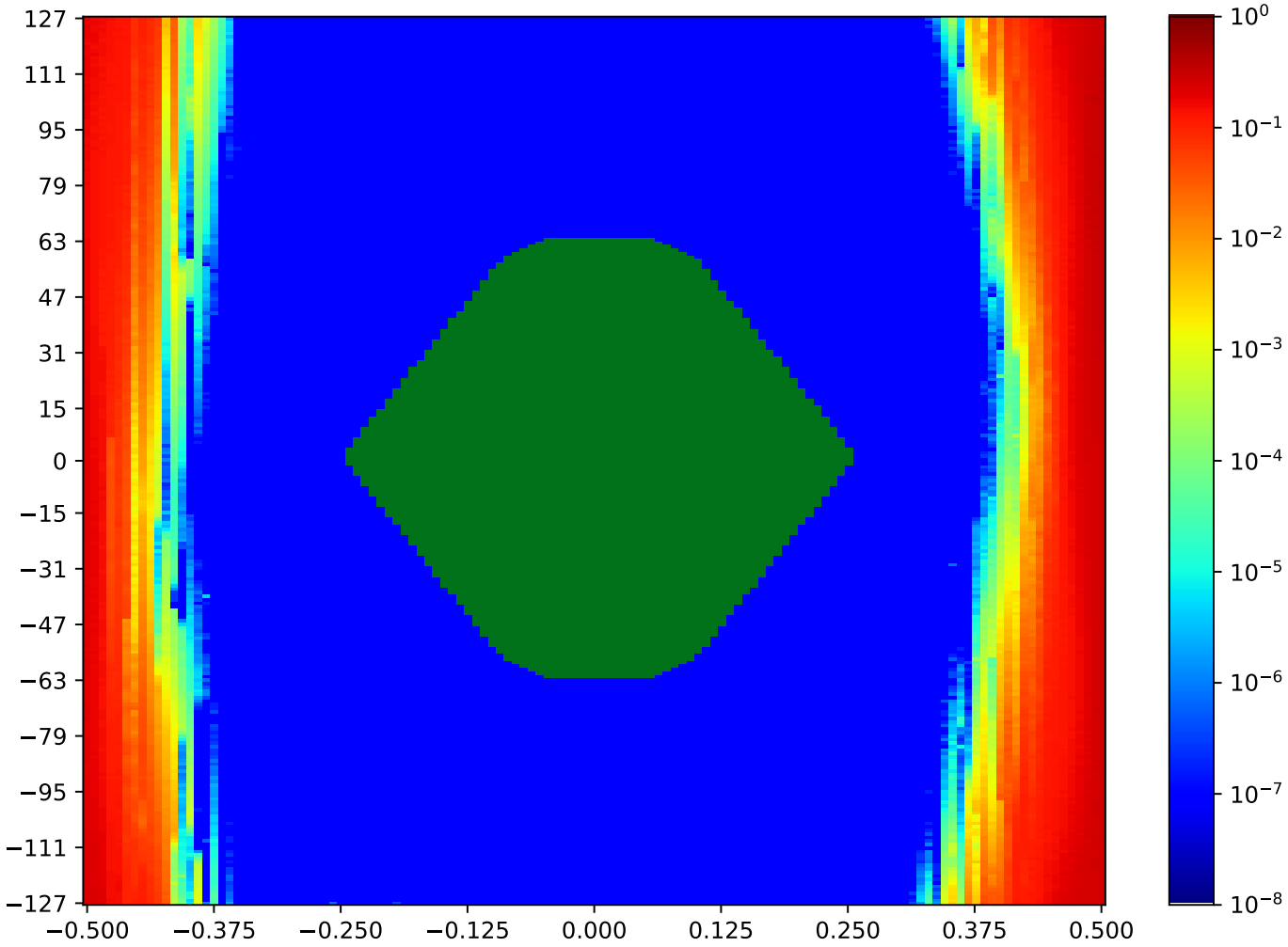


Figure 5.177: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.13.12 MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Table 5.165: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:11:02		2019-Nov-26 13:12:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24512	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

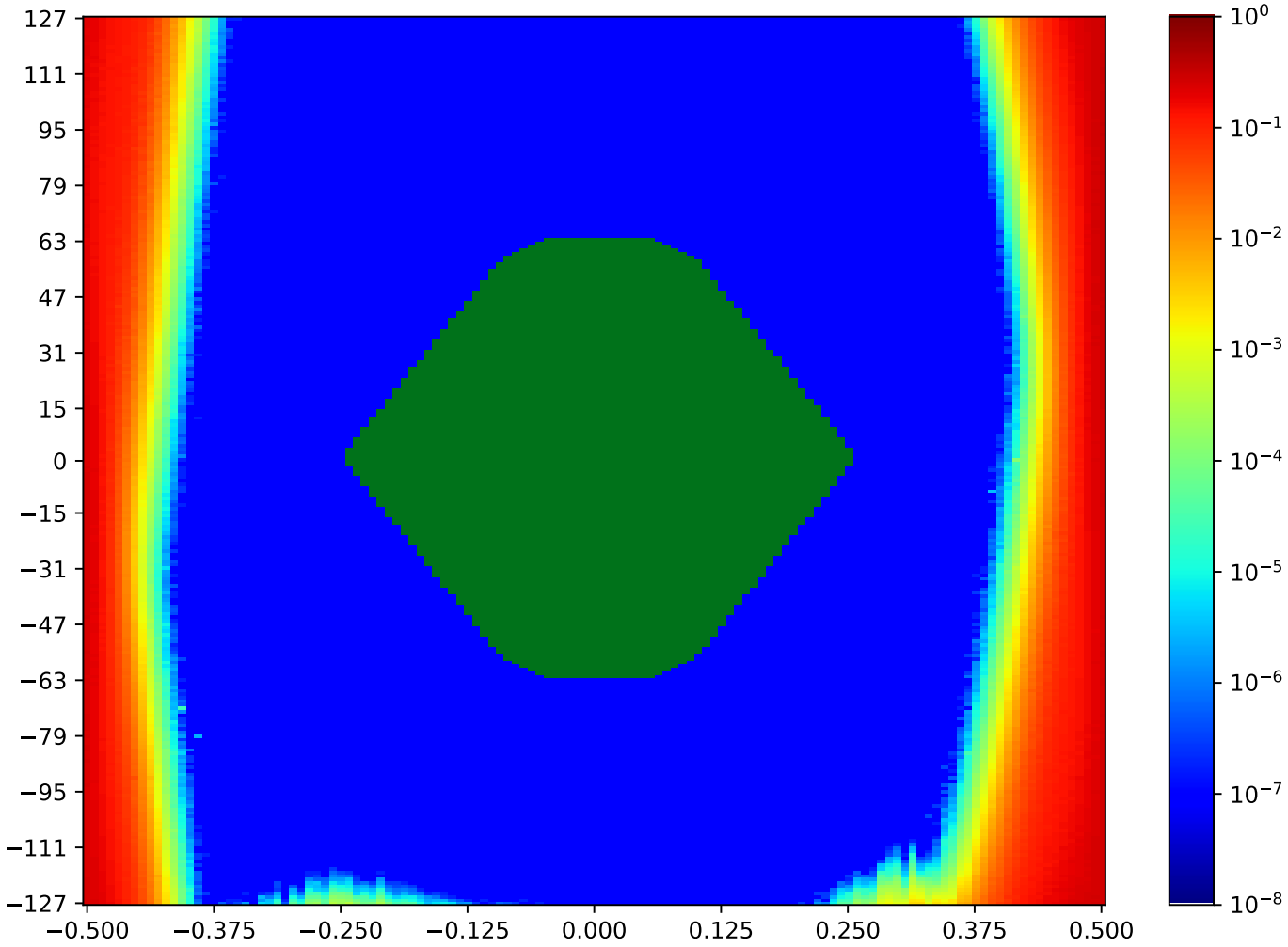


Figure 5.178: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.188.

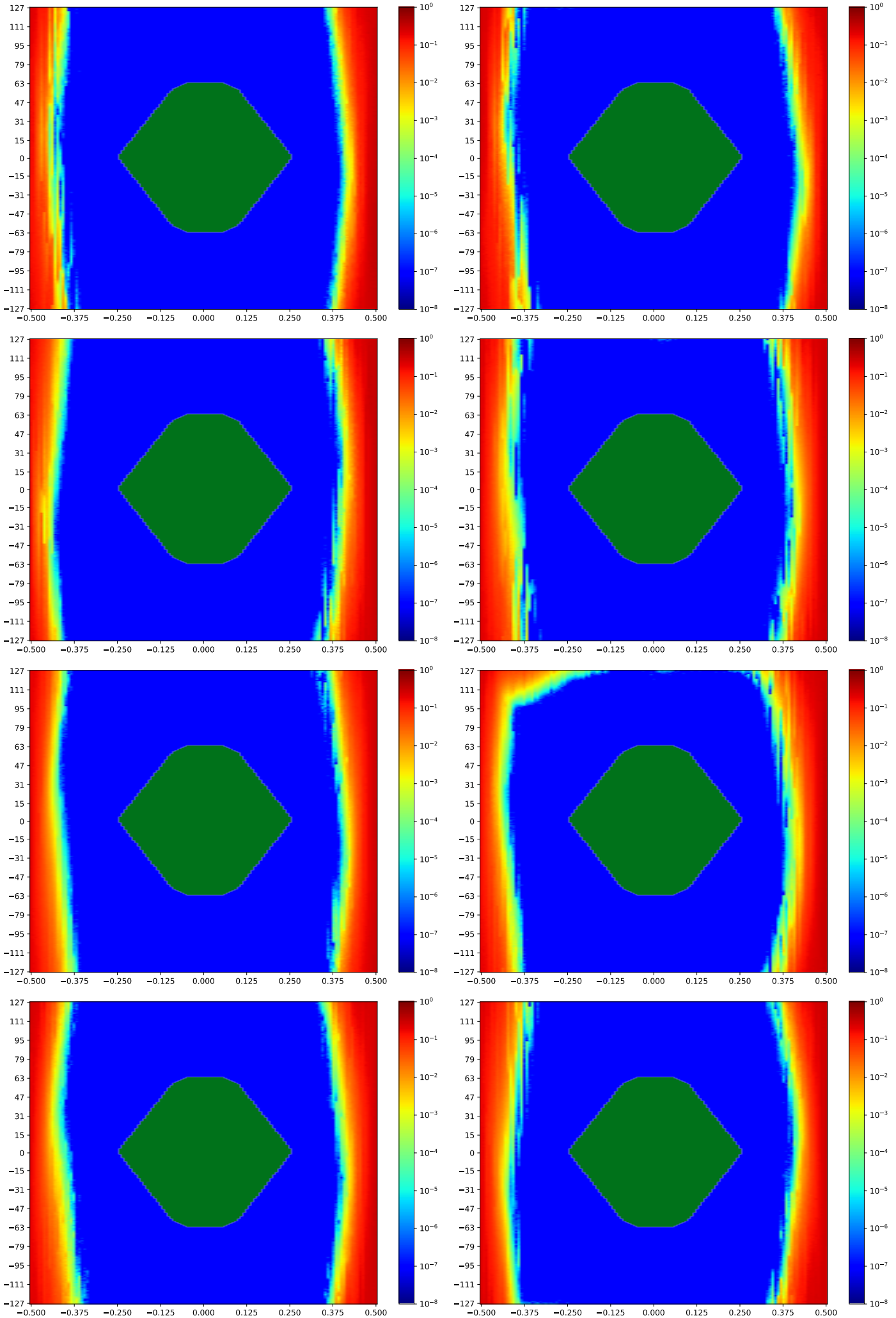


Figure 5.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback

5.14.1 TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Table 5.166: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:20:17		2019-Nov-26 13:21:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24877	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

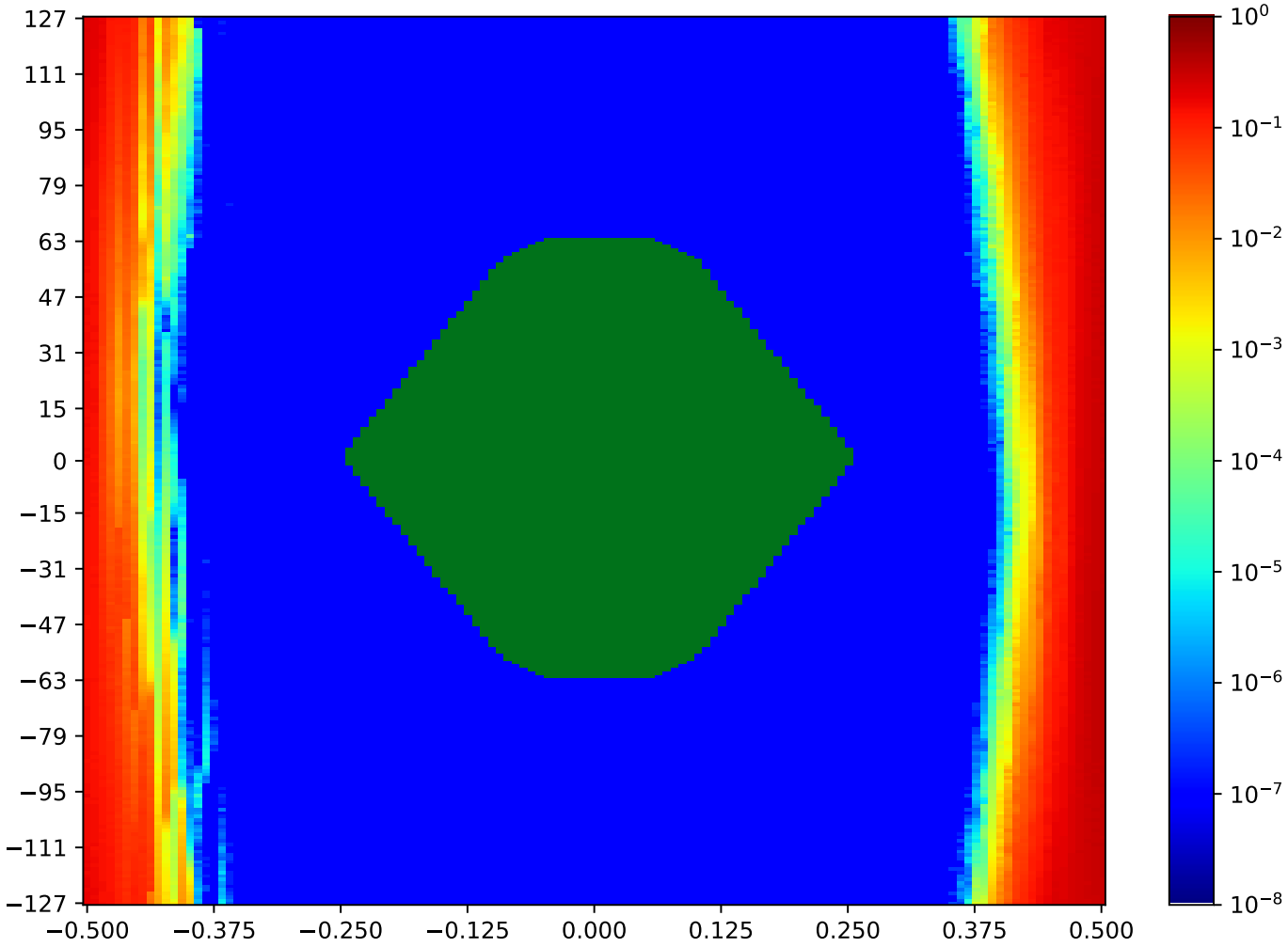


Figure 5.180: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.2 TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Table 5.167: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:17:50		2019-Nov-26 13:19:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24557	103	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

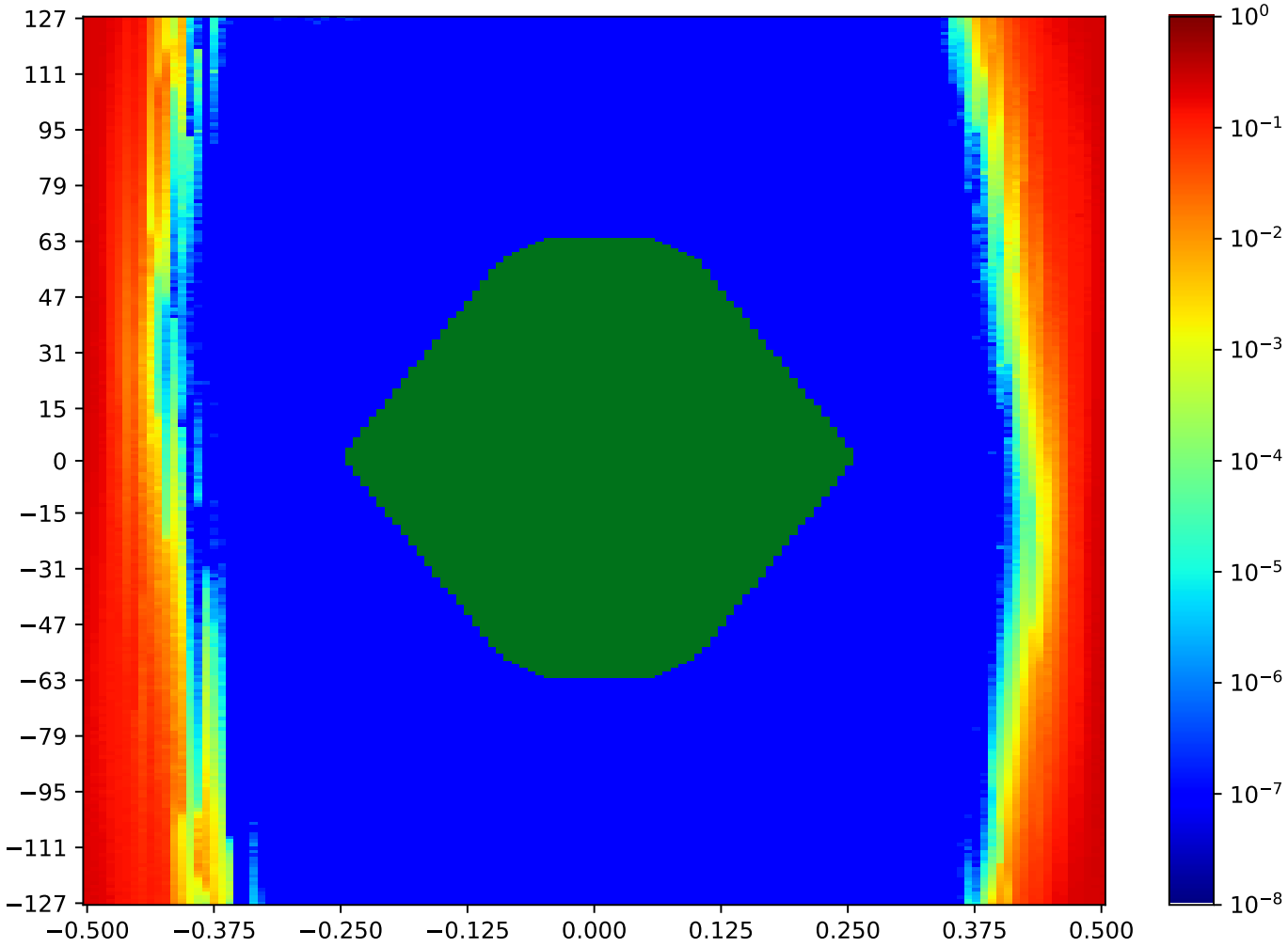


Figure 5.181: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.3 TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Table 5.168: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:22:32		2019-Nov-26 13:23:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24829	102	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

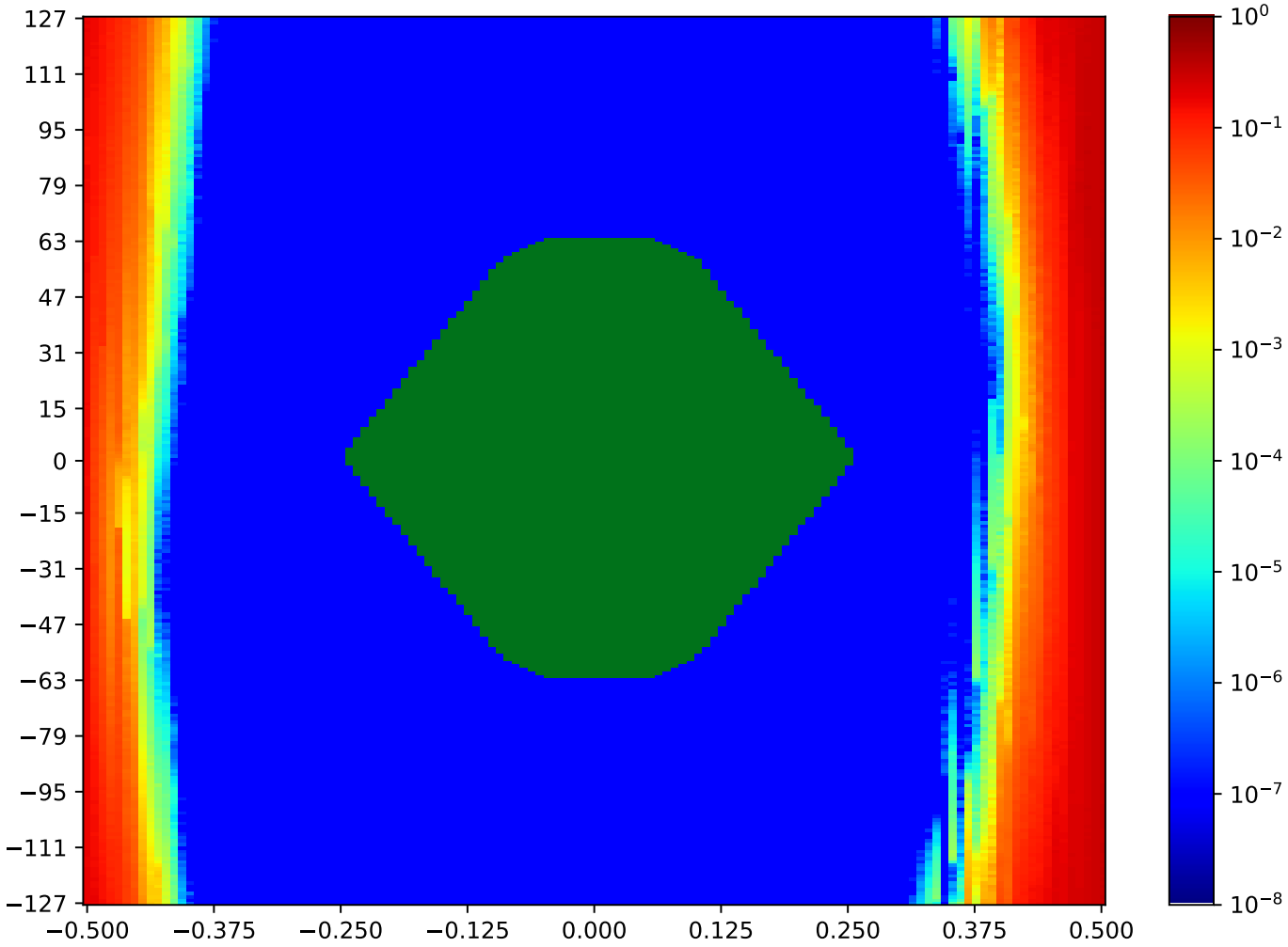


Figure 5.182: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.4 TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Table 5.169: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:19:10		2019-Nov-26 13:20:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23704	100	75.97%	254	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

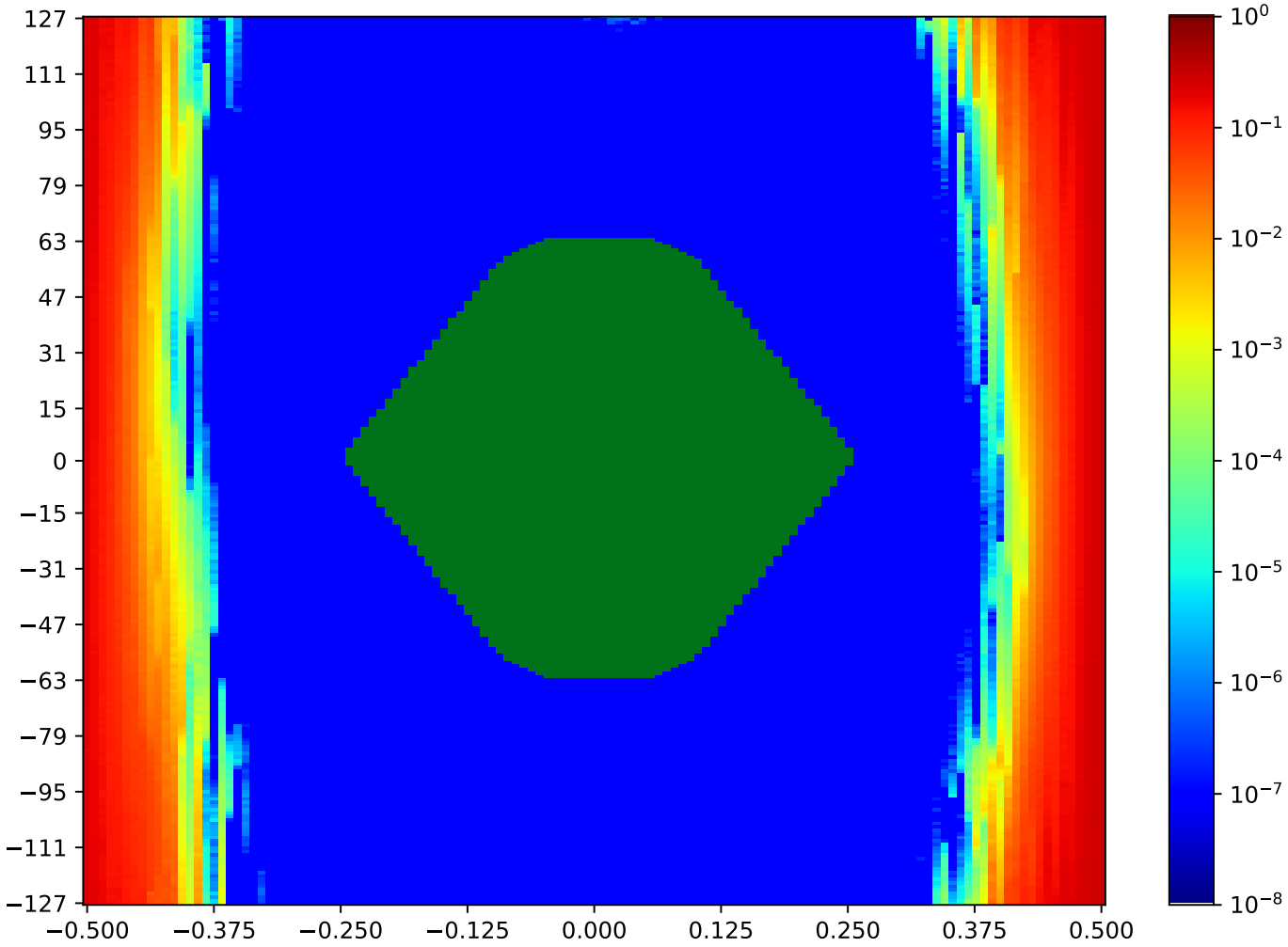


Figure 5.183: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.5 TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Table 5.170: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:25:00		2019-Nov-26 13:26:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24452	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

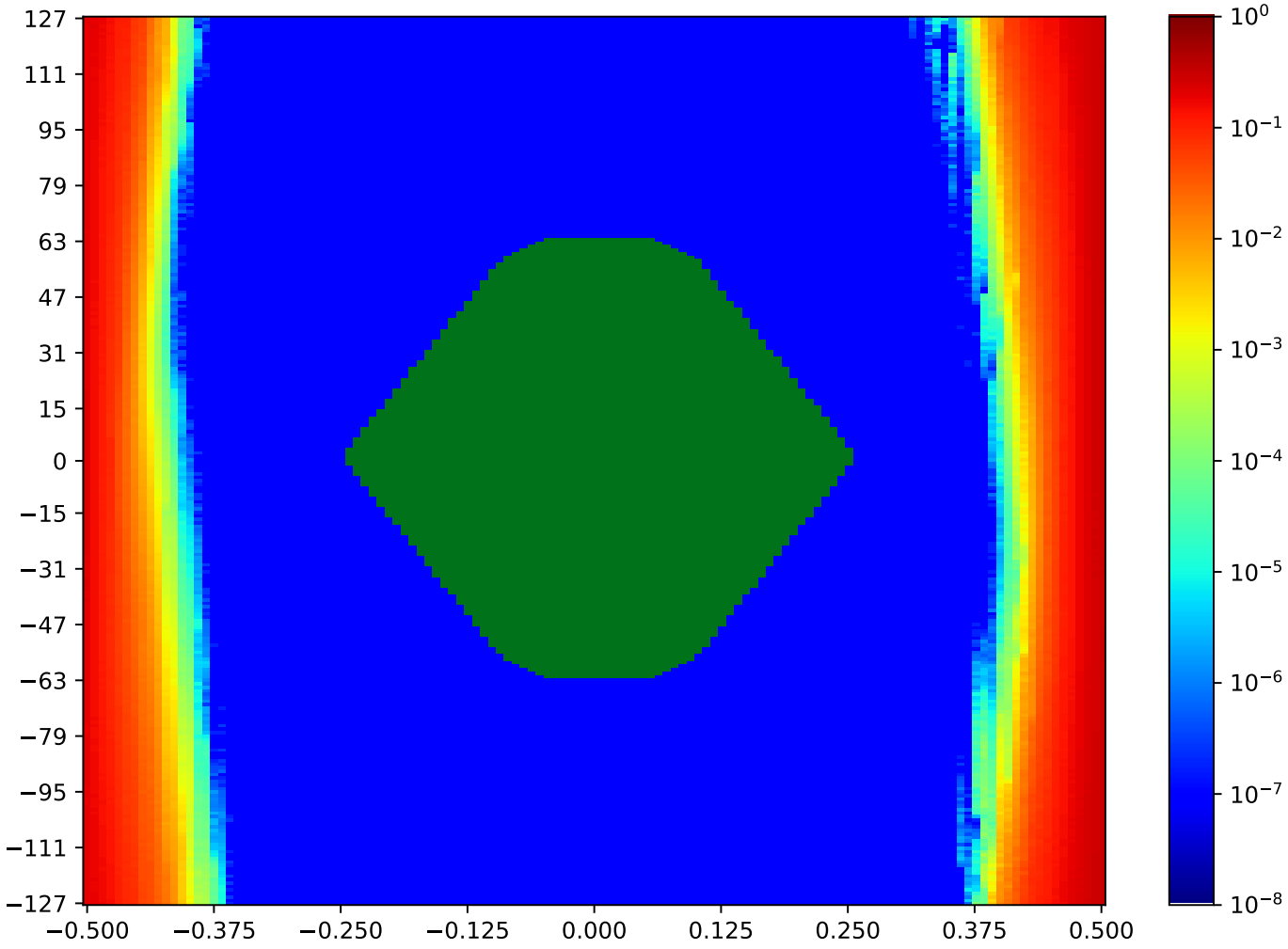


Figure 5.184: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.6 TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Table 5.171: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:16:42		2019-Nov-26 13:17:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23420	98	75.97%	253	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

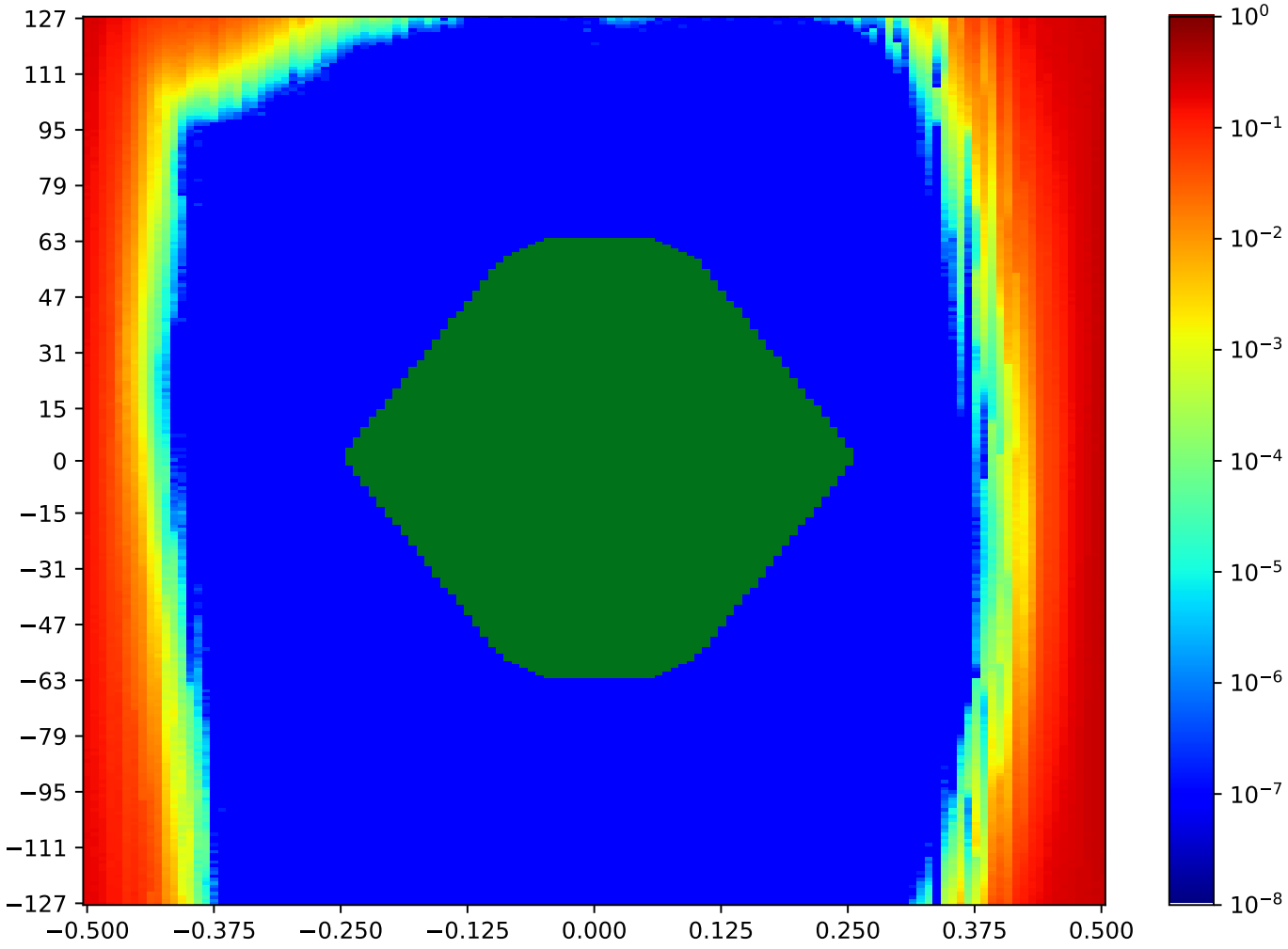


Figure 5.185: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.7 TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Table 5.172: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:21:24		2019-Nov-26 13:22:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23944	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

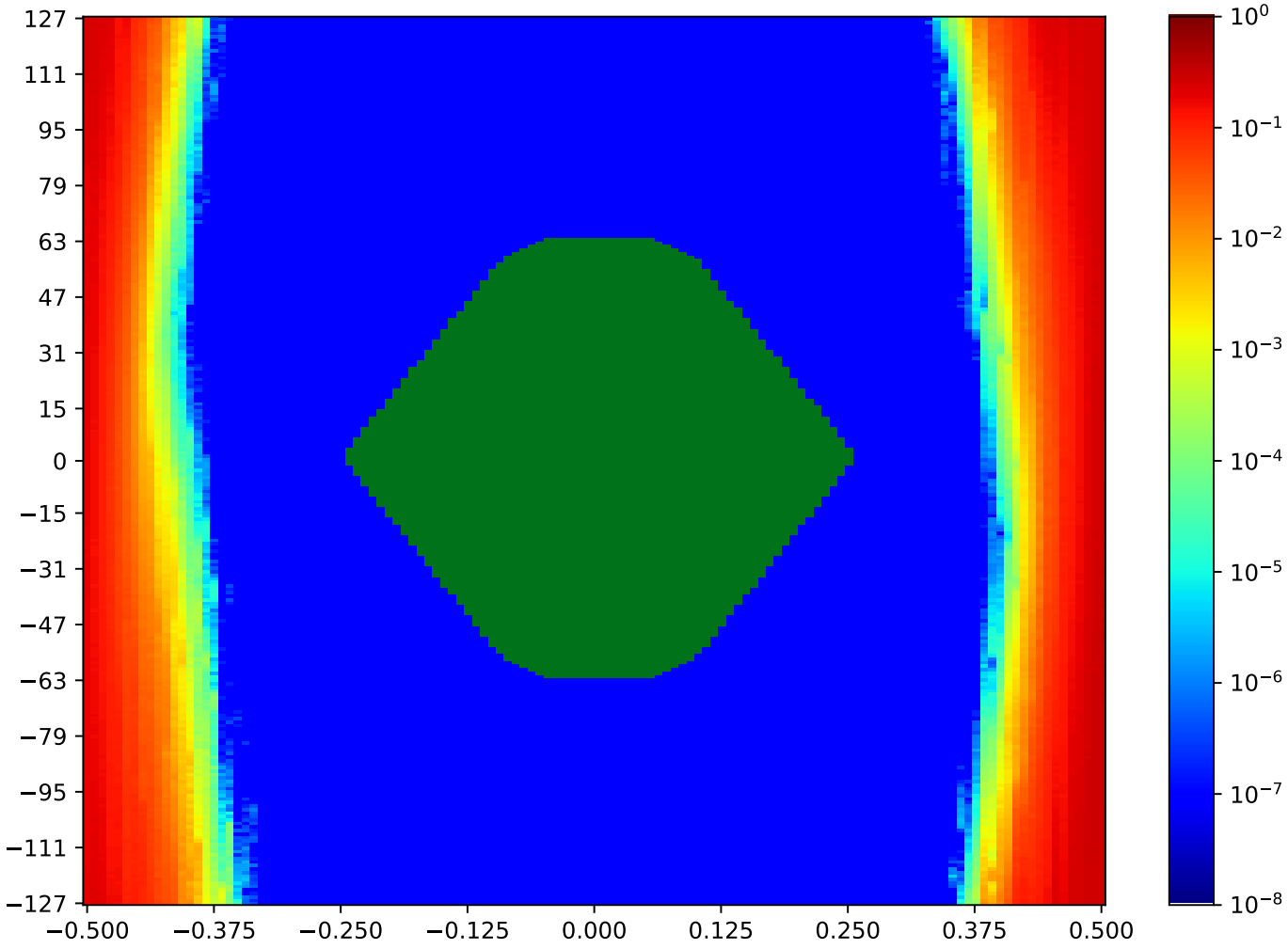


Figure 5.186: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.14.8 TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Table 5.173: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 13:23:53		2019-Nov-26 13:25:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24065	102	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

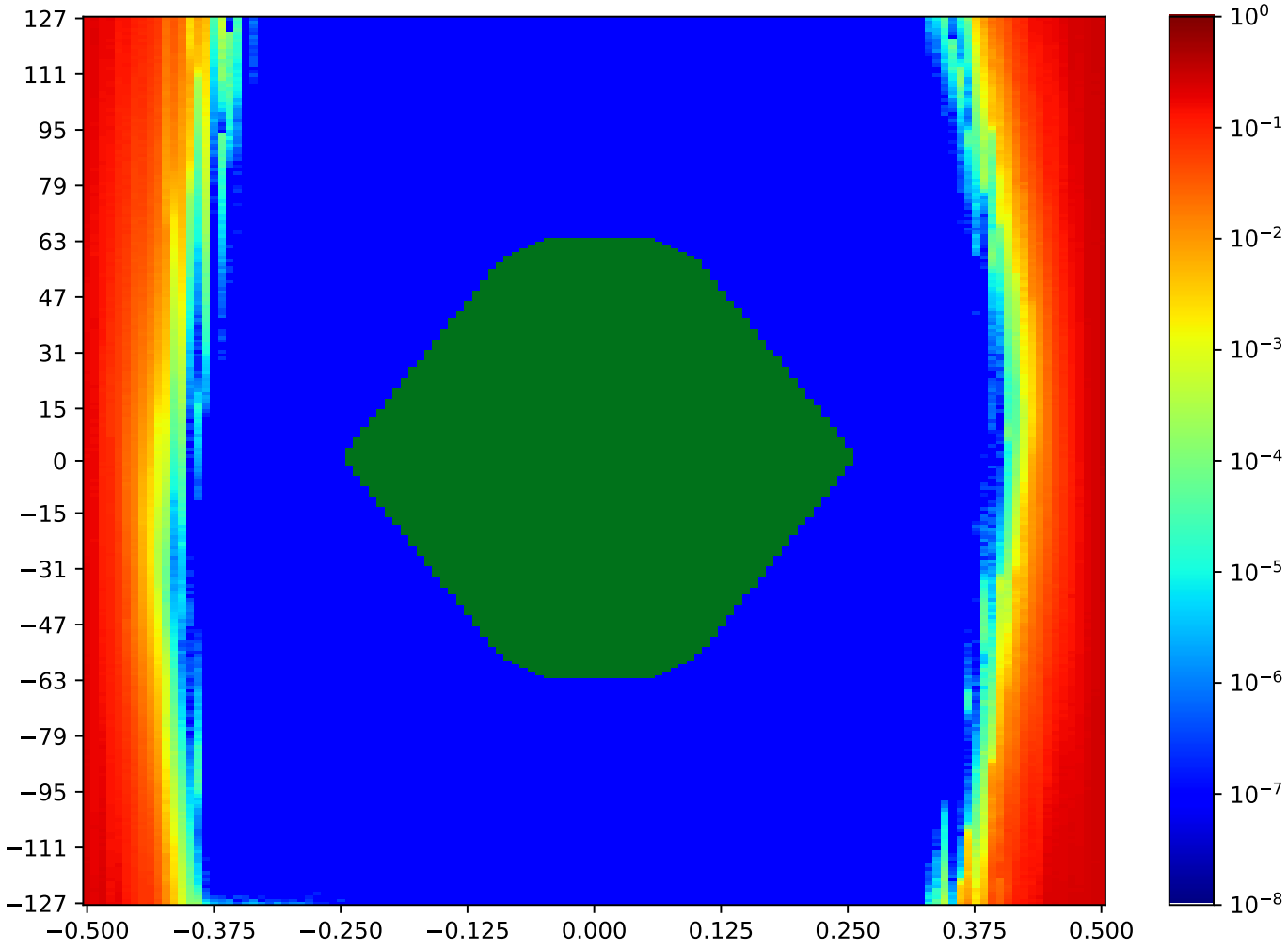


Figure 5.187: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15 MSP_A TX1 MSP_C RX10 Minipod Loopback

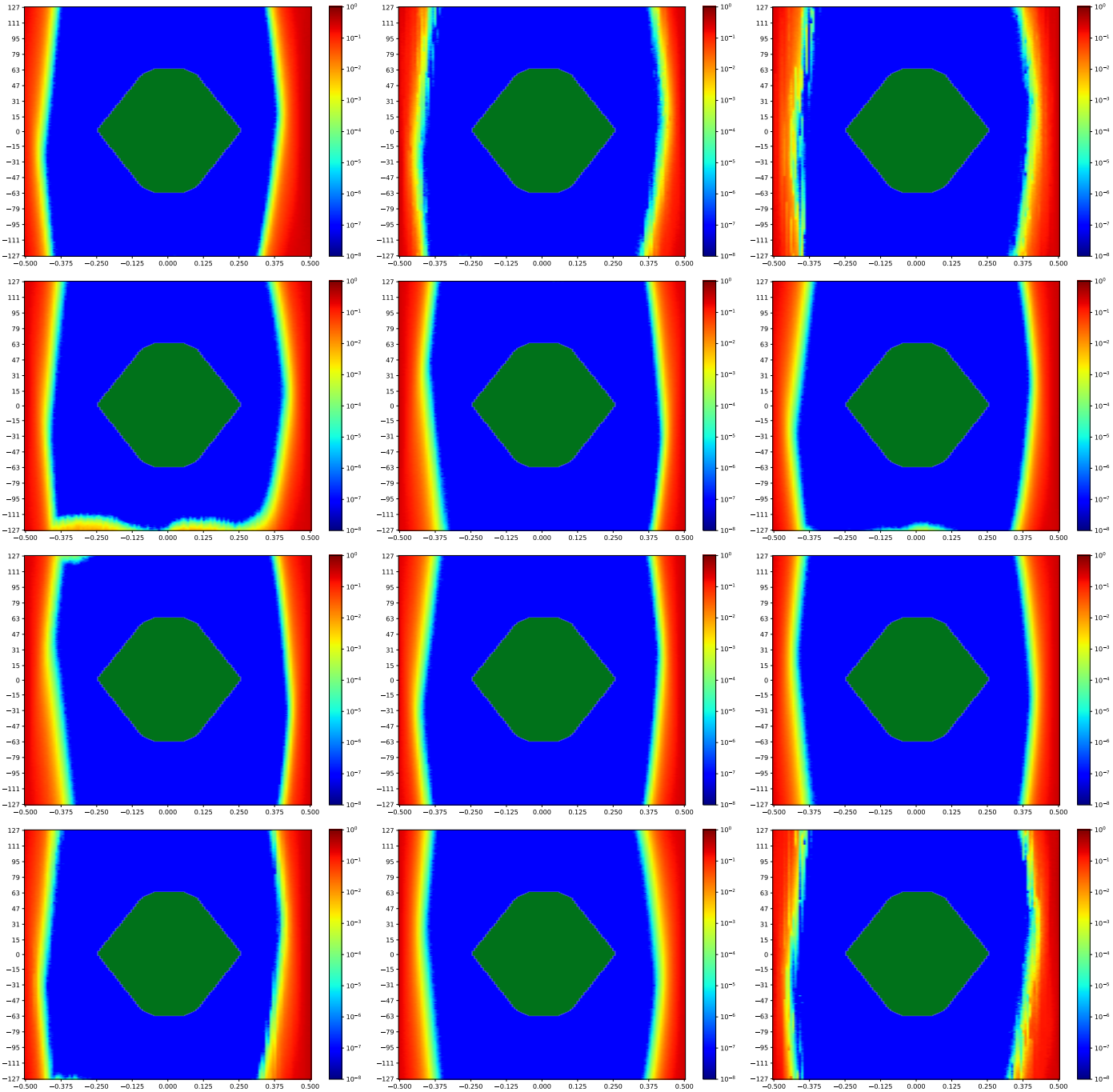


Figure 5.188: MSP_A TX1 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.201.

5.15.1 MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Table 5.174: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:39:40		2019-Nov-26 14:41:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24430	101	78.29%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

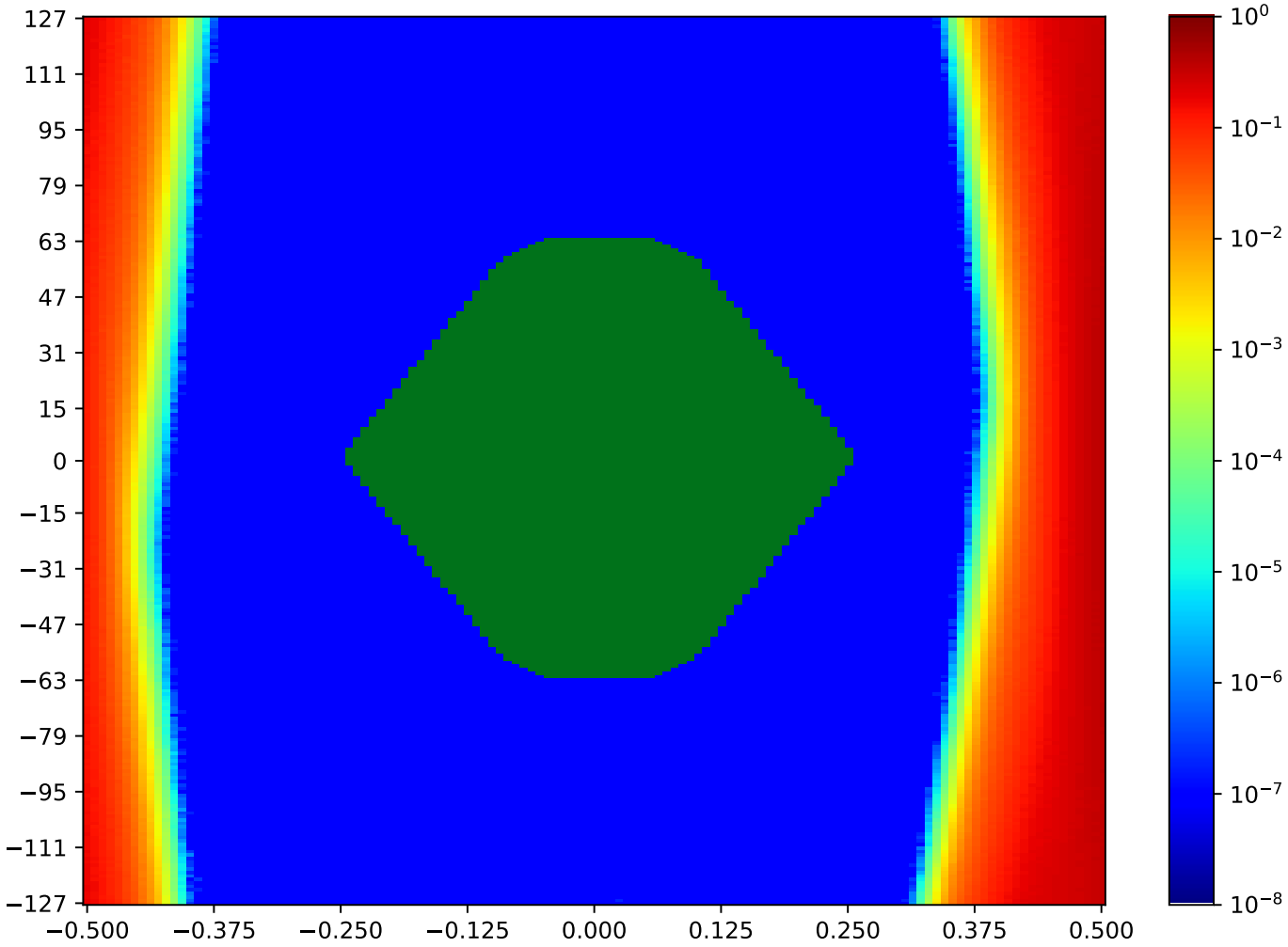


Figure 5.189: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.2 MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Table 5.175: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:42:11		2019-Nov-26 14:43:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25045	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

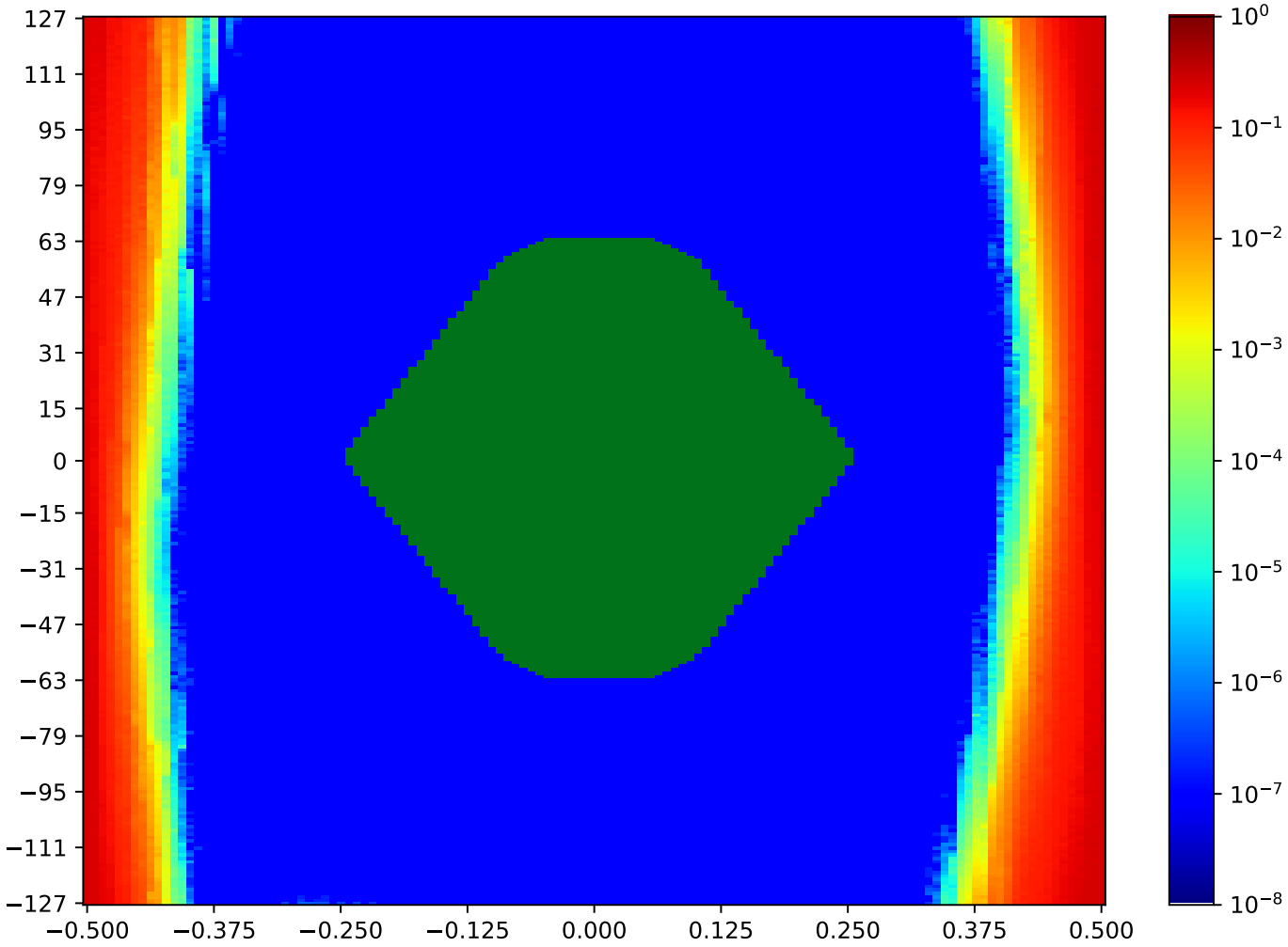


Figure 5.190: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.3 MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Table 5.176: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:43:25		2019-Nov-26 14:44:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24117	99	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

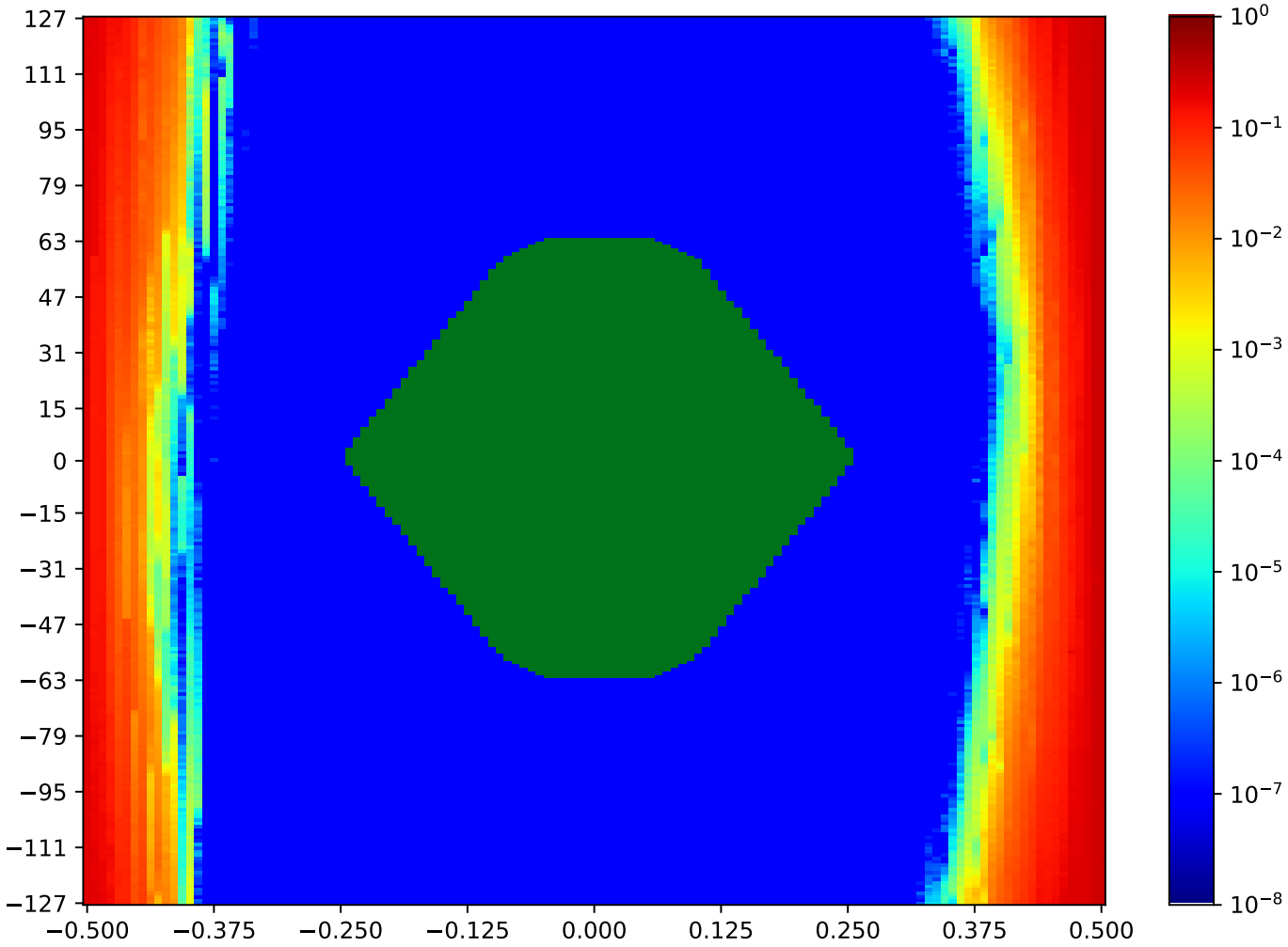


Figure 5.191: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.4 MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Table 5.177: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:37:22		2019-Nov-26 14:38:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23067	100	77.52%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

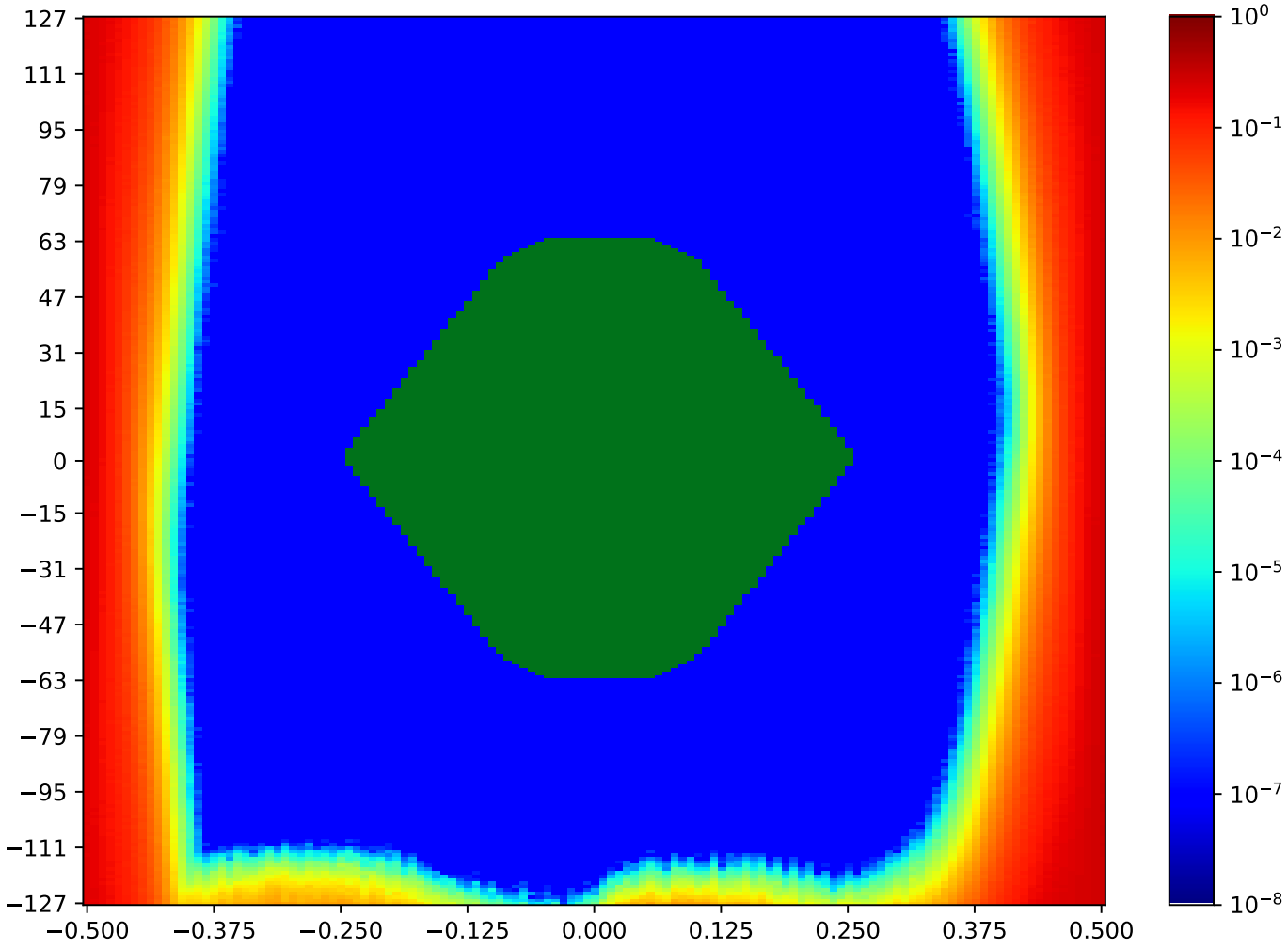


Figure 5.192: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.5 MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Table 5.178: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:47:00		2019-Nov-26 14:48:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24295	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

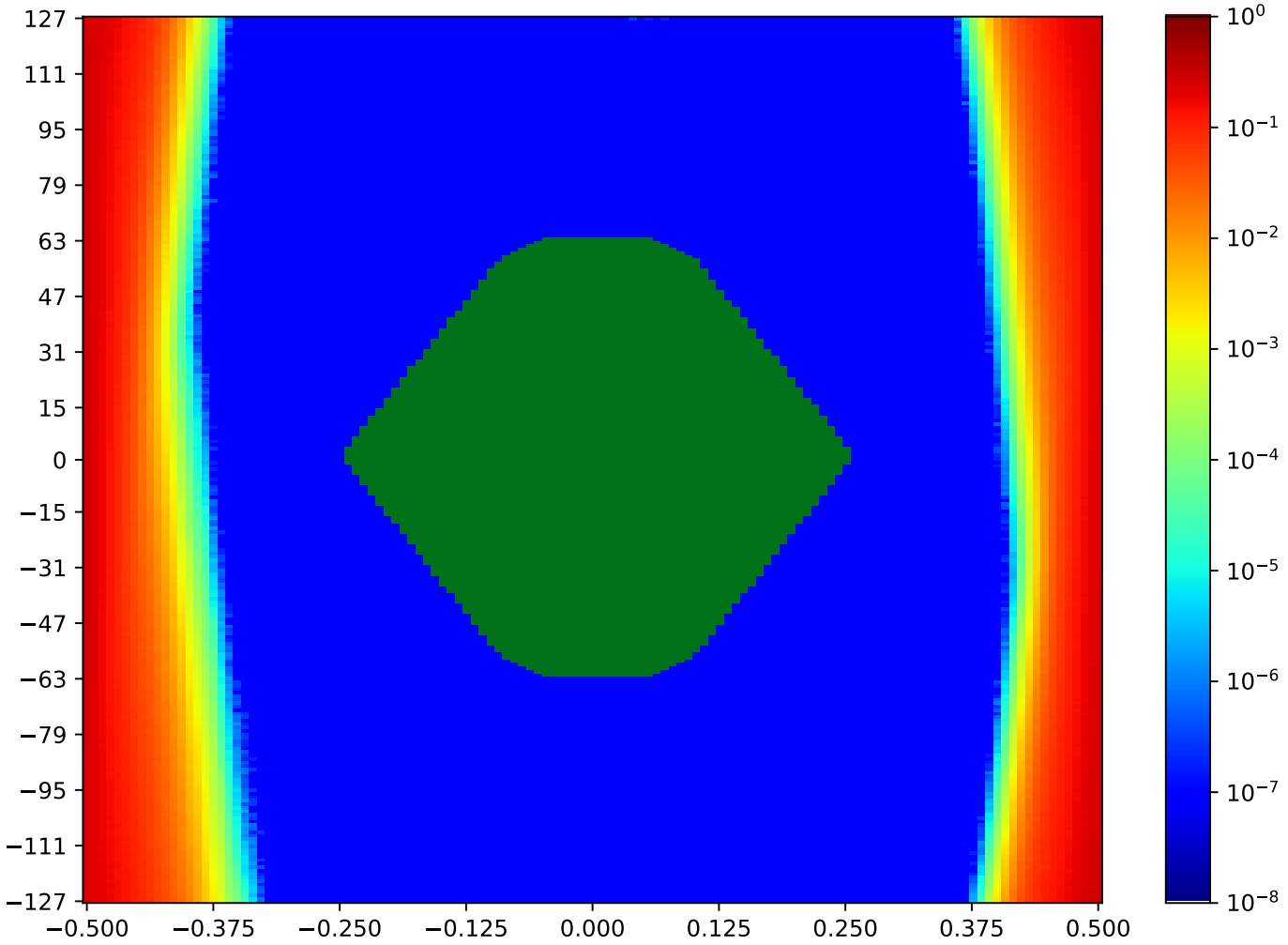


Figure 5.193: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.6 MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Table 5.179: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:36:14		2019-Nov-26 14:37:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24147	99	76.74%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

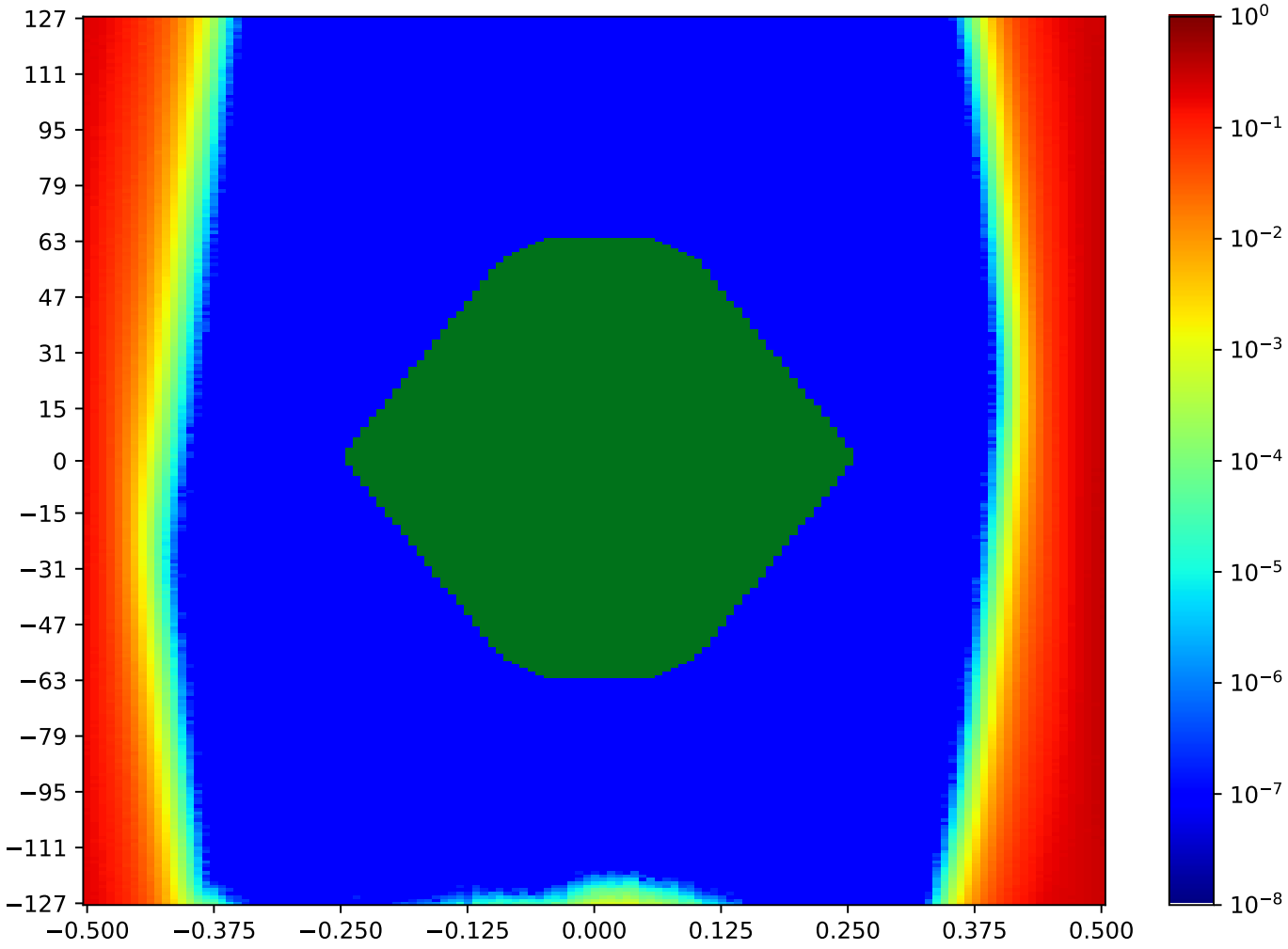


Figure 5.194: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.7 MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Table 5.180: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:49:16		2019-Nov-26 14:50:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24279	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

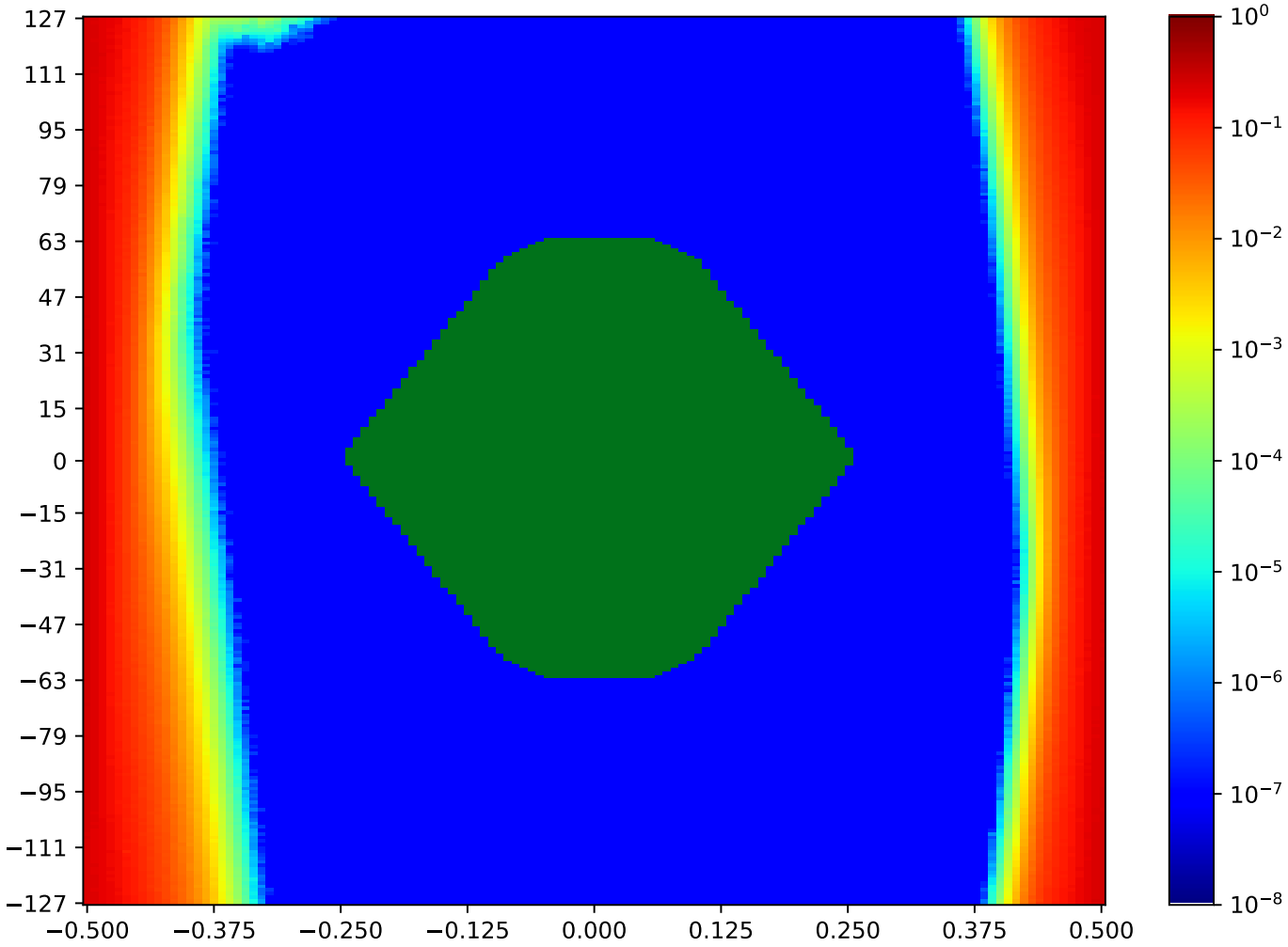


Figure 5.195: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.8 MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Table 5.181: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:38:32		2019-Nov-26 14:39:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24788	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

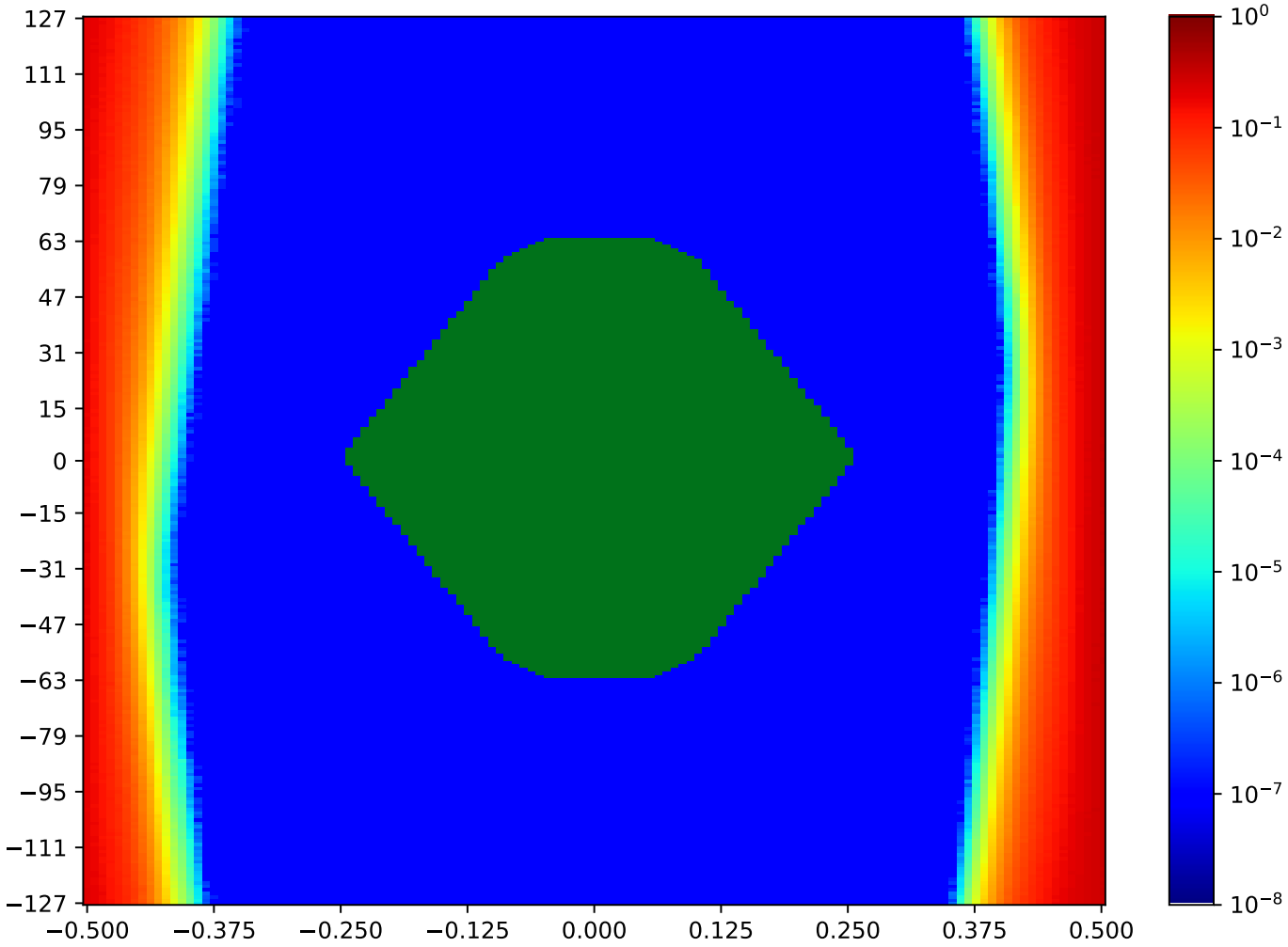


Figure 5.196: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.9 MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Table 5.182: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:48:08		2019-Nov-26 14:49:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24551	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

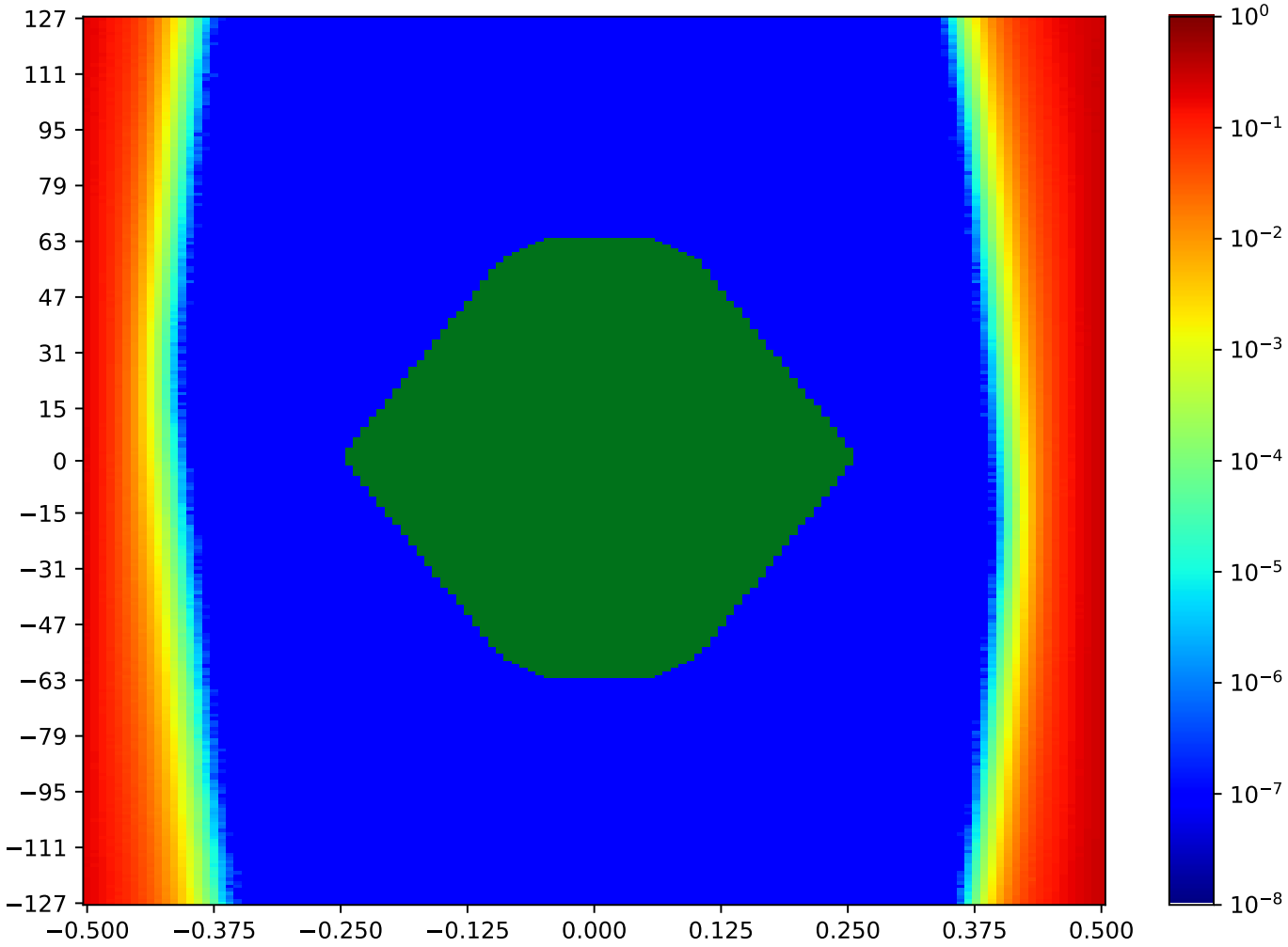


Figure 5.197: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.10 MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Table 5.183: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:41:03		2019-Nov-26 14:42:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24544	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

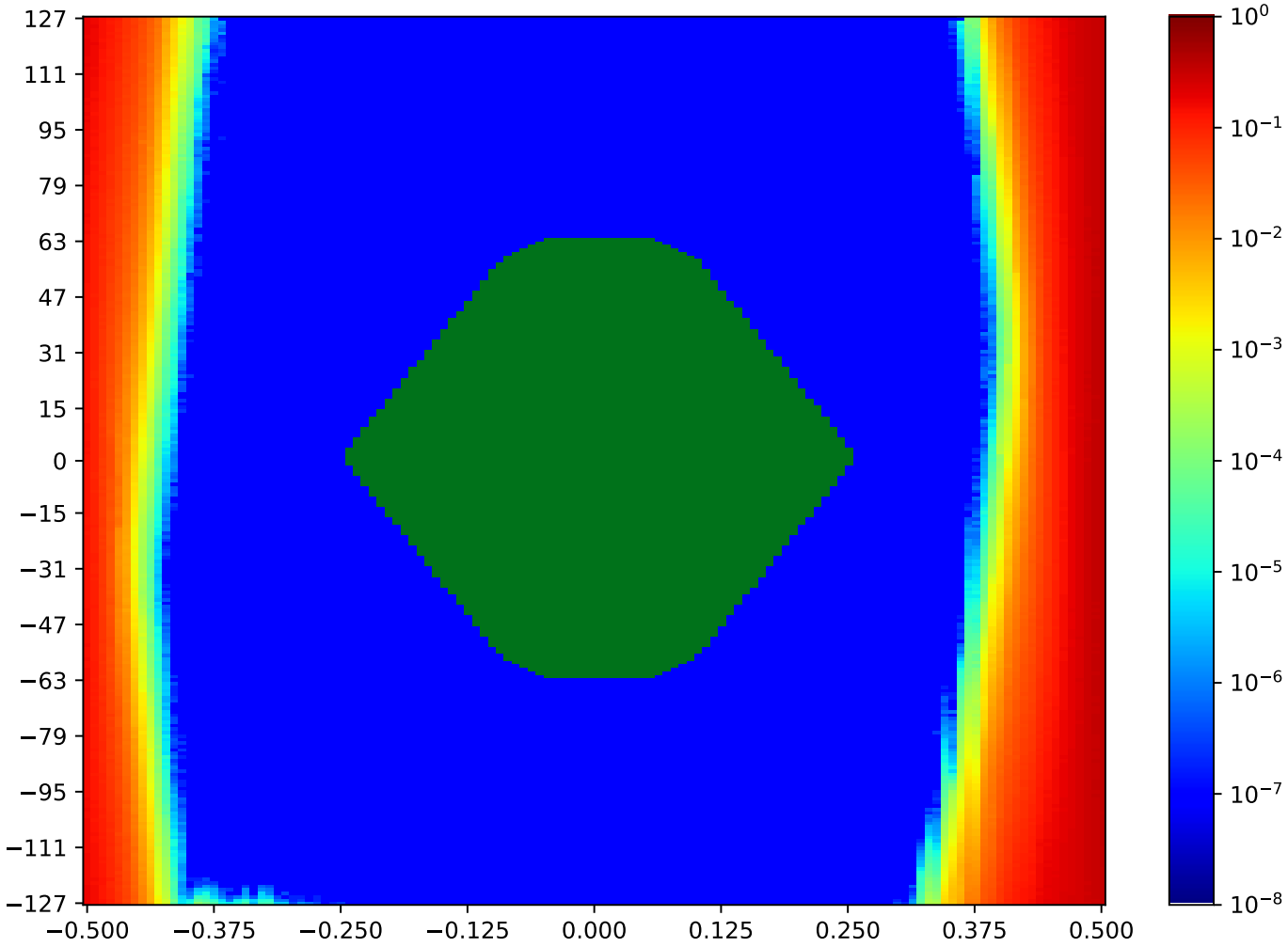


Figure 5.198: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.11 MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Table 5.184: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:45:53		2019-Nov-26 14:47:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23971	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

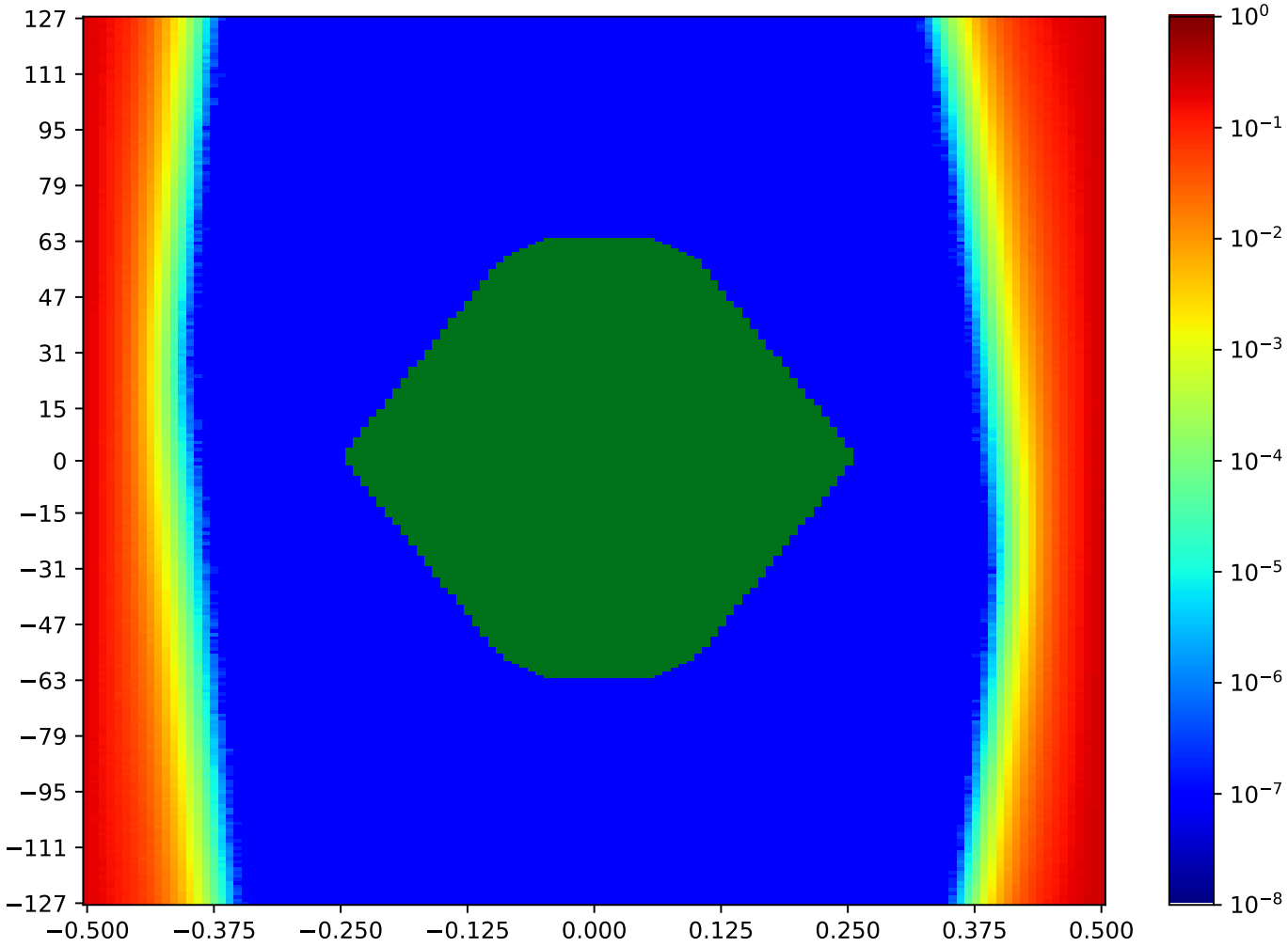


Figure 5.199: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.15.12 MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Table 5.185: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:44:45		2019-Nov-26 14:45:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24833	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

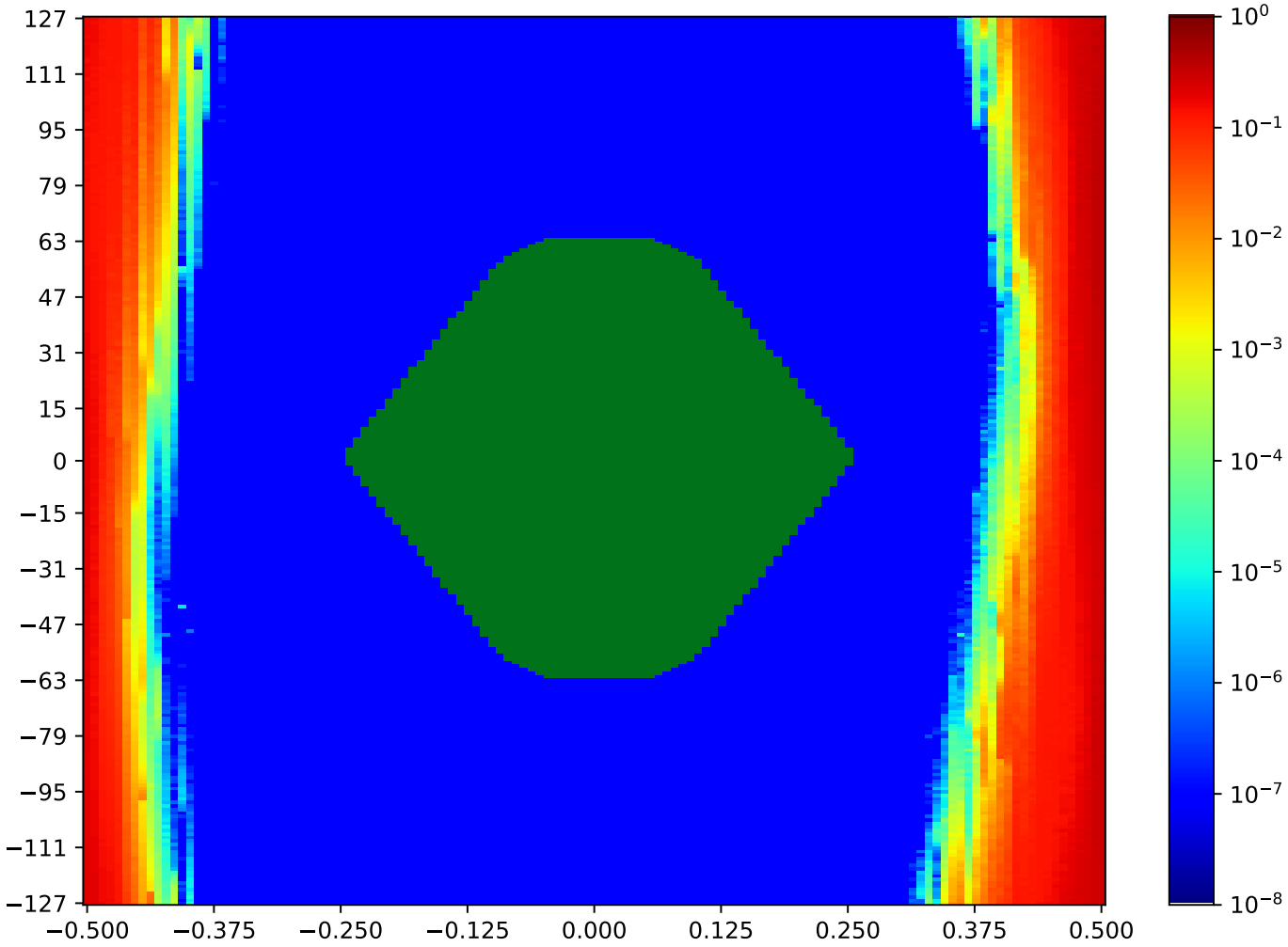


Figure 5.200: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16 MSP_A TX2 MSP_C RX11 Minipod Loopback

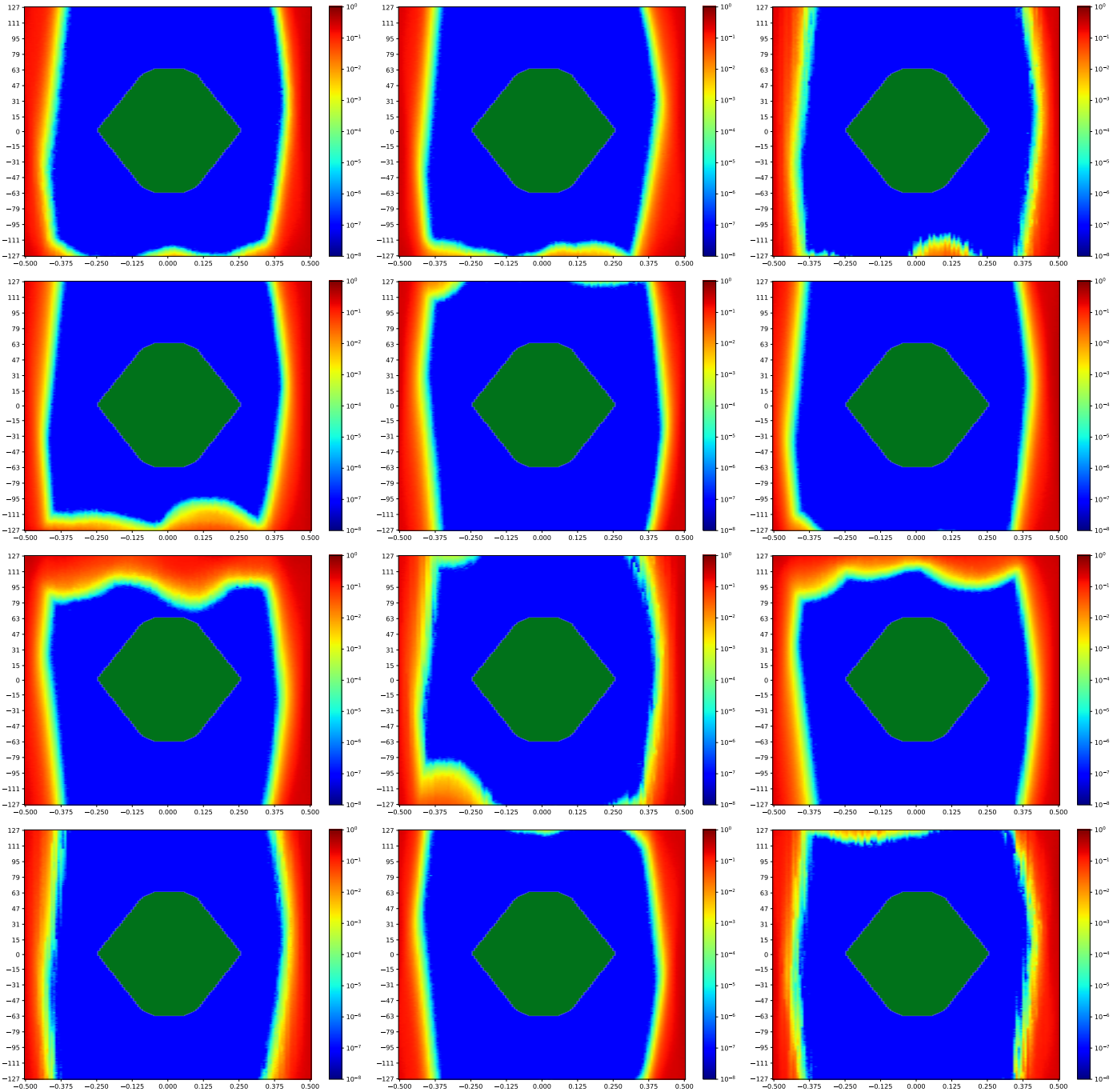


Figure 5.201: MSP_A TX2 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.214.

5.16.1 MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Table 5.186: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:53:47		2019-Nov-26 14:54:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23442	98	75.19%	243	95.29%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

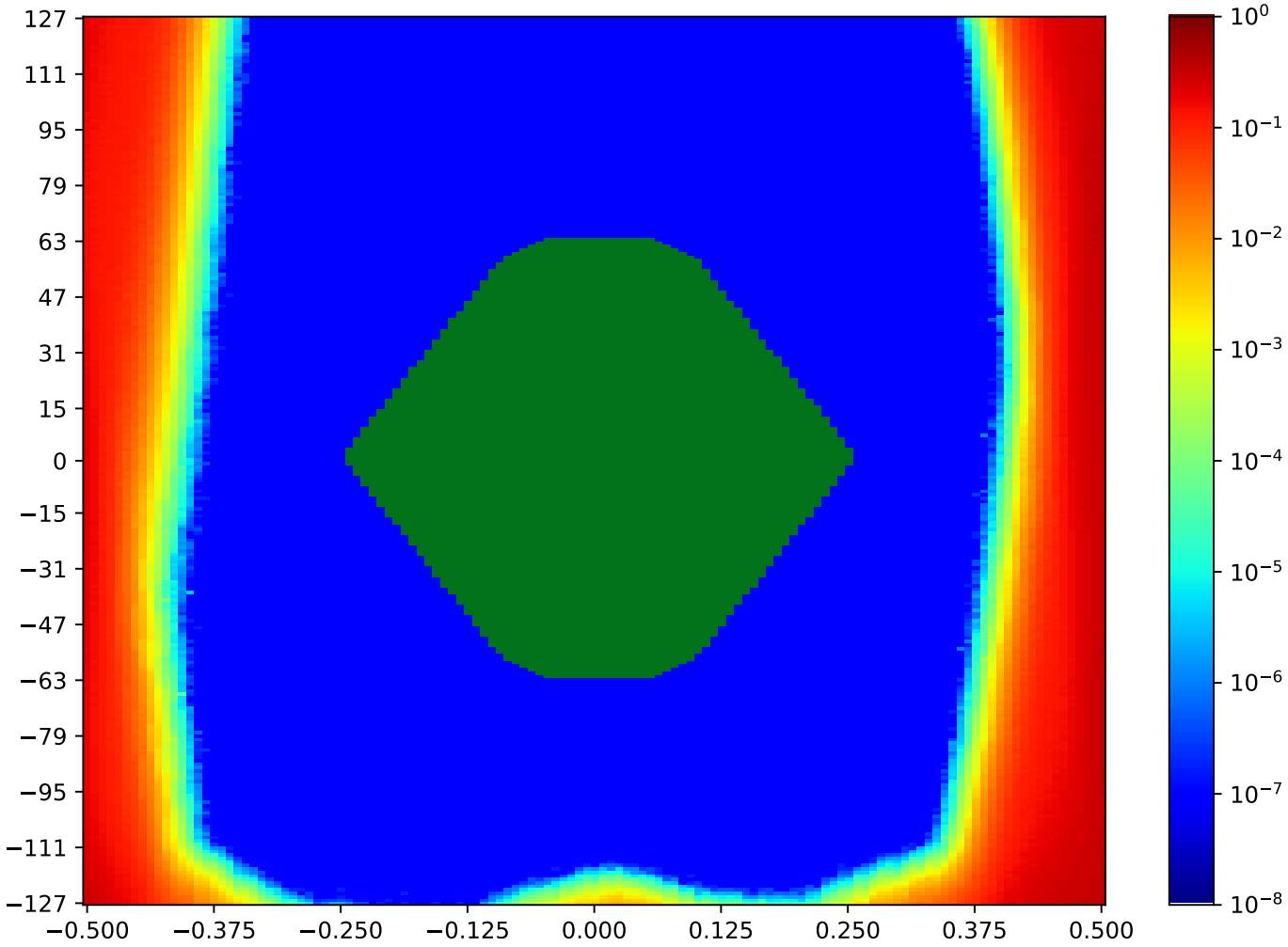


Figure 5.202: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.2 MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Table 5.187: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:51:32		2019-Nov-26 14:52:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22517	96	74.42%	245	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

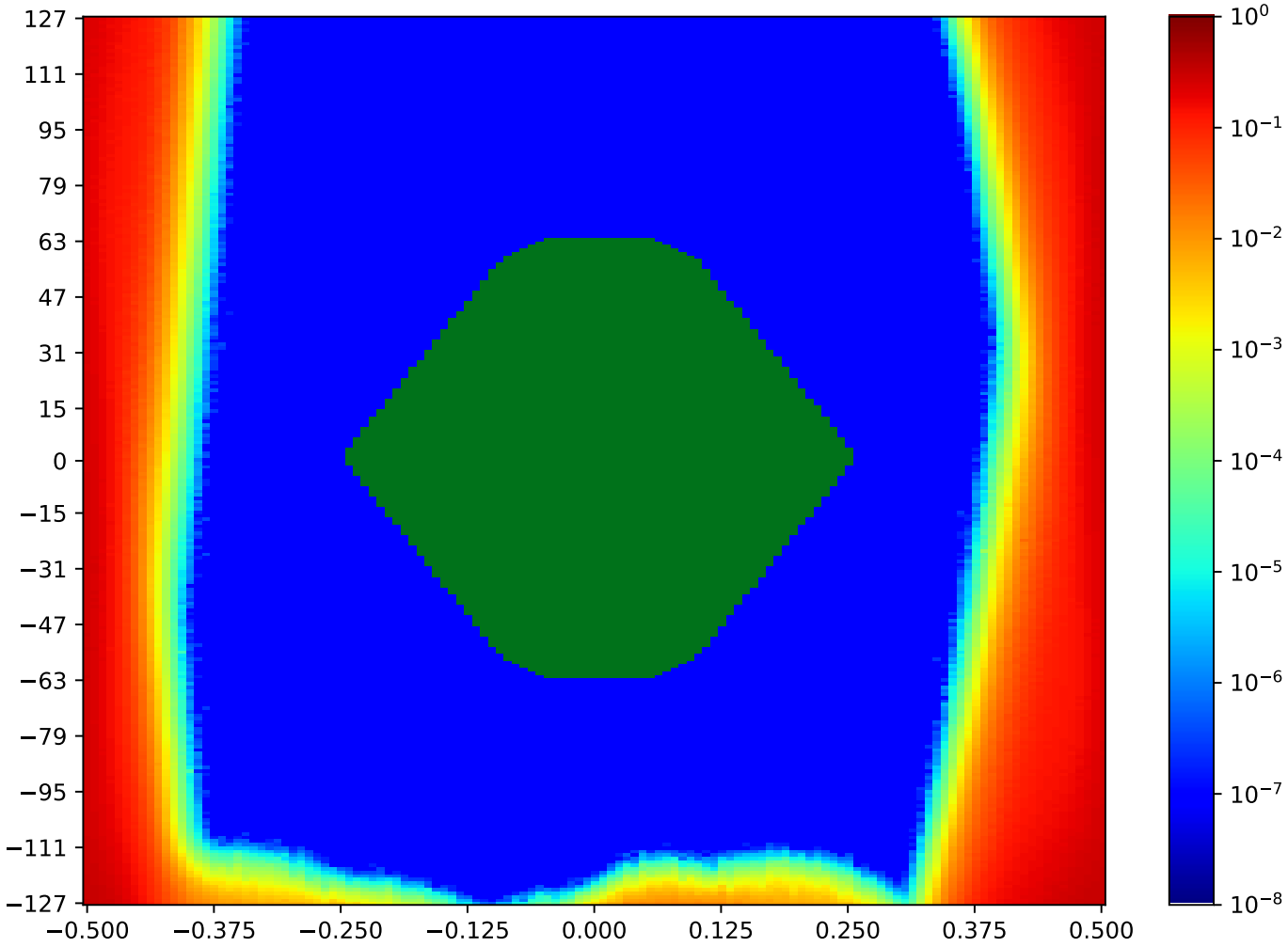


Figure 5.203: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.3 MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Table 5.188: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:57:24		2019-Nov-26 14:58:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23730	99	76.74%	239	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

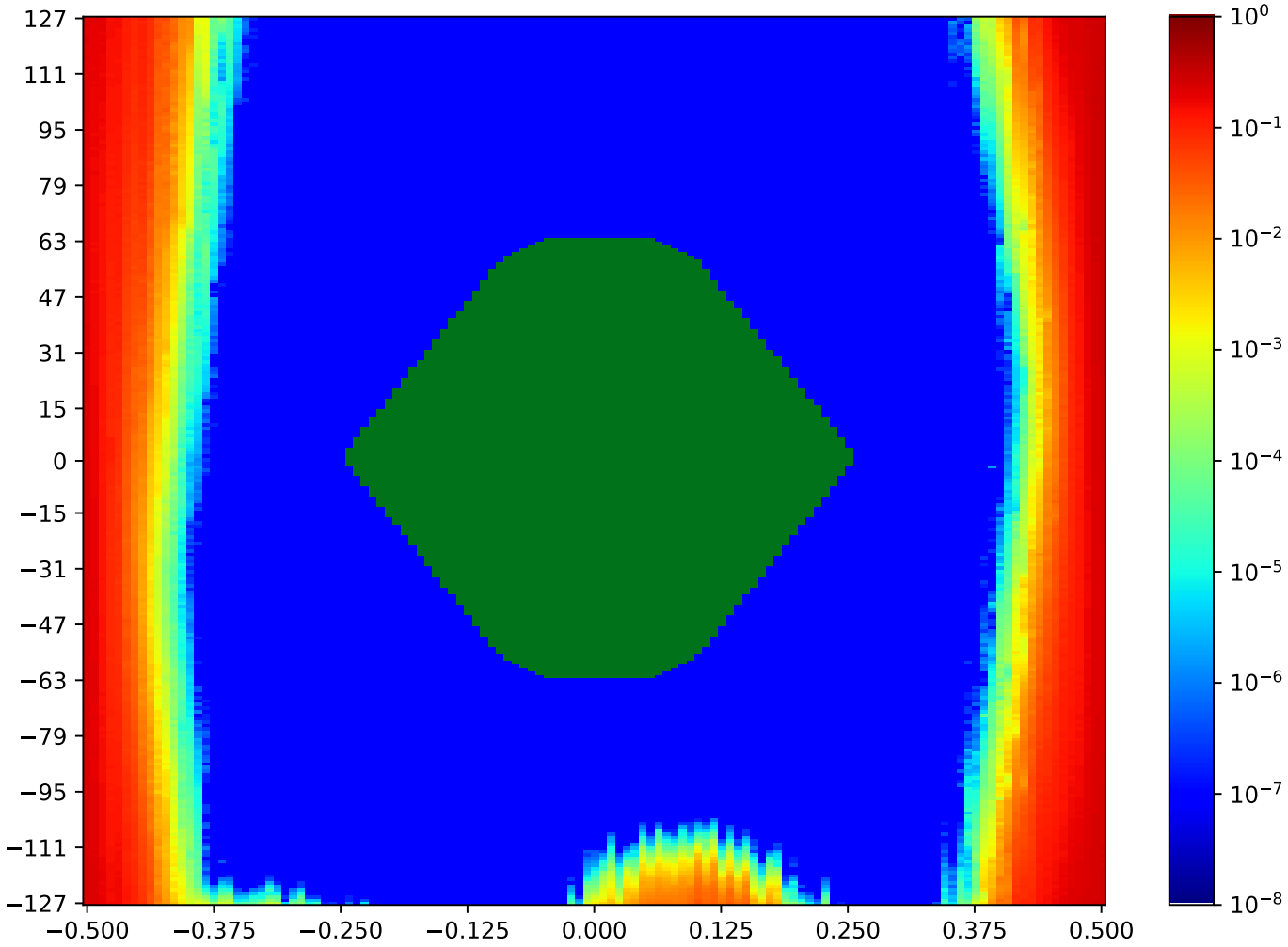


Figure 5.204: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.4 MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Table 5.189: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:50:24		2019-Nov-26 14:51:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22169	100	77.52%	233	90.98%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

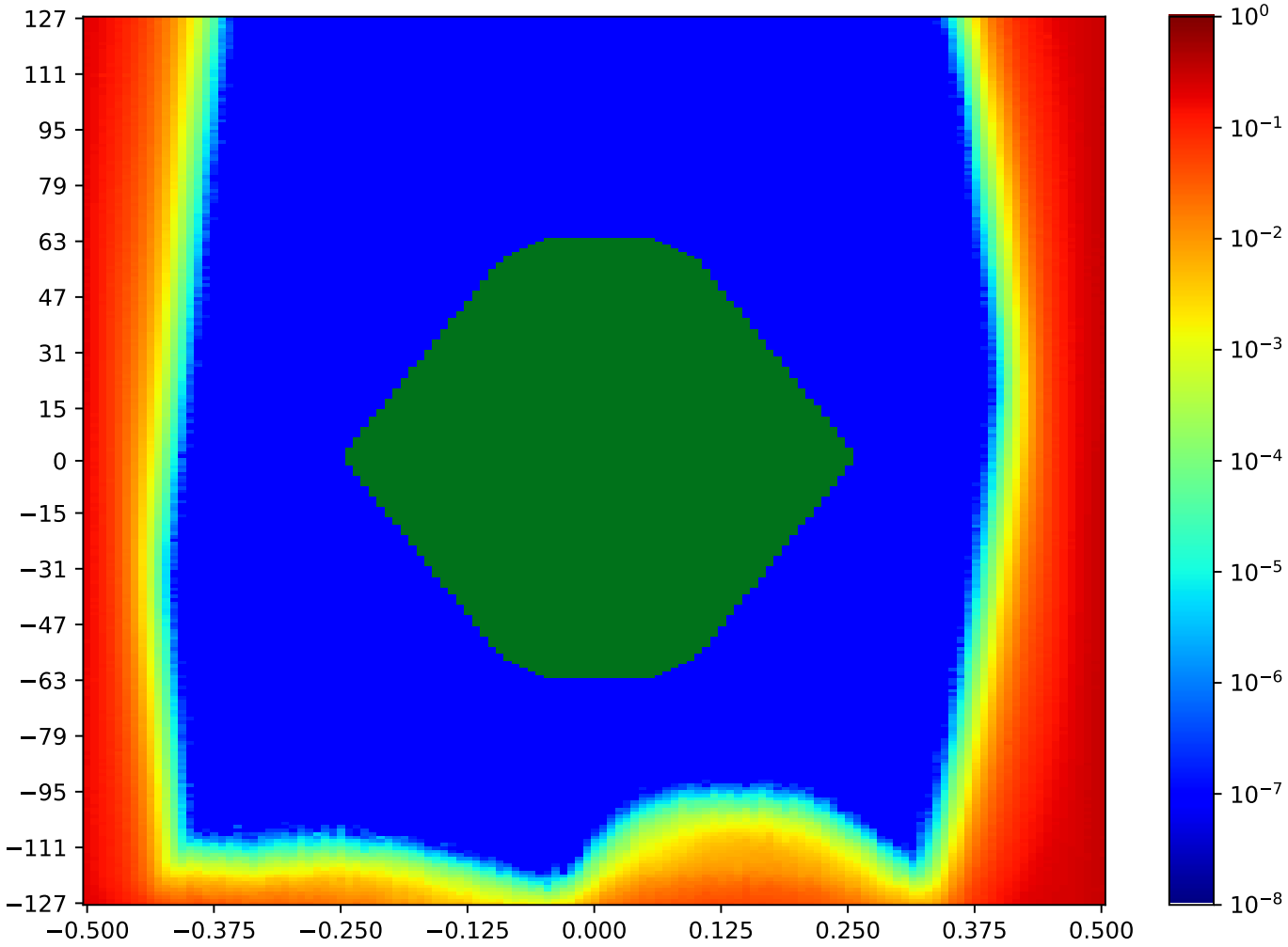


Figure 5.205: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.5 MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Table 5.190: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:01:04		2019-Nov-26 15:02:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23993	98	75.97%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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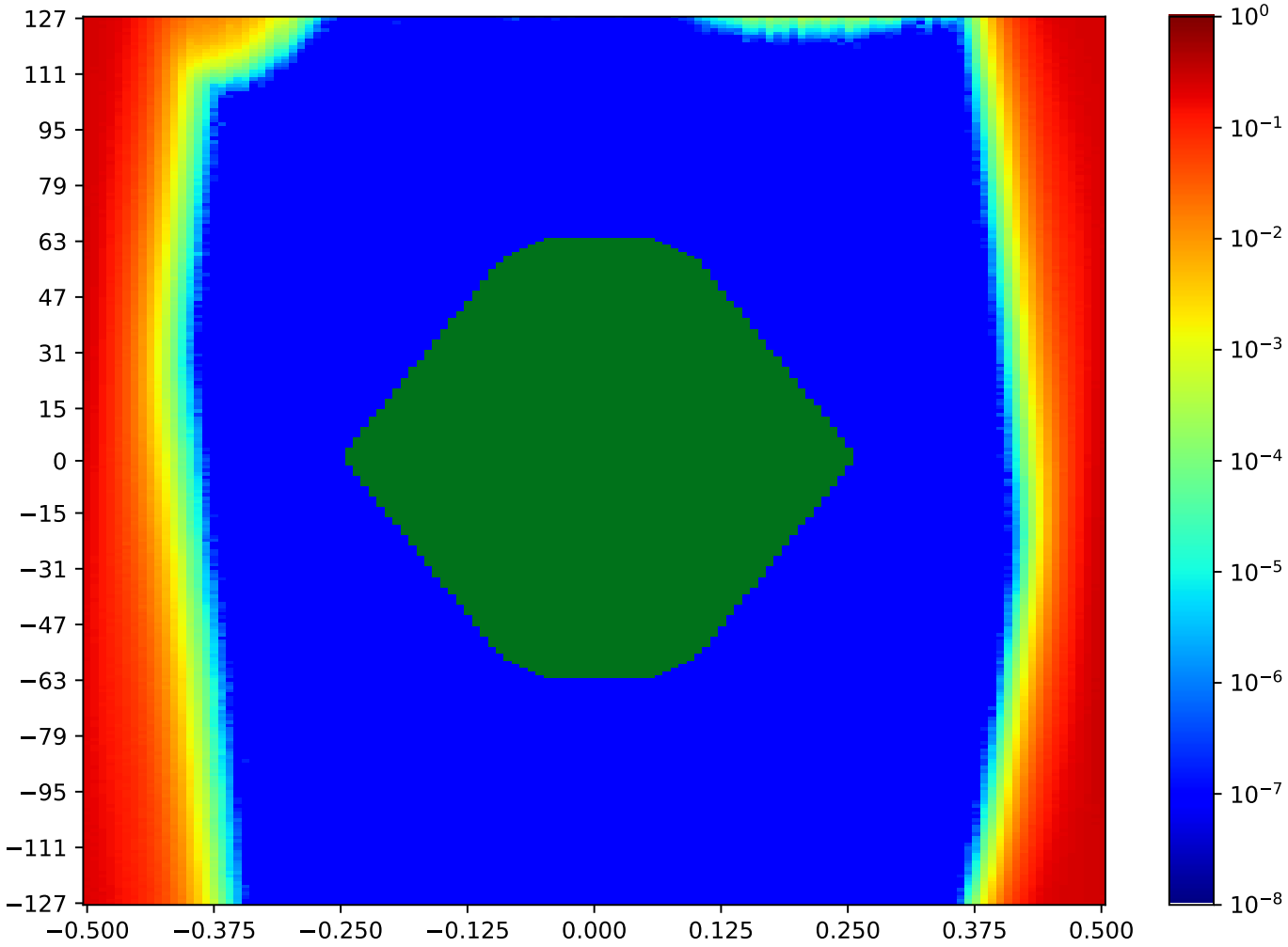


Figure 5.206: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.6 MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Table 5.191: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:52:39		2019-Nov-26 14:53:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24173	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

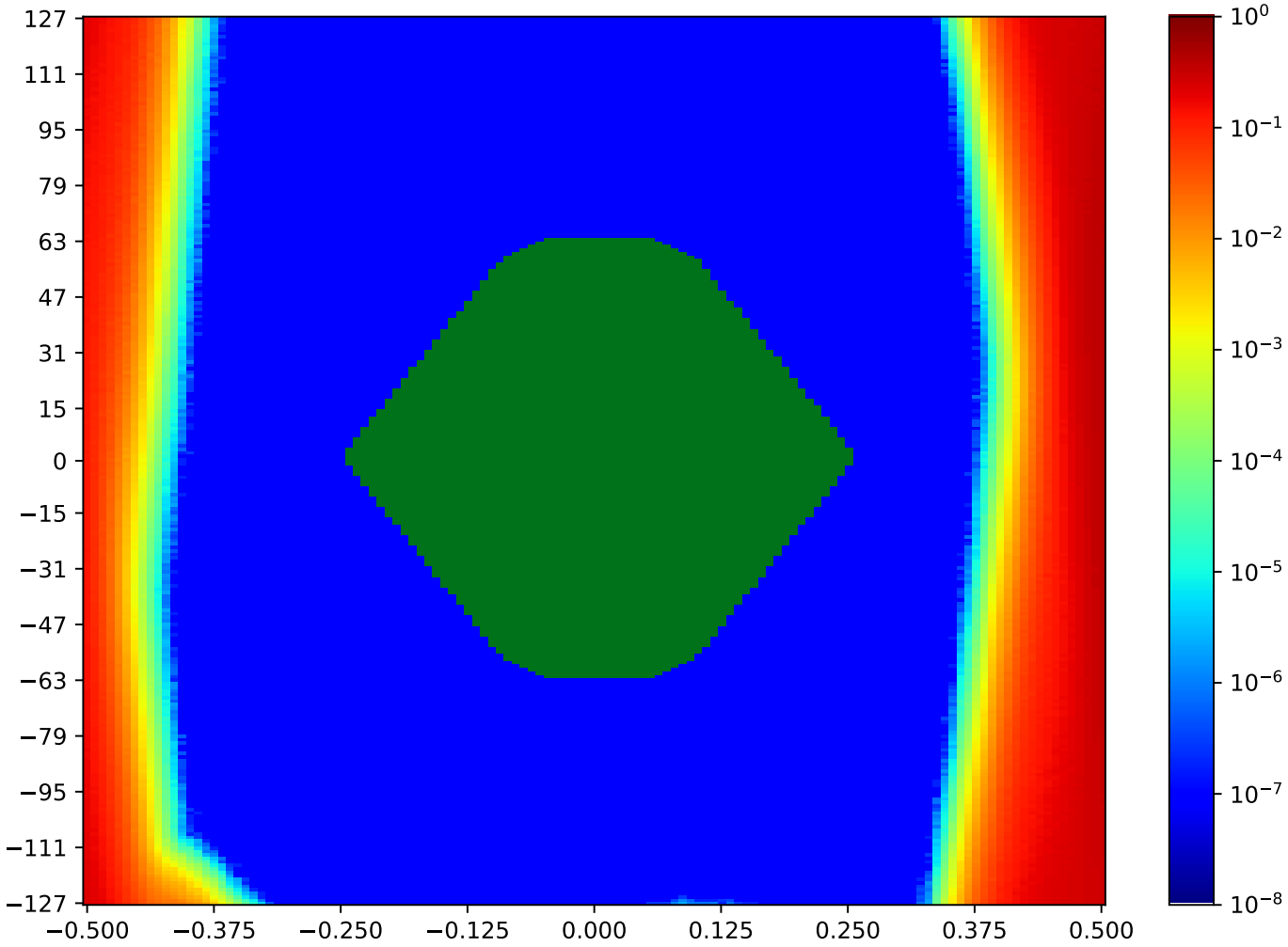


Figure 5.207: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.7 MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Table 5.192: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:03:32		2019-Nov-26 15:04:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	19541	97	75.19%	201	78.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

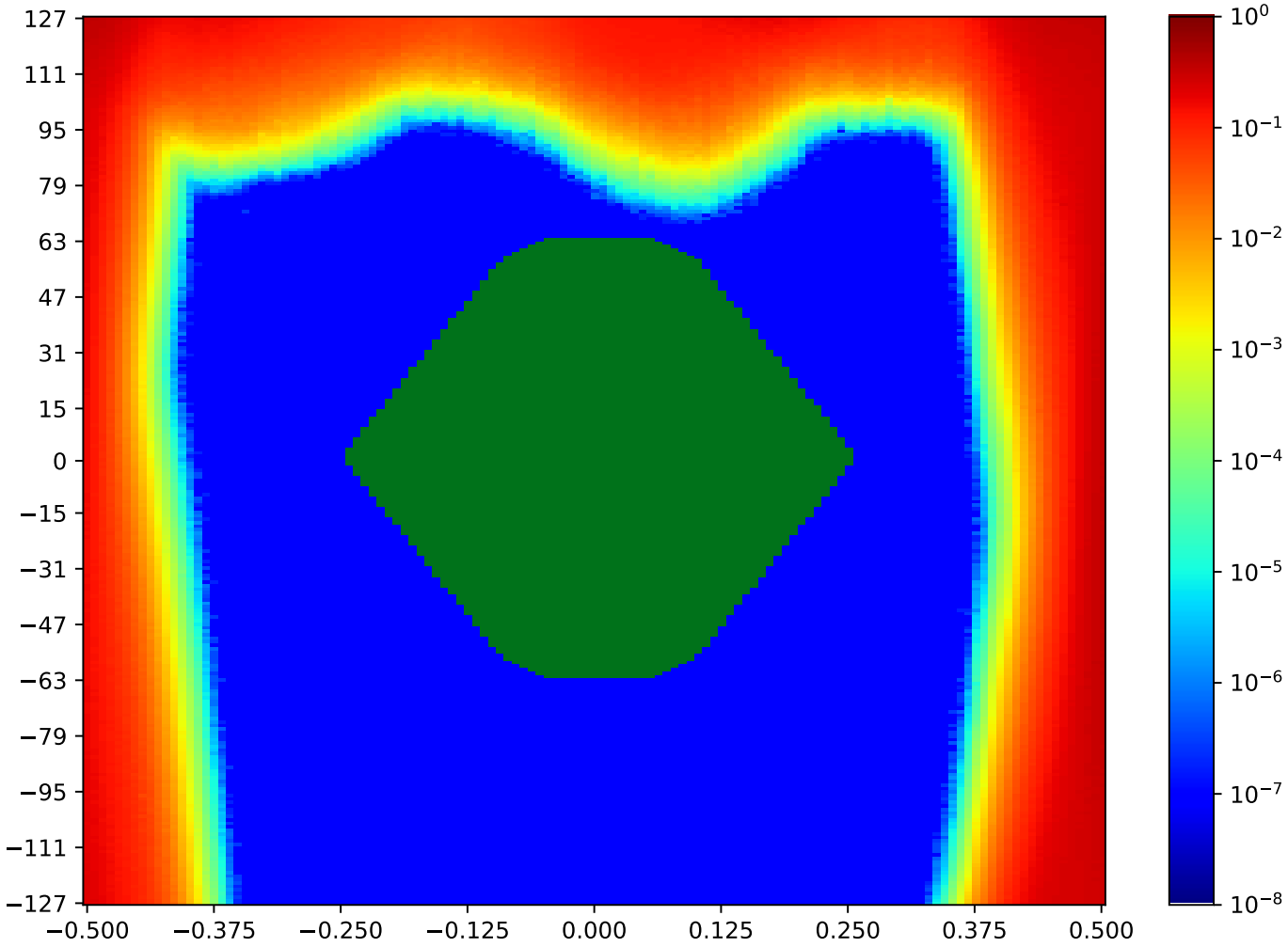


Figure 5.208: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.8 MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Table 5.193: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:54:55		2019-Nov-26 14:56:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22368	101	76.74%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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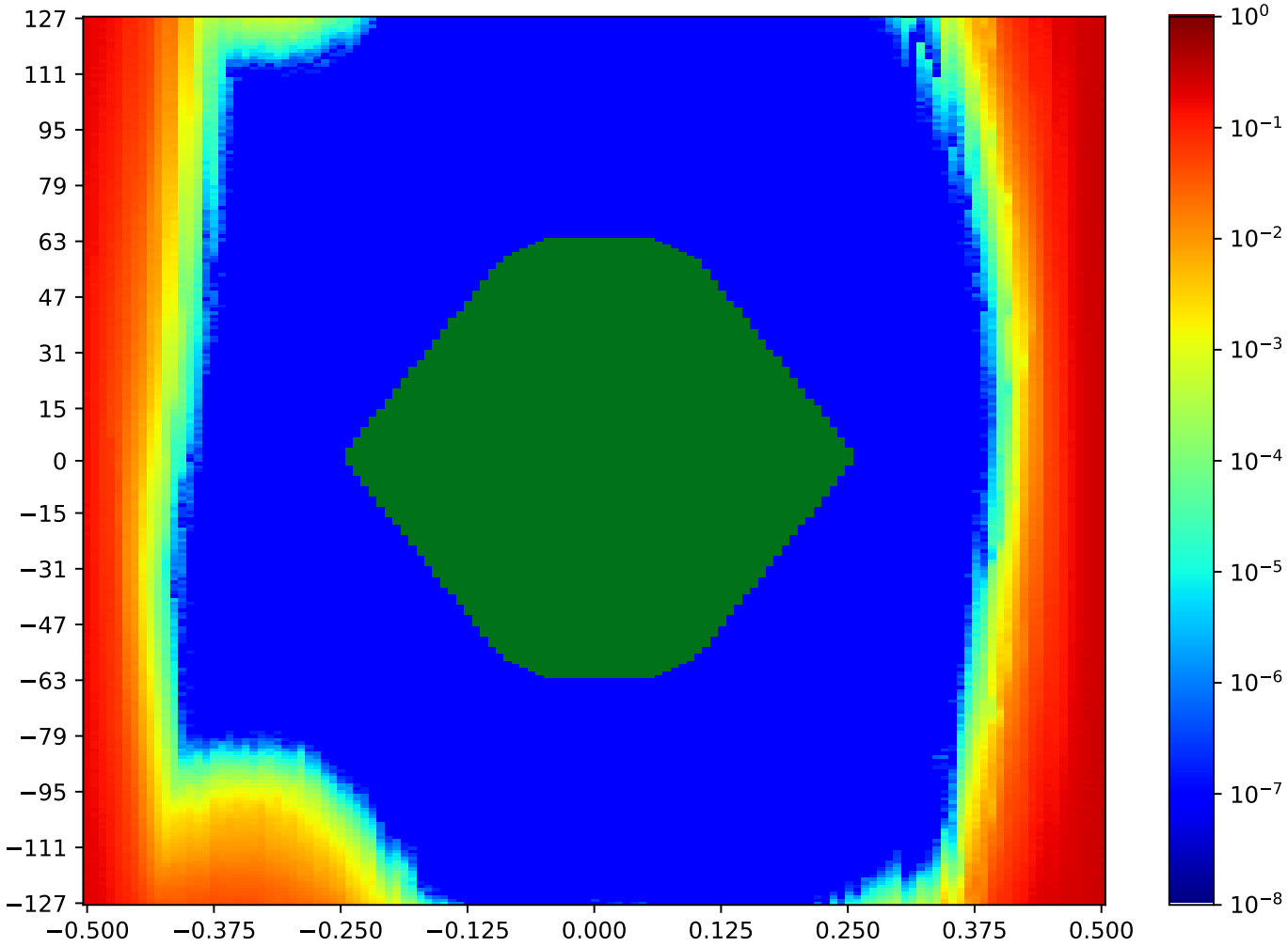


Figure 5.209: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.9 MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Table 5.194: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:02:24		2019-Nov-26 15:03:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21057	99	76.74%	237	92.94%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

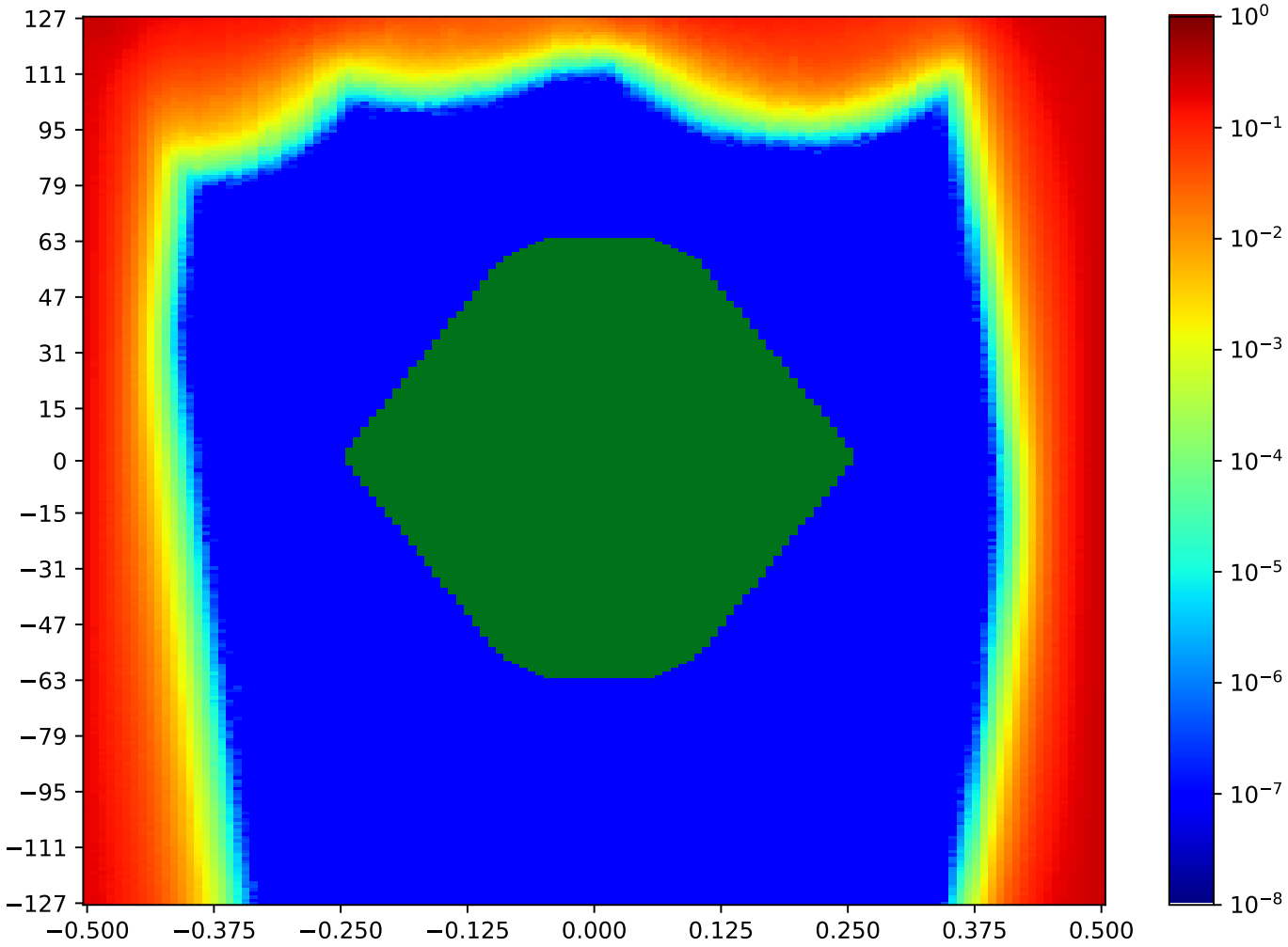


Figure 5.210: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.10 MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Table 5.195: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:56:02		2019-Nov-26 14:57:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24144	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

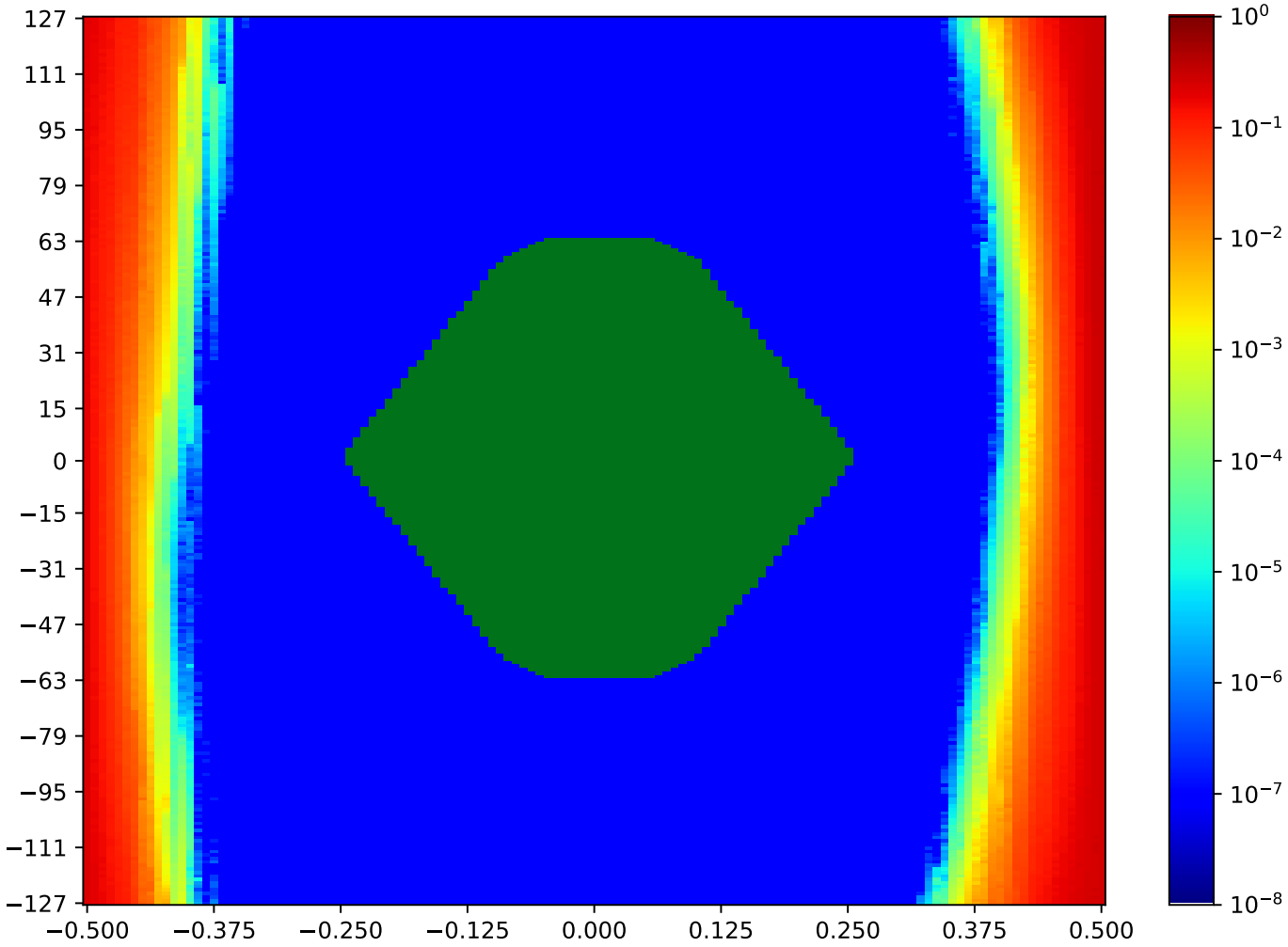


Figure 5.211: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.11 MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Table 5.196: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:59:56		2019-Nov-26 15:01:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24037	99	76.74%	246	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

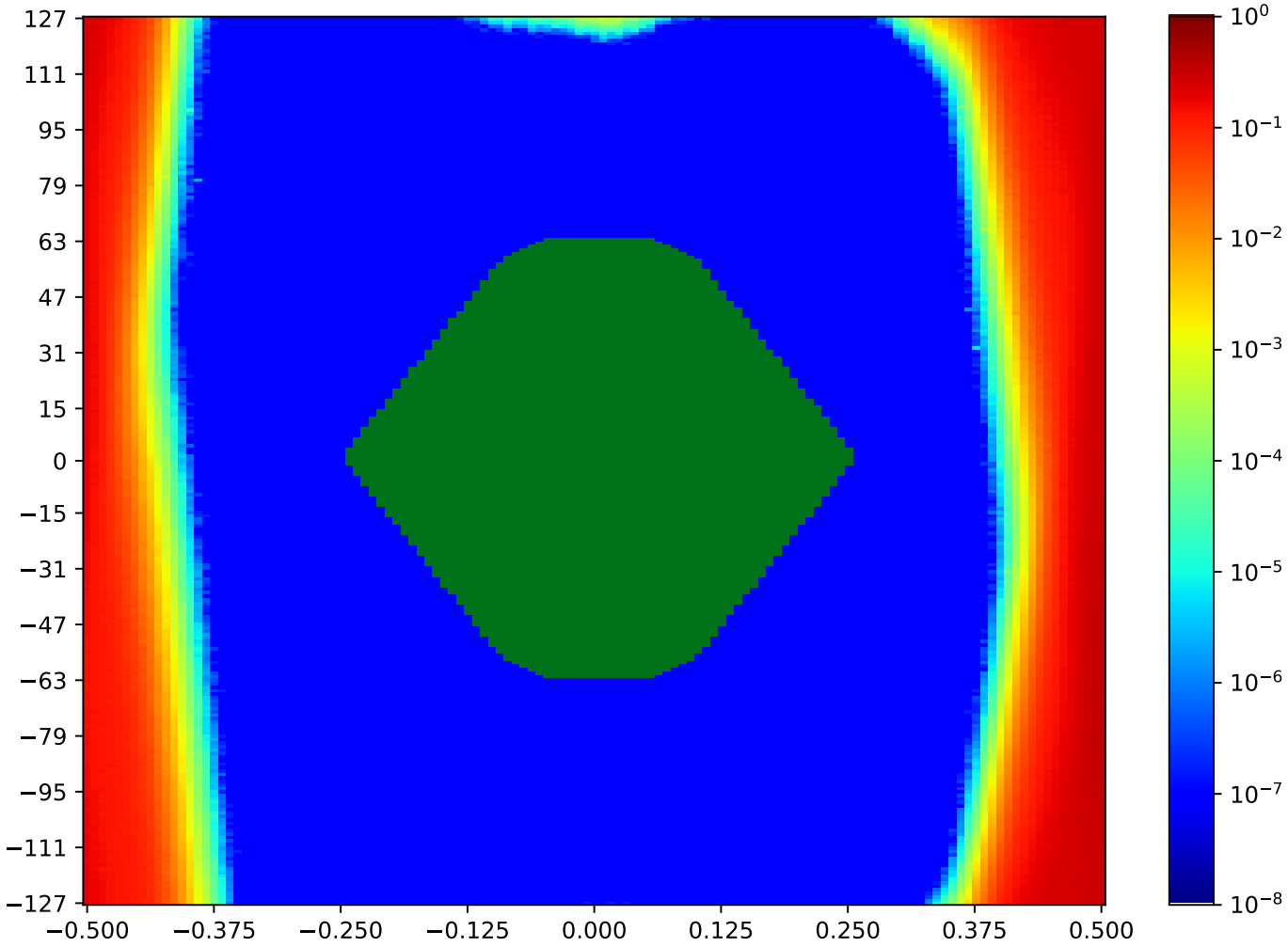


Figure 5.212: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.16.12 MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Table 5.197: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 14:58:49		2019-Nov-26 14:59:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23129	97	75.19%	244	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

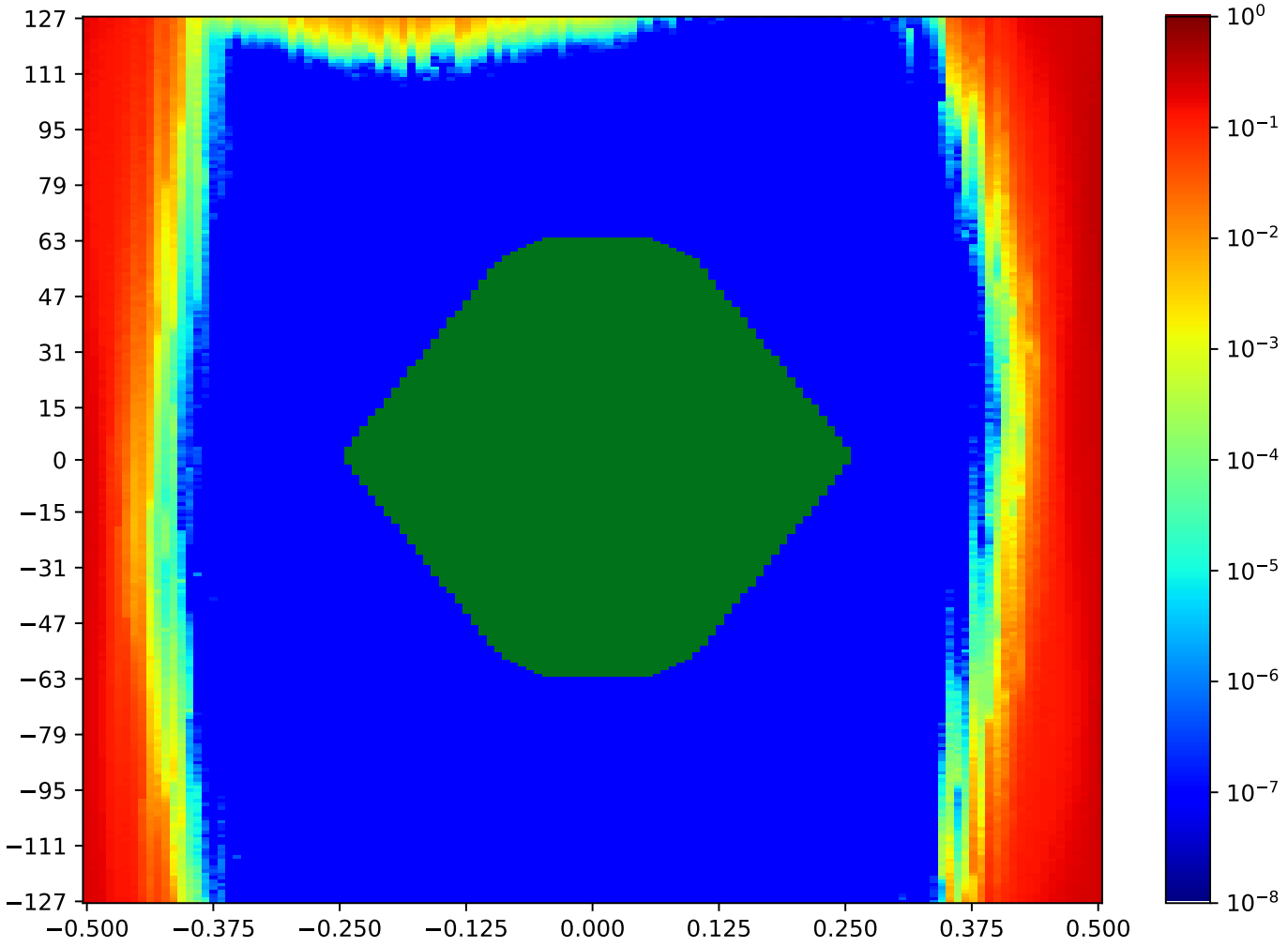


Figure 5.213: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17 MSP_C TX3 MSP_A RX1 Minipod Loopback

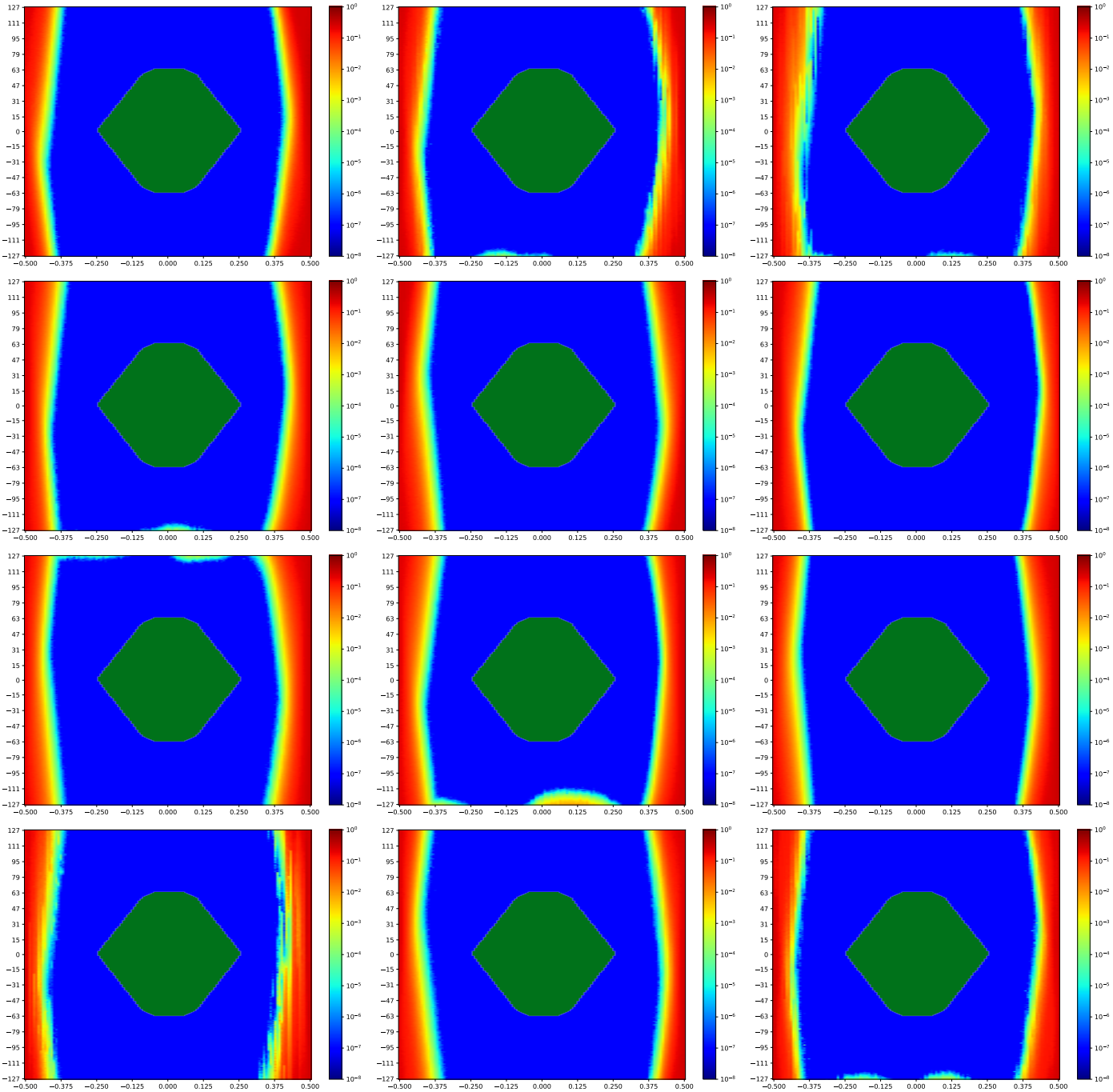


Figure 5.214: MSP_C TX3 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.227.

5.17.1 MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Table 5.198: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:08:21		2019-Nov-26 15:09:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24602	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

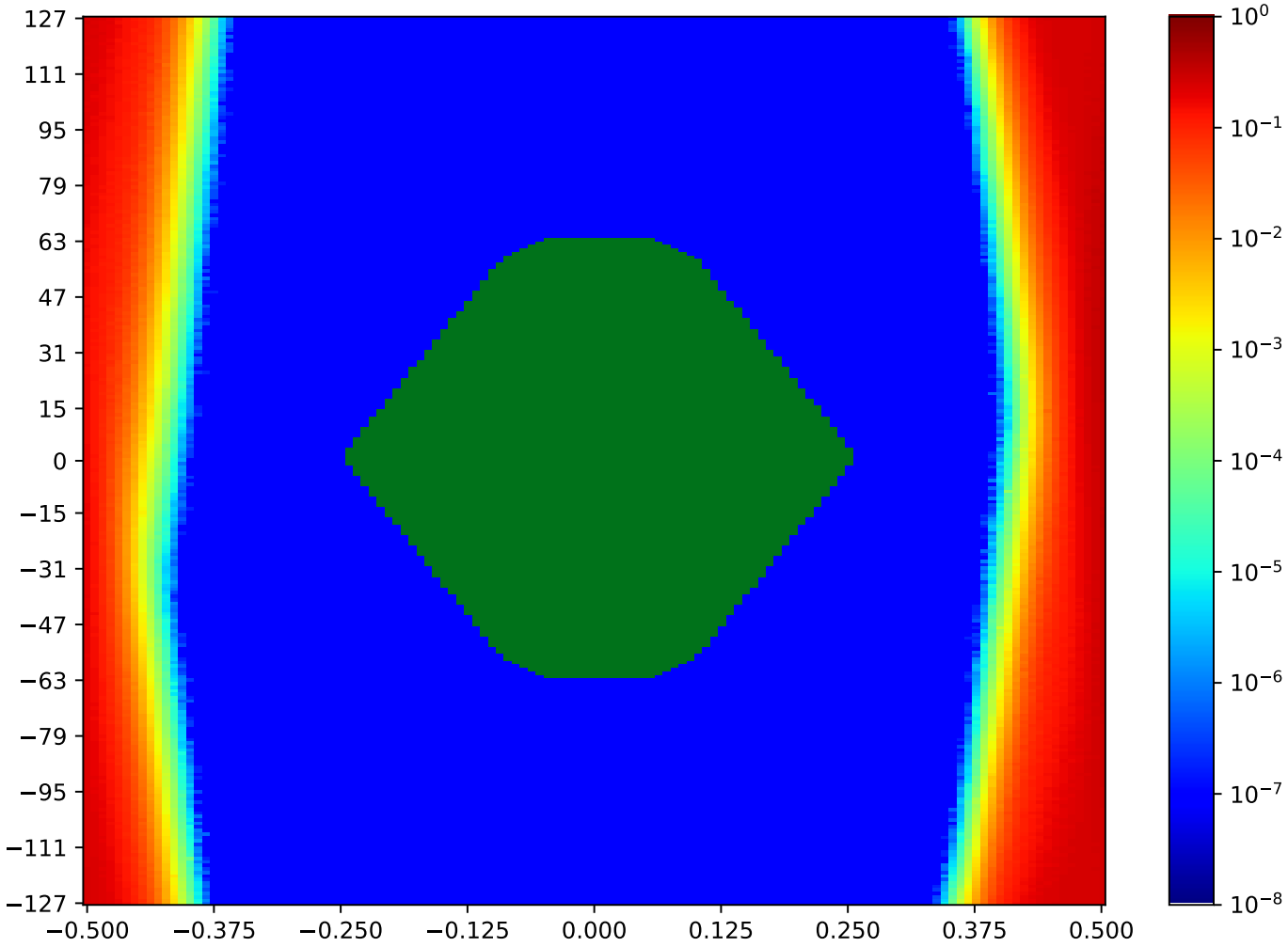


Figure 5.215: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.2 MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Table 5.199: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:10:52		2019-Nov-26 15:12:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24419	101	78.29%	250	97.65%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

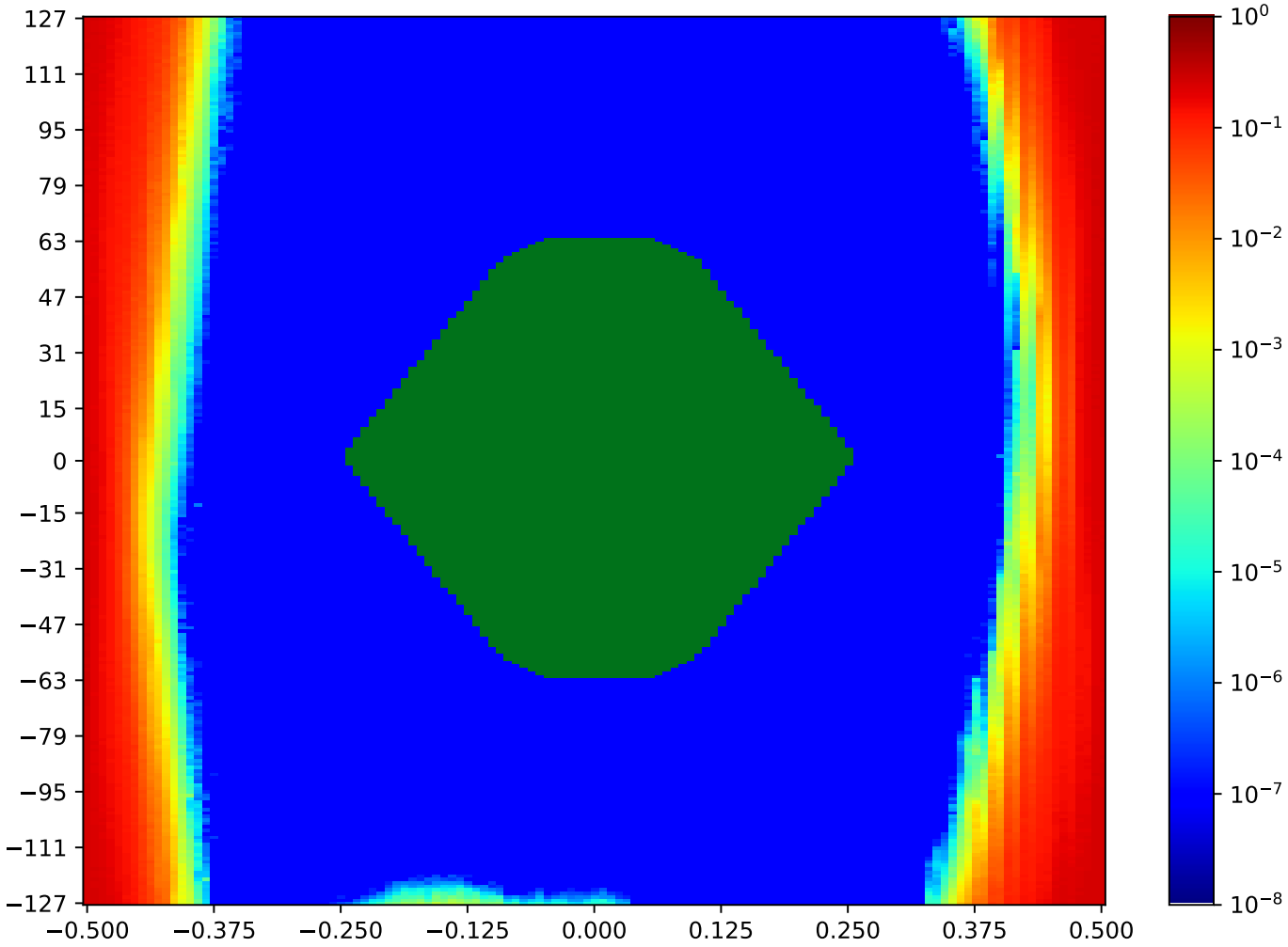


Figure 5.216: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.3 MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Table 5.200: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:12:00		2019-Nov-26 15:13:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23759	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

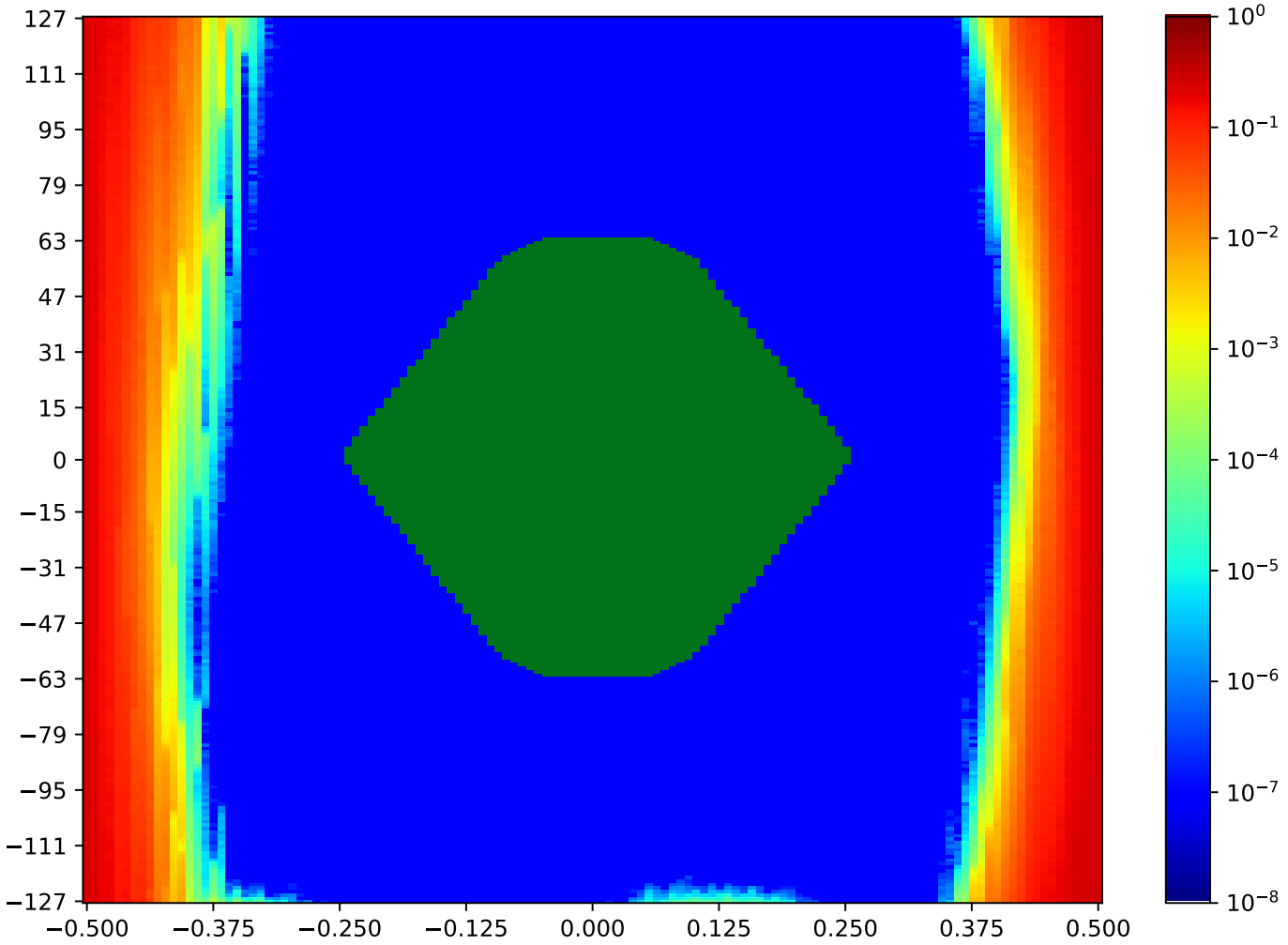


Figure 5.217: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.4 MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Table 5.201: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:05:48		2019-Nov-26 15:06:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24167	101	78.29%	246	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

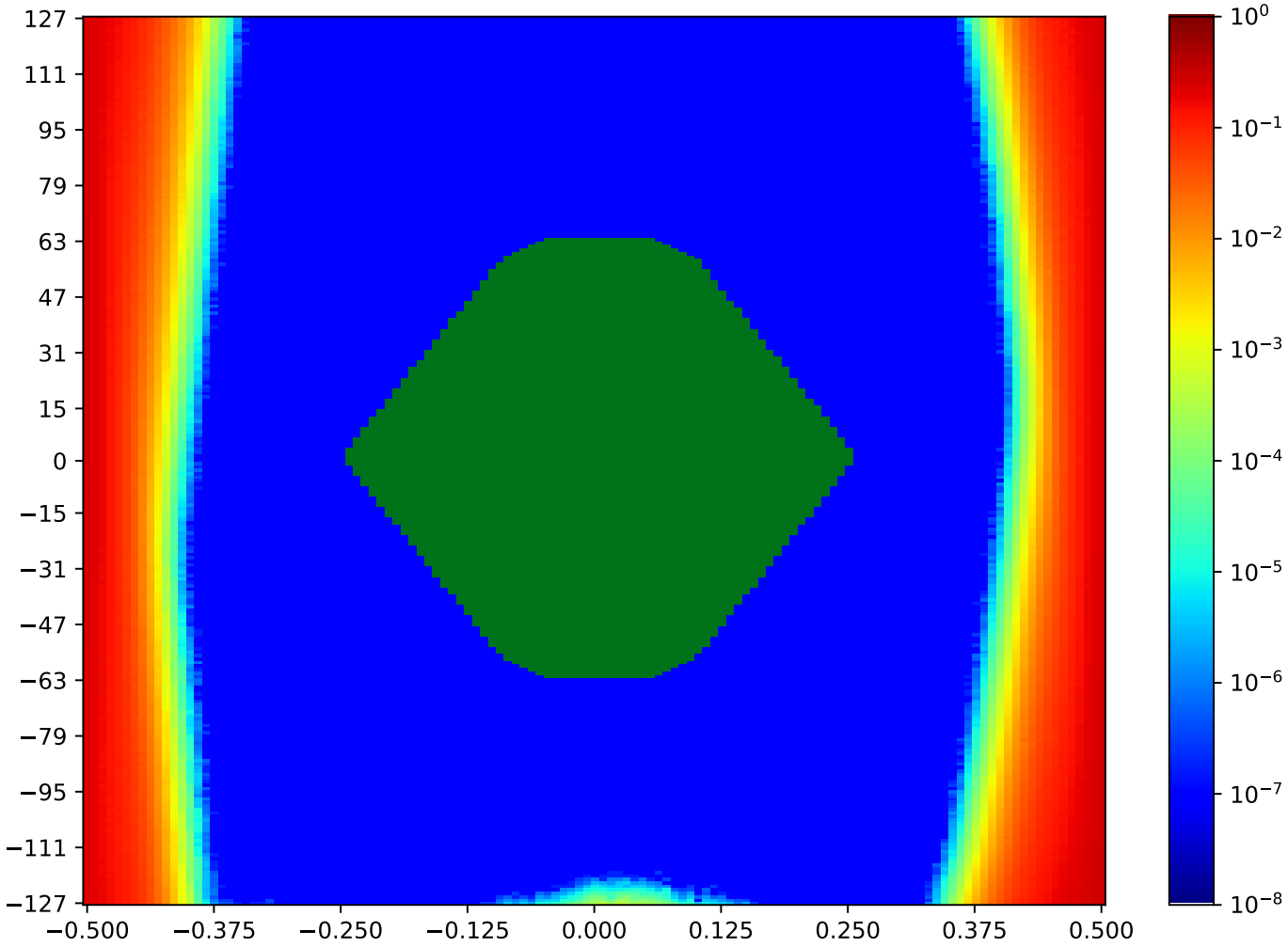


Figure 5.218: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.5 MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Table 5.202: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:15:37		2019-Nov-26 15:16:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23988	96	74.42%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

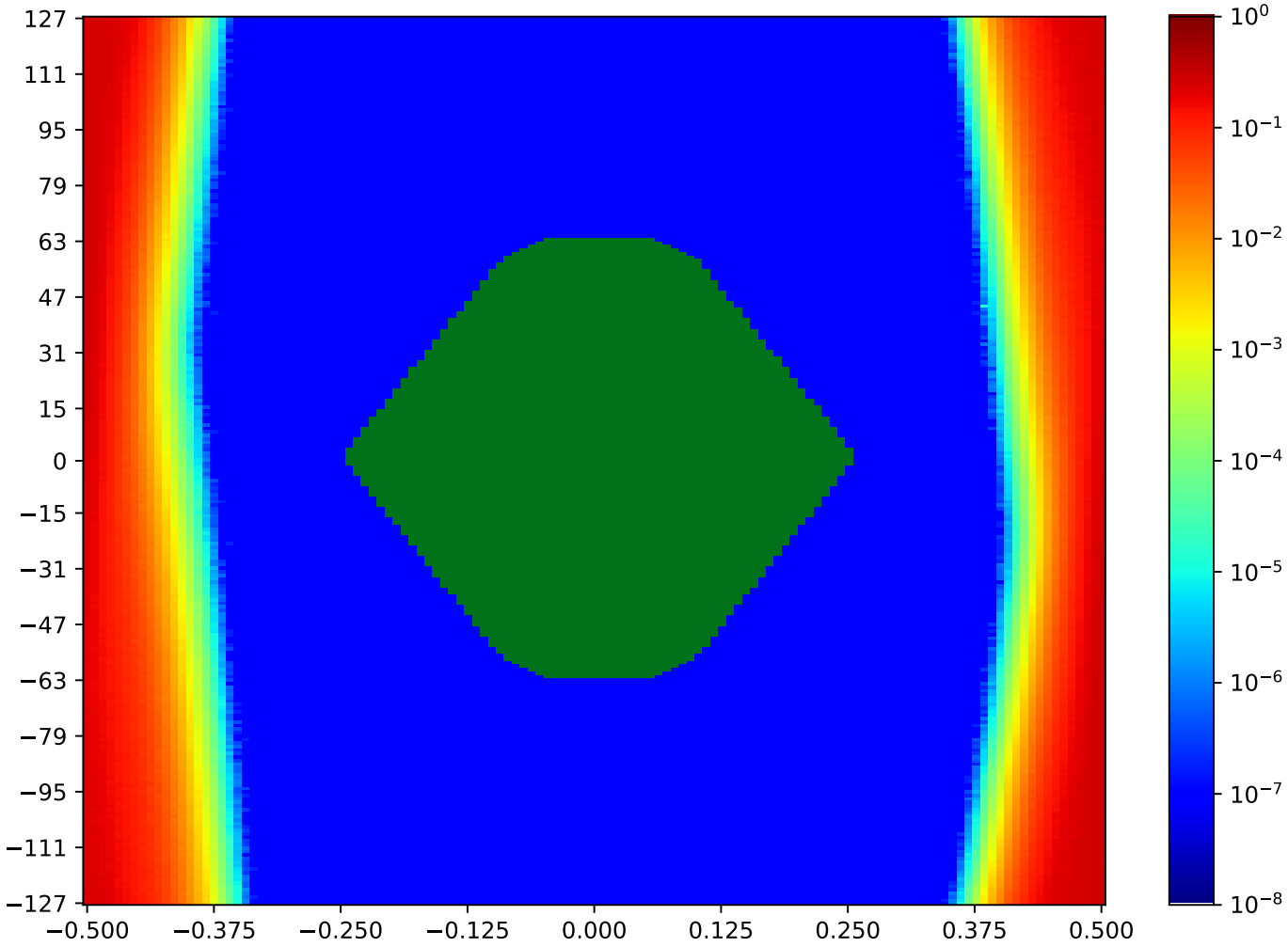


Figure 5.219: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.6 MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Table 5.203: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:04:39		2019-Nov-26 15:05:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24919	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

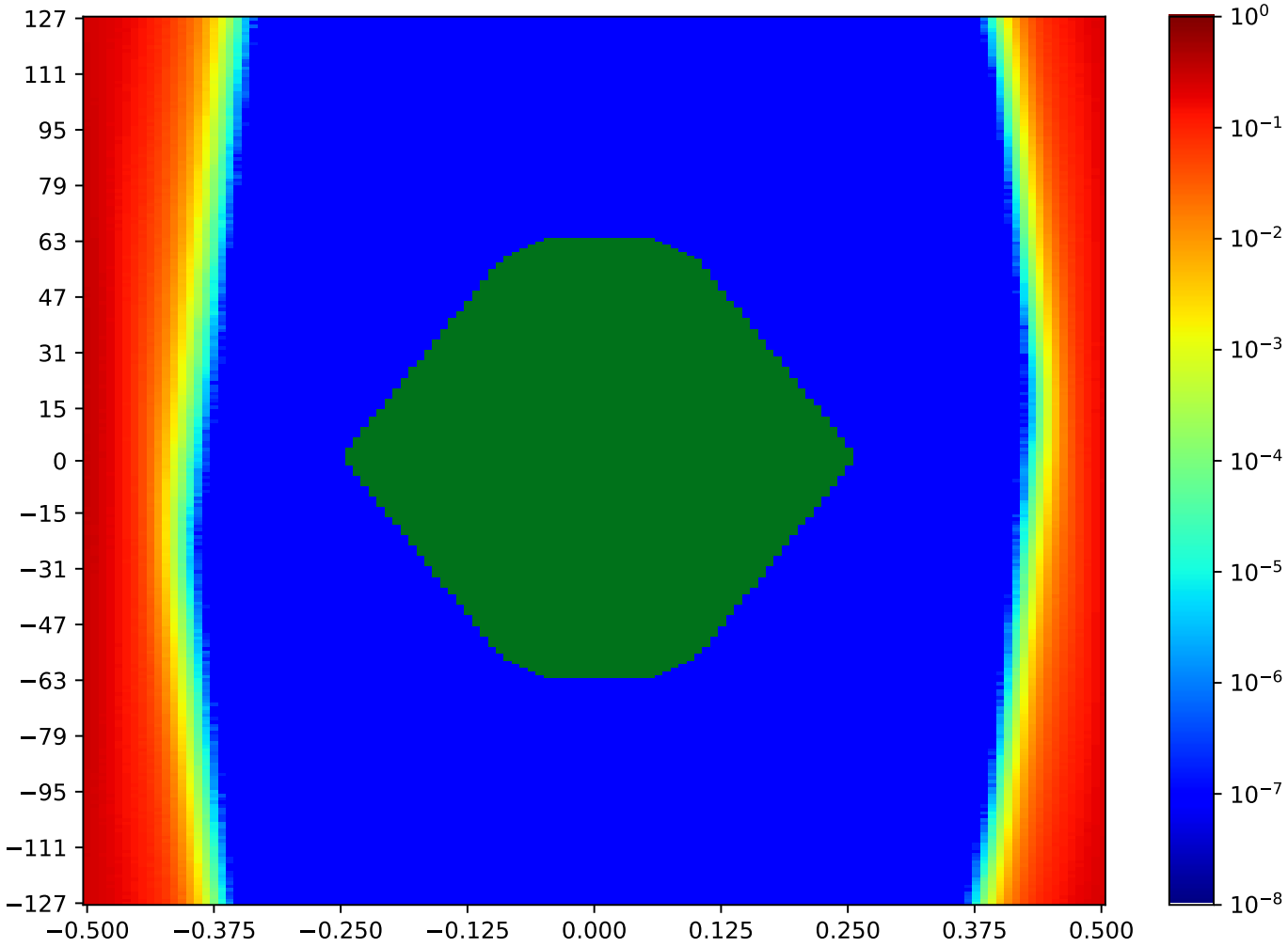


Figure 5.220: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.7 MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Table 5.204: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:17:53		2019-Nov-26 15:19:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23362	99	76.74%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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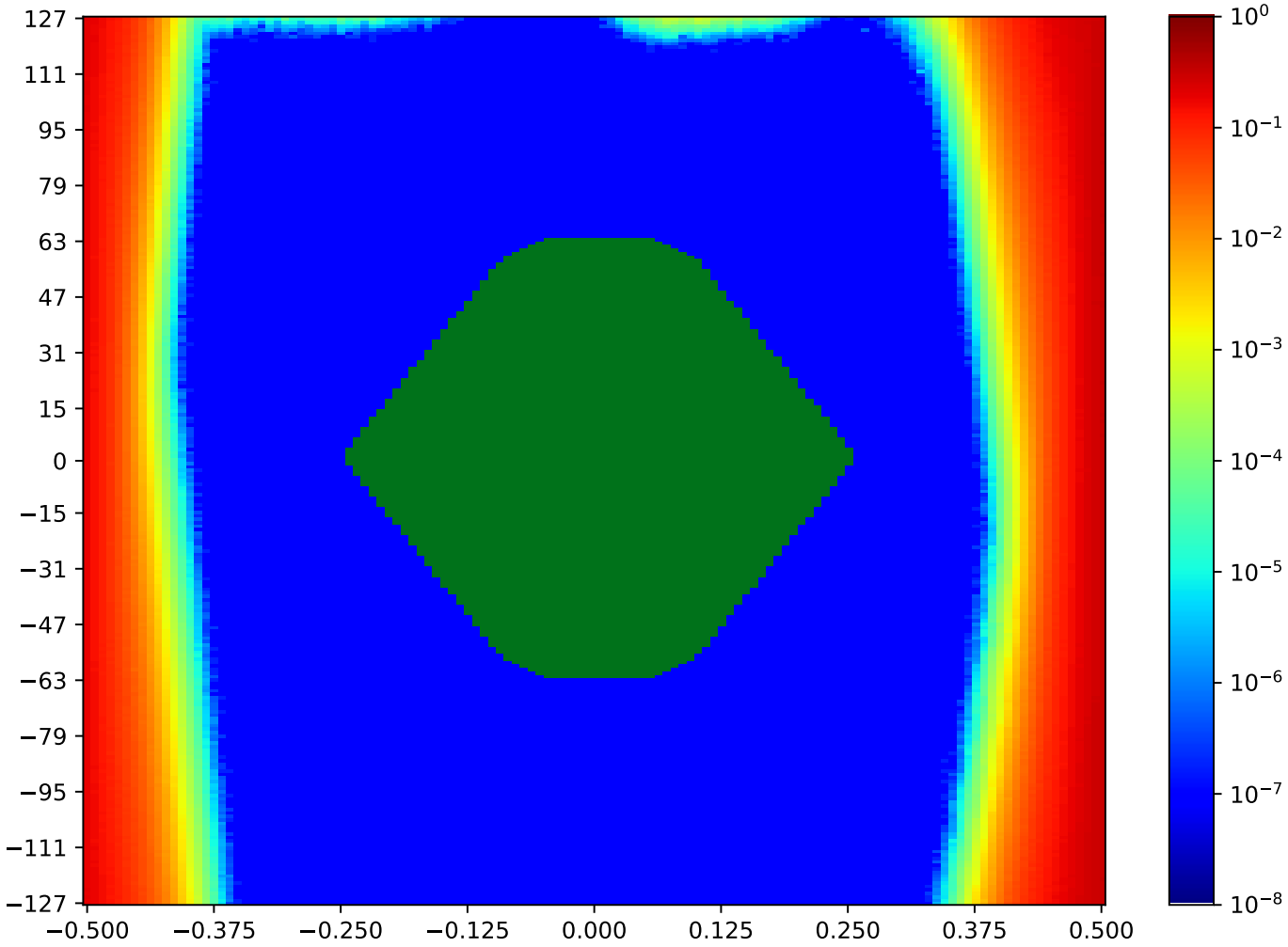


Figure 5.221: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.8 MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Table 5.205: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:06:57		2019-Nov-26 15:08:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23750	100	77.52%	241	94.51%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

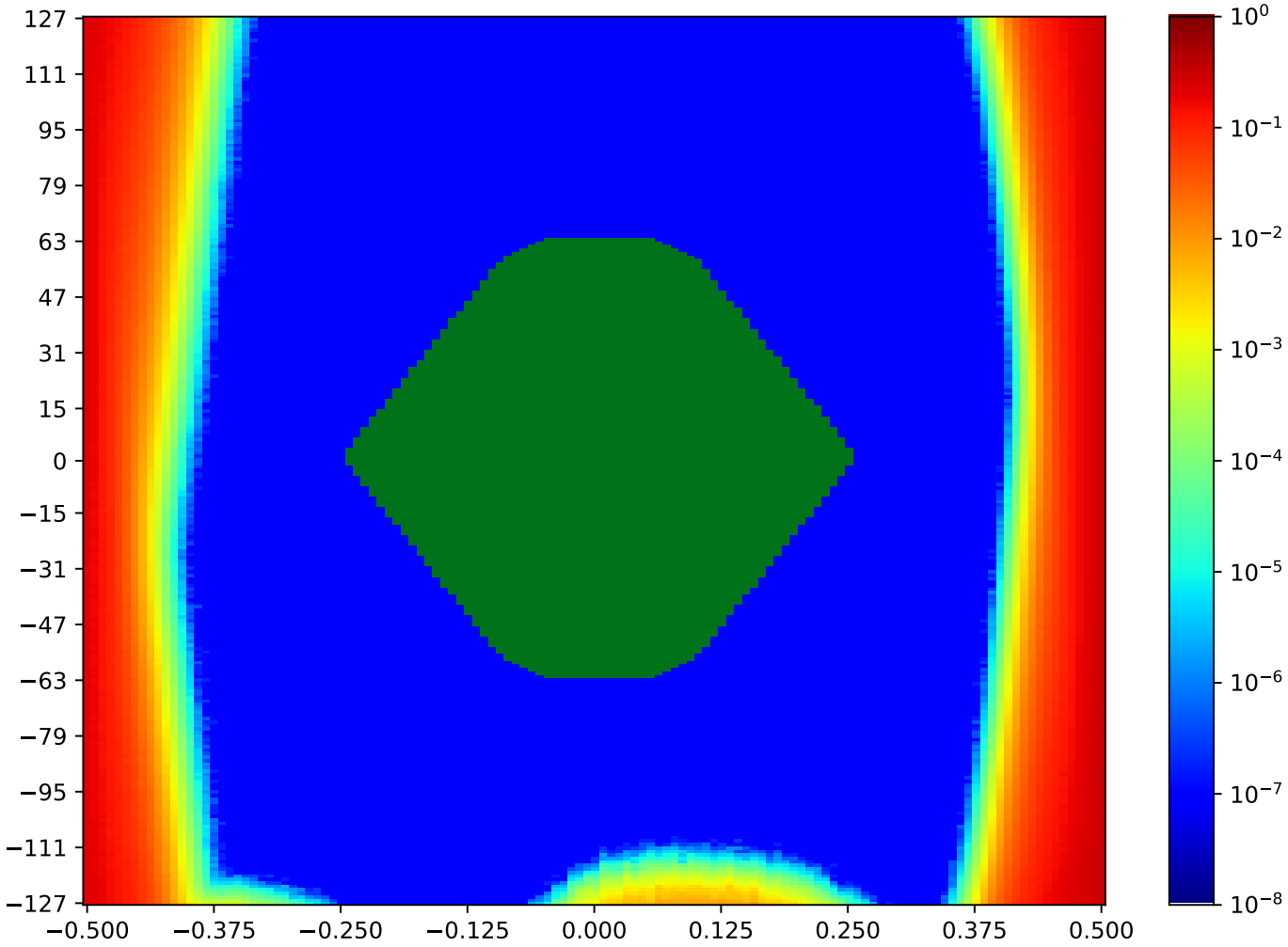


Figure 5.222: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.9 MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Table 5.206: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:16:46		2019-Nov-26 15:17:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24184	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

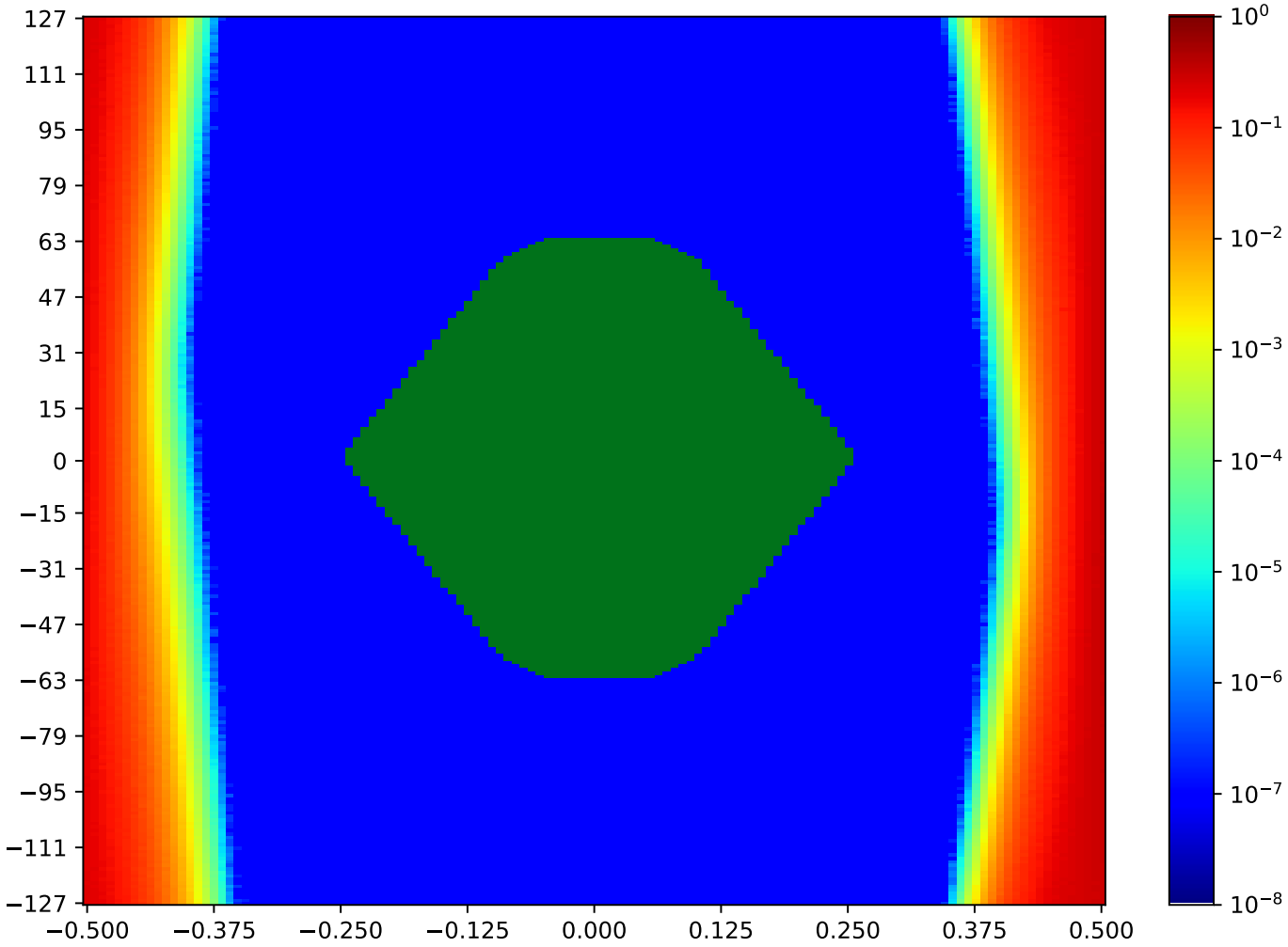


Figure 5.223: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.10 MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Table 5.207: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:09:45		2019-Nov-26 15:10:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24325	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

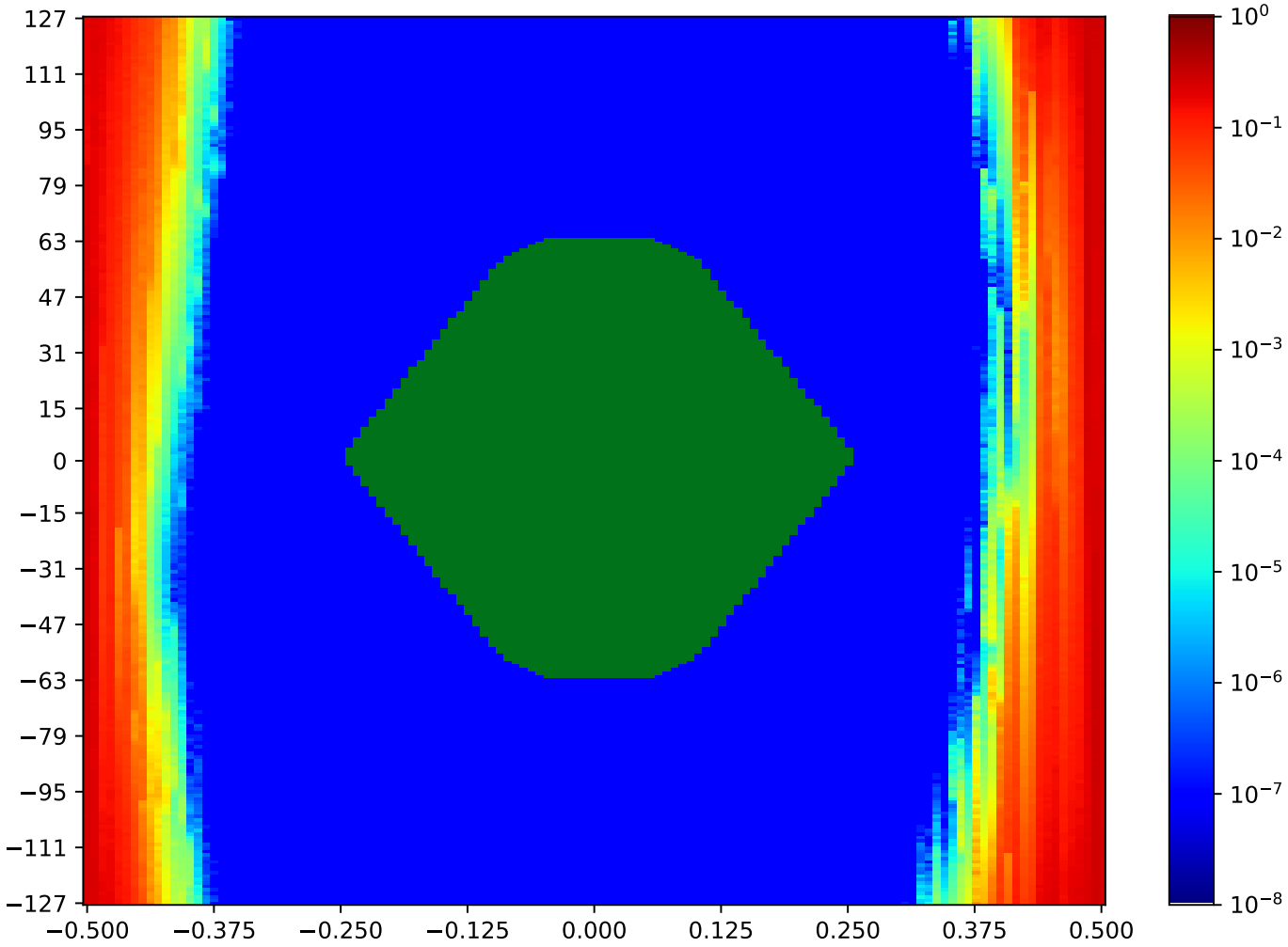


Figure 5.224: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.11 MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Table 5.208: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:14:29		2019-Nov-26 15:15:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24623	101	78.29%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

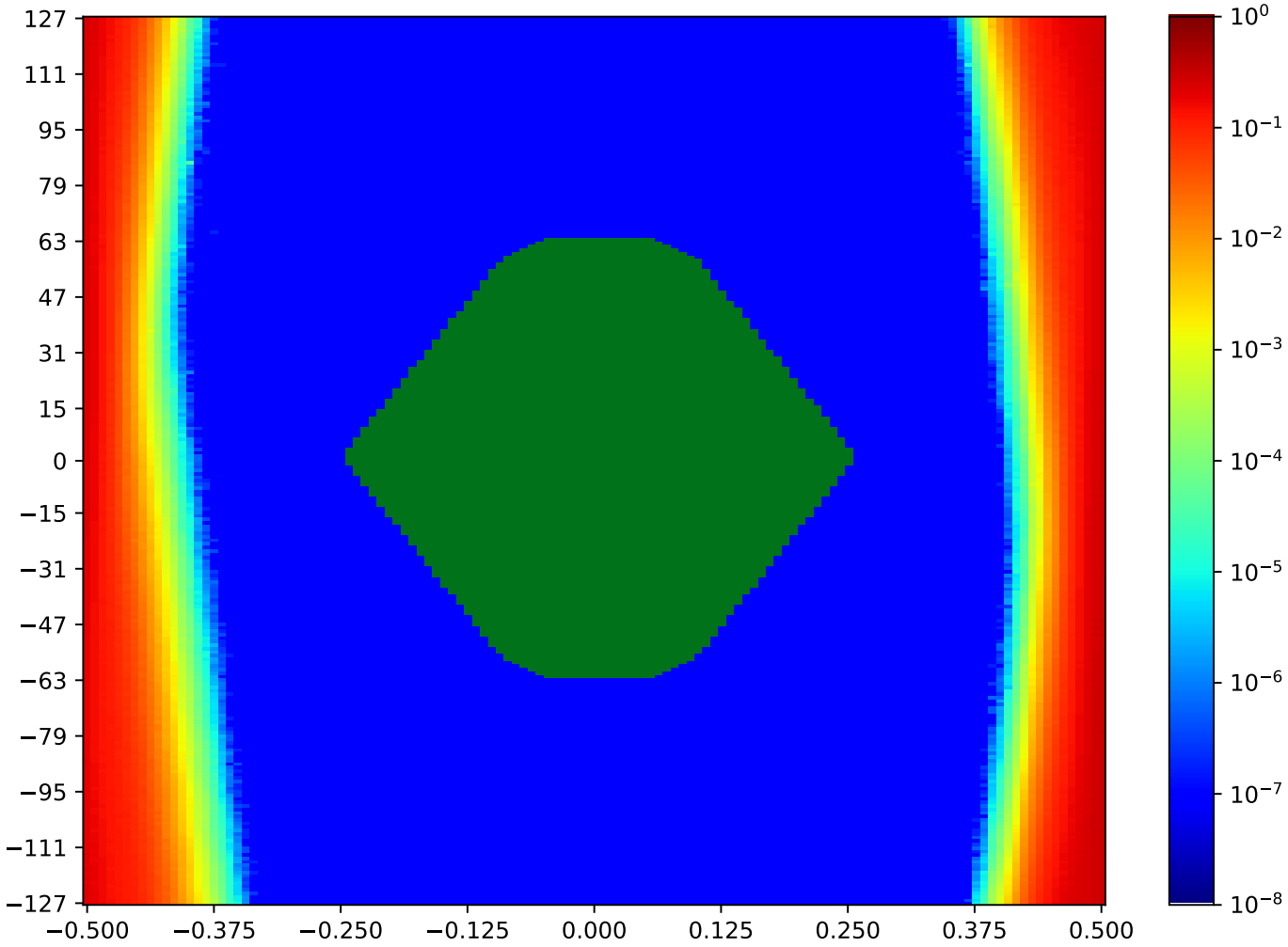


Figure 5.225: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.17.12 MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Table 5.209: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:13:21		2019-Nov-26 15:14:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24997	103	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

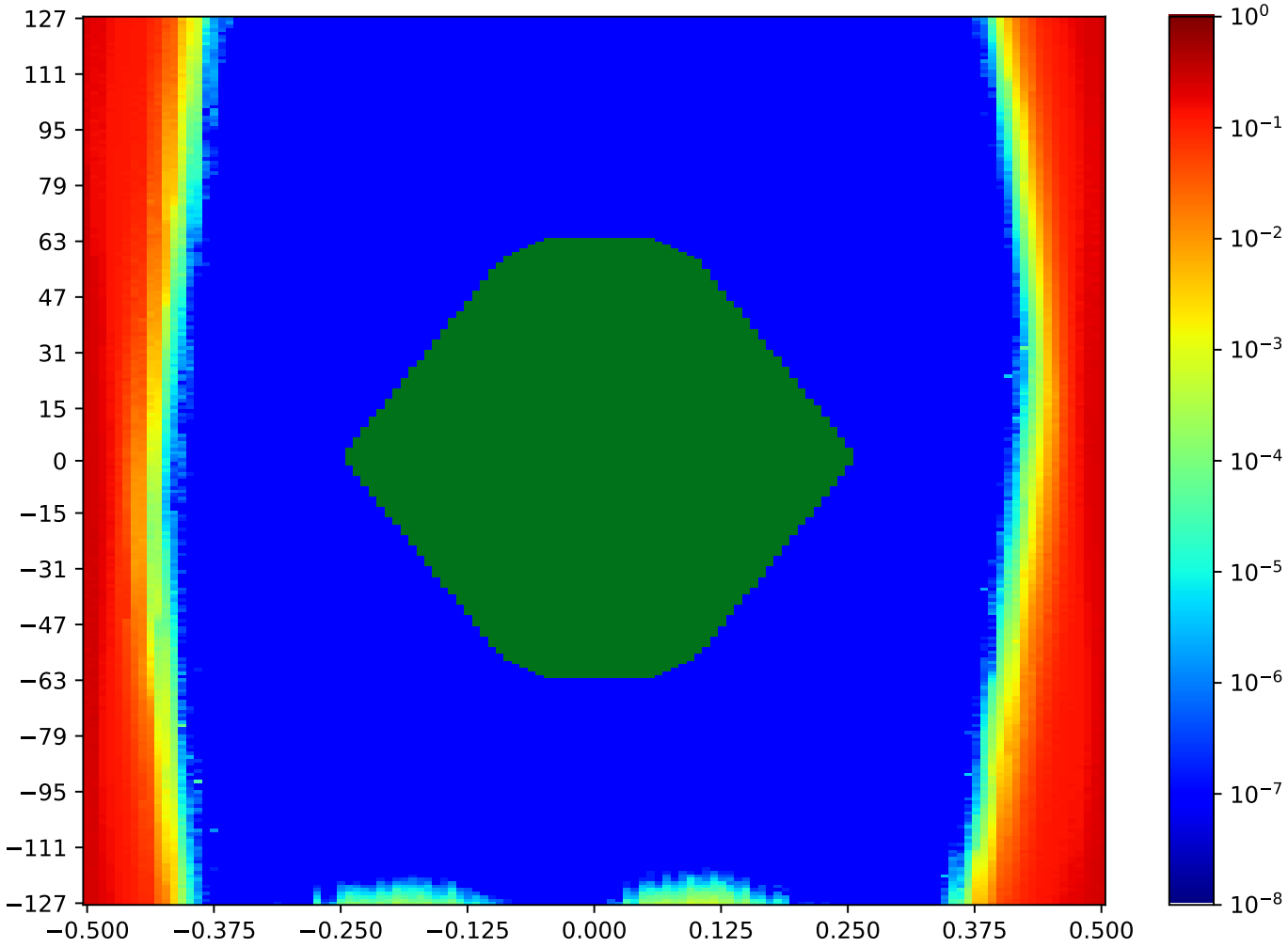


Figure 5.226: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18 MSP_C TX4 MSP_A RX2 Minipod Loopback

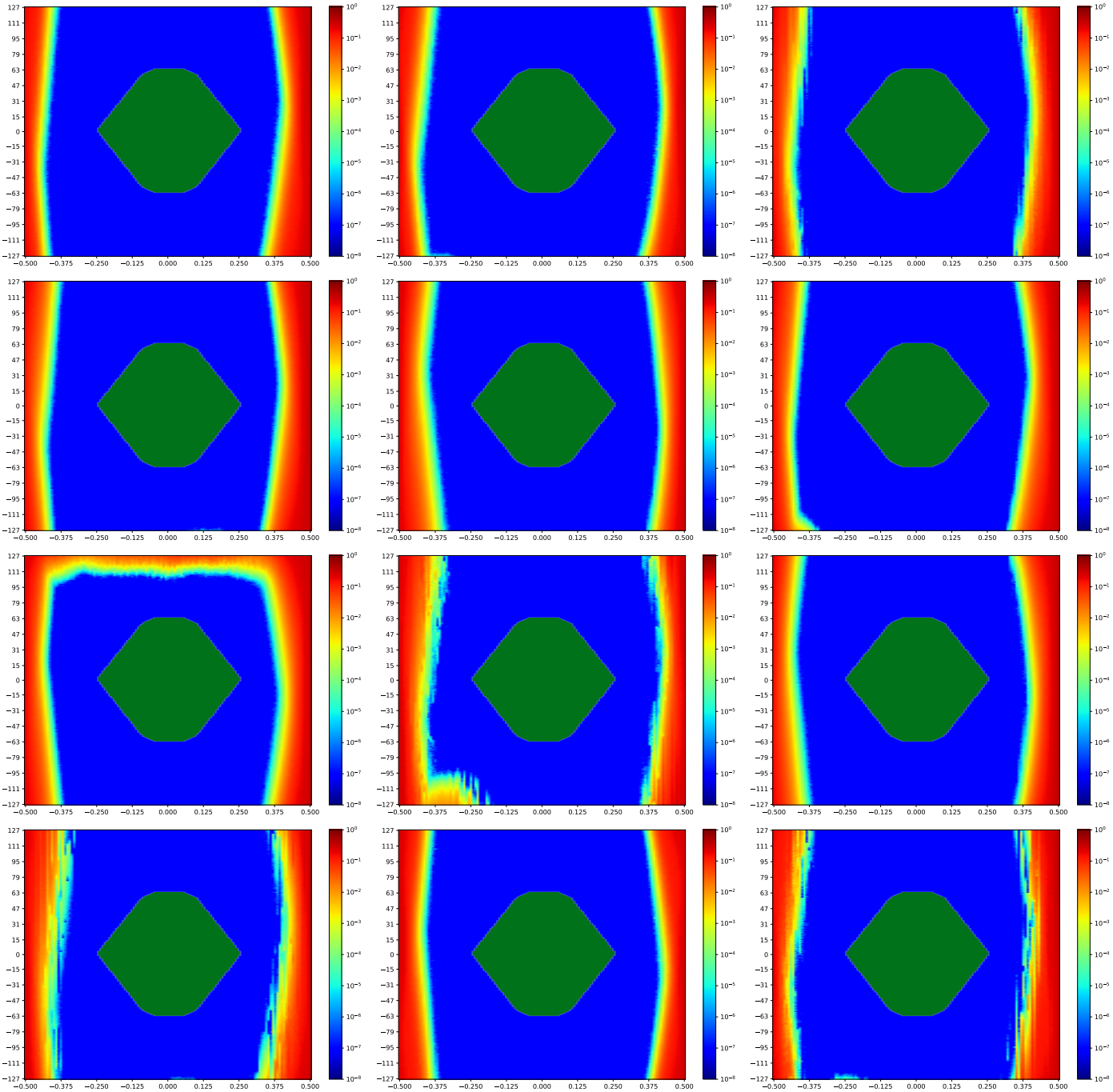


Figure 5.227: MSP_C TX4 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.240.

5.18.1 MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Table 5.210: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:22:25		2019-Nov-26 15:23:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24612	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

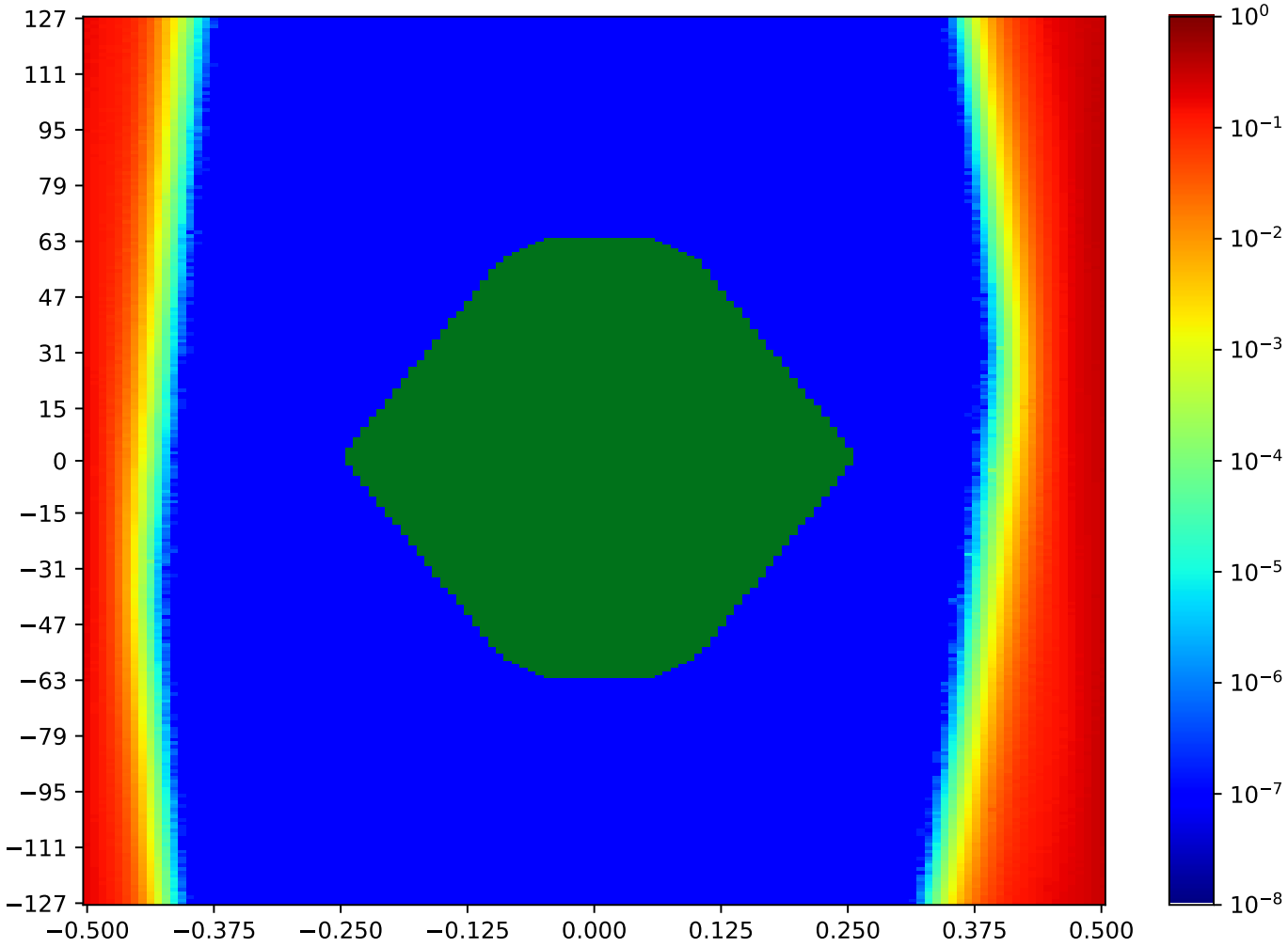


Figure 5.228: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.2 MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Table 5.211: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:20:08		2019-Nov-26 15:21:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24795	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

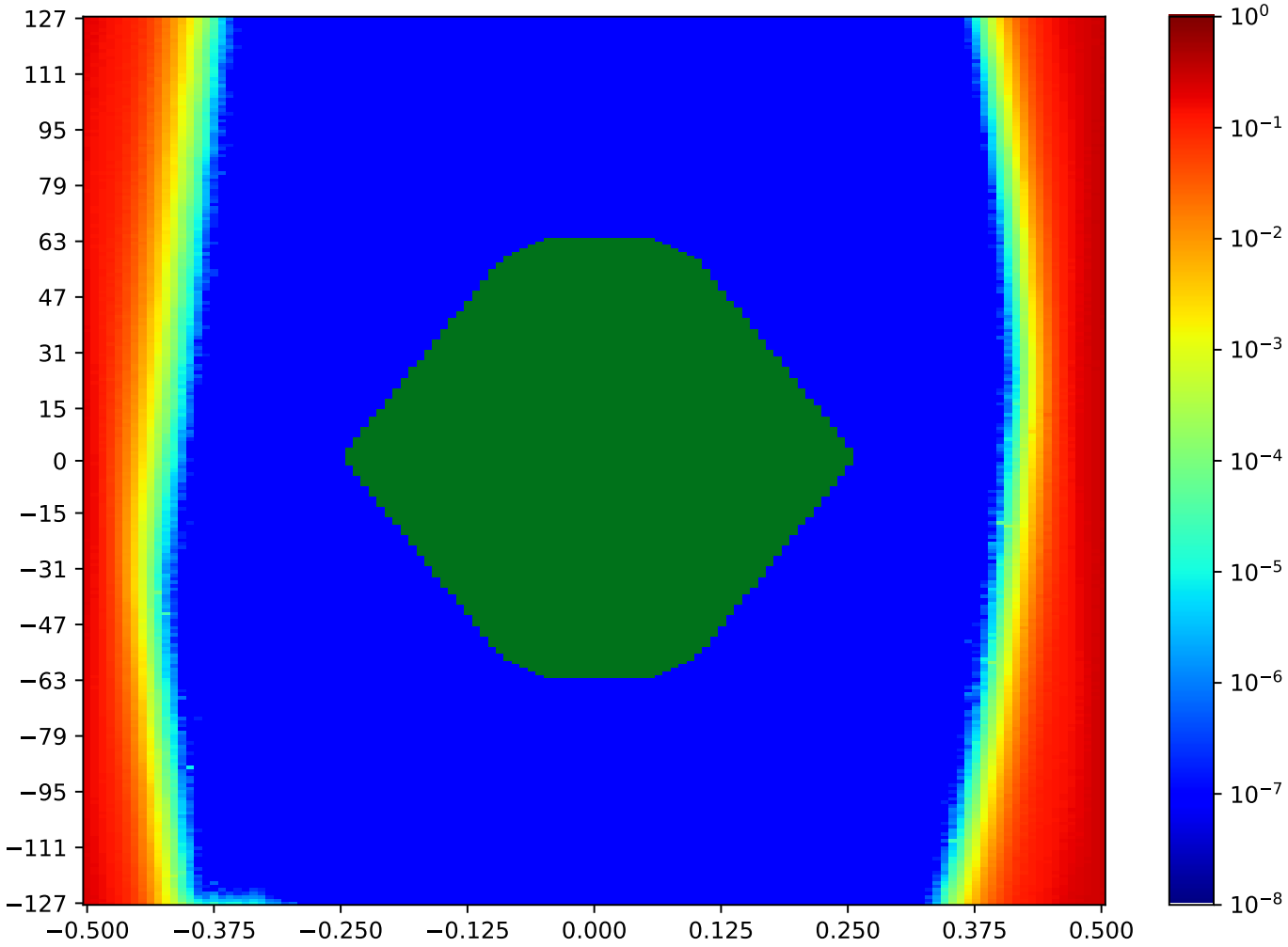


Figure 5.229: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.3 MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Table 5.212: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:25:48		2019-Nov-26 15:26:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24452	100	77.52%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

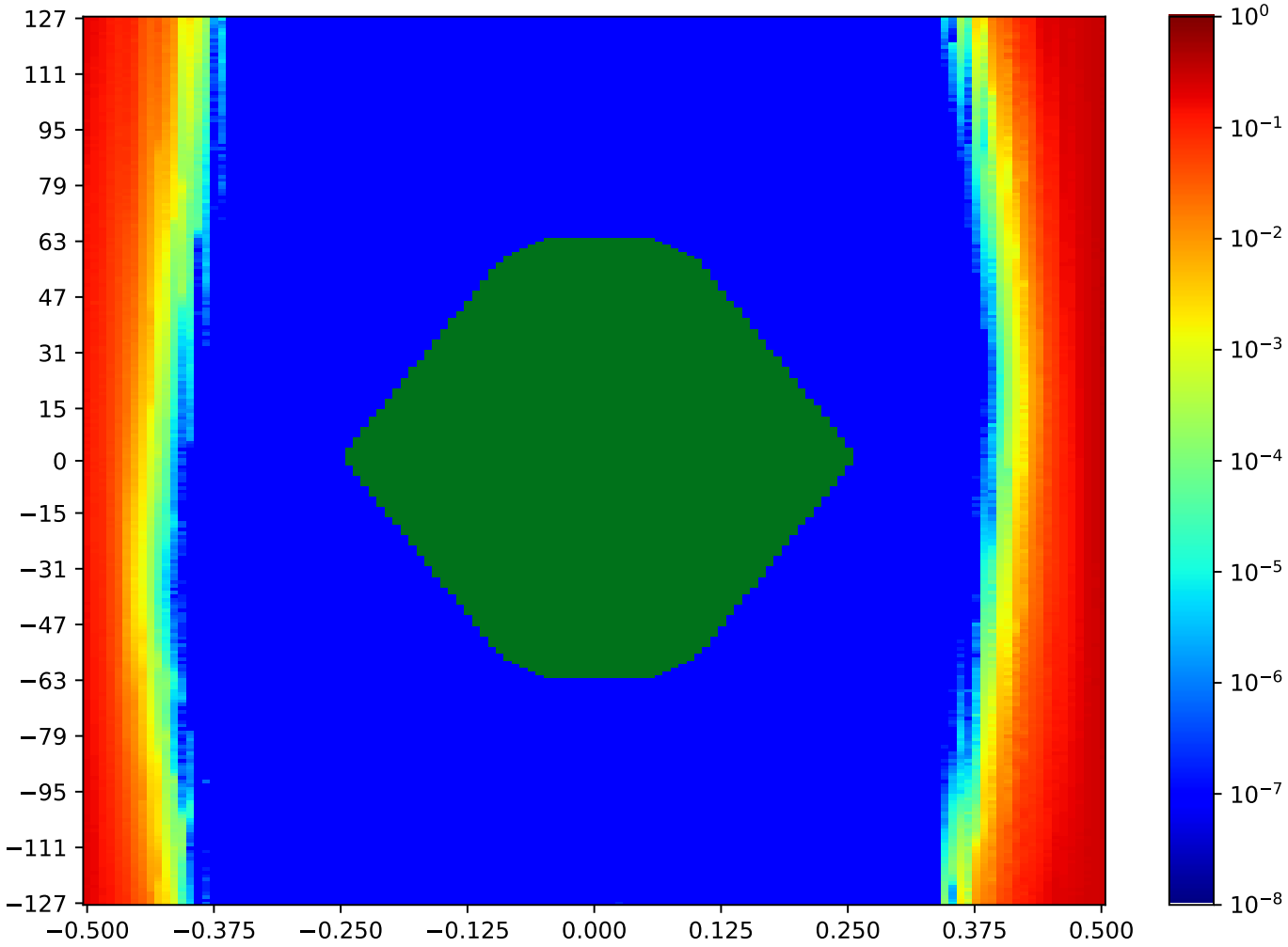


Figure 5.230: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.4 MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Table 5.213: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:19:00		2019-Nov-26 15:20:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24169	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

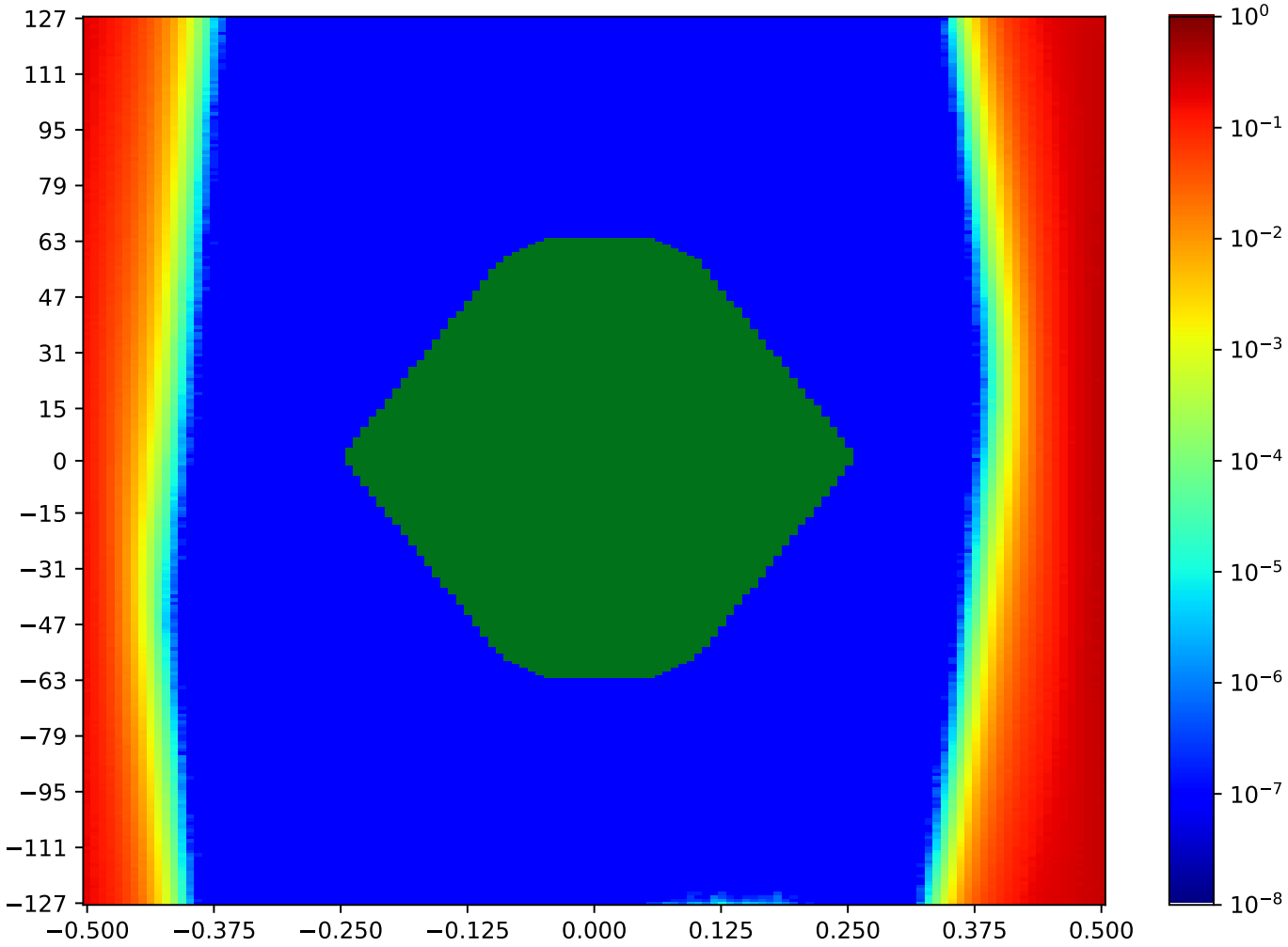


Figure 5.231: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.5 MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Table 5.214: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:29:11		2019-Nov-26 15:30:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24000	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

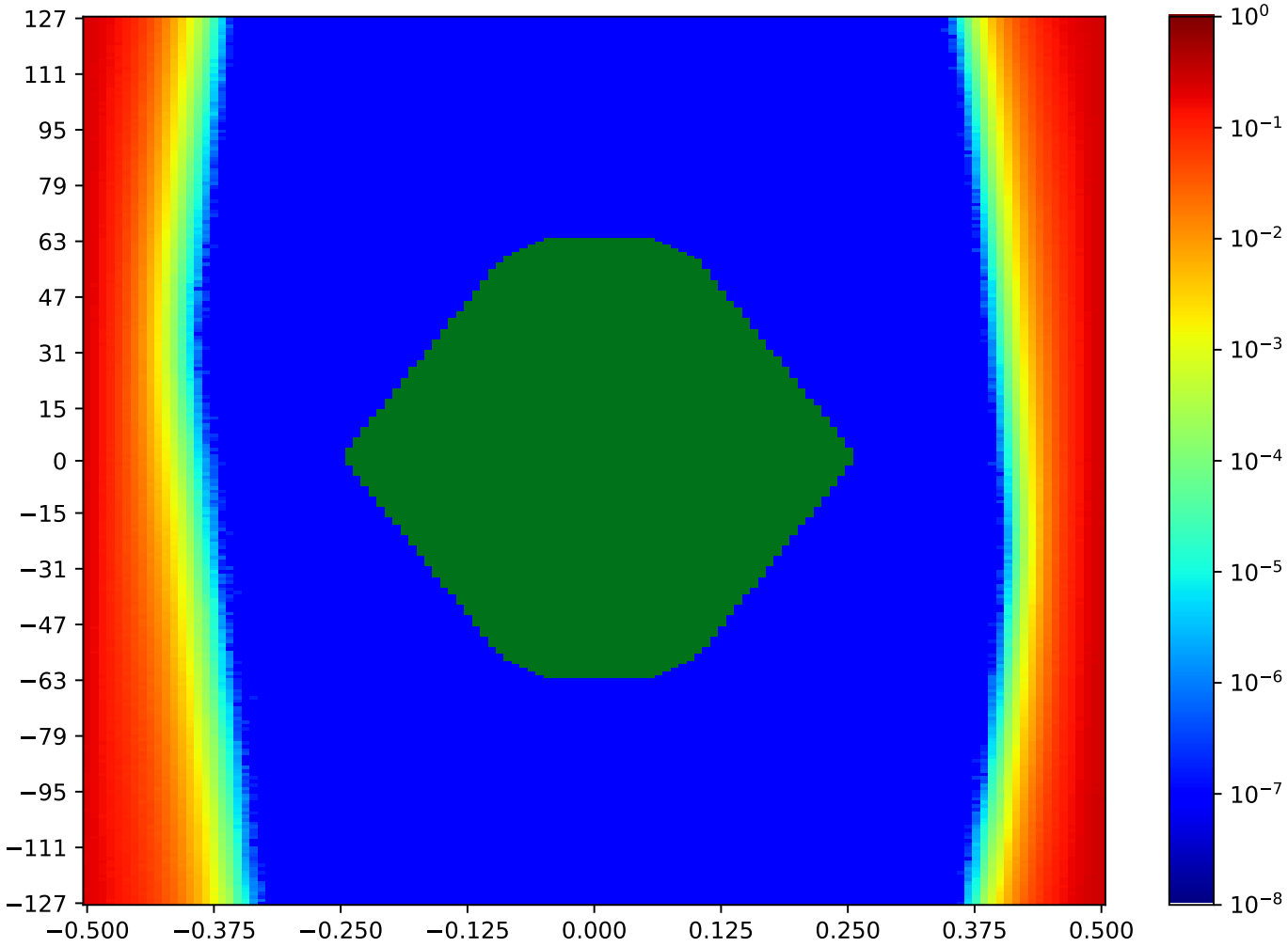


Figure 5.232: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.6 MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Table 5.215: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:21:17		2019-Nov-26 15:22:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24356	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

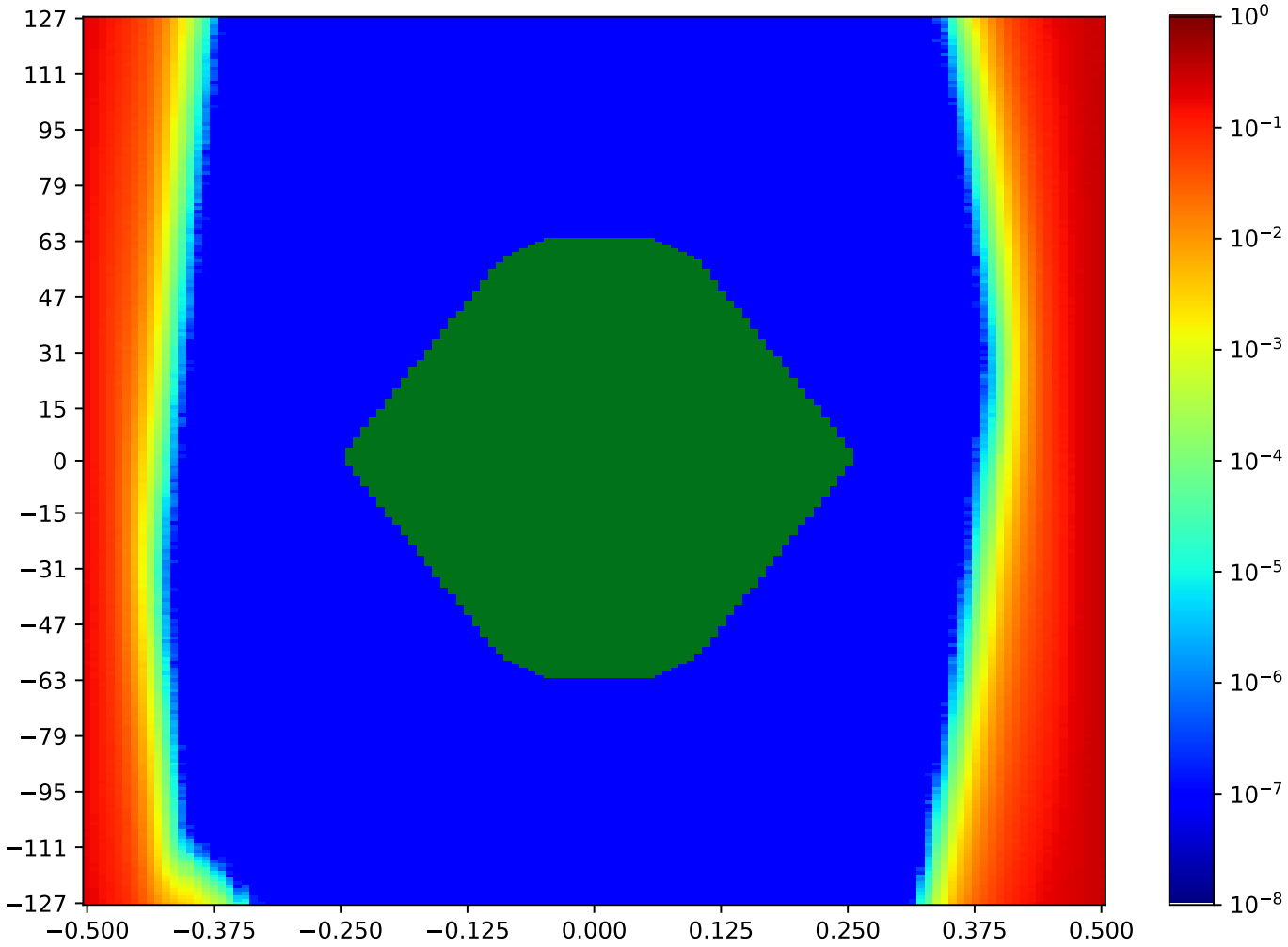


Figure 5.233: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.7 MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Table 5.216: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:31:26		2019-Nov-26 15:32:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21662	99	76.74%	229	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

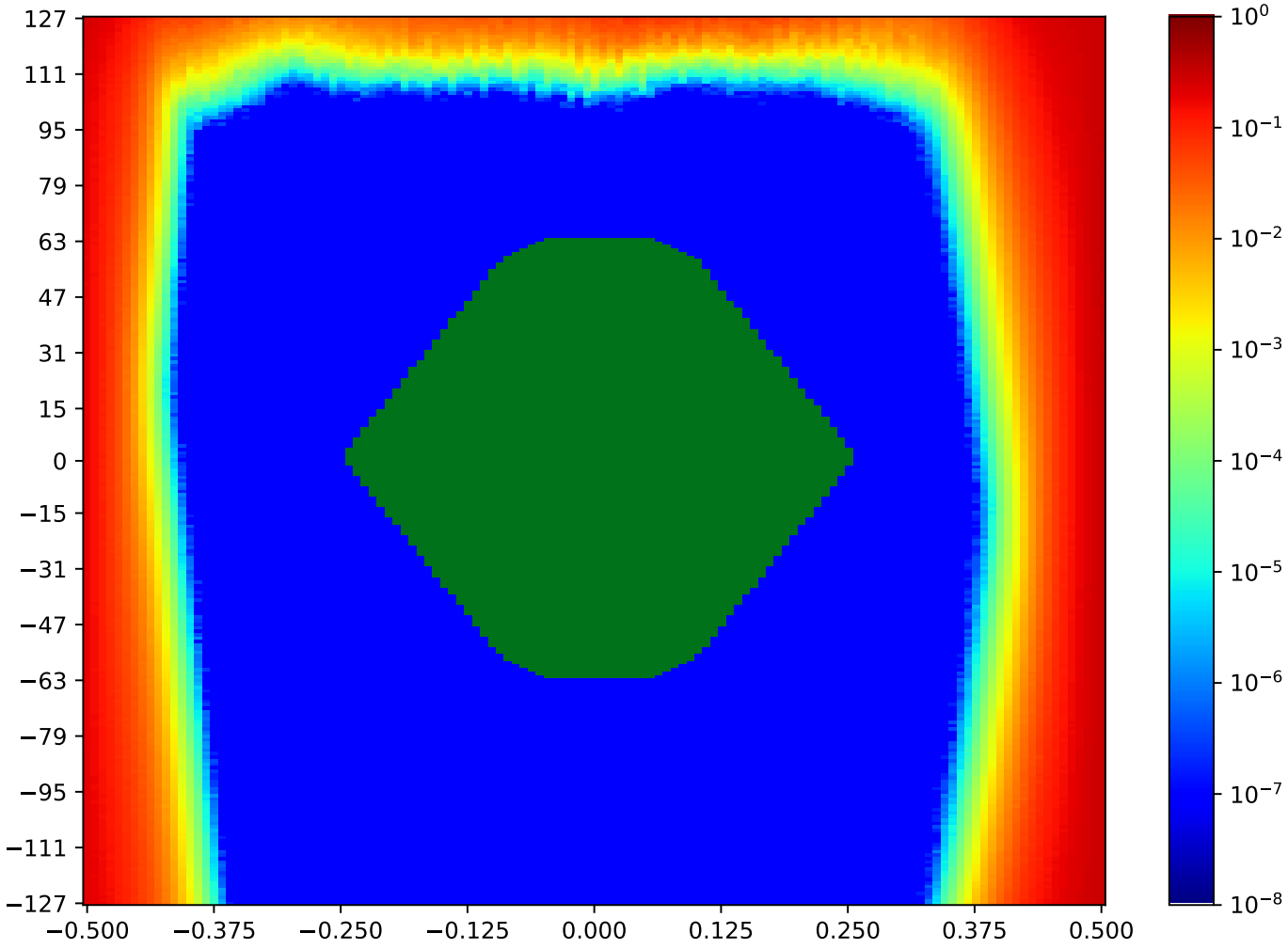


Figure 5.234: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.8 MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Table 5.217: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:23:33		2019-Nov-26 15:24:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23265	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

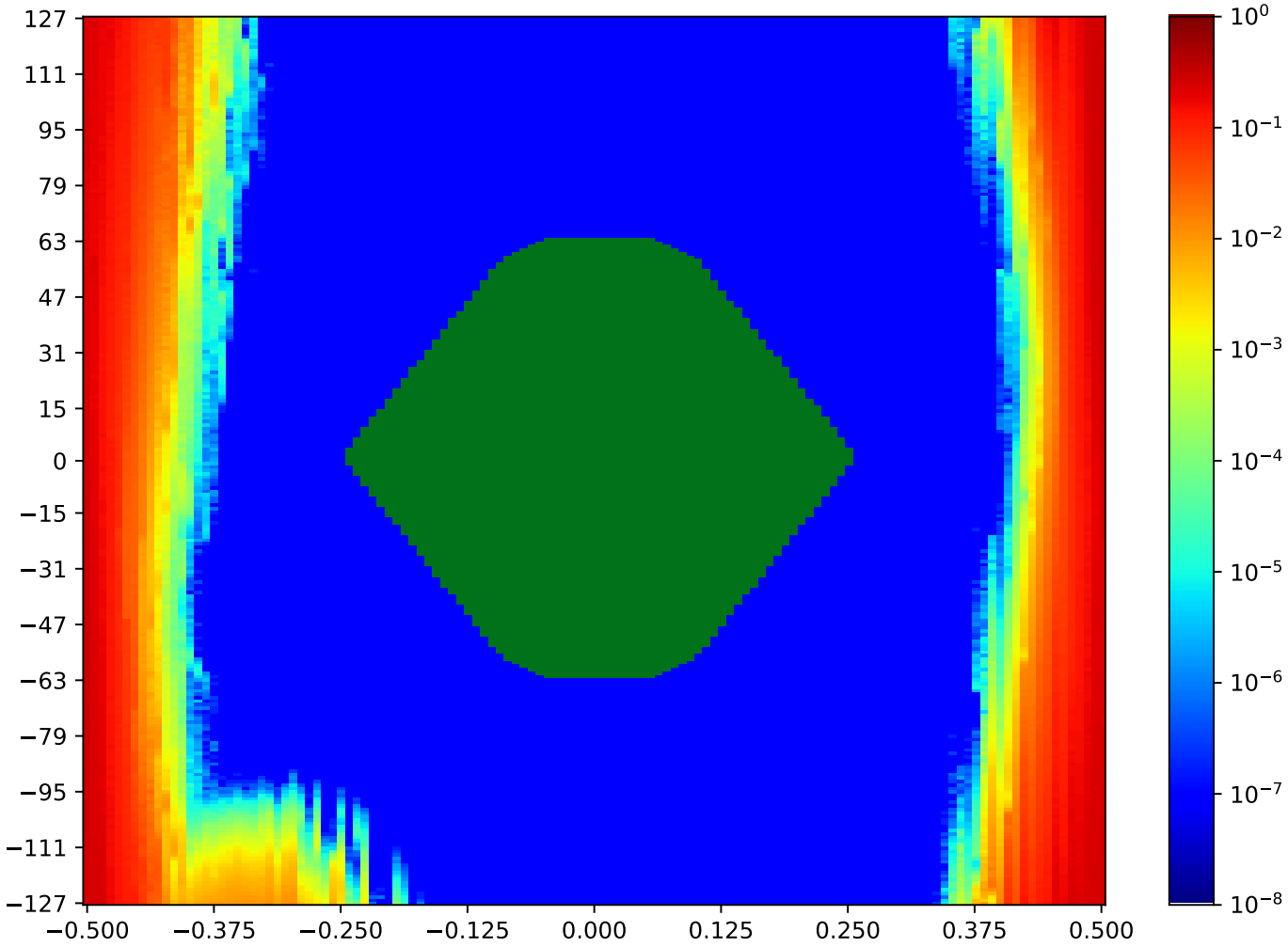


Figure 5.235: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.9 MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Table 5.218: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:30:19		2019-Nov-26 15:31:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24162	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

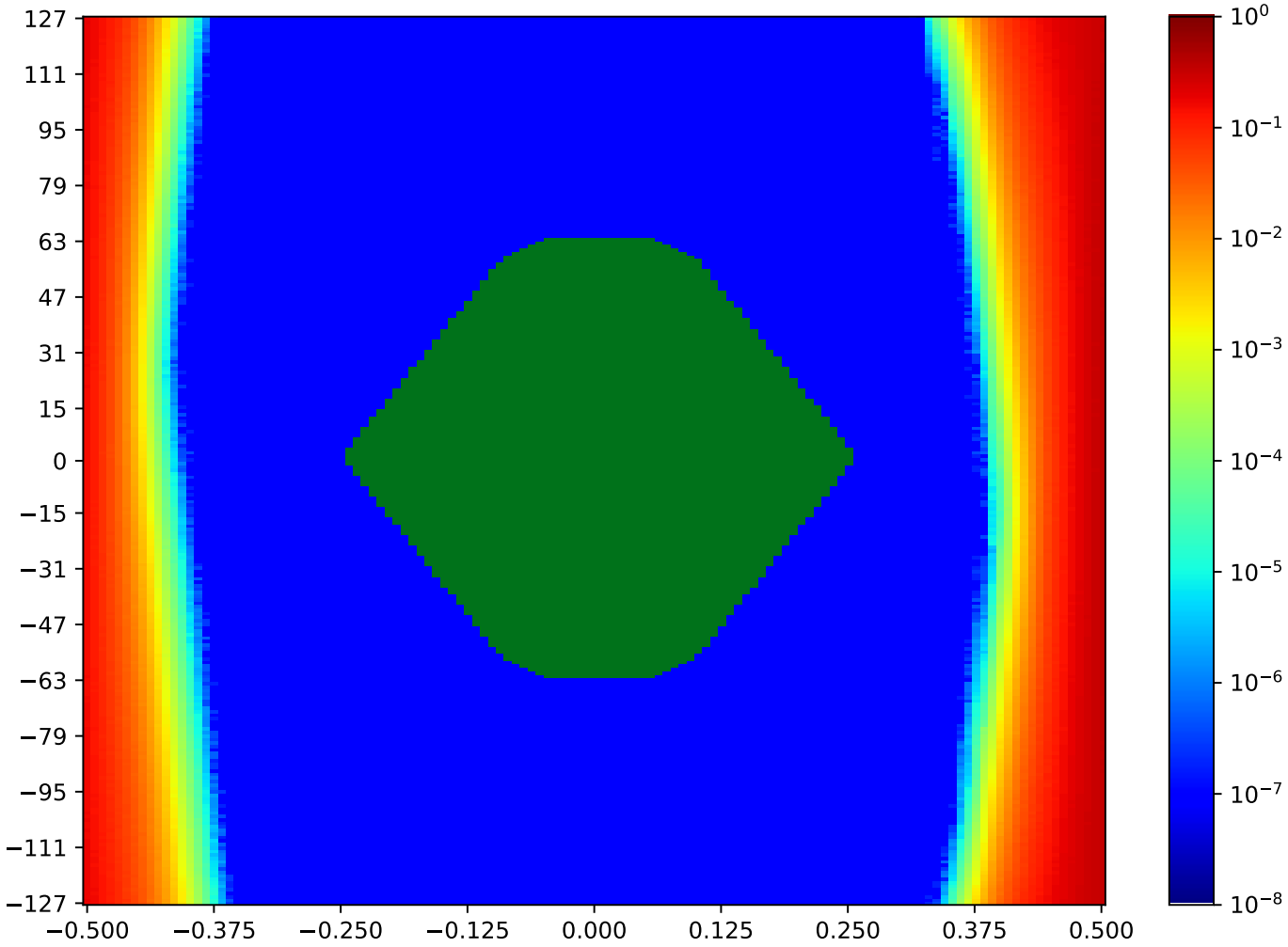


Figure 5.236: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.10 MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Table 5.219: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:24:40		2019-Nov-26 15:25:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23136	95	72.87%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

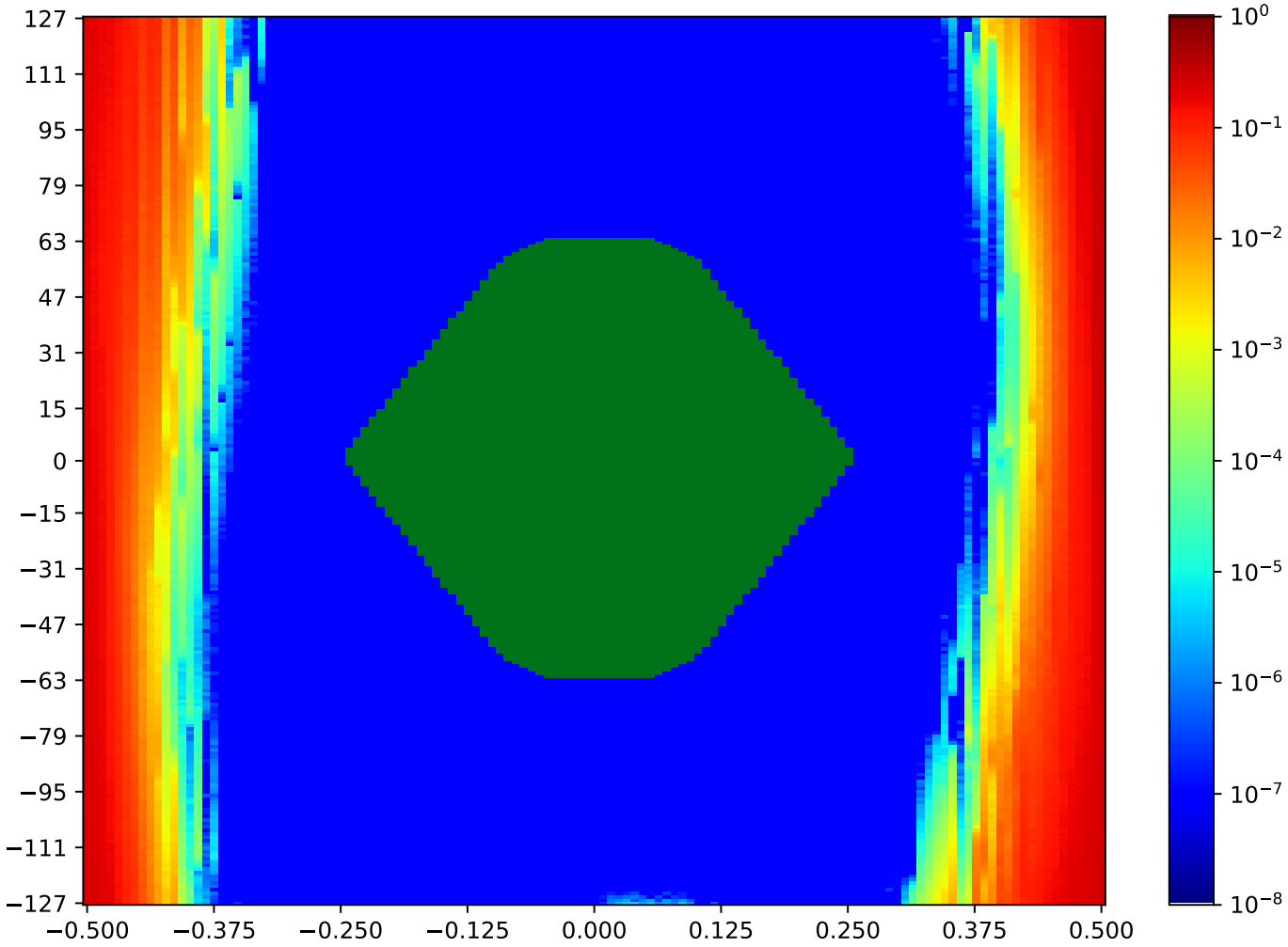


Figure 5.237: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.11 MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Table 5.220: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:28:04		2019-Nov-26 15:29:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24661	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

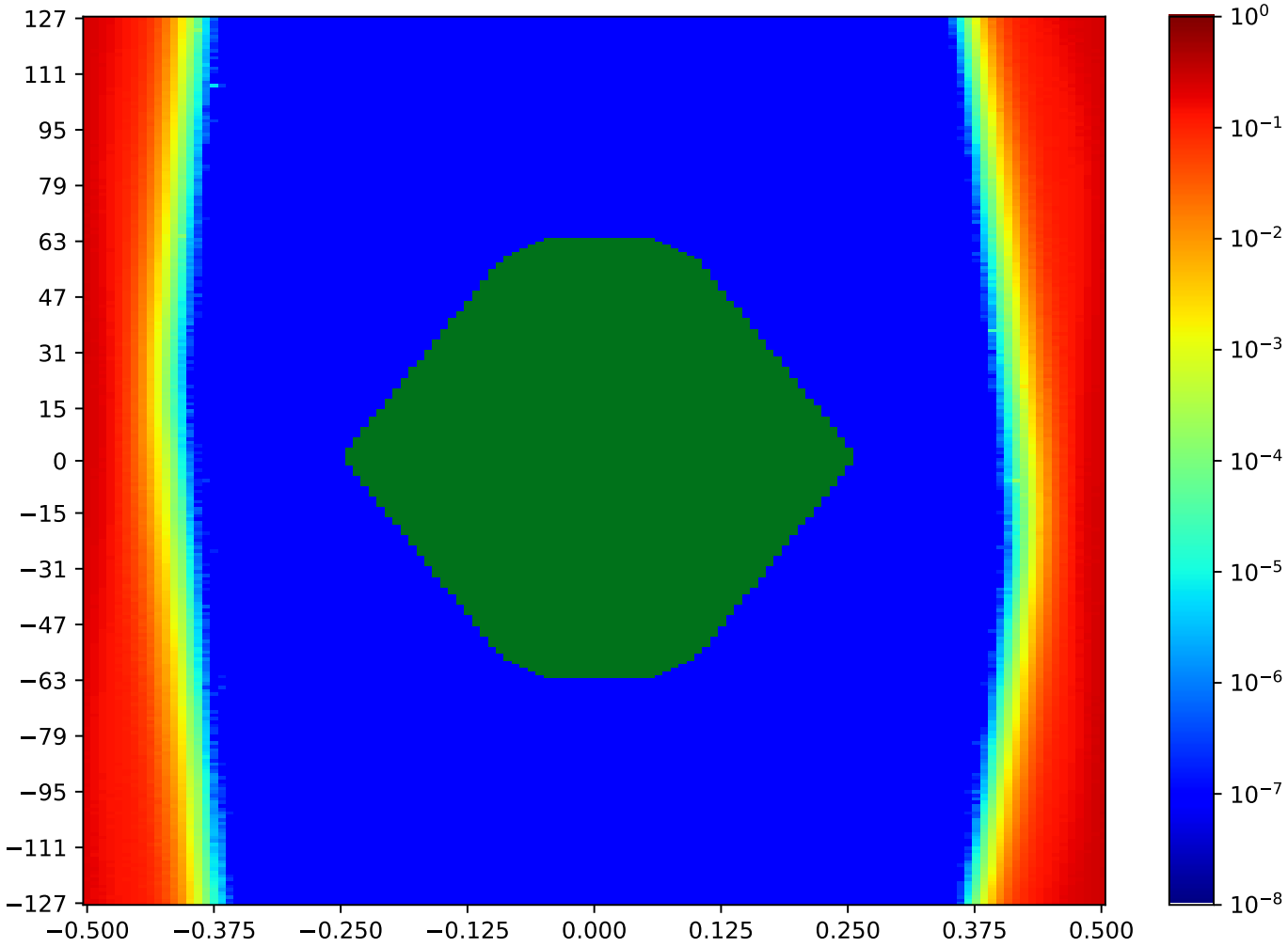


Figure 5.238: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.18.12 MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Table 5.221: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 15:26:56		2019-Nov-26 15:28:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24250	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

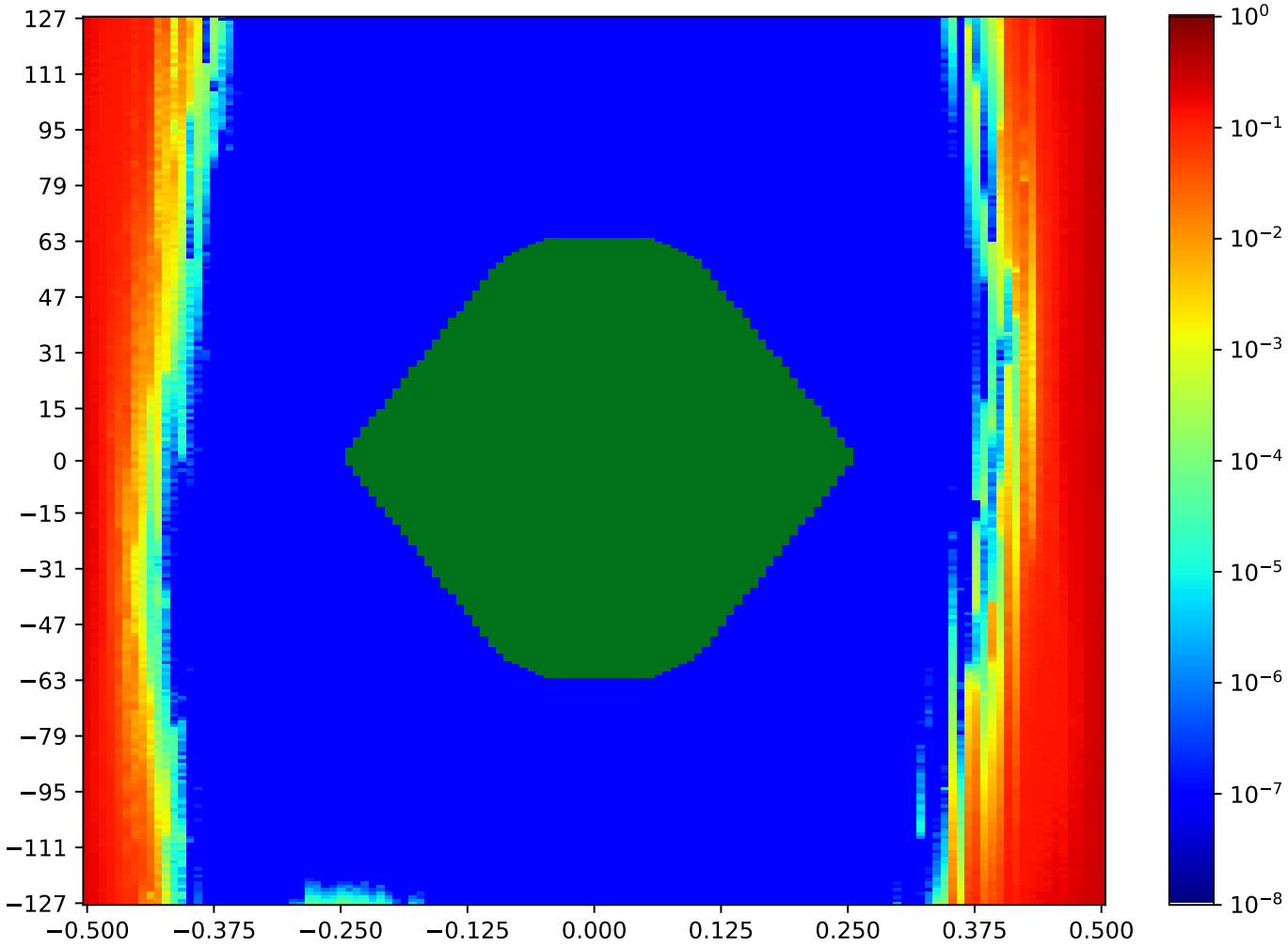


Figure 5.239: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19 MSP_A TX1 MSP_C RX12 Minipod Loopback

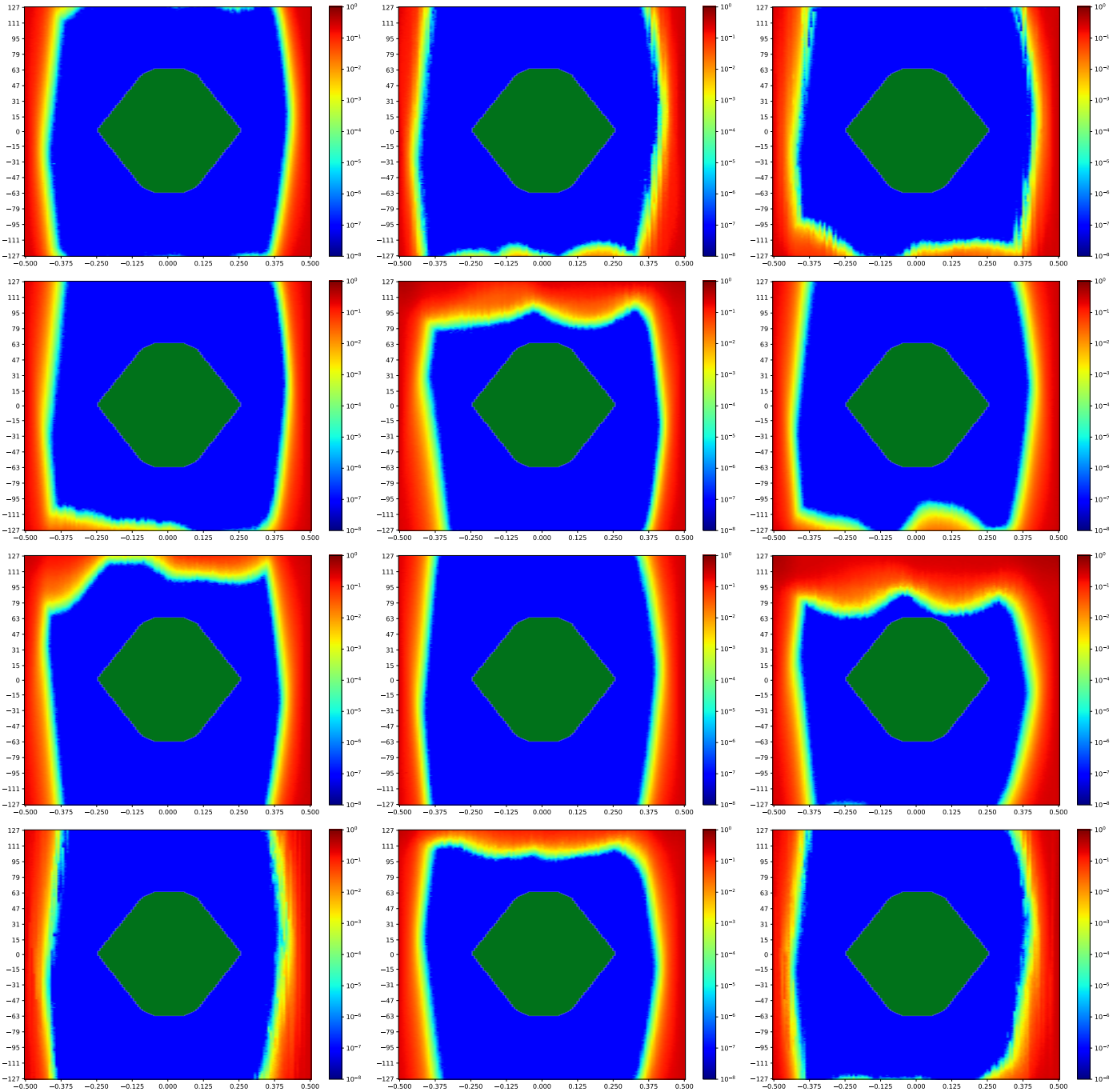


Figure 5.240: MSP_A TX1 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.253.

5.19.1 MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Table 5.222: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:07:21		2019-Nov-26 16:08:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24517	103	79.84%	250	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

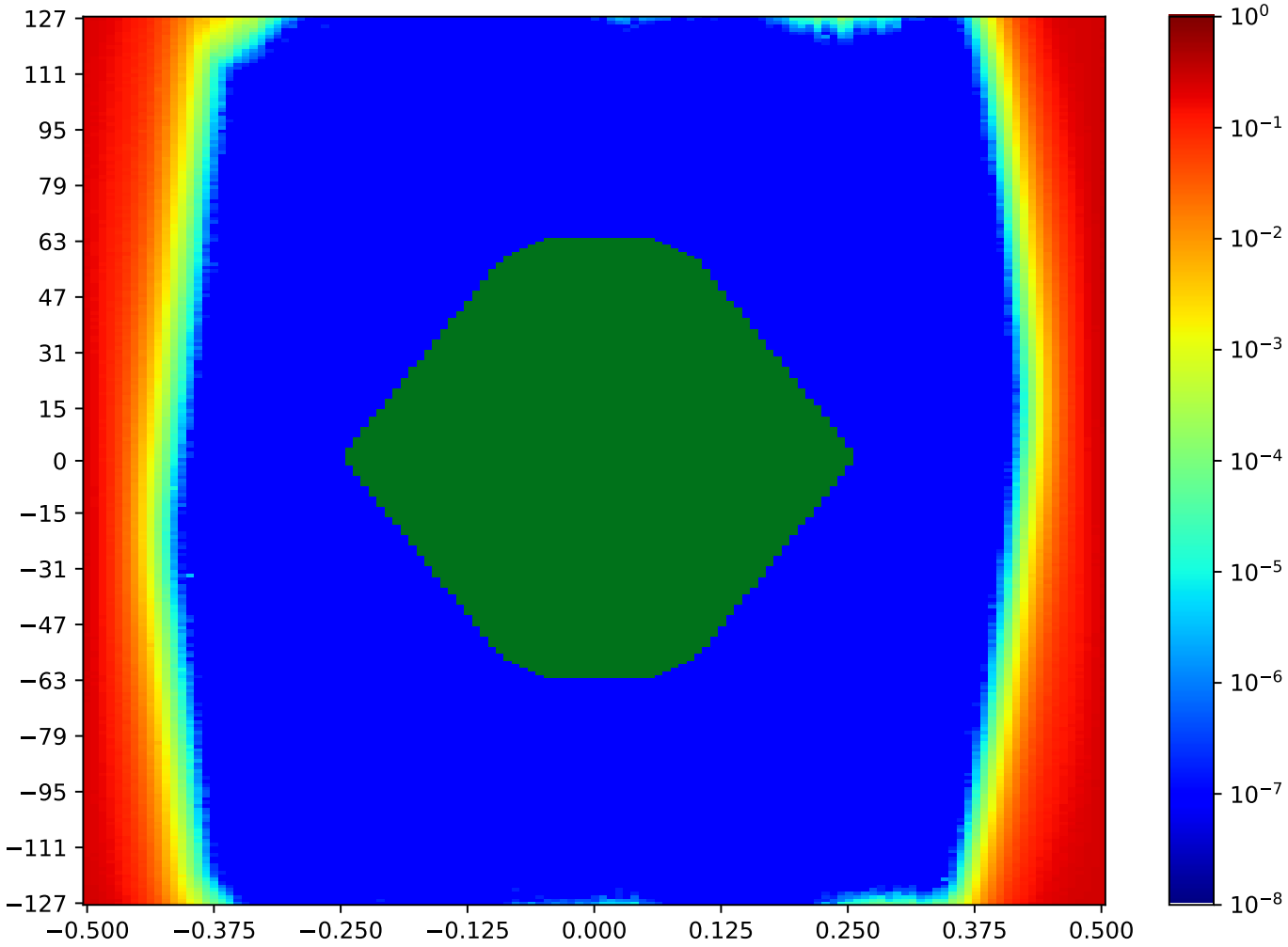


Figure 5.241: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.2 MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Table 5.223: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:09:56		2019-Nov-26 16:11:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23957	104	79.84%	246	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

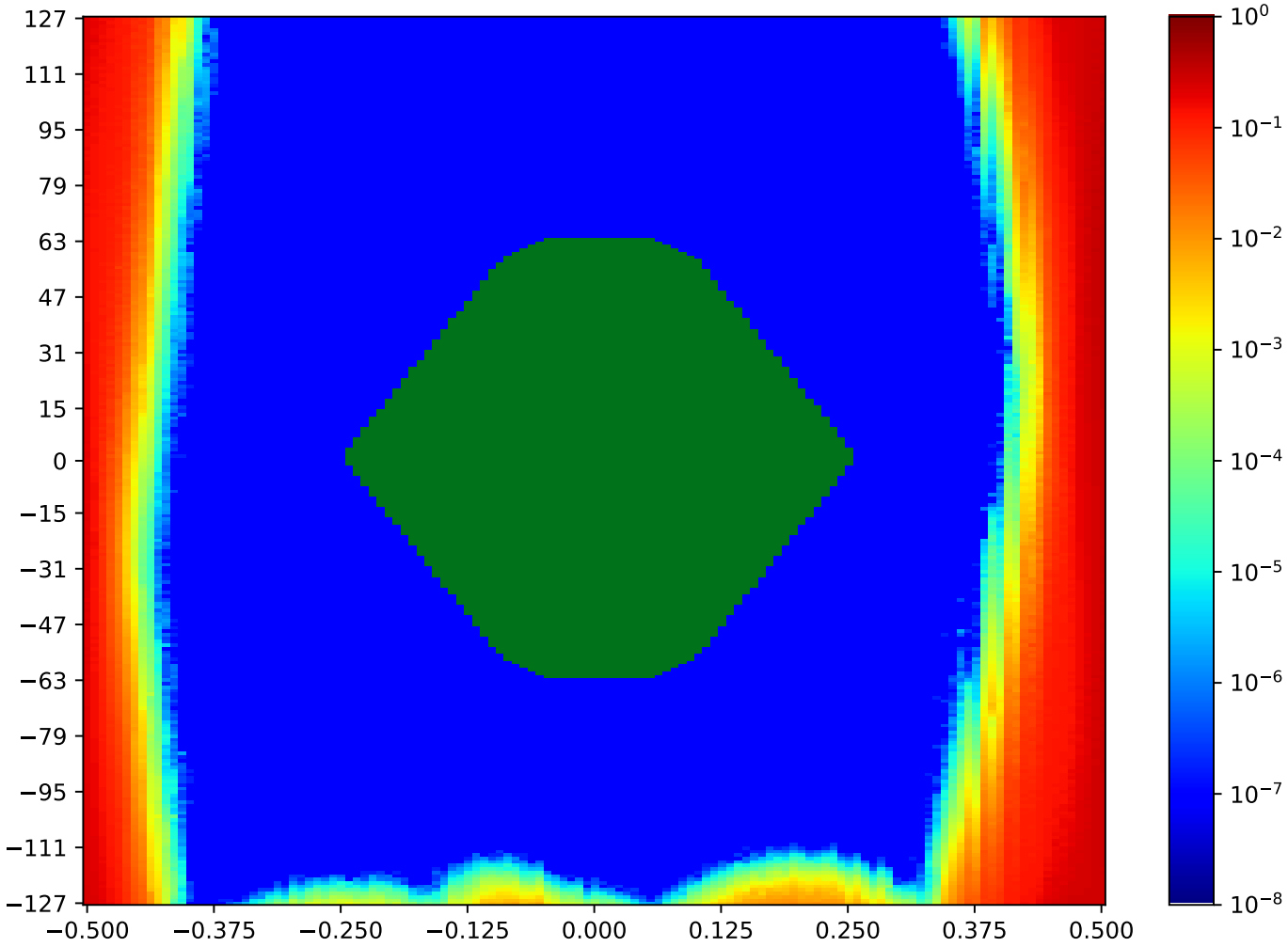


Figure 5.242: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.3 MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Table 5.224: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:11:03		2019-Nov-26 16:12:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22808	100	77.52%	241	94.51%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

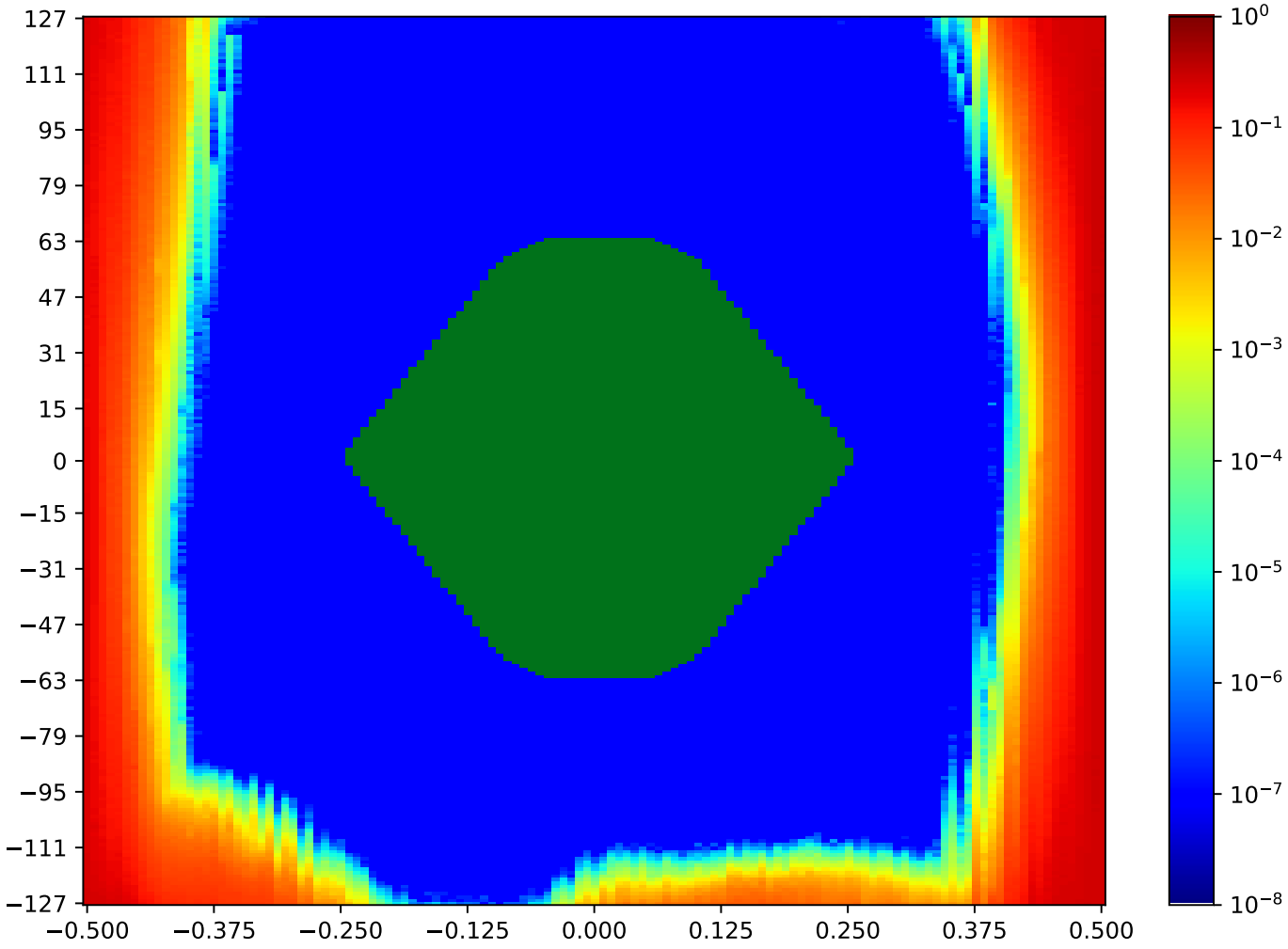


Figure 5.243: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.4 MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Table 5.225: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:05:06		2019-Nov-26 16:06:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23590	101	77.52%	244	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

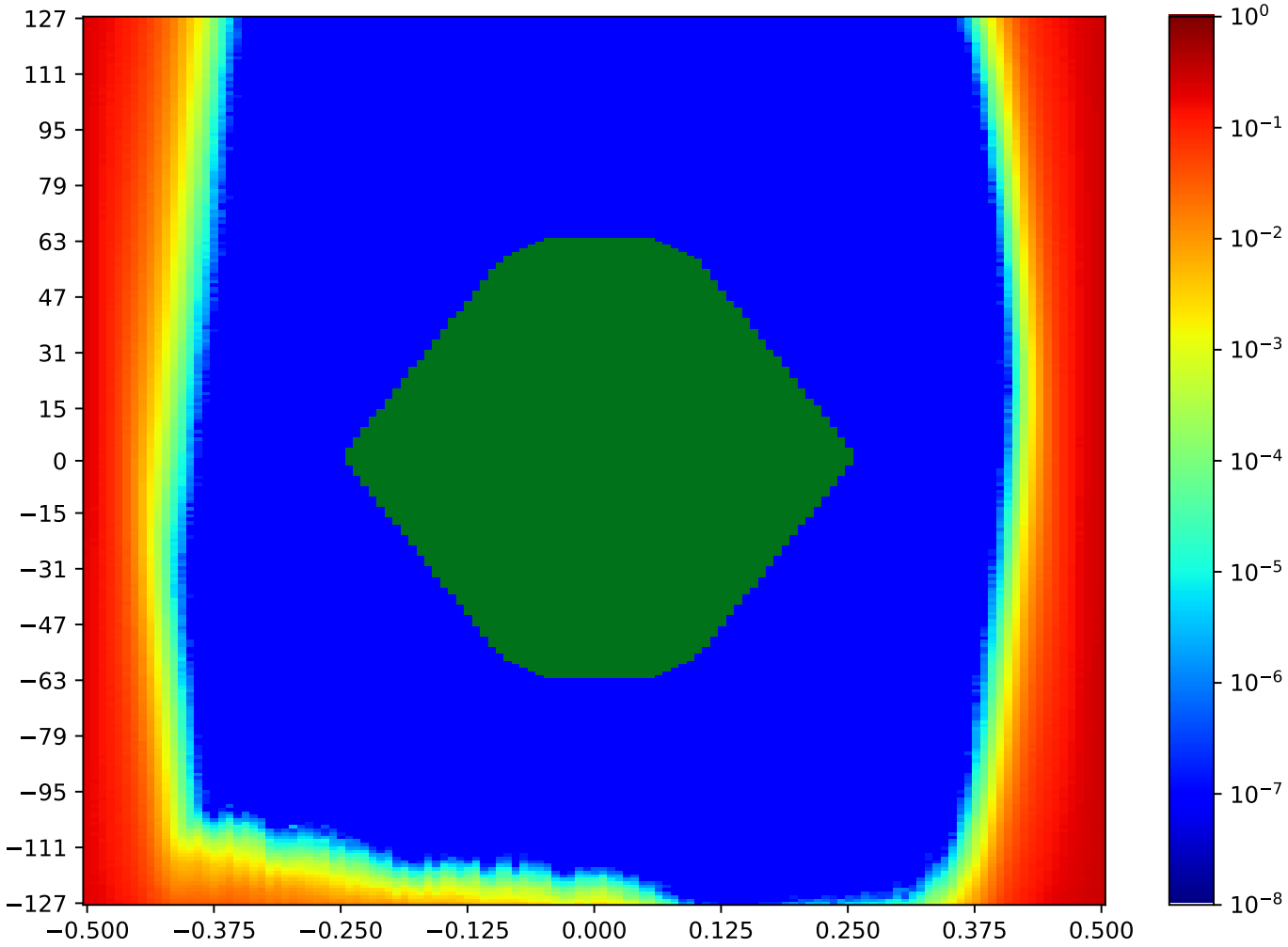


Figure 5.244: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.5 MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Table 5.226: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:14:25		2019-Nov-26 16:15:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	19694	98	75.97%	218	84.71%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

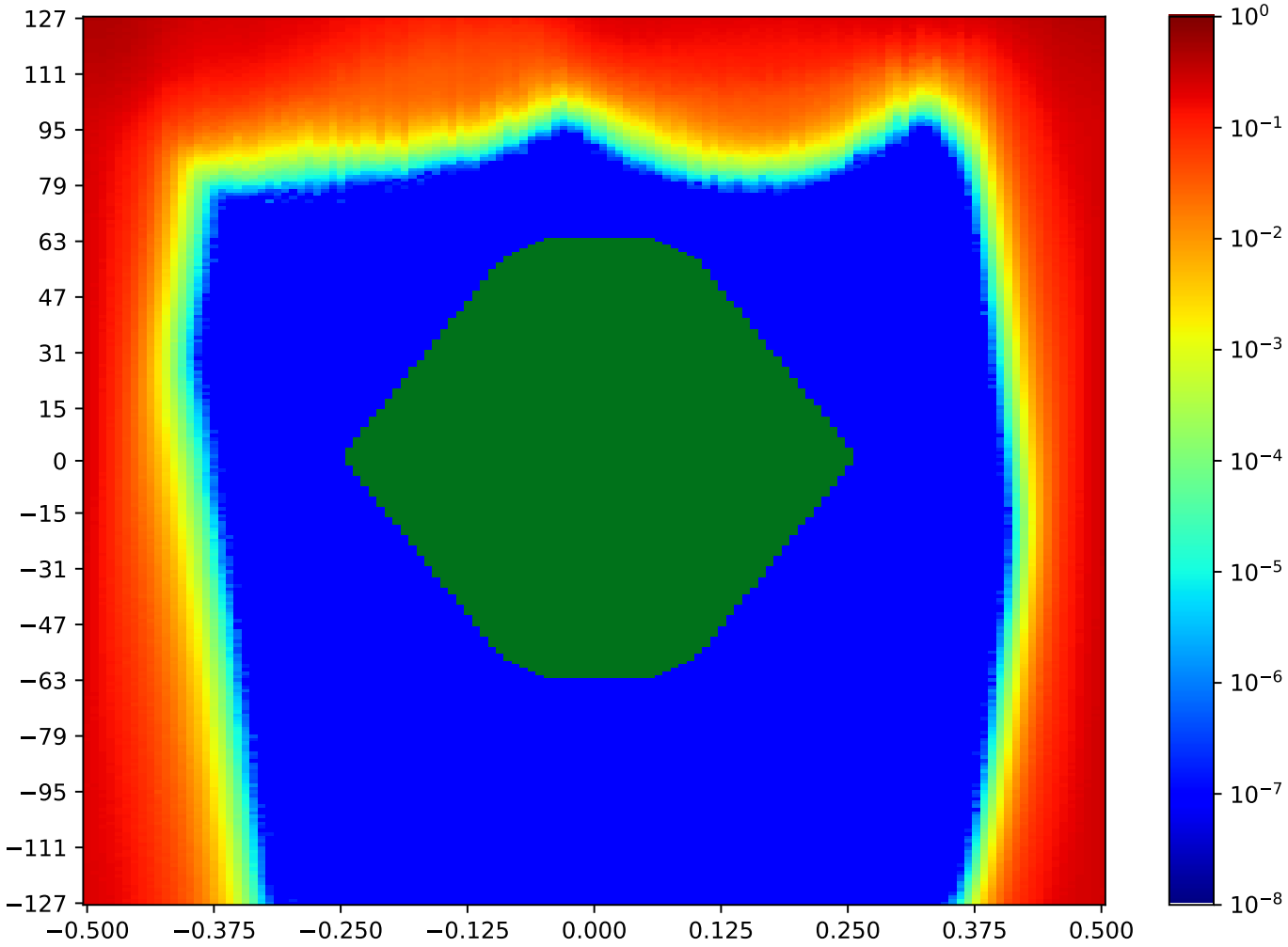


Figure 5.245: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.6 MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Table 5.227: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:03:58		2019-Nov-26 16:05:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22678	100	77.52%	229	89.02%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

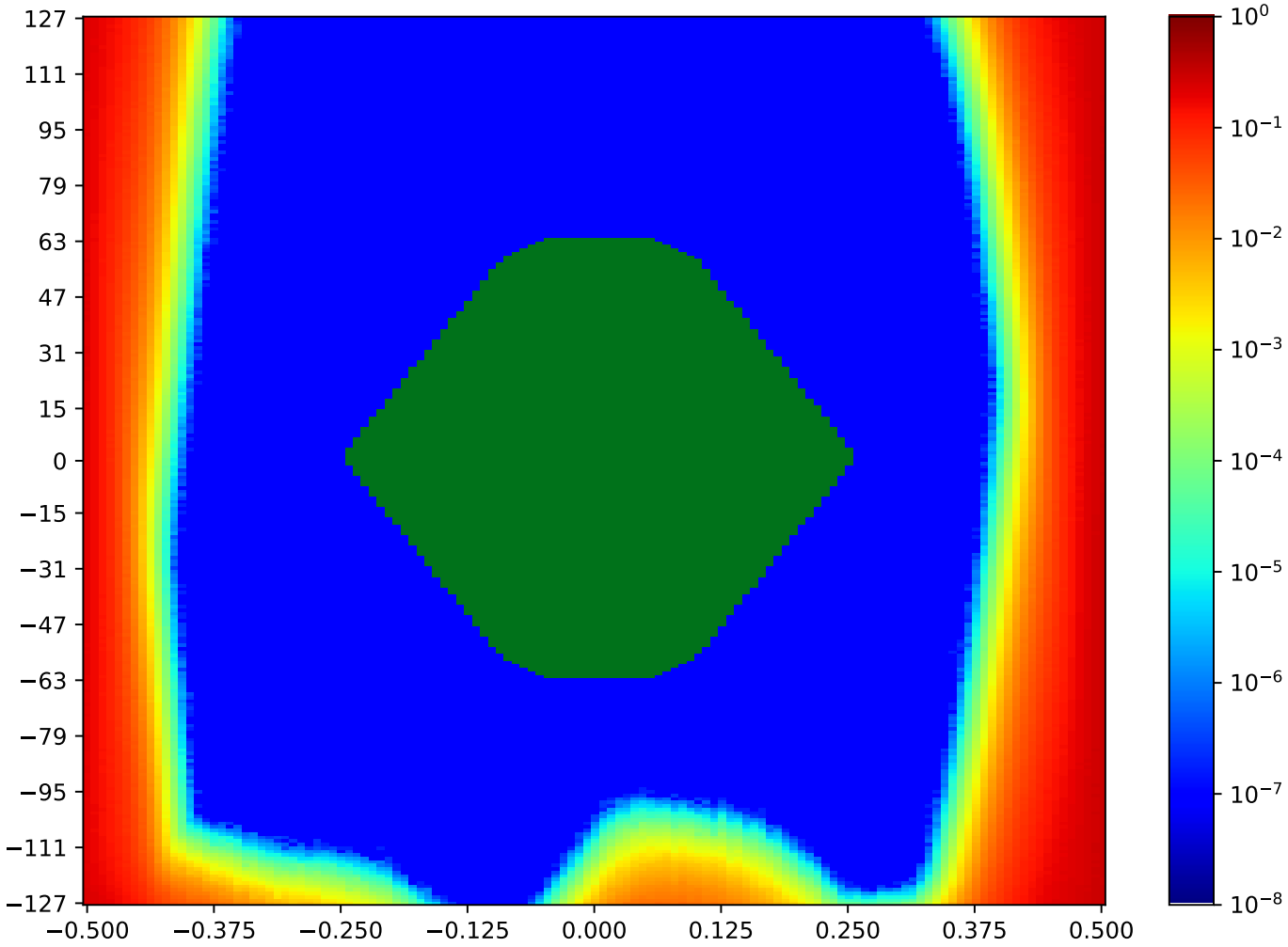


Figure 5.246: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.7 MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Table 5.228: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:16:39		2019-Nov-26 16:17:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21690	100	77.52%	227	89.02%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

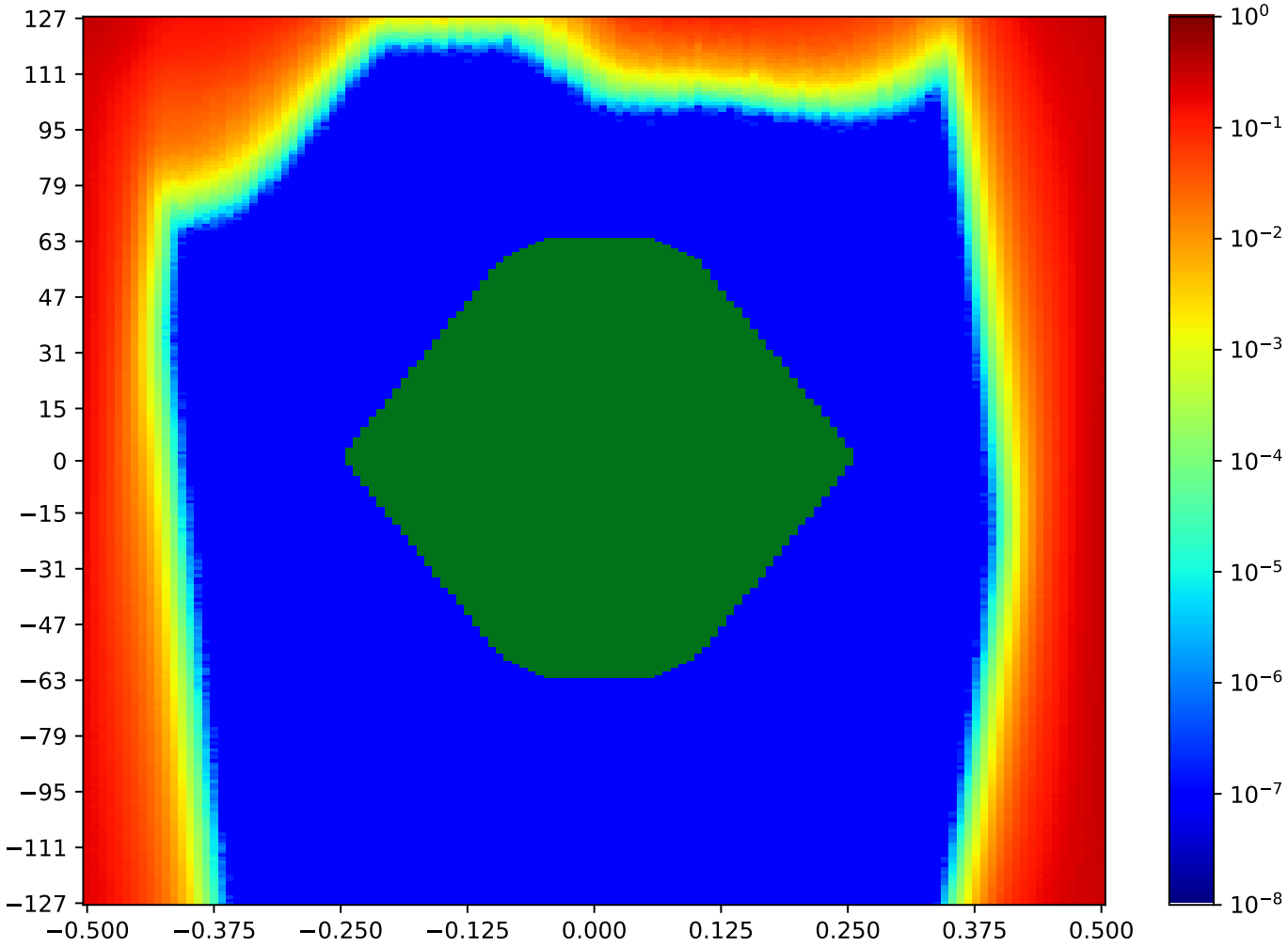


Figure 5.247: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.8 MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Table 5.229: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:06:13		2019-Nov-26 16:07:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24343	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

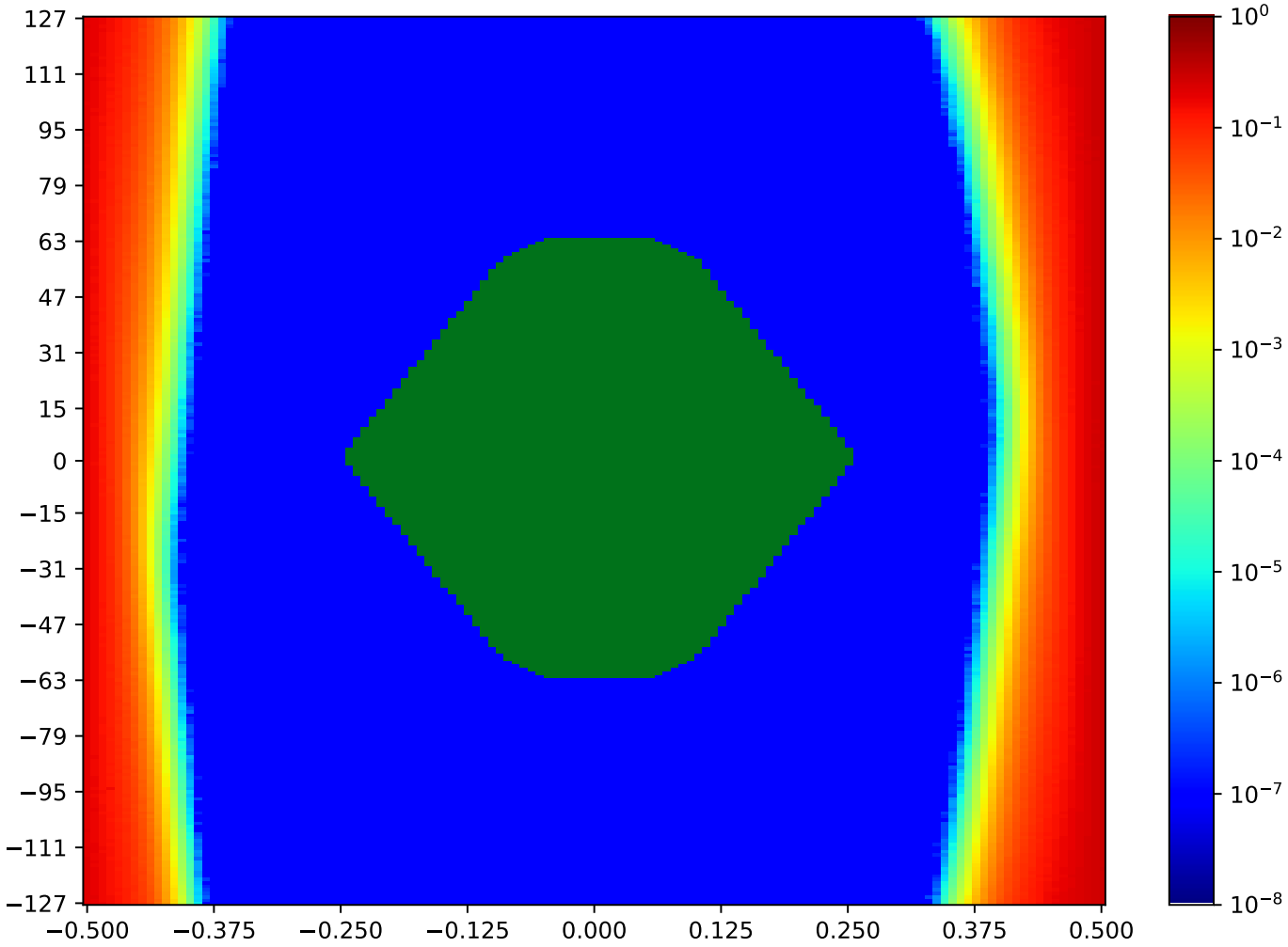


Figure 5.248: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.9 MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Table 5.230: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:15:33		2019-Nov-26 16:16:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	17857	97	75.19%	202	79.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

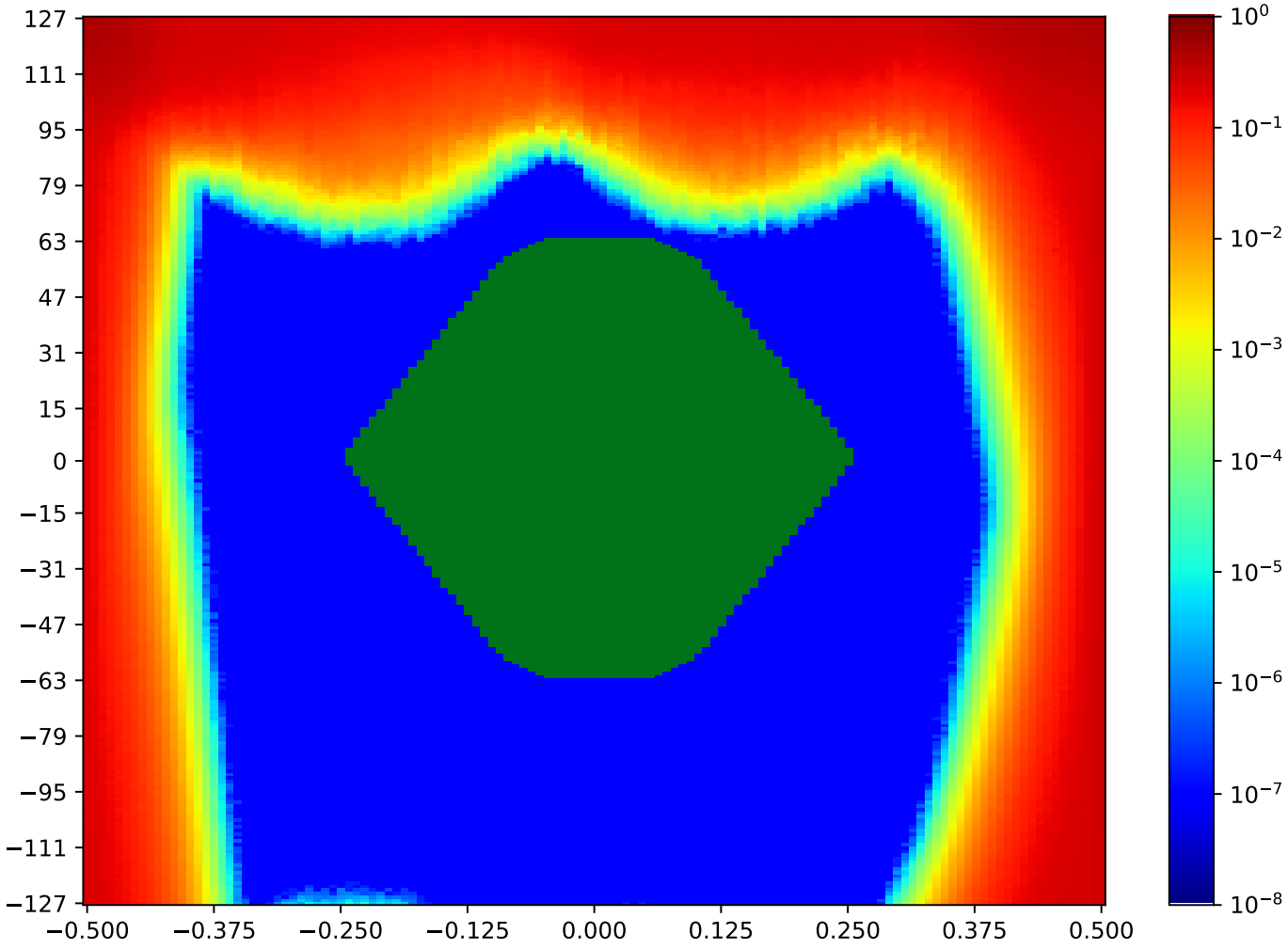


Figure 5.249: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.10 MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Table 5.231: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:08:35		2019-Nov-26 16:09:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24043	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

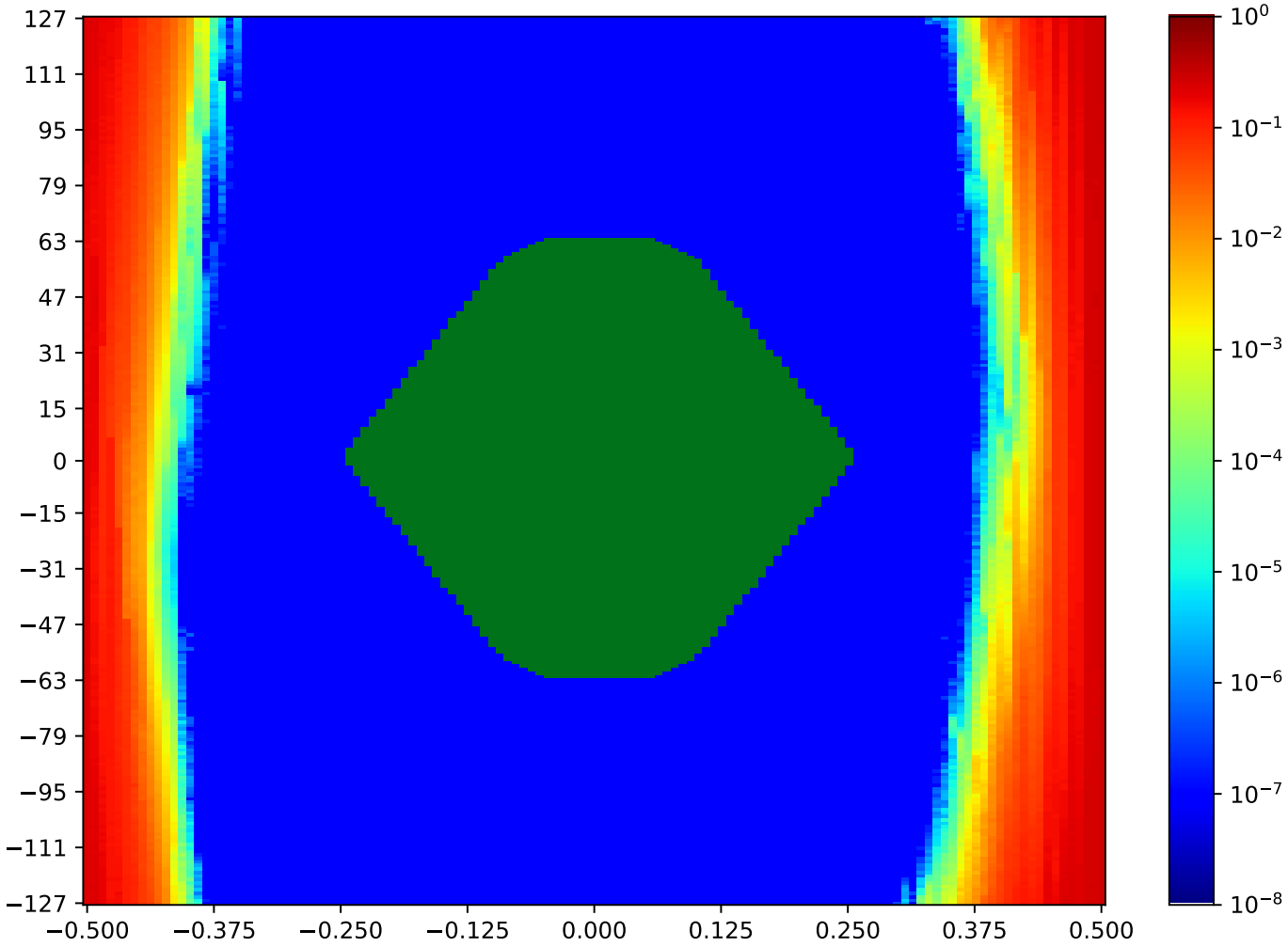


Figure 5.250: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.11 MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Table 5.232: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:13:18		2019-Nov-26 16:14:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	21245	100	77.52%	221	86.67%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

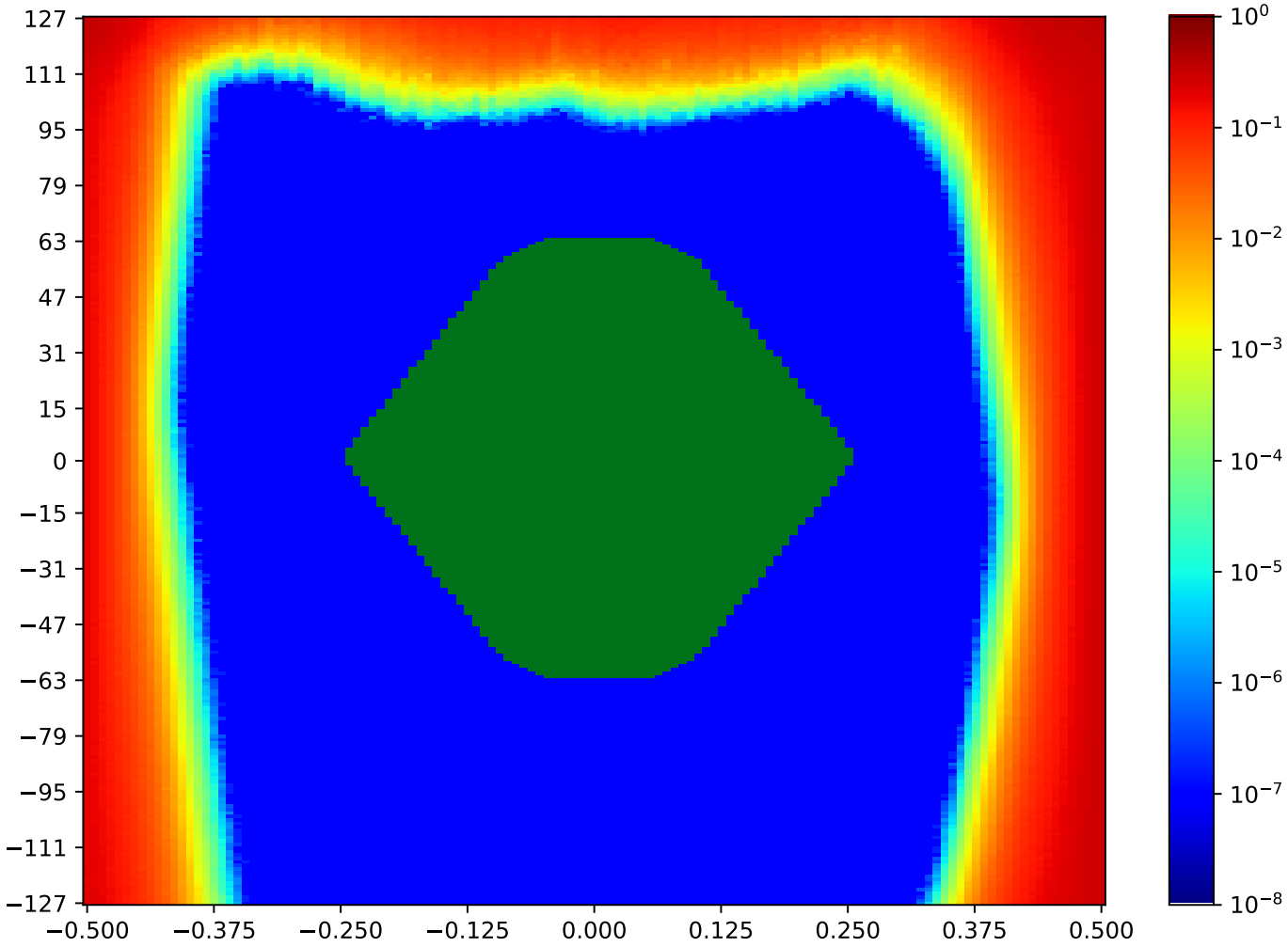


Figure 5.251: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.19.12 MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Table 5.233: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:12:11		2019-Nov-26 16:13:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23594	98	75.97%	250	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

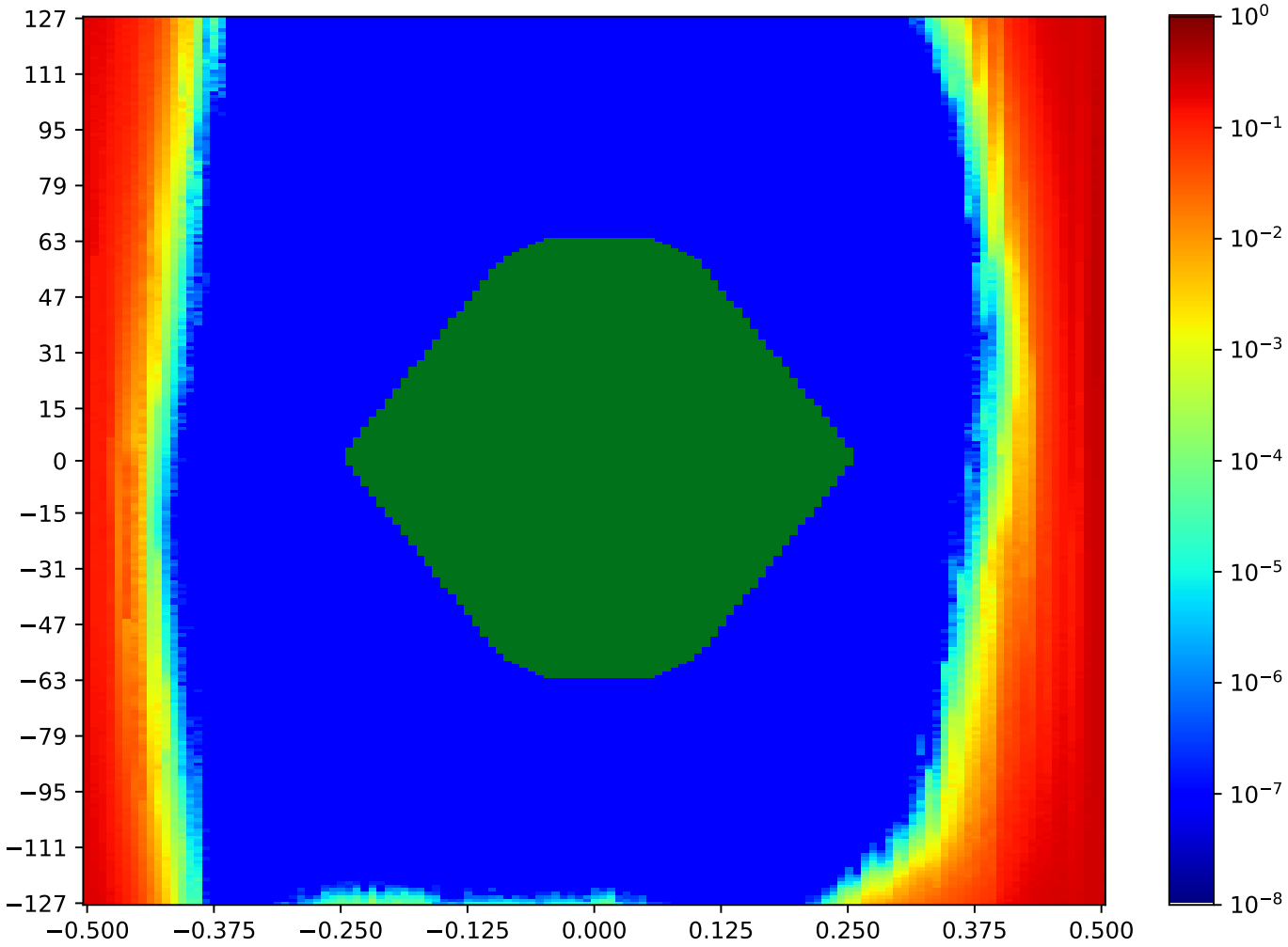


Figure 5.252: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20 MSP_A TX2 MSP_C RX13 Minipod Loopback

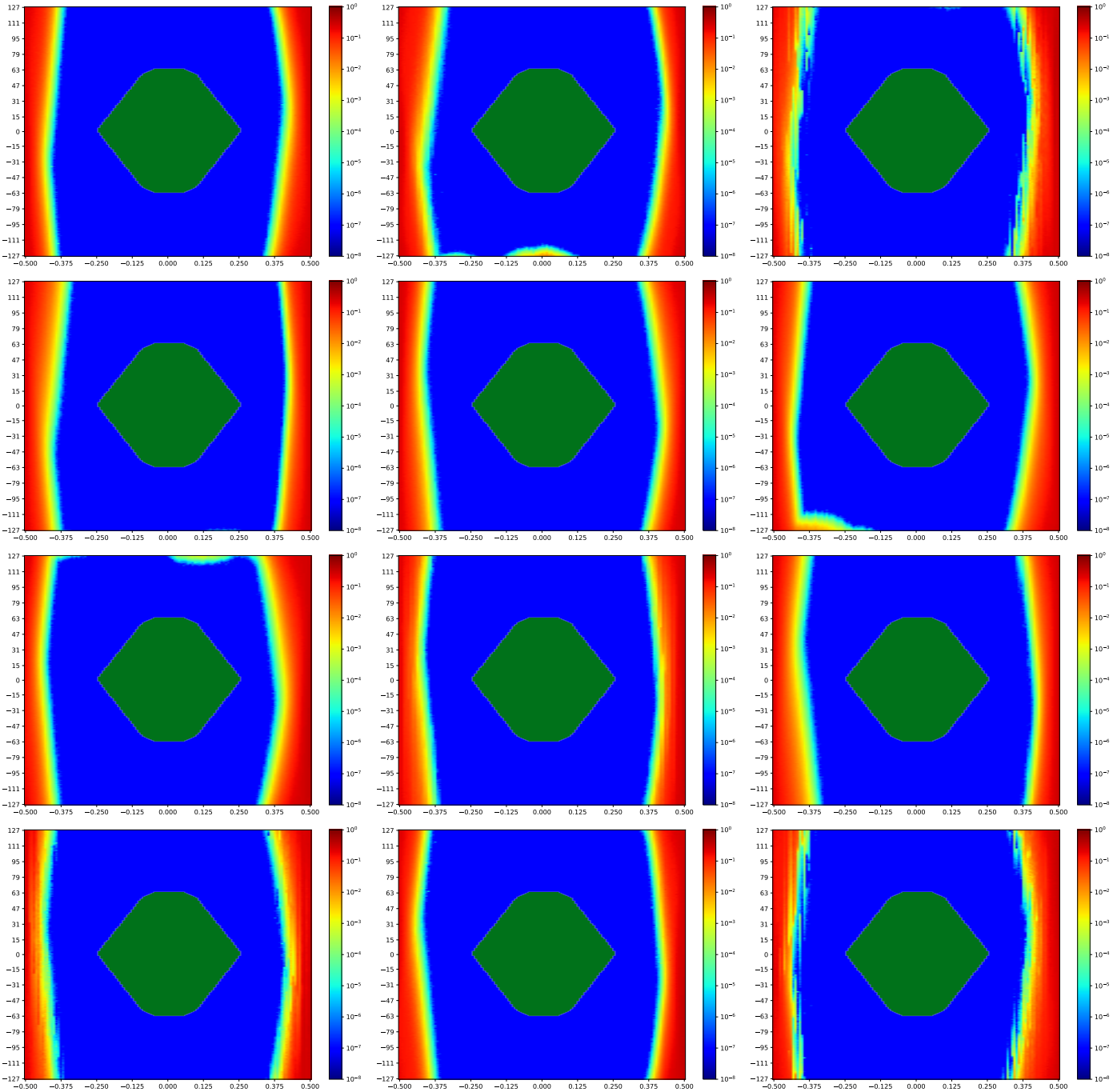


Figure 5.253: MSP_A TX2 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.266.

5.20.1 MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Table 5.234: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:21:35		2019-Nov-26 16:22:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24249	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

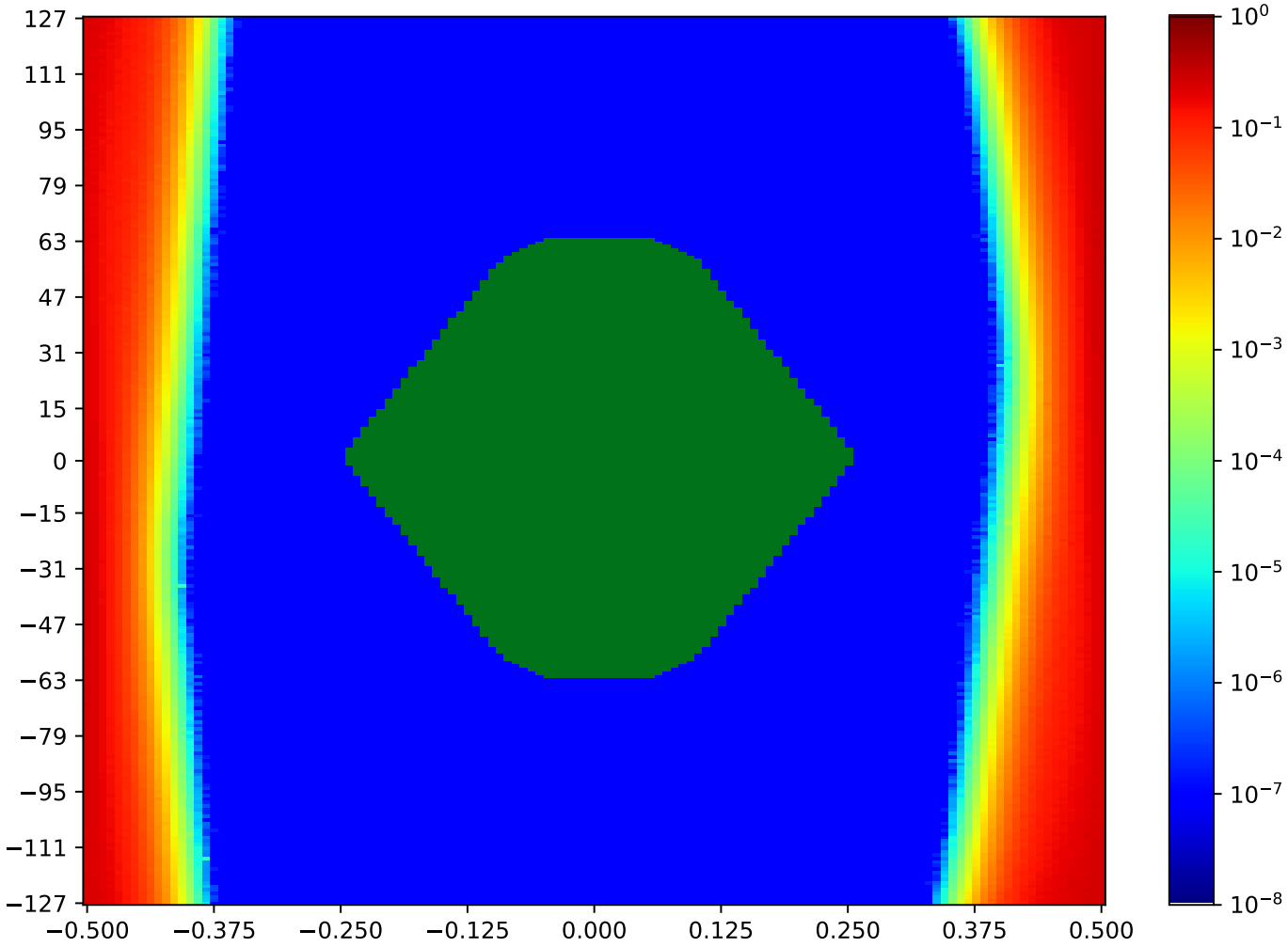


Figure 5.254: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.2 MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Table 5.235: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:19:10		2019-Nov-26 16:20:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23503	100	77.52%	241	94.51%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

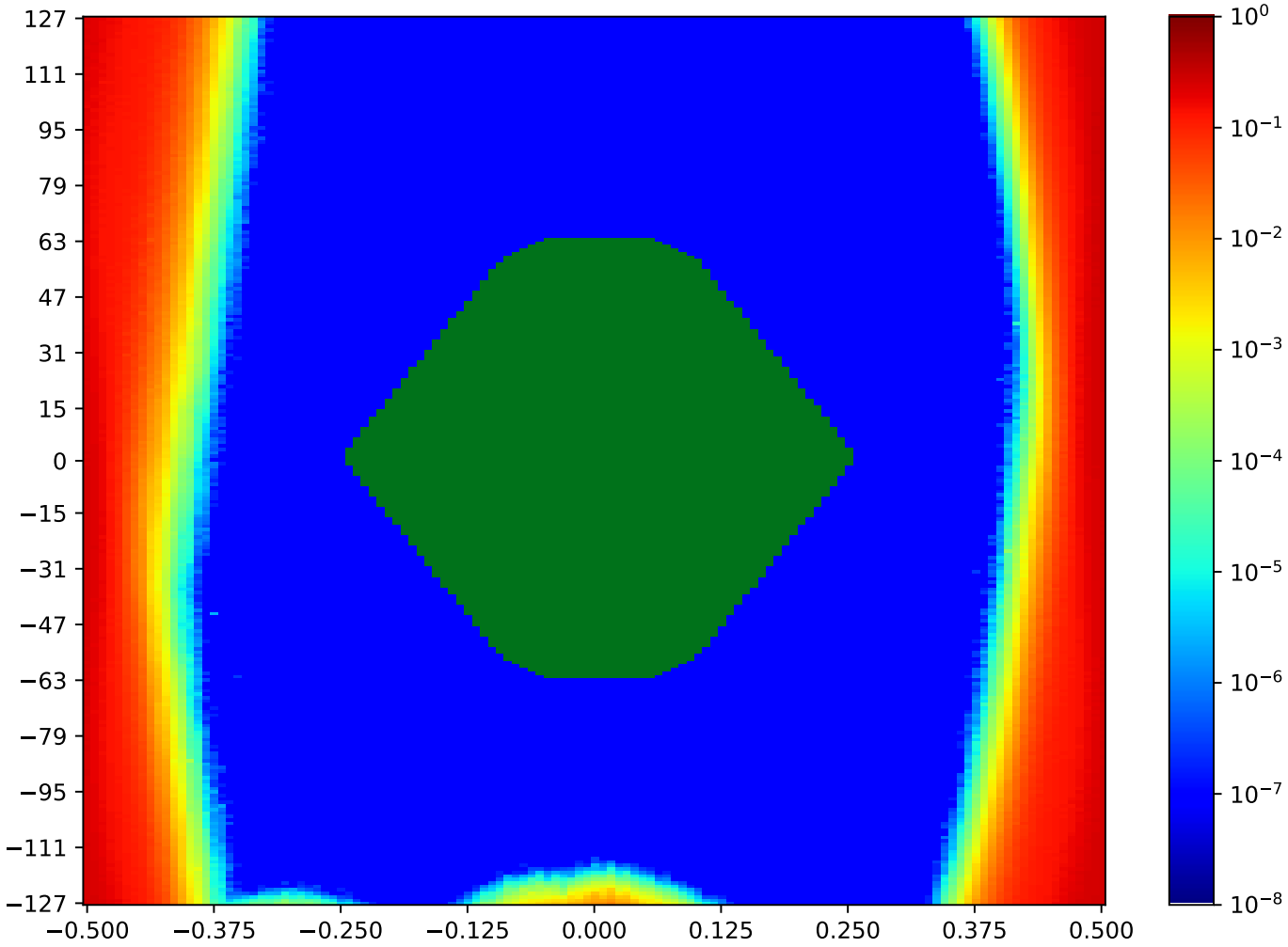


Figure 5.255: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.3 MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Table 5.236: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:25:27		2019-Nov-26 16:26:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23953	101	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

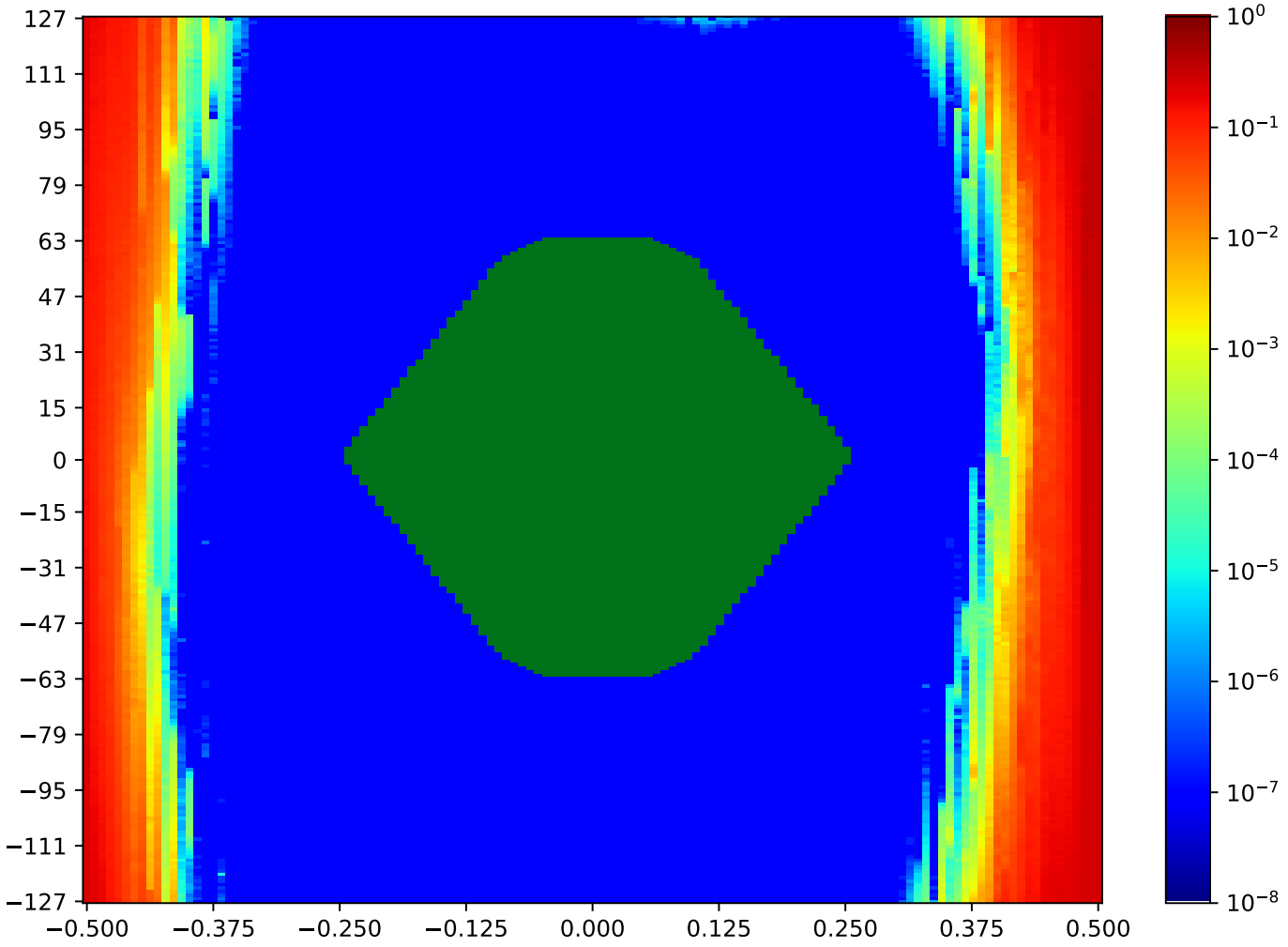


Figure 5.256: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.4 MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Table 5.237: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:17:46		2019-Nov-26 16:19:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24334	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

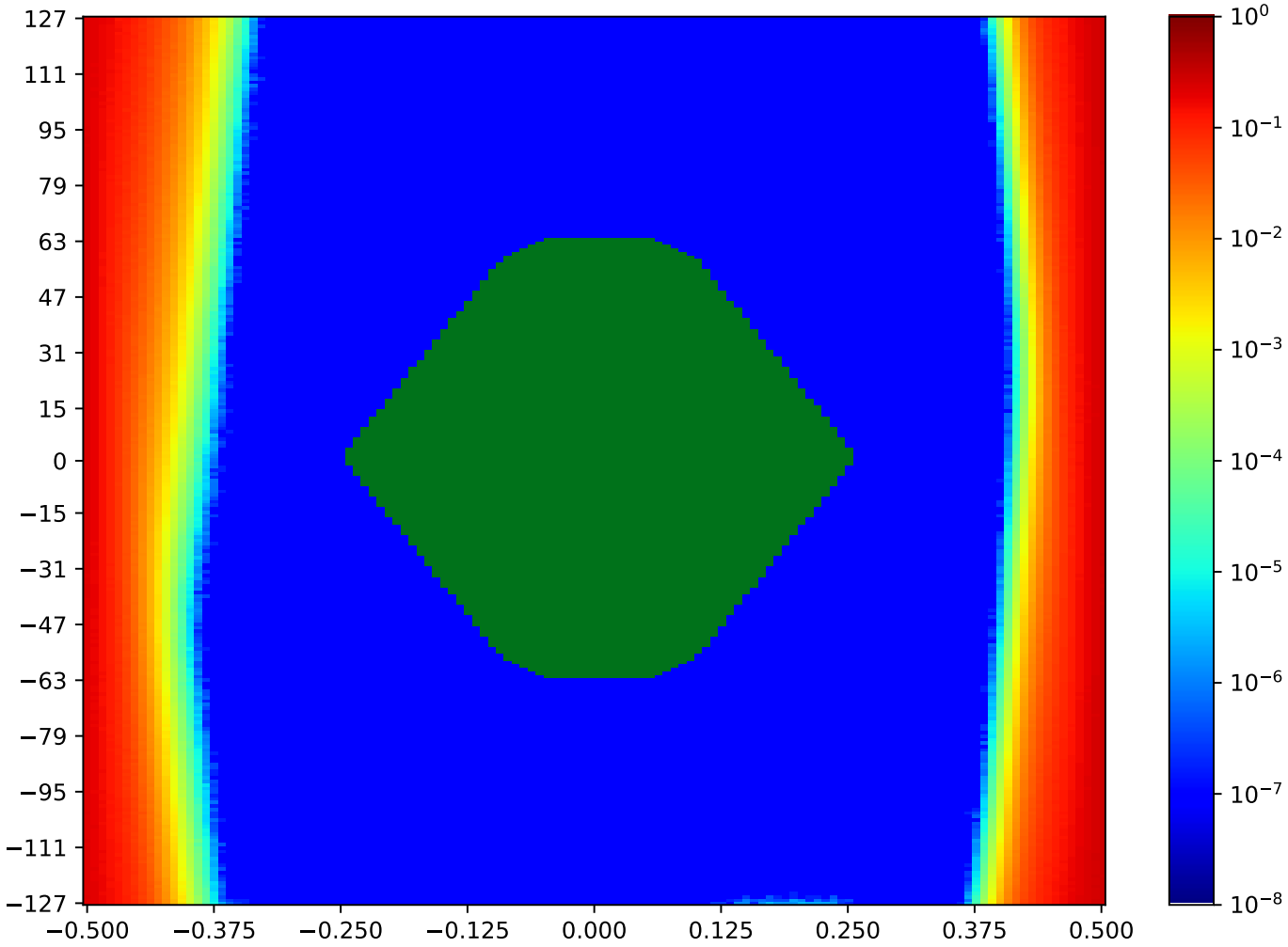


Figure 5.257: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.5 MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Table 5.238: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:29:16		2019-Nov-26 16:30:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24081	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

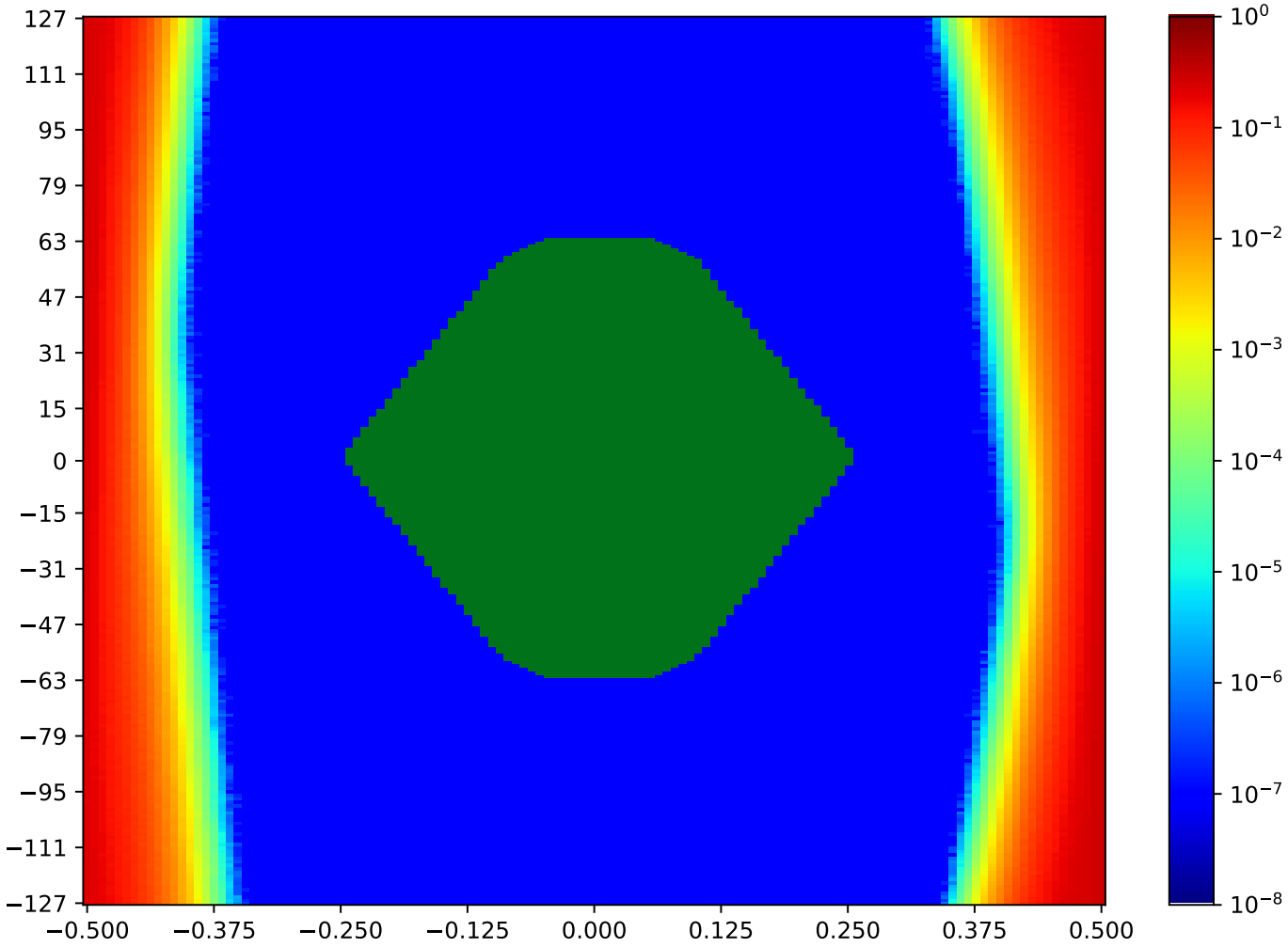


Figure 5.258: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.6 MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Table 5.239: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:20:28		2019-Nov-26 16:21:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23791	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

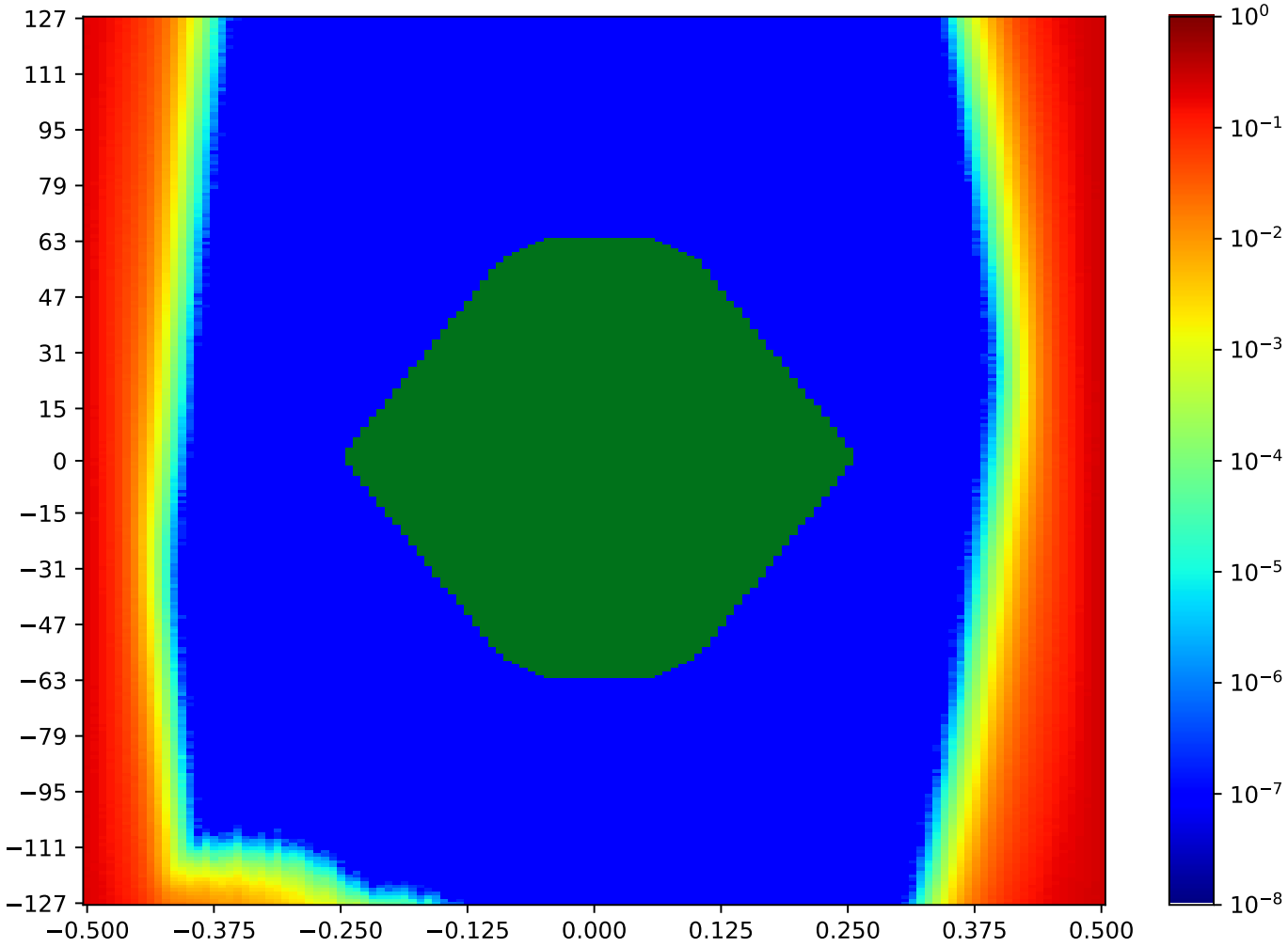


Figure 5.259: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.7 MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Table 5.240: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:31:32		2019-Nov-26 16:32:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23238	97	75.19%	252	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

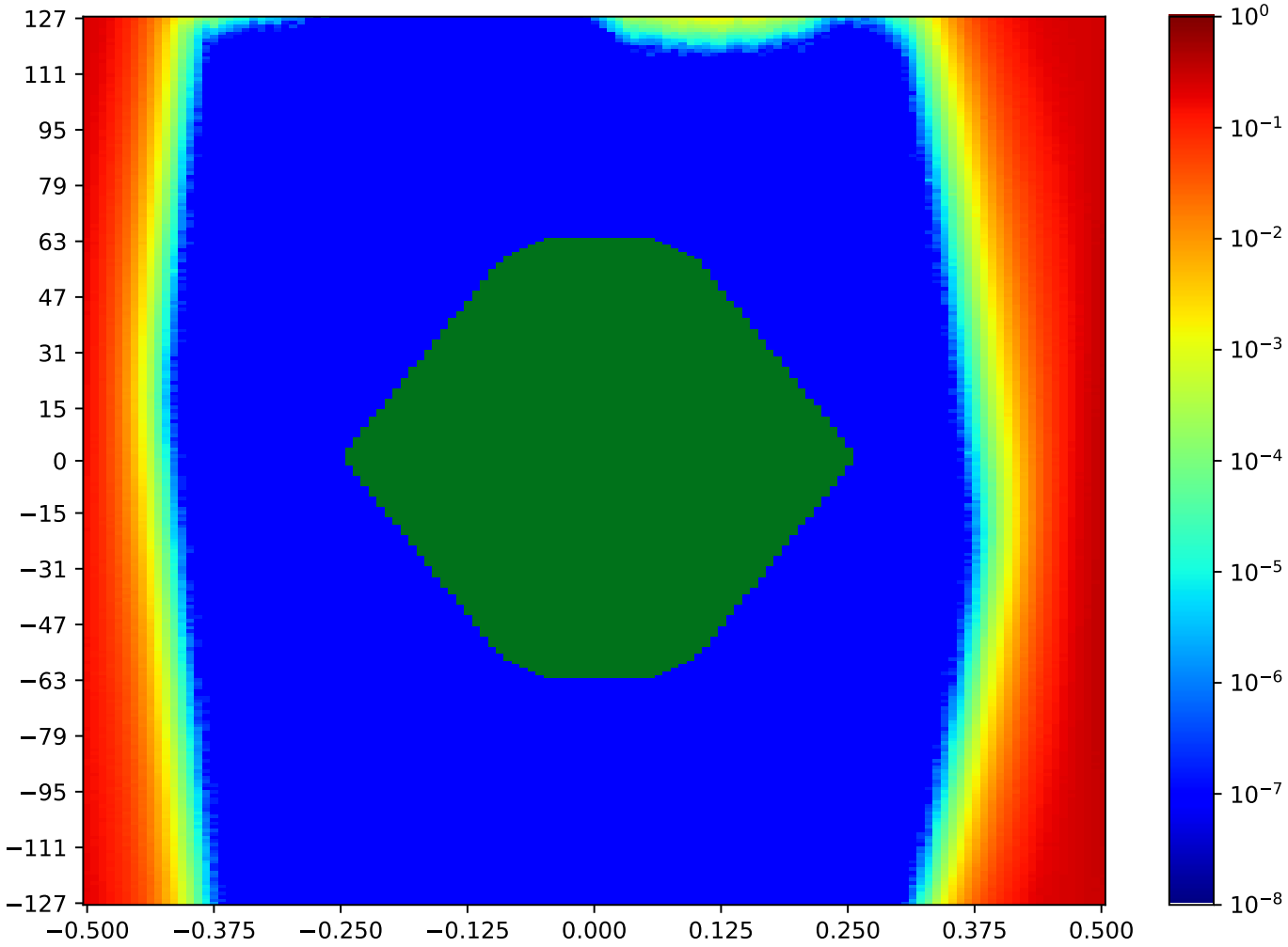


Figure 5.260: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.8 MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Table 5.241: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:22:43		2019-Nov-26 16:24:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24521	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

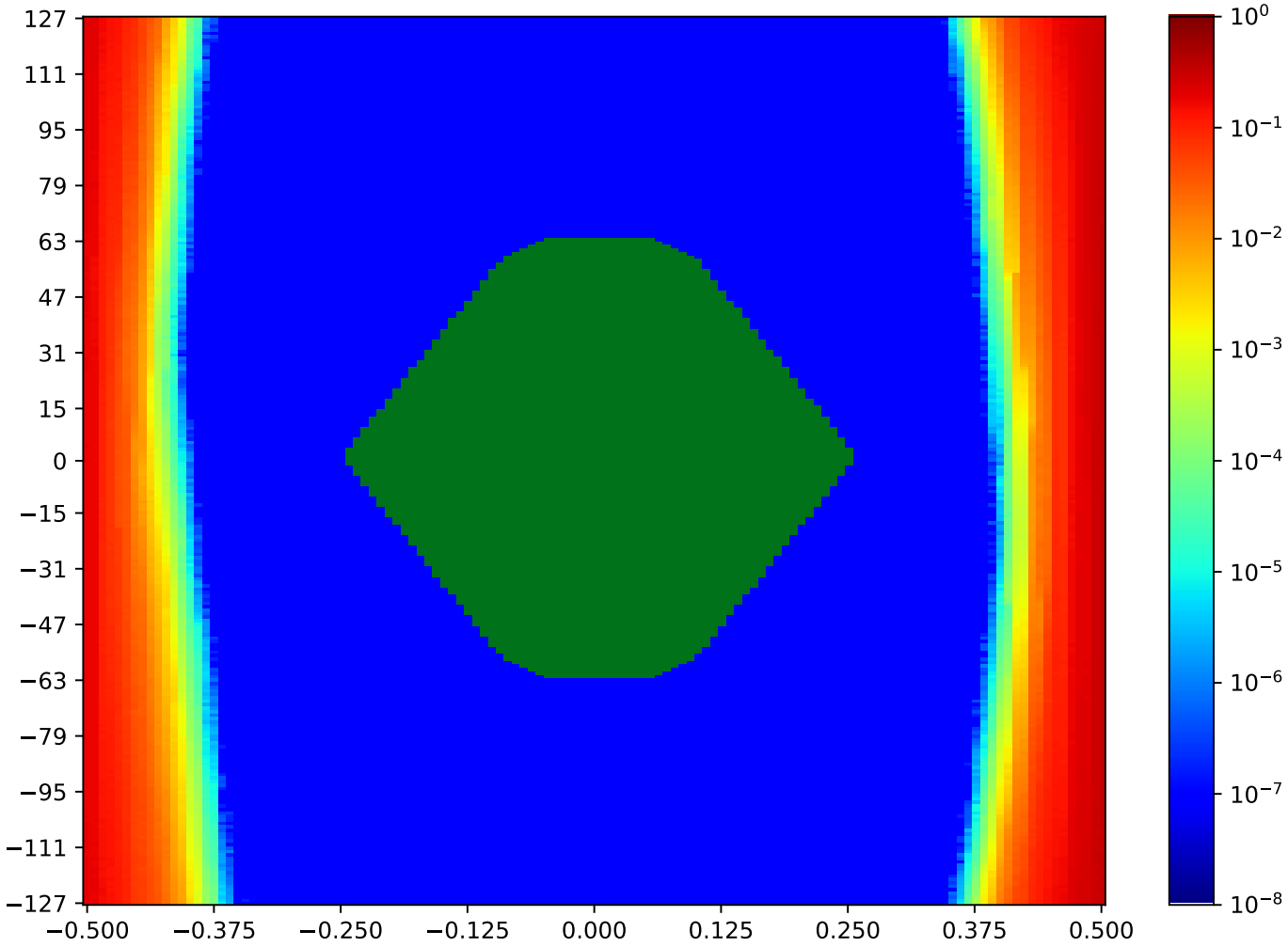


Figure 5.261: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.9 MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Table 5.242: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:30:24		2019-Nov-26 16:31:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23861	96	74.42%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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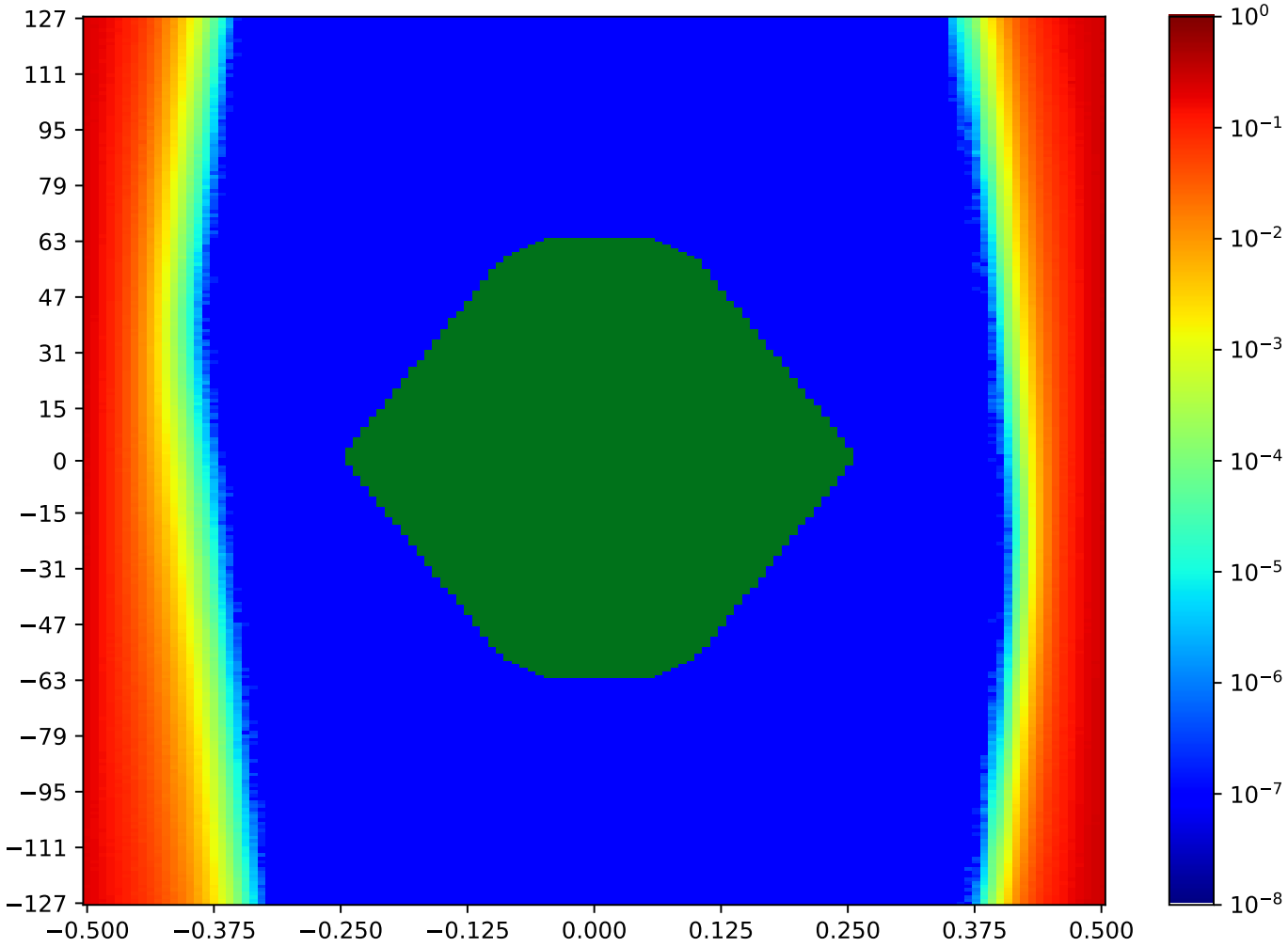


Figure 5.262: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.10 MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Table 5.243: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:24:06		2019-Nov-26 16:25:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24844	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

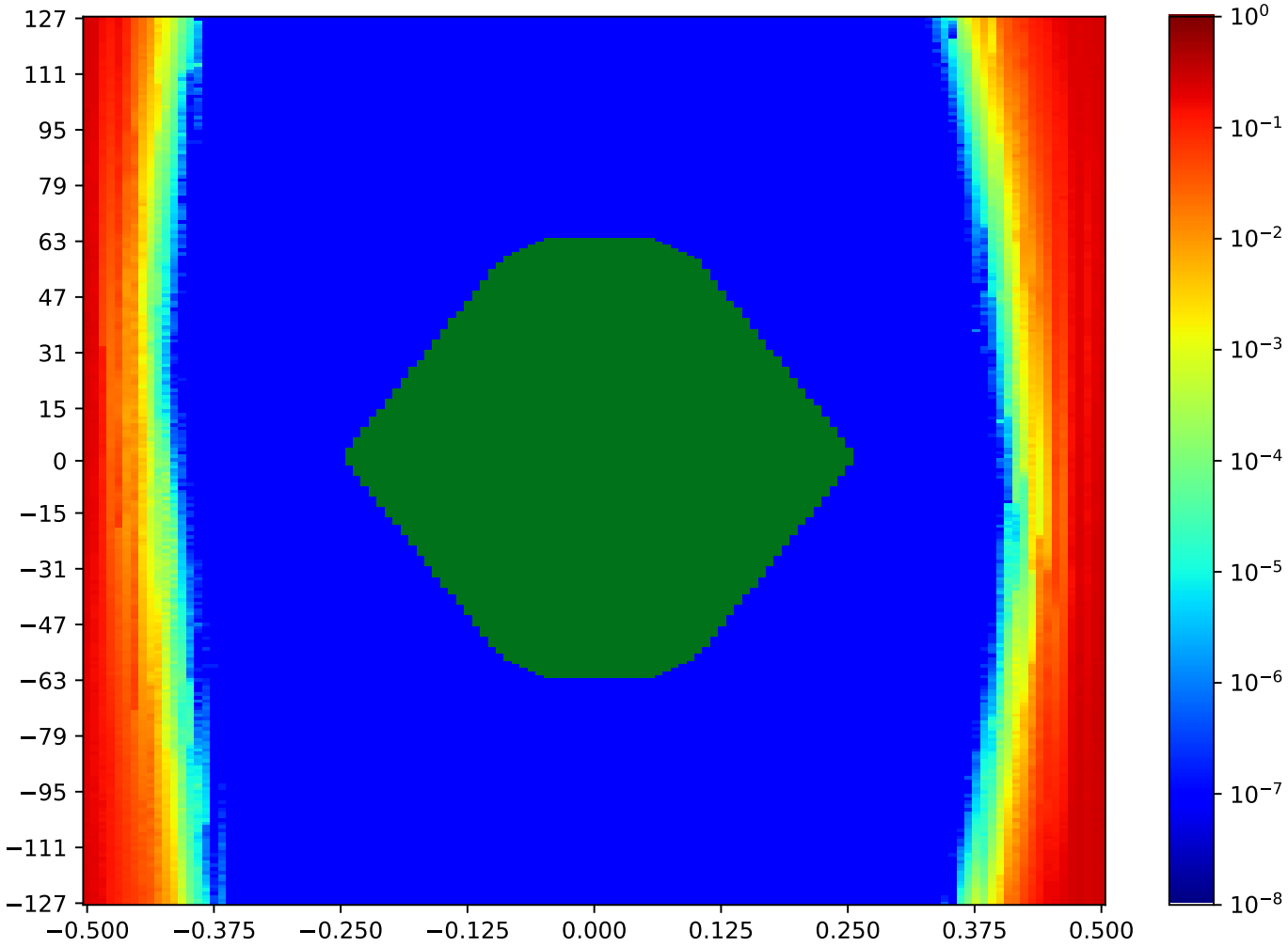


Figure 5.263: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.11 MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Table 5.244: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:27:57		2019-Nov-26 16:29:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24881	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

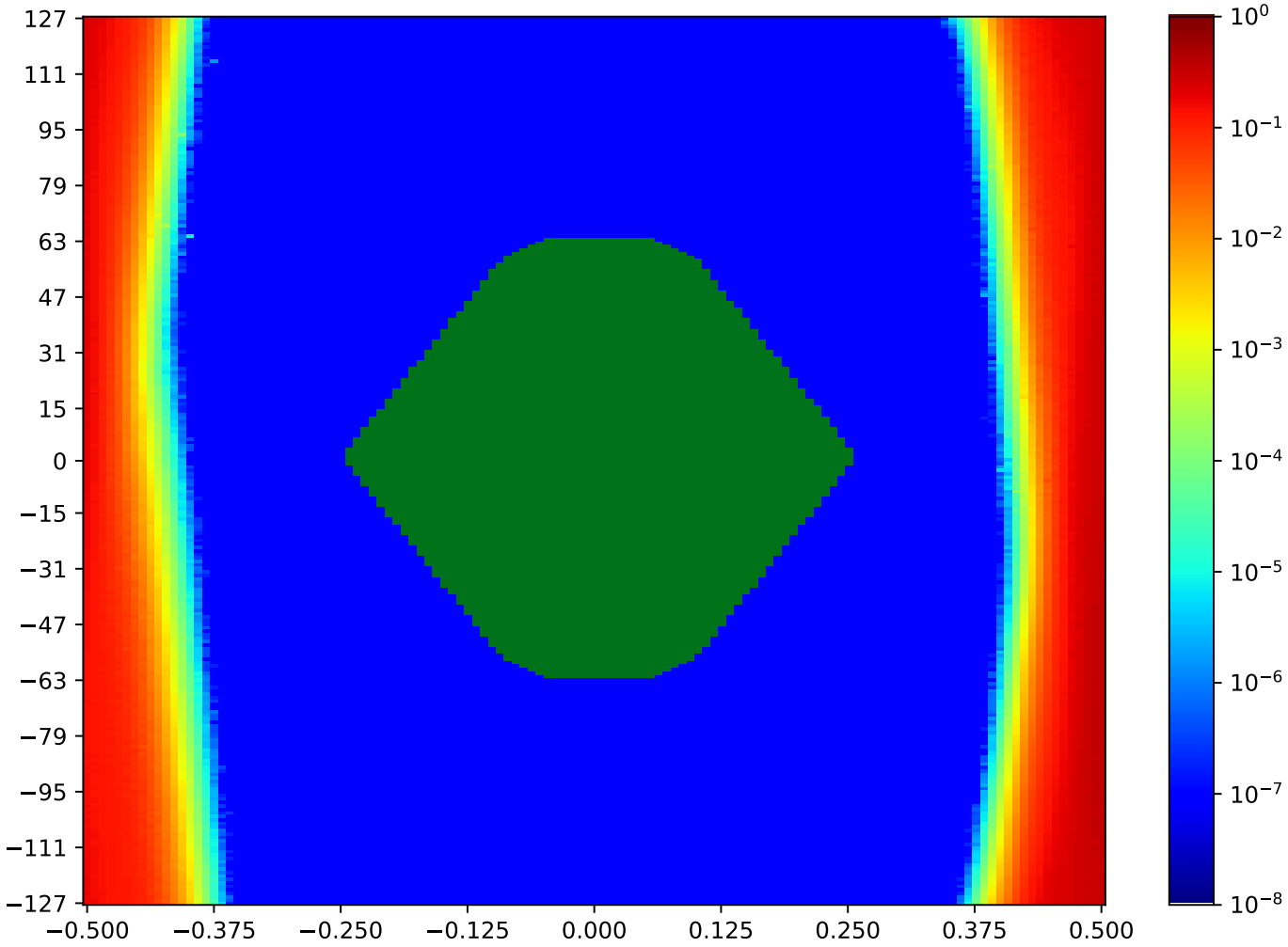


Figure 5.264: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.20.12 MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Table 5.245: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:26:34		2019-Nov-26 16:27:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24108	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

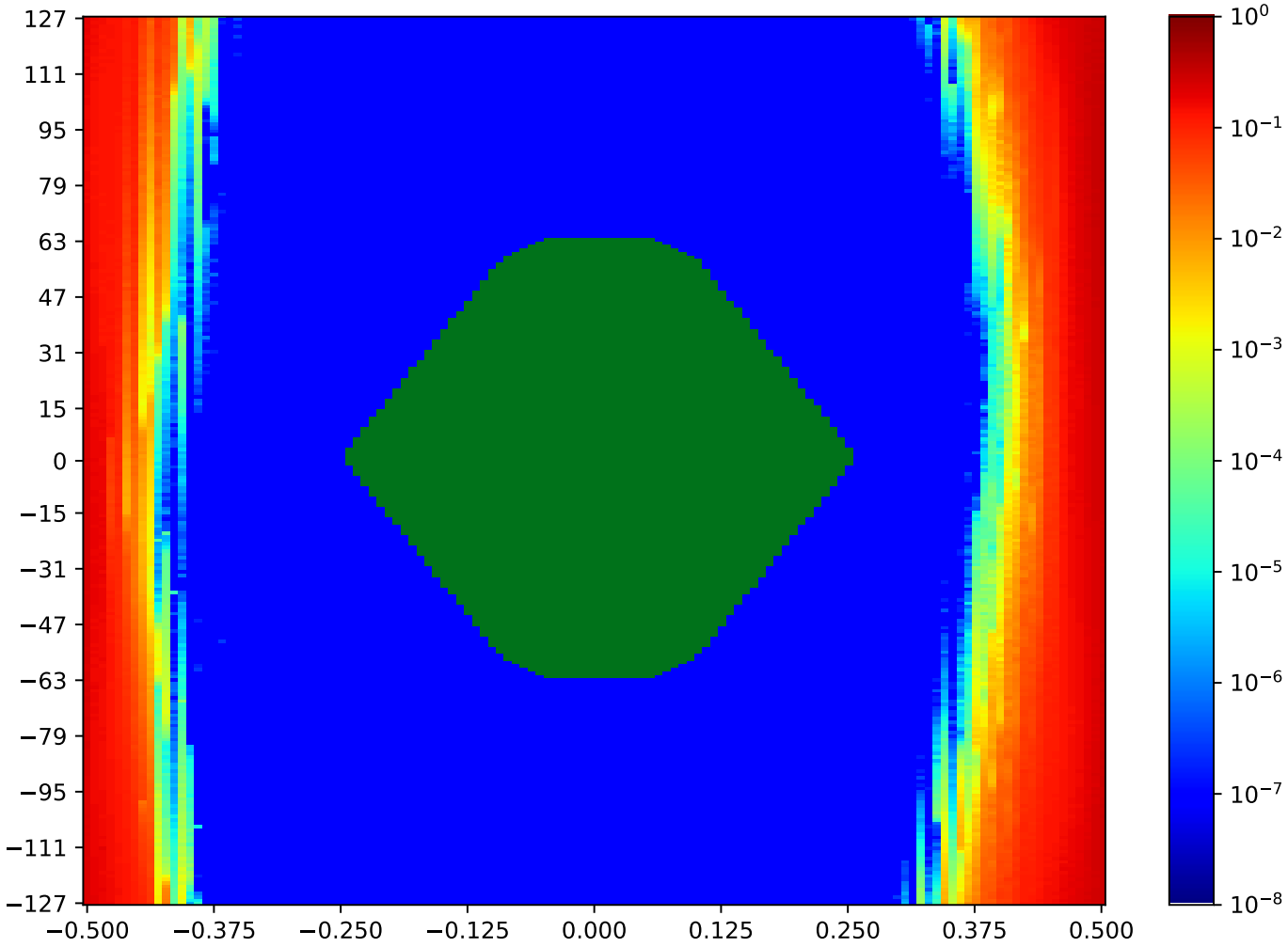


Figure 5.265: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21 MSP_C TX3 MSP_A RX3 Minipod Loopback

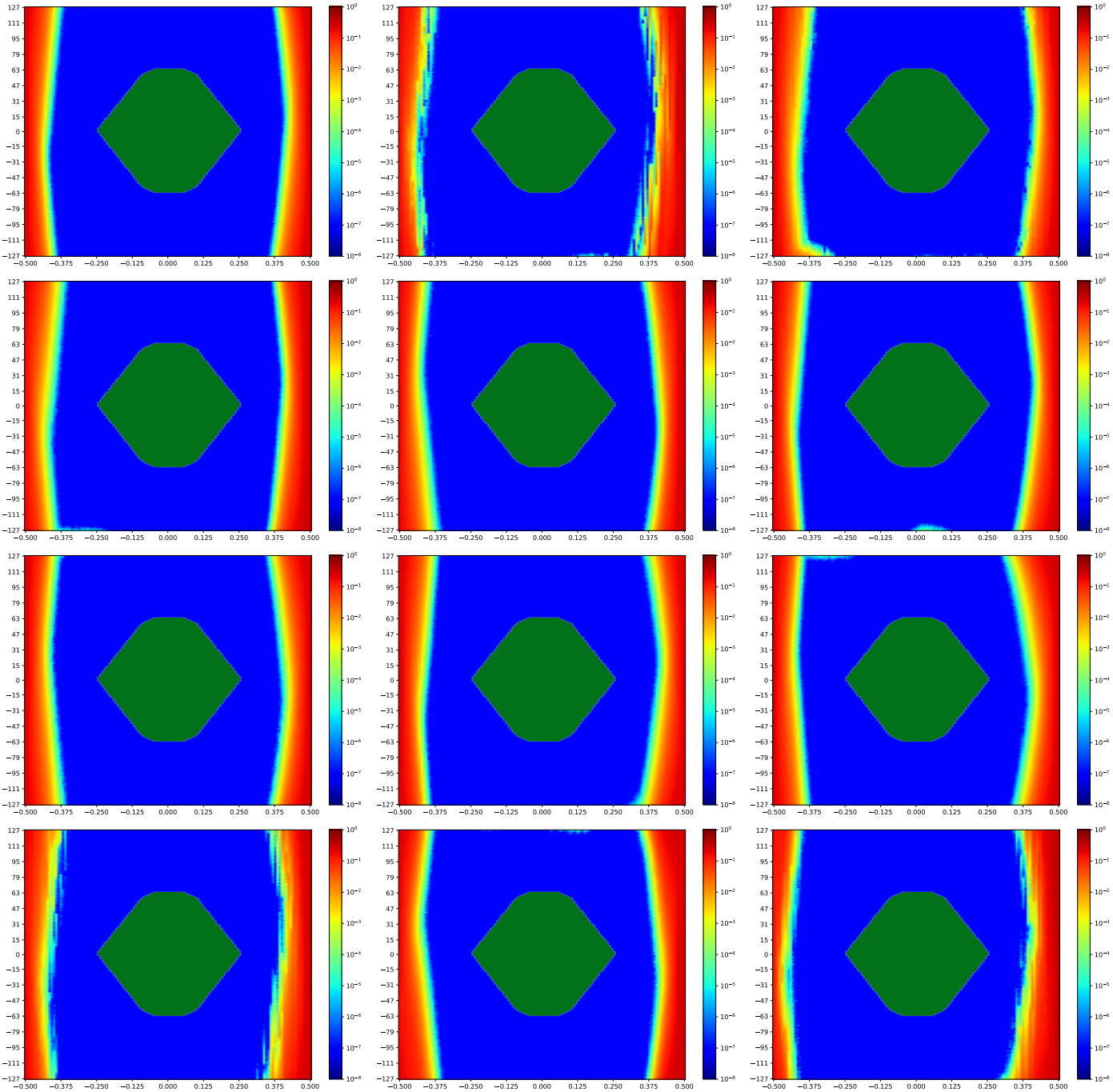


Figure 5.266: MSP_C TX3 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 5.279.

5.21.1 MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Table 5.246: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:36:19		2019-Nov-26 16:37:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	25040	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

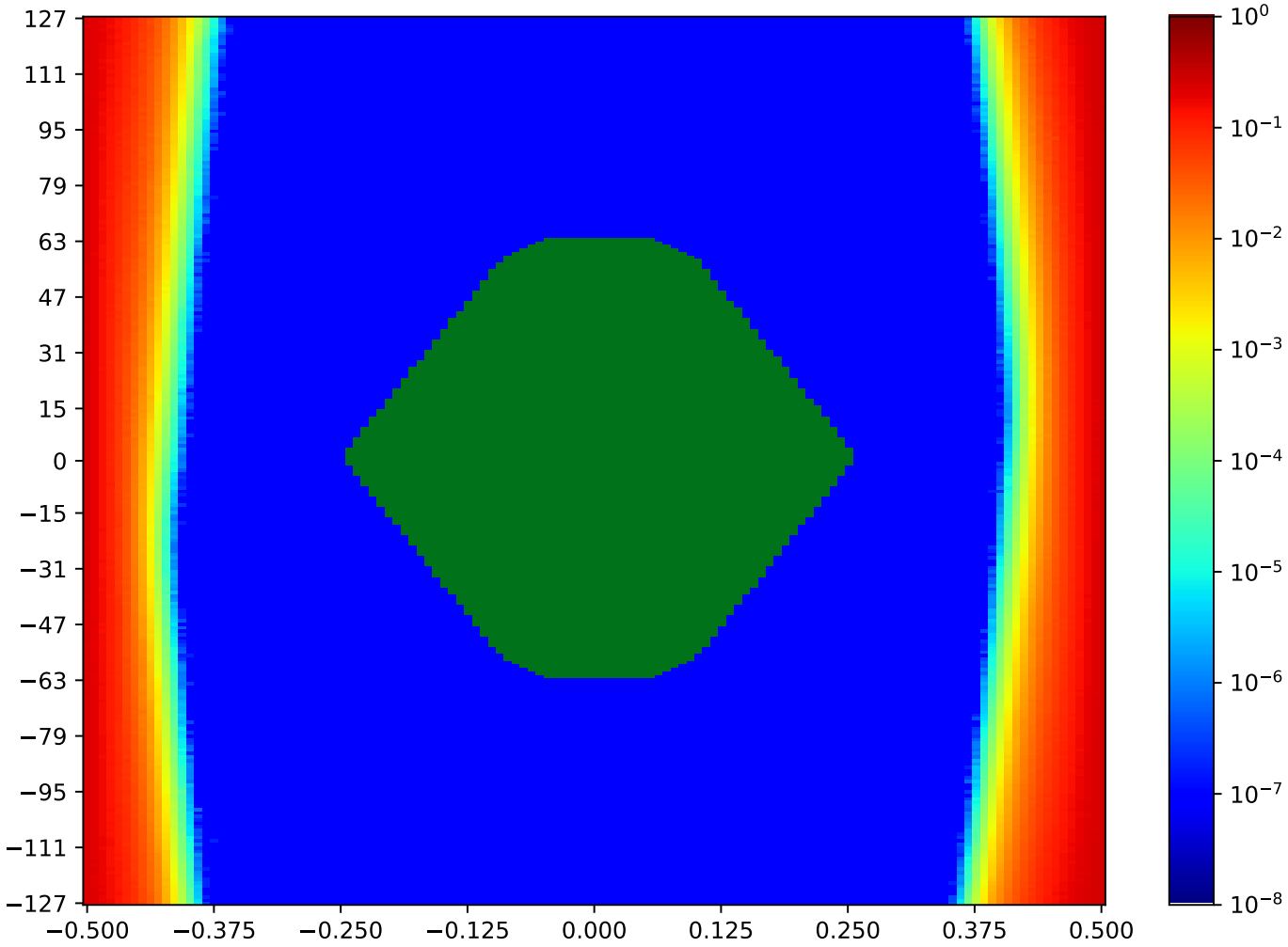


Figure 5.267: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.2 MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Table 5.247: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:38:45		2019-Nov-26 16:39:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24233	100	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

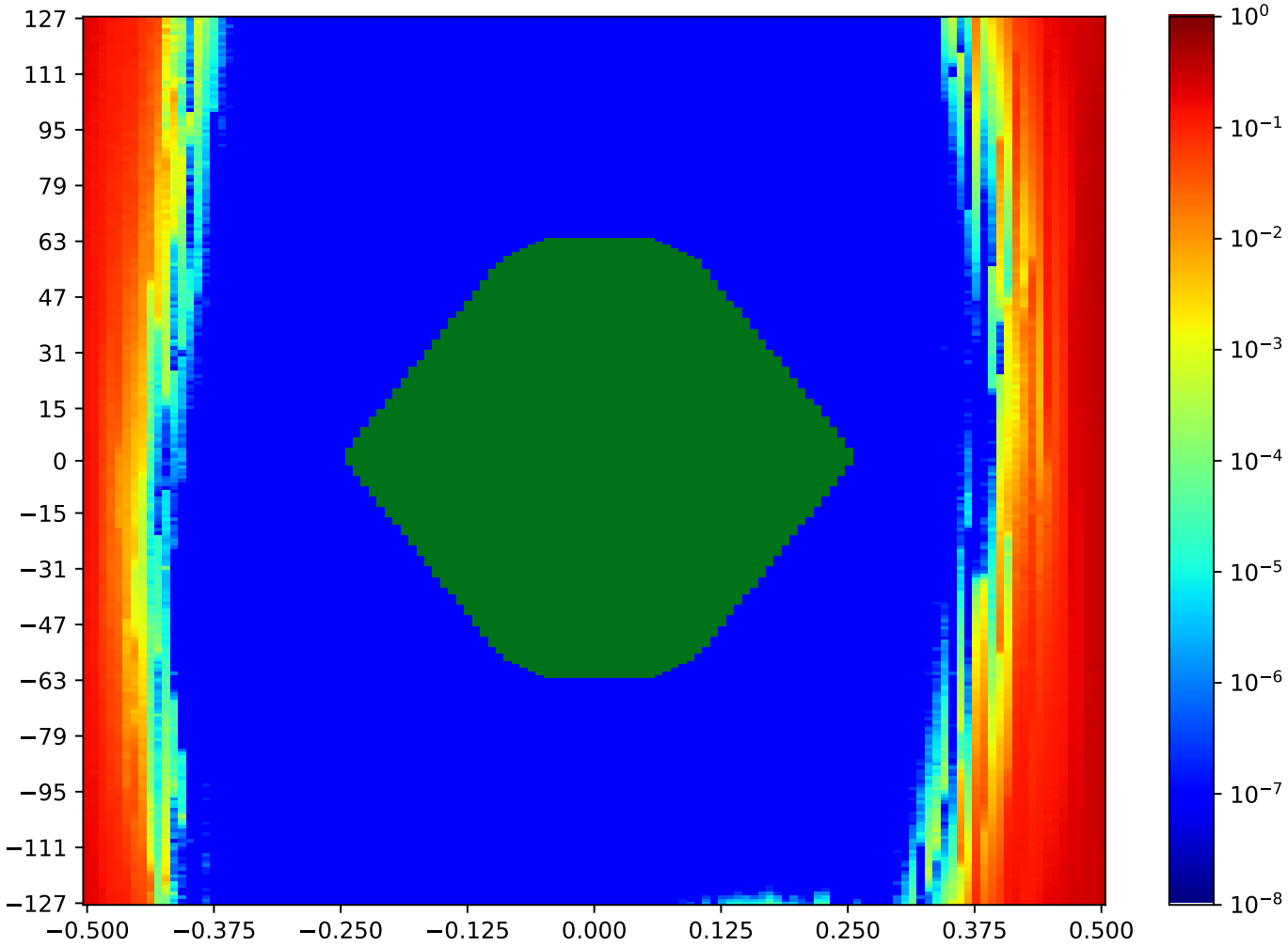


Figure 5.268: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.3 MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Table 5.248: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:39:53		2019-Nov-26 16:41:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24167	99	76.74%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

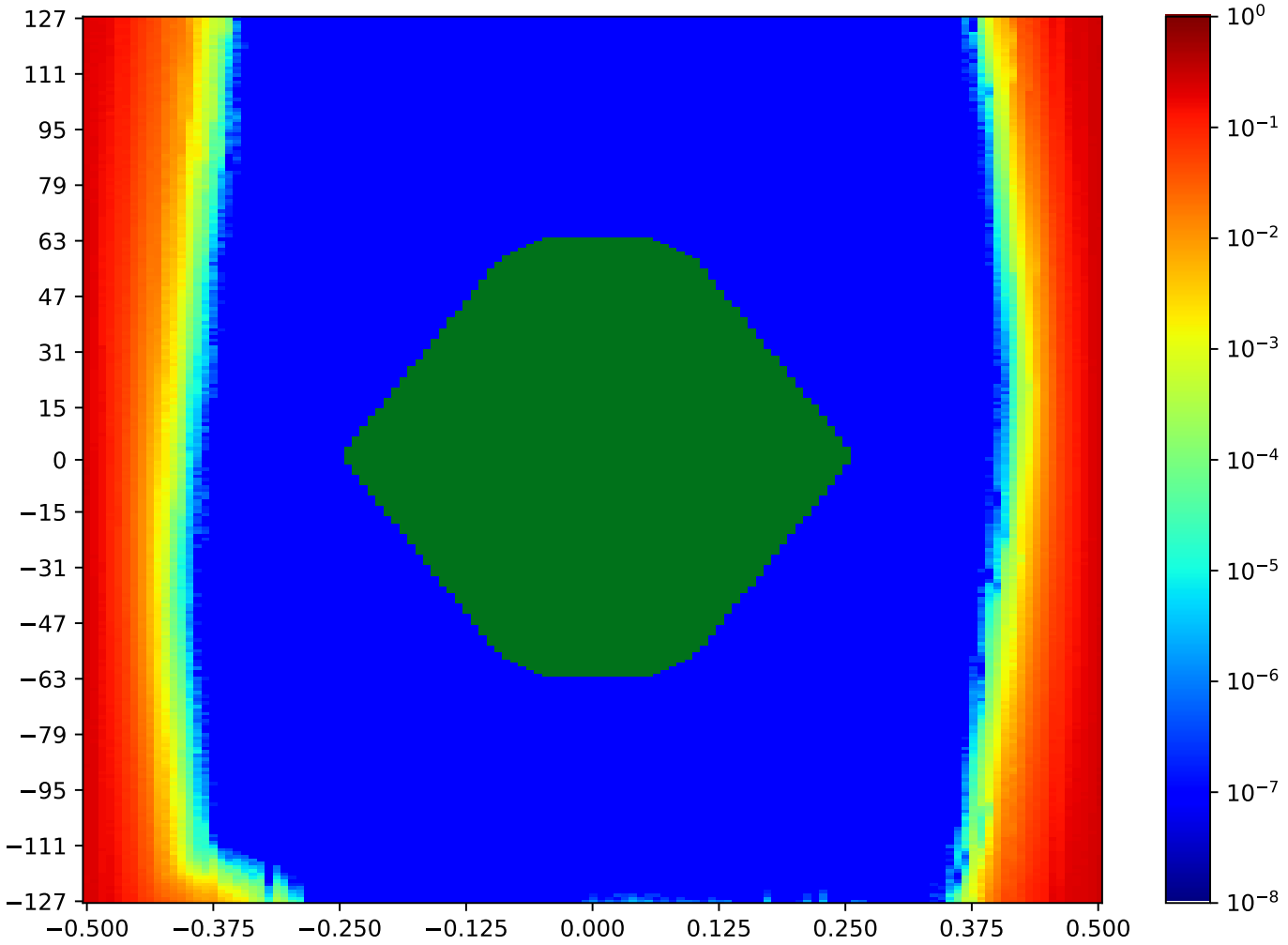


Figure 5.269: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.4 MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Table 5.249: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:33:48		2019-Nov-26 16:34:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24181	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

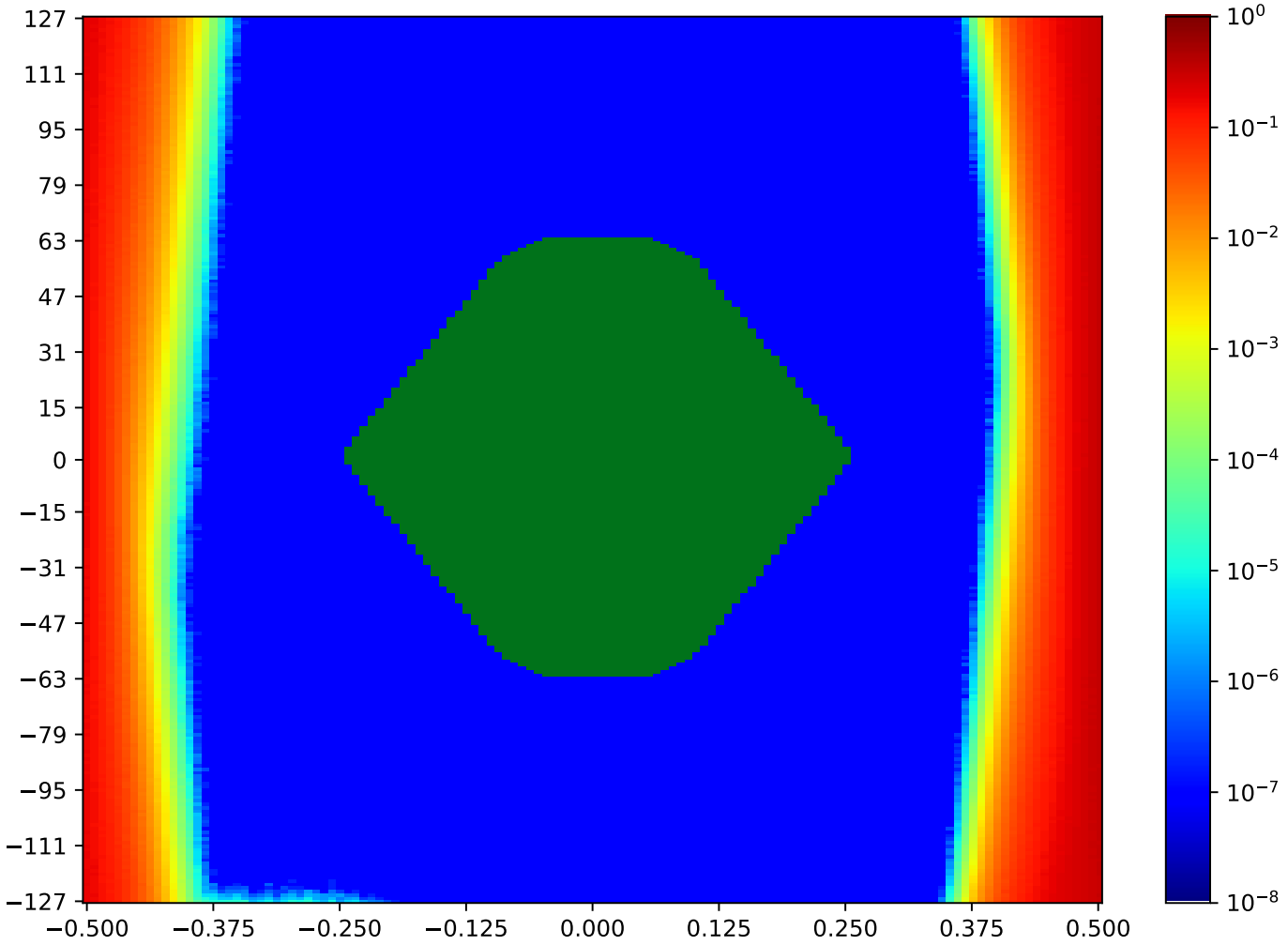


Figure 5.270: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.5 MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Table 5.250: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:43:33		2019-Nov-26 16:44:41	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24515	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

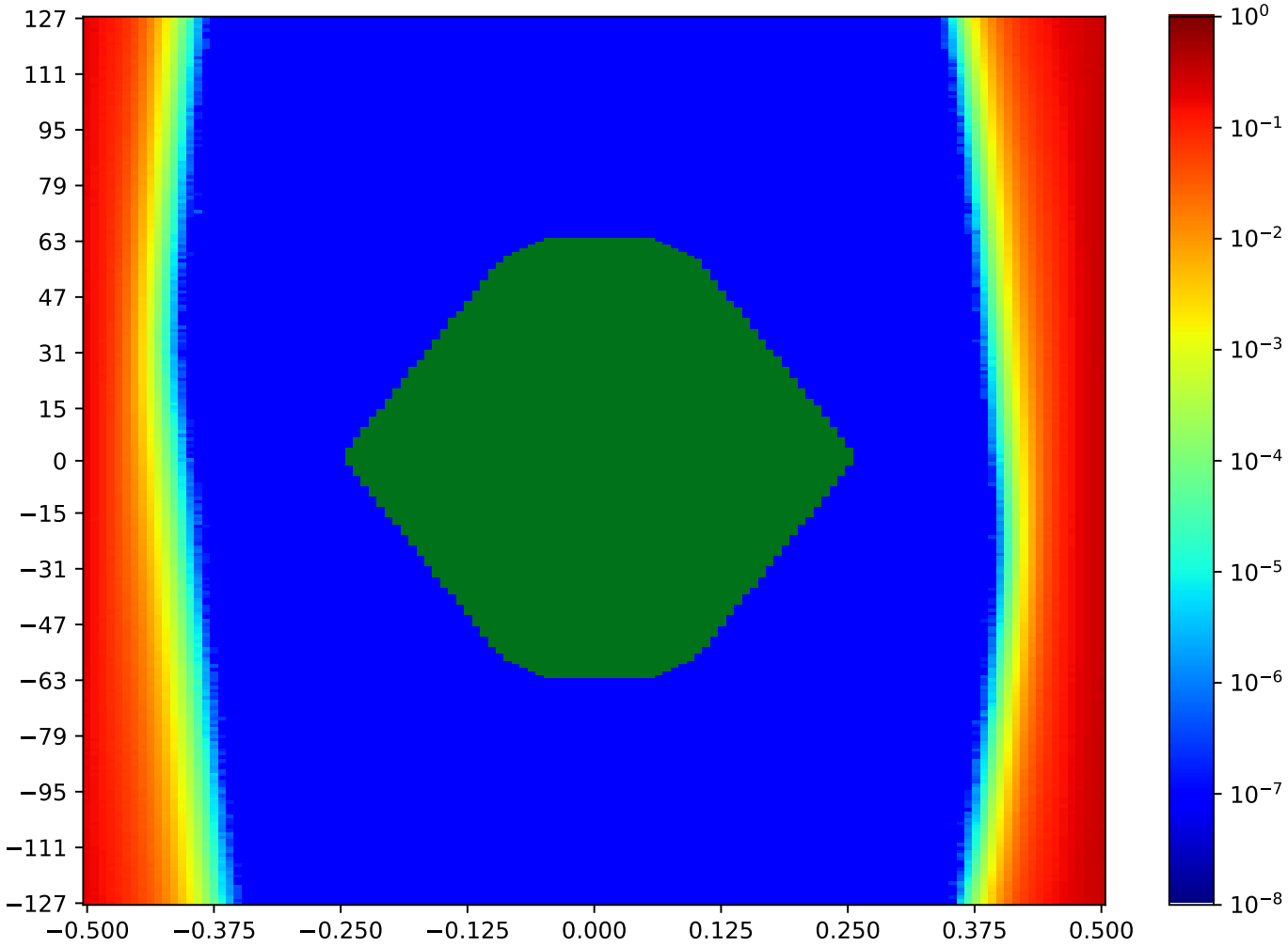


Figure 5.271: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.6 MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Table 5.251: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:32:39		2019-Nov-26 16:33:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24646	102	79.07%	249	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

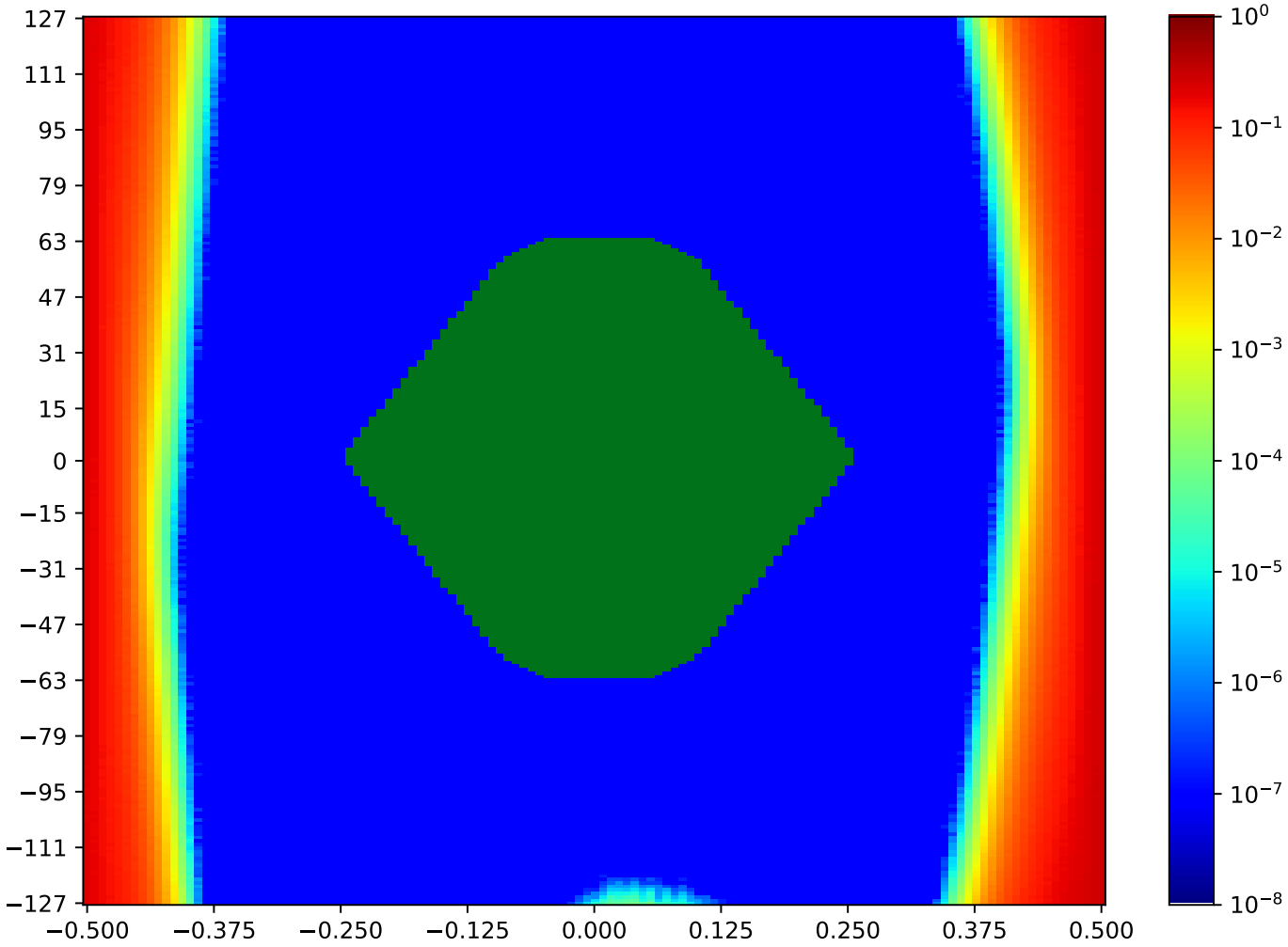


Figure 5.272: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.7 MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Table 5.252: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:45:49		2019-Nov-26 16:46:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24252	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

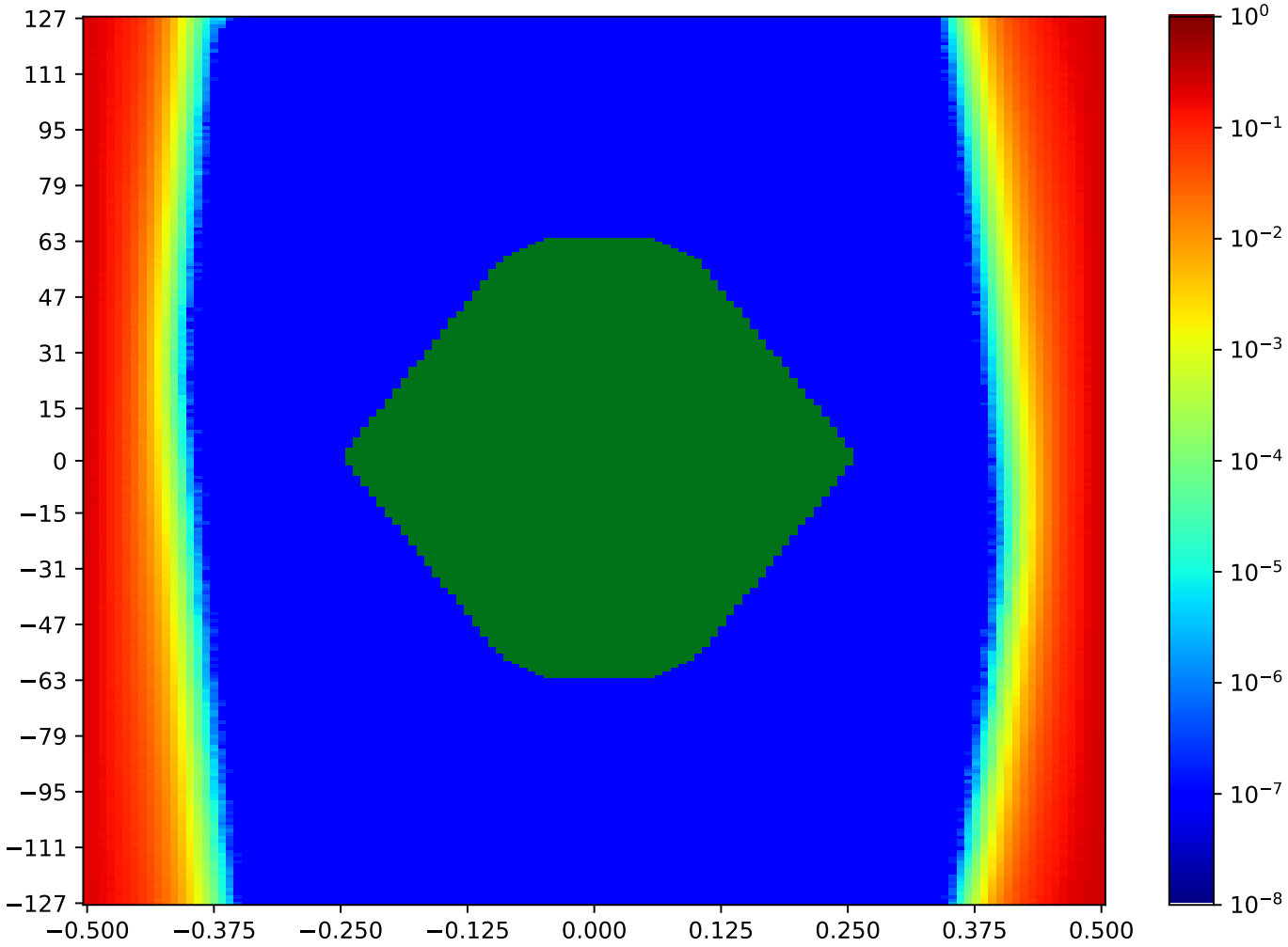


Figure 5.273: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.8 MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Table 5.253: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:34:56		2019-Nov-26 16:36:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24405	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

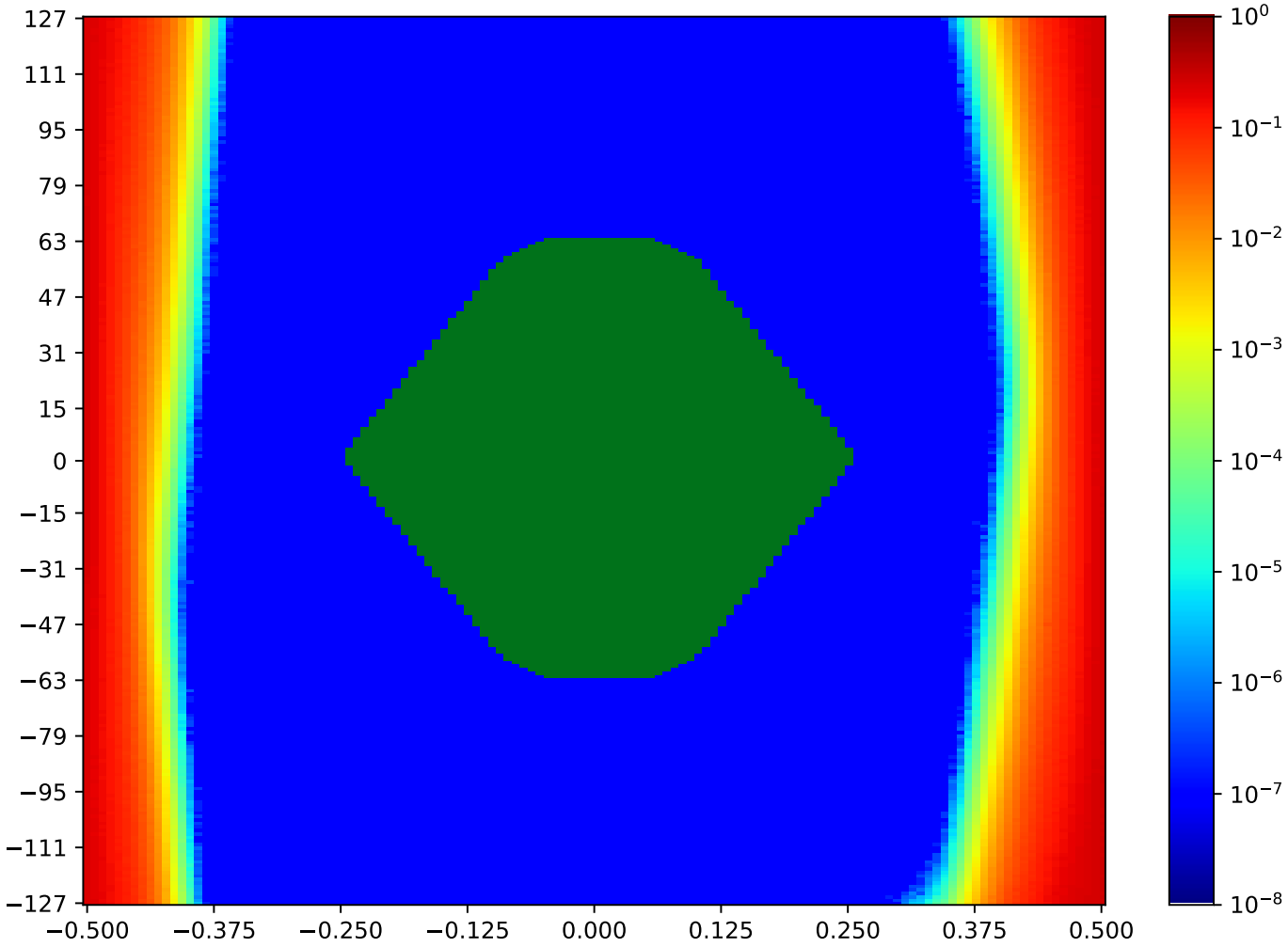


Figure 5.274: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.9 MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Table 5.254: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:44:41		2019-Nov-26 16:45:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23829	98	75.97%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

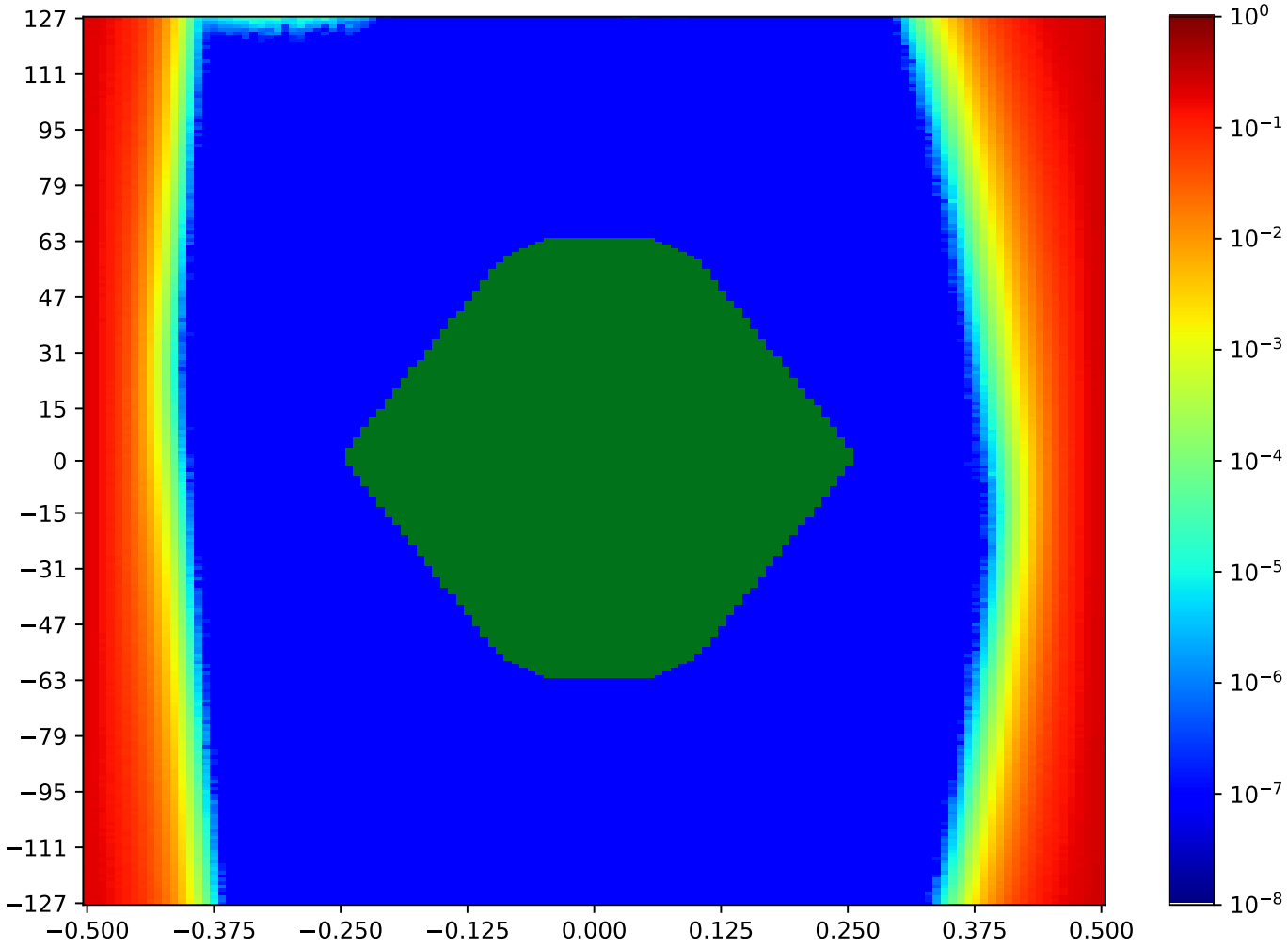


Figure 5.275: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.10 MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Table 5.255: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:37:27		2019-Nov-26 16:38:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24260	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

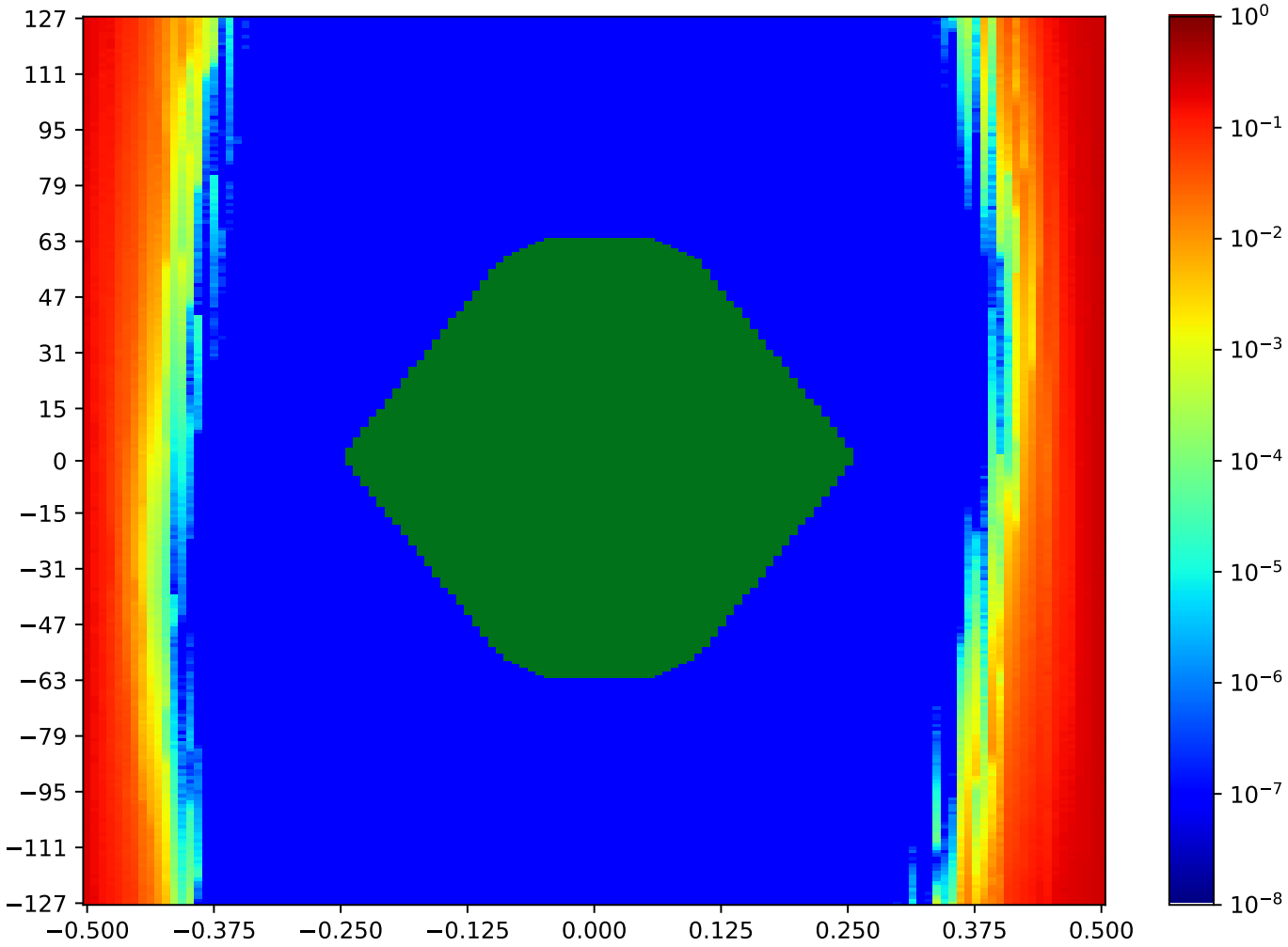


Figure 5.276: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.11 MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Table 5.256: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:42:26		2019-Nov-26 16:43:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24087	99	76.74%	255	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

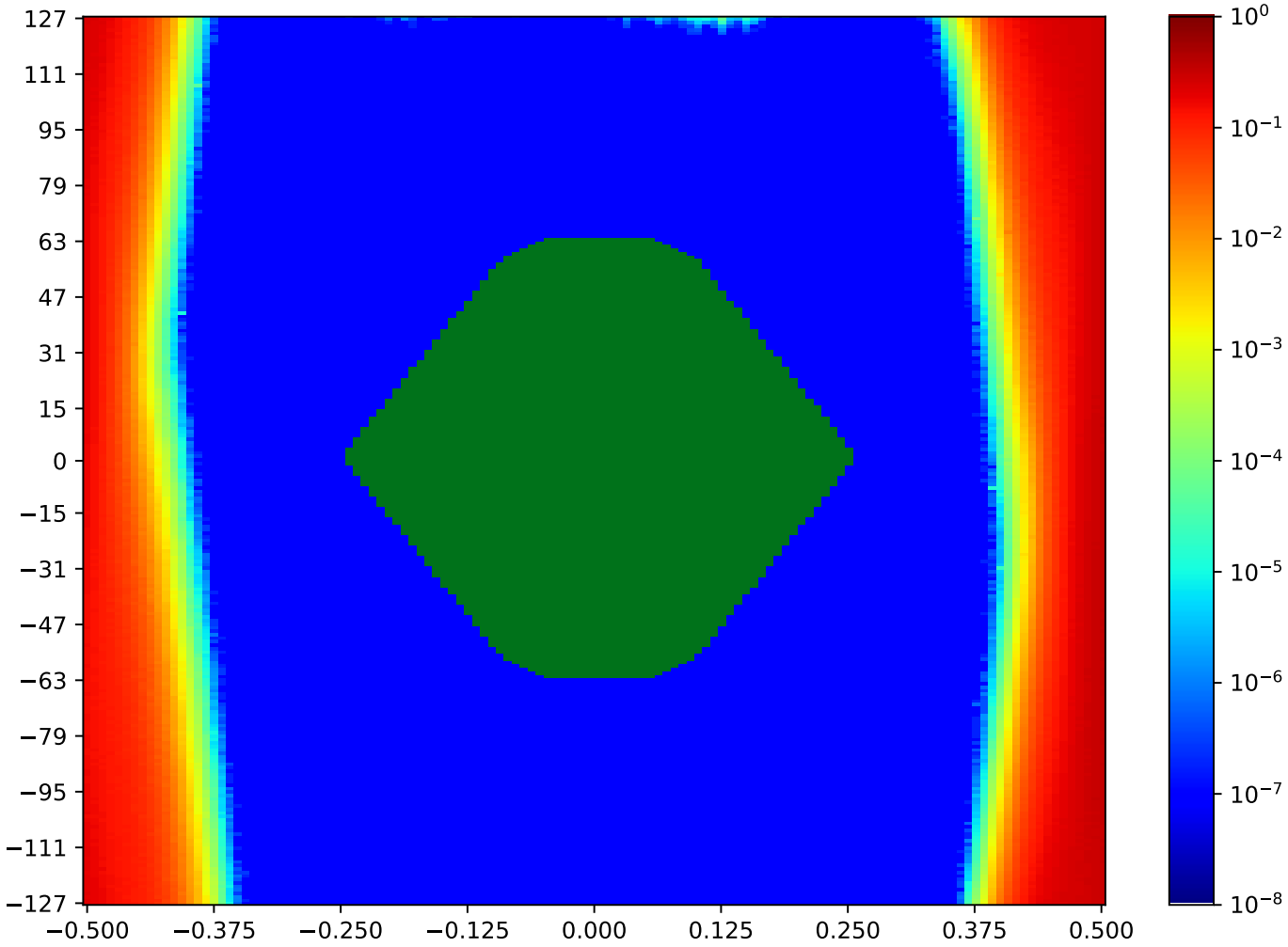


Figure 5.277: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.21.12 MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Table 5.257: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:41:18		2019-Nov-26 16:42:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24826	104	79.84%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

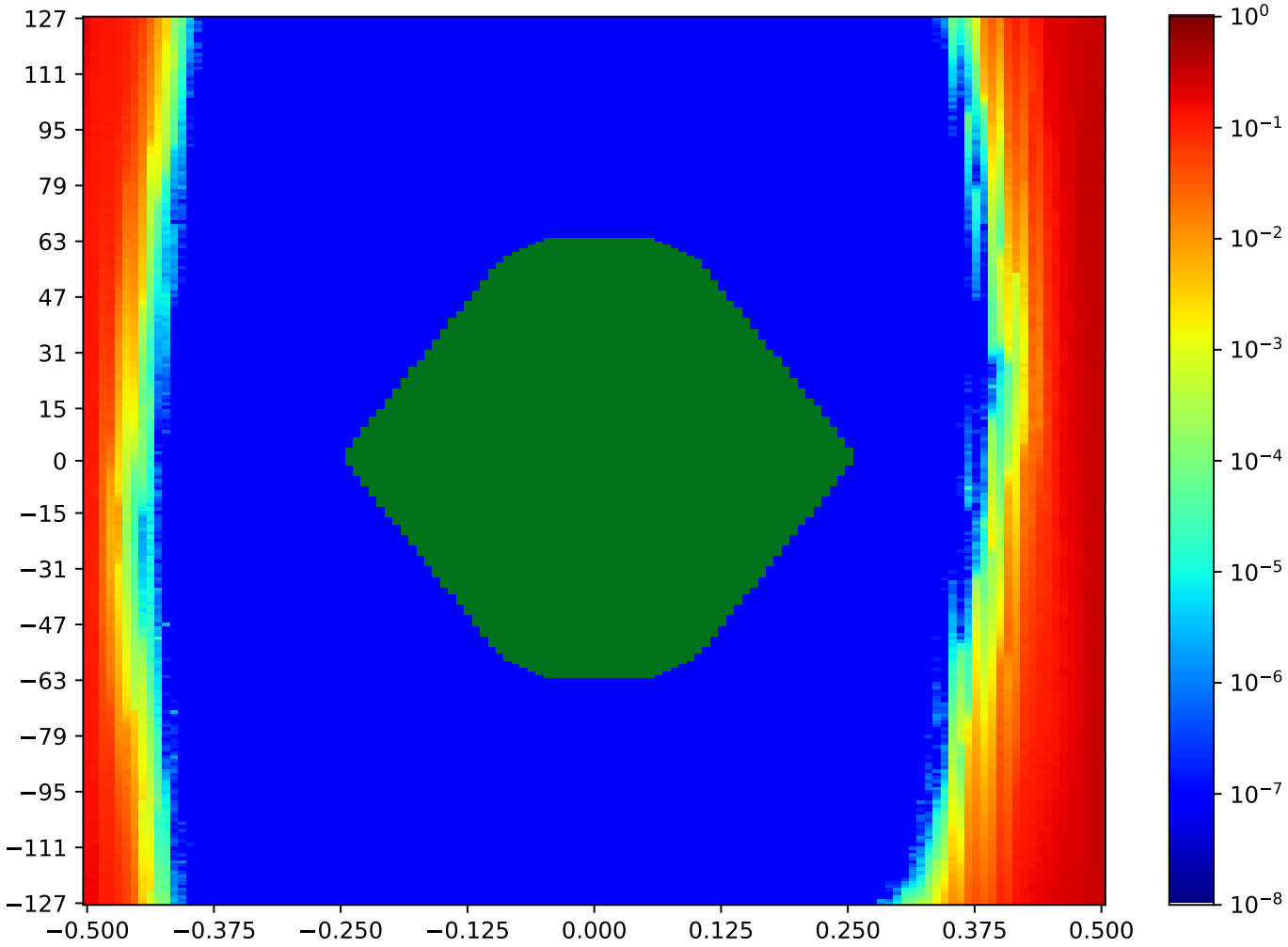


Figure 5.278: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22 MSP_C TX4 MSP_A RX4 Minipod Loopback

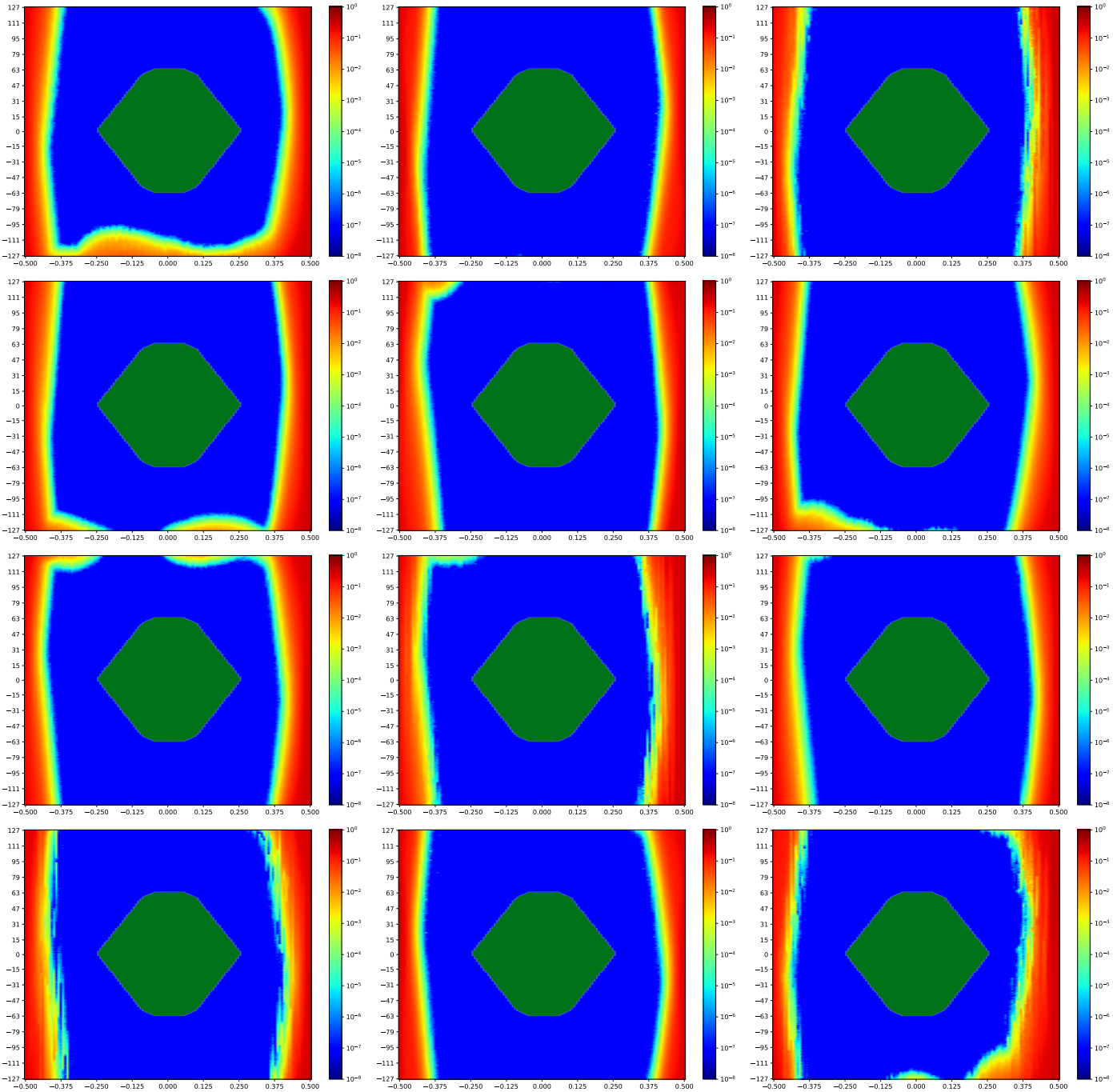


Figure 5.279: MSP_C TX4 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.
Next summary Figure 6.1.

5.22.1 MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Table 5.258: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:50:37		2019-Nov-26 16:51:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	22132	100	77.52%	233	90.98%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

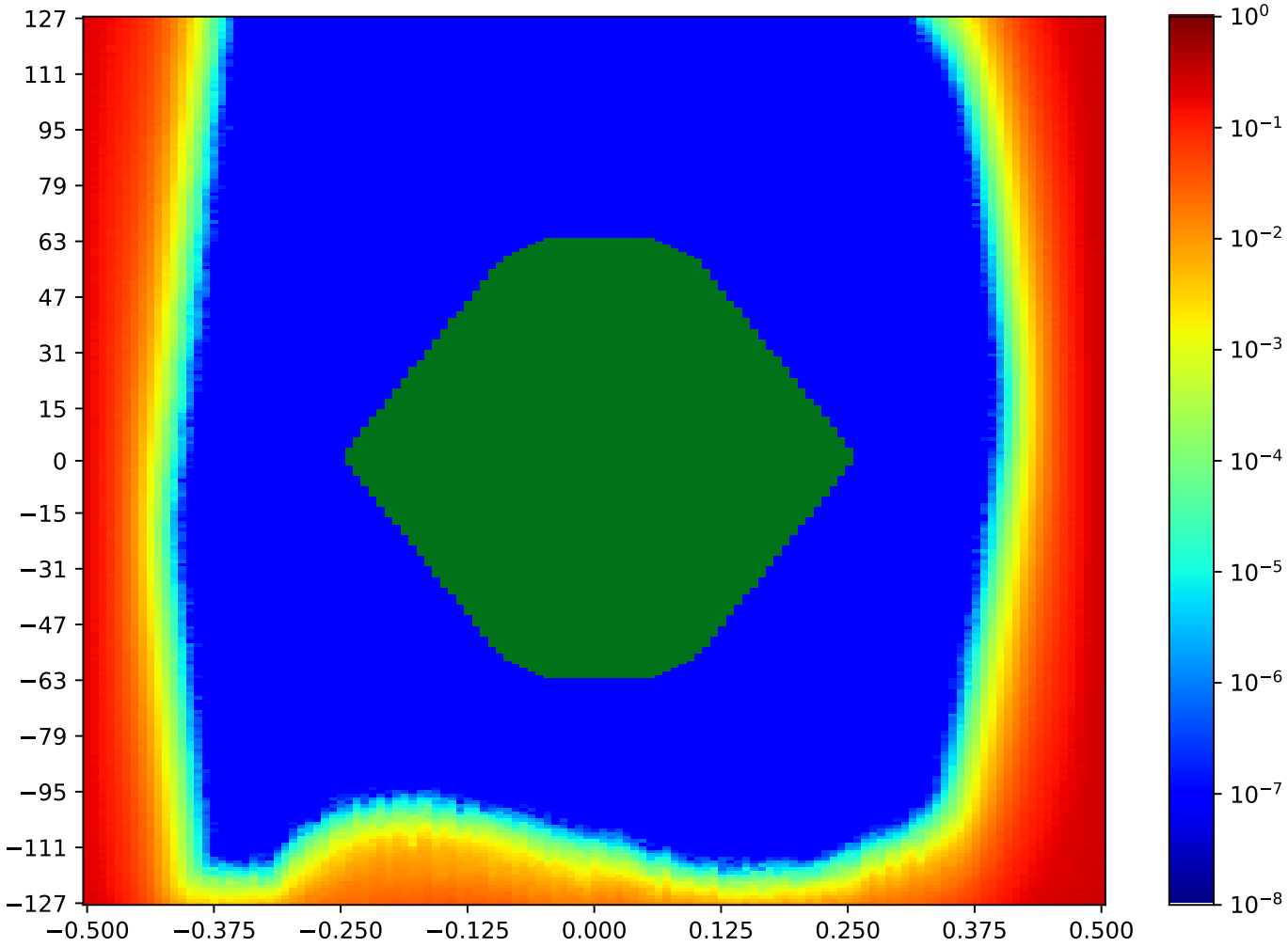


Figure 5.280: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.2 MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Table 5.259: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:48:21		2019-Nov-26 16:49:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24845	100	77.52%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

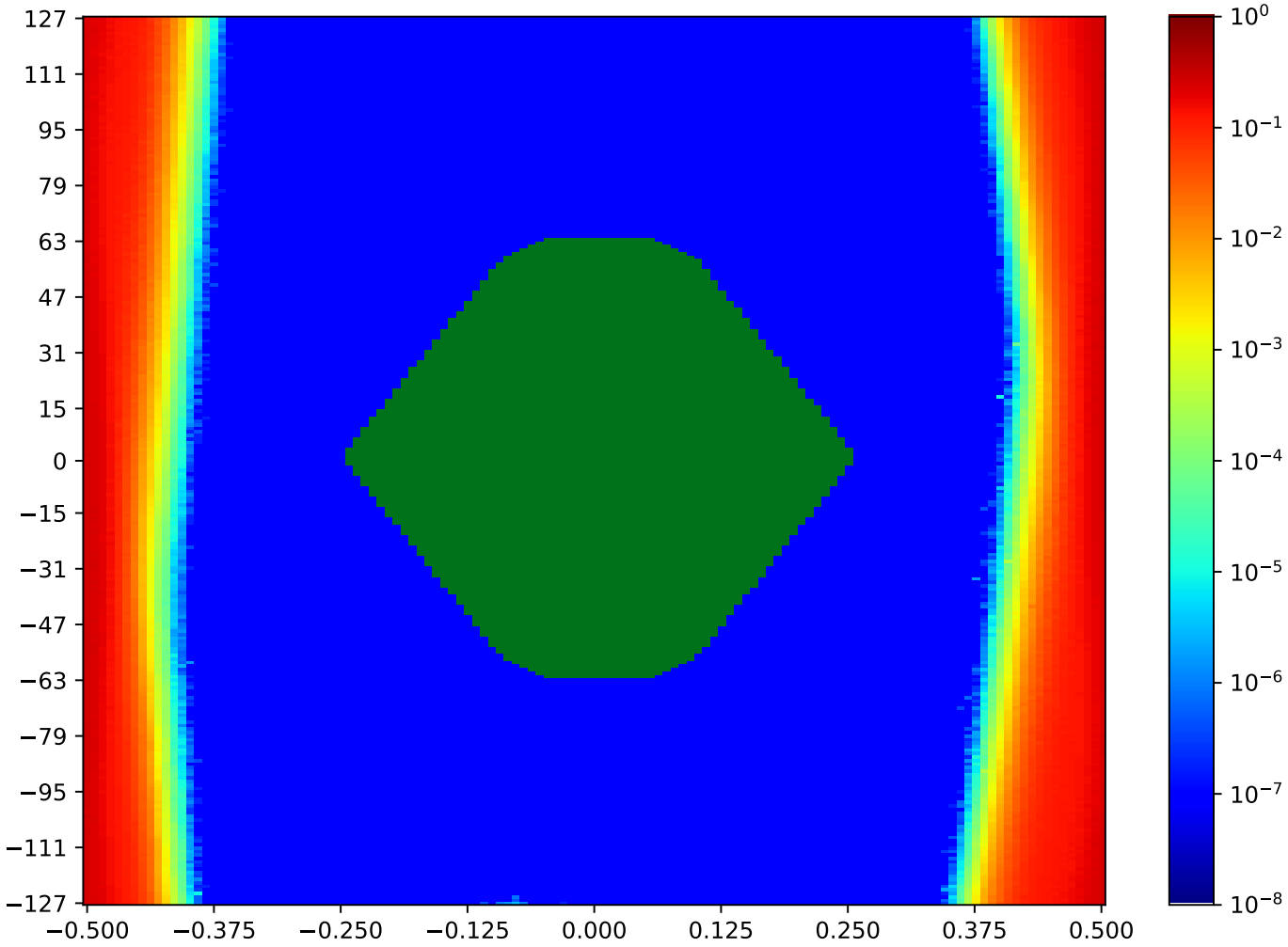


Figure 5.281: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.3 MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Table 5.260: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:54:02		2019-Nov-26 16:55:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24534	99	76.74%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

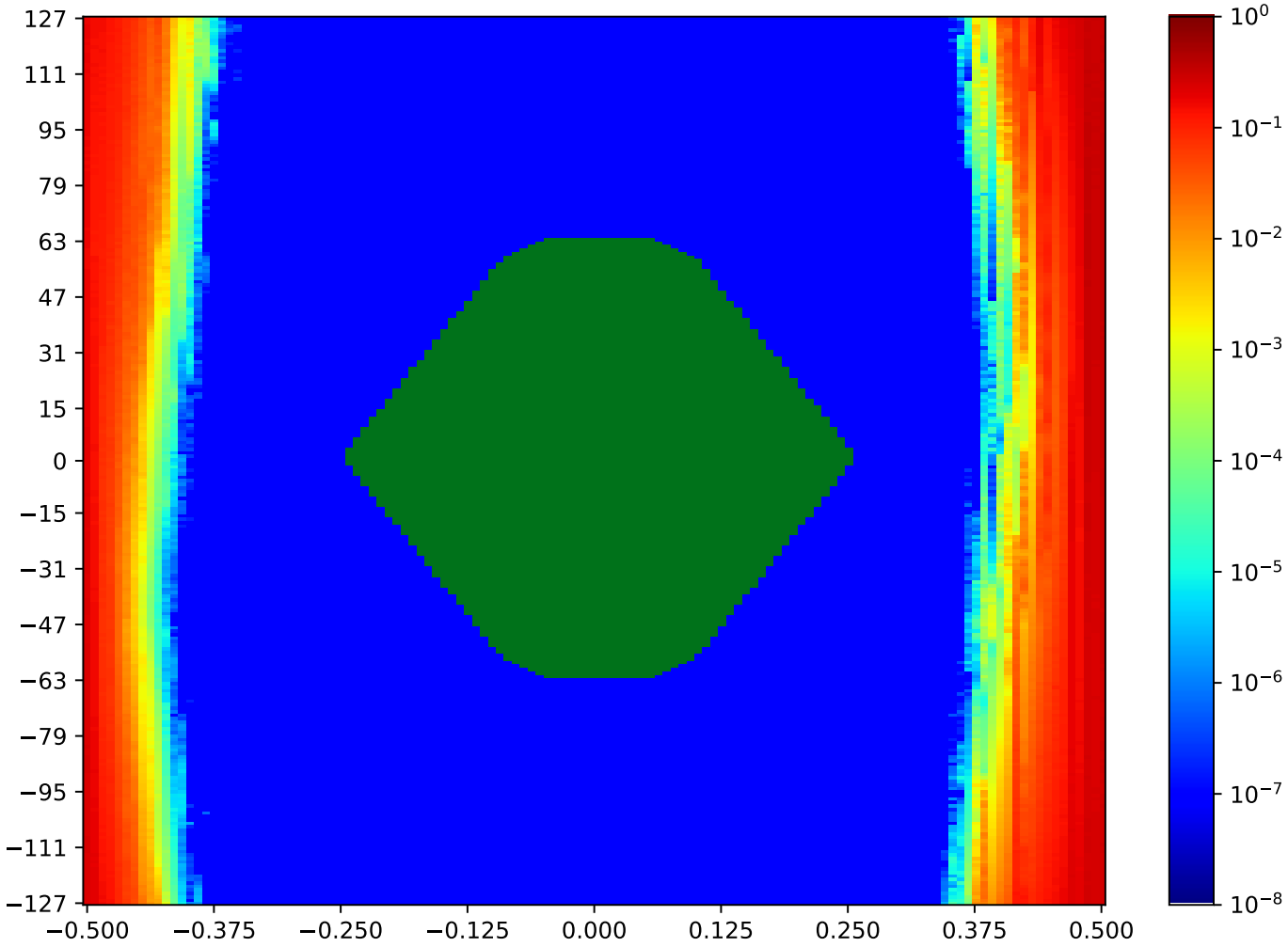


Figure 5.282: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.4 MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Table 5.261: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:46:57		2019-Nov-26 16:48:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23578	100	77.52%	247	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

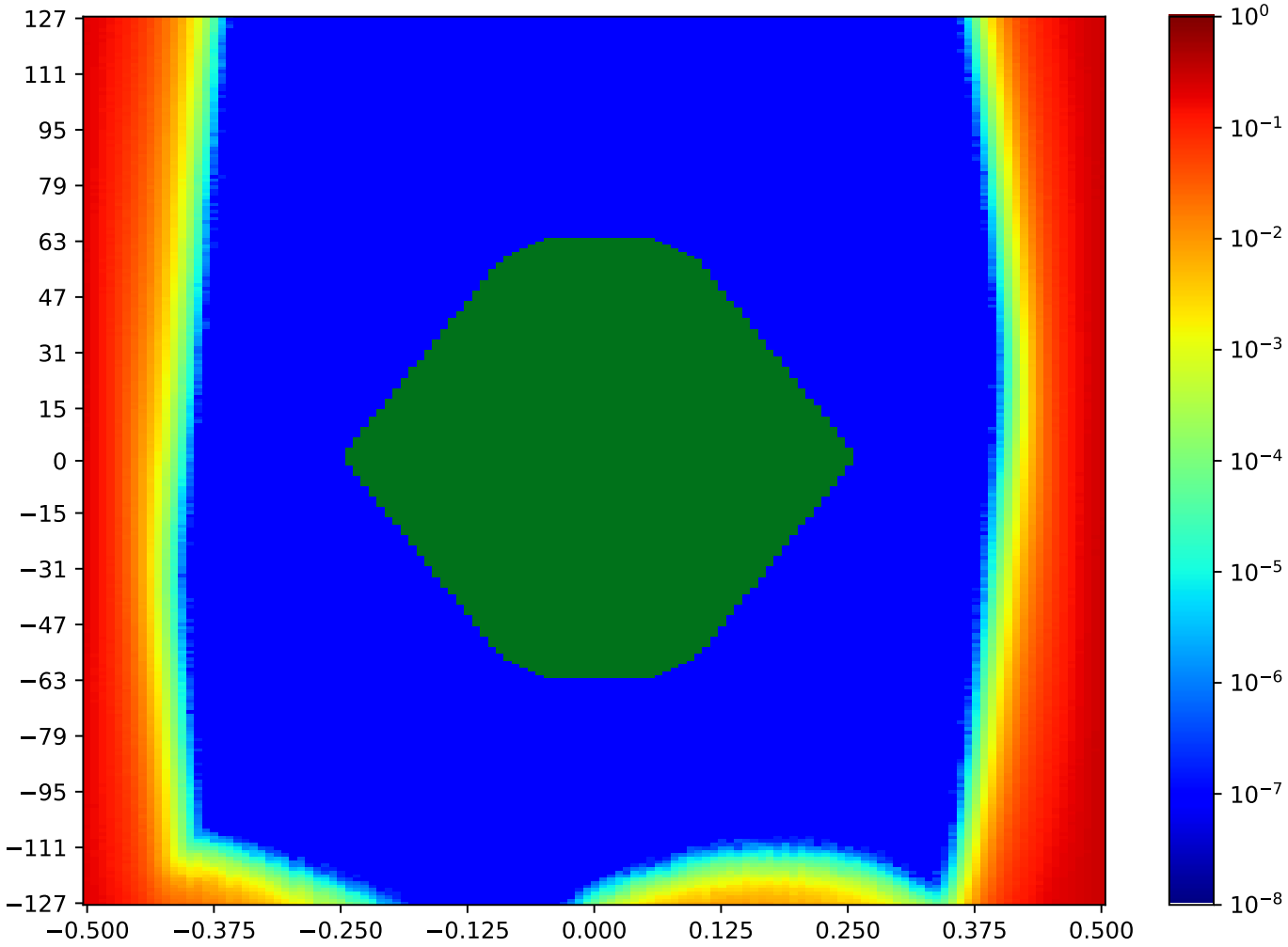


Figure 5.283: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.5 MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Table 5.262: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:57:37		2019-Nov-26 16:58:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24134	98	75.97%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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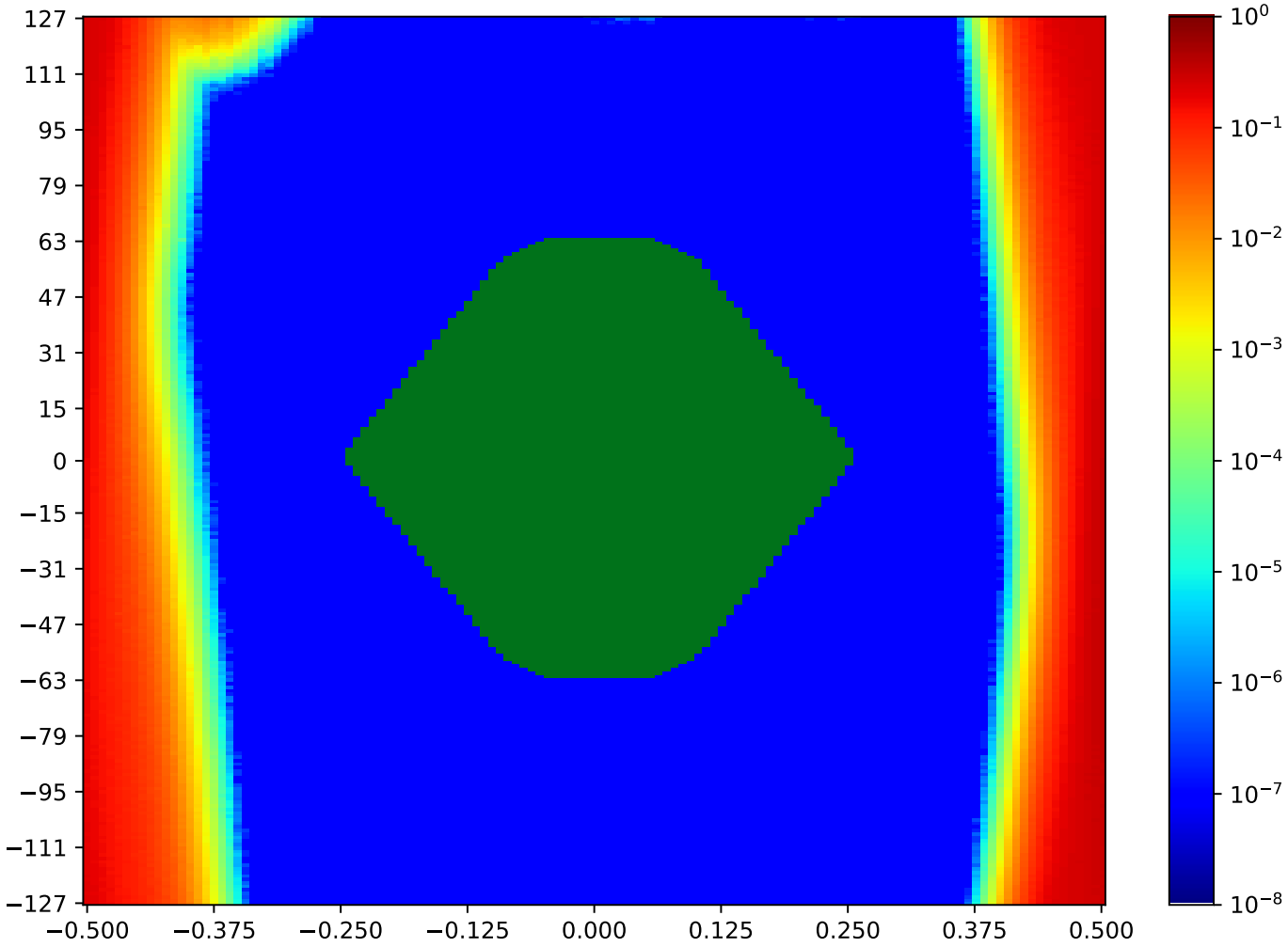


Figure 5.284: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.6 MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Table 5.263: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:49:29		2019-Nov-26 16:50:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23410	99	76.74%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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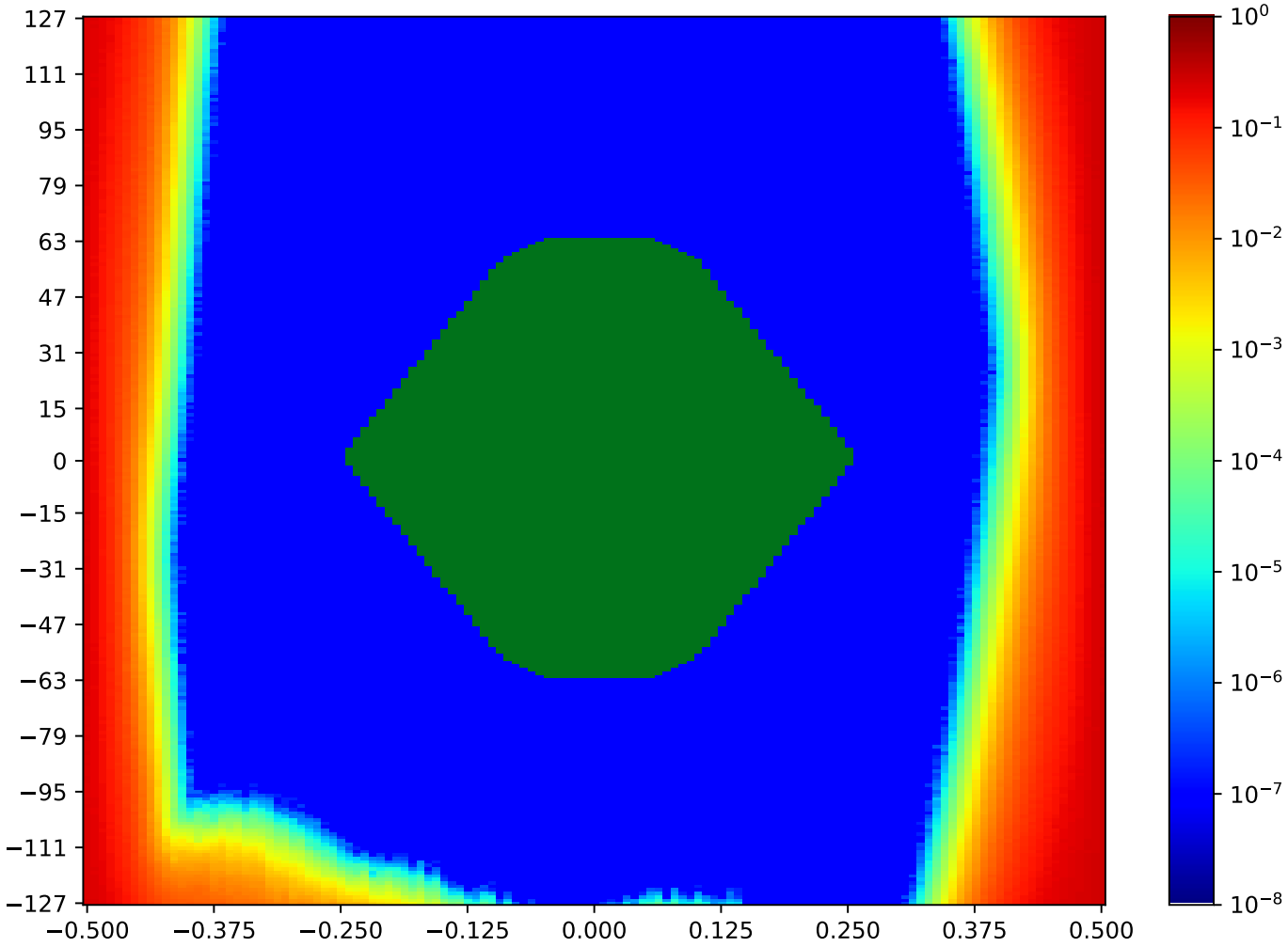


Figure 5.285: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.7 MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Table 5.264: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:59:53		2019-Nov-26 17:01:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23641	100	77.52%	247	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

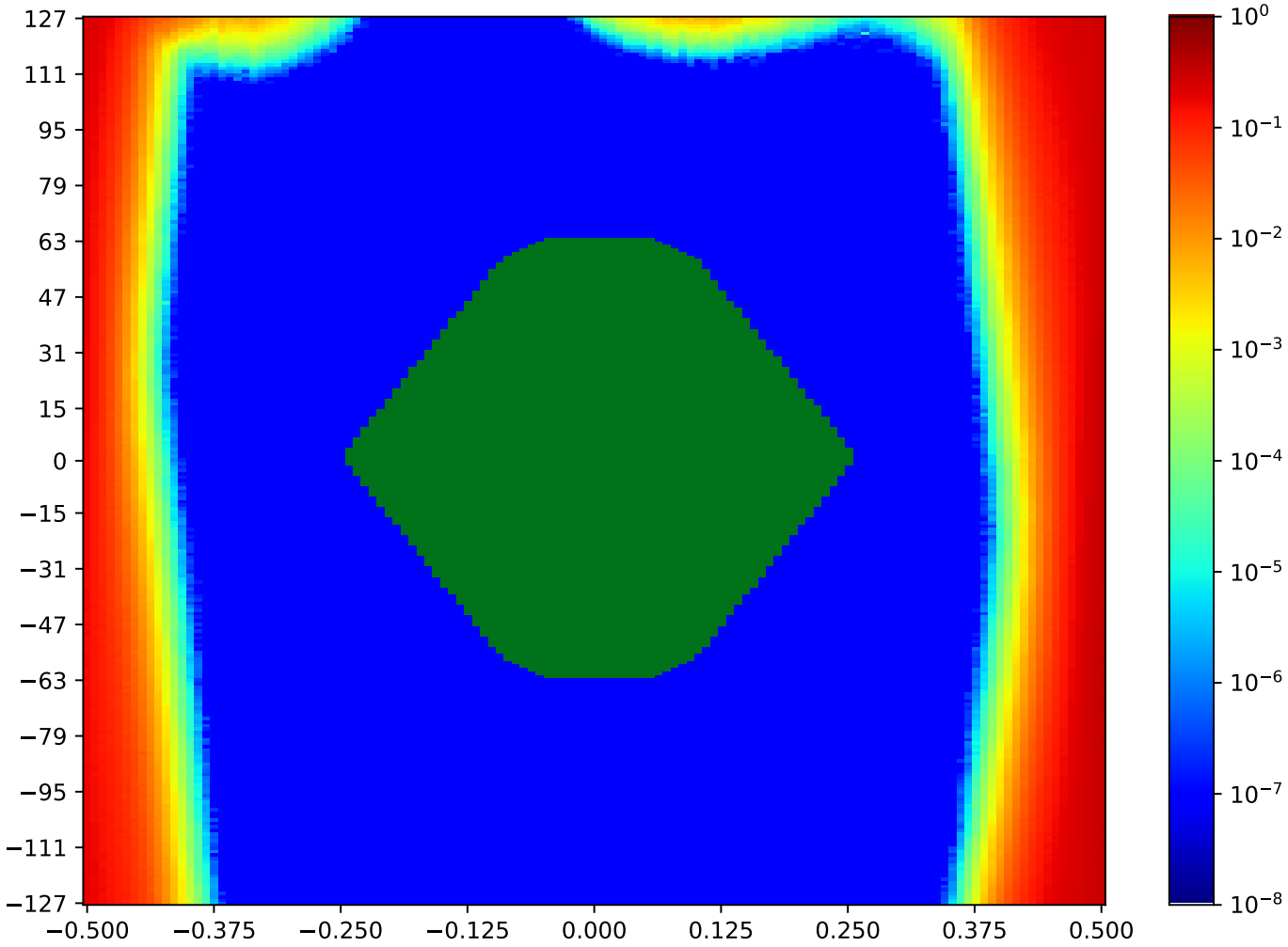


Figure 5.286: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.8 MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Table 5.265: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:51:45		2019-Nov-26 16:52:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23637	97	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

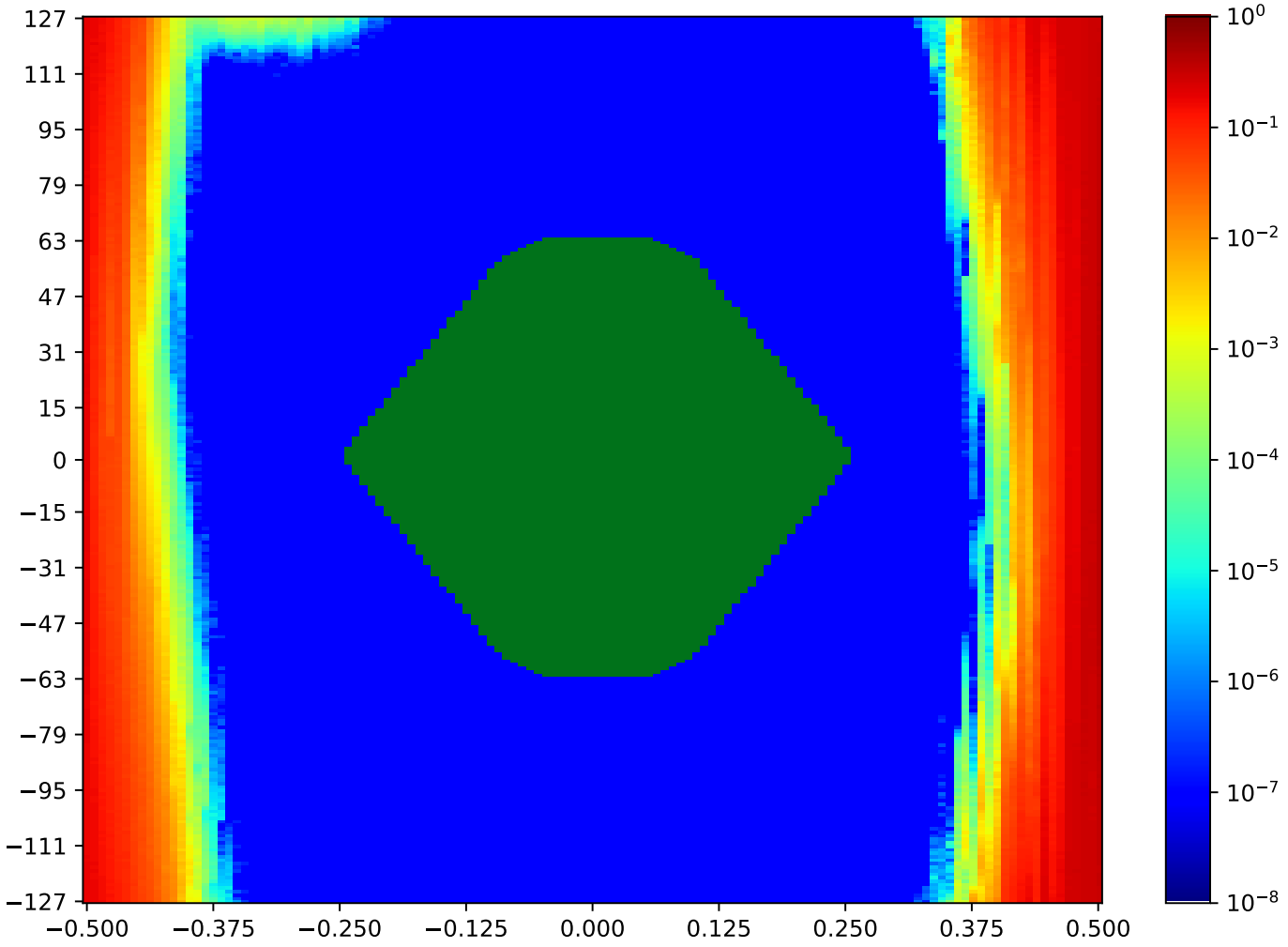


Figure 5.287: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.9 MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Table 5.266: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:58:45		2019-Nov-26 16:59:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24158	100	77.52%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

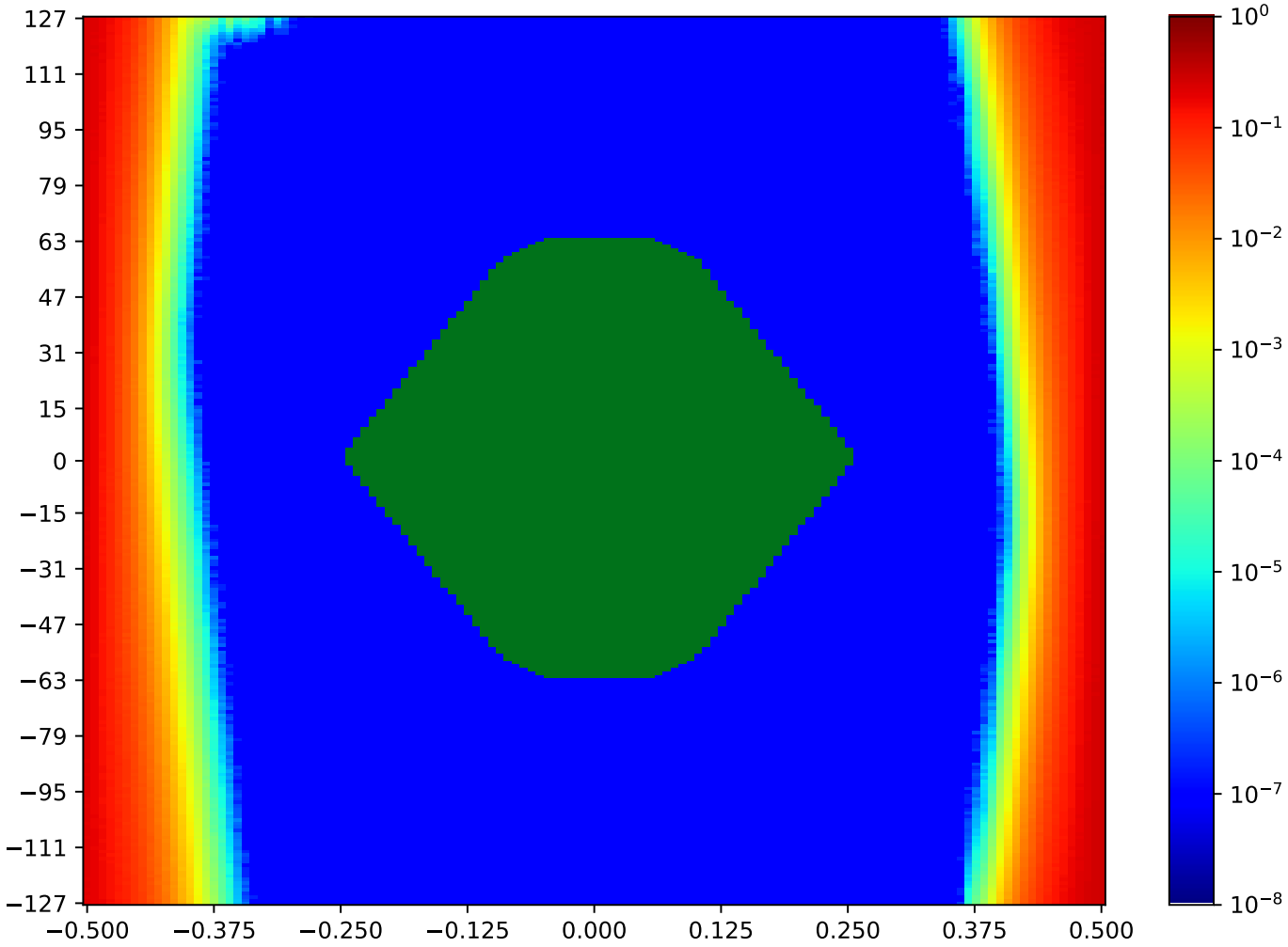


Figure 5.288: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.10 MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Table 5.267: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:52:54		2019-Nov-26 16:54:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23882	98	75.19%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

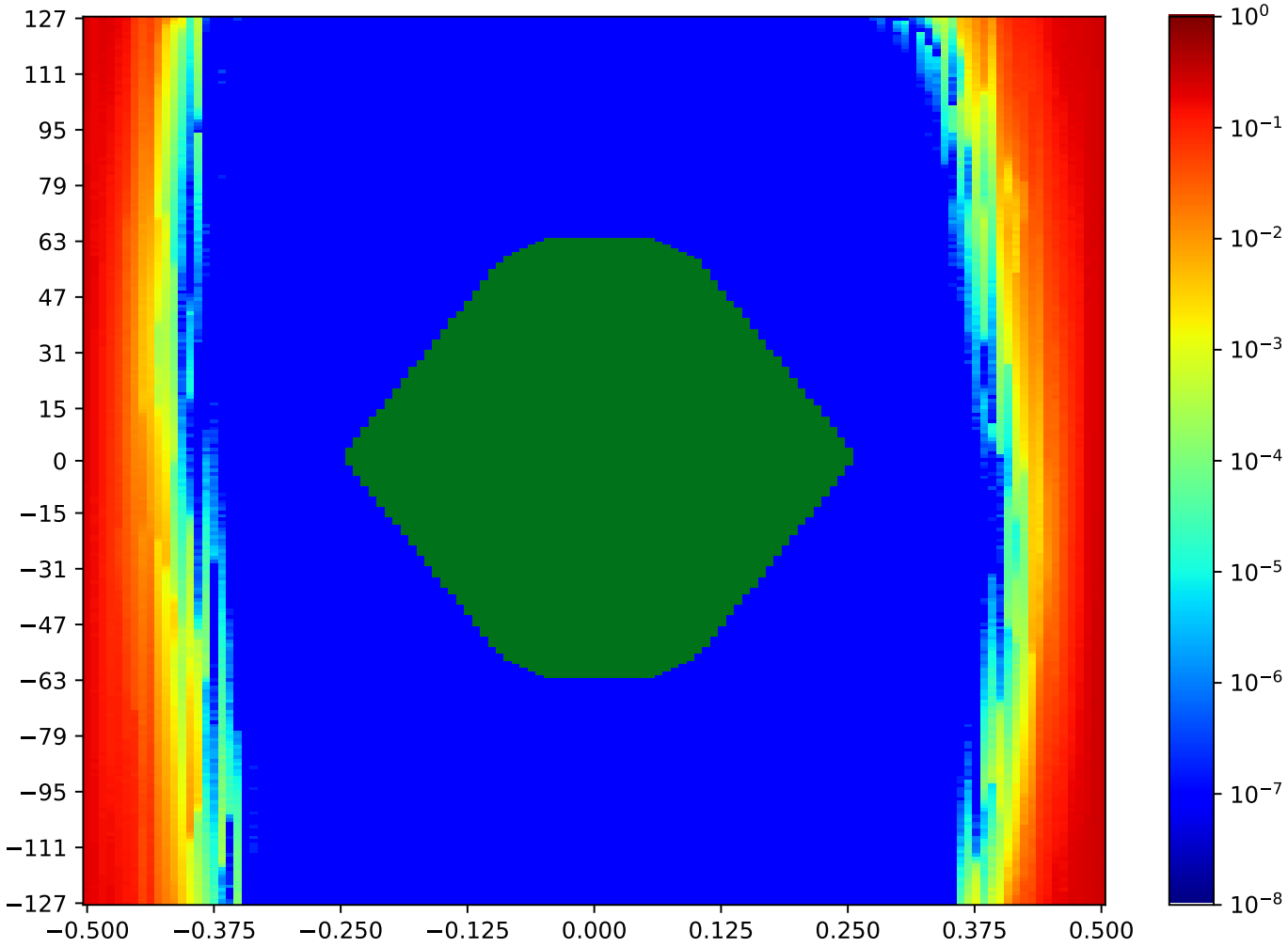


Figure 5.289: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.11 MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Table 5.268: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:56:29		2019-Nov-26 16:57:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	24940	102	79.07%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

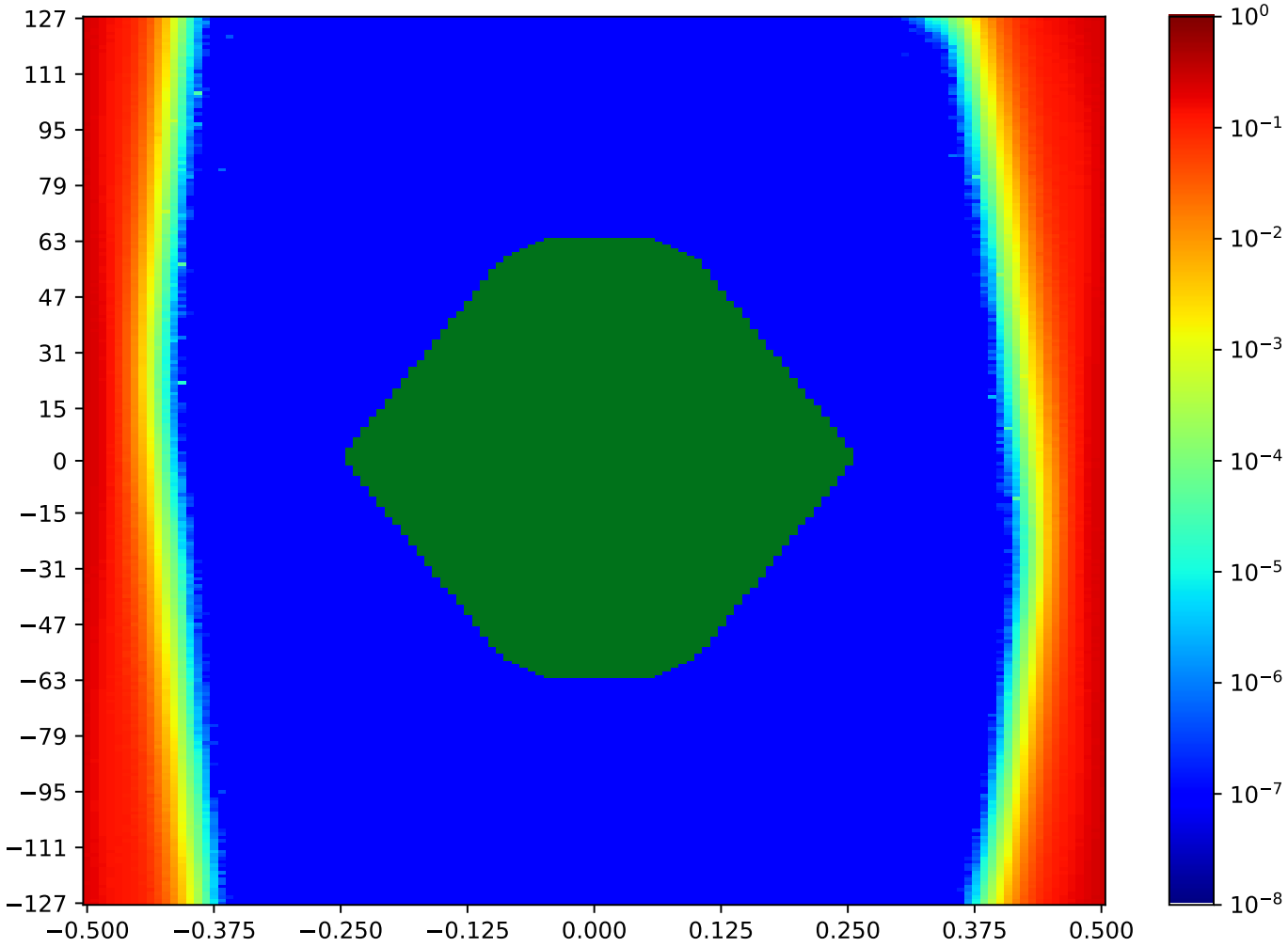


Figure 5.290: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

5.22.12 MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Table 5.269: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 16:55:10		2019-Nov-26 16:56:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	23083	98	75.97%	243	95.29%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

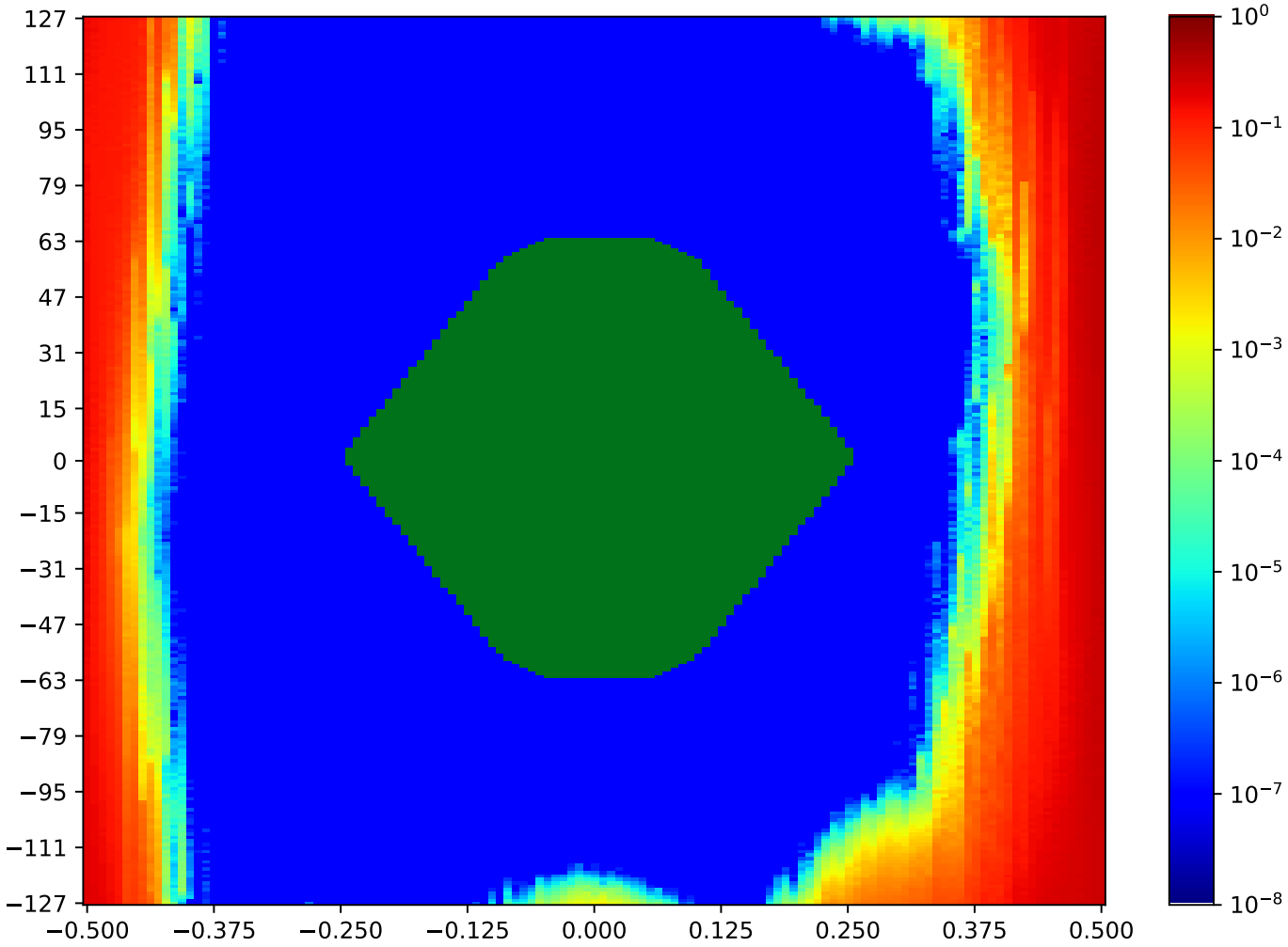


Figure 5.291: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-12.8.

Chapter 6

MUCTPI V3 12.8 Gbps

6.1 MSP_A TX1 MSP_C RX15 Minipod Loopback

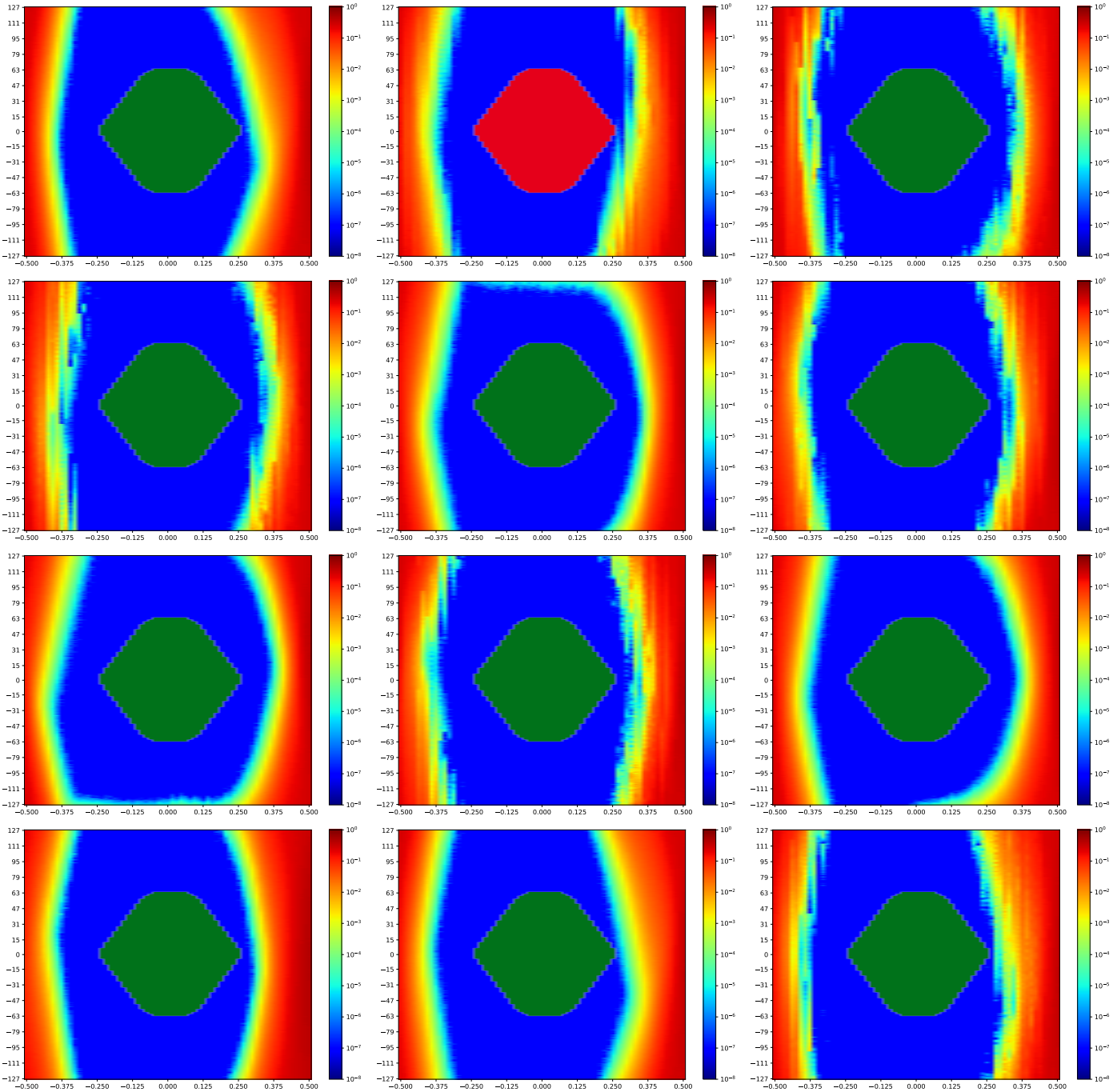


Figure 6.1: MSP_A TX1 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.14.

6.1.1 MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Table 6.1: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:19:34		2019-Nov-26 17:19:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9228	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

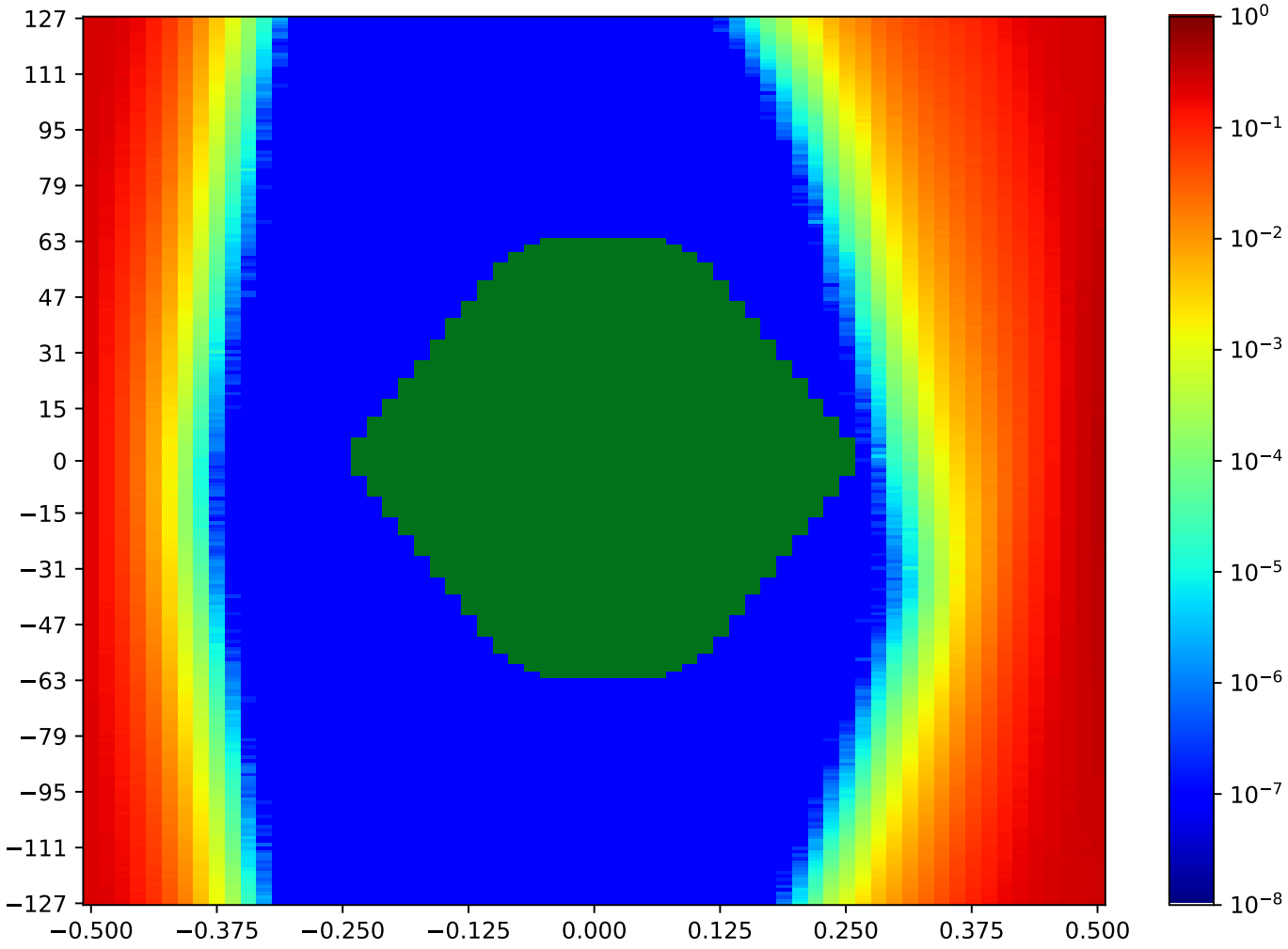


Figure 6.2: MSP_A_FPGA-TX1-00–RX15-00-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.2 MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Table 6.2: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:20:21		2019-Nov-26 17:20:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9099	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

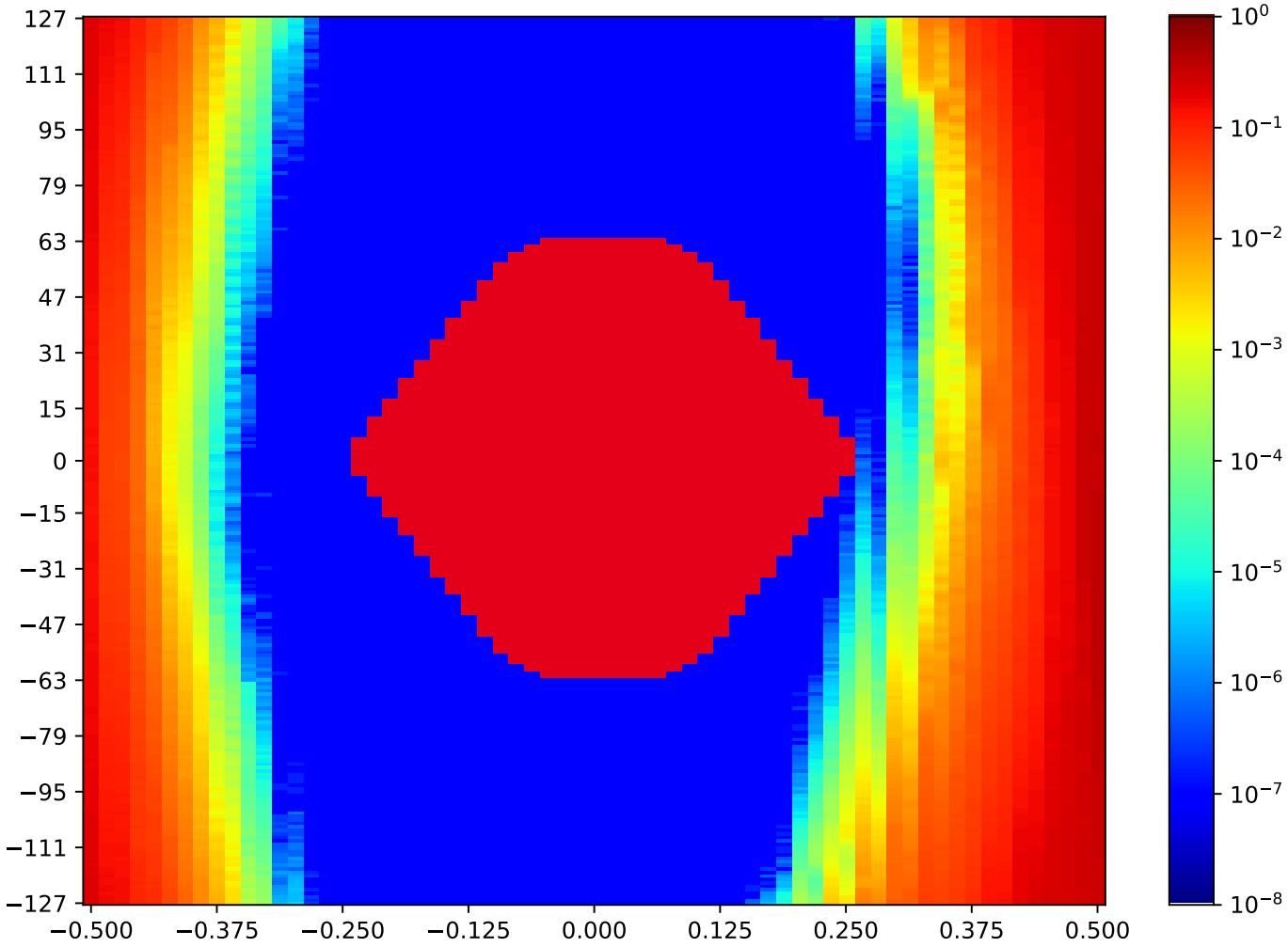


Figure 6.3: MSP_A_FPGA-TX1-01–RX15-01-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.3 MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Table 6.3: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:20:46		2019-Nov-26 17:21:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9397	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

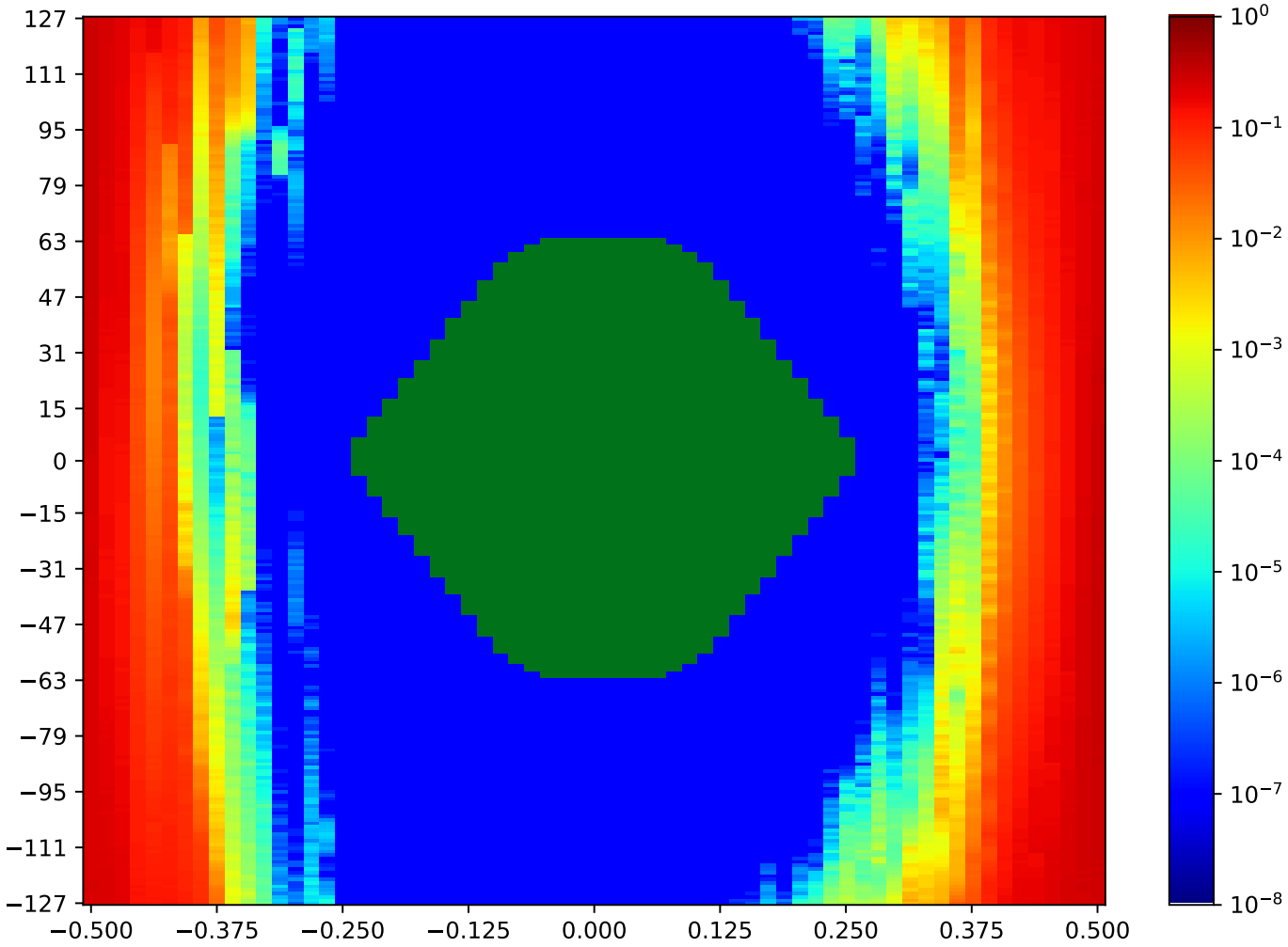


Figure 6.4: MSP_A_FPGA-TX1-02–RX15-02-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.4 MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Table 6.4: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:18:38		2019-Nov-26 17:19:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9677	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

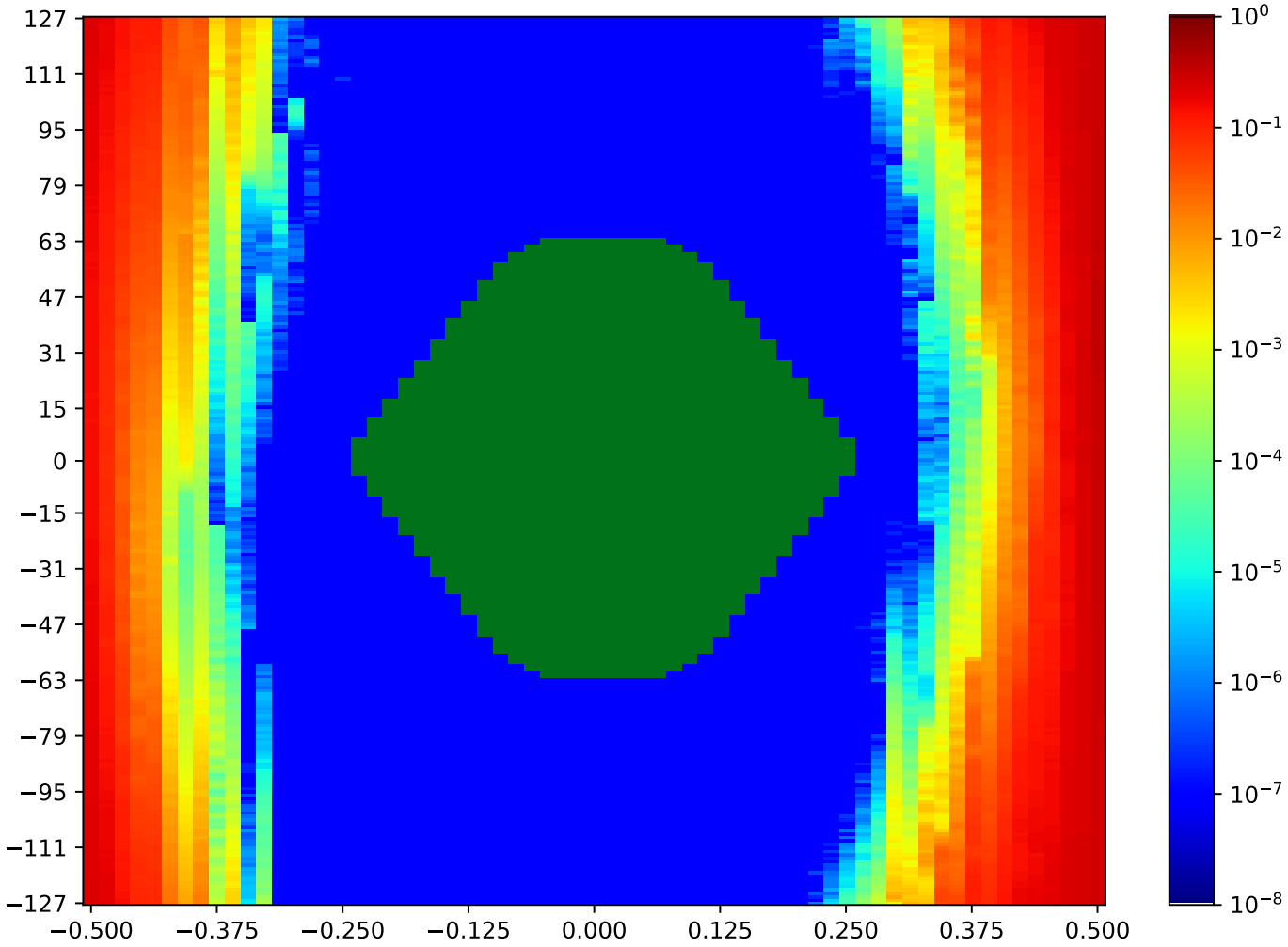


Figure 6.5: MSP_A_FPGA-TX1-03–RX15-03-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.5 MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Table 6.5: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:22:09		2019-Nov-26 17:22:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9124	43	66.15%	241	93.73%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

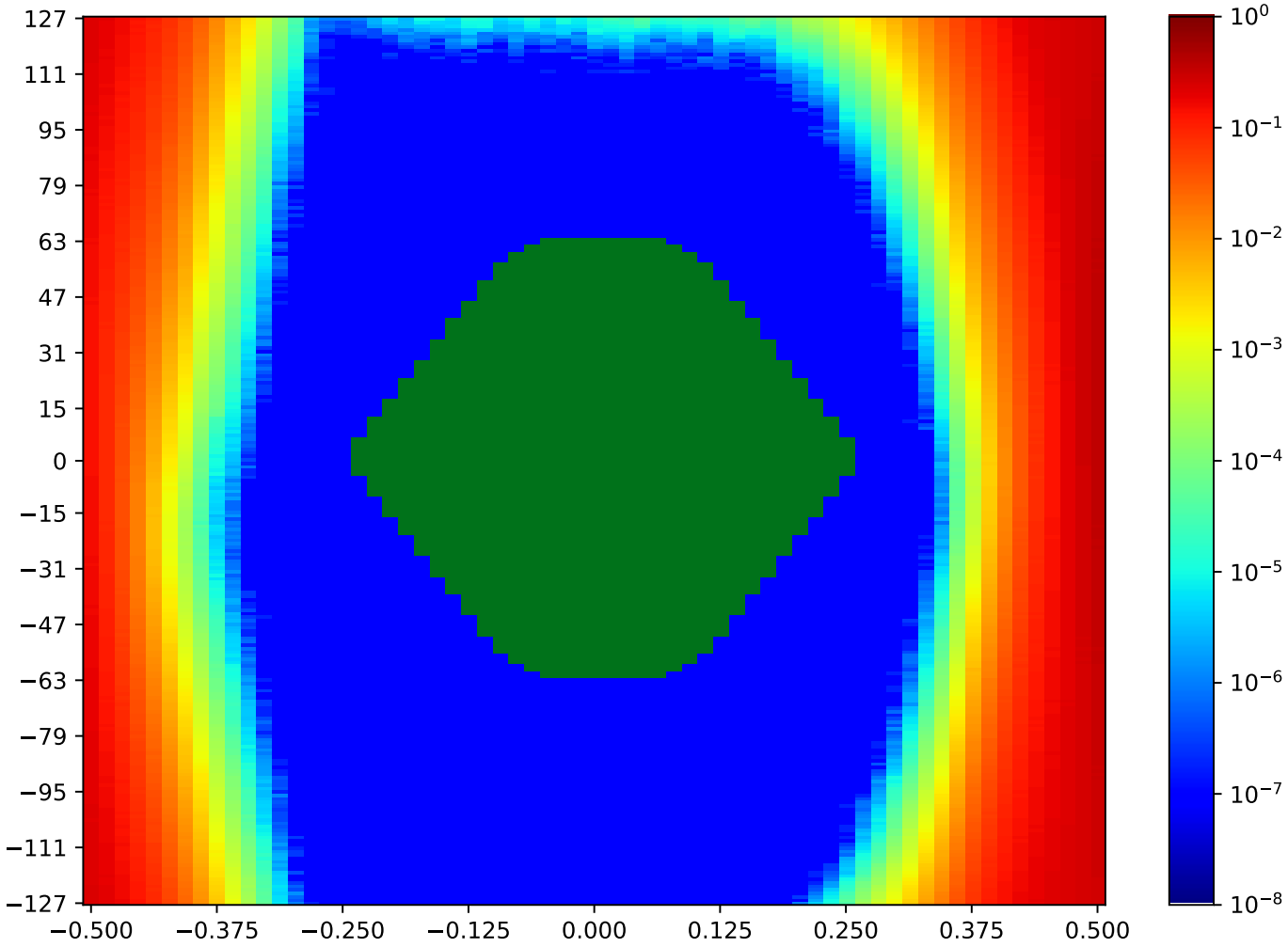


Figure 6.6: MSP_A_FPGA-TX1-04–RX15-04-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.6 MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Table 6.6: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:18:11		2019-Nov-26 17:18:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9672	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

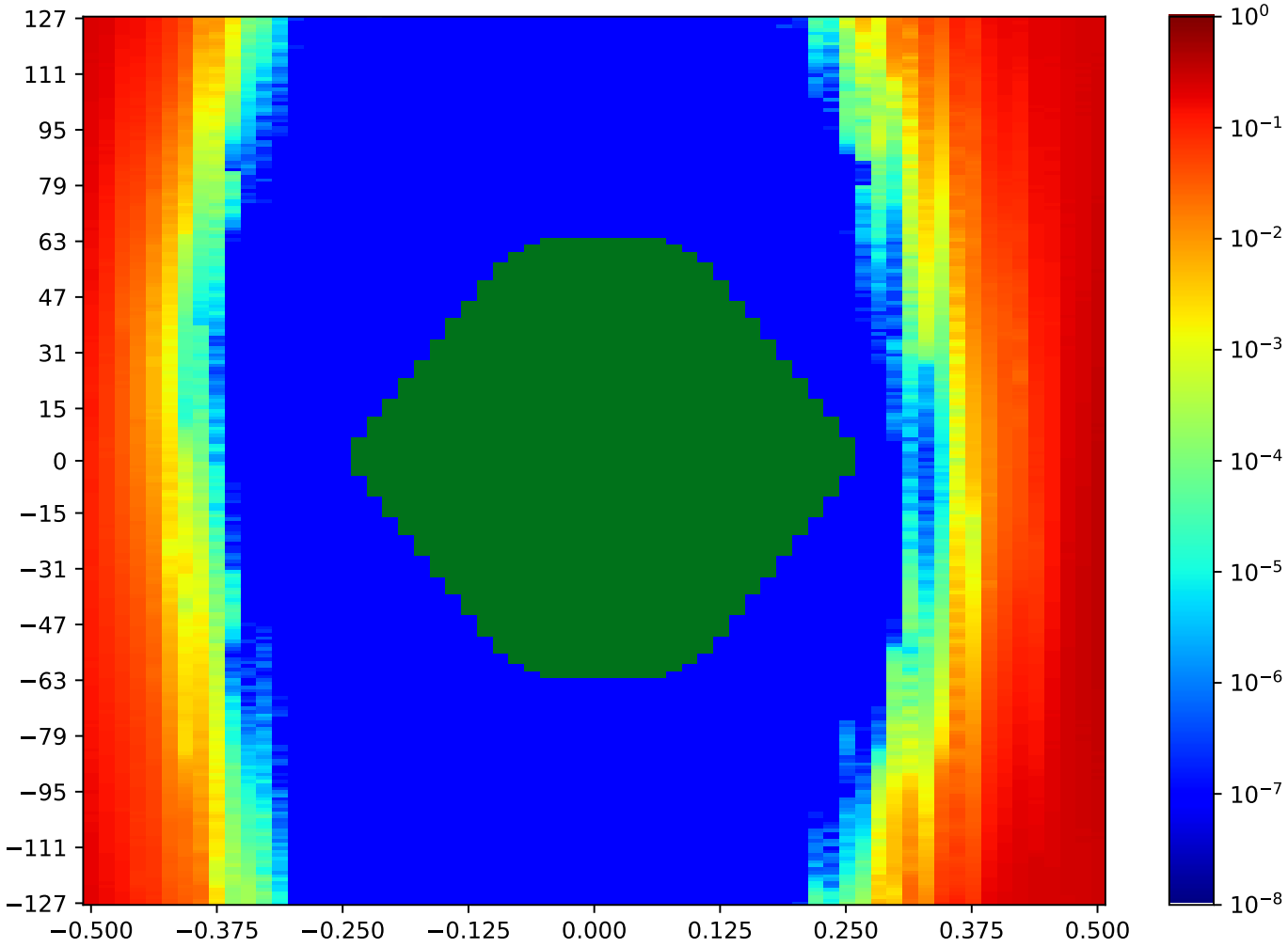


Figure 6.7: MSP_A_FPGA-TX1-05–RX15-05-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.7 MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Table 6.7: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:23:05		2019-Nov-26 17:23:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9721	46	70.77%	246	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

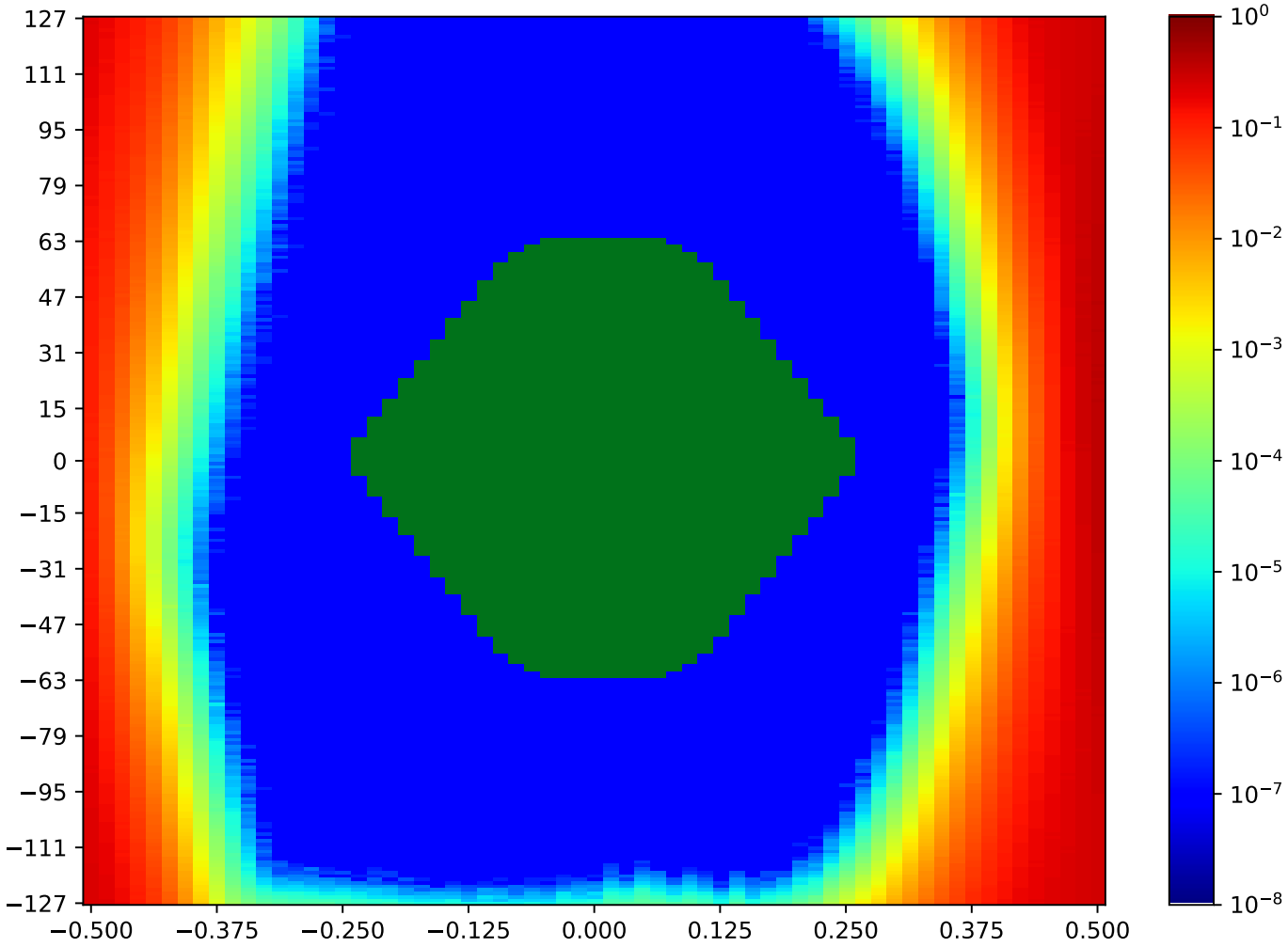


Figure 6.8: MSP_A_FPGA-TX1-06–RX15-06-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.8 MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Table 6.8: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:19:06		2019-Nov-26 17:19:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9596	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

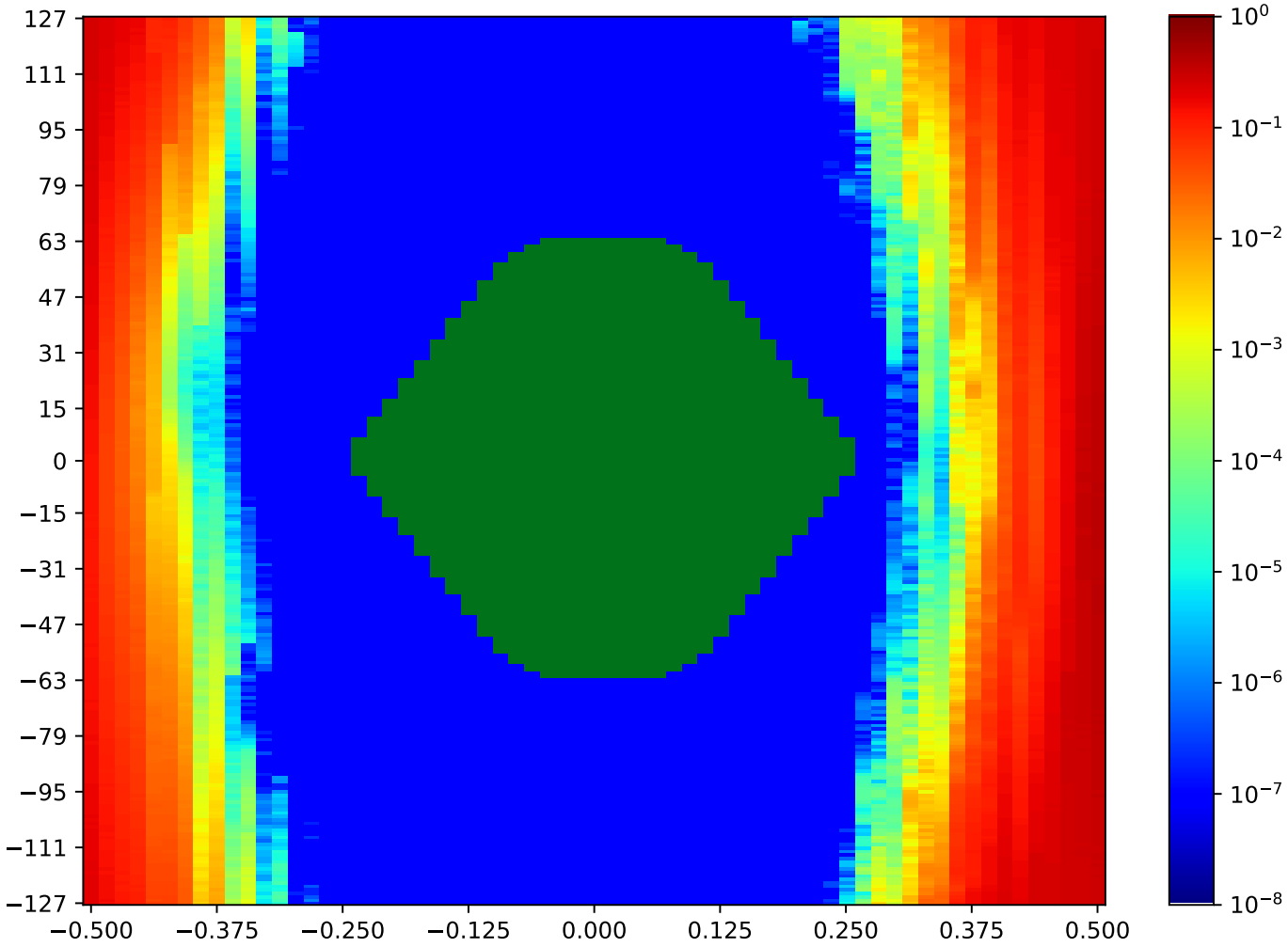


Figure 6.9: MSP_A_FPGA-TX1-07–RX15-07-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.9 MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Table 6.9: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:22:37		2019-Nov-26 17:23:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9423	44	67.69%	249	97.65%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

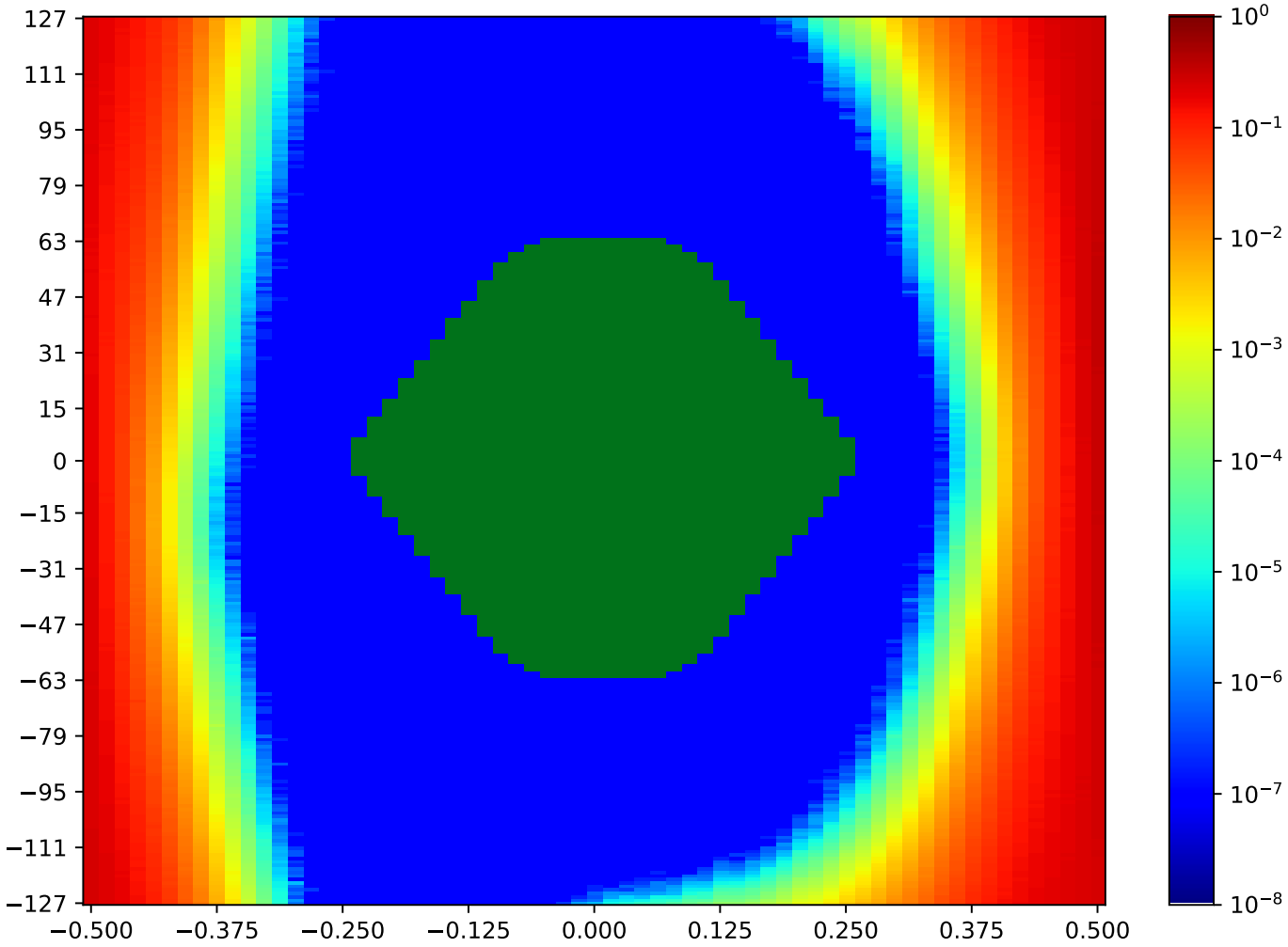


Figure 6.10: MSP_A_FPGA-TX1-08–RX15-08-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.10 MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Table 6.10: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:19:53		2019-Nov-26 17:20:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9567	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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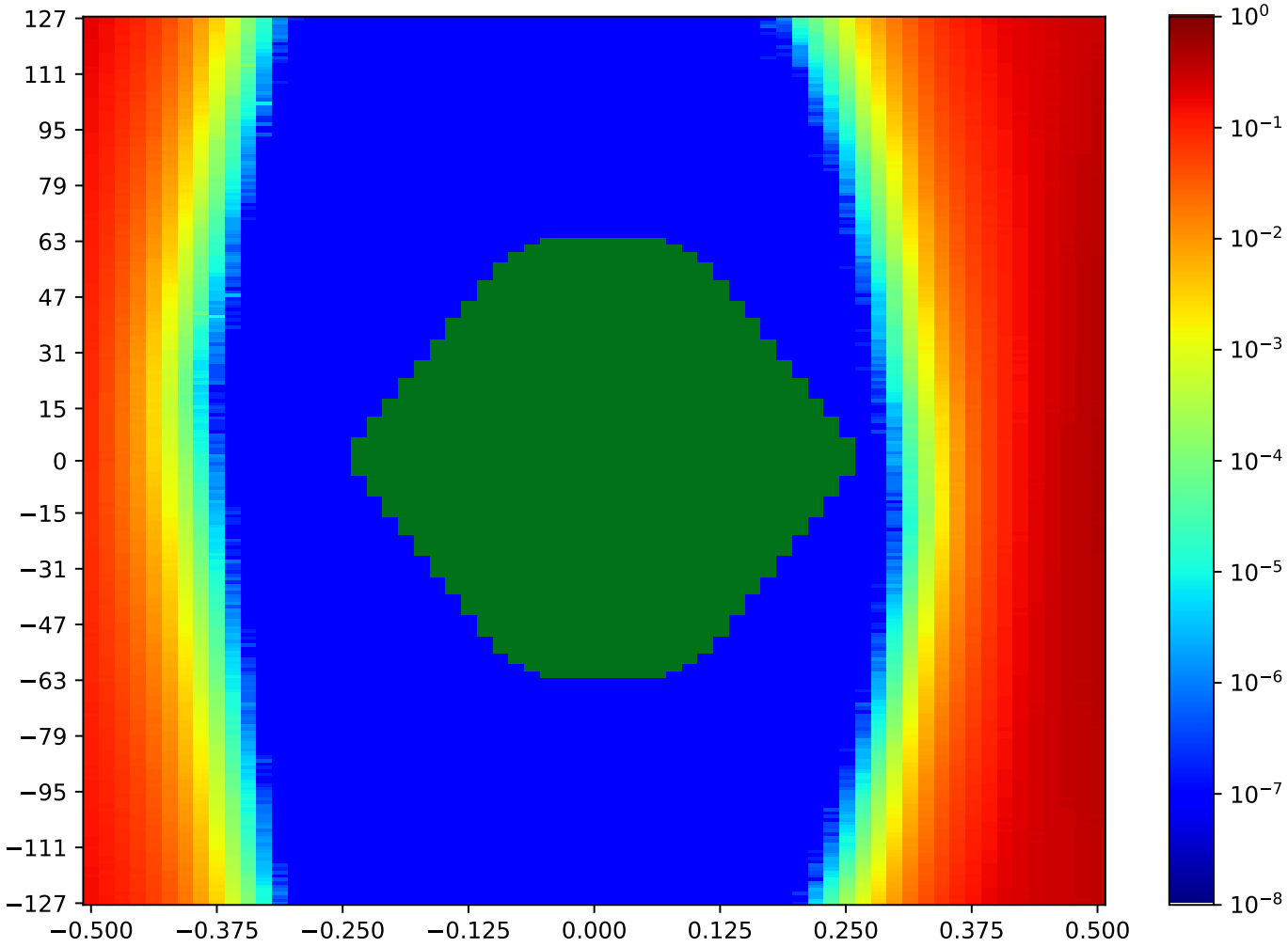


Figure 6.11: MSP_A_FPGA-TX1-09–RX15-09-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.11 MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Table 6.11: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:21:42		2019-Nov-26 17:22:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9044	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

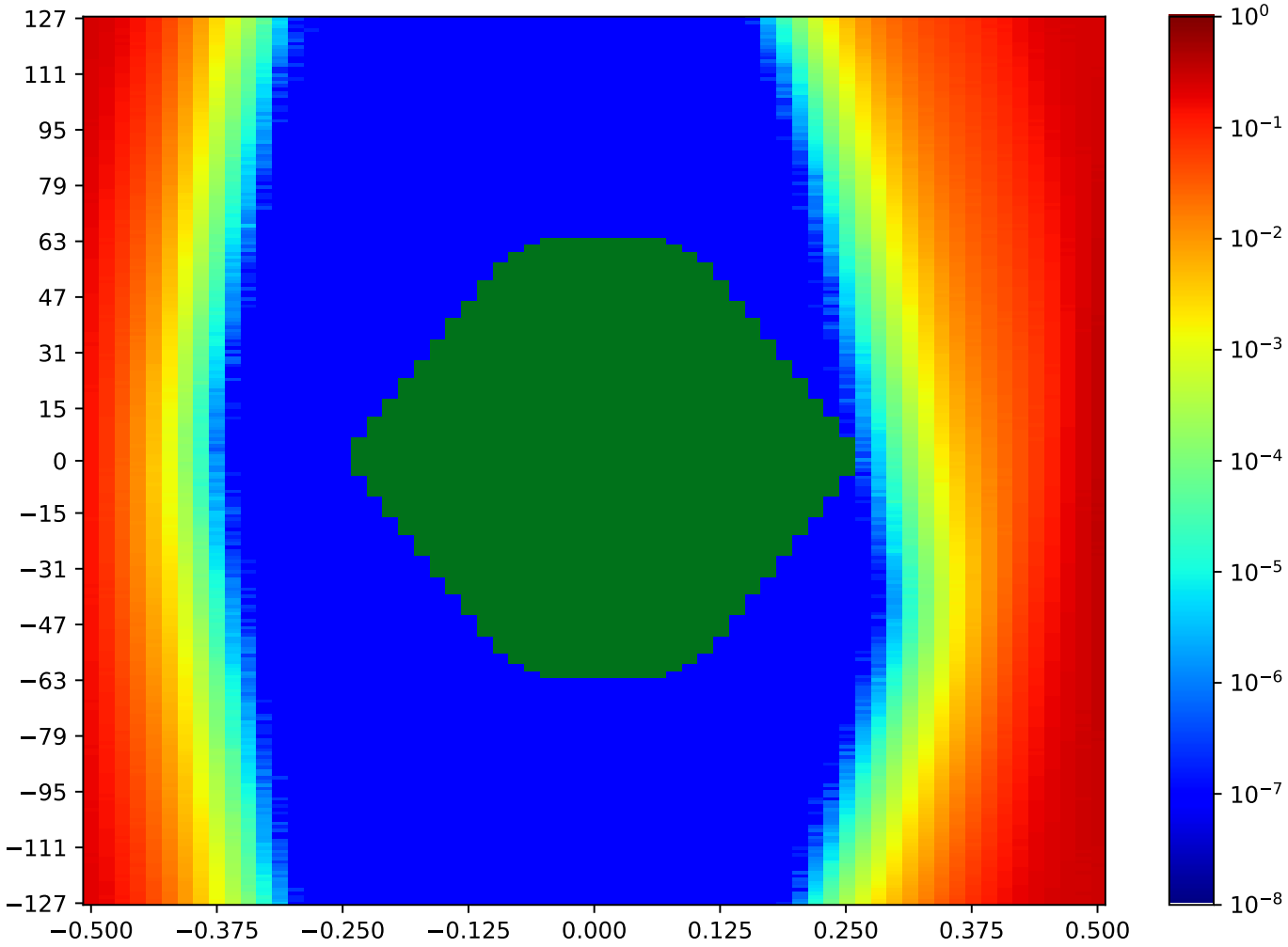


Figure 6.12: MSP_A_FPGA-TX1-10–RX15-10-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.1.12 MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Table 6.12: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:21:15		2019-Nov-26 17:21:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9737	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

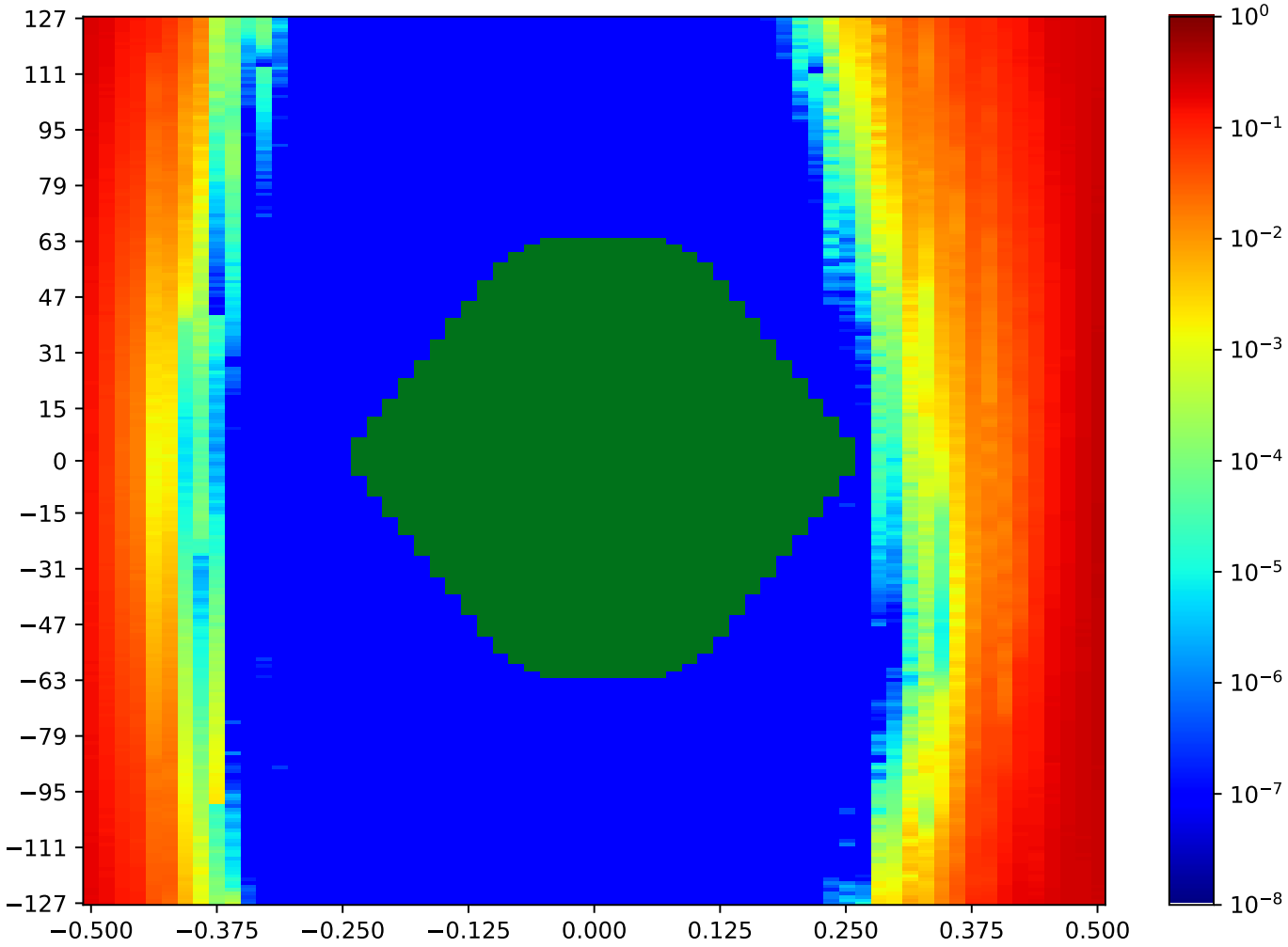


Figure 6.13: MSP_A_FPGA-TX1-11–RX15-11-MSP_C_FPGA

Call back to summary Figure 6.1. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2 MSP_A TX2 MSP_C RX16 Minipod Loopback

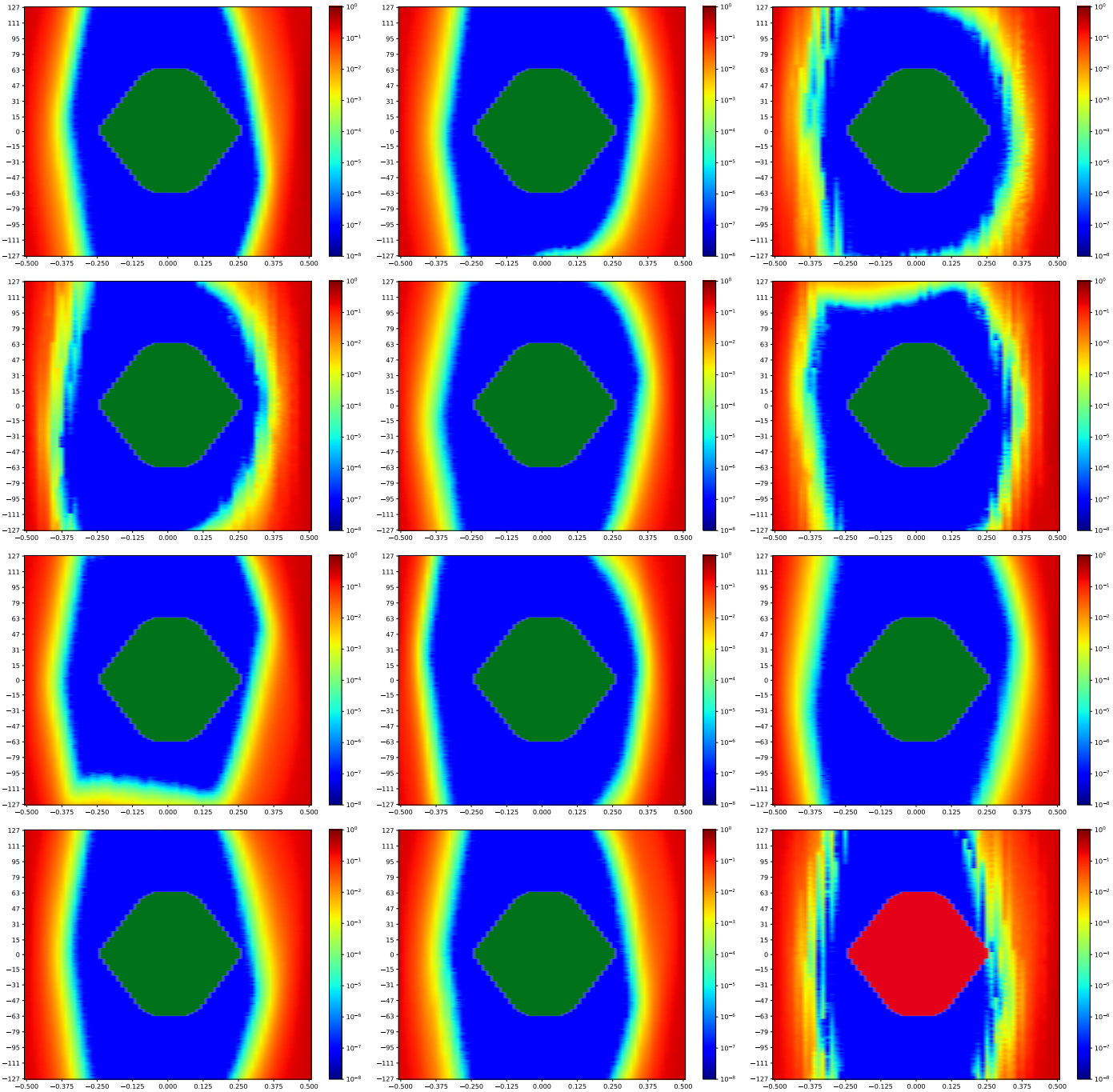


Figure 6.14: MSP_A TX2 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.27.

6.2.1 MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Table 6.13: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:24:42		2019-Nov-26 17:25:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8973	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

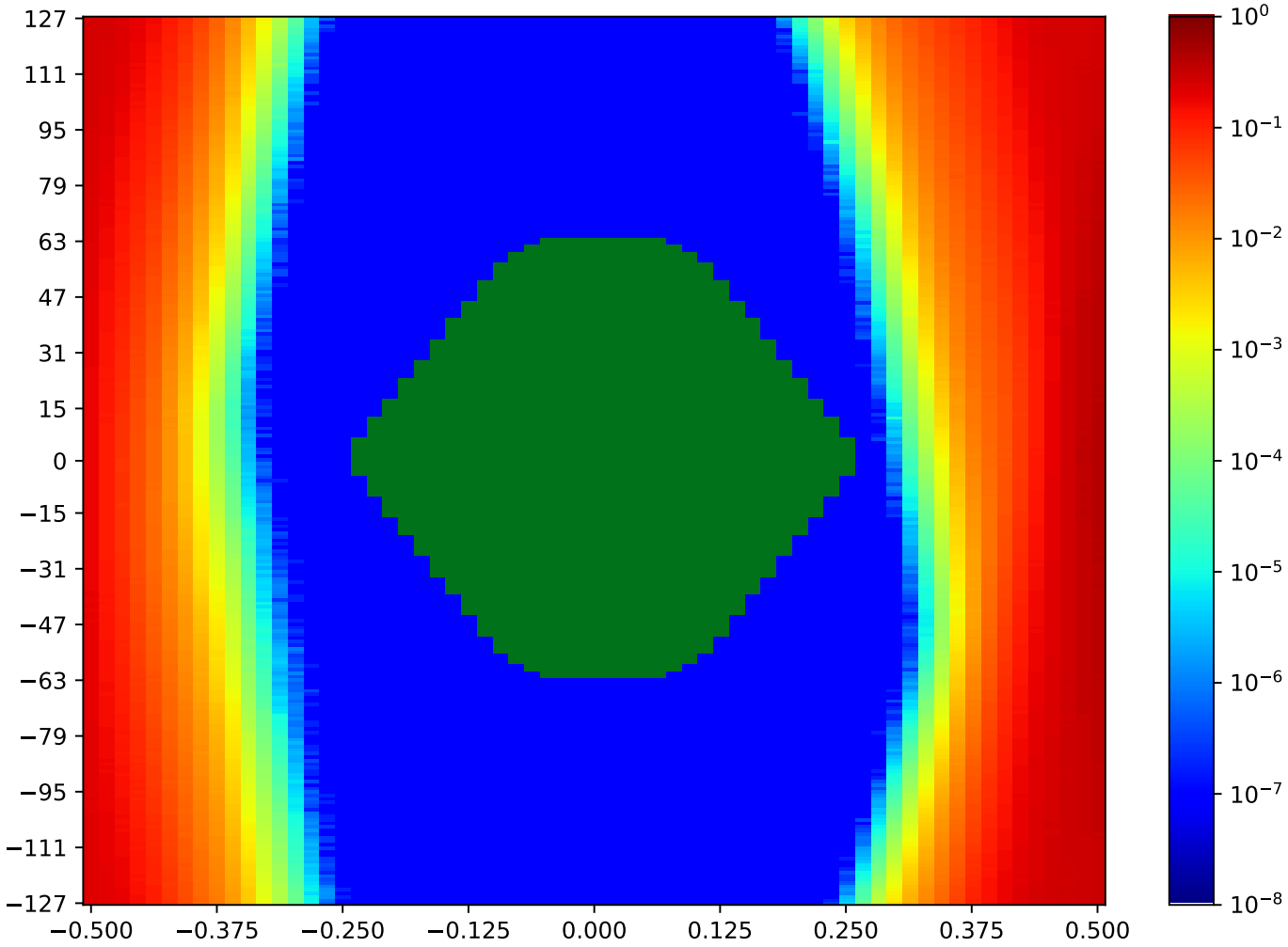


Figure 6.15: MSP_A_FPGA-TX2-00–RX16-00-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.2 MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Table 6.14: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:23:52		2019-Nov-26 17:24:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8668	39	60.00%	248	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

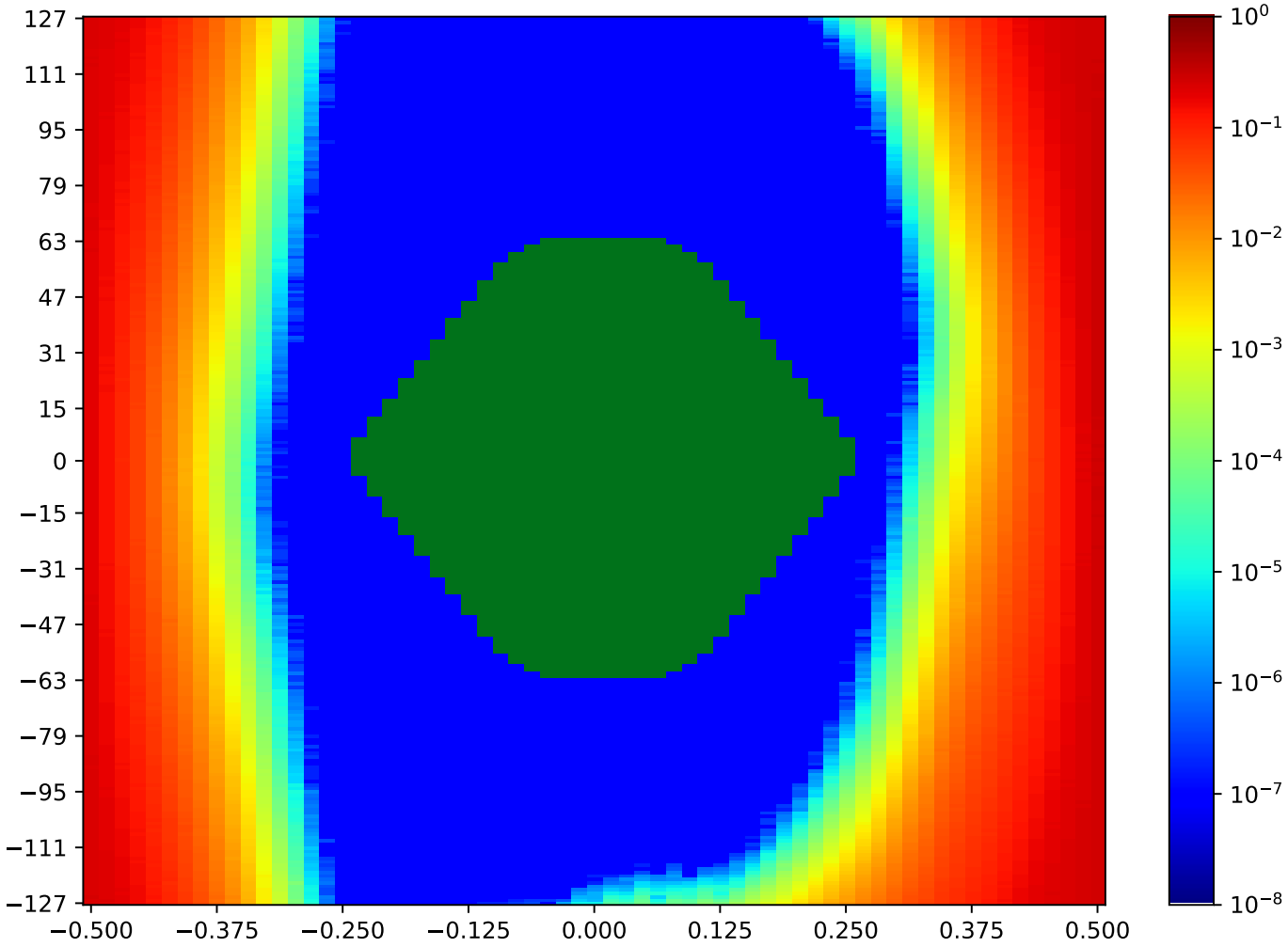


Figure 6.16: MSP_A_FPGA-TX2-01–RX16-01-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.3 MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Table 6.15: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:26:04		2019-Nov-26 17:26:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8301	40	61.54%	246	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

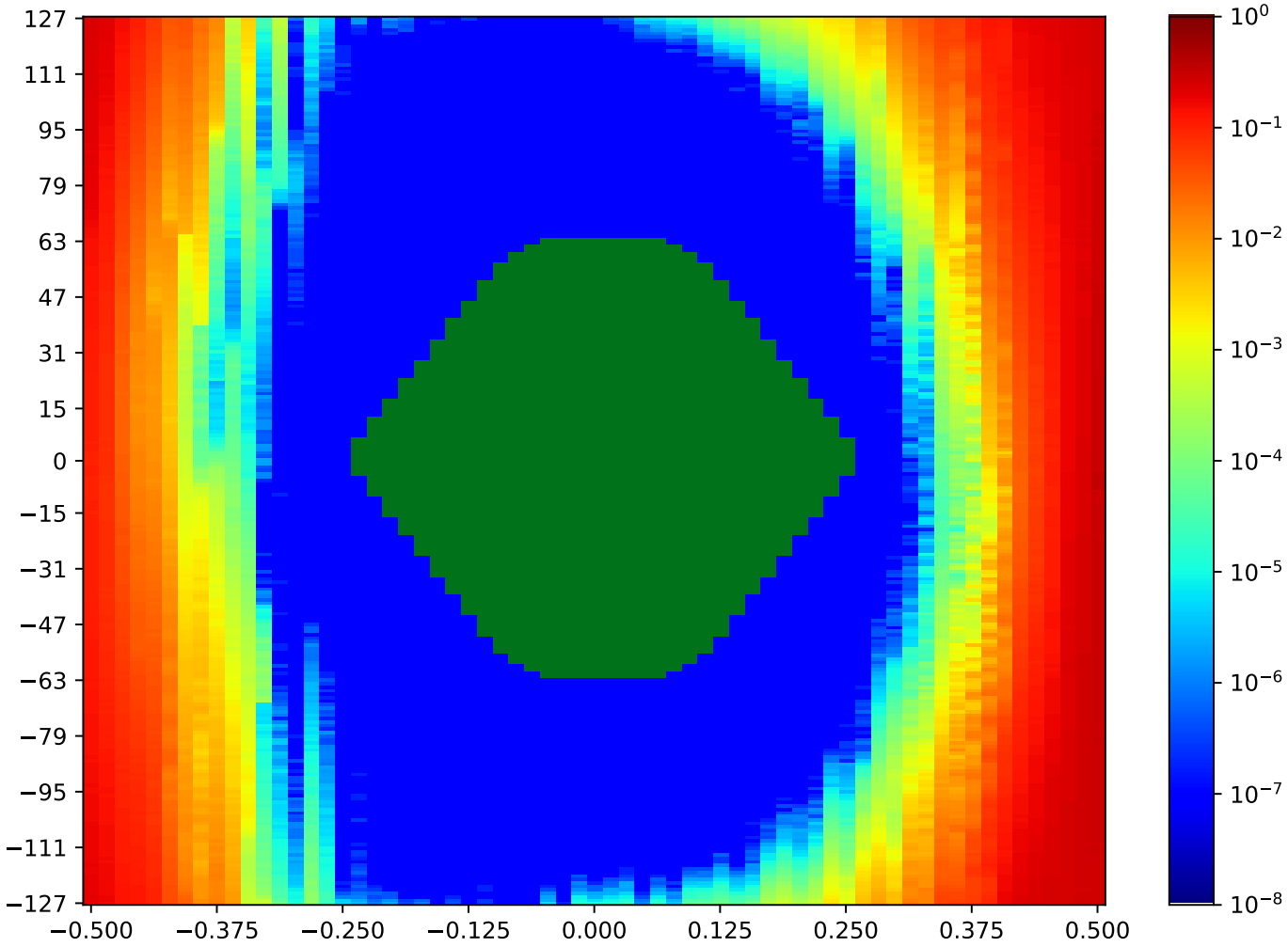


Figure 6.17: MSP_A_FPGA-TX2-02–RX16-02-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.4 MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Table 6.16: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:23:33		2019-Nov-26 17:23:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8964	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

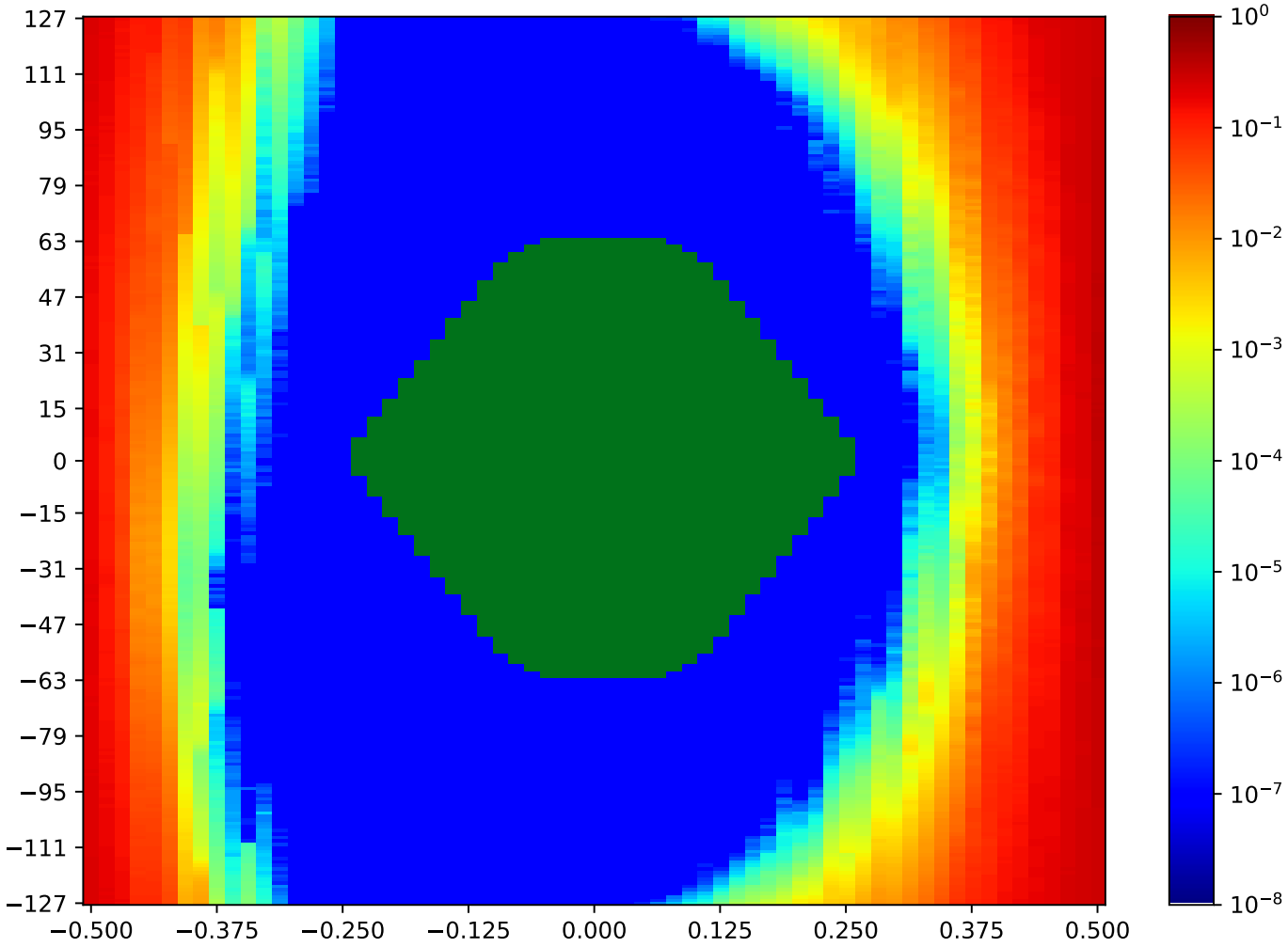


Figure 6.18: MSP_A_FPGA-TX2-03–RX16-03-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.5 MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Table 6.17: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:27:15		2019-Nov-26 17:27:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9094	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

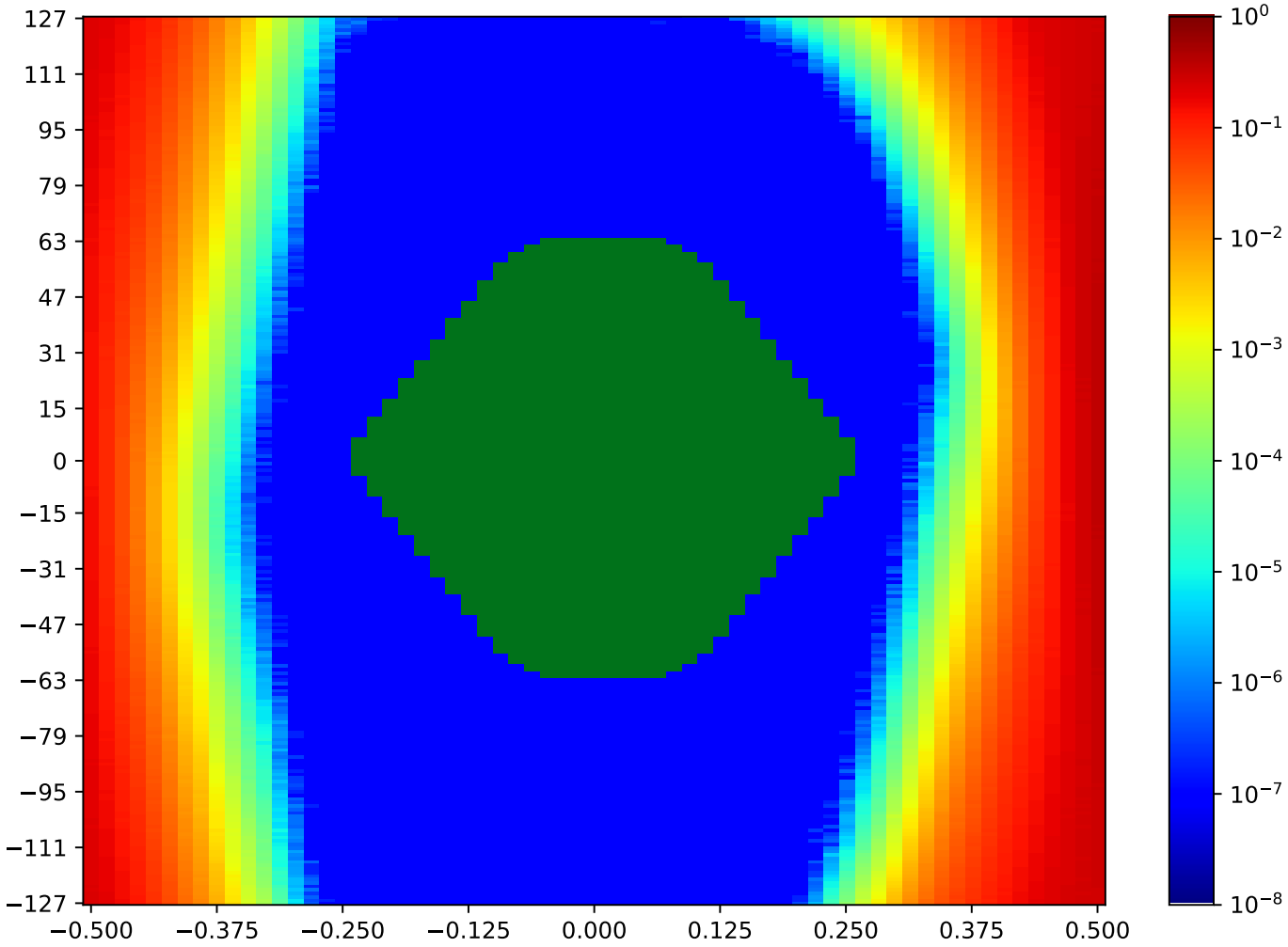


Figure 6.19: MSP_A_FPGA-TX2-04–RX16-04-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.6 MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Table 6.18: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:24:17		2019-Nov-26 17:24:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8427	41	63.08%	228	89.41%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

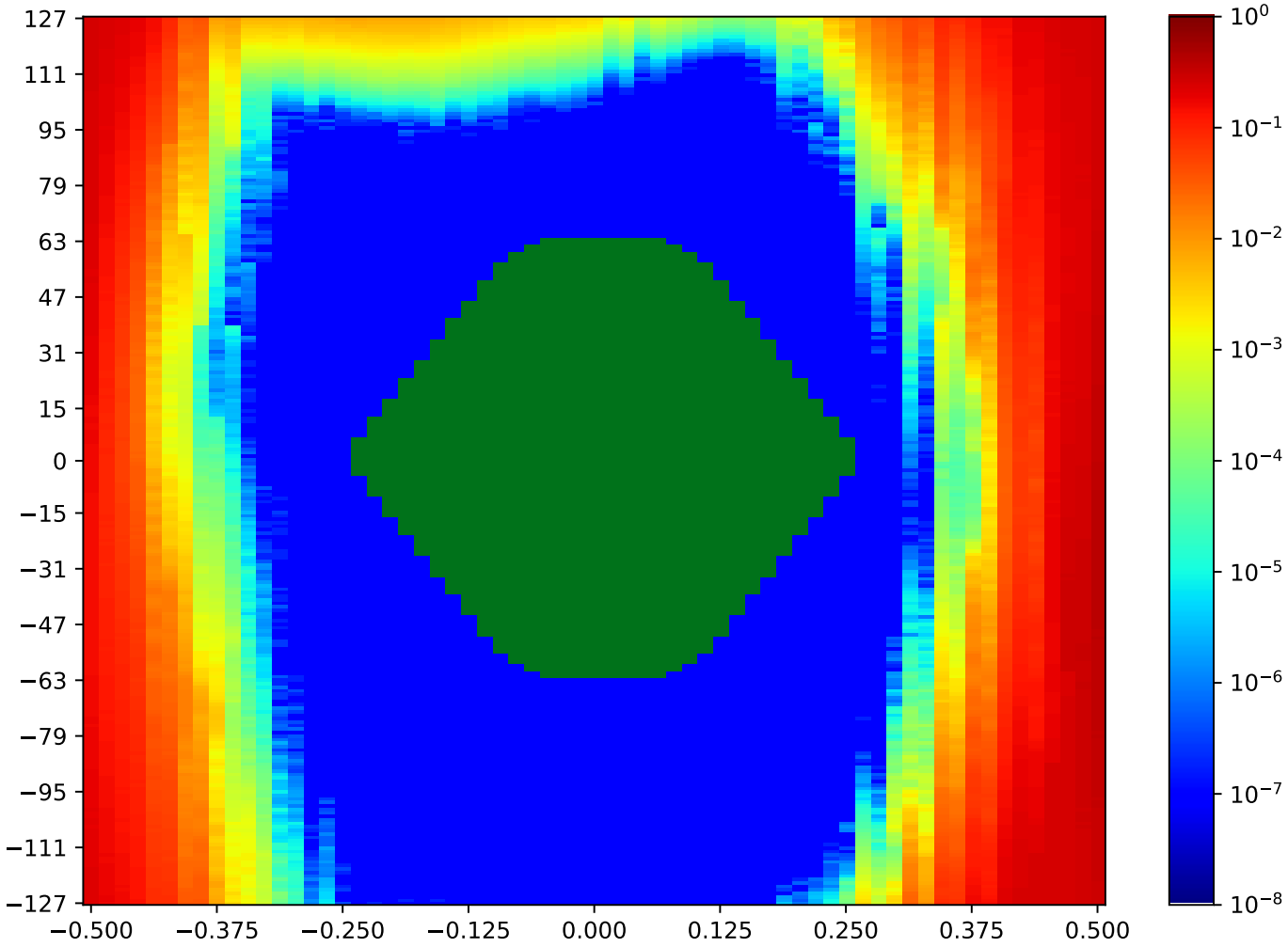


Figure 6.20: MSP_A_FPGA-TX2-05–RX16-05-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.7 MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Table 6.19: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:28:10		2019-Nov-26 17:28:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8230	40	61.54%	229	89.41%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

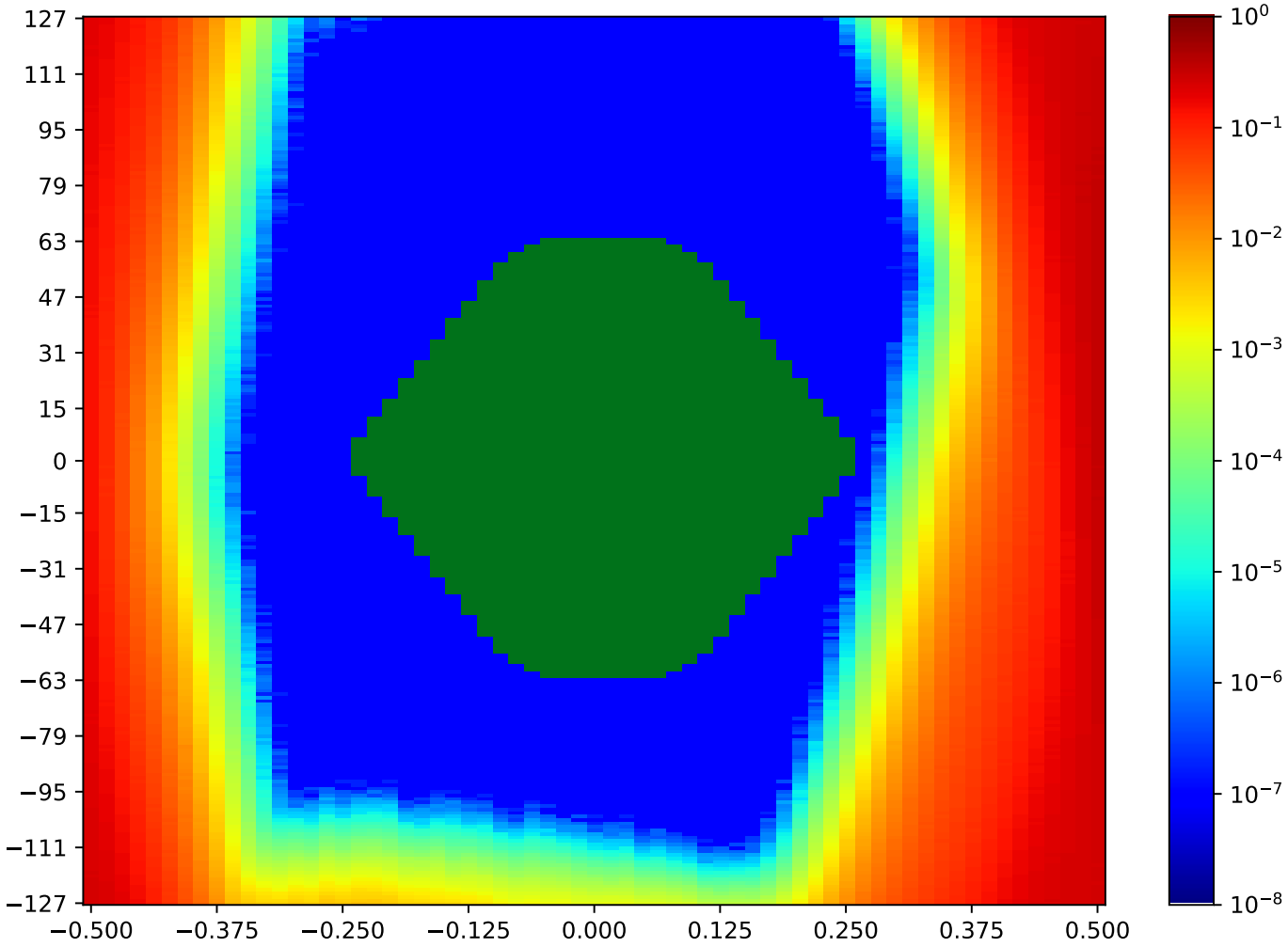


Figure 6.21: MSP_A_FPGA-TX2-06–RX16-06-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.8 MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Table 6.20: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:25:09		2019-Nov-26 17:25:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9966	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

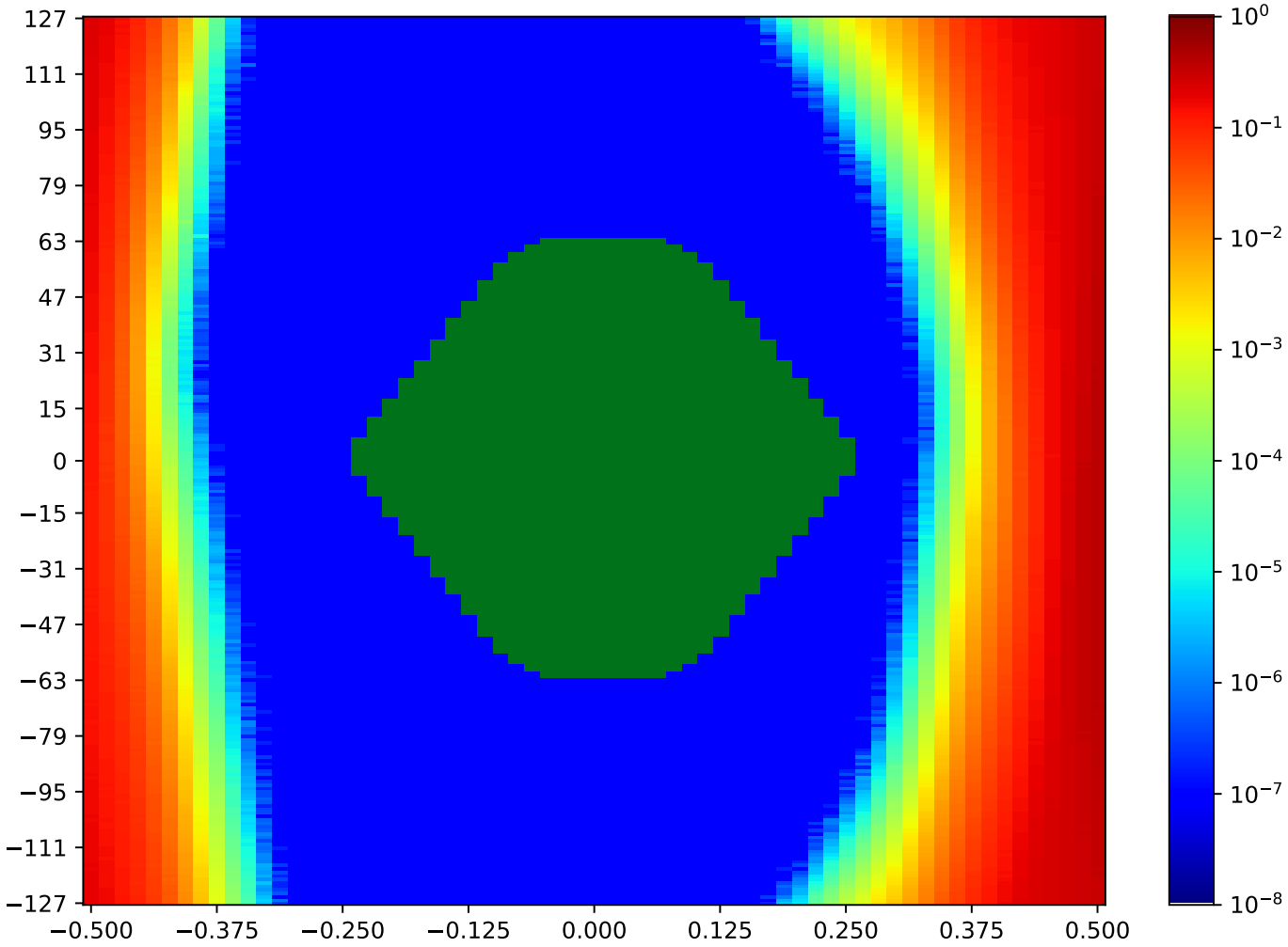


Figure 6.22: MSP_A_FPGA-TX2-07–RX16-07-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.9 MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Table 6.21: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:27:42		2019-Nov-26 17:28:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9285	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

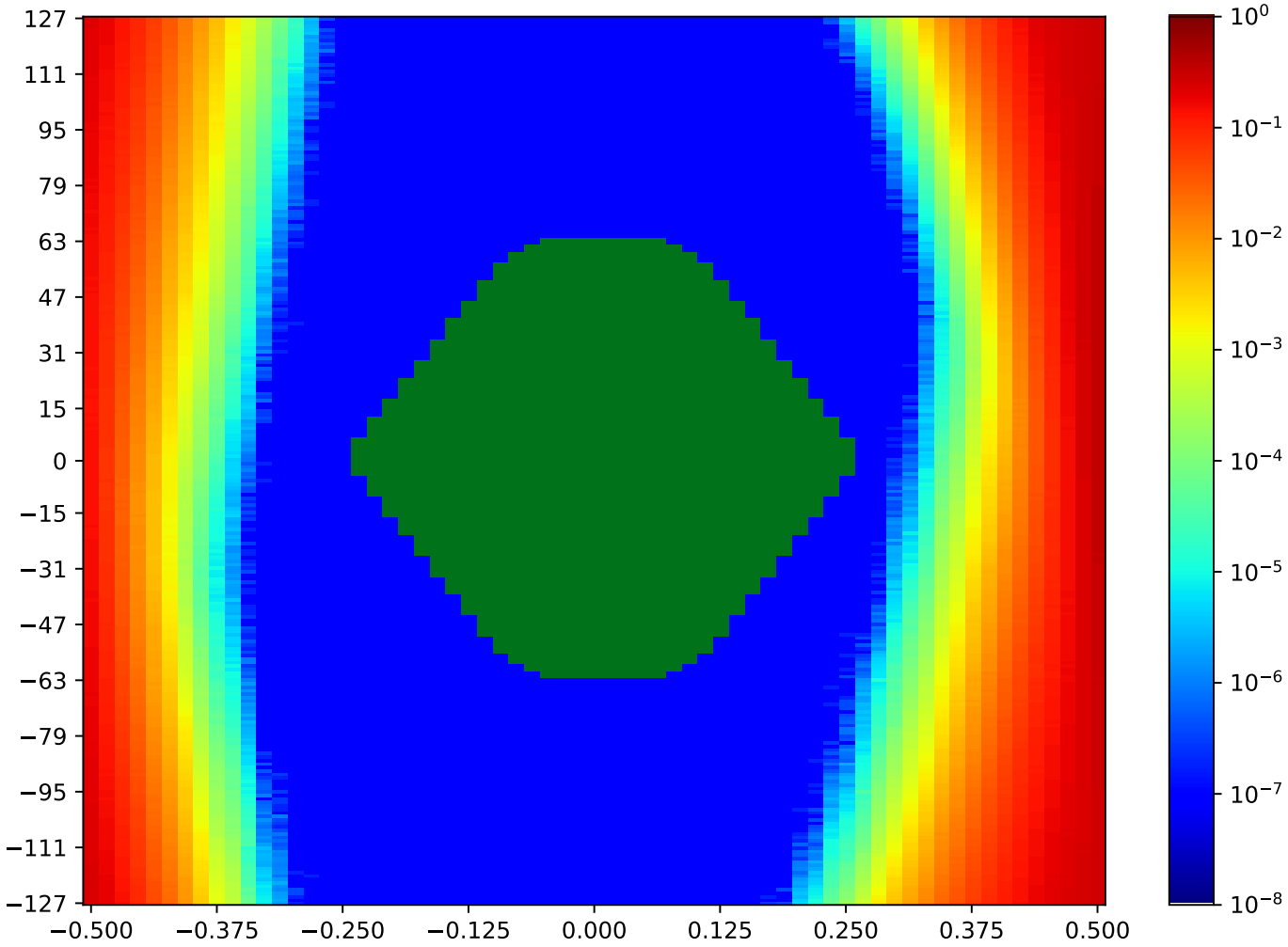


Figure 6.23: MSP_A_FPGA-TX2-08–RX16-08-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.10 MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Table 6.22: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:25:36		2019-Nov-26 17:26:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8575	38	58.46%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

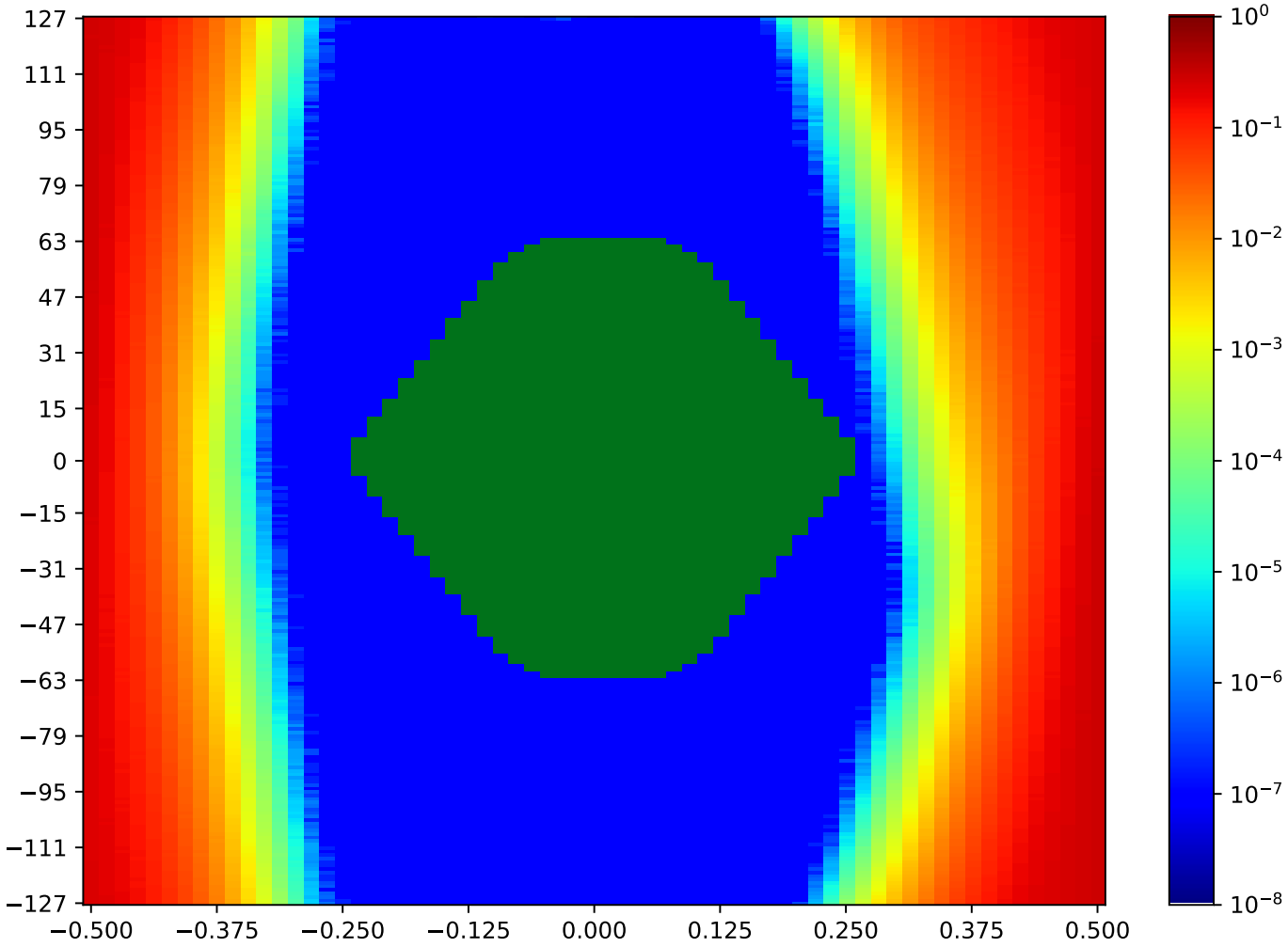


Figure 6.24: MSP_A_FPGA-TX2-09–RX16-09-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.11 MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Table 6.23: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:26:50		2019-Nov-26 17:27:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8700	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

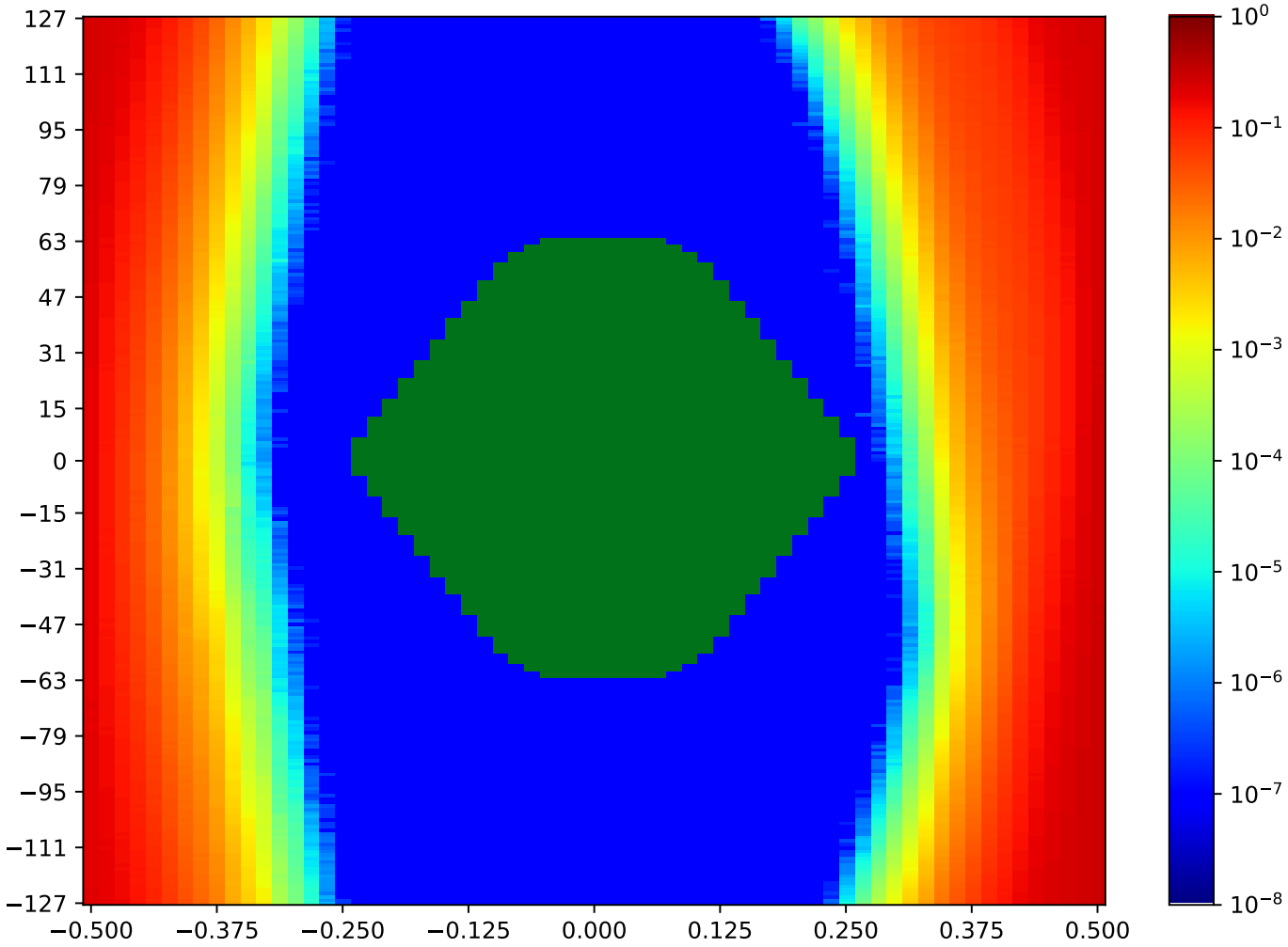


Figure 6.25: MSP_A_FPGA-TX2-10–RX16-10-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.2.12 MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Table 6.24: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:26:30		2019-Nov-26 17:26:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8089	36	53.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

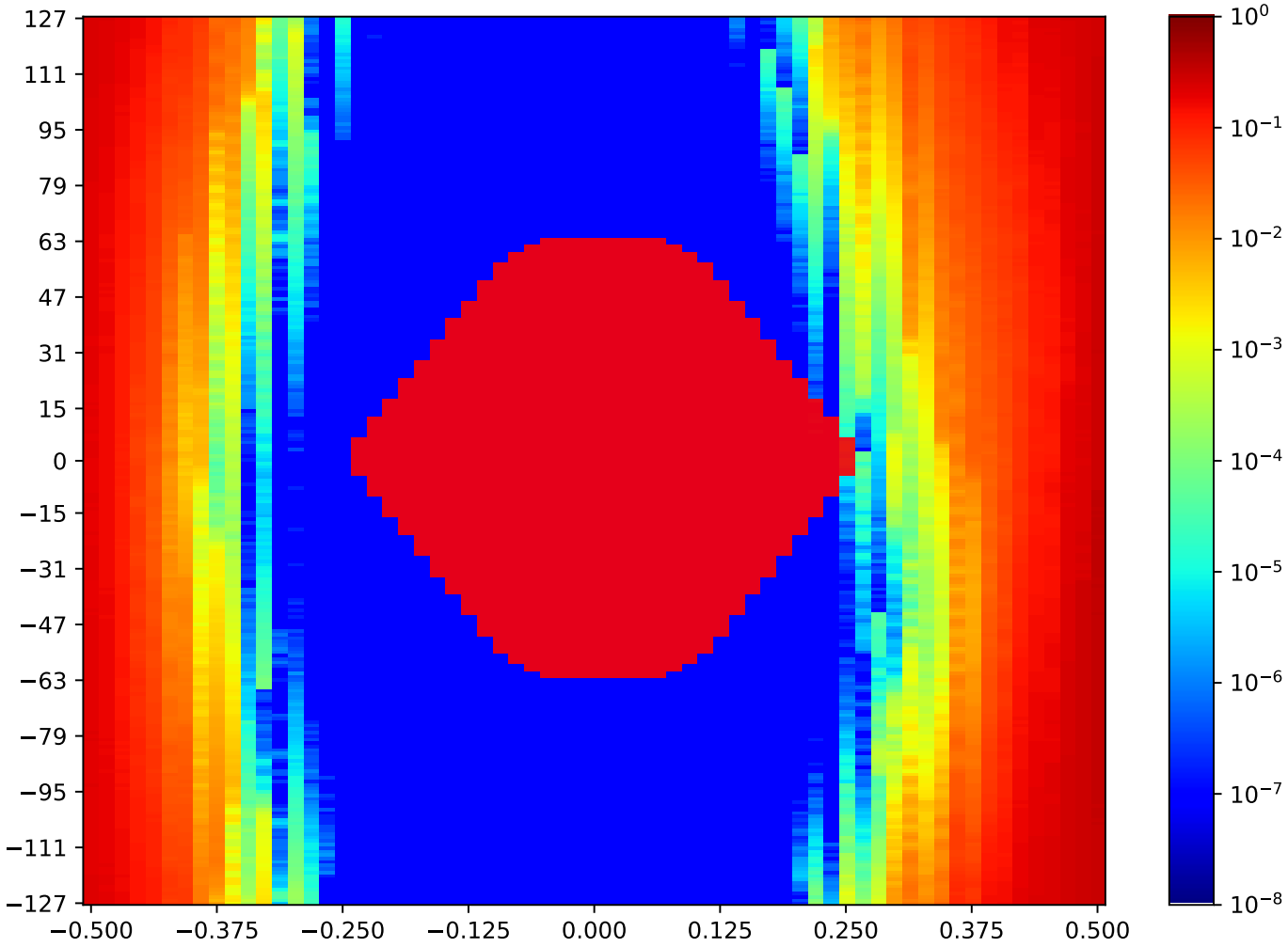


Figure 6.26: MSP_A_FPGA-TX2-11–RX16-11-MSP_C_FPGA

Call back to summary Figure 6.14. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3 MSP_C TX3 MSP_A RX6 Minipod Loopback

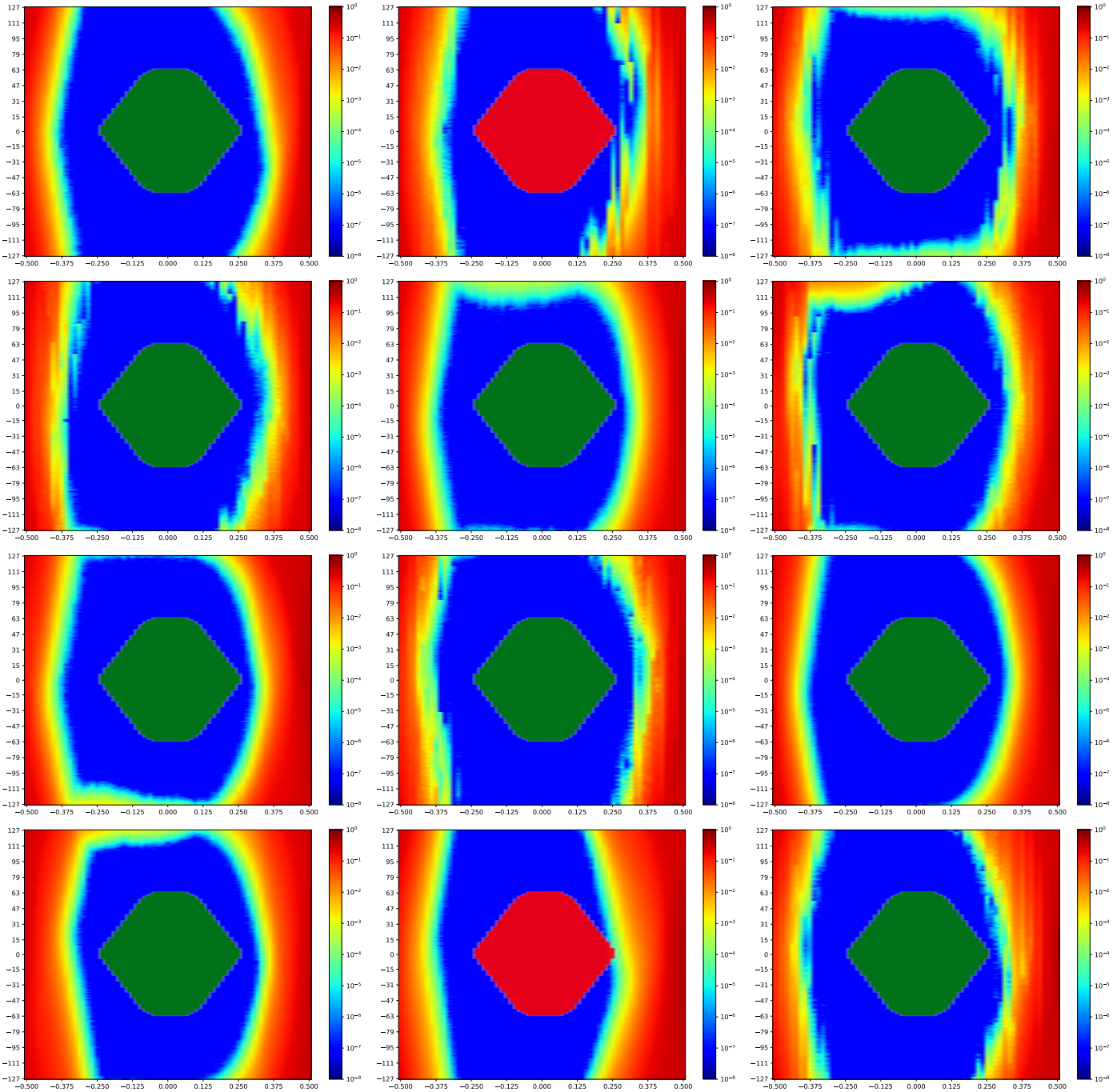


Figure 6.27: MSP_C TX3 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.40.

6.3.1 MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Table 6.25: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:29:50		2019-Nov-26 17:30:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9689	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

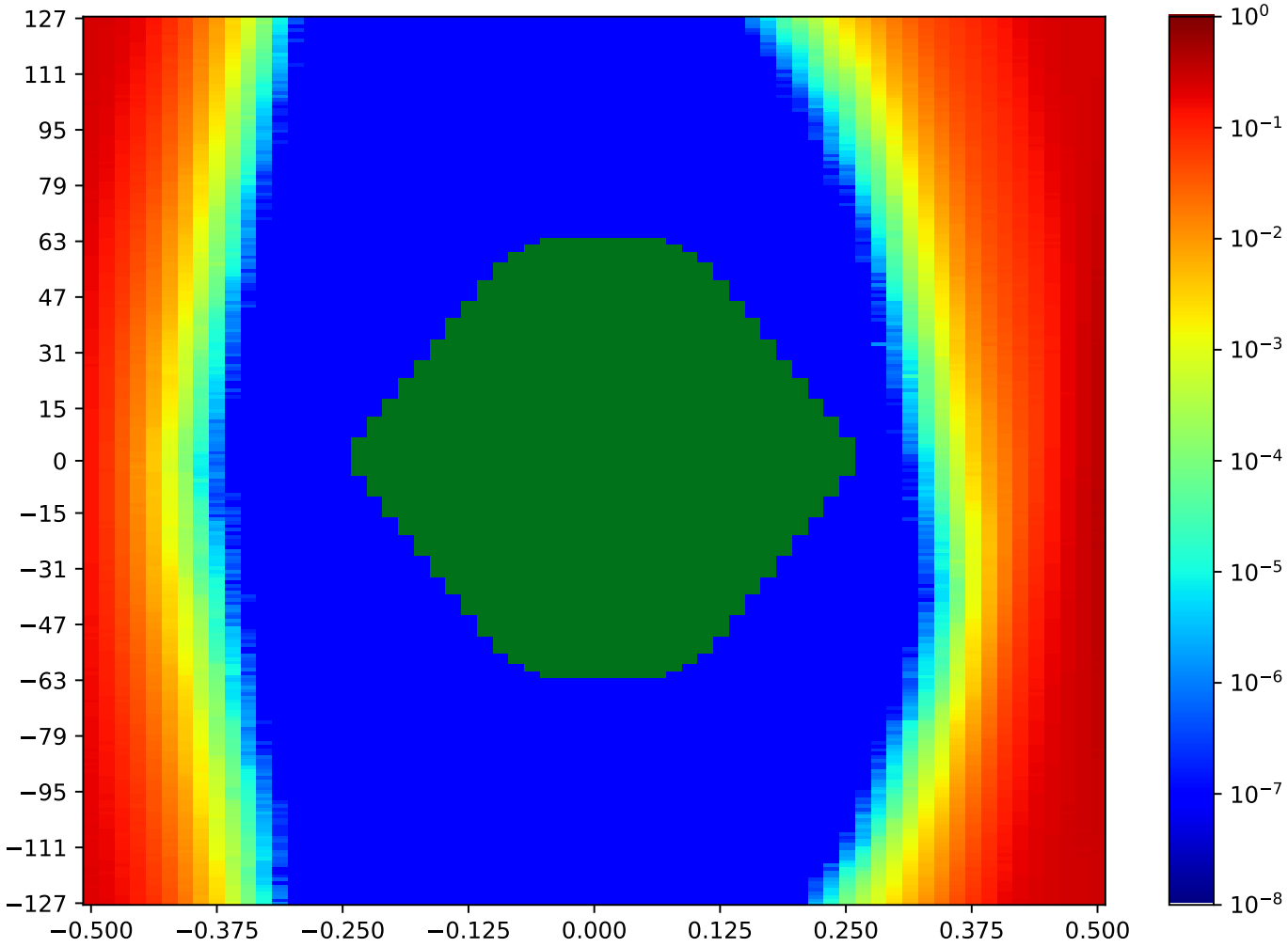


Figure 6.28: MSP_C_FPGA-TX3-00–RX6-00-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.2 MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Table 6.26: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:30:44		2019-Nov-26 17:31:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8661	38	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

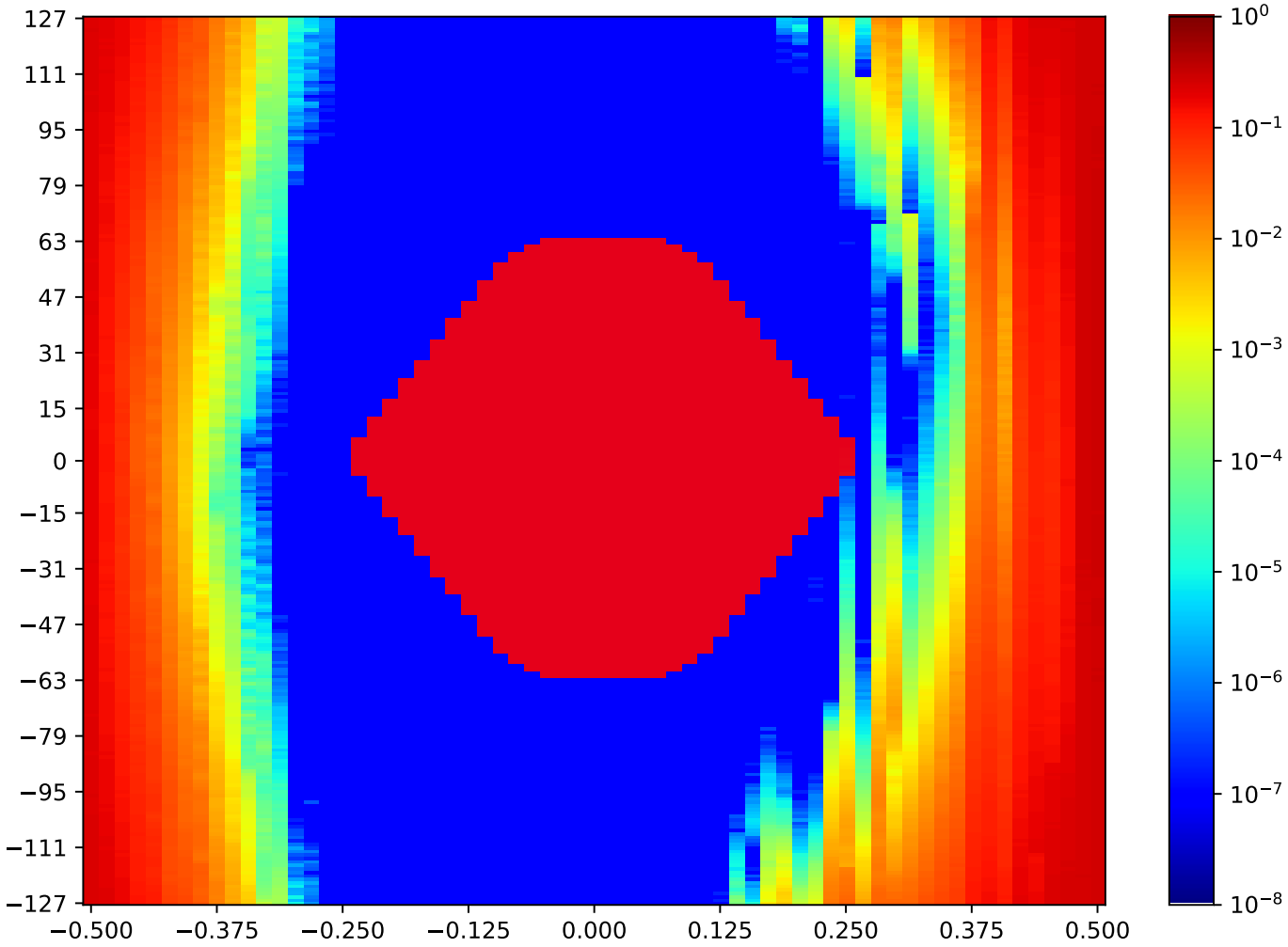


Figure 6.29: MSP_C_FPGA-TX3-01–RX6-01-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.3 MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Table 6.27: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:31:12		2019-Nov-26 17:31:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8149	43	64.62%	225	87.06%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

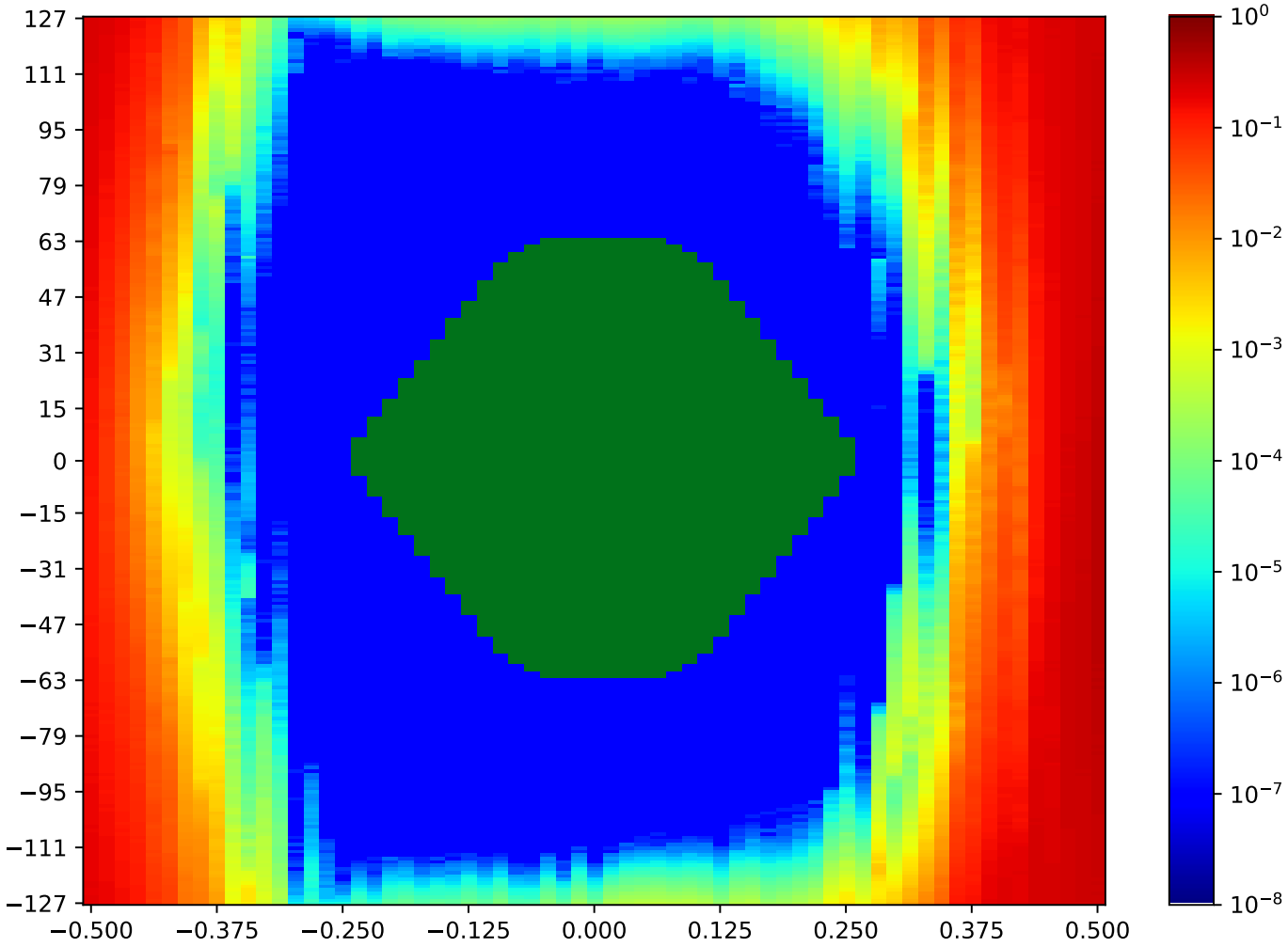


Figure 6.30: MSP_C_FPGA-TX3-02–RX6-02-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.4 MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Table 6.28: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:28:56		2019-Nov-26 17:29:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9159	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

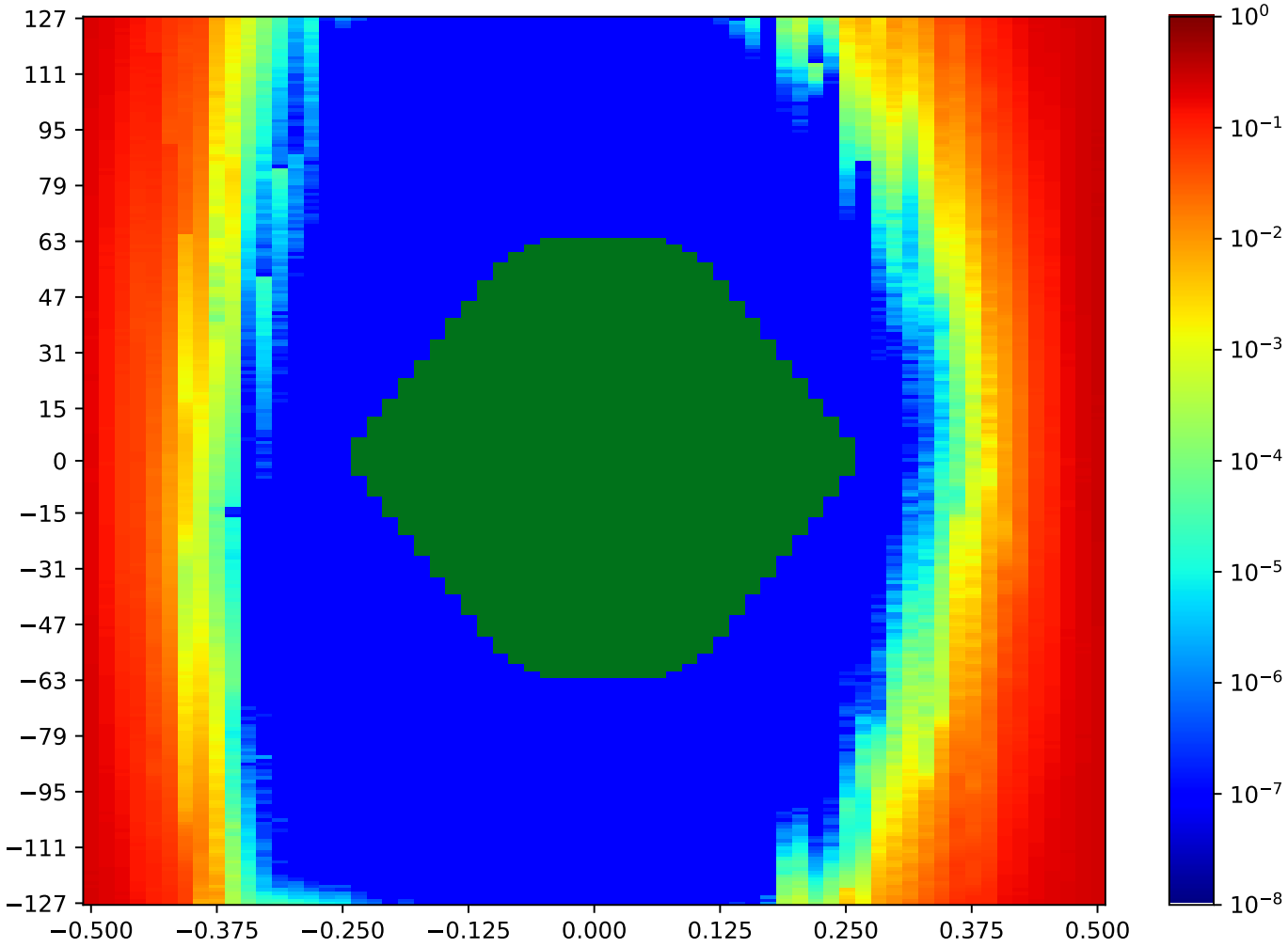


Figure 6.31: MSP_C_FPGA-TX3-03–RX6-03-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.5 MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Table 6.29: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:32:24		2019-Nov-26 17:32:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7875	41	63.08%	223	87.06%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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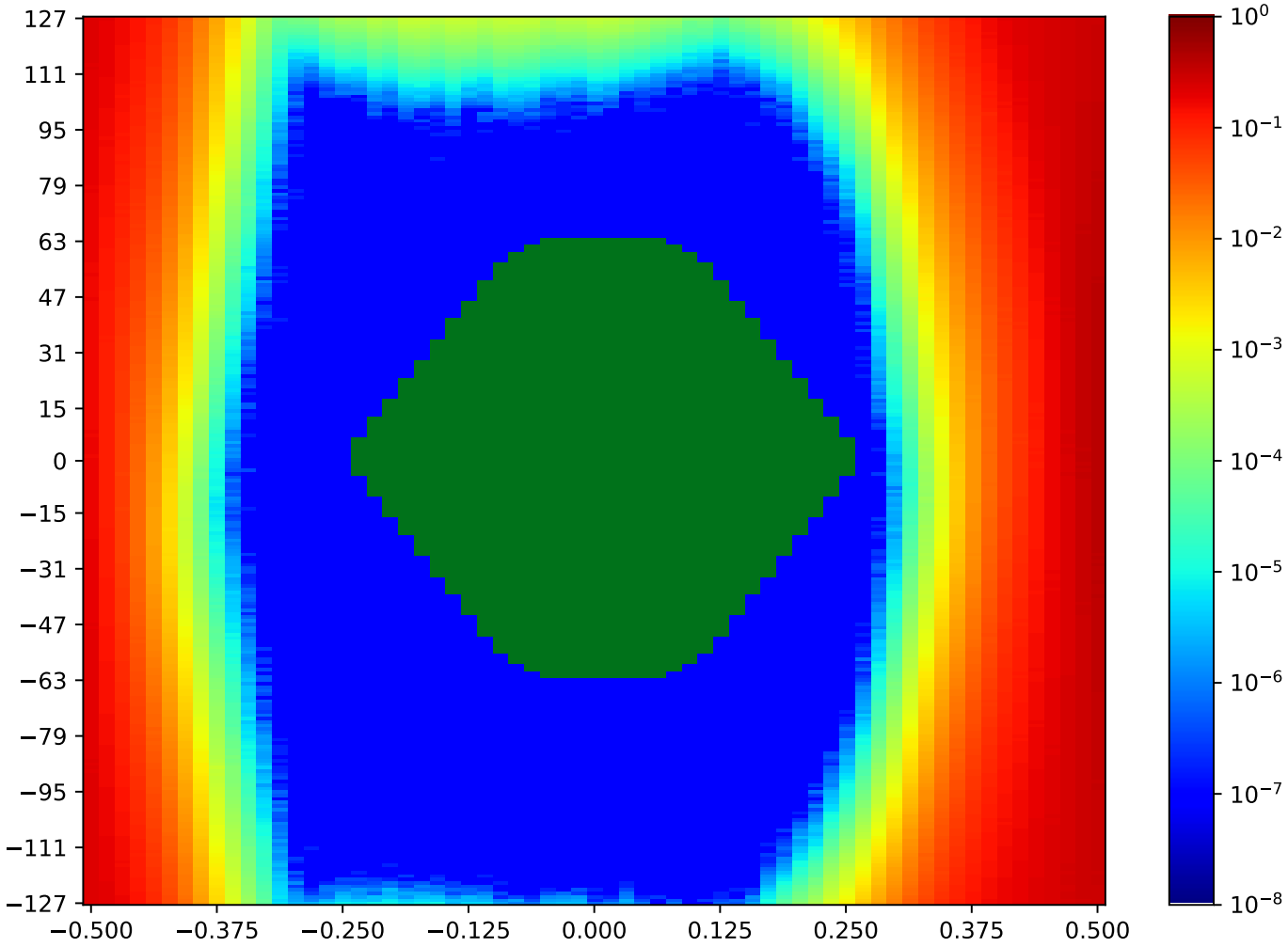


Figure 6.32: MSP_C_FPGA-TX3-04–RX6-04-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.6 MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Table 6.30: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:28:37		2019-Nov-26 17:28:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8631	41	63.08%	247	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

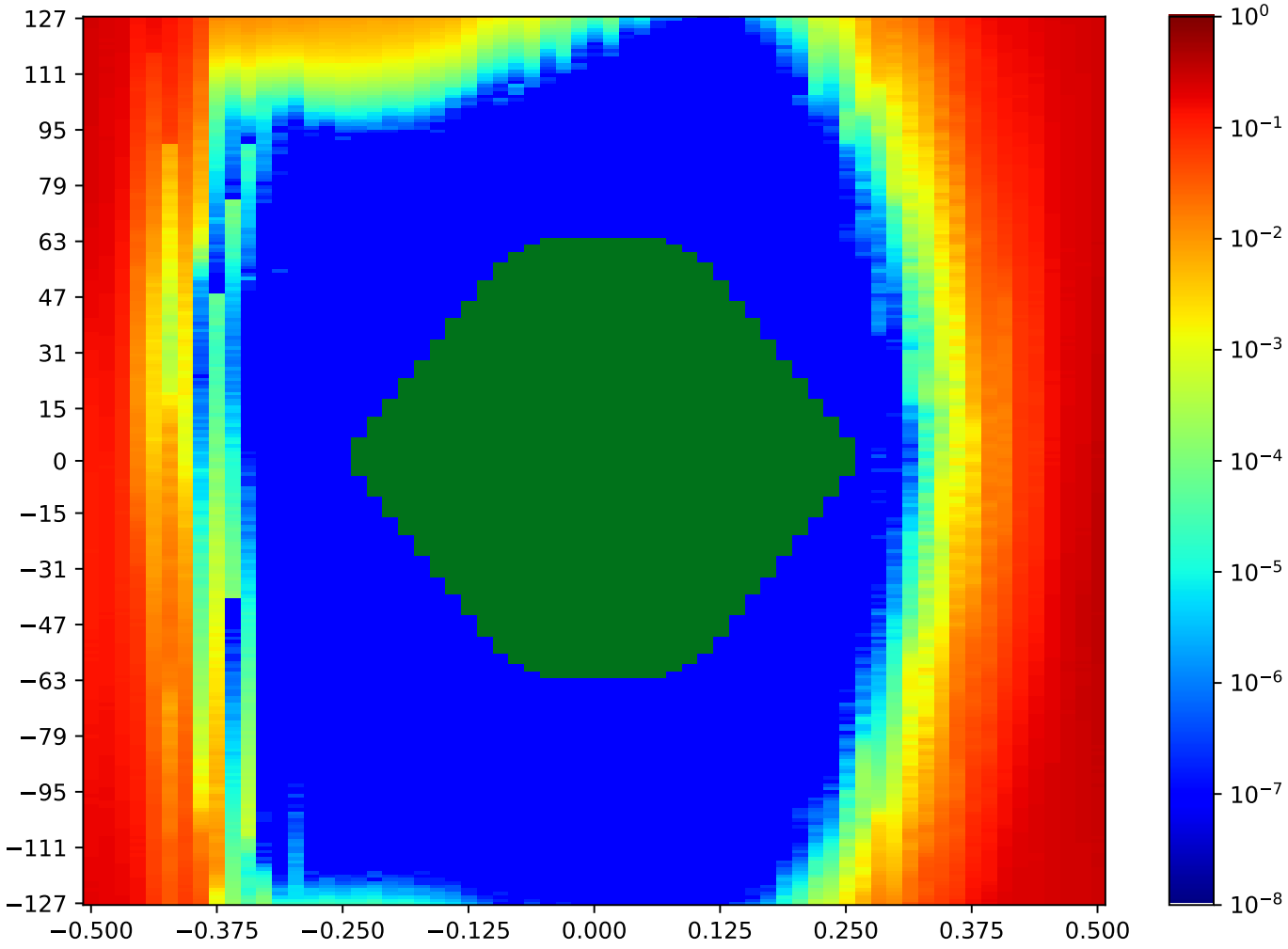


Figure 6.33: MSP_C_FPGA-TX3-05–RX6-05-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.7 MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Table 6.31: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:33:18		2019-Nov-26 17:33:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8257	40	61.54%	239	93.73%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

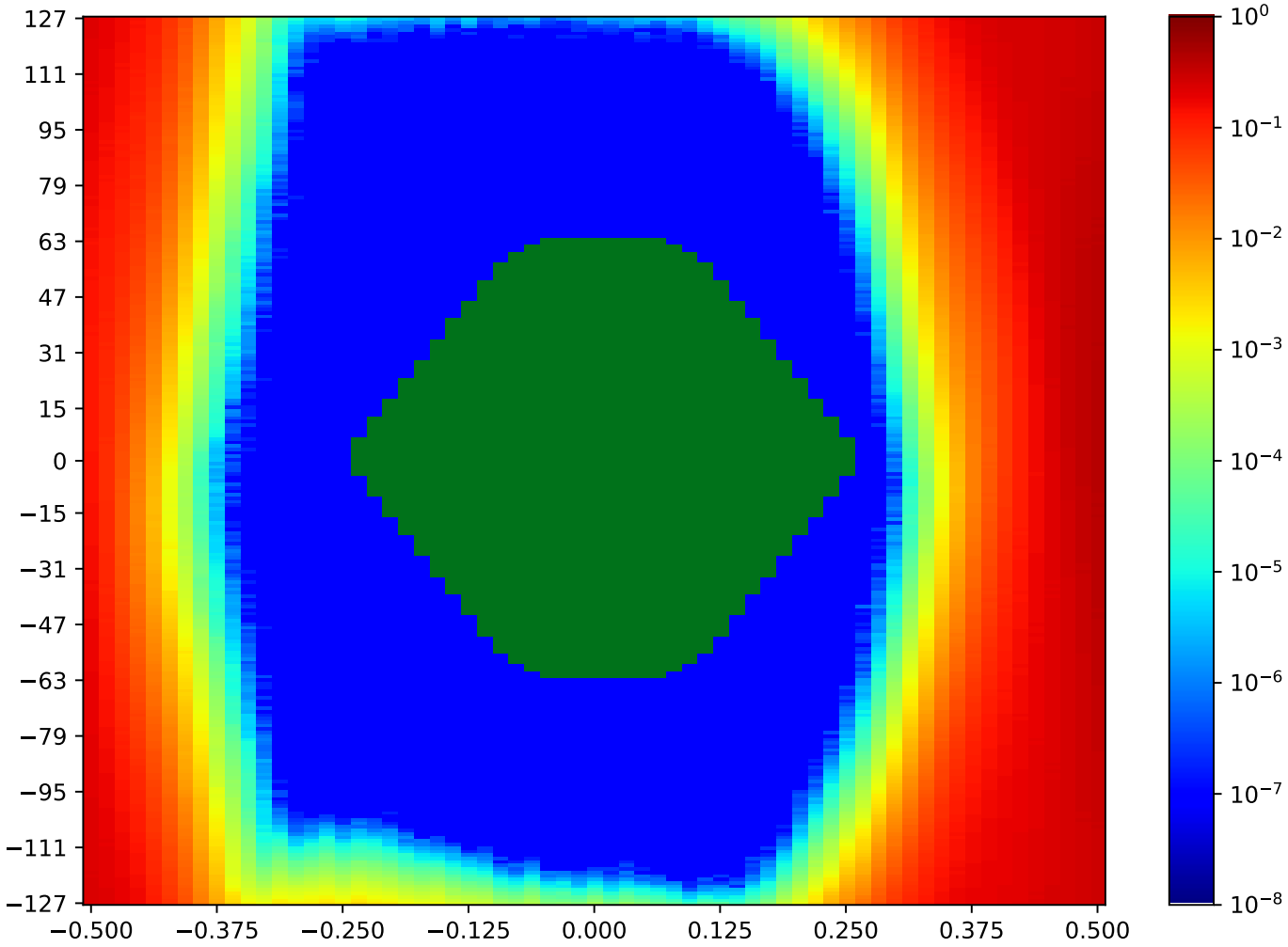


Figure 6.34: MSP_C_FPGA-TX3-06–RX6-06-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.8 MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Table 6.32: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:29:23		2019-Nov-26 17:29:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9776	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

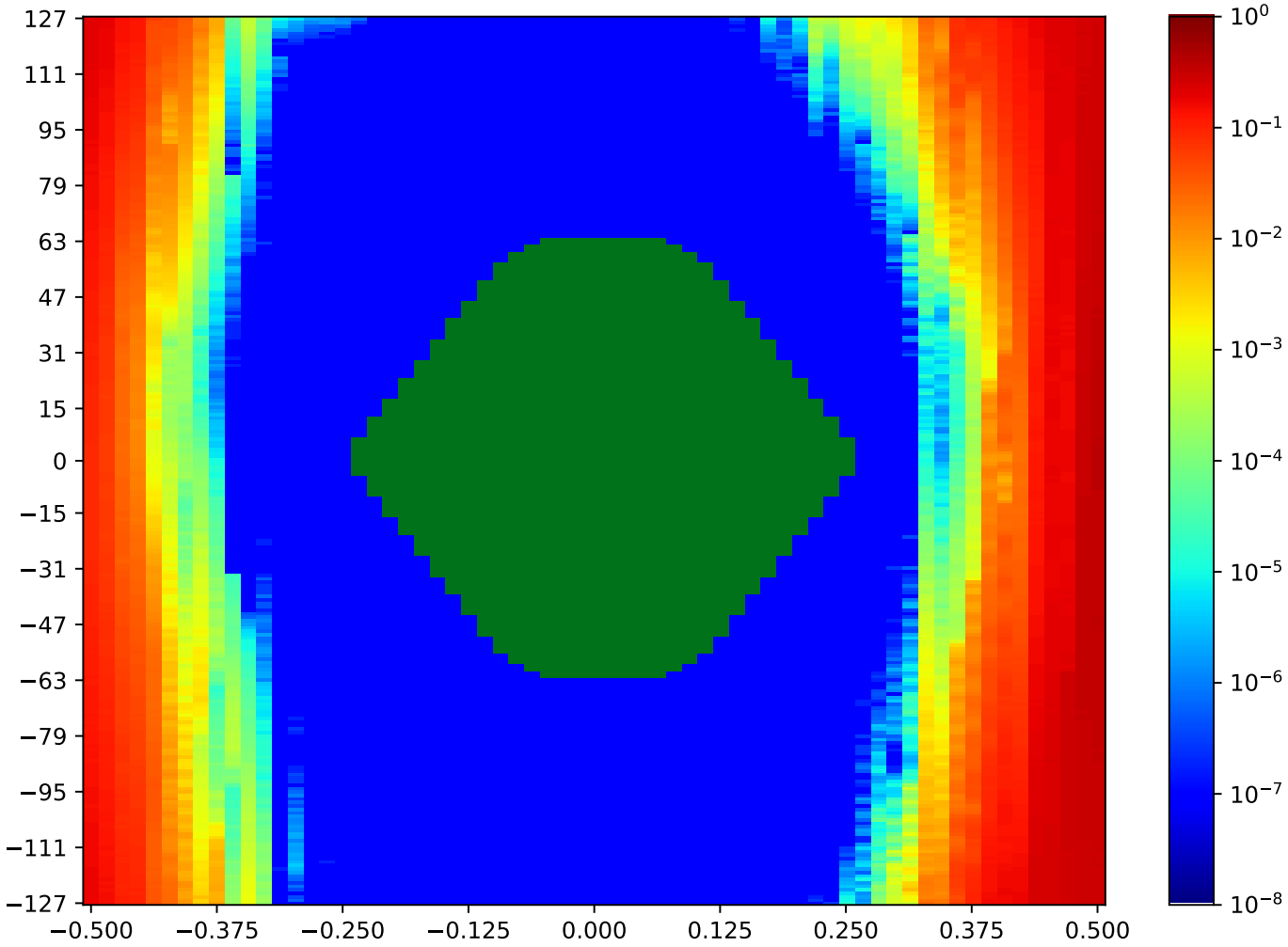


Figure 6.35: MSP_C_FPGA-TX3-07–RX6-07-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.9 MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Table 6.33: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:32:51		2019-Nov-26 17:33:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9348	42	64.62%	253	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

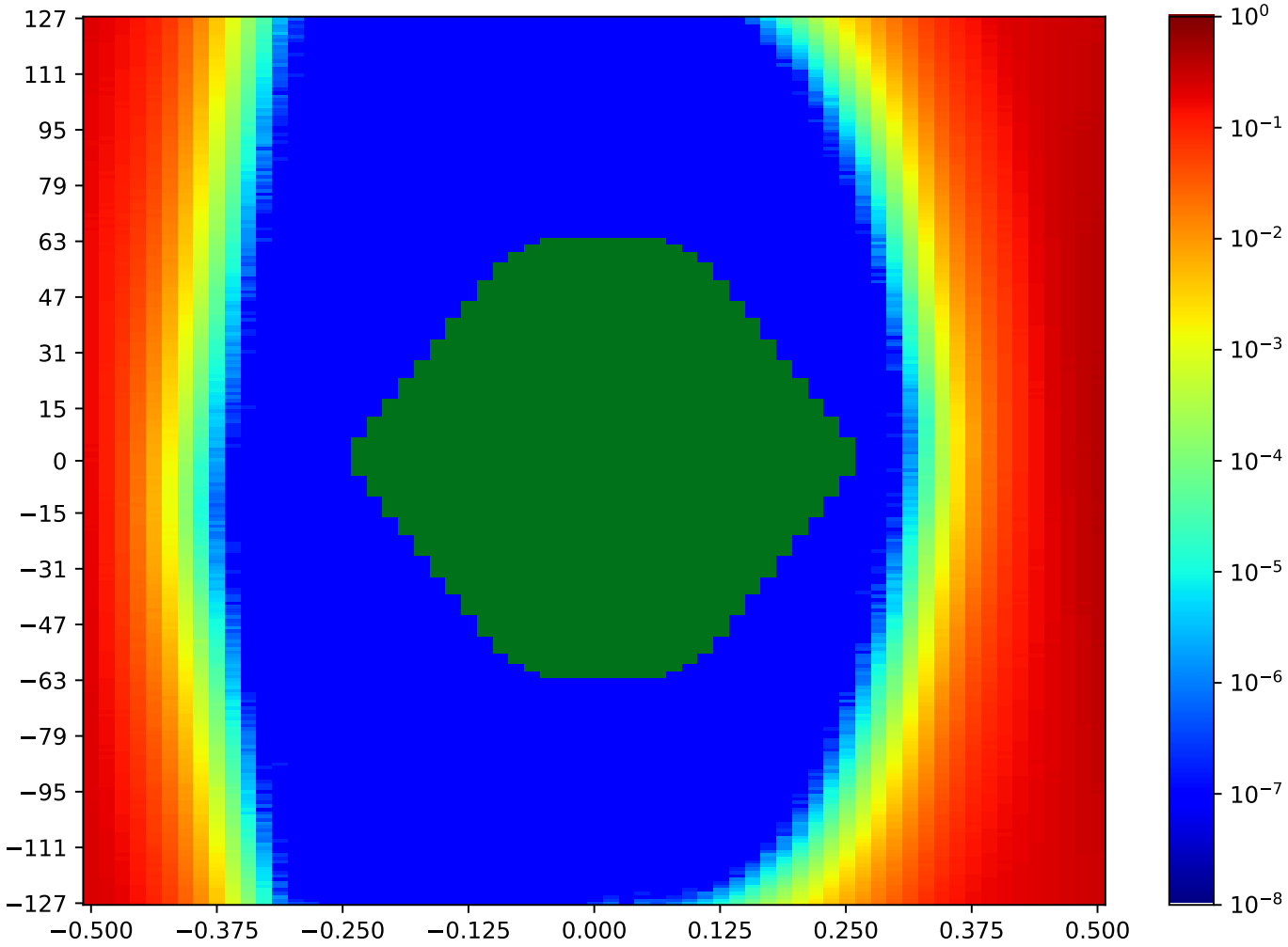


Figure 6.36: MSP_C_FPGA-TX3-08–RX6-08-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.10 MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Table 6.34: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:30:17		2019-Nov-26 17:30:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7907	39	60.00%	235	91.76%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

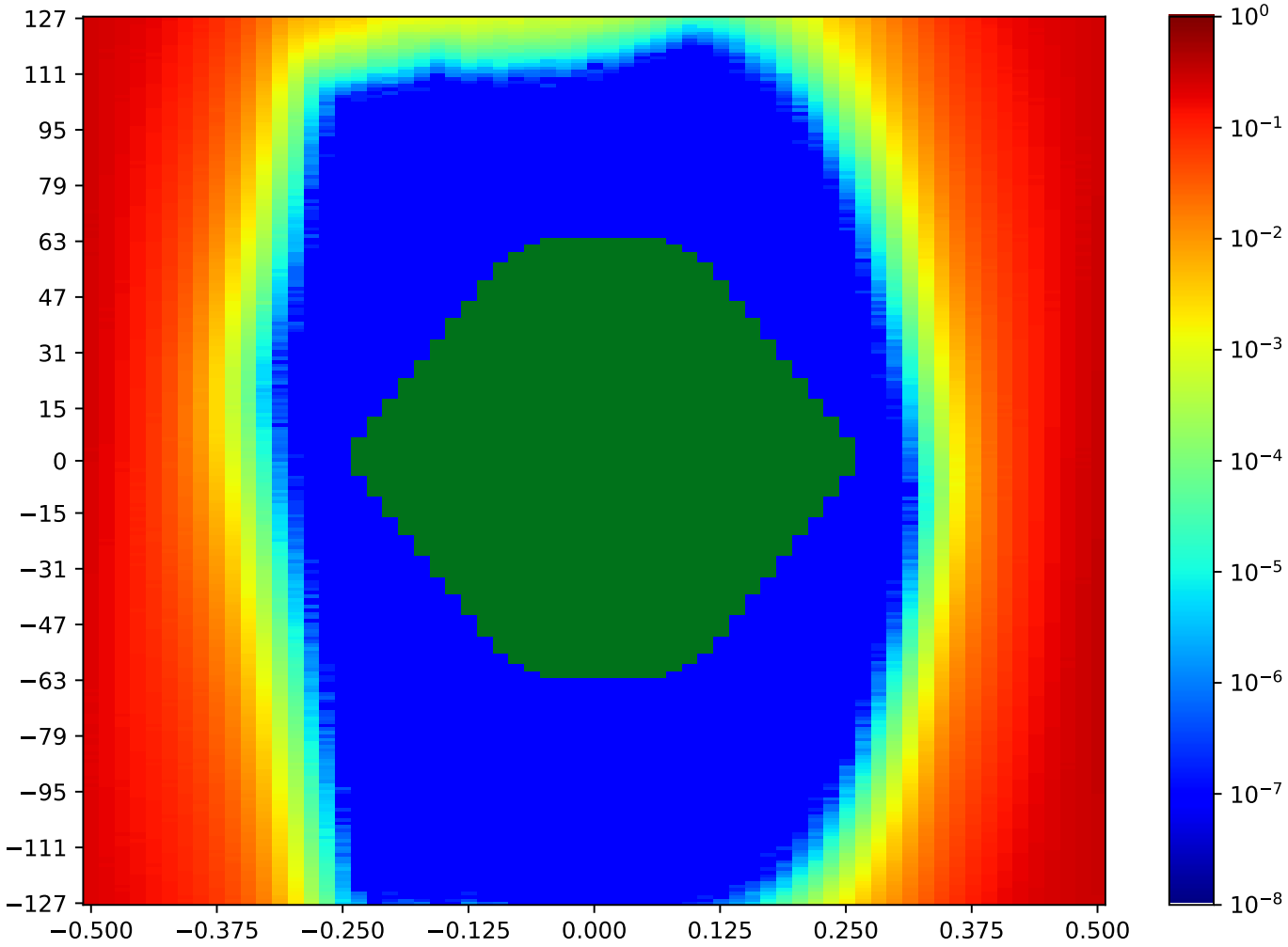


Figure 6.37: MSP_C_FPGA-TX3-09–RX6-09-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.11 MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Table 6.35: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:31:59		2019-Nov-26 17:32:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8336	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

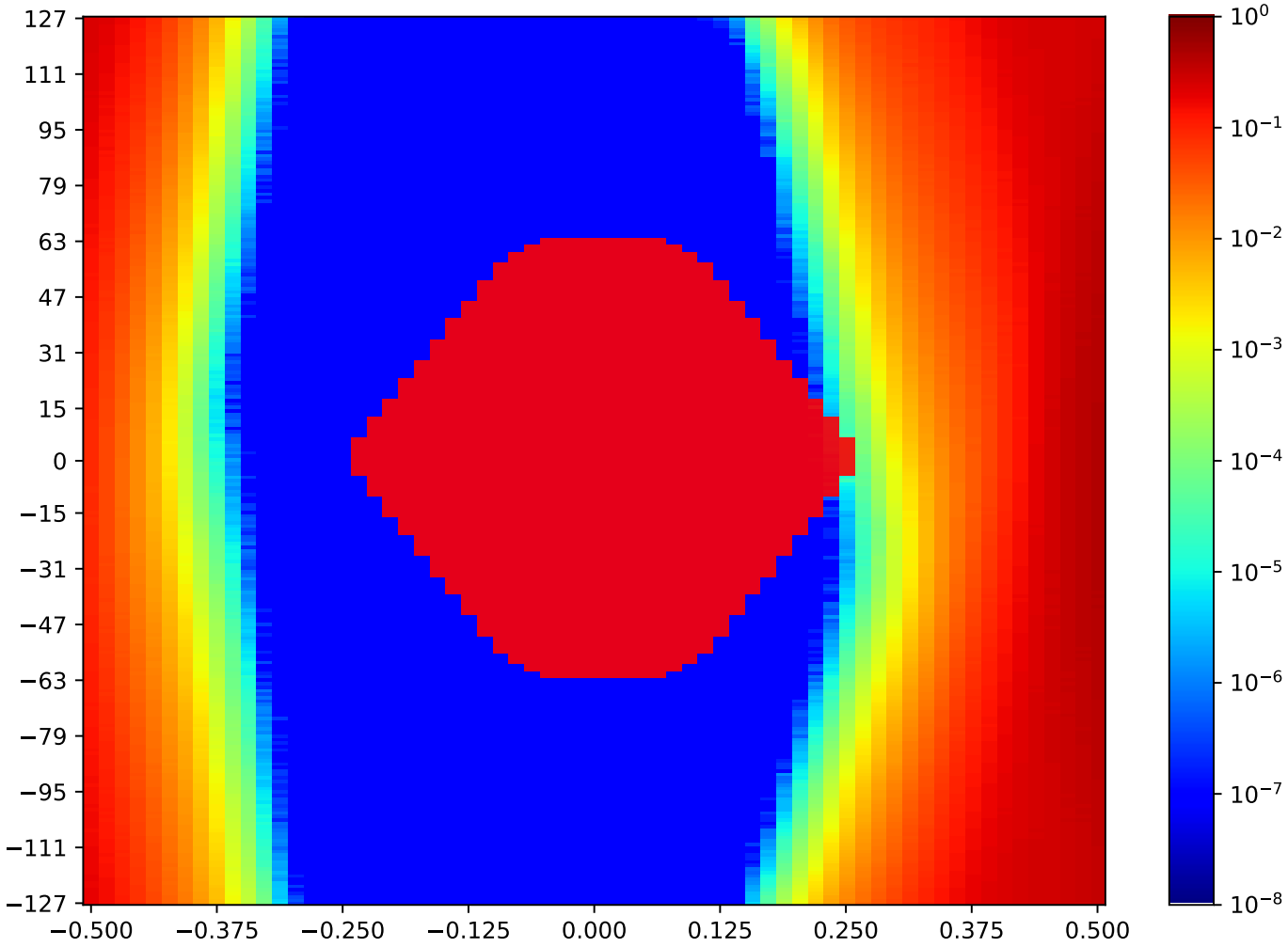


Figure 6.38: MSP_C_FPGA-TX3-10–RX6-10-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.3.12 MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Table 6.36: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:31:39		2019-Nov-26 17:31:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9338	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

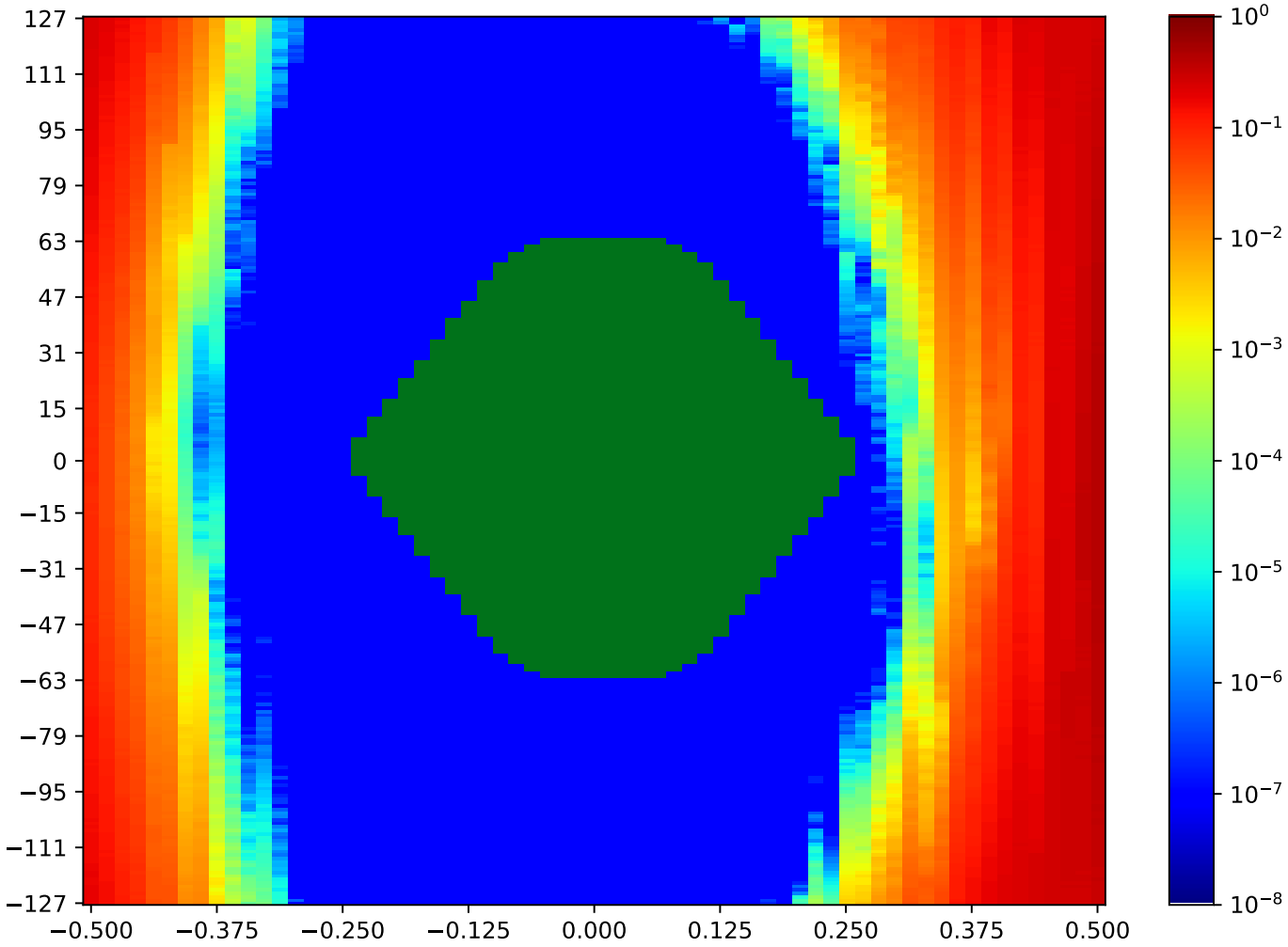


Figure 6.39: MSP_C_FPGA-TX3-11–RX6-11-MSP_A_FPGA

Call back to summary Figure 6.27. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4 MSP_C TX4 MSP_A RX7 Minipod Loopback

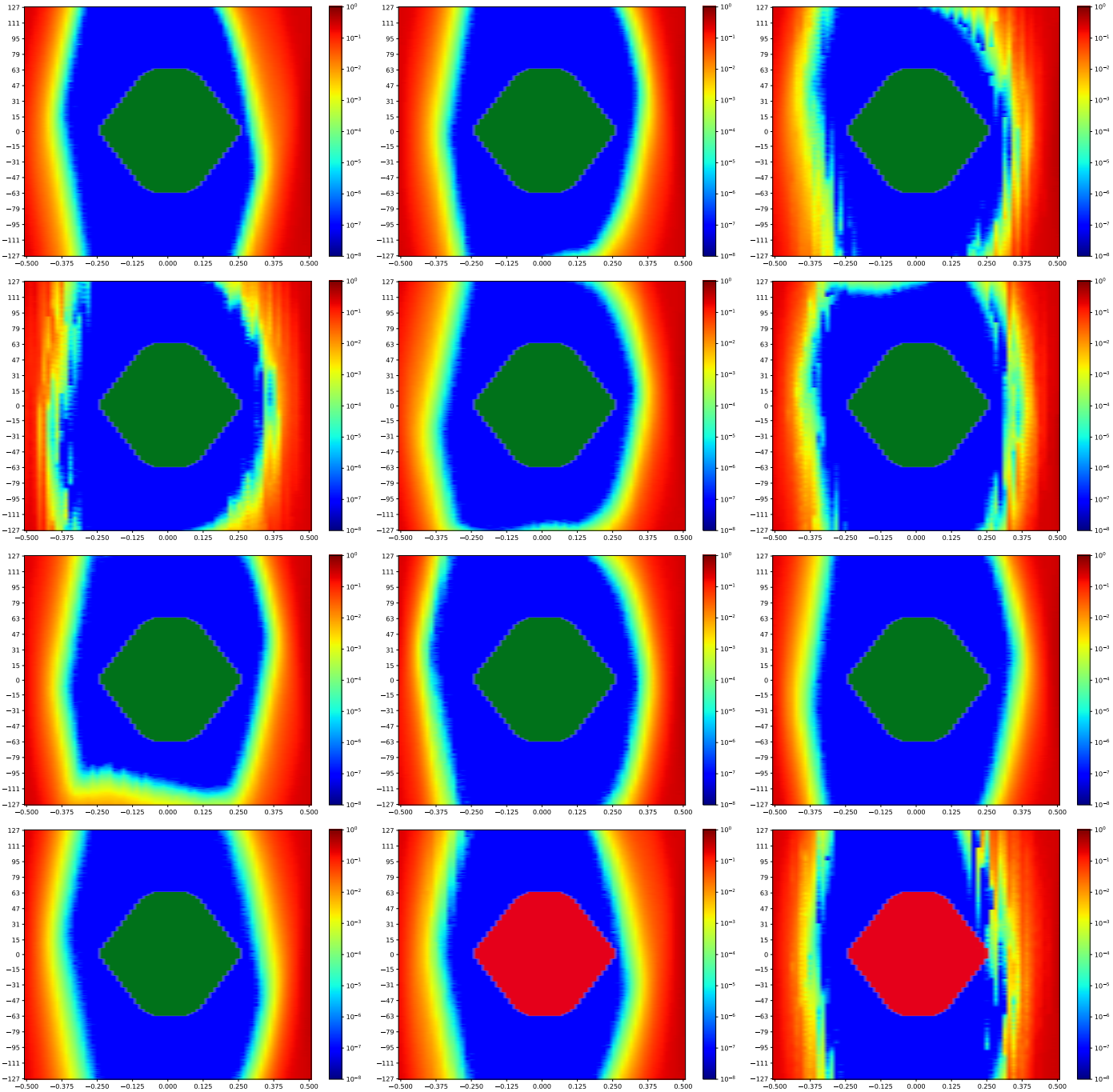


Figure 6.40: MSP_C TX4 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.53.

6.4.1 MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Table 6.37: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:34:50		2019-Nov-26 17:35:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9022	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

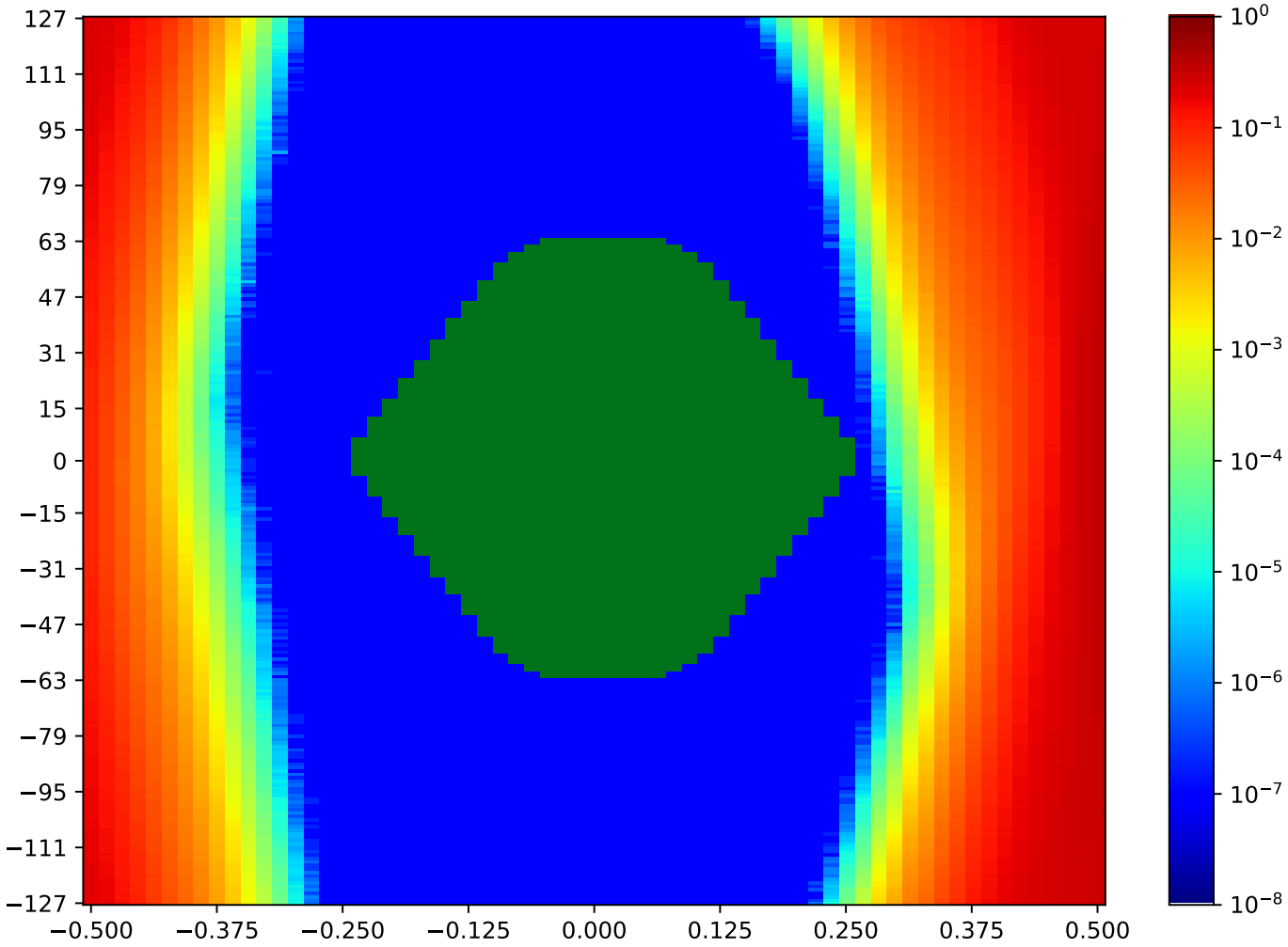


Figure 6.41: MSP_C_FPGA-TX4-00–RX7-00-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.2 MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Table 6.38: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:34:04		2019-Nov-26 17:34:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8758	40	61.54%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

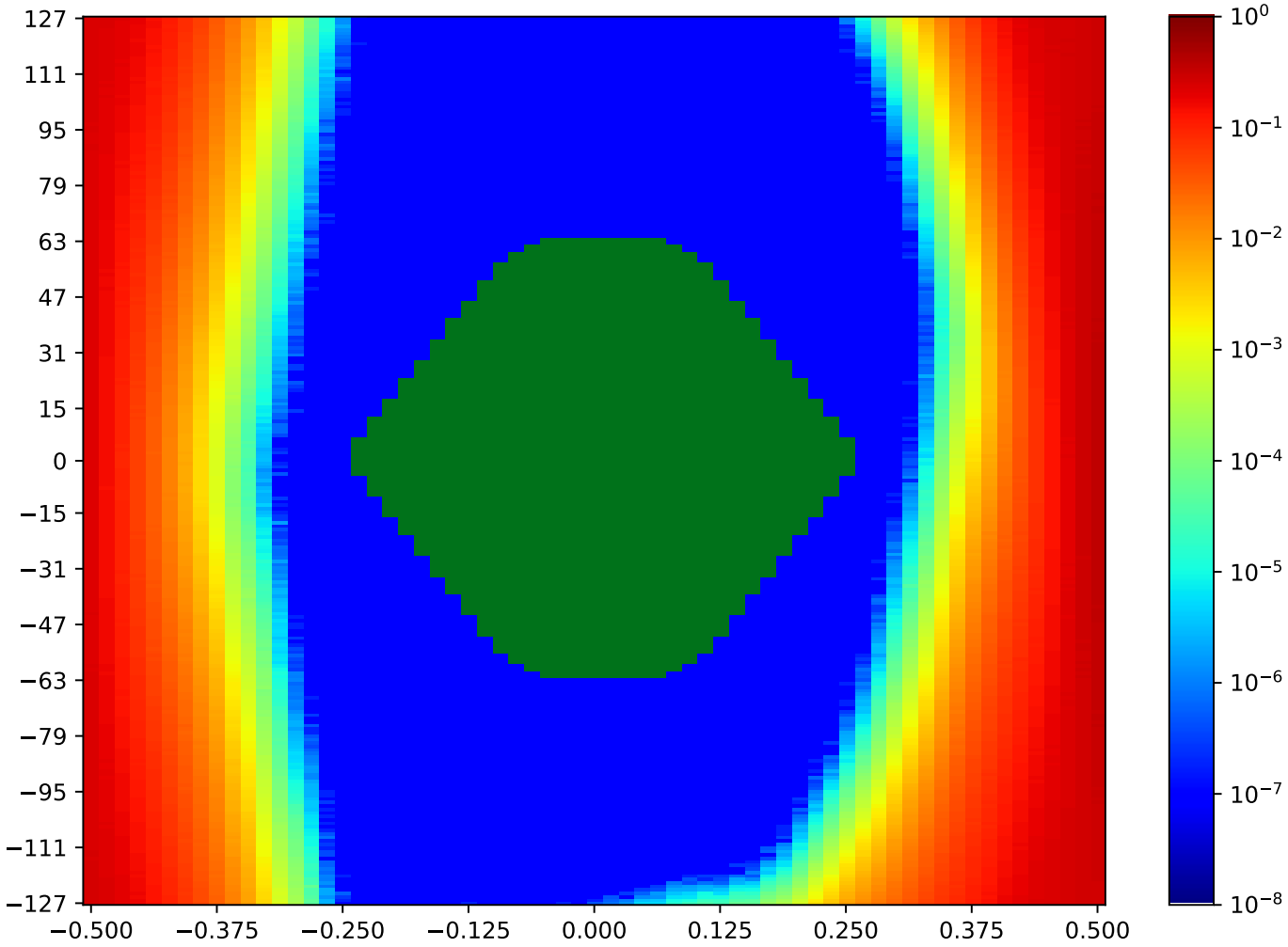


Figure 6.42: MSP_C_FPGA-TX4-01–RX7-01-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.3 MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Table 6.39: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:36:11		2019-Nov-26 17:36:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8413	40	60.00%	254	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

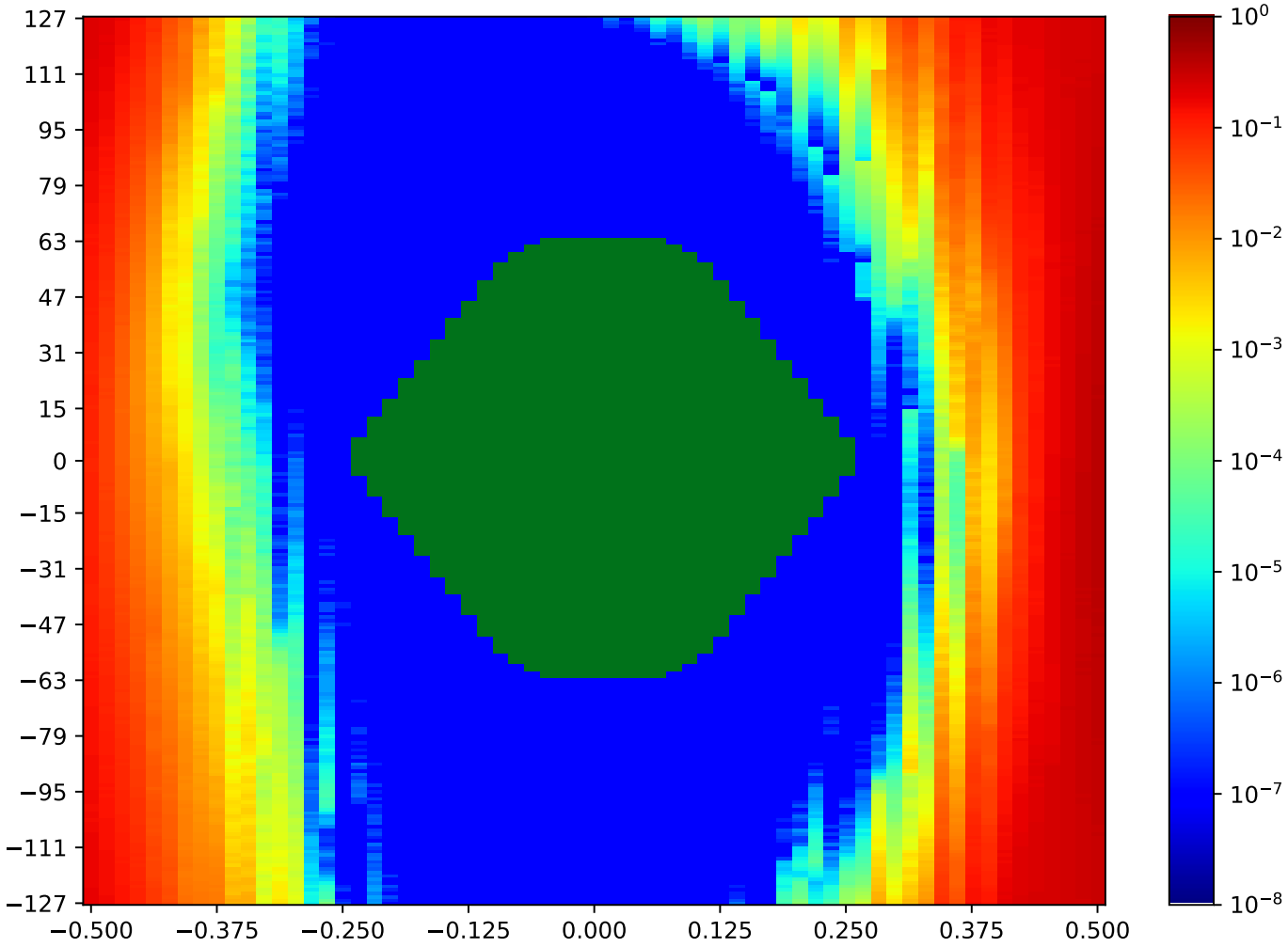


Figure 6.43: MSP_C_FPGA-TX4-02–RX7-02-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.4 MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Table 6.40: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:33:44		2019-Nov-26 17:34:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9343	42	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

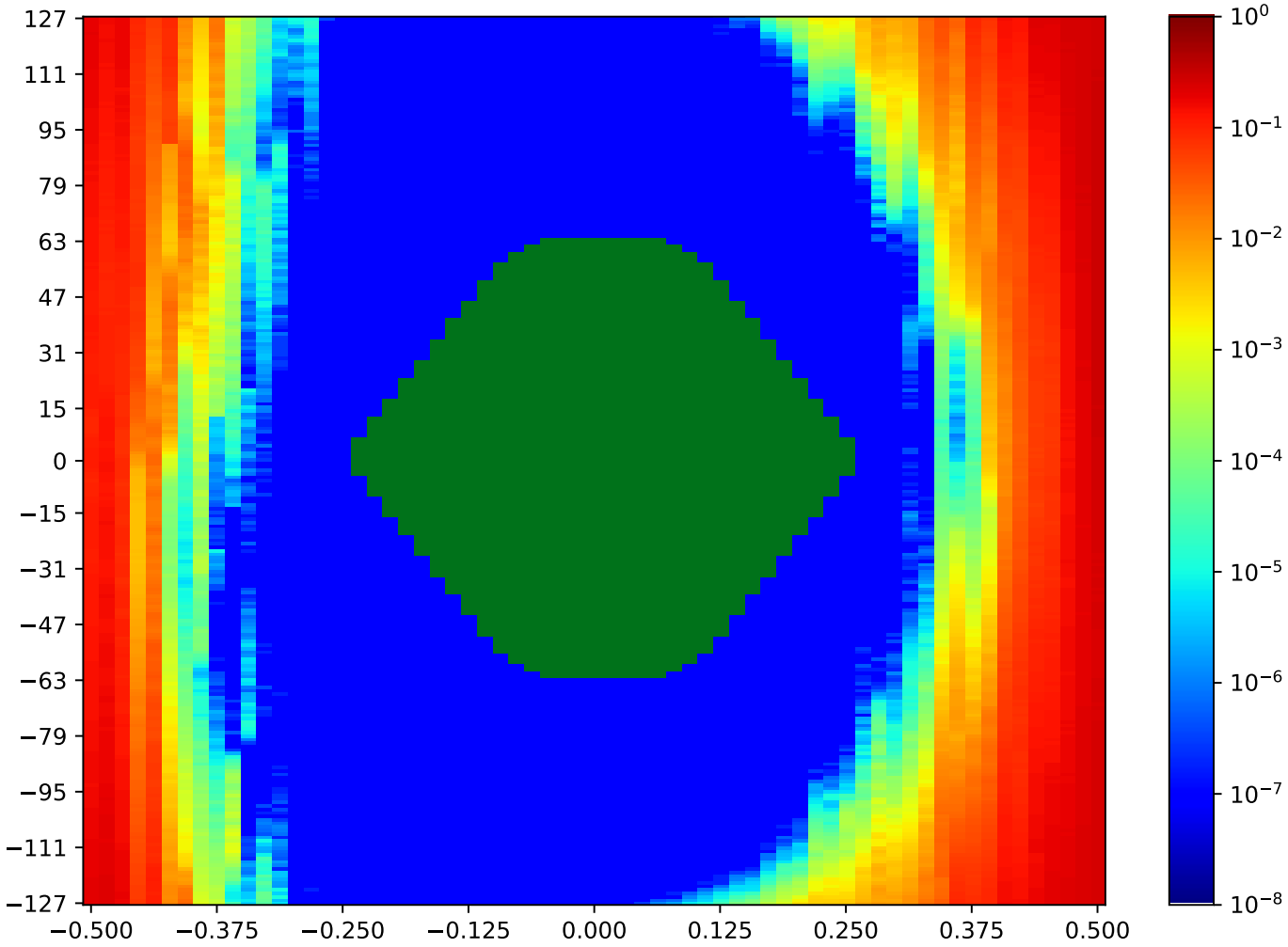


Figure 6.44: MSP_C_FPGA-TX4-03–RX7-03-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.5 MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Table 6.41: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:37:22		2019-Nov-26 17:37:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8470	39	60.00%	244	95.29%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

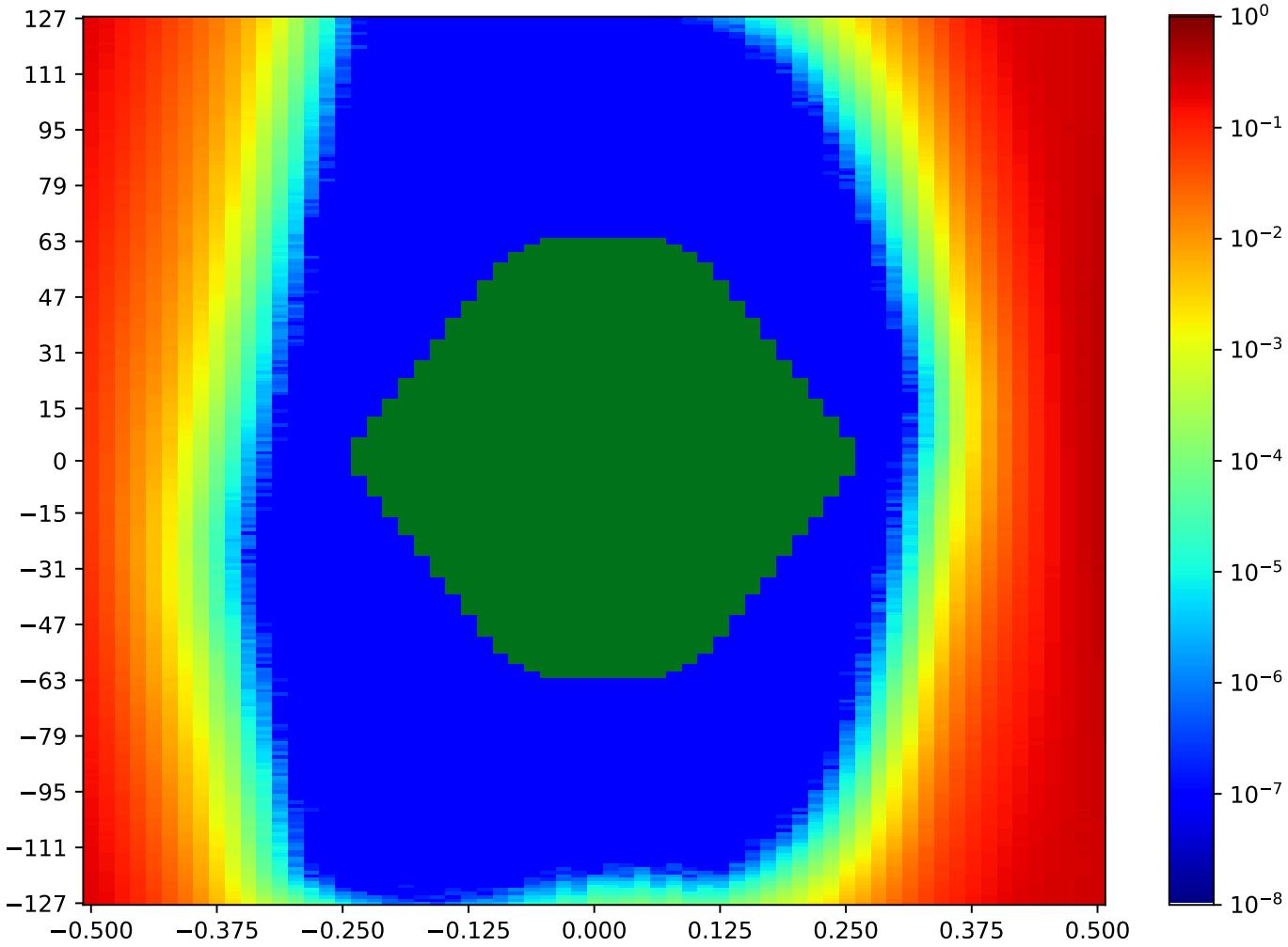


Figure 6.45: MSP_C_FPGA-TX4-04–RX7-04-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.6 MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Table 6.42: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:34:23		2019-Nov-26 17:34:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9046	41	63.08%	245	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

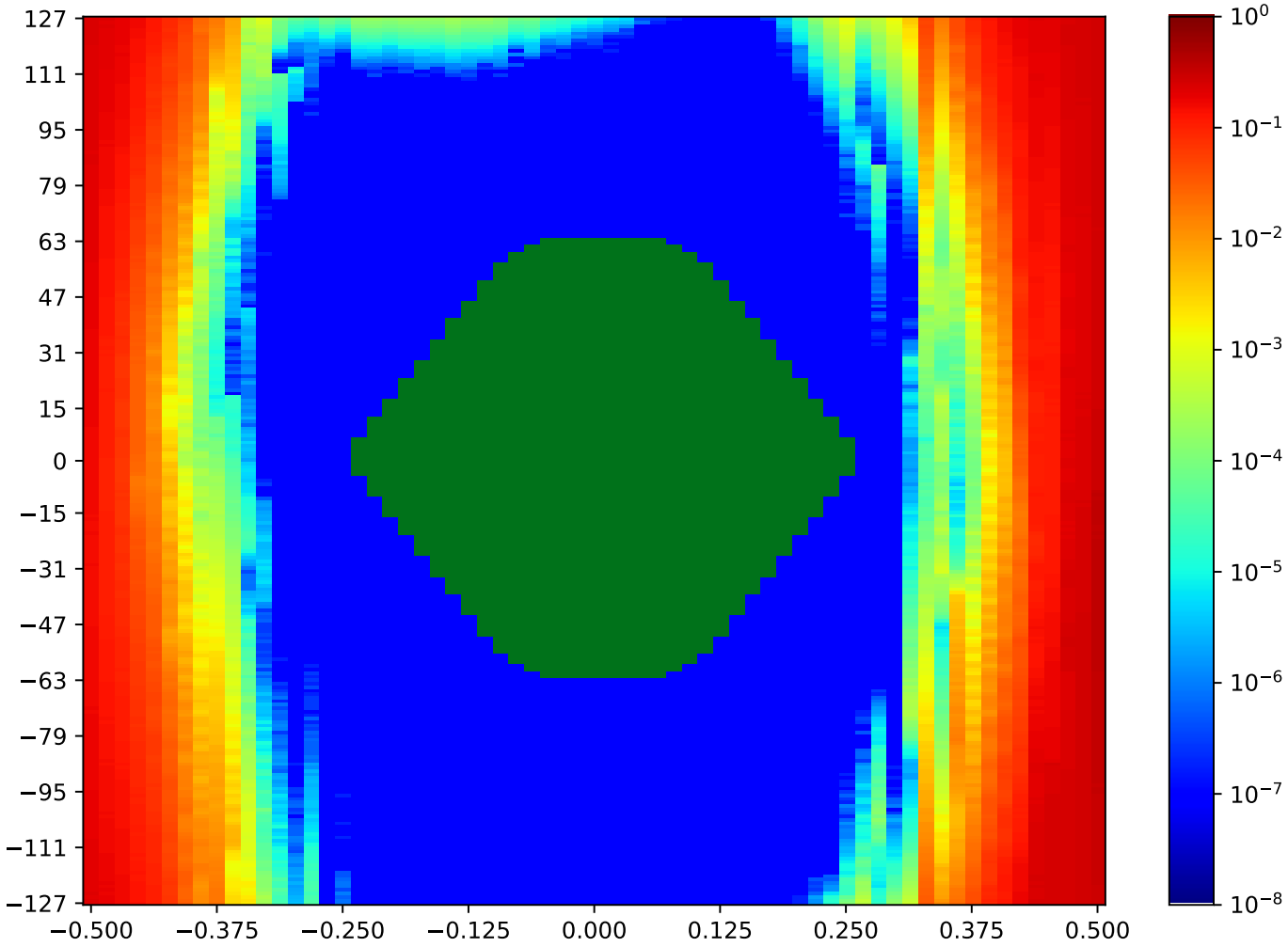


Figure 6.46: MSP_C_FPGA-TX4-05–RX7-05-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.7 MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Table 6.43: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:38:17		2019-Nov-26 17:38:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8305	41	63.08%	228	88.63%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

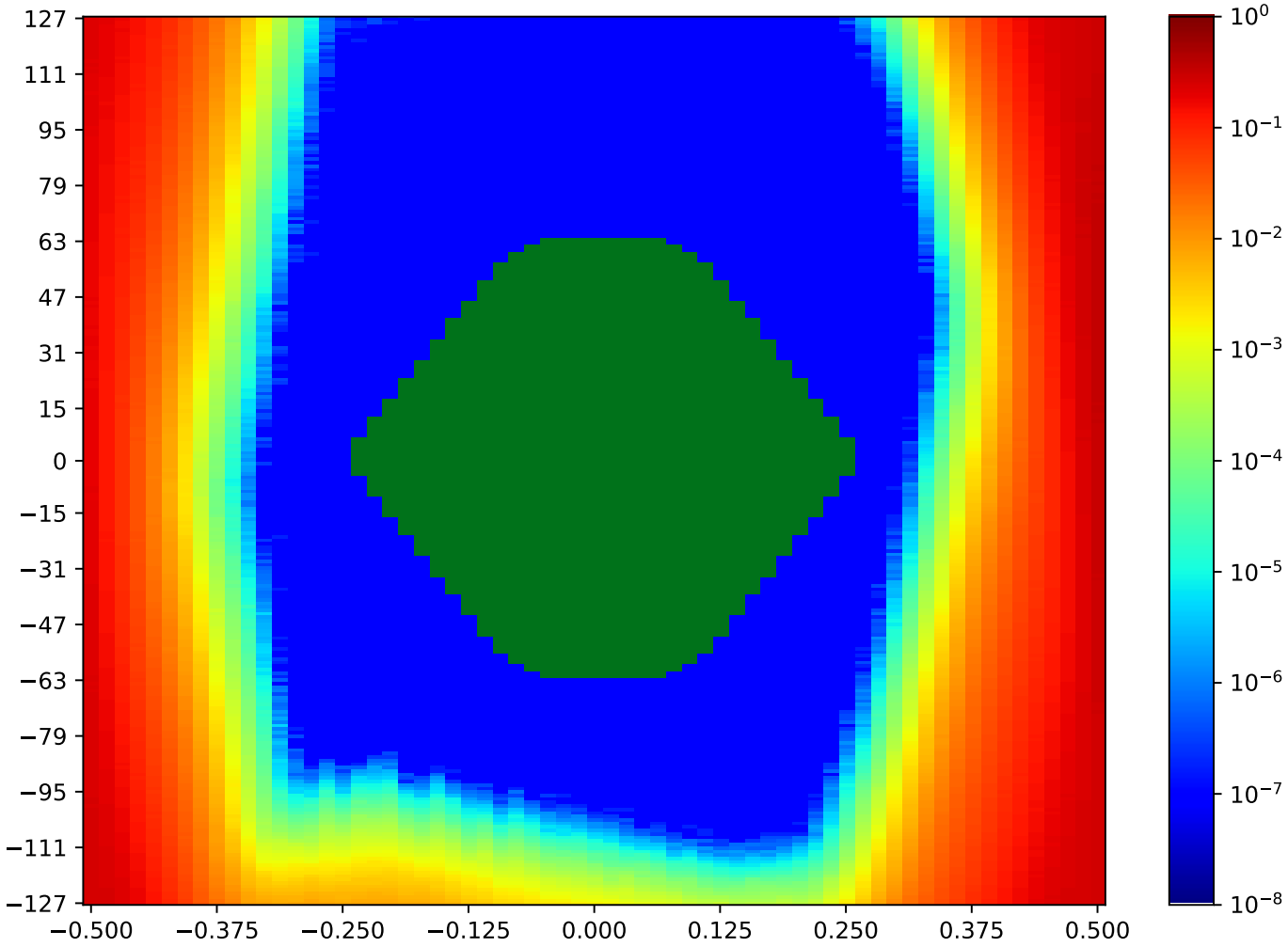


Figure 6.47: MSP_C_FPGA-TX4-06–RX7-06-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.8 MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Table 6.44: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:35:15		2019-Nov-26 17:35:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9676	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

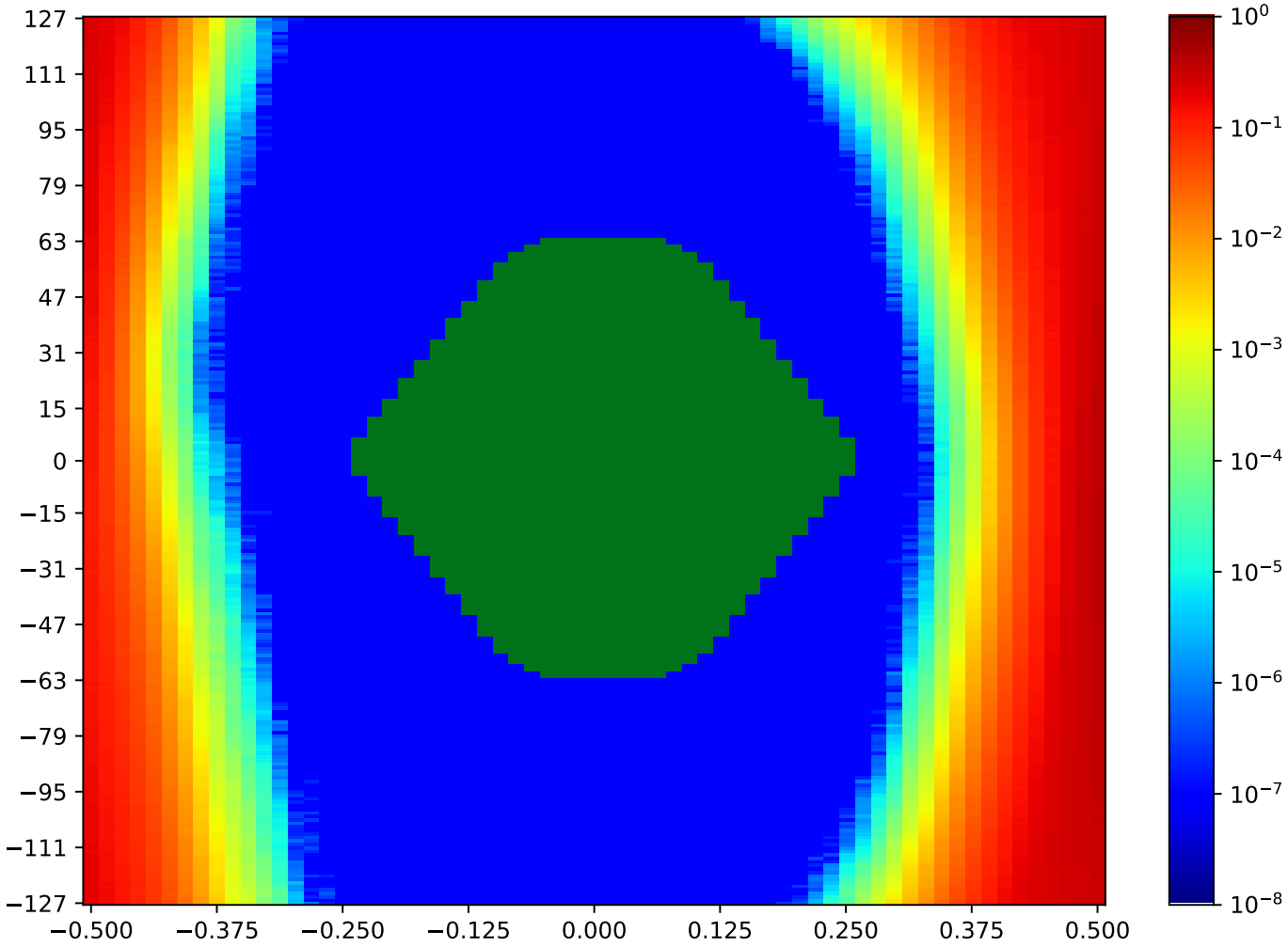


Figure 6.48: MSP_C_FPGA-TX4-07–RX7-07-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.9 MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Table 6.45: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:37:49		2019-Nov-26 17:38:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9618	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

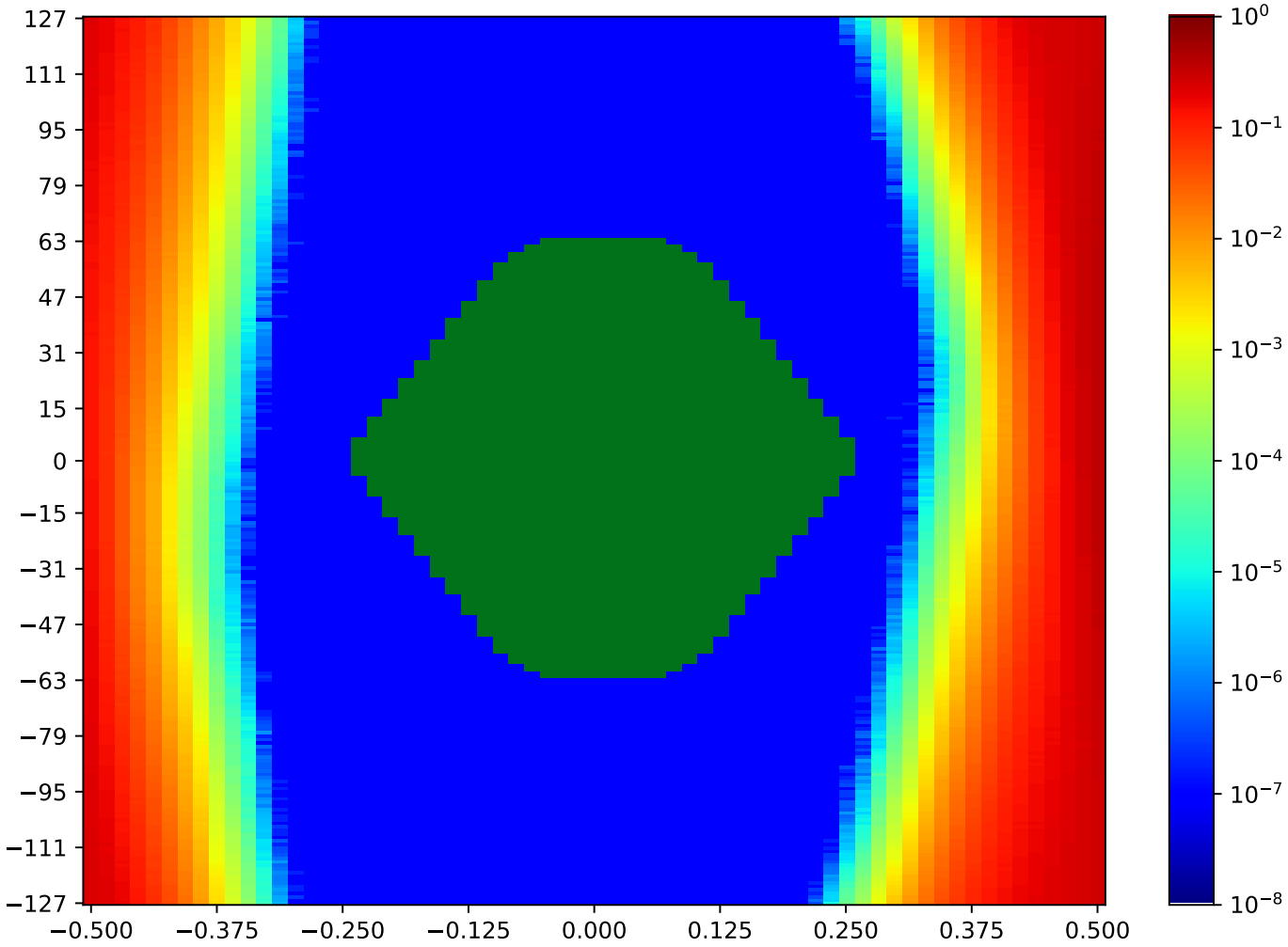


Figure 6.49: MSP_C_FPGA-TX4-08–RX7-08-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.10 MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Table 6.46: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:35:43		2019-Nov-26 17:36:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8959	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

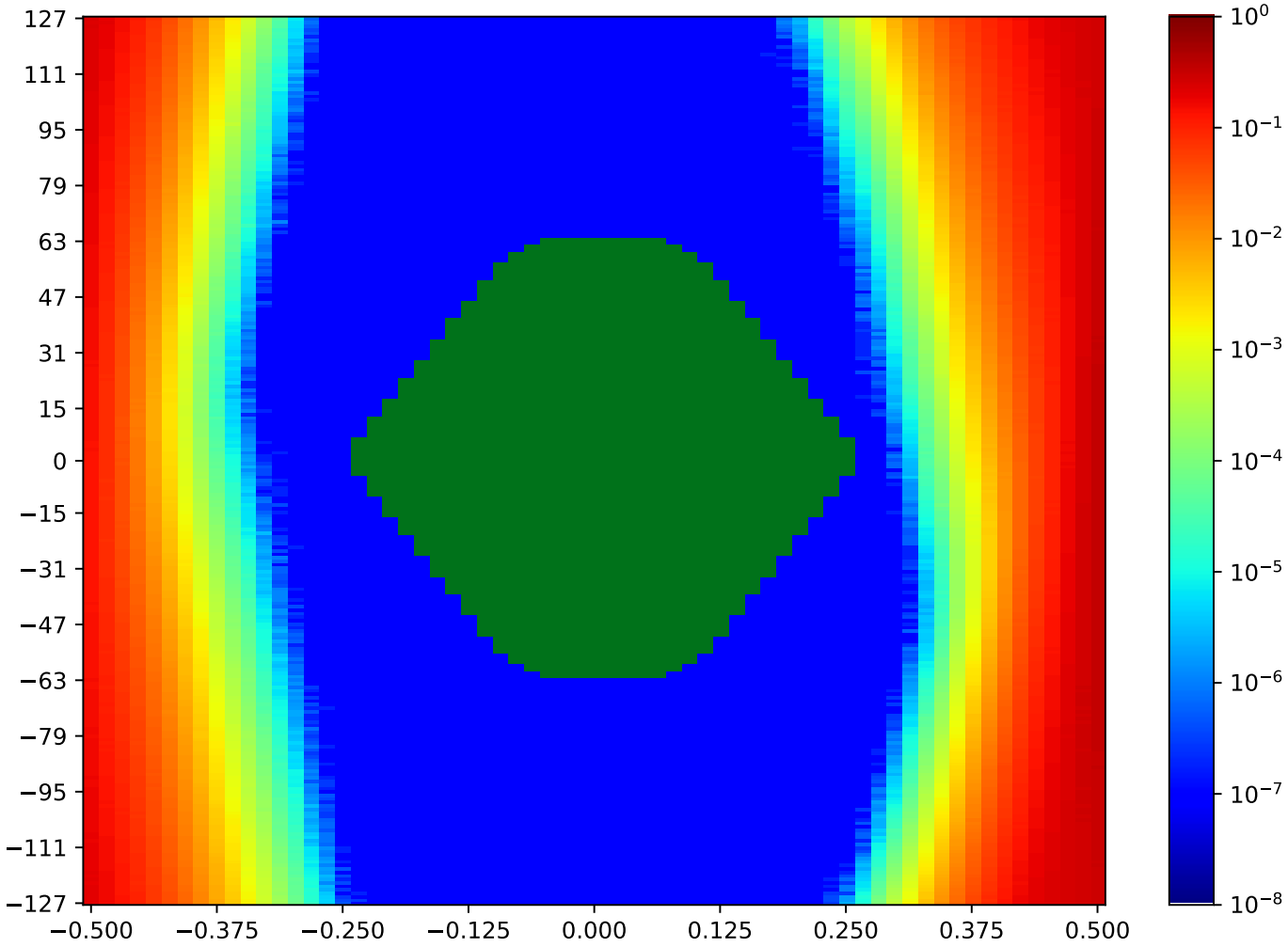


Figure 6.50: MSP_C_FPGA-TX4-09–RX7-09-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.11 MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Table 6.47: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:36:57		2019-Nov-26 17:37:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8310	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

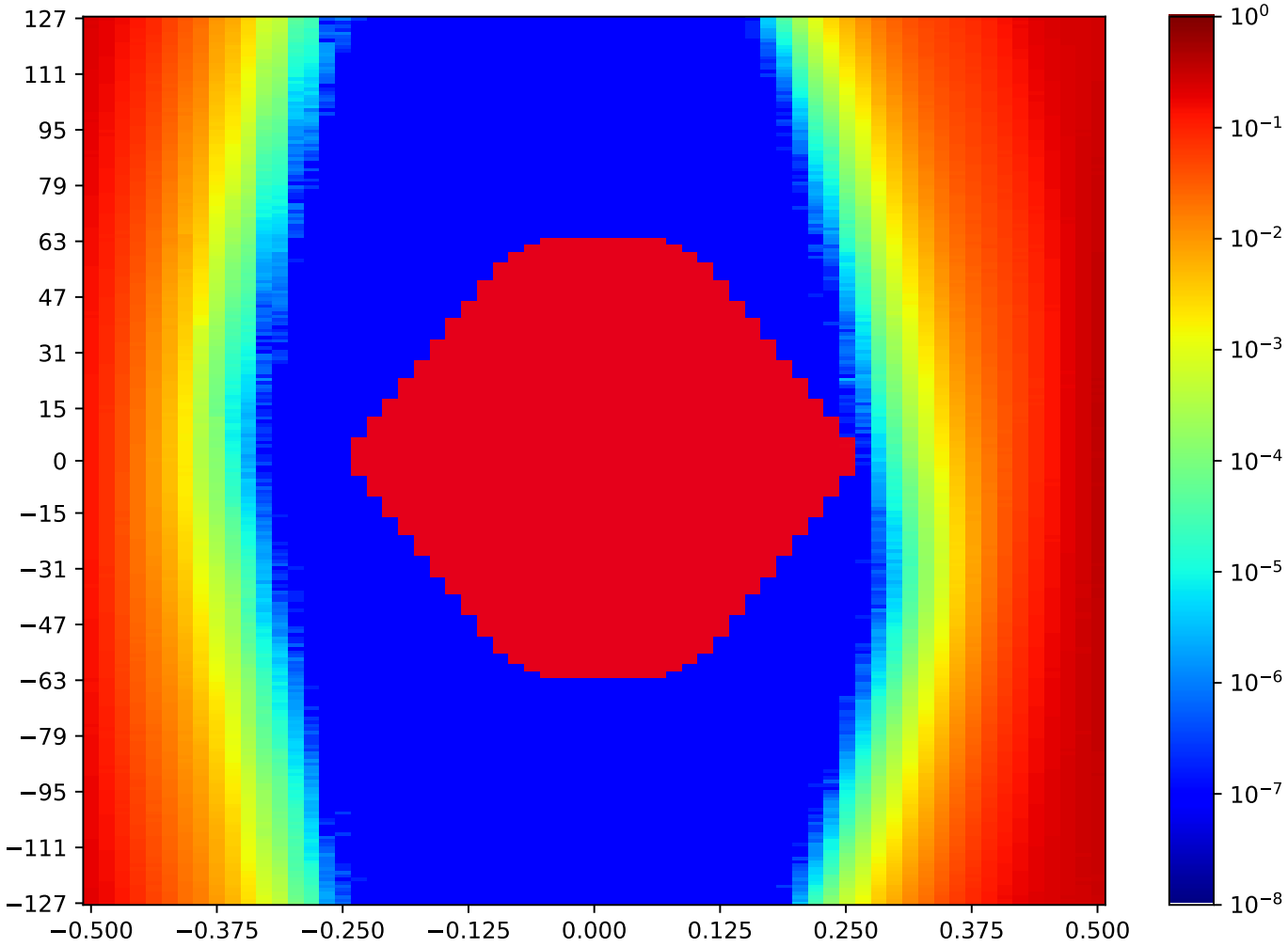


Figure 6.51: MSP_C_FPGA-TX4-10–RX7-10-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.4.12 MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Table 6.48: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:36:38		2019-Nov-26 17:36:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8916	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

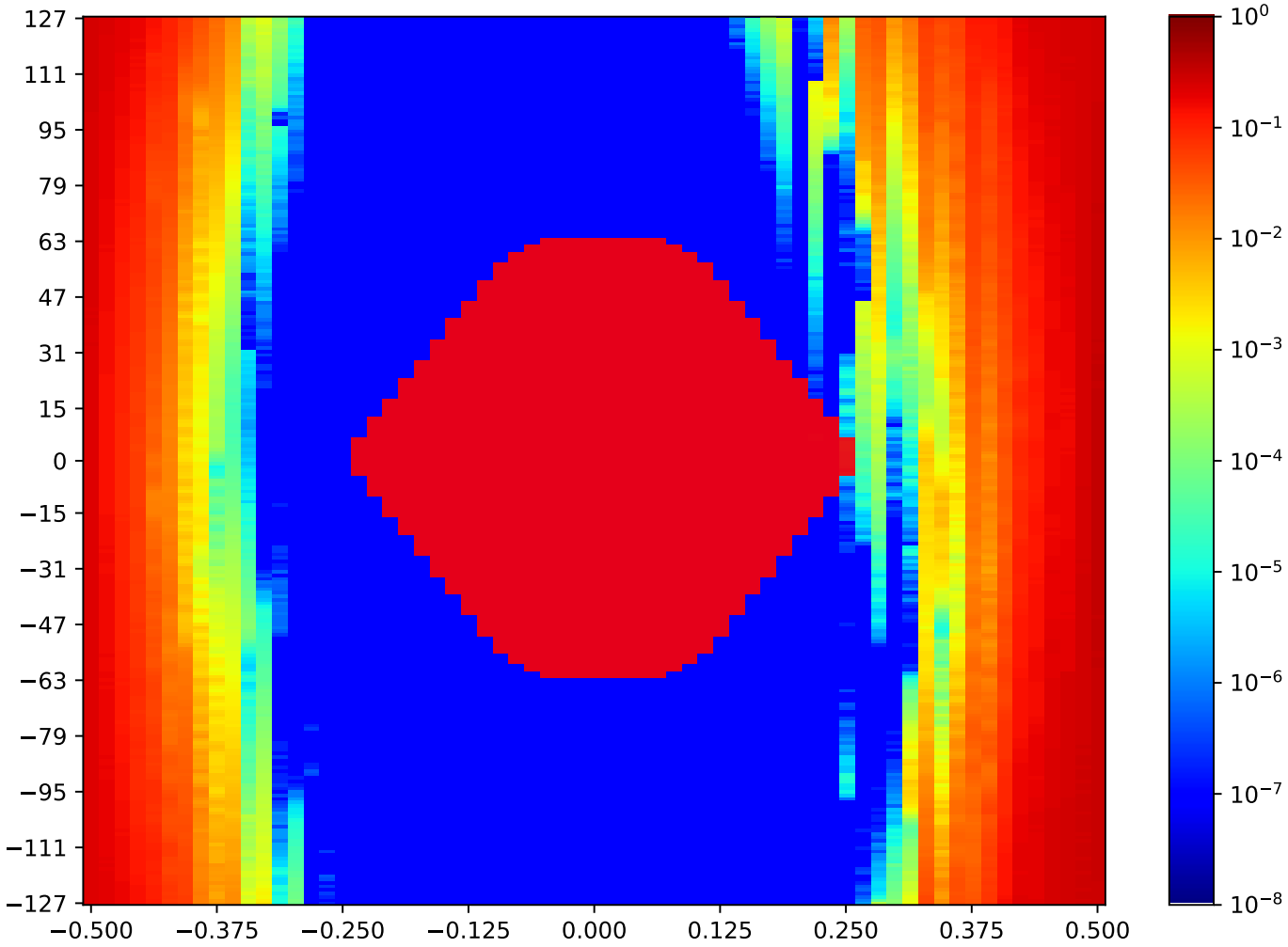


Figure 6.52: MSP_C_FPGA-TX4-11–RX7-11-MSP_A_FPGA

Call back to summary Figure 6.40. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.62.

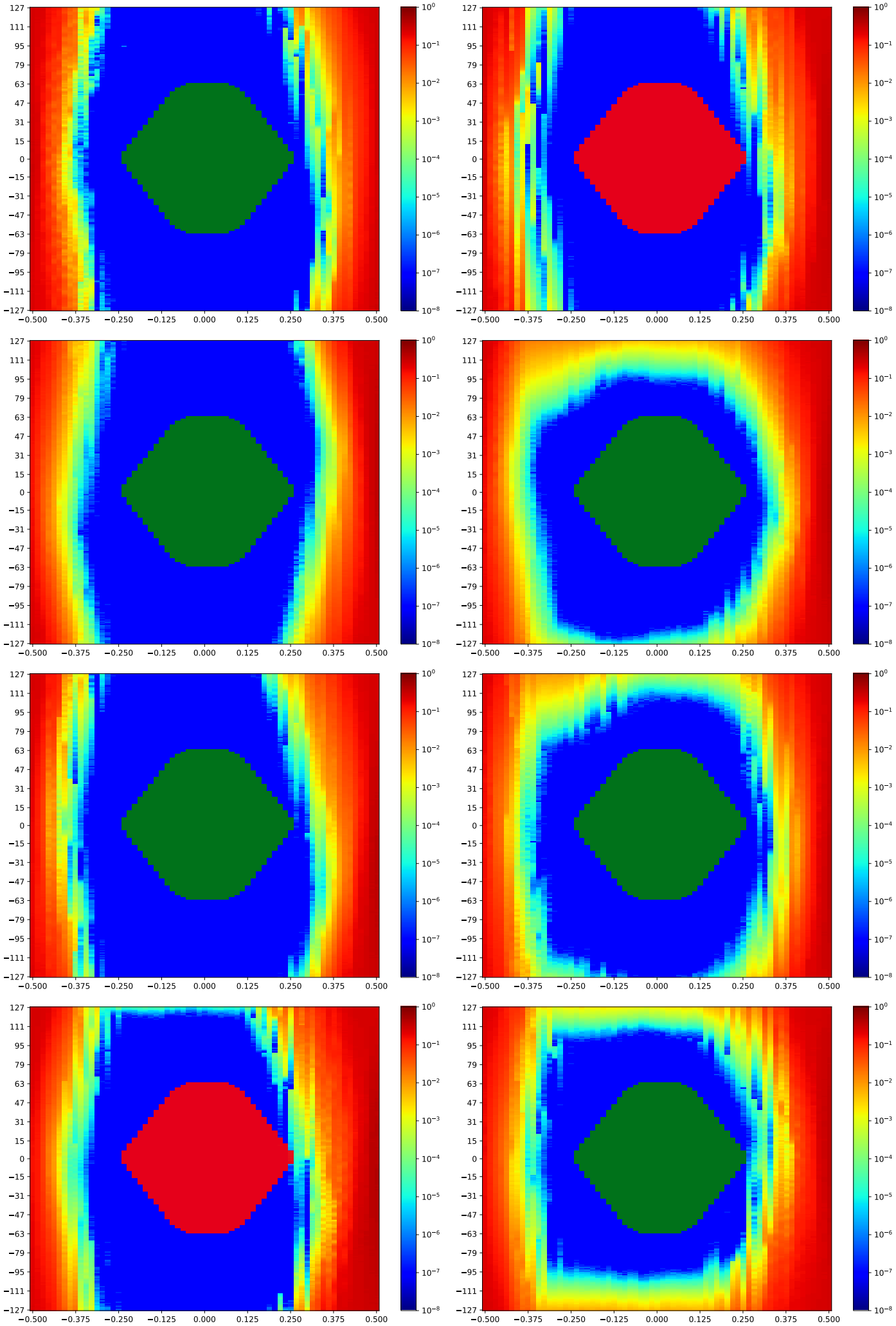


Figure 6.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

6.5.1 TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Table 6.49: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:40:06		2019-Nov-26 17:40:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9507	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

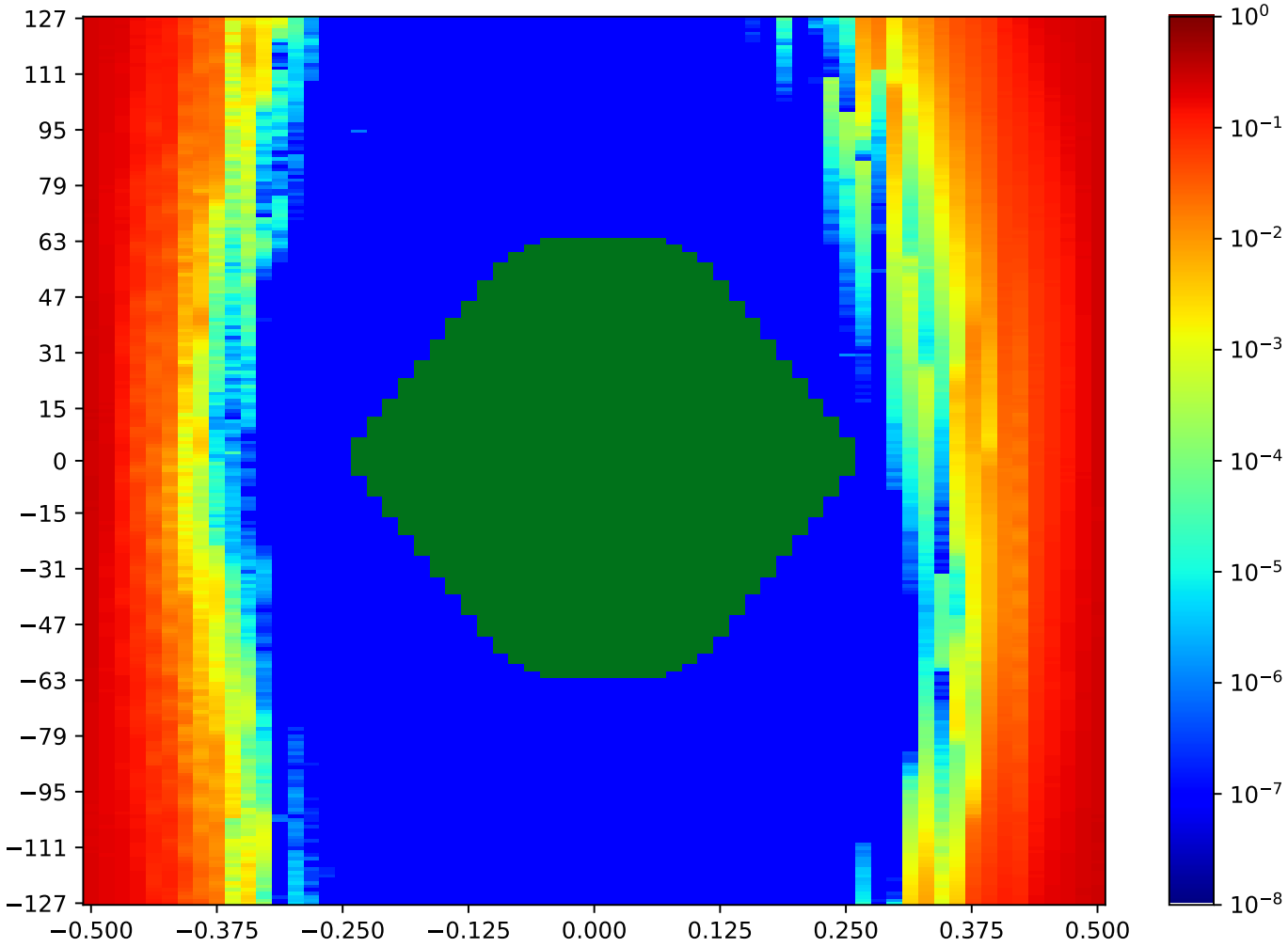


Figure 6.54: TRP_FPGA-TX5-00–RX5-00-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.2 TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Table 6.50: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:39:12		2019-Nov-26 17:39:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8577	39	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

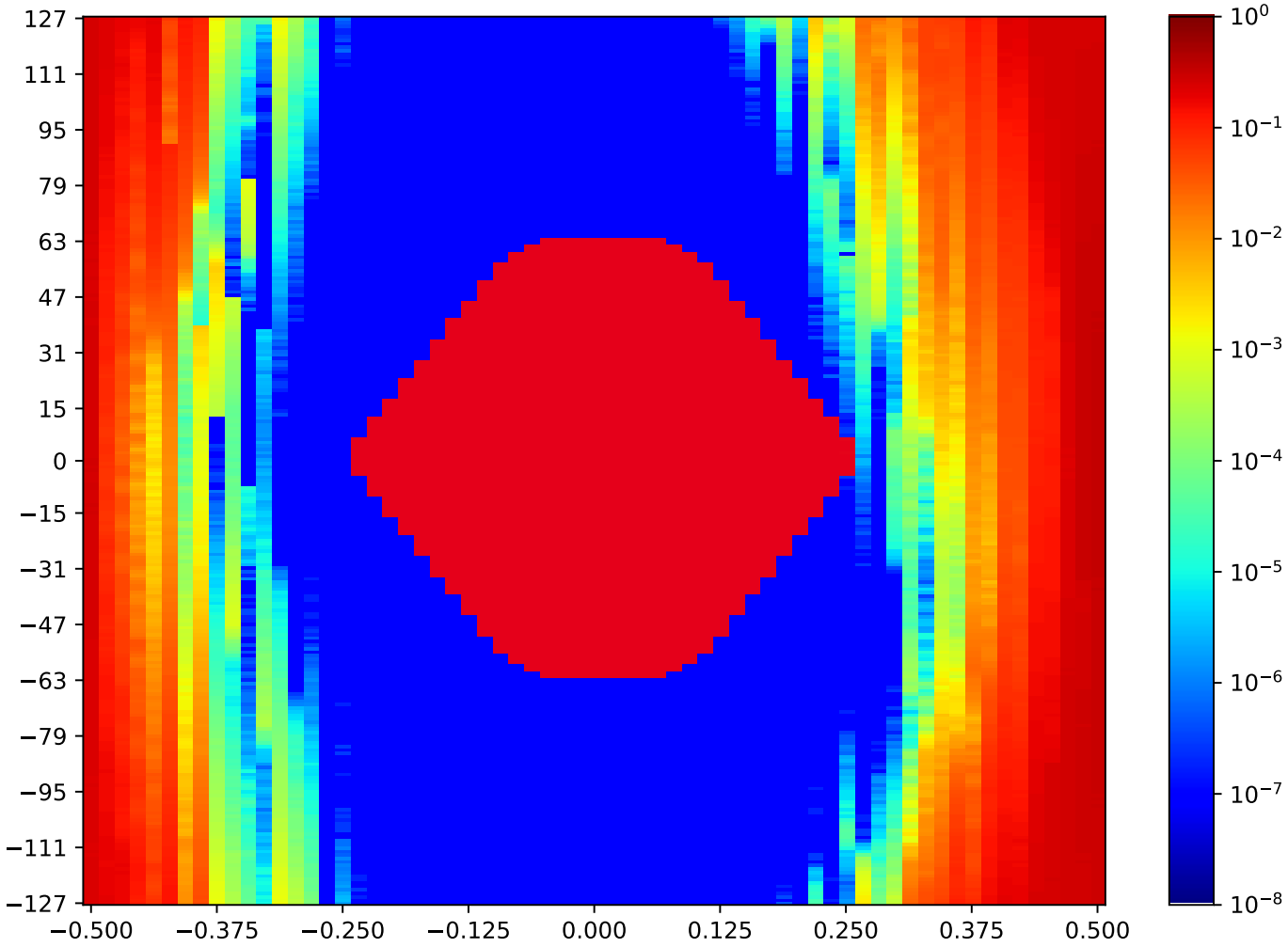


Figure 6.55: TRP_FPGA-TX5-01–RX5-01-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.3 TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Table 6.51: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:40:53		2019-Nov-26 17:41:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9209	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

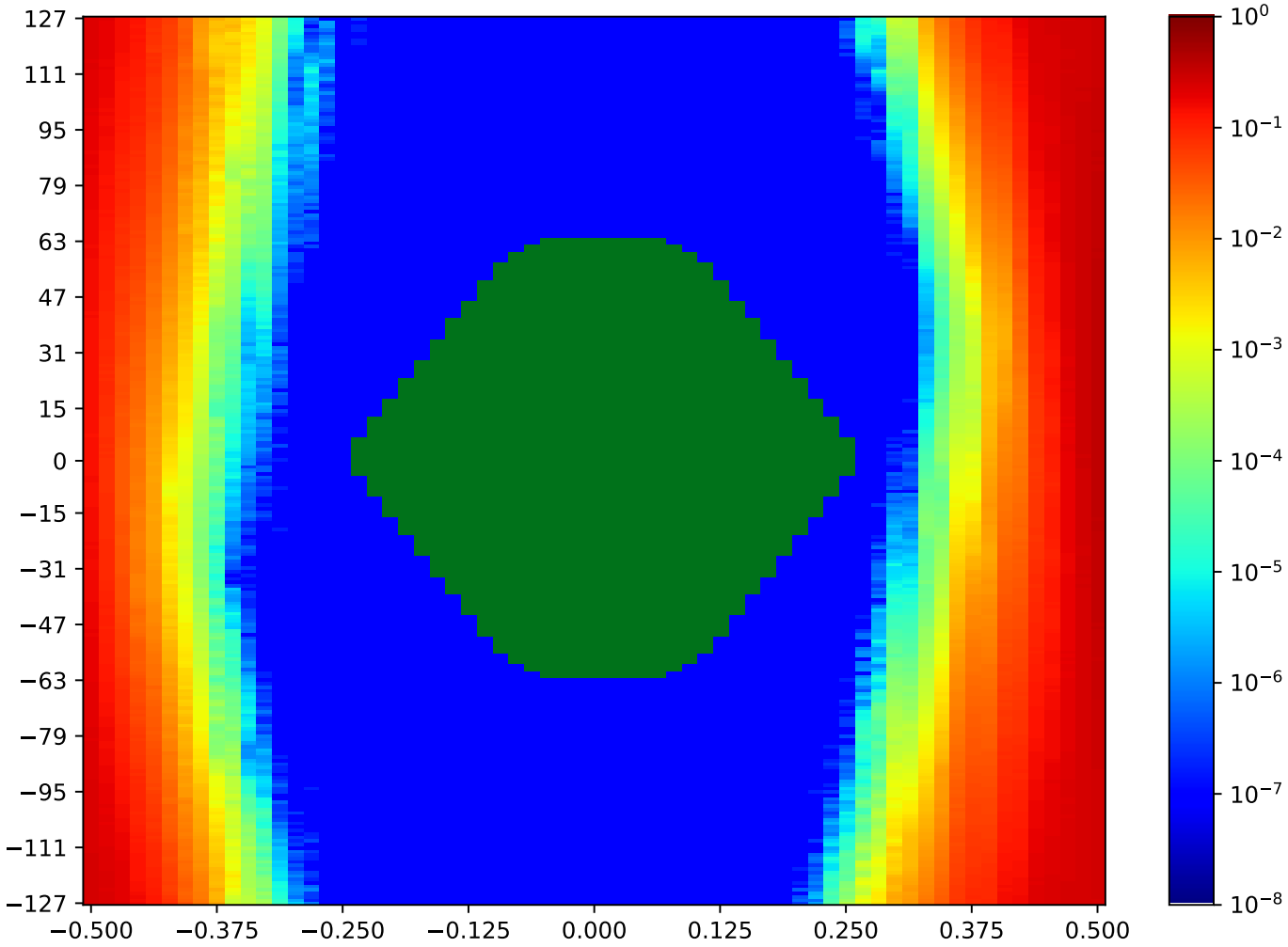


Figure 6.56: TRP_FPGA-TX5-02–RX5-02-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.4 TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Table 6.52: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:39:38		2019-Nov-26 17:40:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6912	40	61.54%	203	79.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

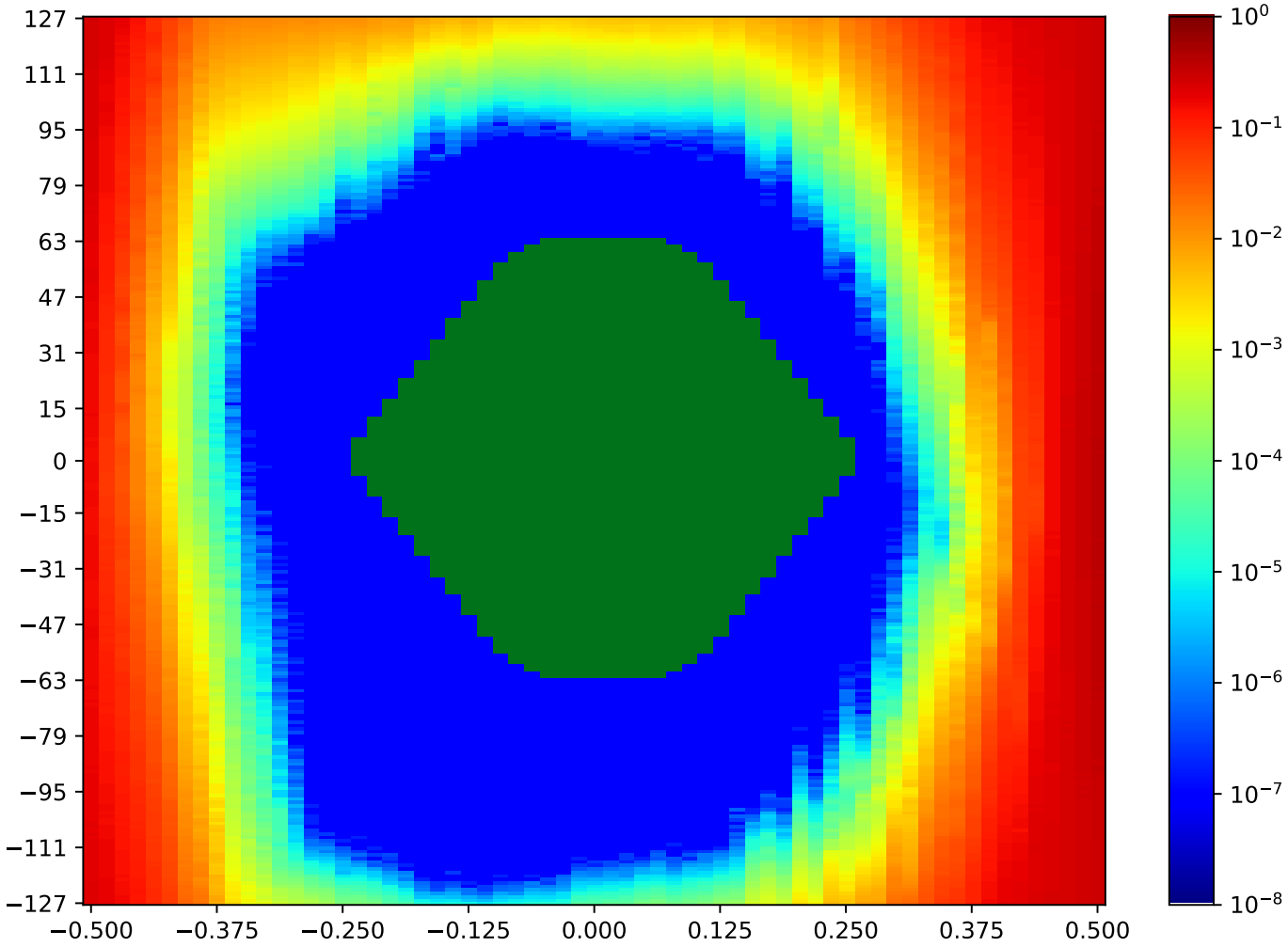


Figure 6.57: TRP_FPGA-TX5-03–RX5-03-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.5 TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Table 6.53: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:41:47		2019-Nov-26 17:42:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9314	40	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

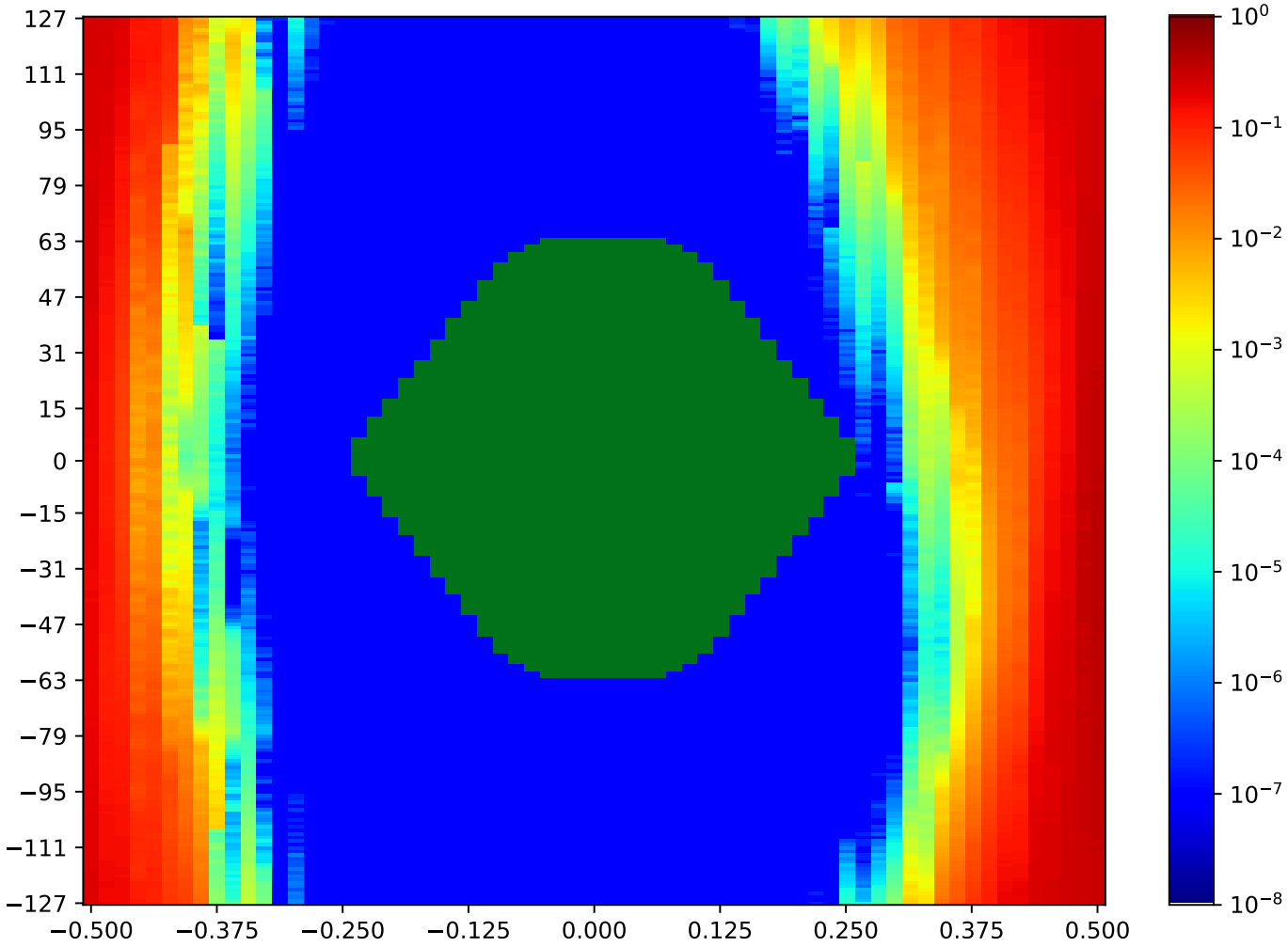


Figure 6.58: TRP_FPGA-TX5-04–RX5-04-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.6 TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Table 6.54: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:38:45		2019-Nov-26 17:39:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7562	39	60.00%	229	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

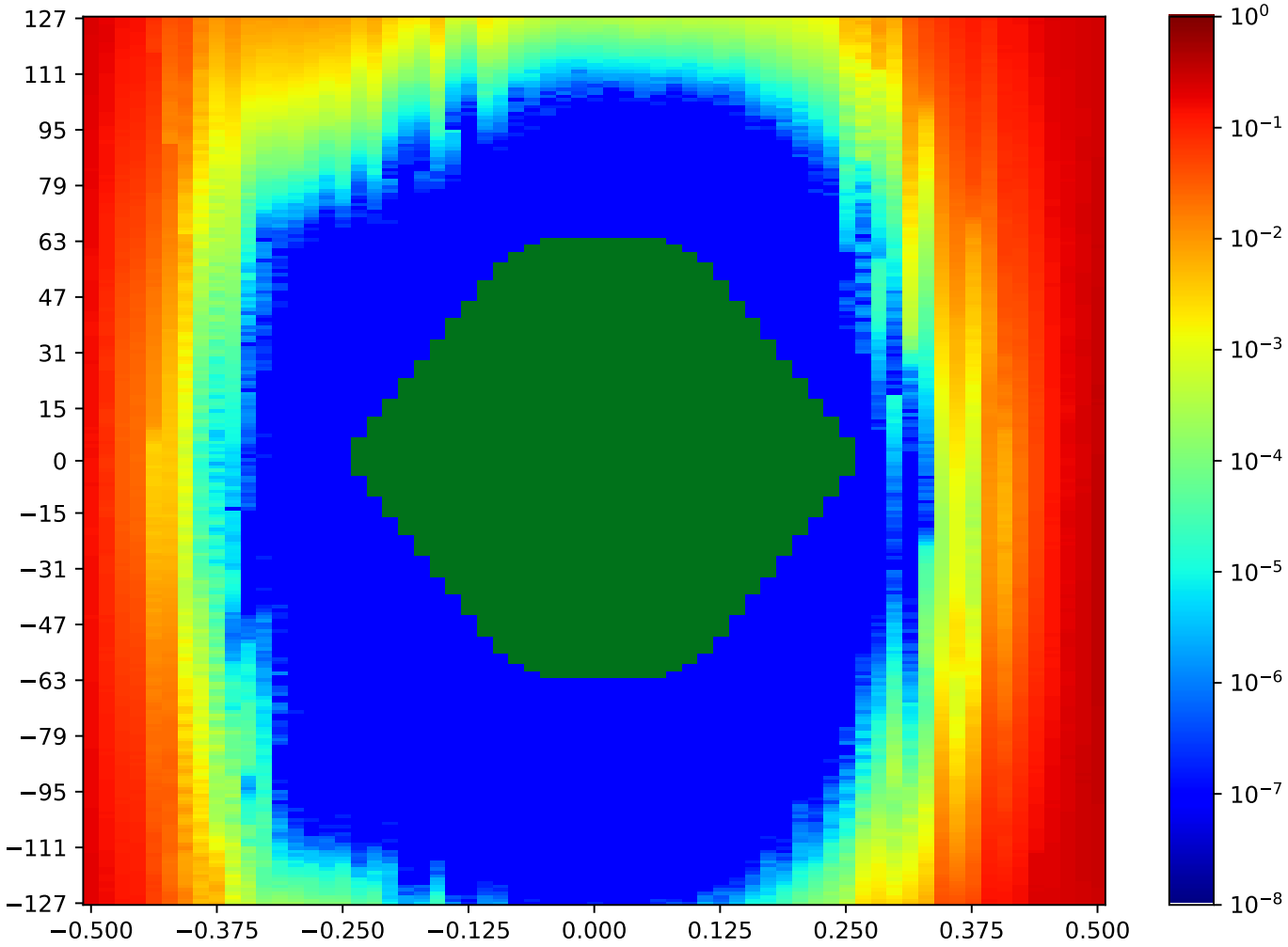


Figure 6.59: TRP_FPGA-TX5-05–RX5-05-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.7 TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Table 6.55: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:40:34		2019-Nov-26 17:40:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8265	36	55.38%	246	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

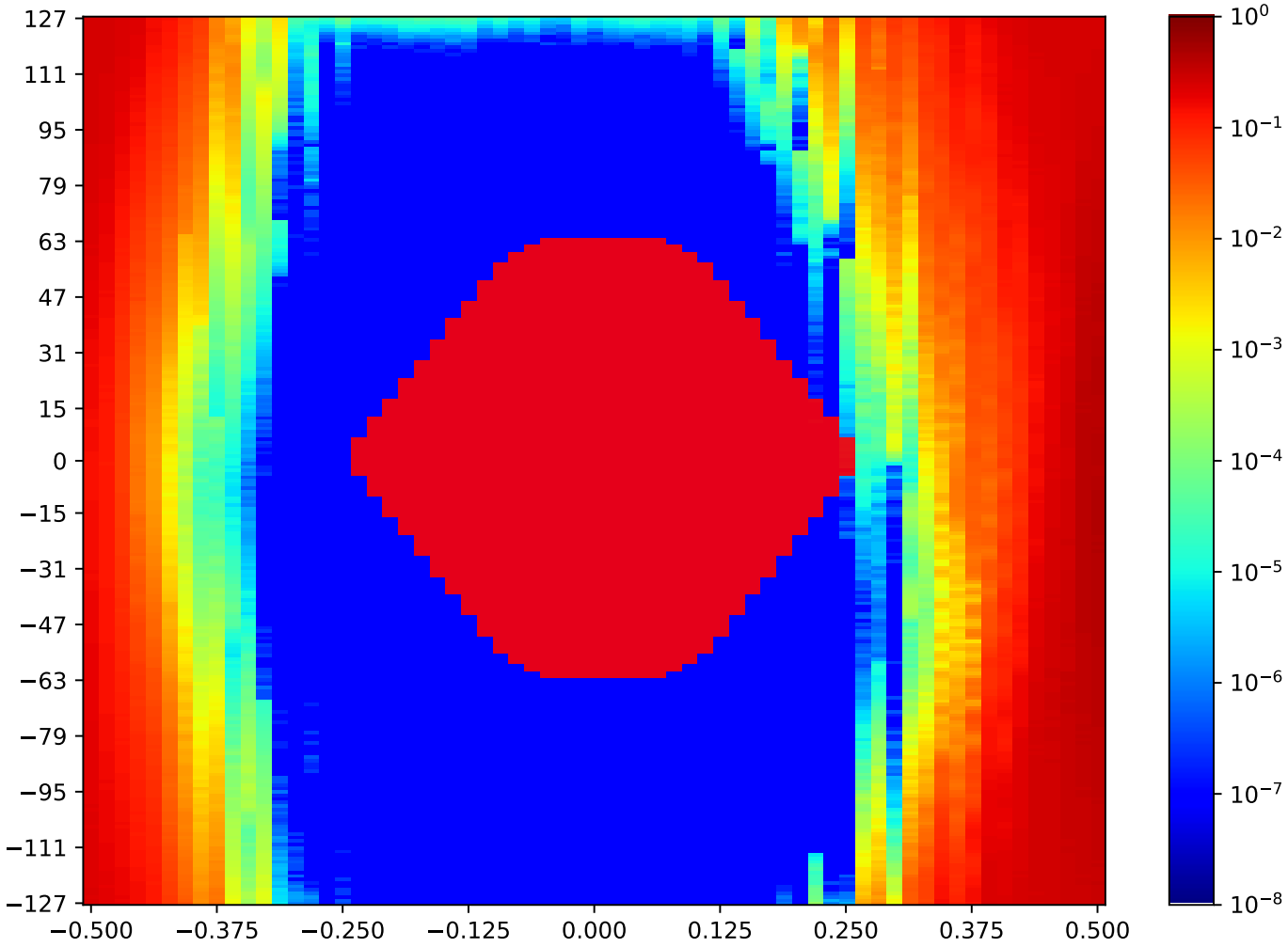


Figure 6.60: TRP_FPGA-TX5-06–RX5-06-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.5.8 TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Table 6.56: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-26 17:41:21		2019-Nov-26 17:41:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6349	37	56.92%	200	76.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

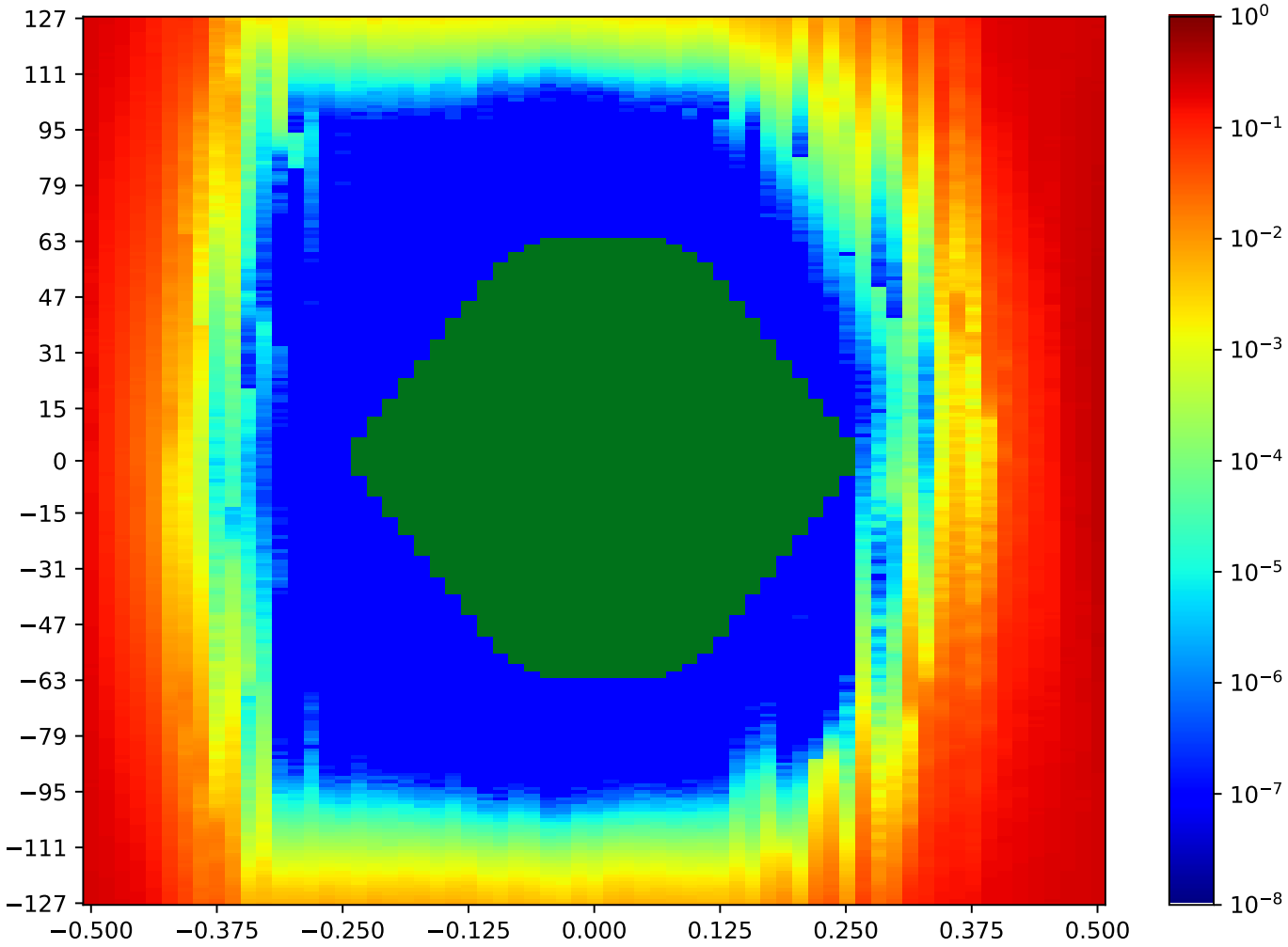


Figure 6.61: TRP_FPGA-TX5-07–RX5-07-MSP_A_FPGA

Call back to summary Figure 6.53. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.6 TRP J1 QSFP Loopback

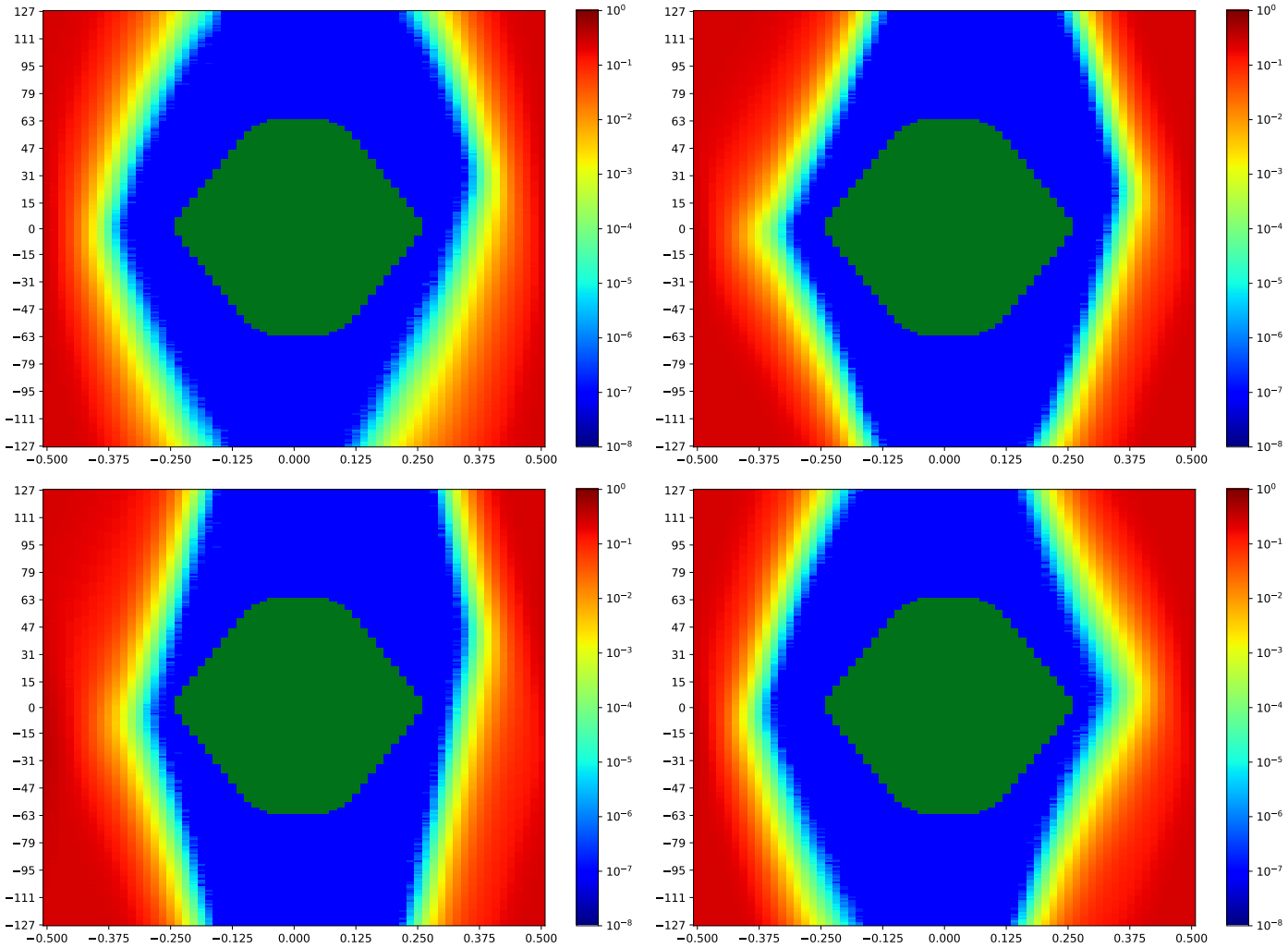


Figure 6.62: TRP J1 QSFP Loopback

A cross-reference to Figure 6.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.67.

6.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 6.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:42:14		2019-Nov-26 17:42:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8095	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

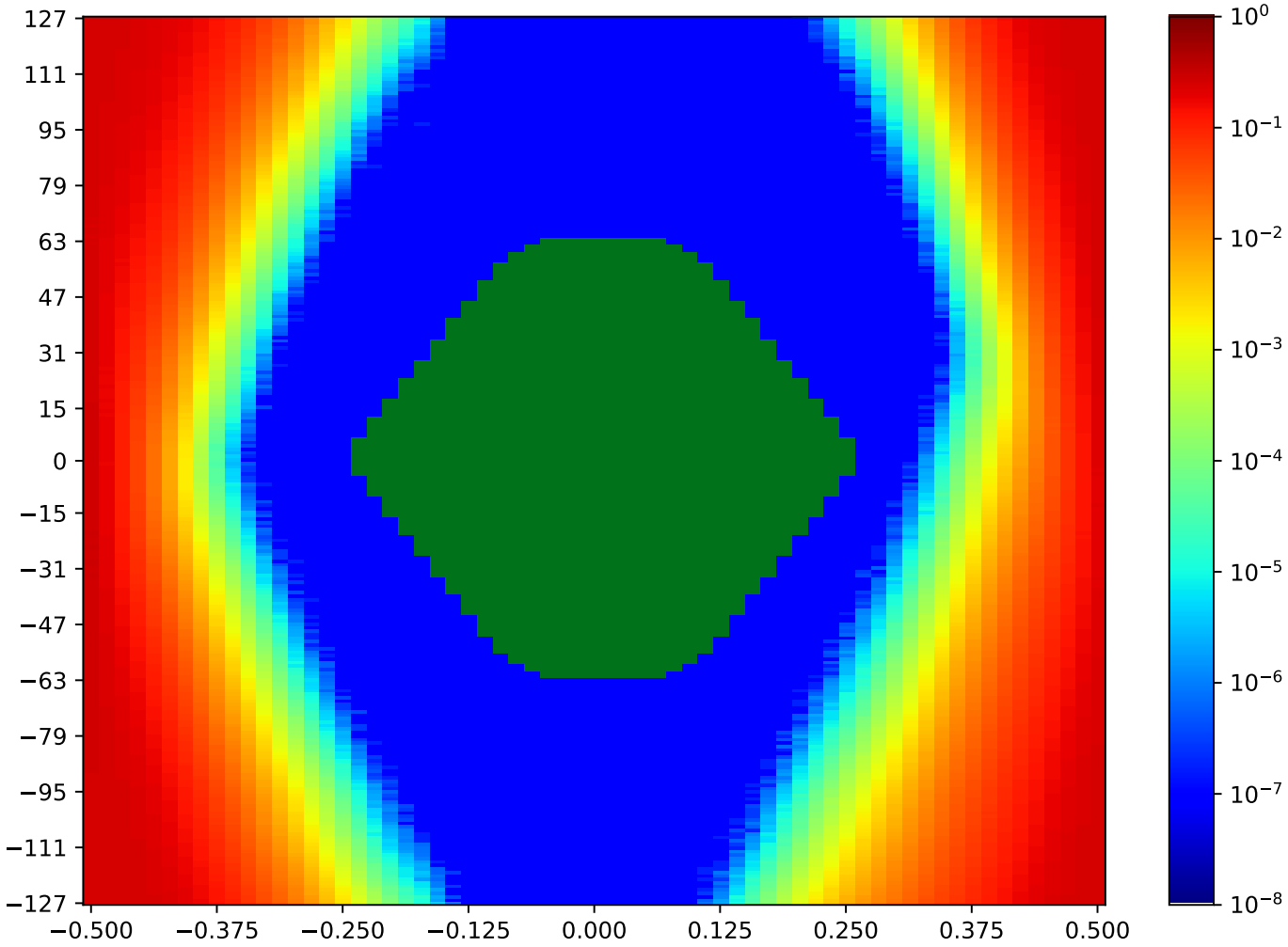


Figure 6.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 6.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 6.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:42:33		2019-Nov-26 17:42:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7744	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

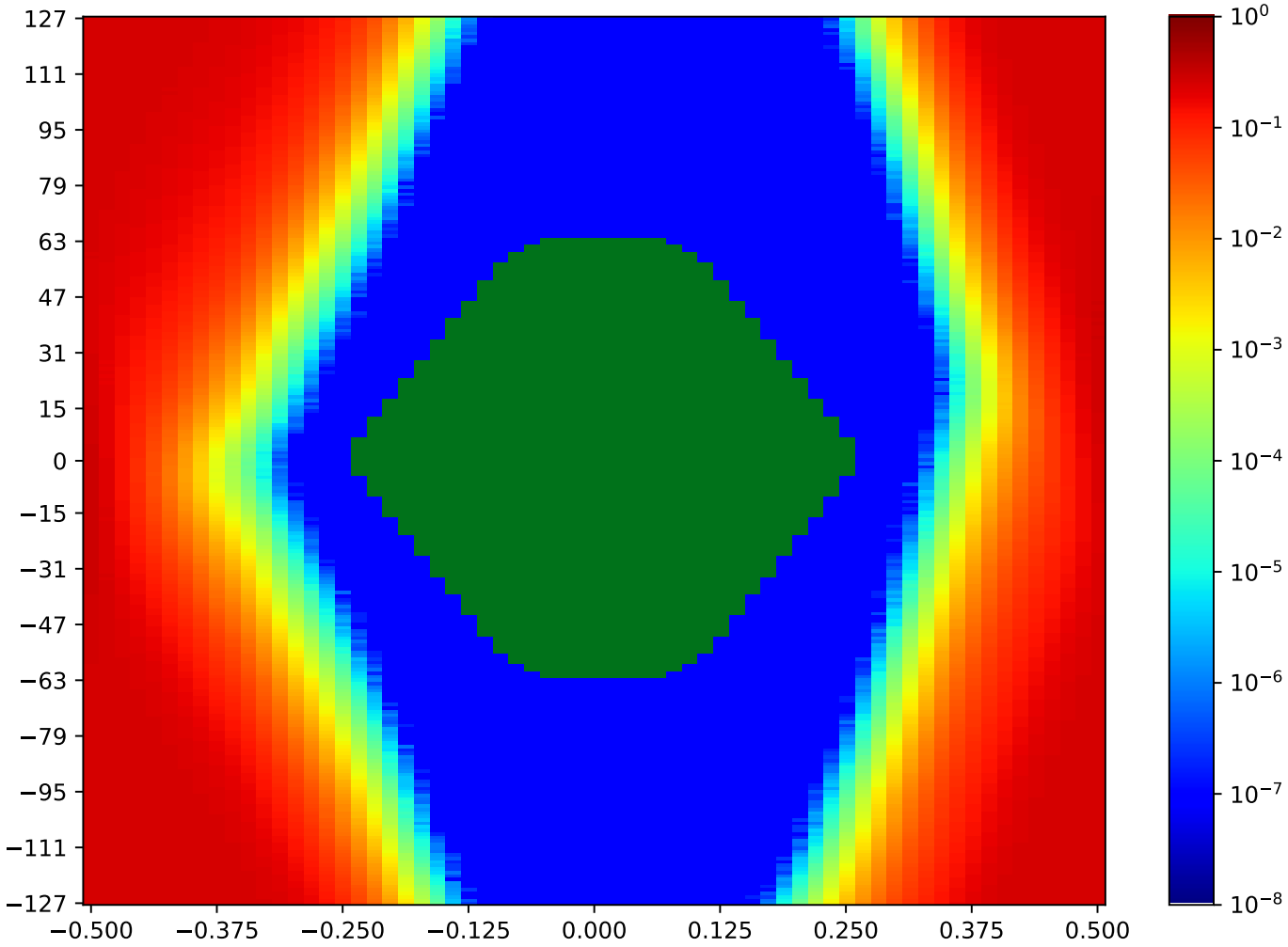


Figure 6.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 6.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 6.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:42:52		2019-Nov-26 17:43:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8013	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

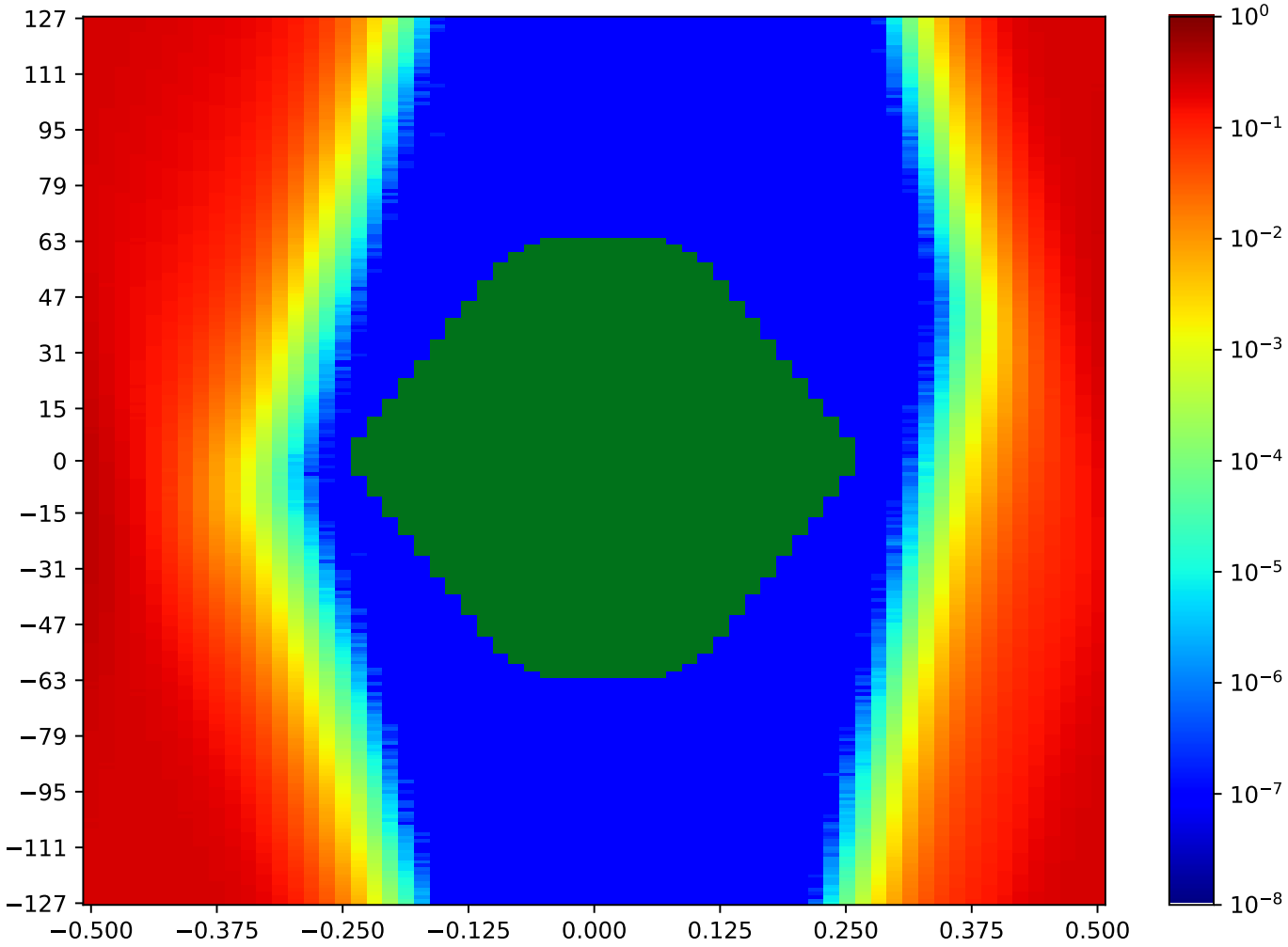


Figure 6.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 6.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 6.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:43:11		2019-Nov-26 17:43:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7703	41	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

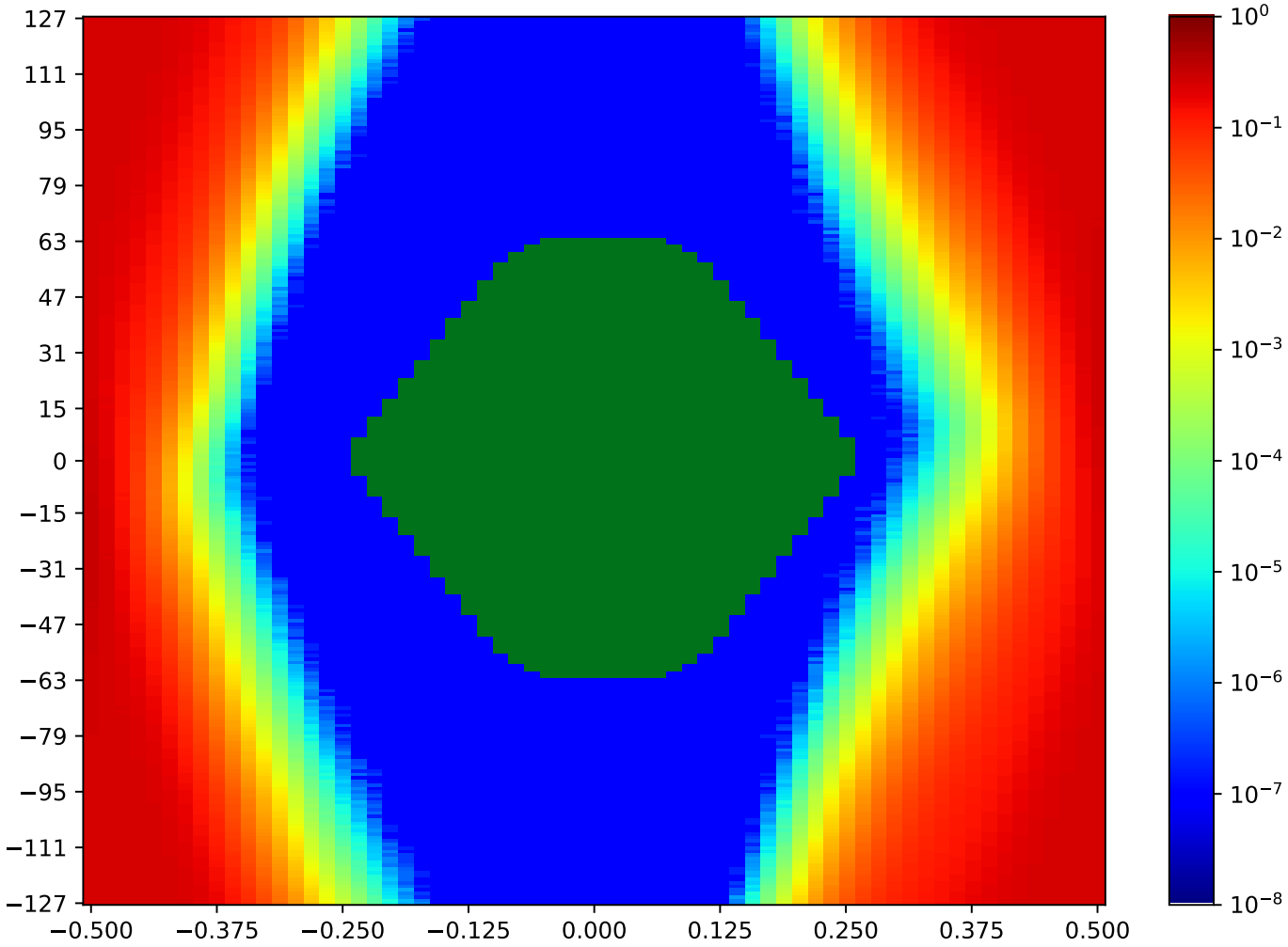


Figure 6.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 6.62. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.7 TRP J3 SFP Loopback

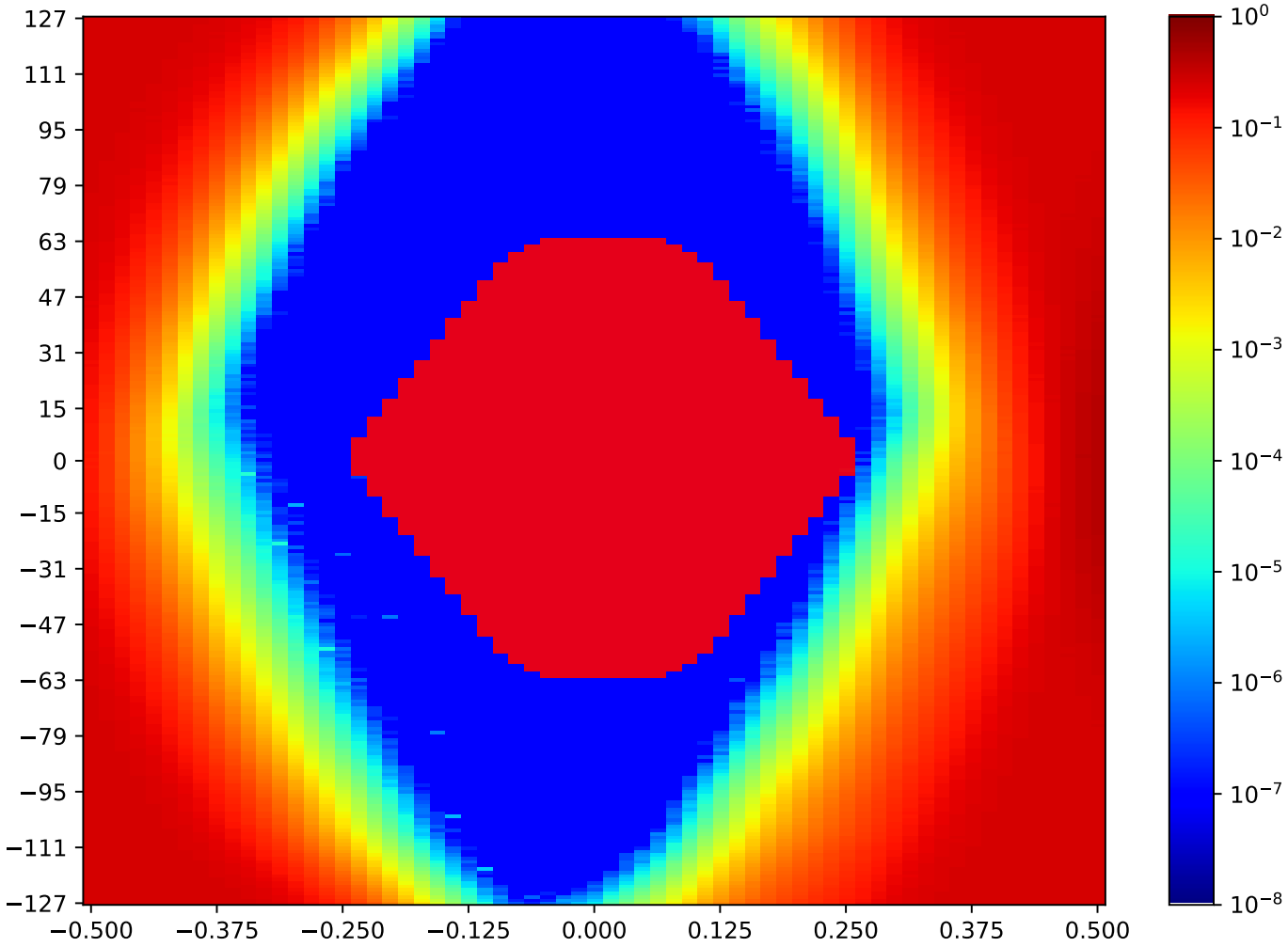


Figure 6.67: TRP J3 SFP Loopback

A cross-reference to Figure 6.67. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.69.

6.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 6.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:43:30		2019-Nov-26 17:43:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6654	38	58.46%	247	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

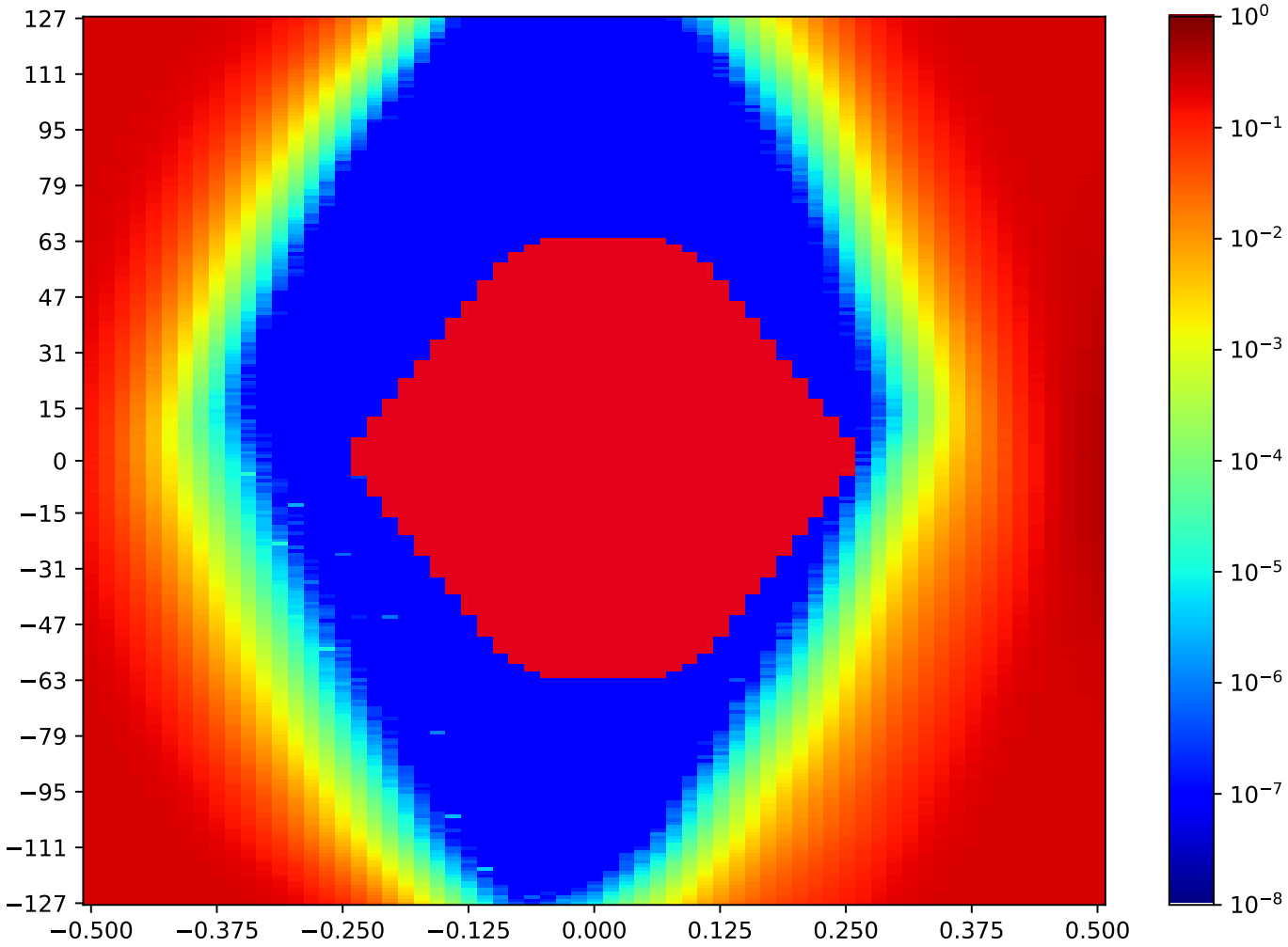


Figure 6.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 6.67. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8 MSP_A TRP On board links

A cross-reference to Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.98.

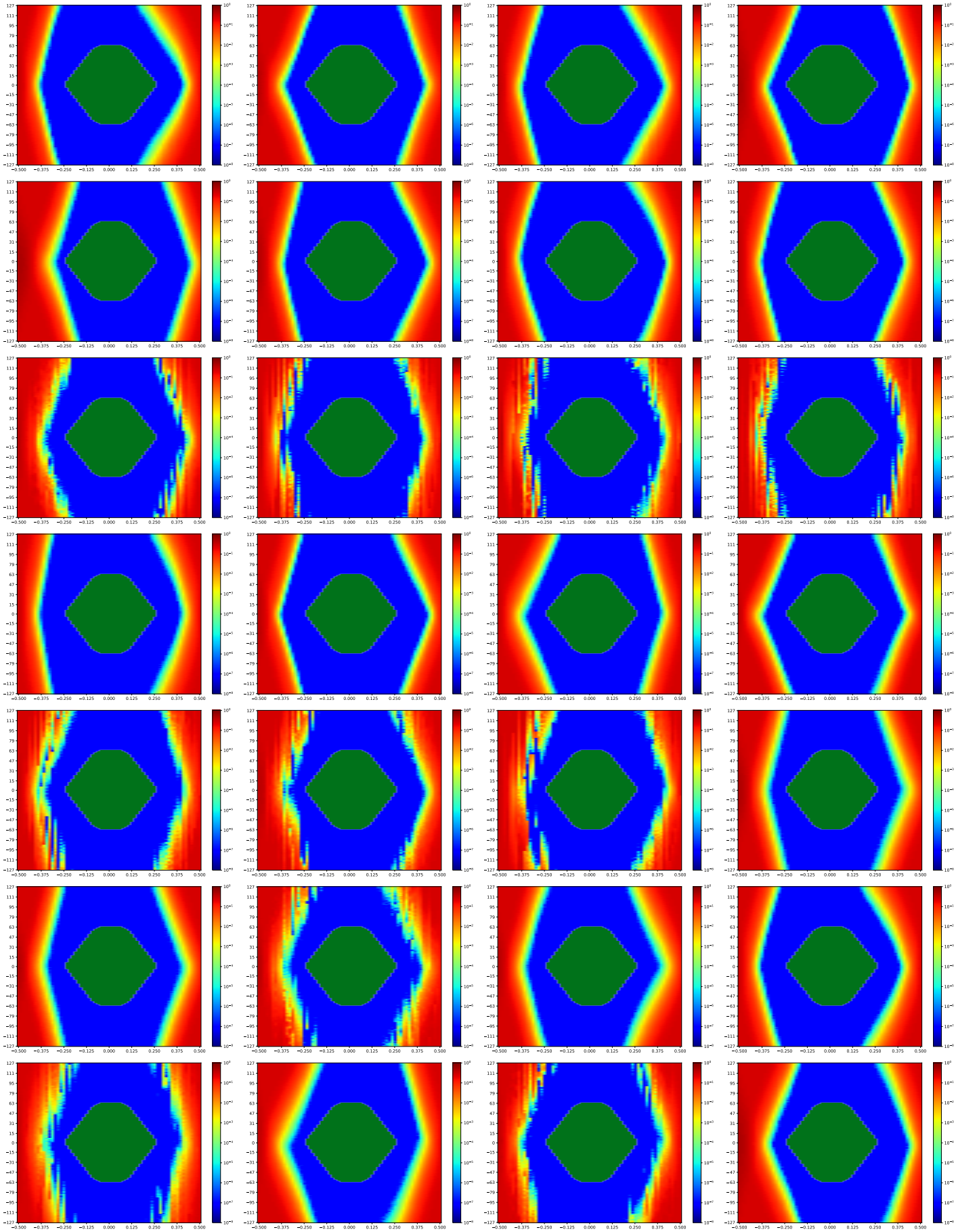


Figure 6.69: MSP_A TRP On board links

6.8.1 MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Table 6.62: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:43:54		2019-Nov-26 17:44:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9603	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

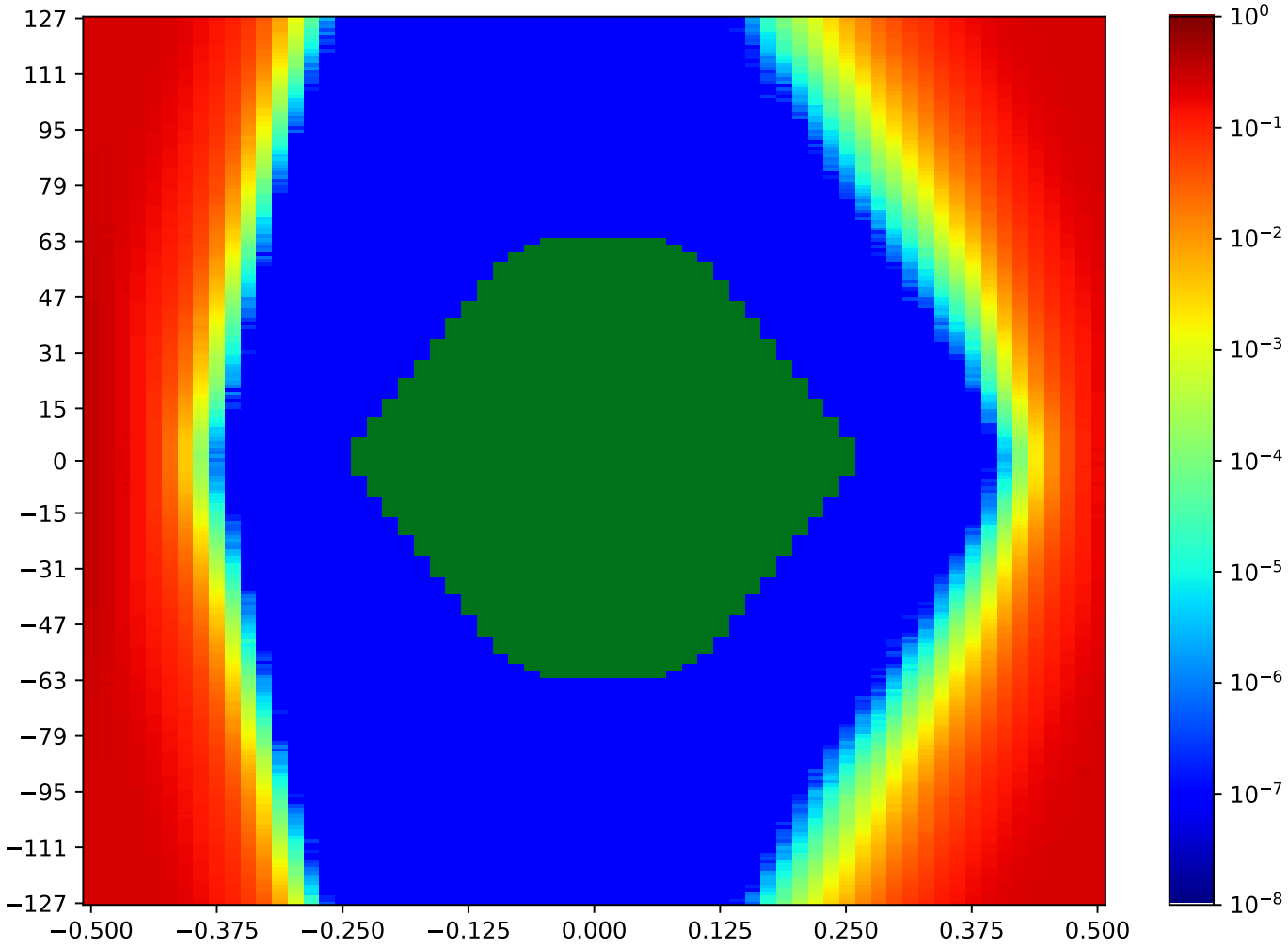


Figure 6.70: MSP_A_FPGA-IC39-00–IC4-00-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.2 MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Table 6.63: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:44:13		2019-Nov-26 17:44:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9477	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

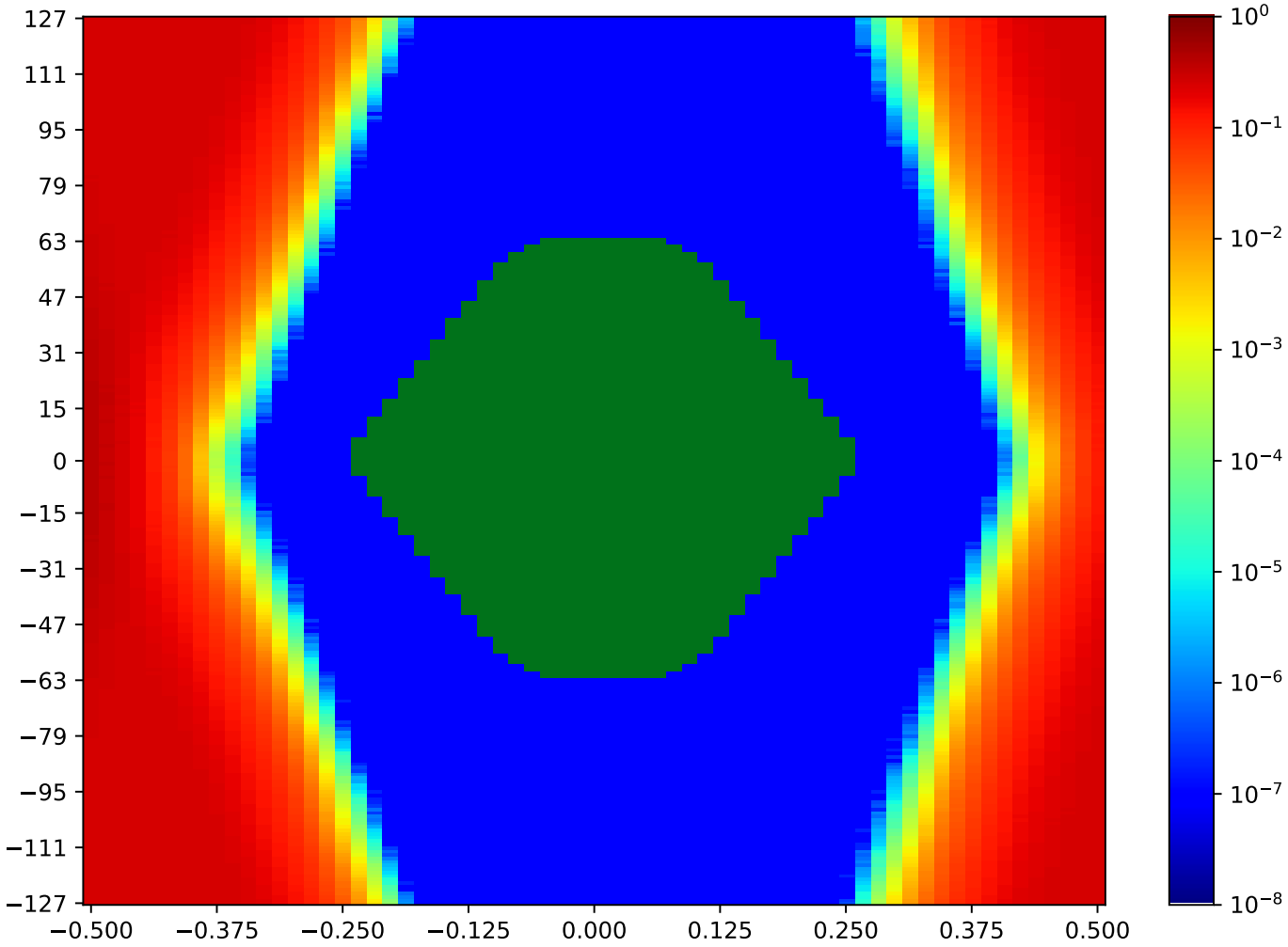


Figure 6.71: MSP_A_FPGA-IC39-01–IC4-01-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.3 MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Table 6.64: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:44:32		2019-Nov-26 17:44:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9509	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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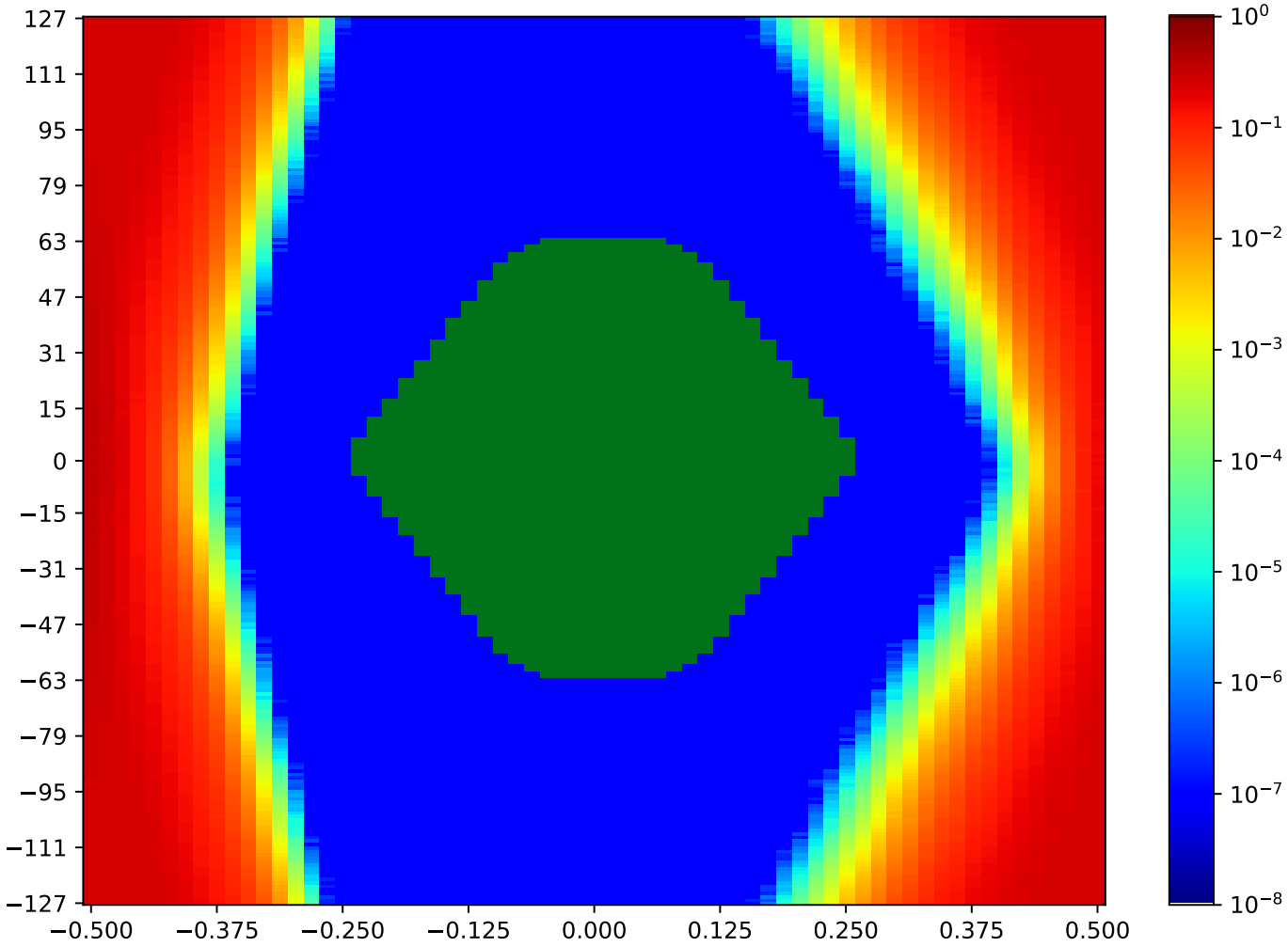


Figure 6.72: MSP_A_FPGA-IC39-02–IC4-02-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.4 MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Table 6.65: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:44:51		2019-Nov-26 17:45:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9697	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

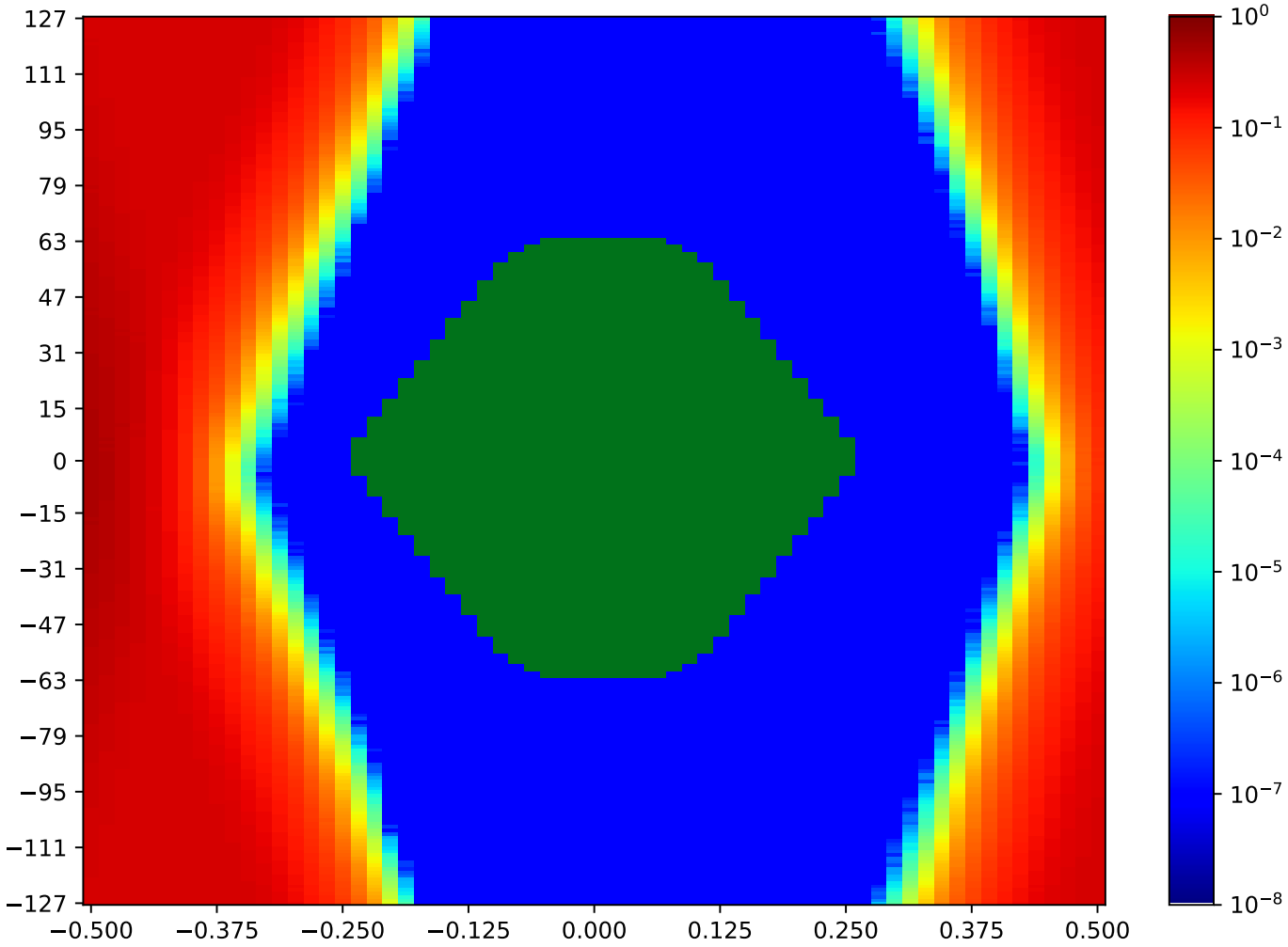


Figure 6.73: MSP_A_FPGA-IC39-03–IC4-03-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.5 MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Table 6.66: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:45:10		2019-Nov-26 17:45:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9313	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

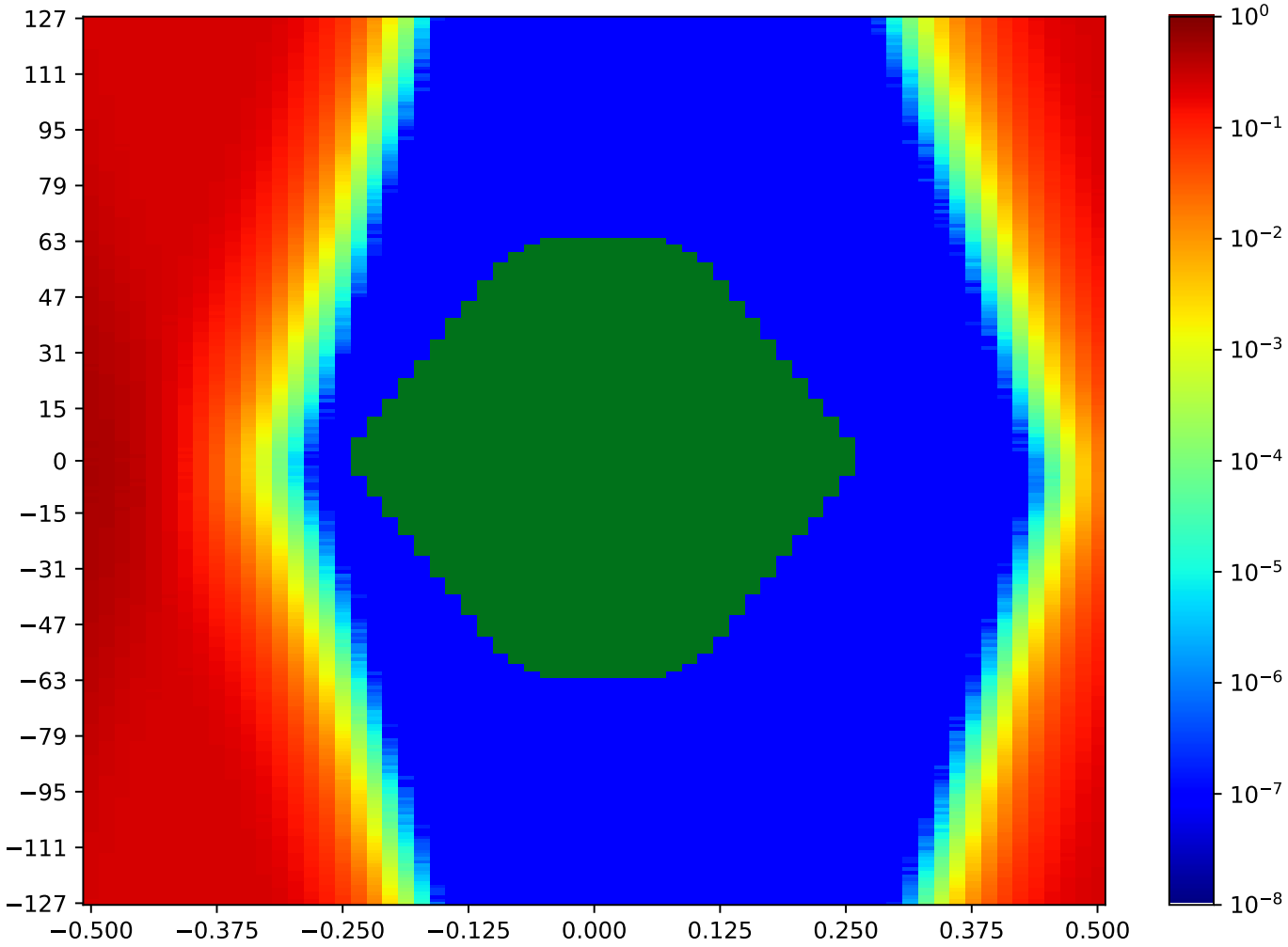


Figure 6.74: MSP_A_FPGA-IC39-04–IC4-04-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.6 MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Table 6.67: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:45:29		2019-Nov-26 17:45:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10056	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

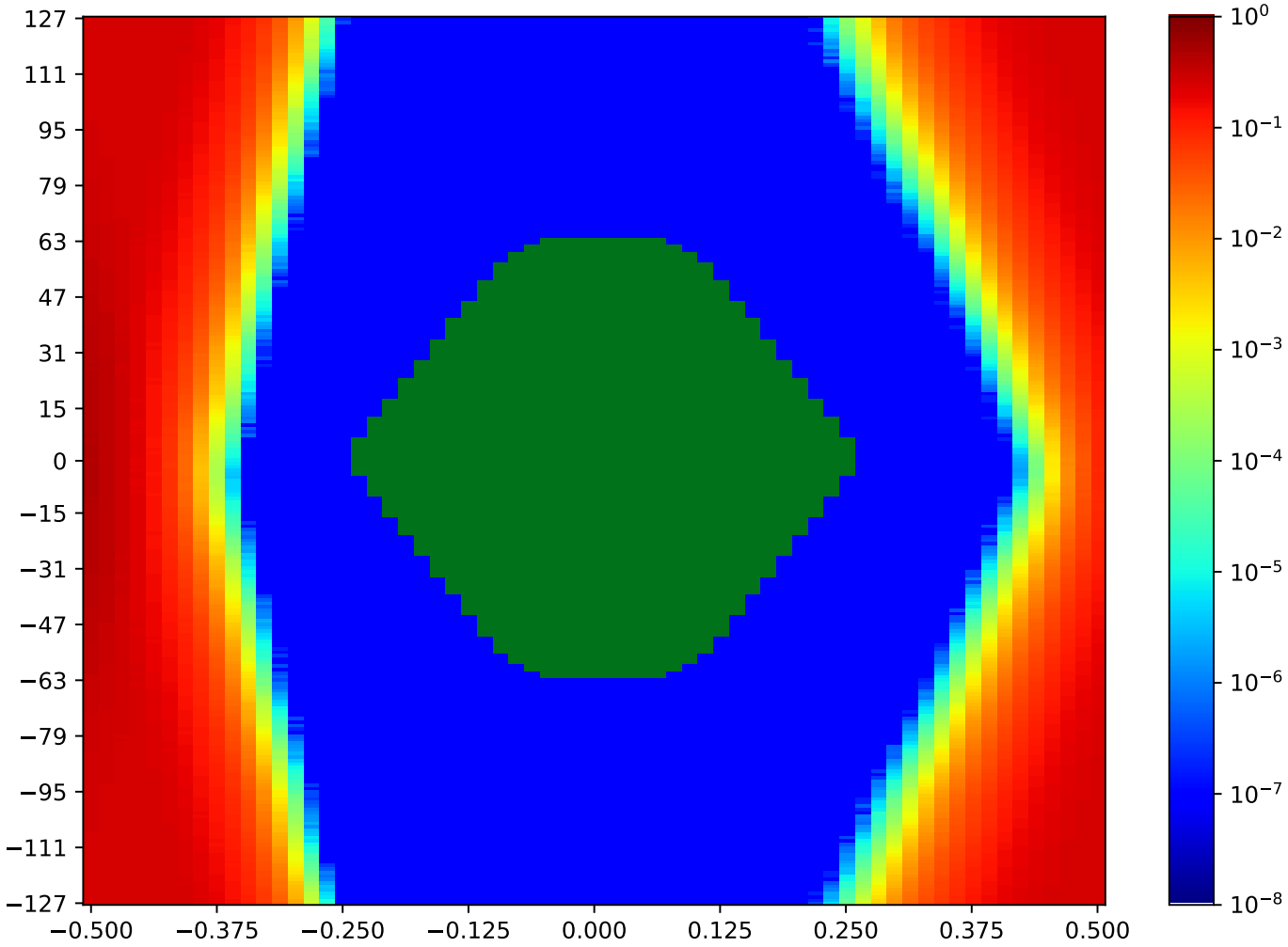


Figure 6.75: MSP_A_FPGA-IC39-05–IC4-05-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.7 MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Table 6.68: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:45:48		2019-Nov-26 17:46:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10305	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

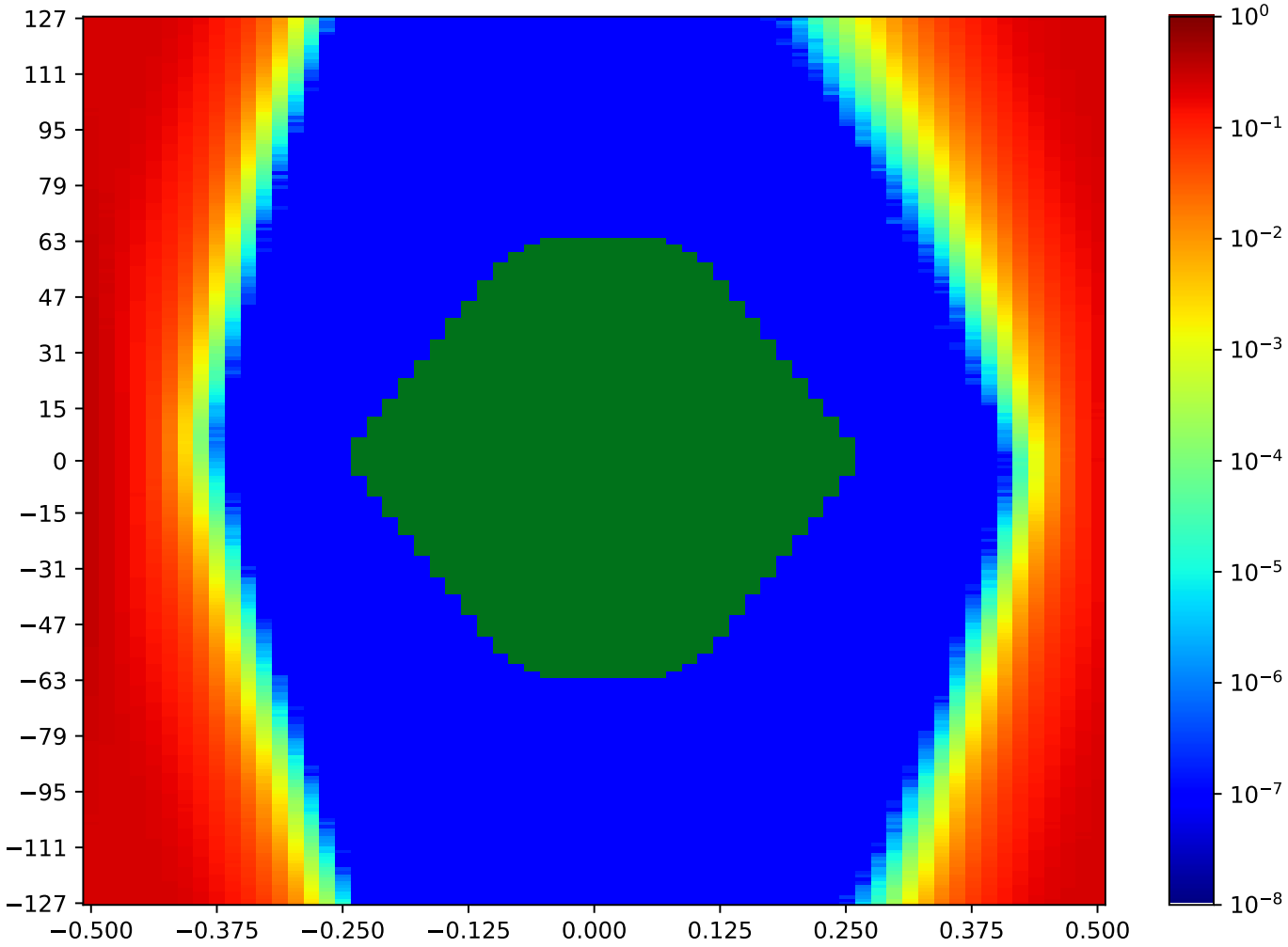


Figure 6.76: MSP_A_FPGA-IC39-06–IC4-06-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.8 MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Table 6.69: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:46:07		2019-Nov-26 17:46:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10204	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

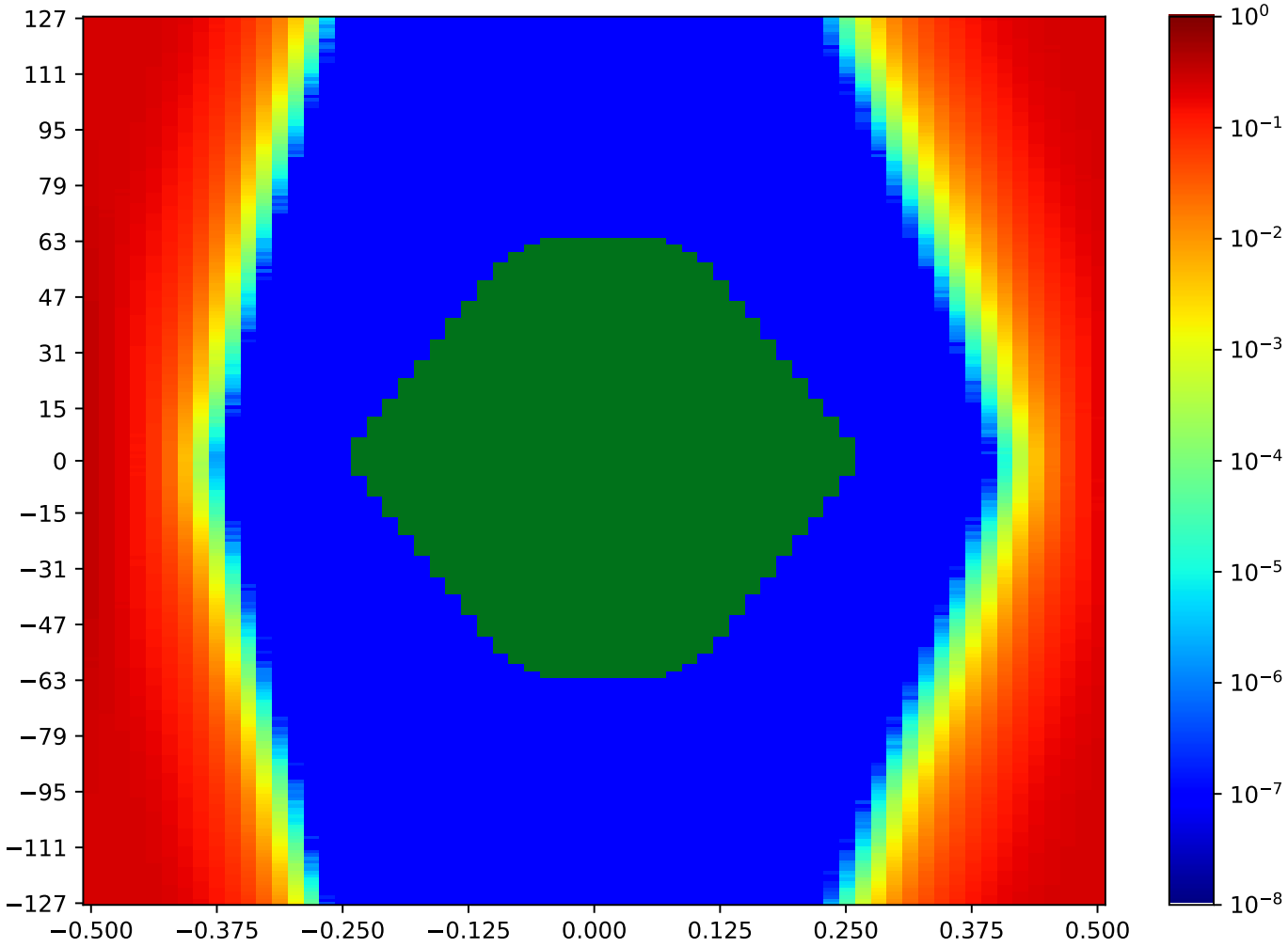


Figure 6.77: MSP_A_FPGA-IC39-07–IC4-07-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.9 MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Table 6.70: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:46:26		2019-Nov-26 17:46:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9684	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

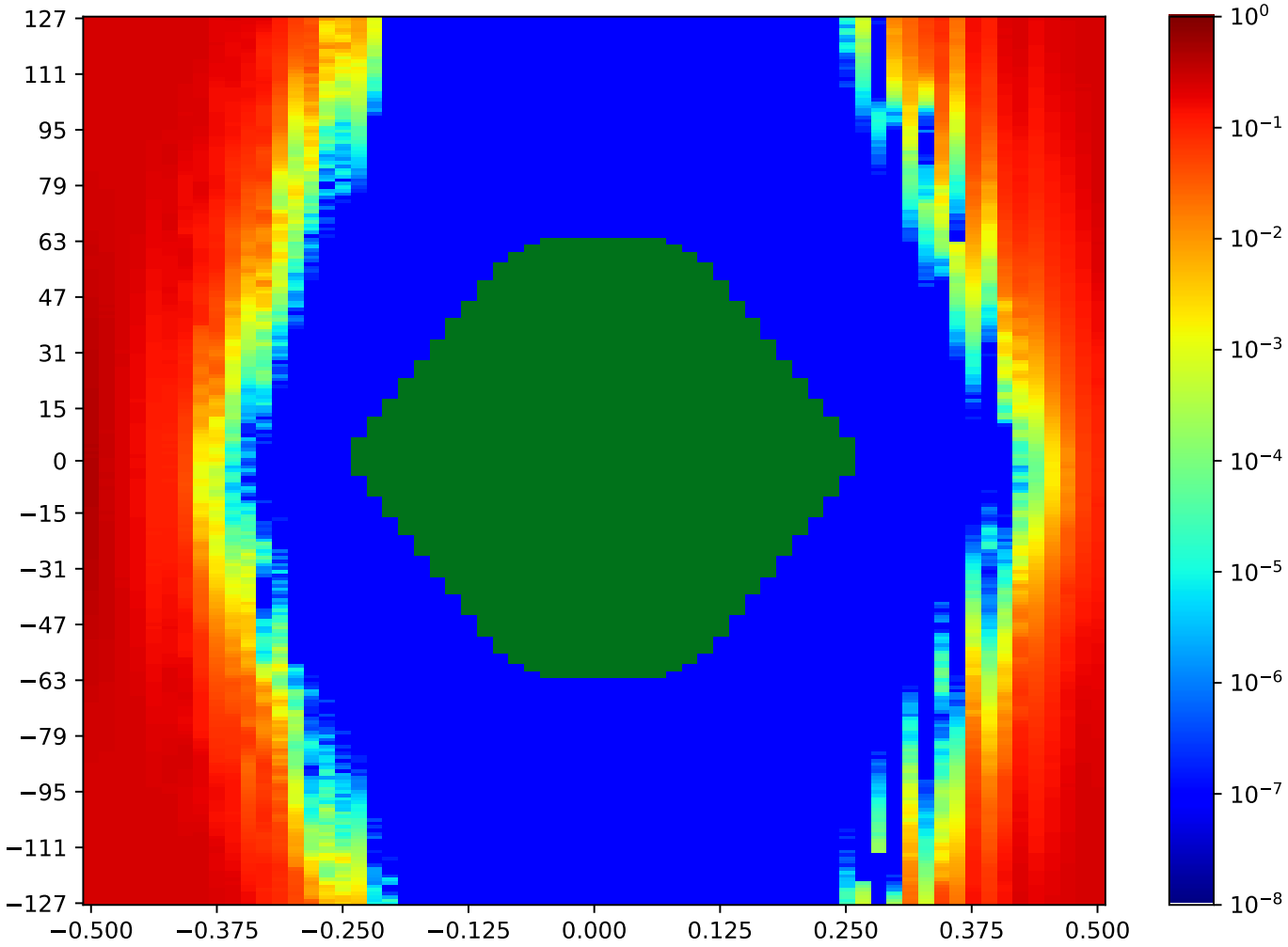


Figure 6.78: MSP_A_FPGA-IC39-08–IC4-08-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.10 MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Table 6.71: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:46:45		2019-Nov-26 17:47:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10280	49	75.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

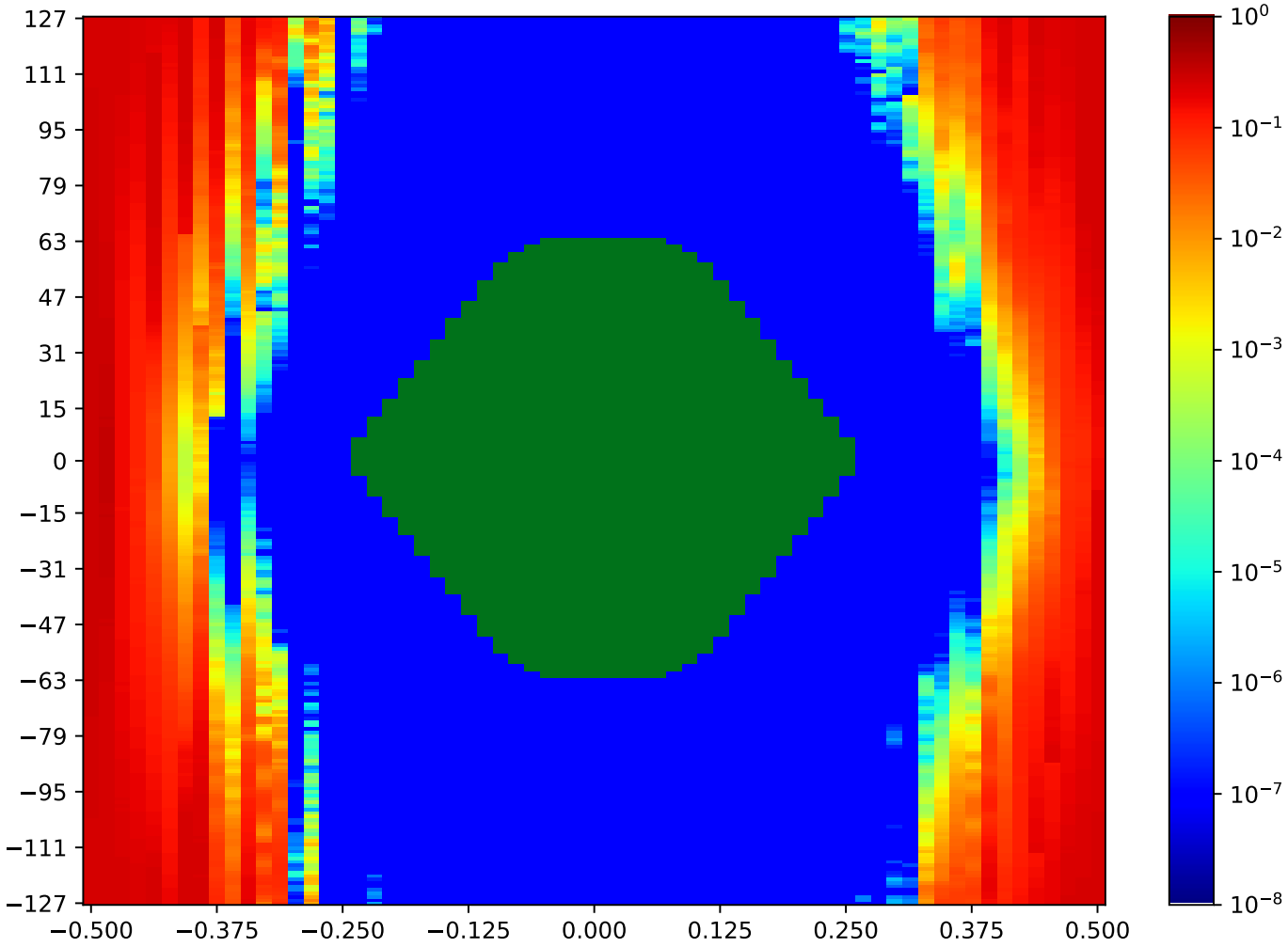


Figure 6.79: MSP_A_FPGA-IC39-09–IC4-09-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.11 MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Table 6.72: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:47:05		2019-Nov-26 17:47:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9928	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

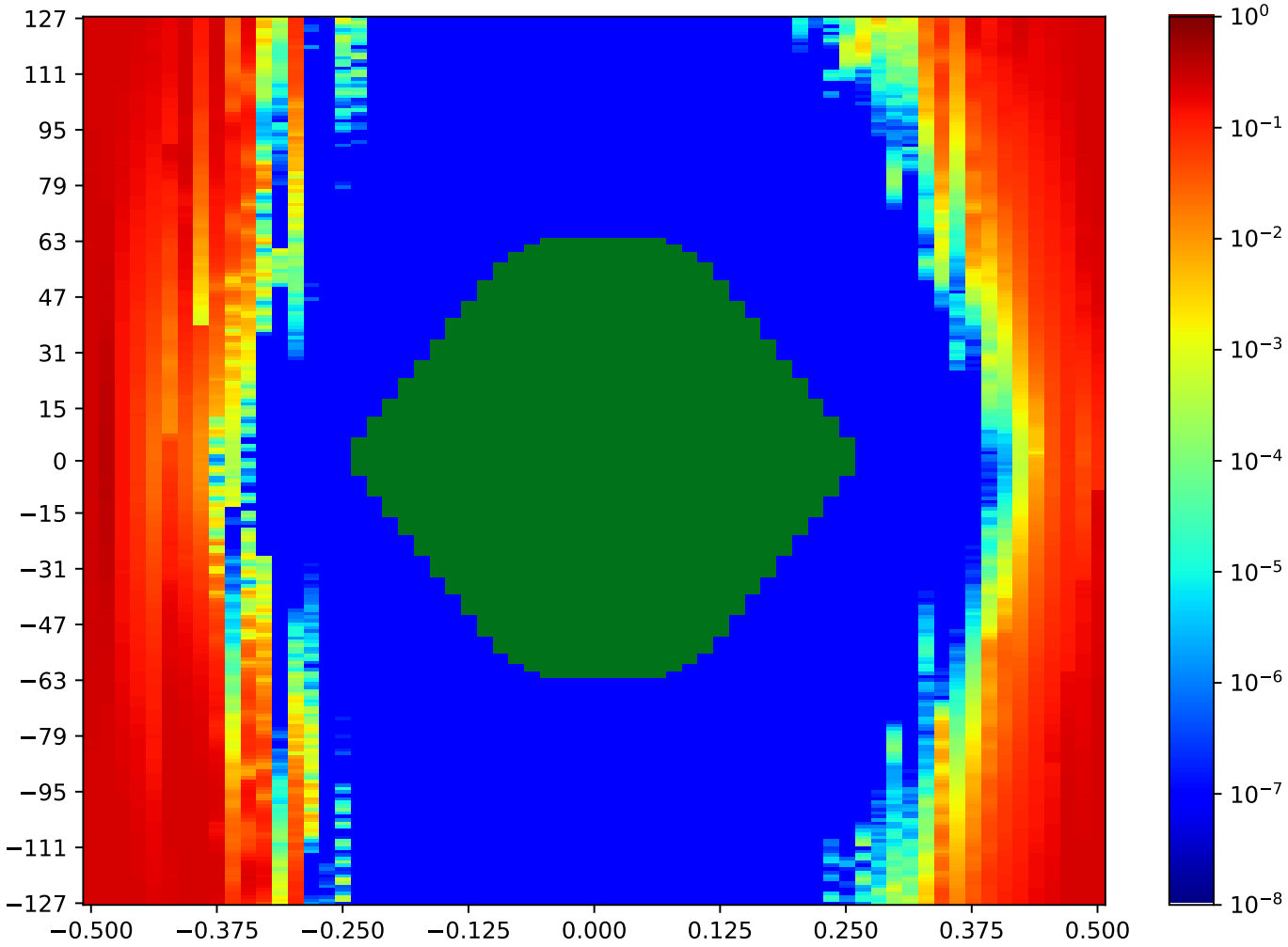


Figure 6.80: MSP_A_FPGA-IC39-10–IC4-10-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.12 MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Table 6.73: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:47:24		2019-Nov-26 17:47:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10217	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

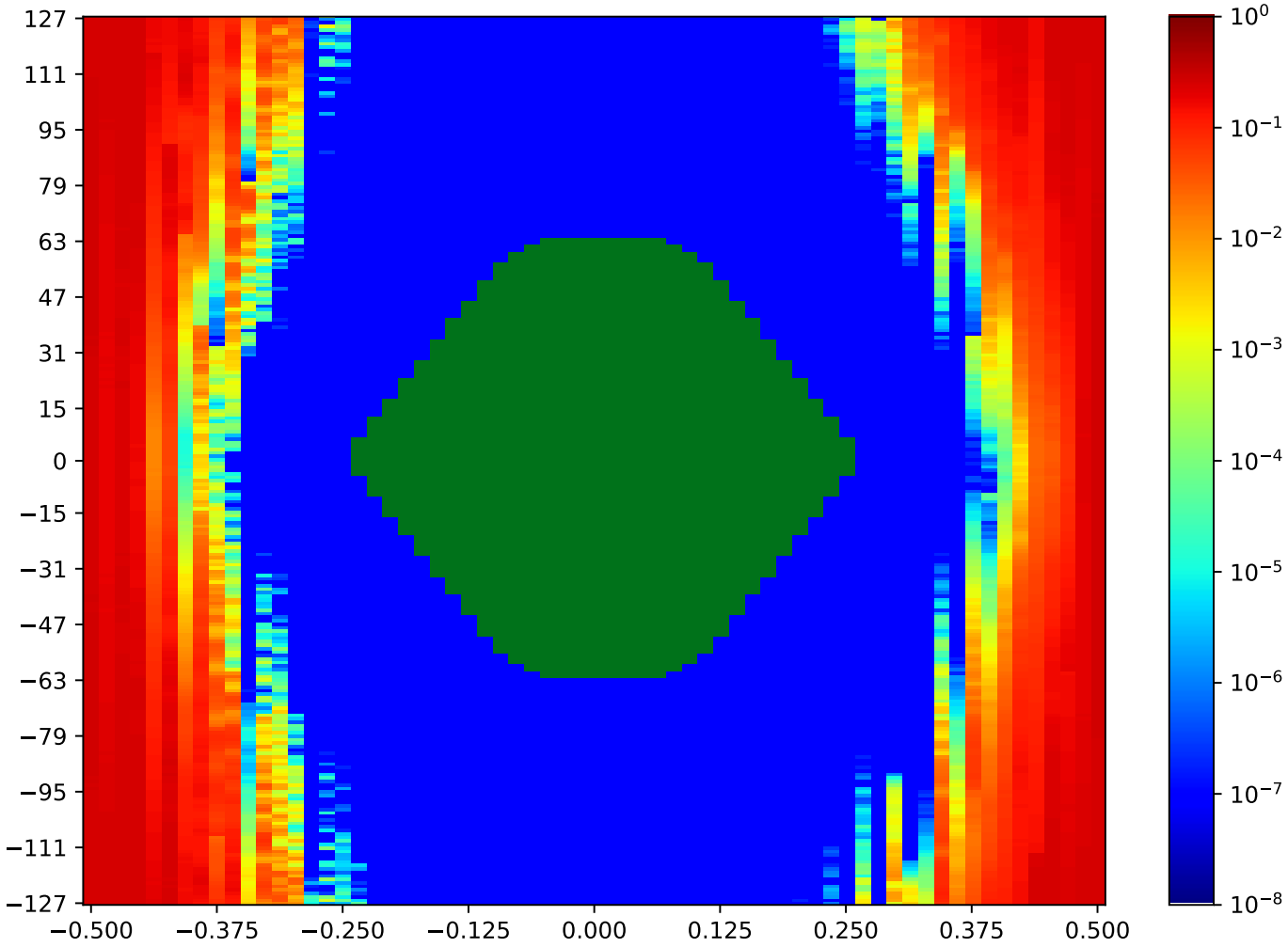


Figure 6.81: MSP_A_FPGA-IC39-11–IC4-11-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.13 MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Table 6.74: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:47:43		2019-Nov-26 17:48:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10436	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

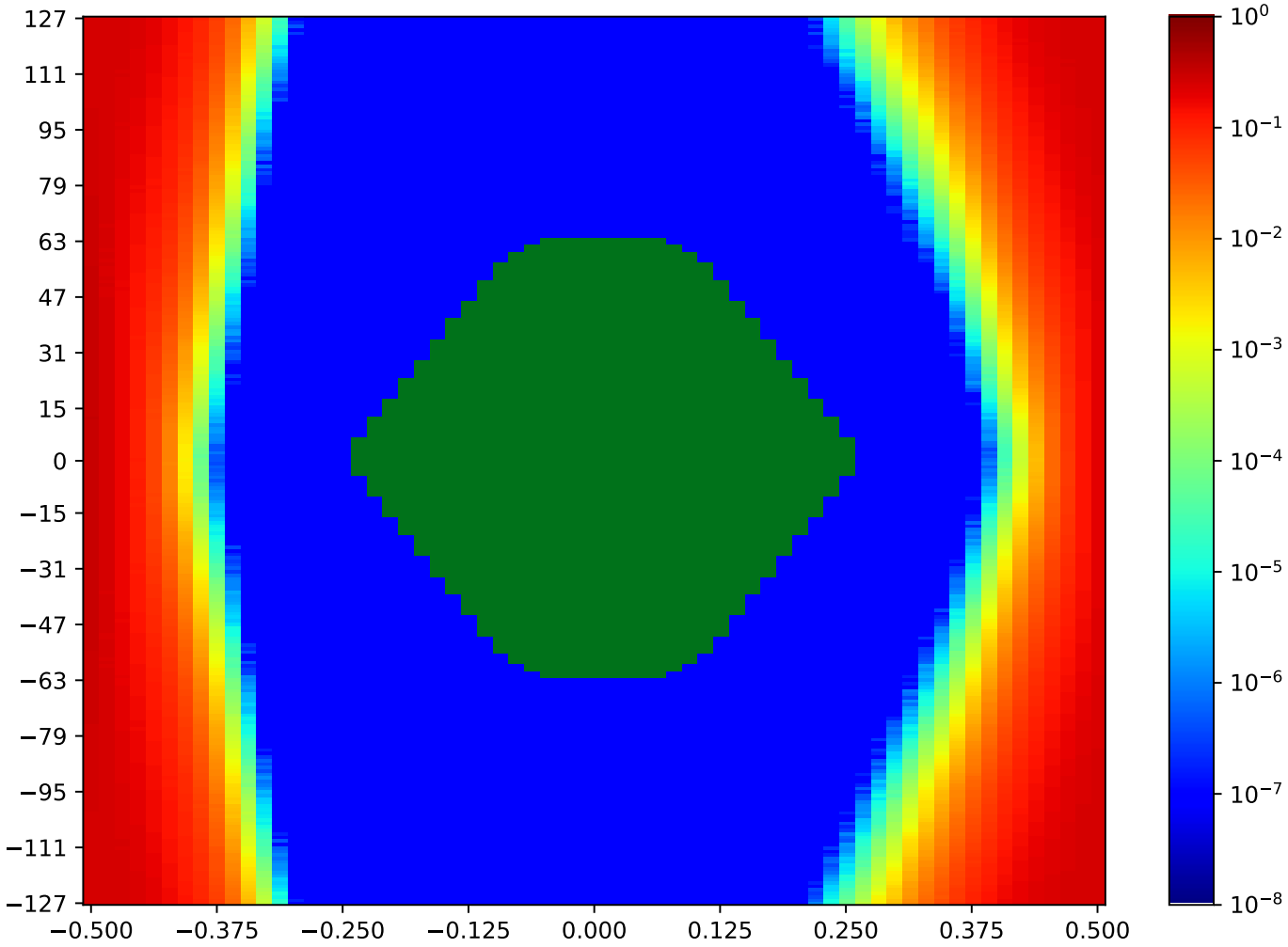


Figure 6.82: MSP_A_FPGA-IC39-12–IC4-12-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.14 MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Table 6.75: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:48:02		2019-Nov-26 17:48:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10341	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

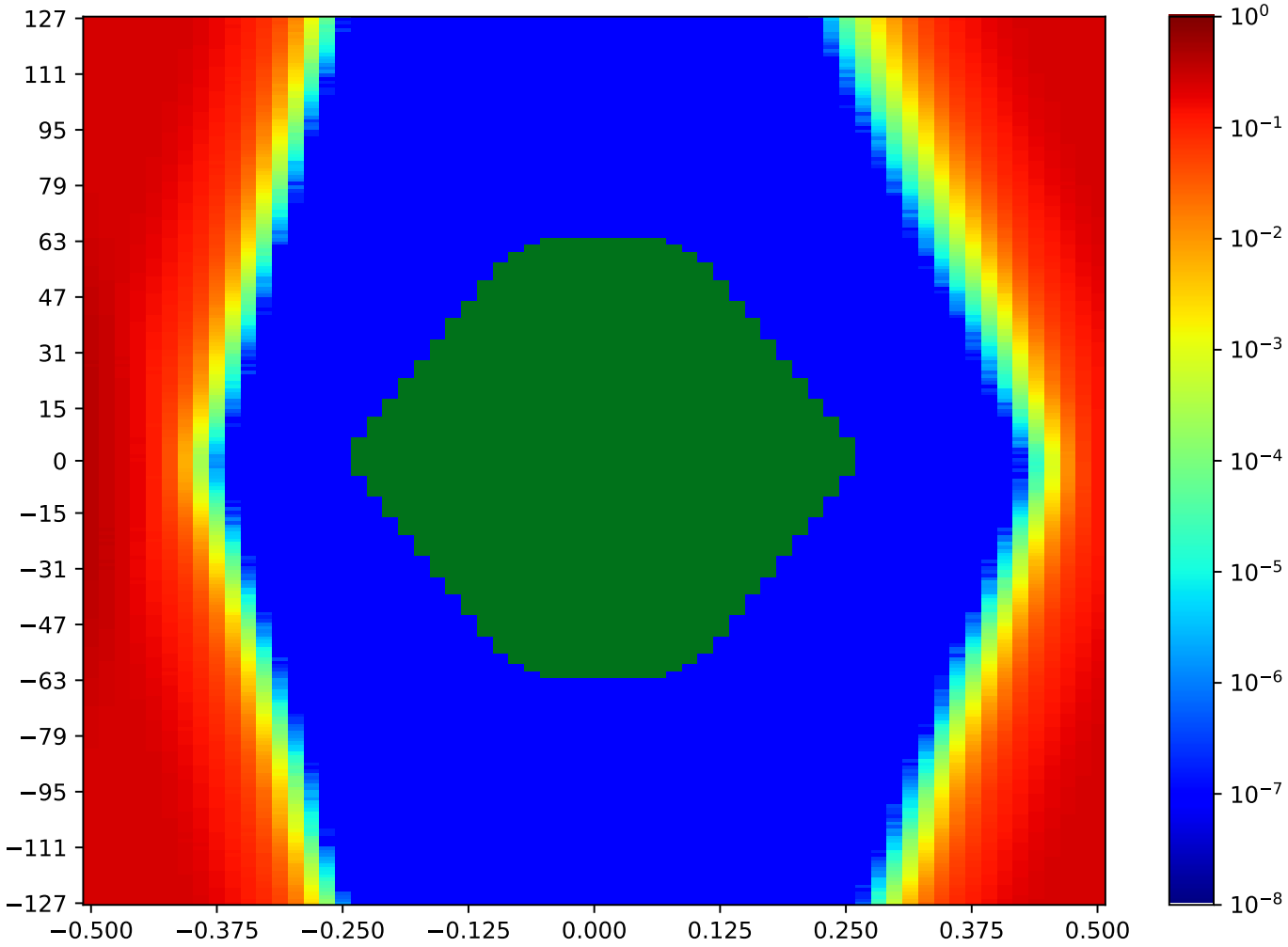


Figure 6.83: MSP_A_FPGA-IC39-13–IC4-13-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.15 MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Table 6.76: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:48:21		2019-Nov-26 17:48:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9274	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

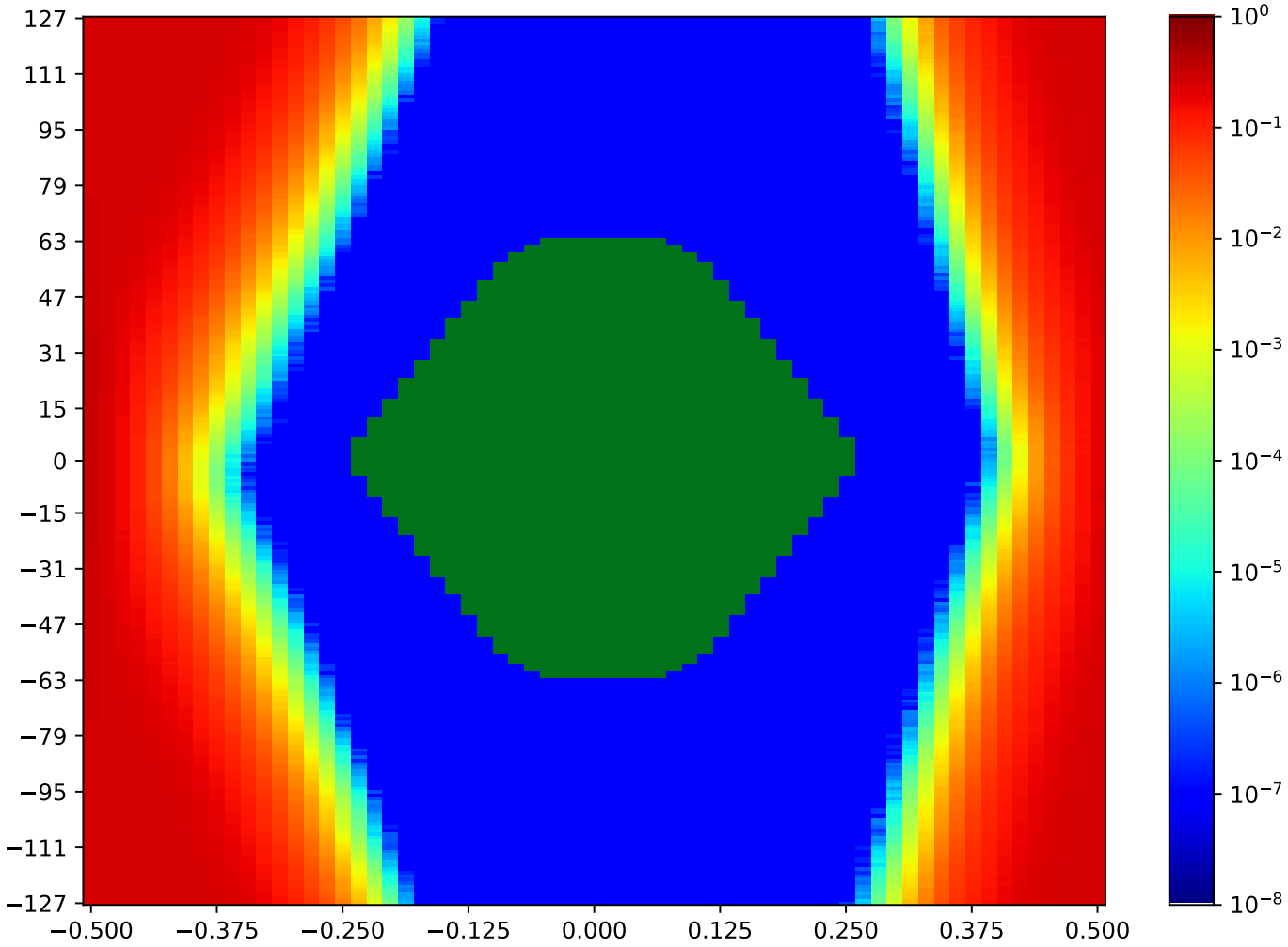


Figure 6.84: MSP_A_FPGA-IC39-14–IC4-14-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.16 MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Table 6.77: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:48:40		2019-Nov-26 17:48:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9295	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

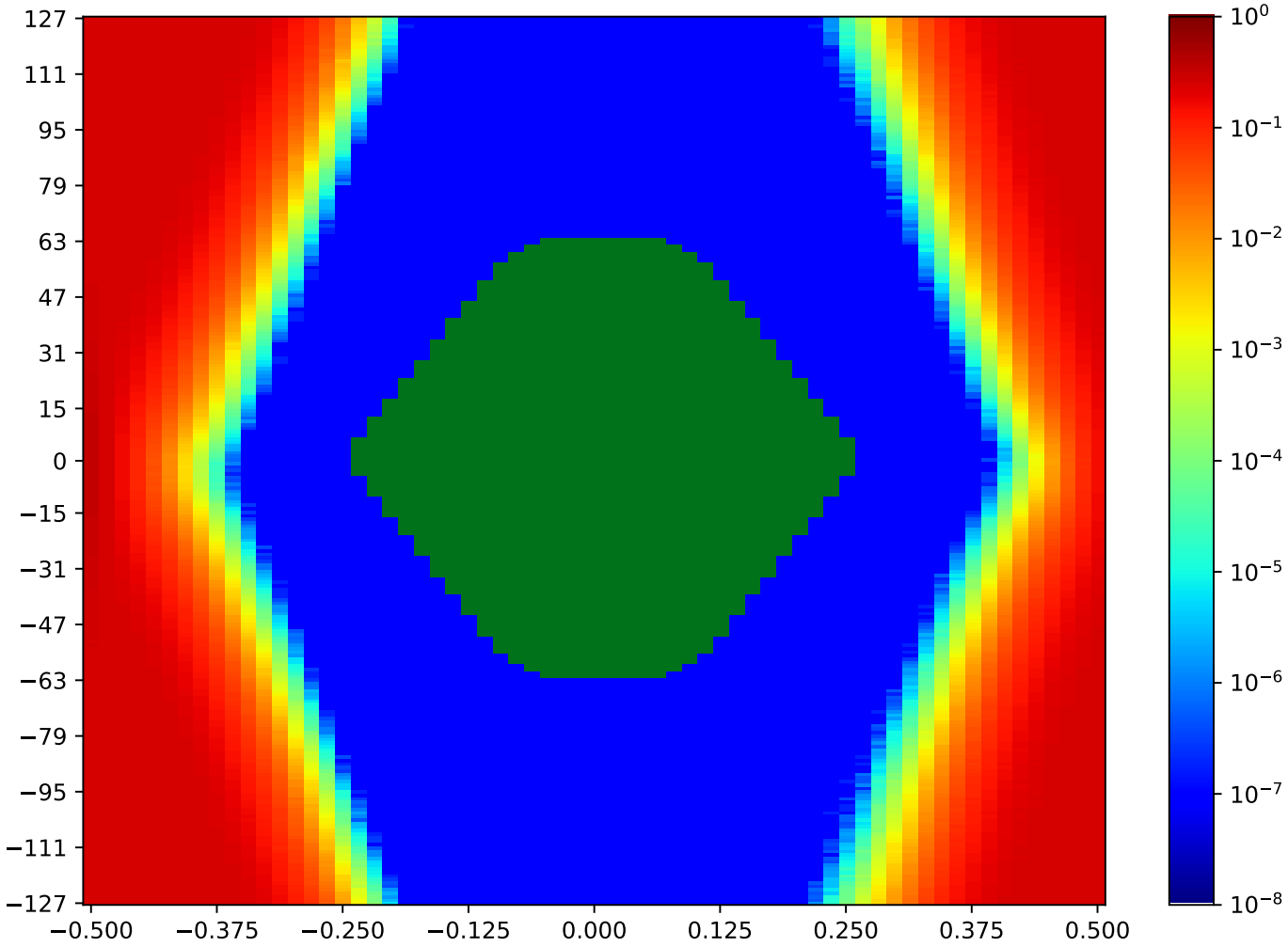


Figure 6.85: MSP_A_FPGA-IC39-15–IC4-15-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.17 MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Table 6.78: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:48:59		2019-Nov-26 17:49:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9758	47	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

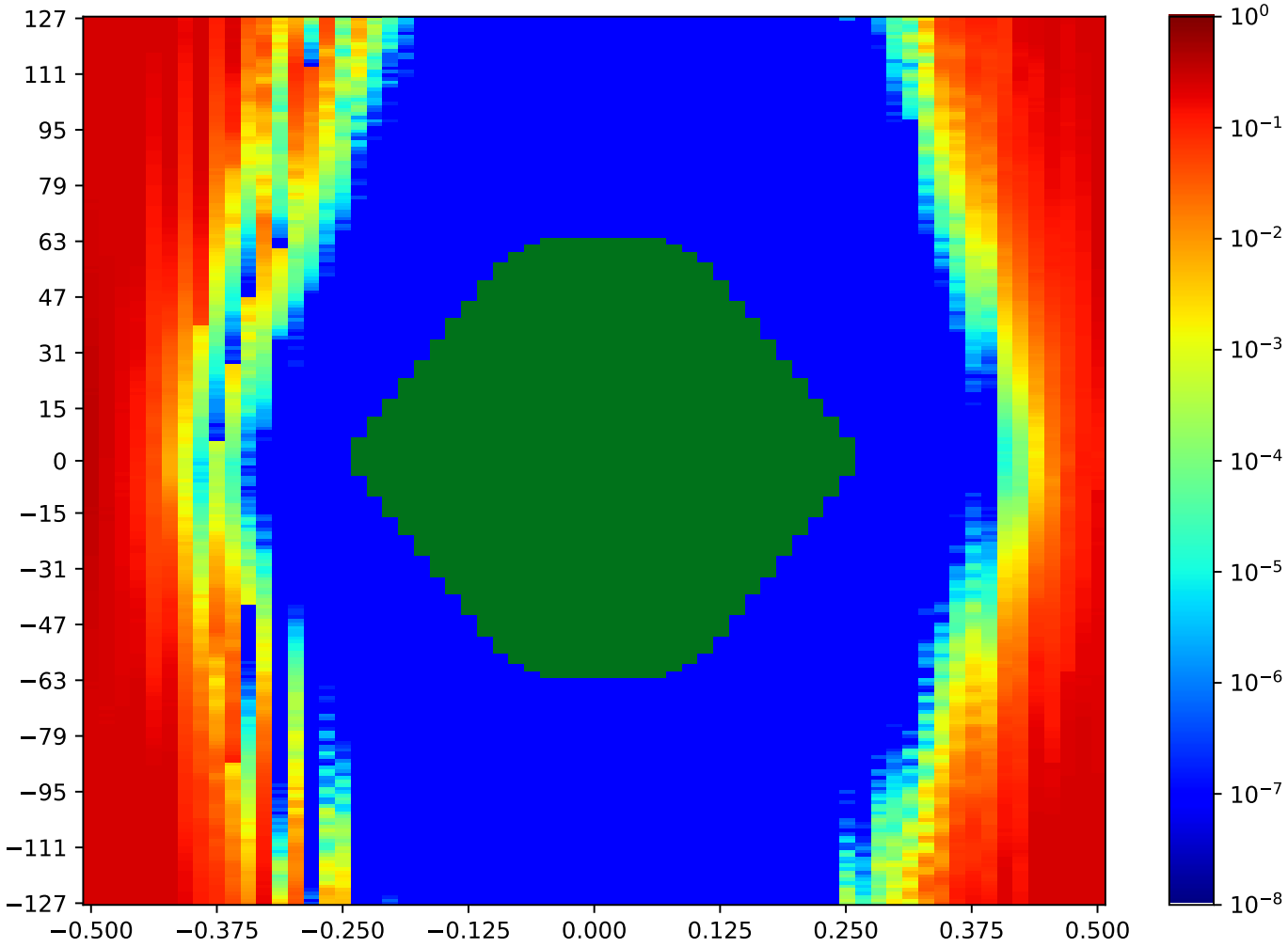


Figure 6.86: MSP_A_FPGA-IC39-16–IC4-16-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.18 MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Table 6.79: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:49:18		2019-Nov-26 17:49:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9425	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

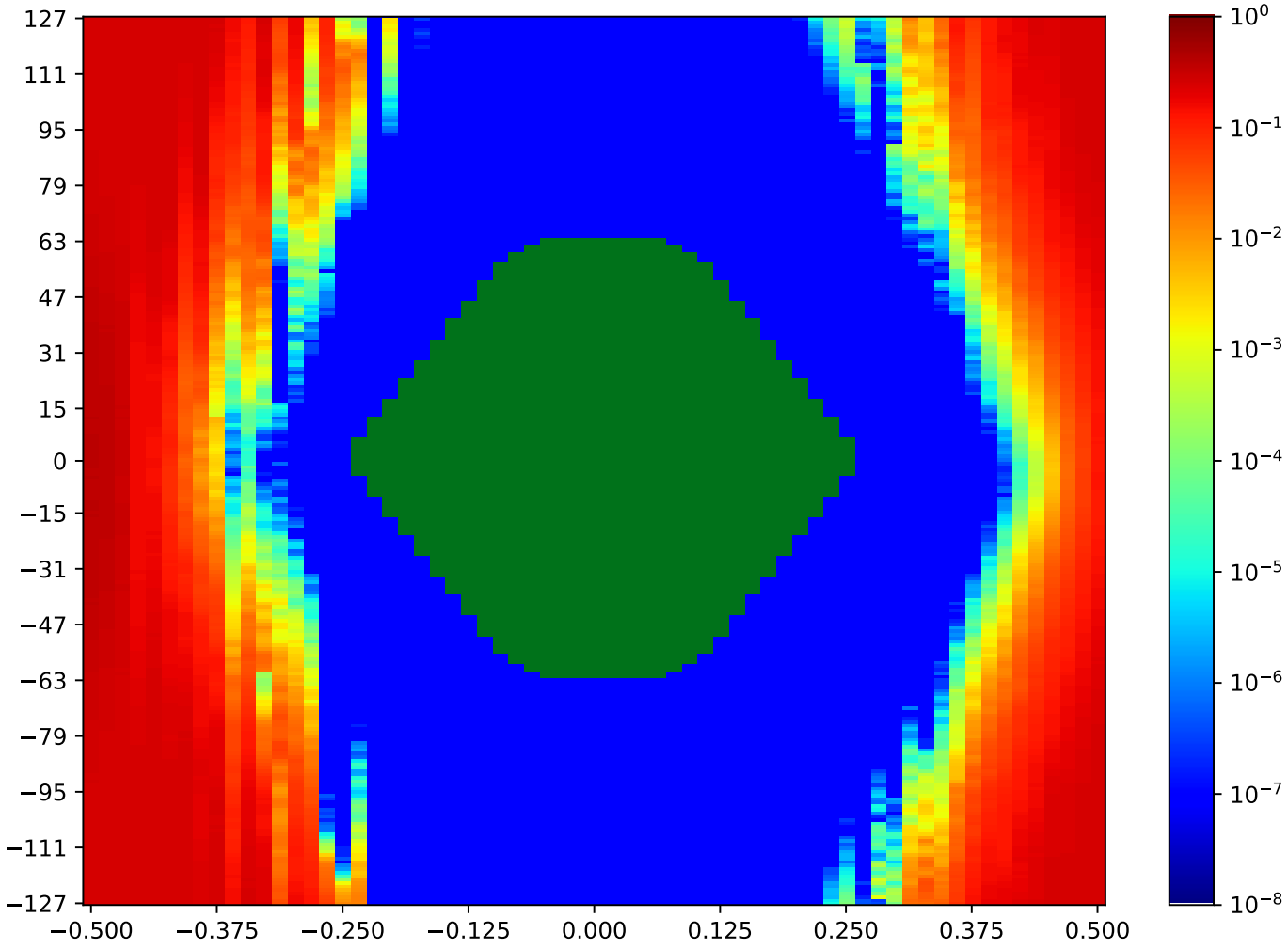


Figure 6.87: MSP_A_FPGA-IC39-17–IC4-17-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.19 MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Table 6.80: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:49:37		2019-Nov-26 17:49:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9818	48	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

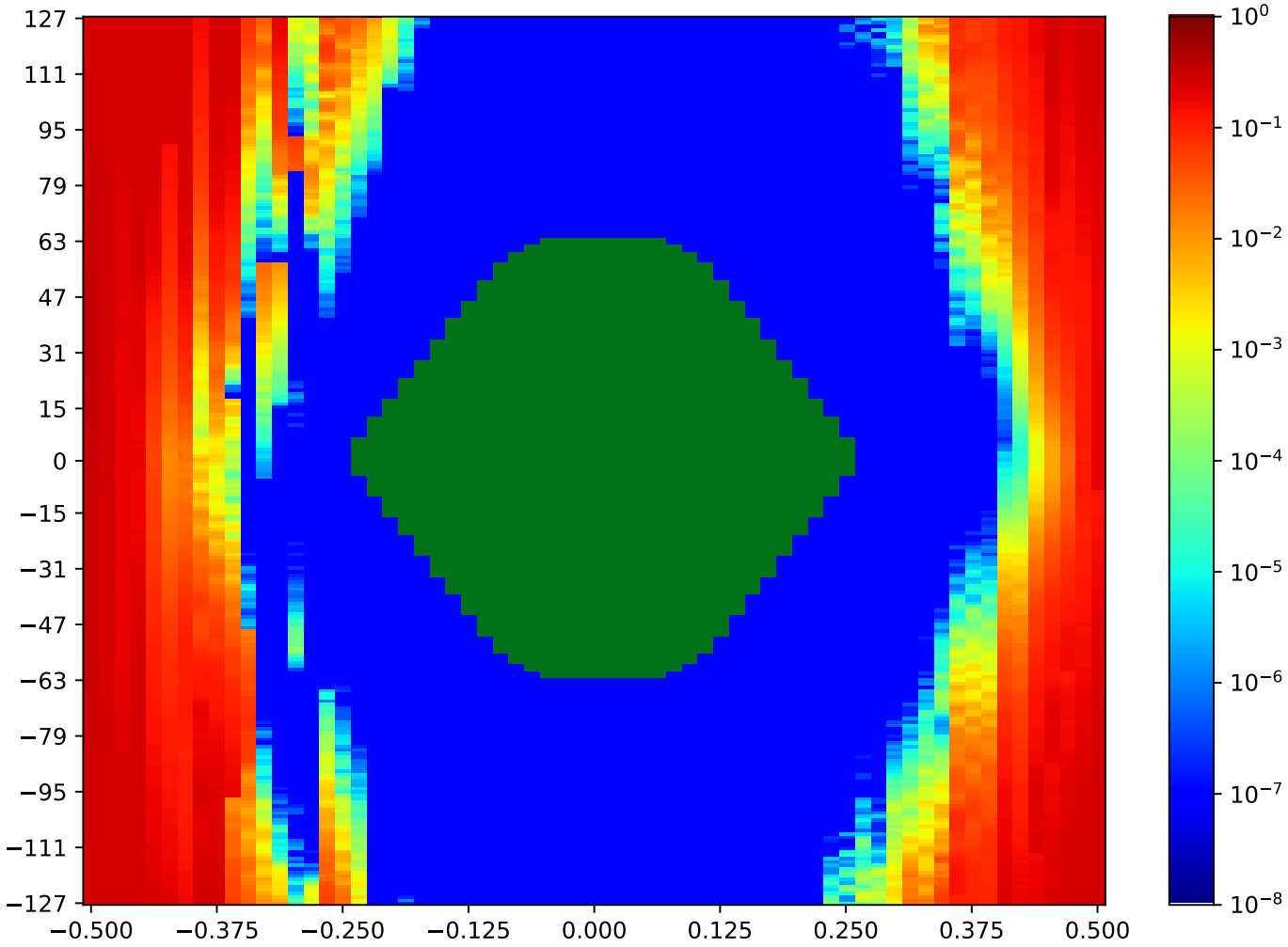


Figure 6.88: MSP_A_FPGA-IC39-18–IC4-18-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.20 MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Table 6.81: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:49:56		2019-Nov-26 17:50:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9182	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

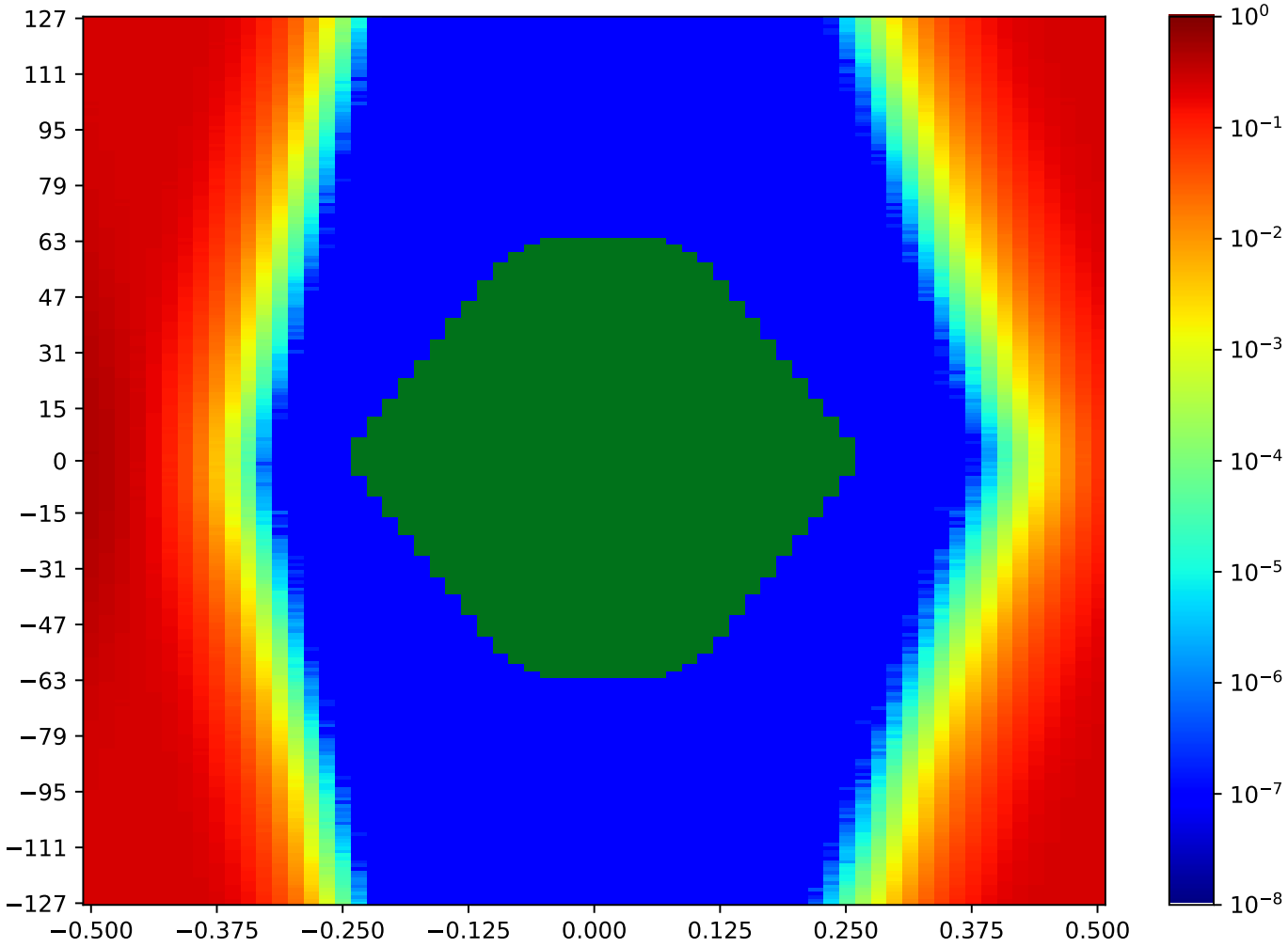


Figure 6.89: MSP_A_FPGA-IC39-19–IC4-19-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.21 MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Table 6.82: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:50:15		2019-Nov-26 17:50:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9516	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

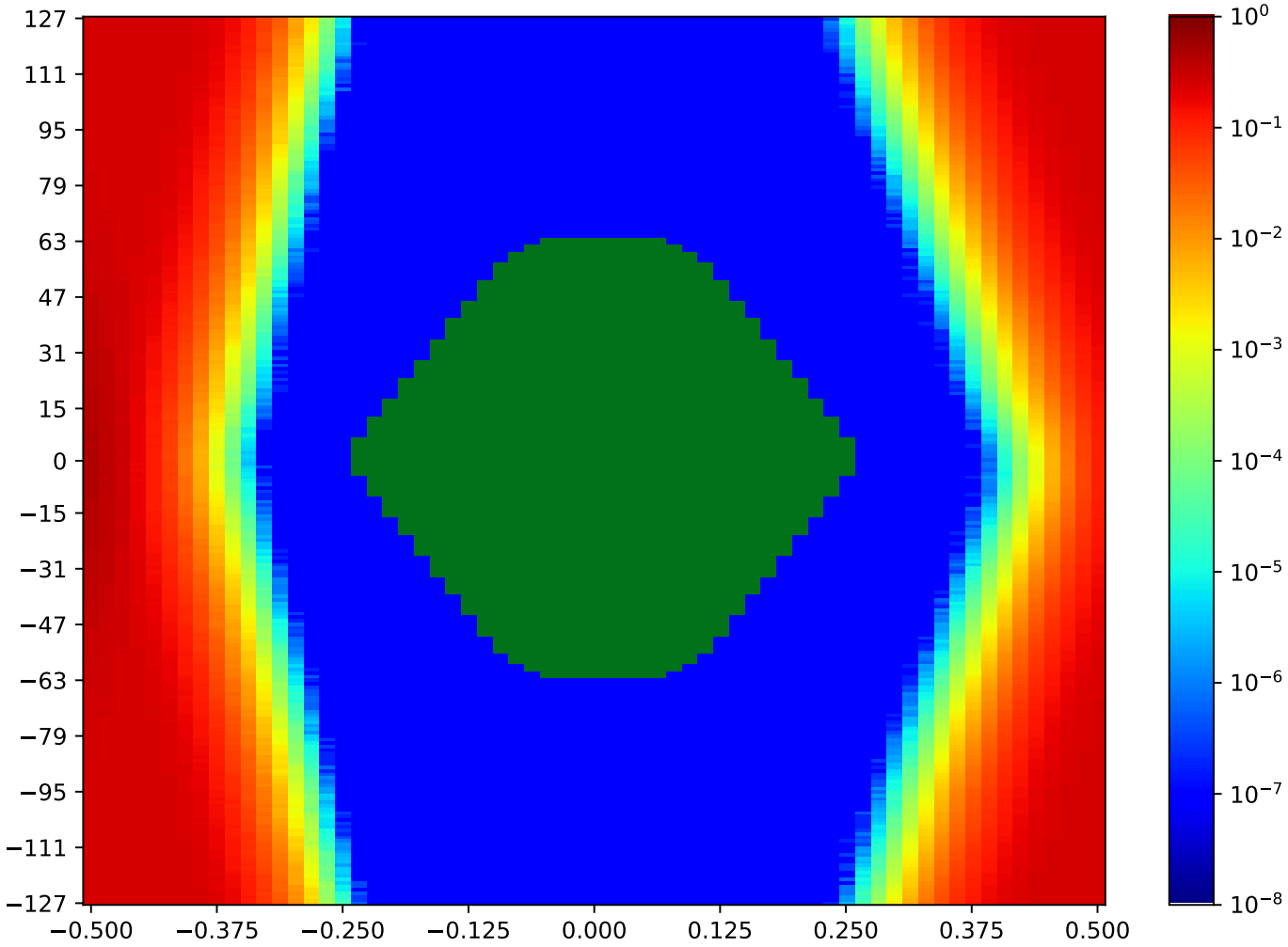


Figure 6.90: MSP_A_FPGA-IC39-20–IC4-20-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.22 MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Table 6.83: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:50:34		2019-Nov-26 17:50:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8659	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

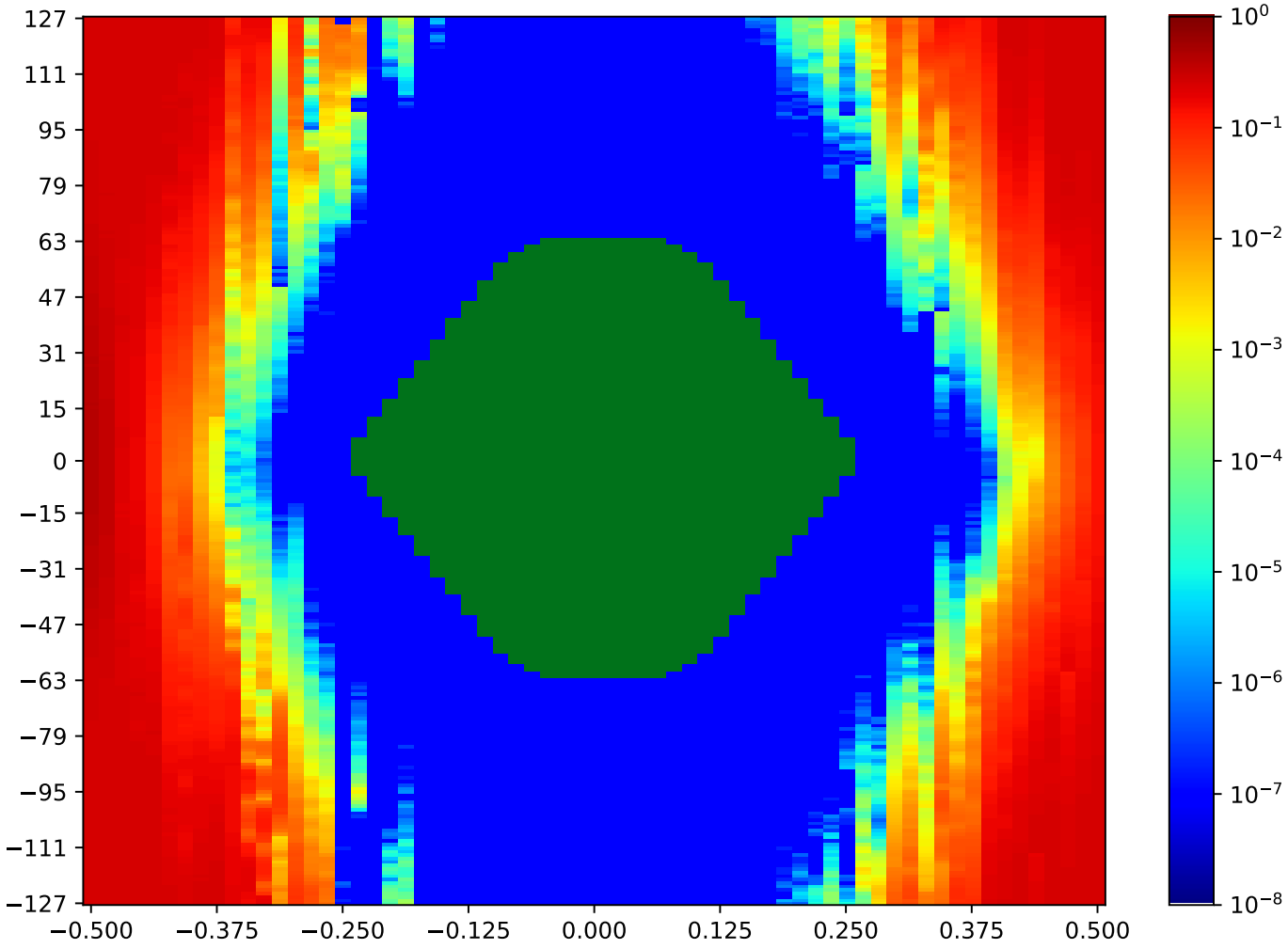


Figure 6.91: MSP_A_FPGA-IC39-21–IC4-21-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.23 MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Table 6.84: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:50:53		2019-Nov-26 17:51:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8903	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

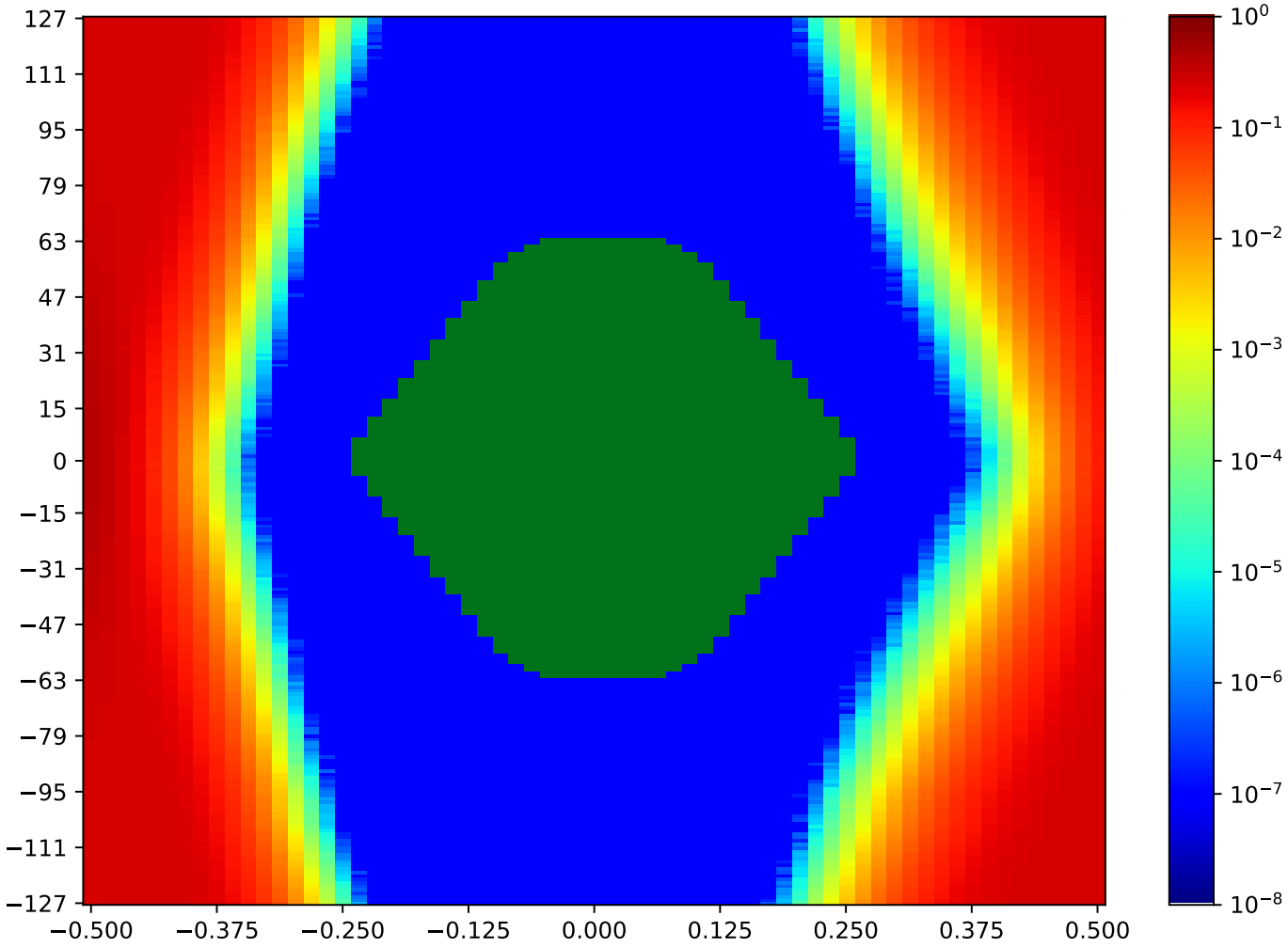


Figure 6.92: MSP_A_FPGA-IC39-22–IC4-22-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.24 MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Table 6.85: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:51:12		2019-Nov-26 17:51:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9746	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

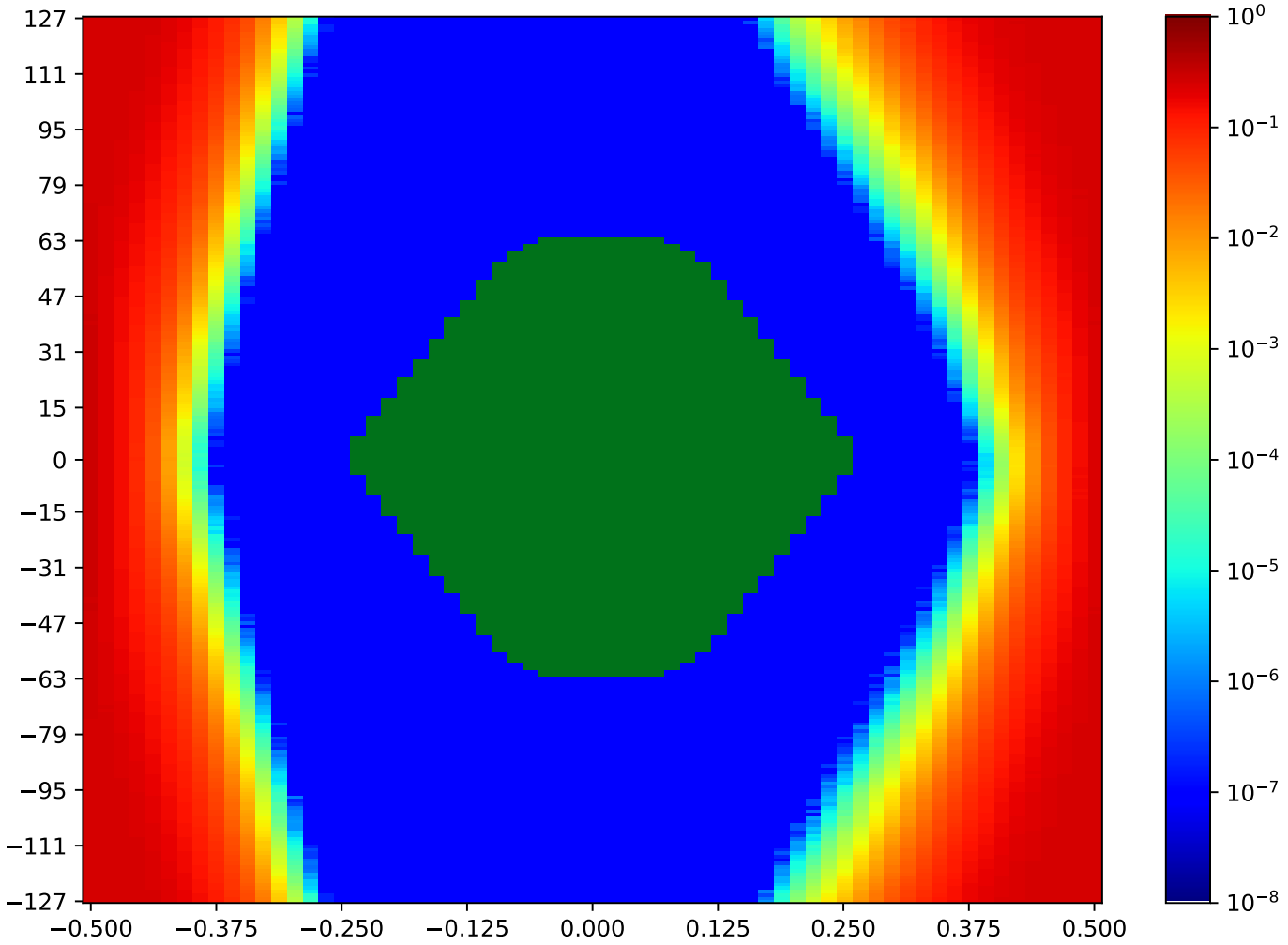


Figure 6.93: MSP_A_FPGA-IC39-23–IC4-23-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.25 MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Table 6.86: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:51:31		2019-Nov-26 17:51:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9250	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

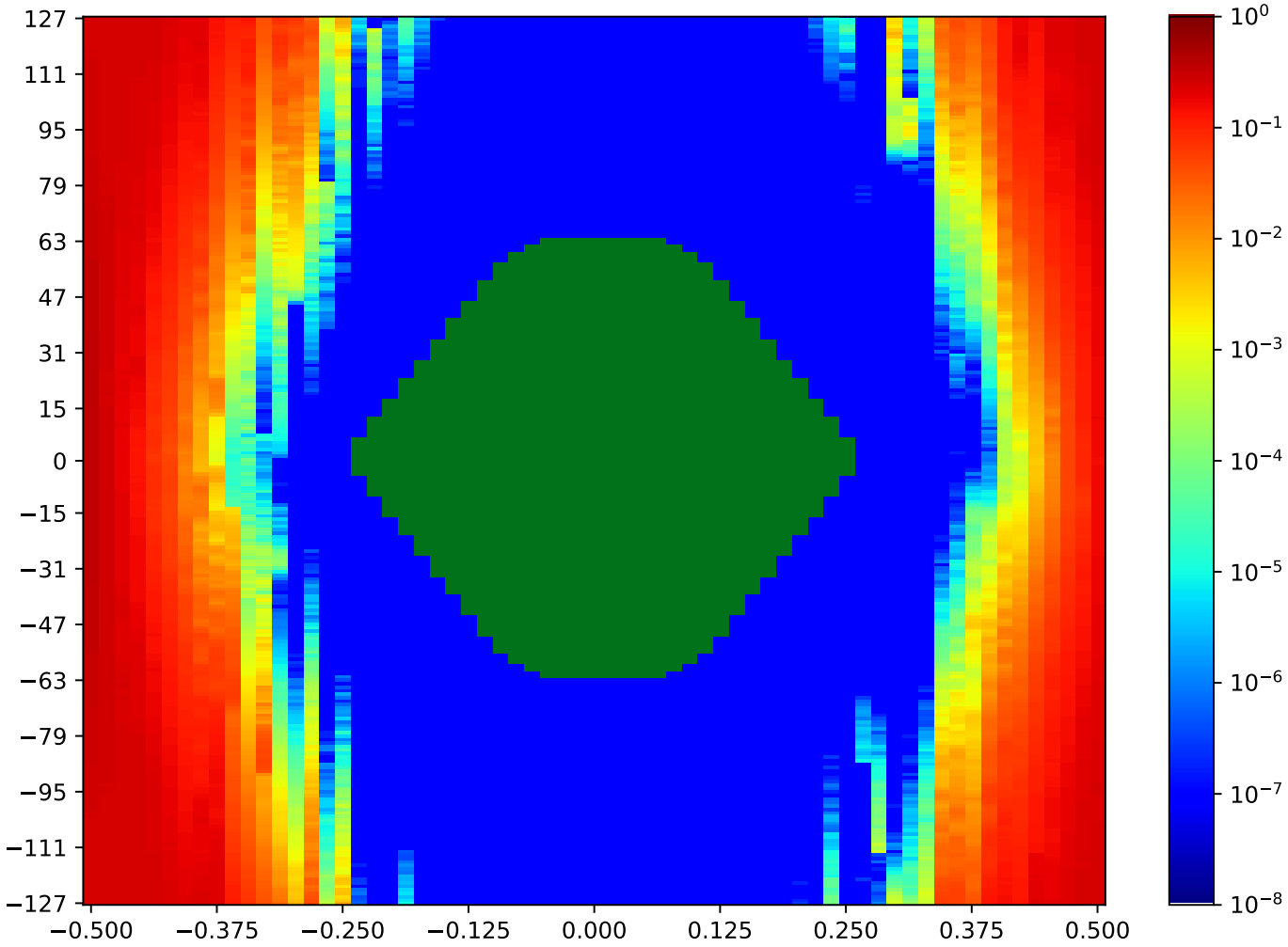


Figure 6.94: MSP_A_FPGA-IC39-24–IC4-24-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.26 MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Table 6.87: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:51:50		2019-Nov-26 17:52:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8555	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

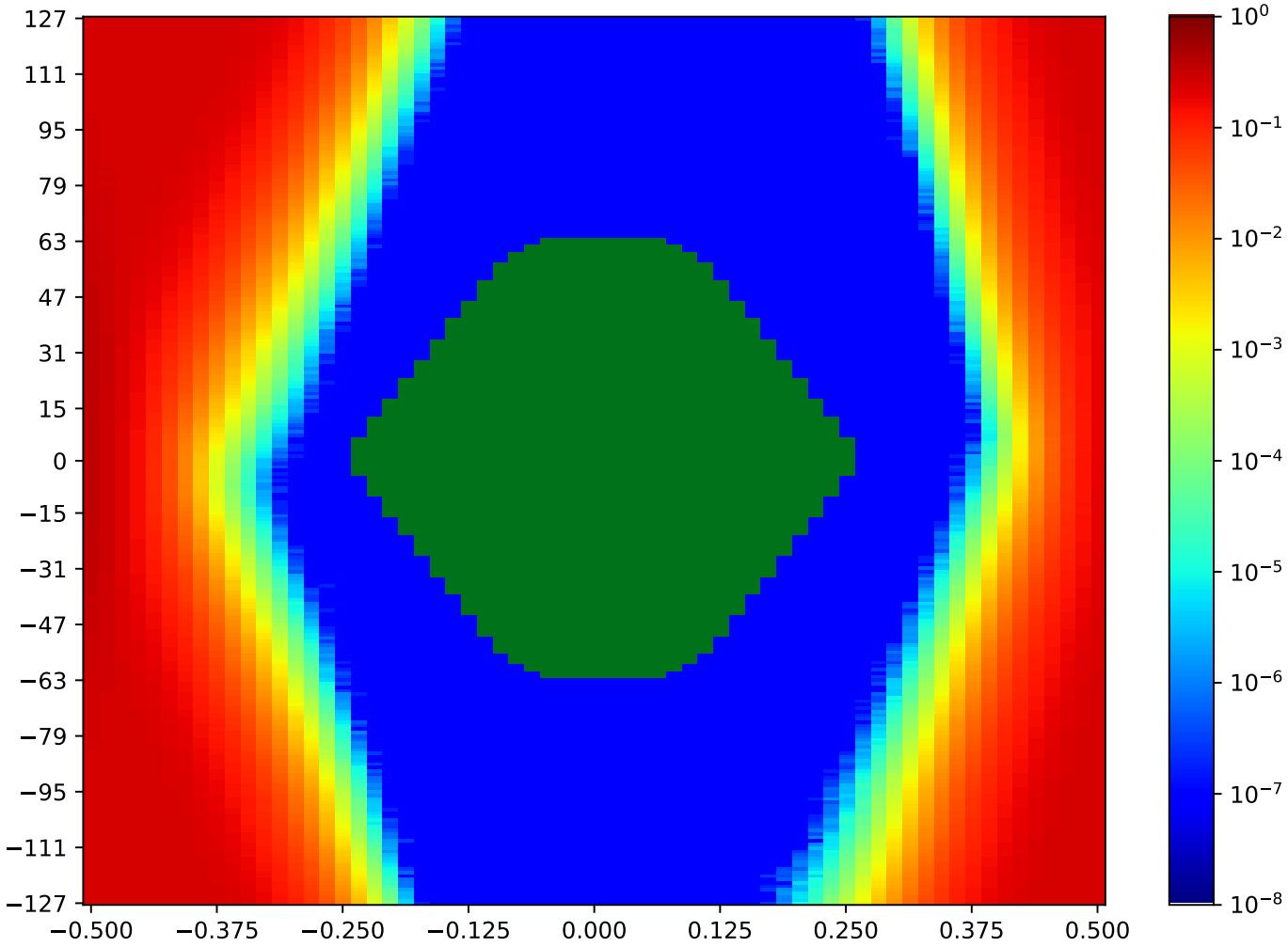


Figure 6.95: MSP_A_FPGA-IC39-25–IC4-25-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.27 MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Table 6.88: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:52:09		2019-Nov-26 17:52:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9732	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

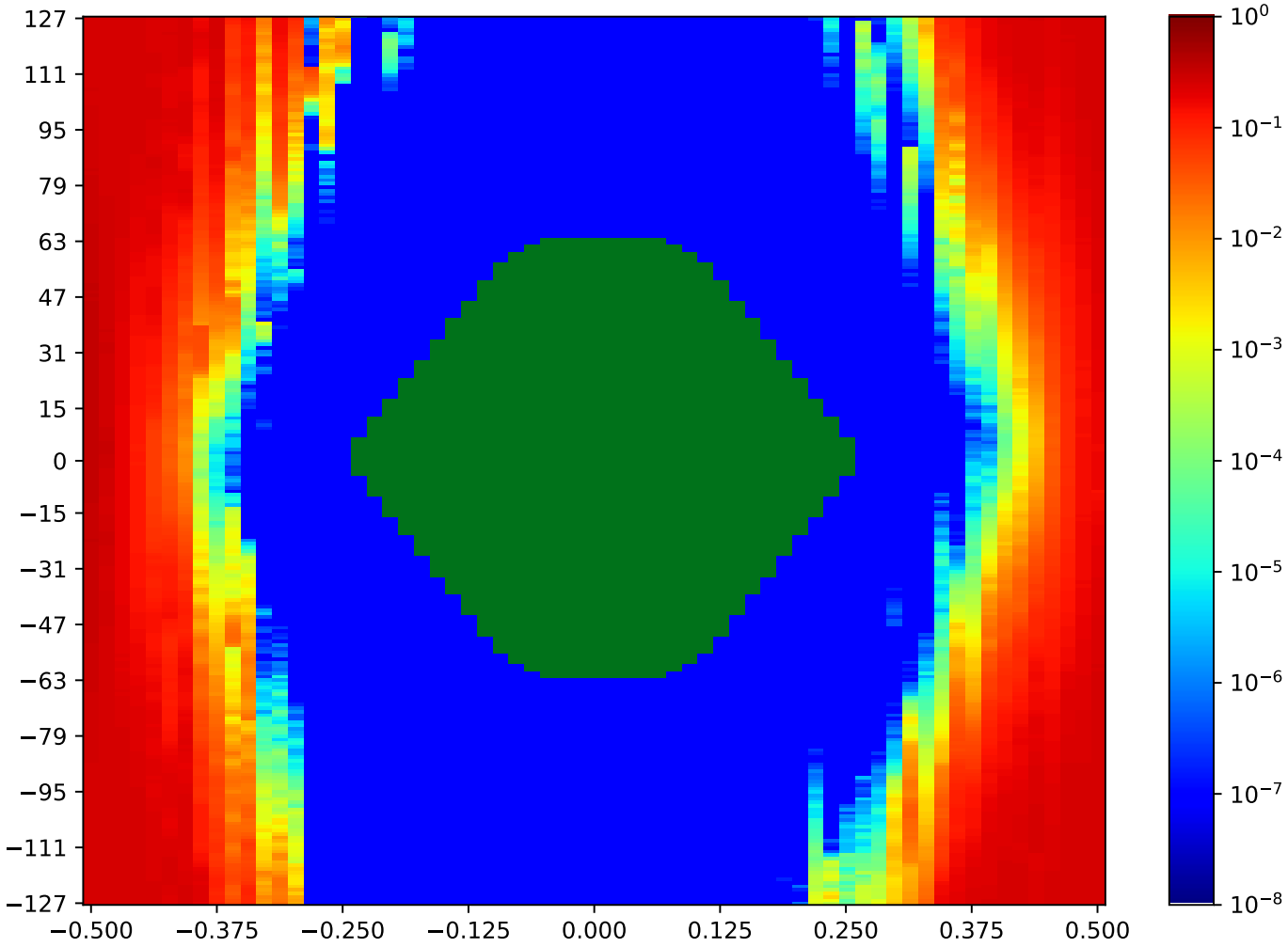


Figure 6.96: MSP_A_FPGA-IC39-26–IC4-26-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.8.28 MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Table 6.89: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTH	2019-Nov-26 17:52:28		2019-Nov-26 17:52:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9285	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

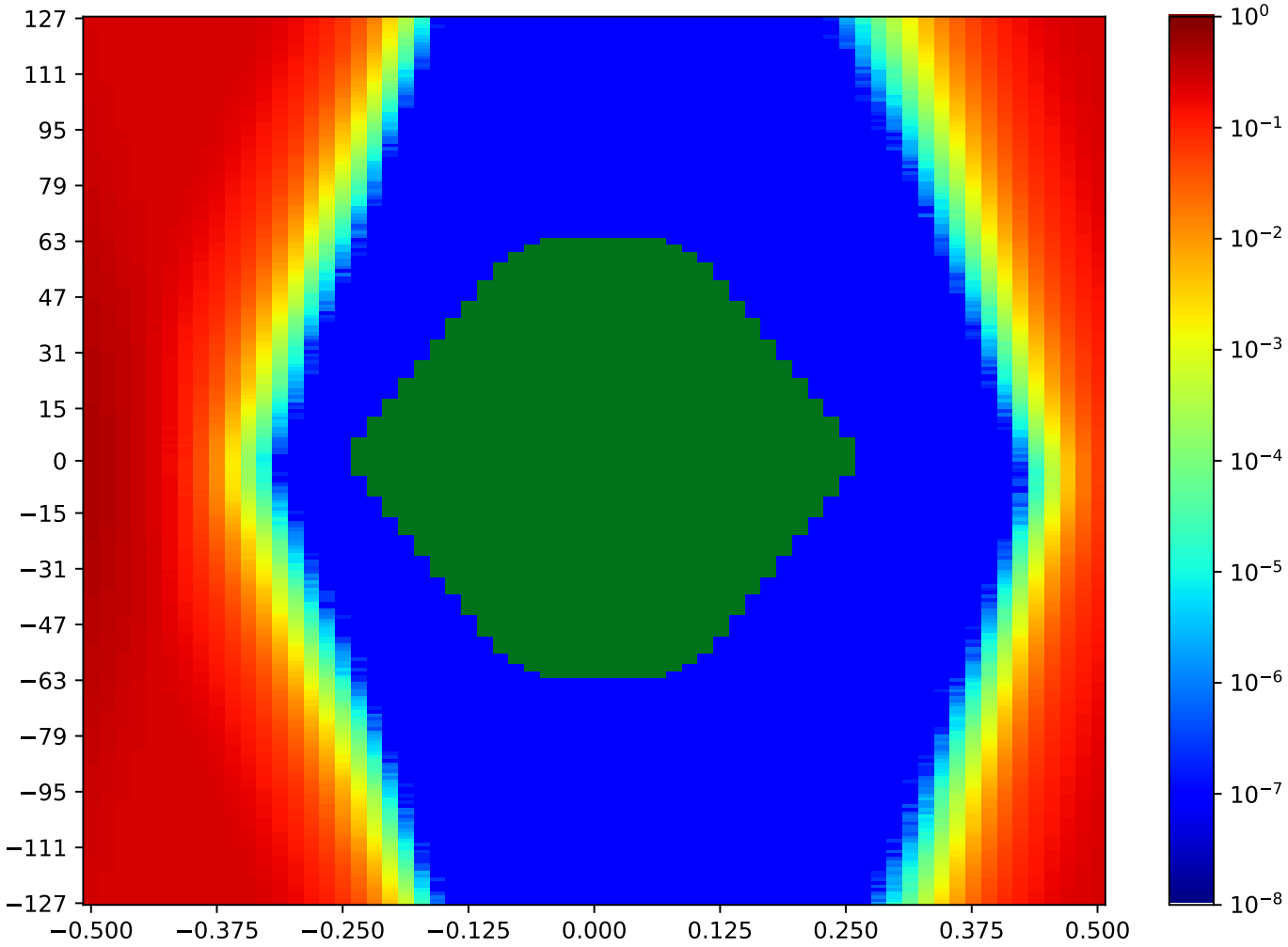


Figure 6.97: MSP_A_FPGA-IC39-27–IC4-27-TRP_FPGA

Call back to summary Figure 6.69. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9 MSP_C TRP On board links

A cross-reference to Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.127.

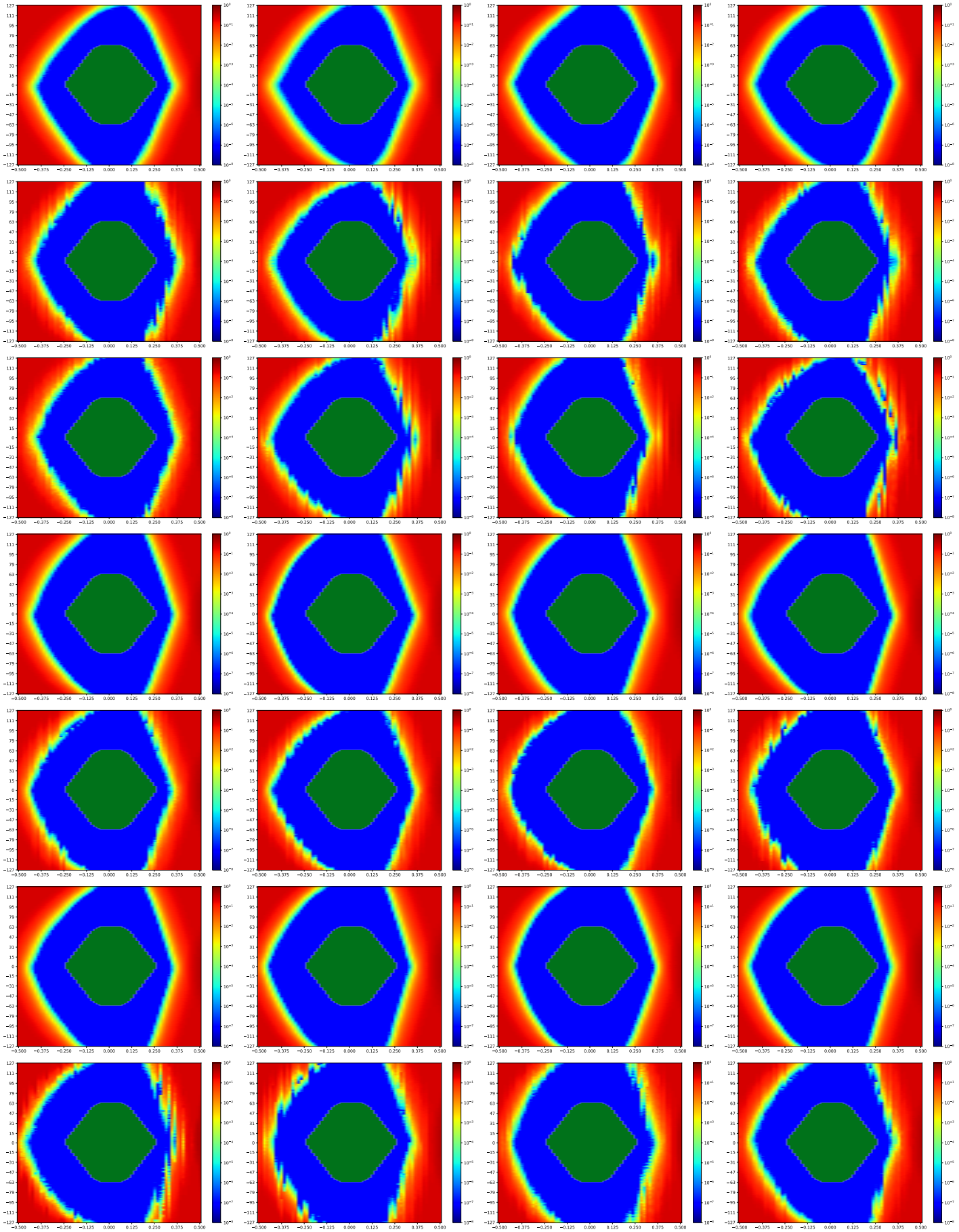


Figure 6.98: MSP_C TRP On board links

6.9.1 MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Table 6.90: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:52:48		2019-Nov-26 17:53:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7553	46	70.77%	245	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

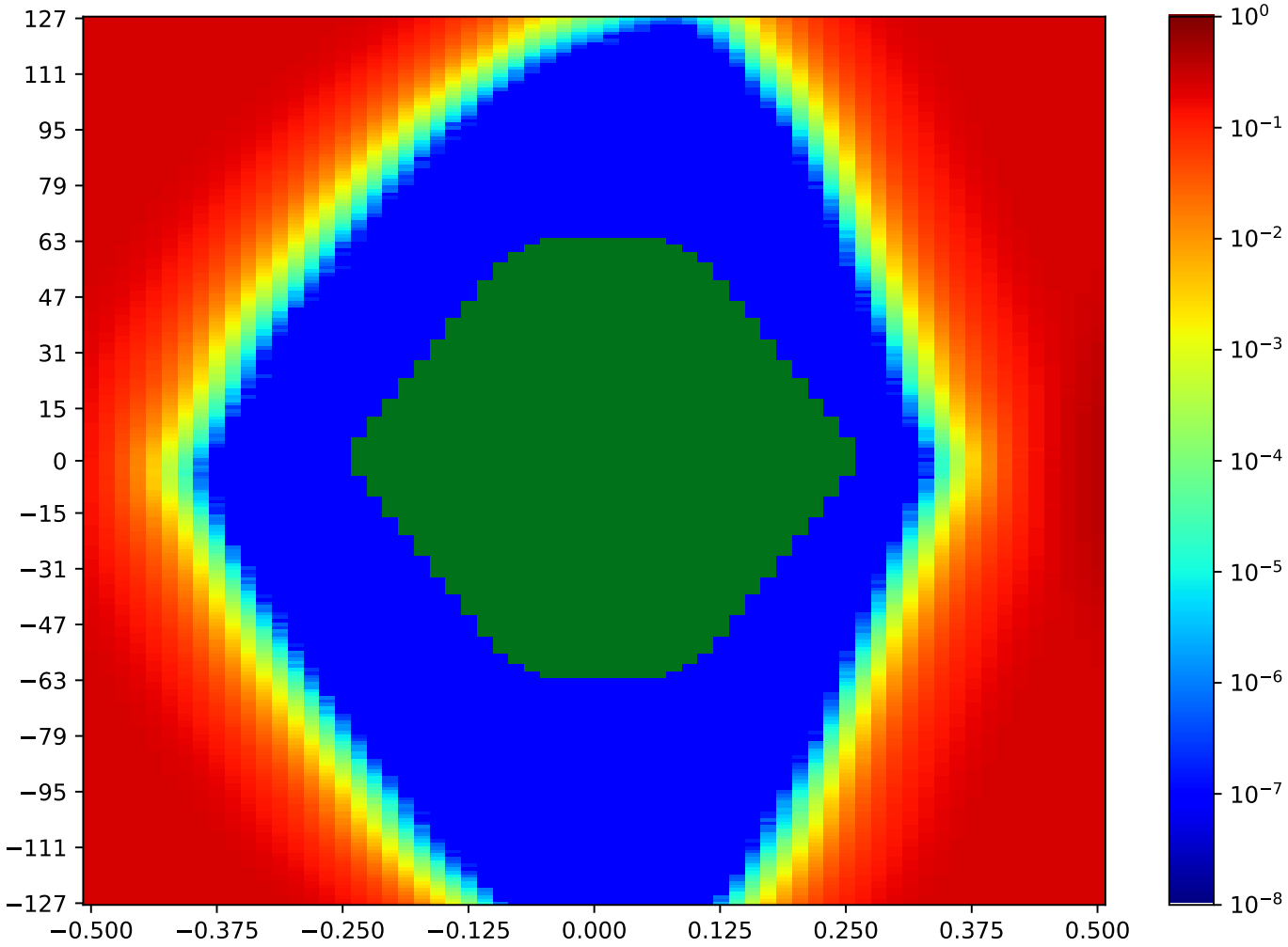


Figure 6.99: MSP_C_FPGA-IC39-00–IC15-00-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.2 MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Table 6.91: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:53:11		2019-Nov-26 17:53:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7408	44	67.69%	247	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

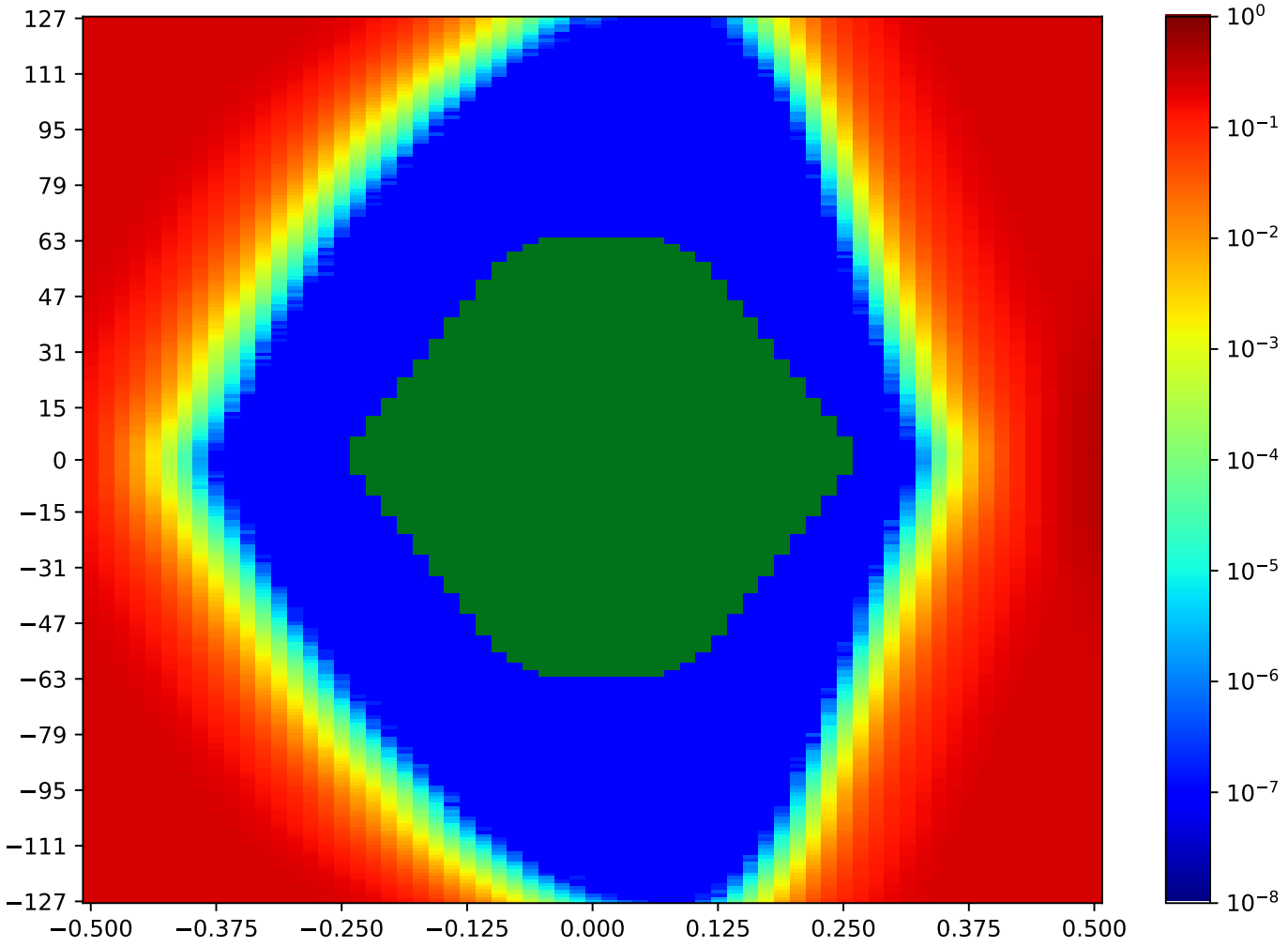


Figure 6.100: MSP_C_FPGA-IC39-01–IC15-01-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.3 MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Table 6.92: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:53:31		2019-Nov-26 17:53:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8465	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

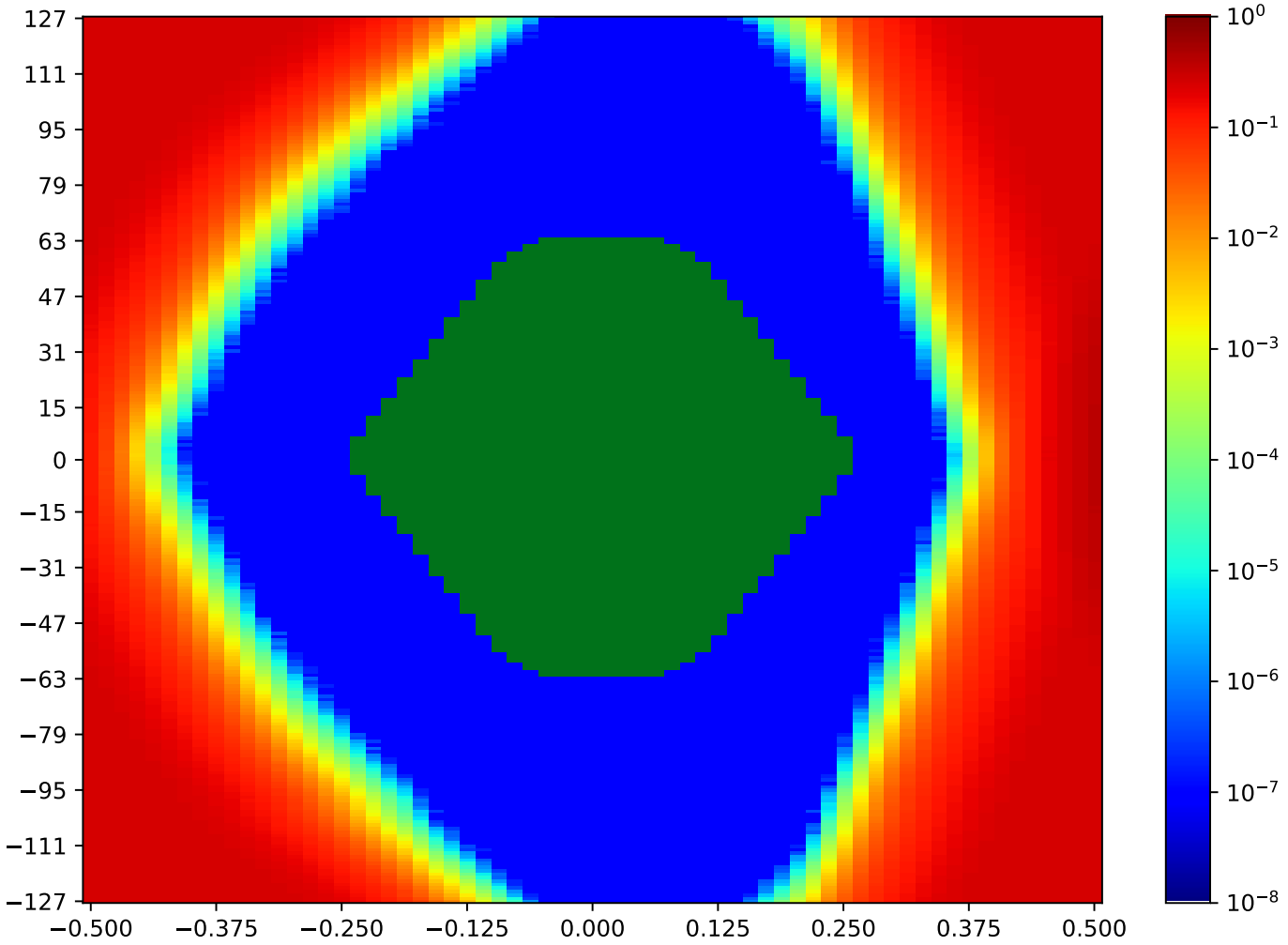


Figure 6.101: MSP_C_FPGA-IC39-02–IC15-02-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.4 MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Table 6.93: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:53:50		2019-Nov-26 17:54:09	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8170	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

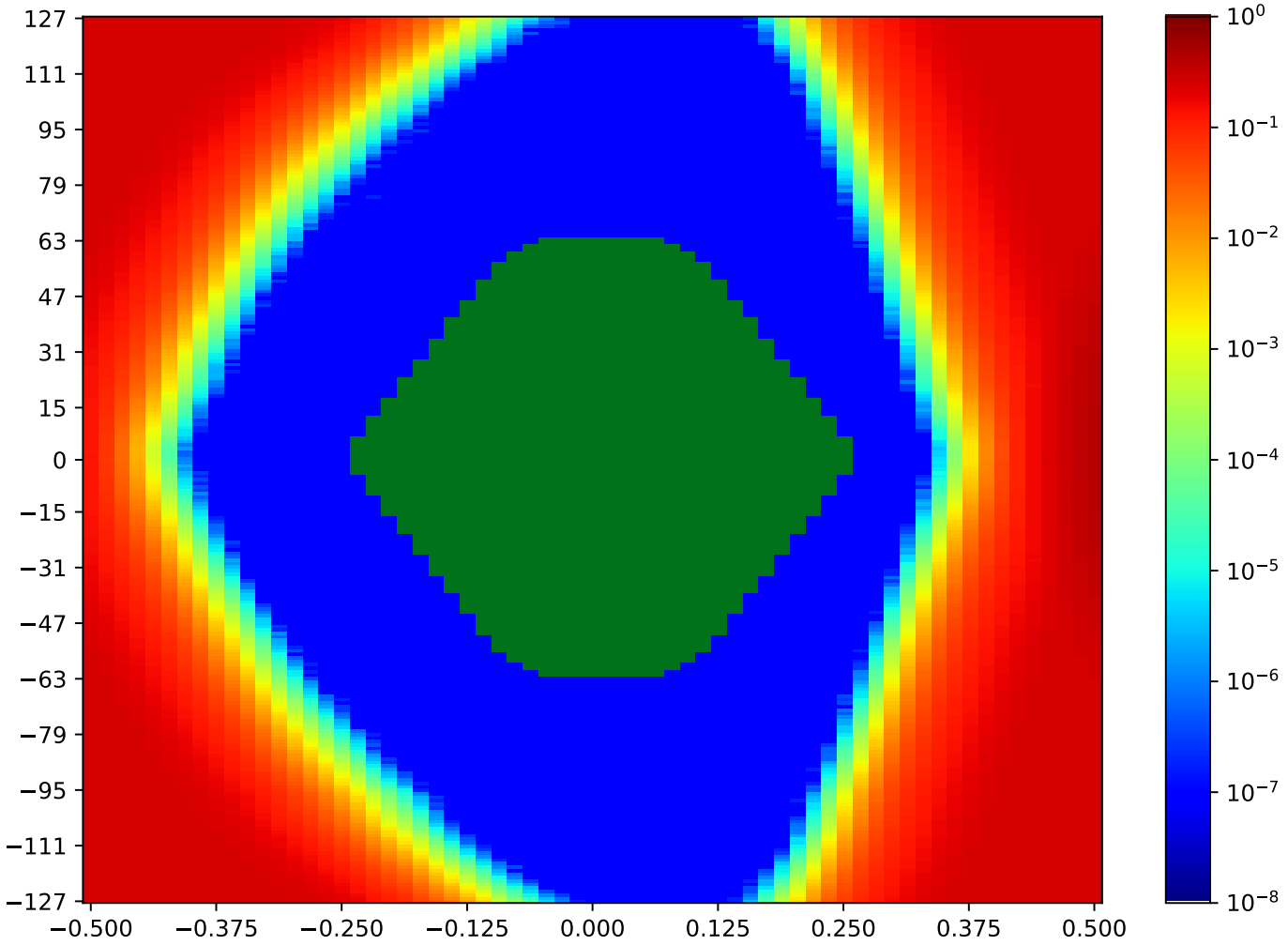


Figure 6.102: MSP_C_FPGA-IC39-03–IC15-03-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.5 MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Table 6.94: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:54:09		2019-Nov-26 17:54:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8738	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

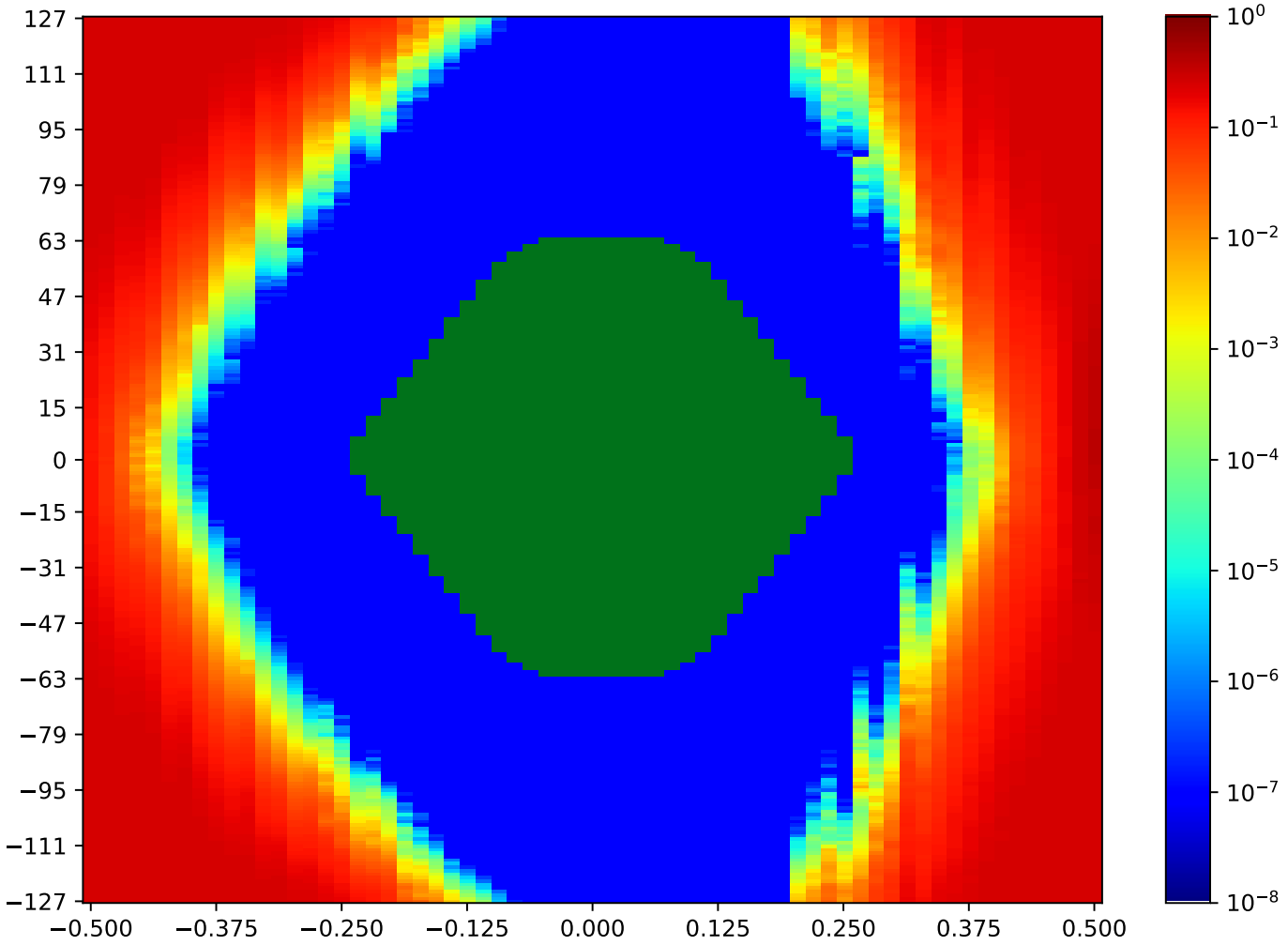


Figure 6.103: MSP_C_FPGA-IC39-04–IC15-04-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.6 MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Table 6.95: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:54:33		2019-Nov-26 17:54:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7845	45	69.23%	246	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

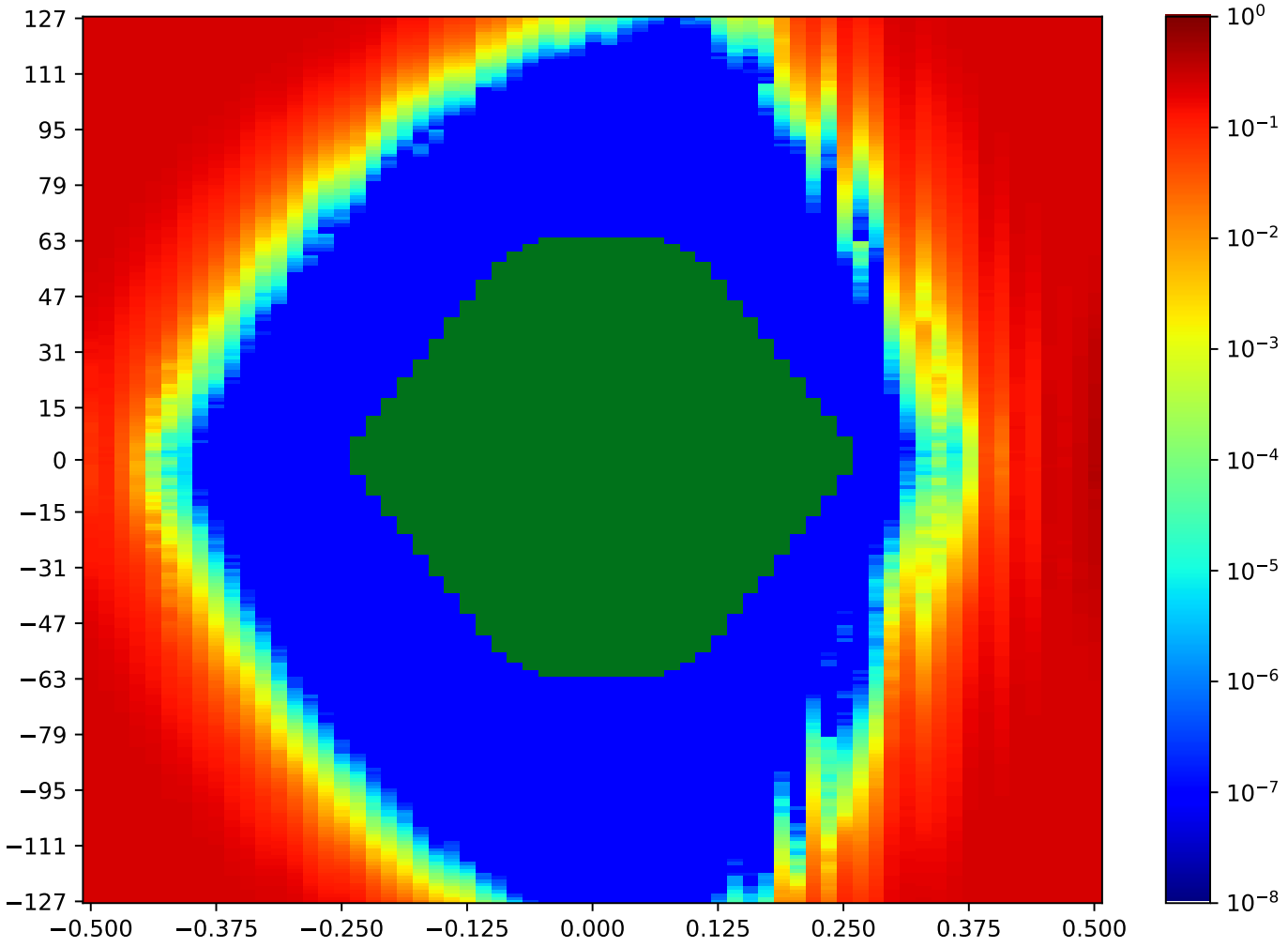


Figure 6.104: MSP_C_FPGA-IC39-05–IC15-05-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.7 MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Table 6.96: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:54:52		2019-Nov-26 17:55:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8661	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

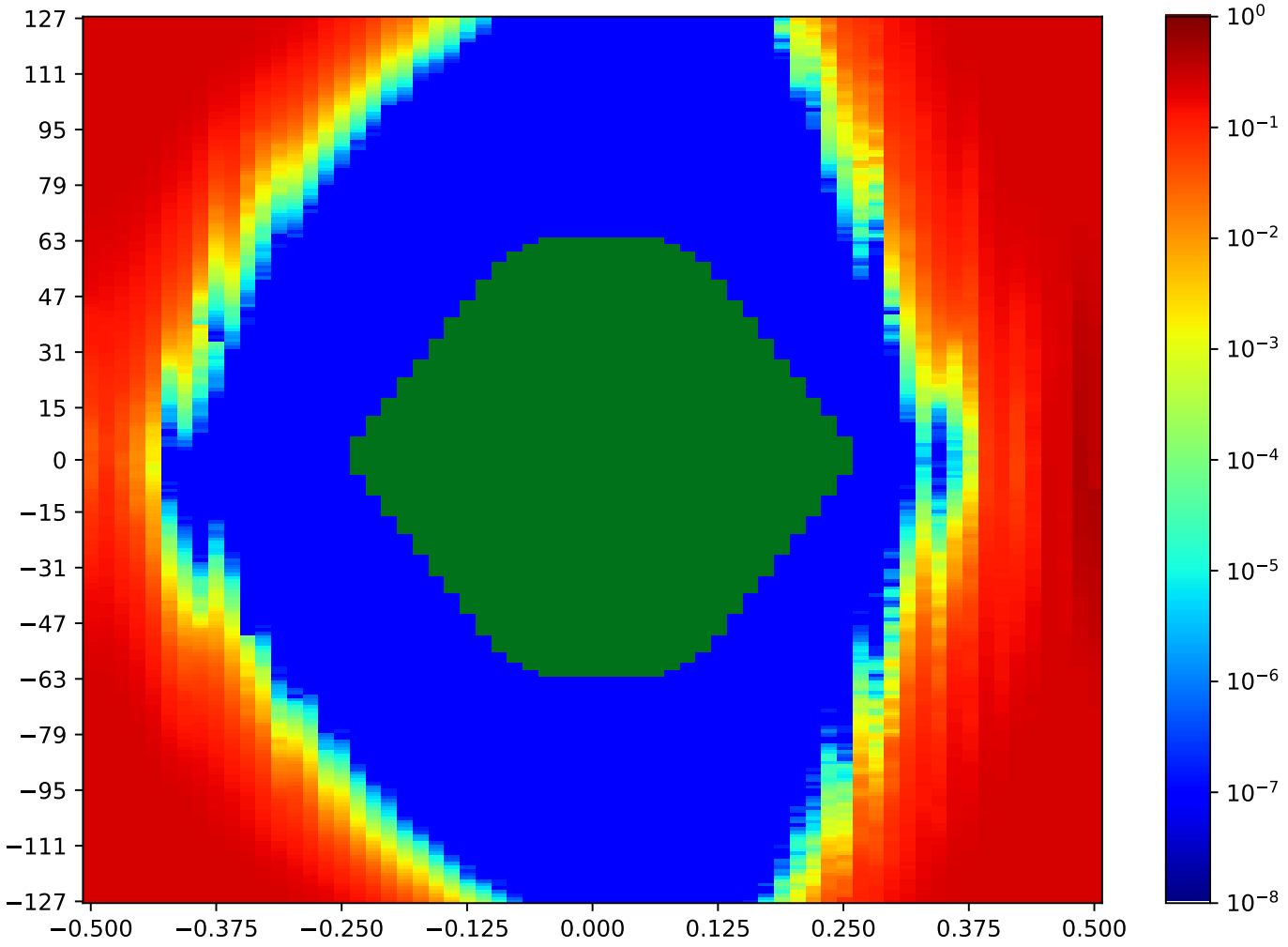


Figure 6.105: MSP_C_FPGA-IC39-06–IC15-06-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.8 MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Table 6.97: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:55:11		2019-Nov-26 17:55:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8512	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

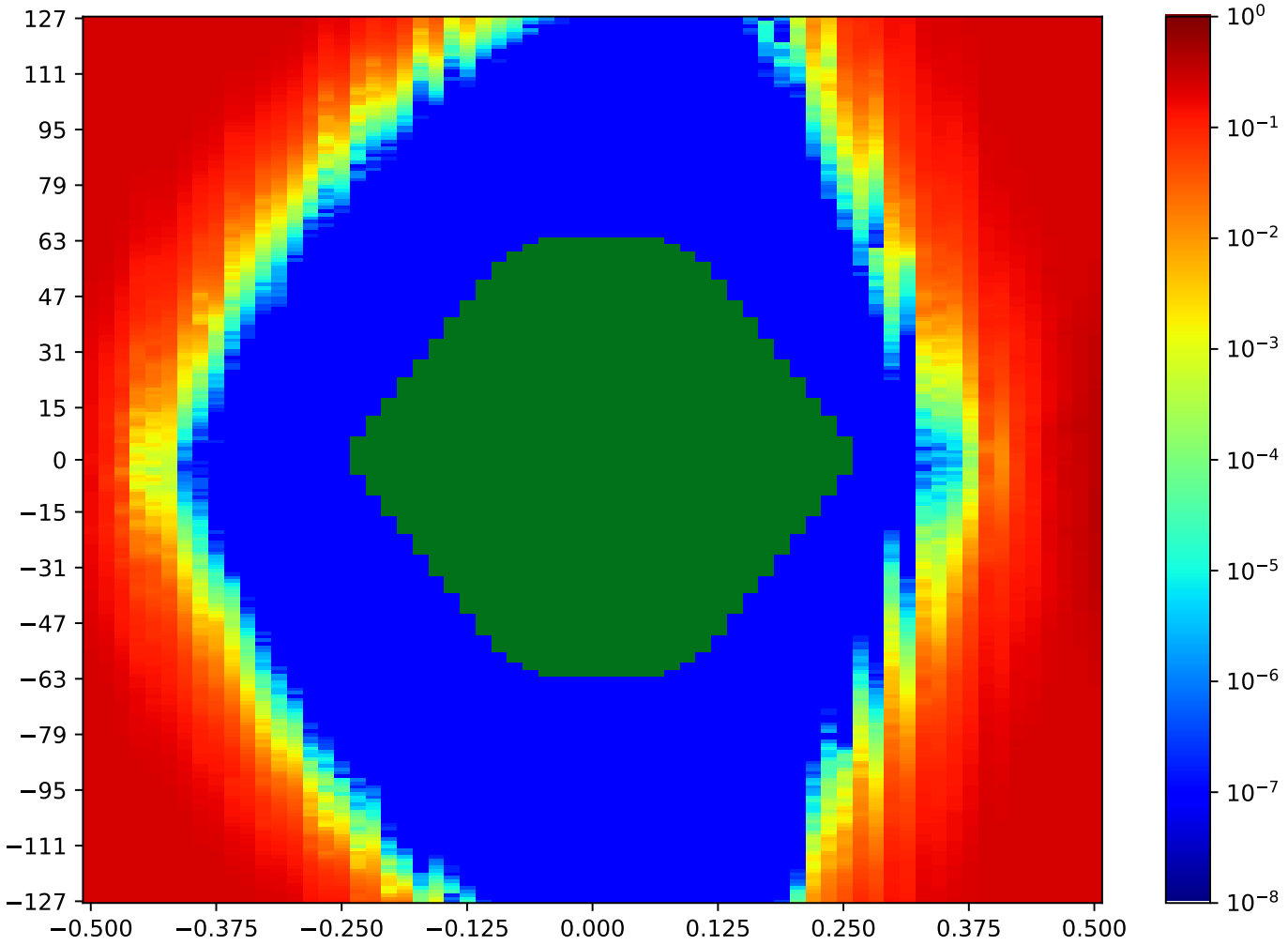


Figure 6.106: MSP_C_FPGA-IC39-07–IC15-07-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.9 MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Table 6.98: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:55:30		2019-Nov-26 17:55:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8443	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

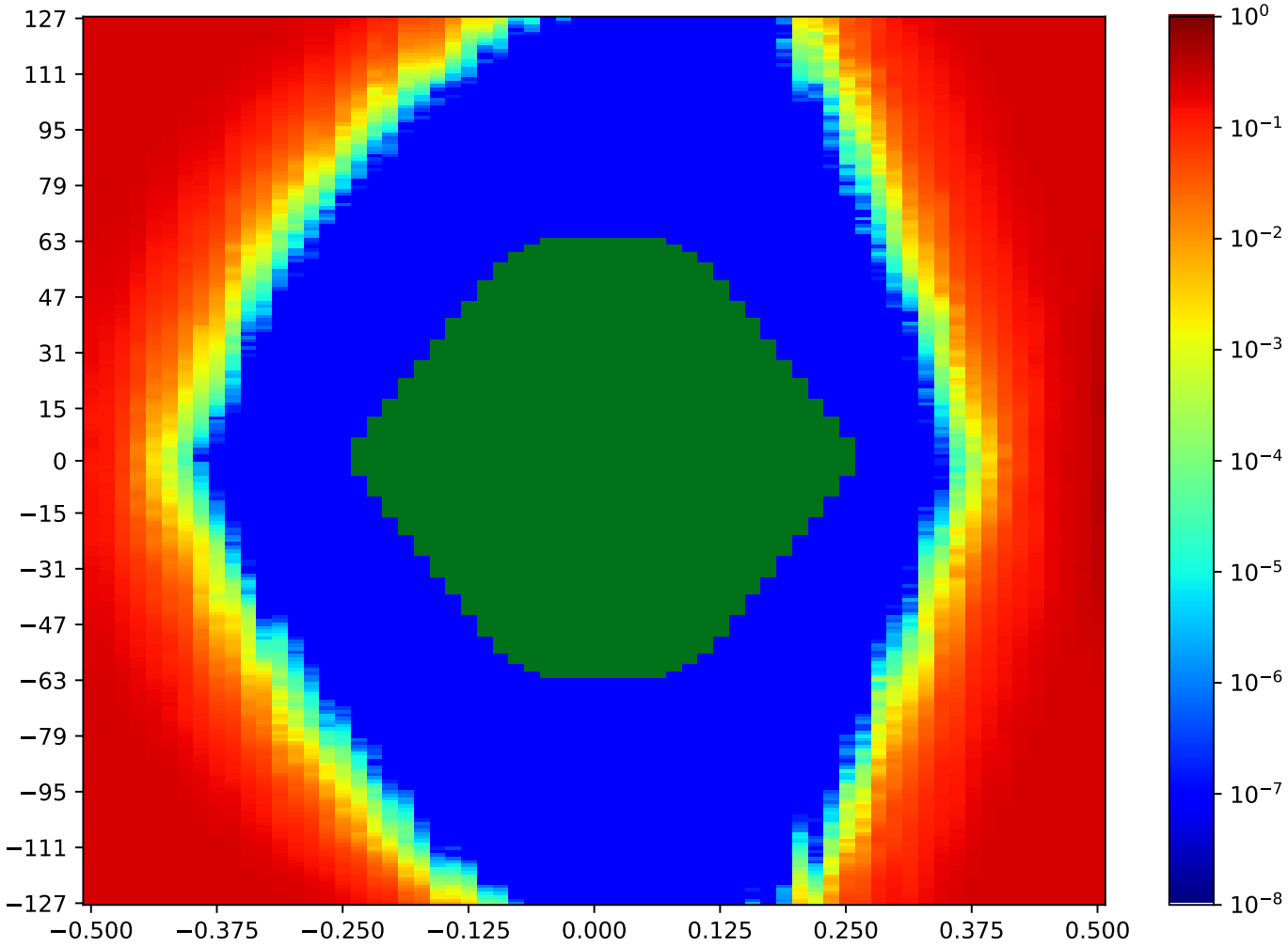


Figure 6.107: MSP_C_FPGA-IC39-08–IC15-08-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.10 MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Table 6.99: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:55:49		2019-Nov-26 17:56:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8354	48	73.85%	252	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

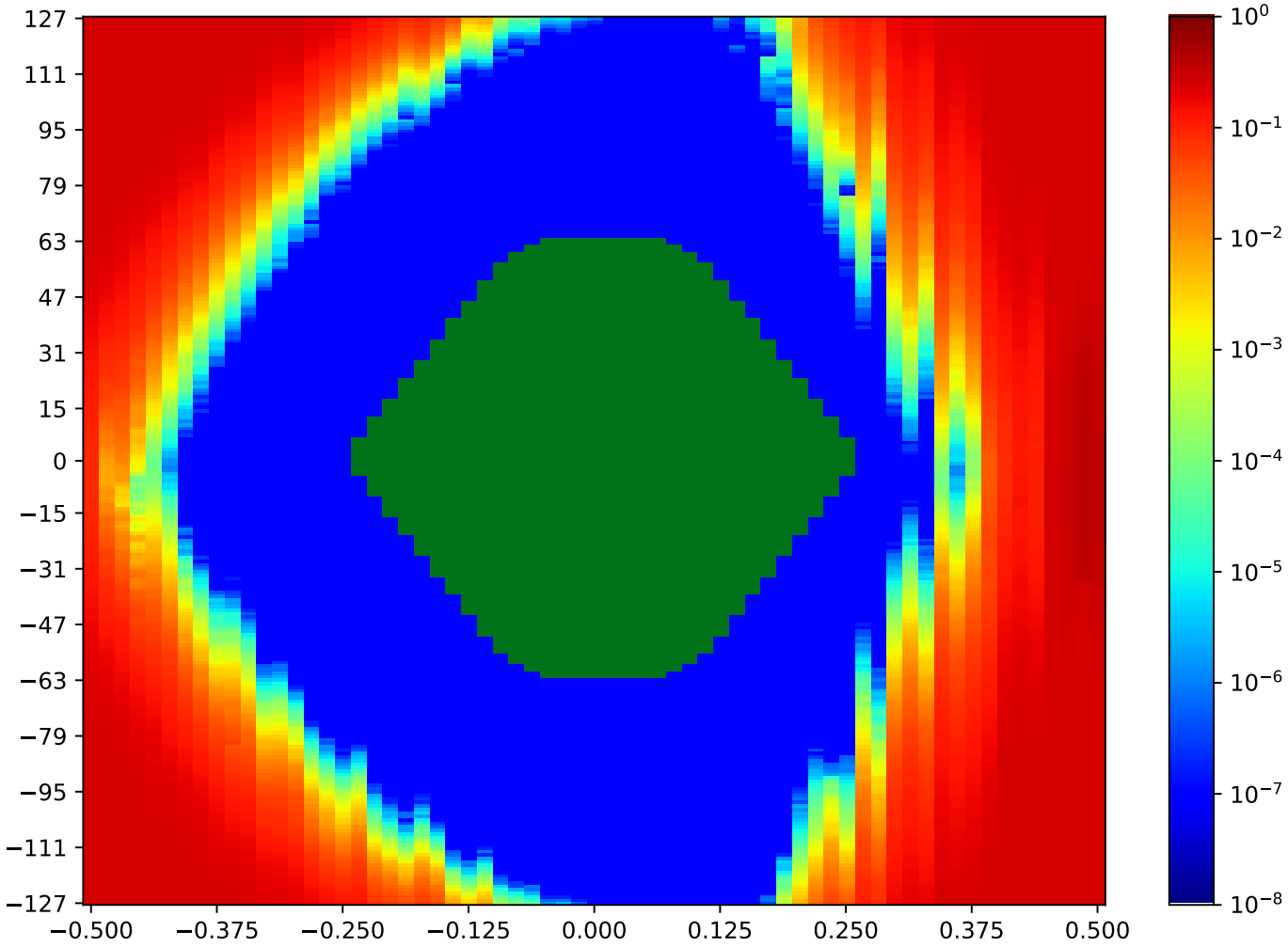


Figure 6.108: MSP_C_FPGA-IC39-09–IC15-09-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.11 MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Table 6.100: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:56:08		2019-Nov-26 17:56:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8531	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

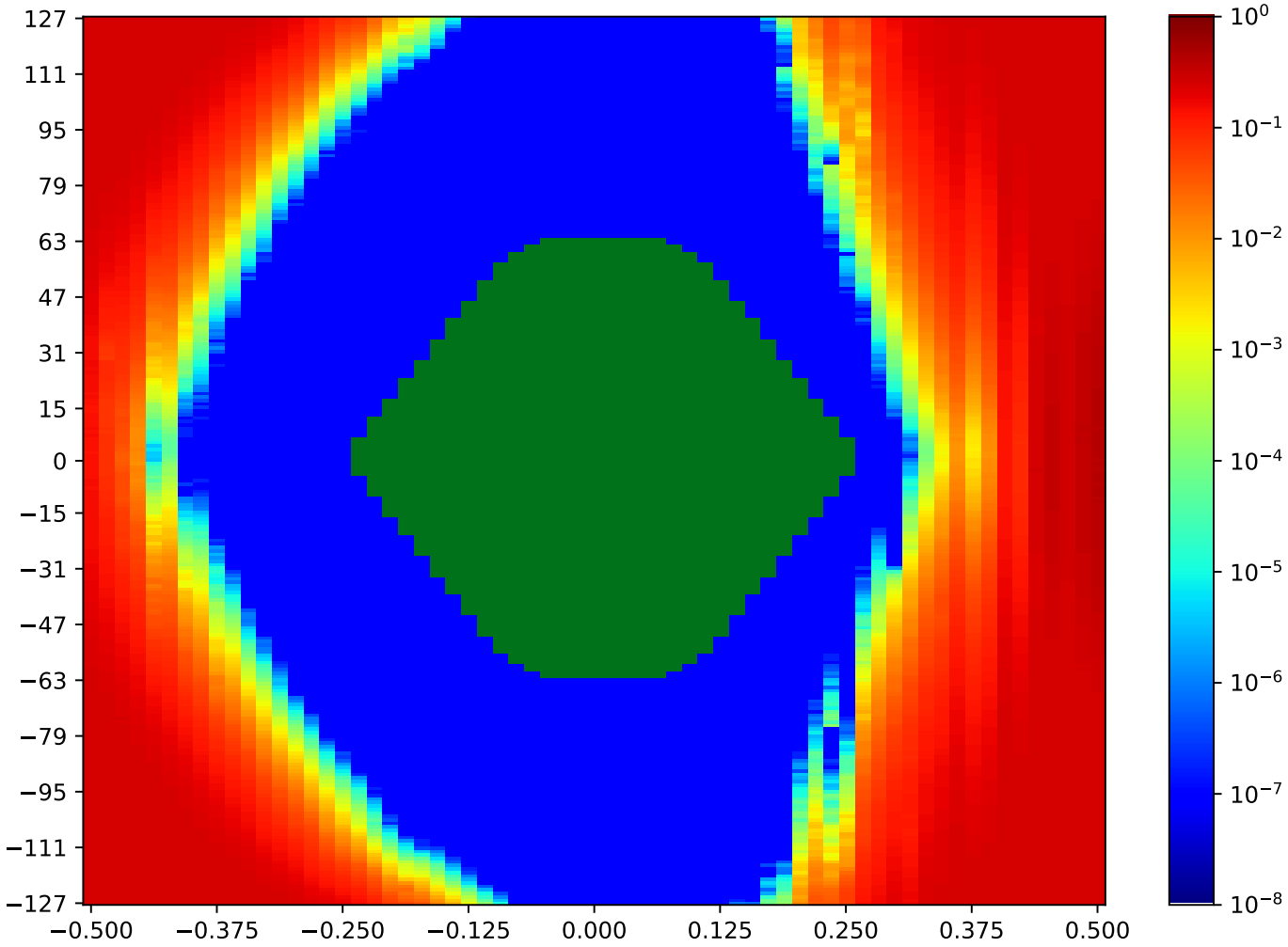


Figure 6.109: MSP_C_FPGA-IC39-10–IC15-10-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.12 MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Table 6.101: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:56:27		2019-Nov-26 17:56:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8727	51	75.38%	251	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

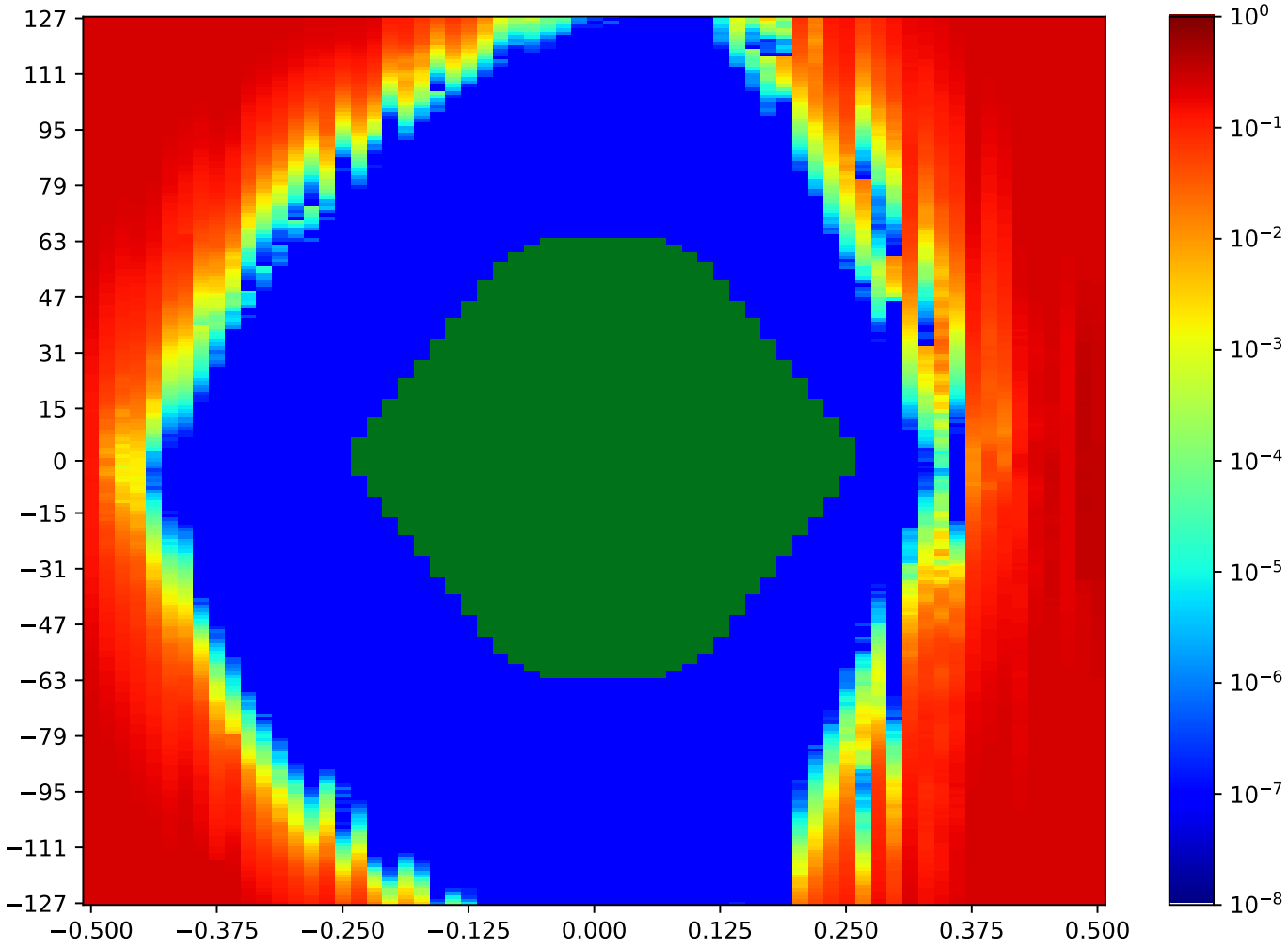


Figure 6.110: MSP_C_FPGA-IC39-11–IC15-11-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.13 MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Table 6.102: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:56:46		2019-Nov-26 17:57:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8832	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

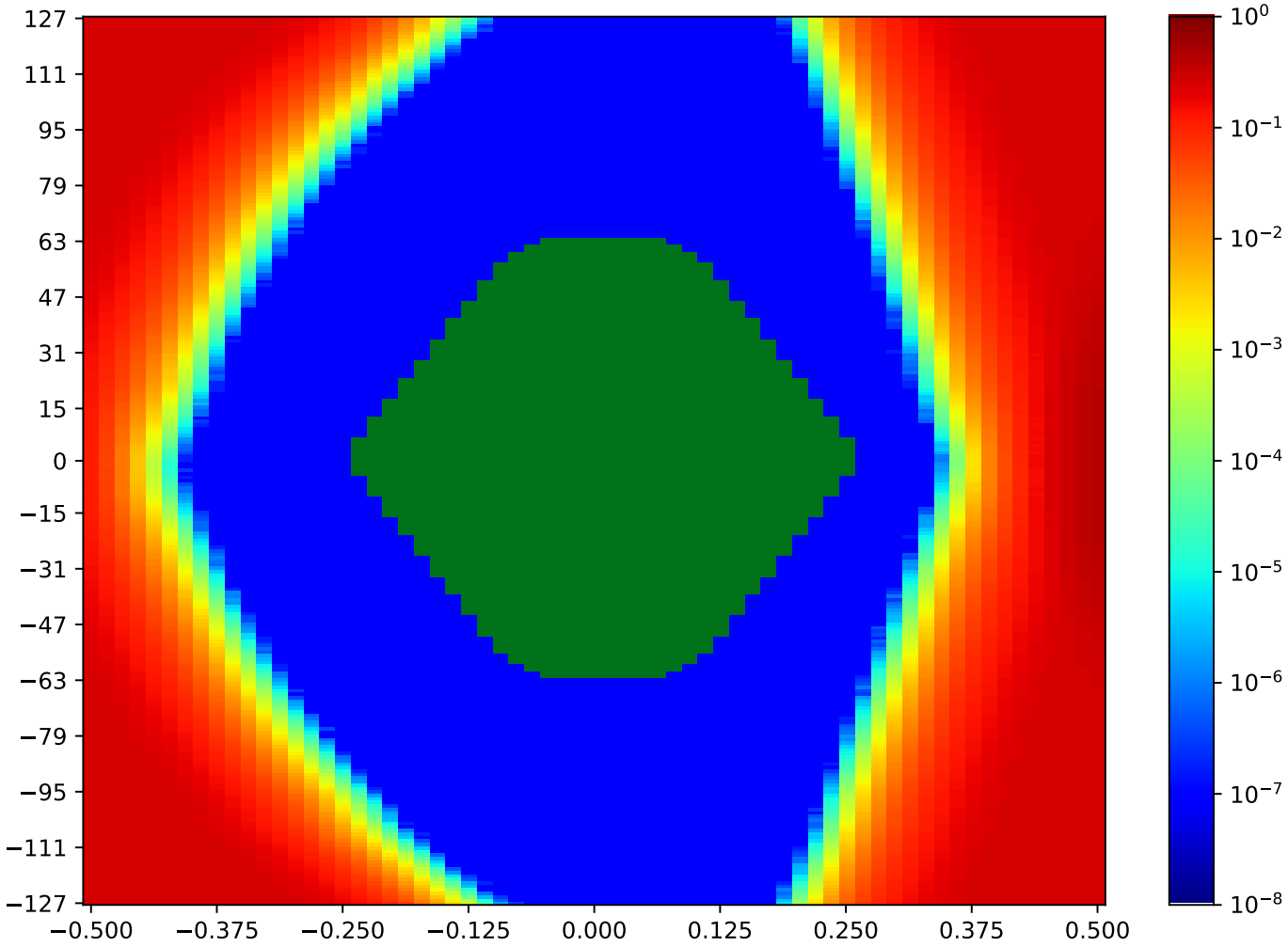


Figure 6.111: MSP_C_FPGA-IC39-12–IC15-12-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.14 MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Table 6.103: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:57:11		2019-Nov-26 17:57:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9281	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

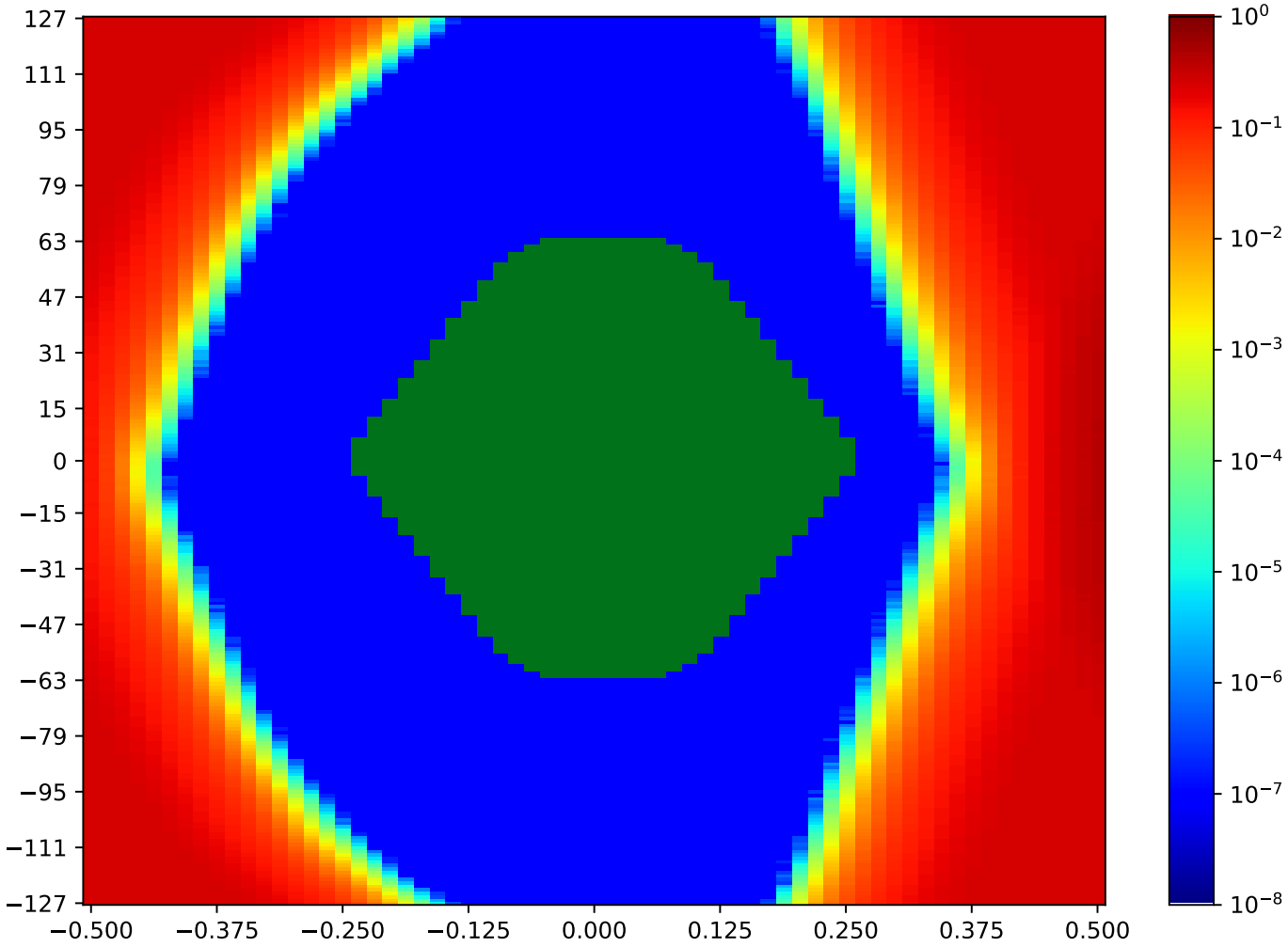


Figure 6.112: MSP_C_FPGA-IC39-13–IC15-13-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.15 MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Table 6.104: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:57:32		2019-Nov-26 17:57:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8831	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

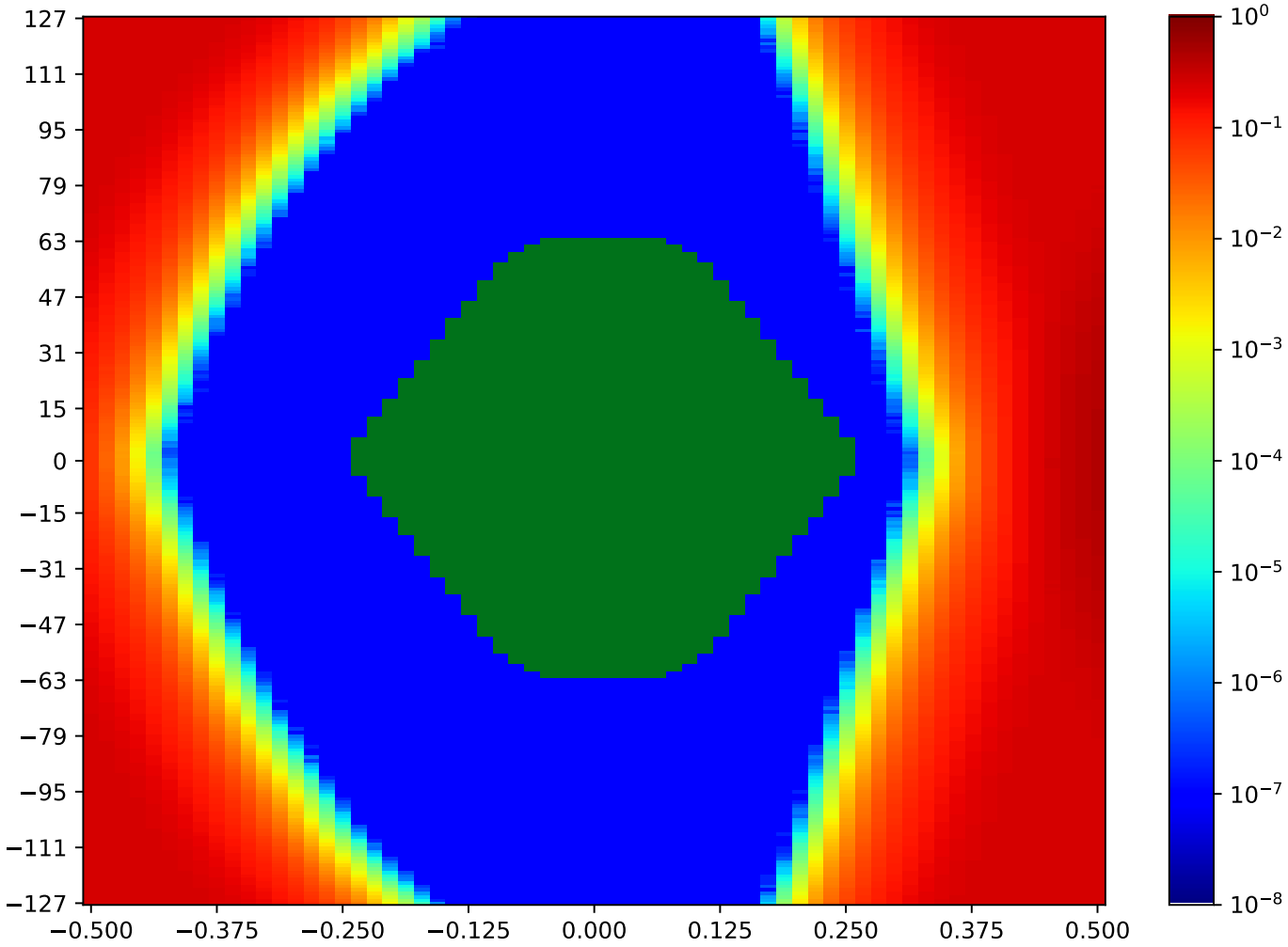


Figure 6.113: MSP_C_FPGA-IC39-14–IC15-14-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.16 MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Table 6.105: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:57:51		2019-Nov-26 17:58:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9136	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

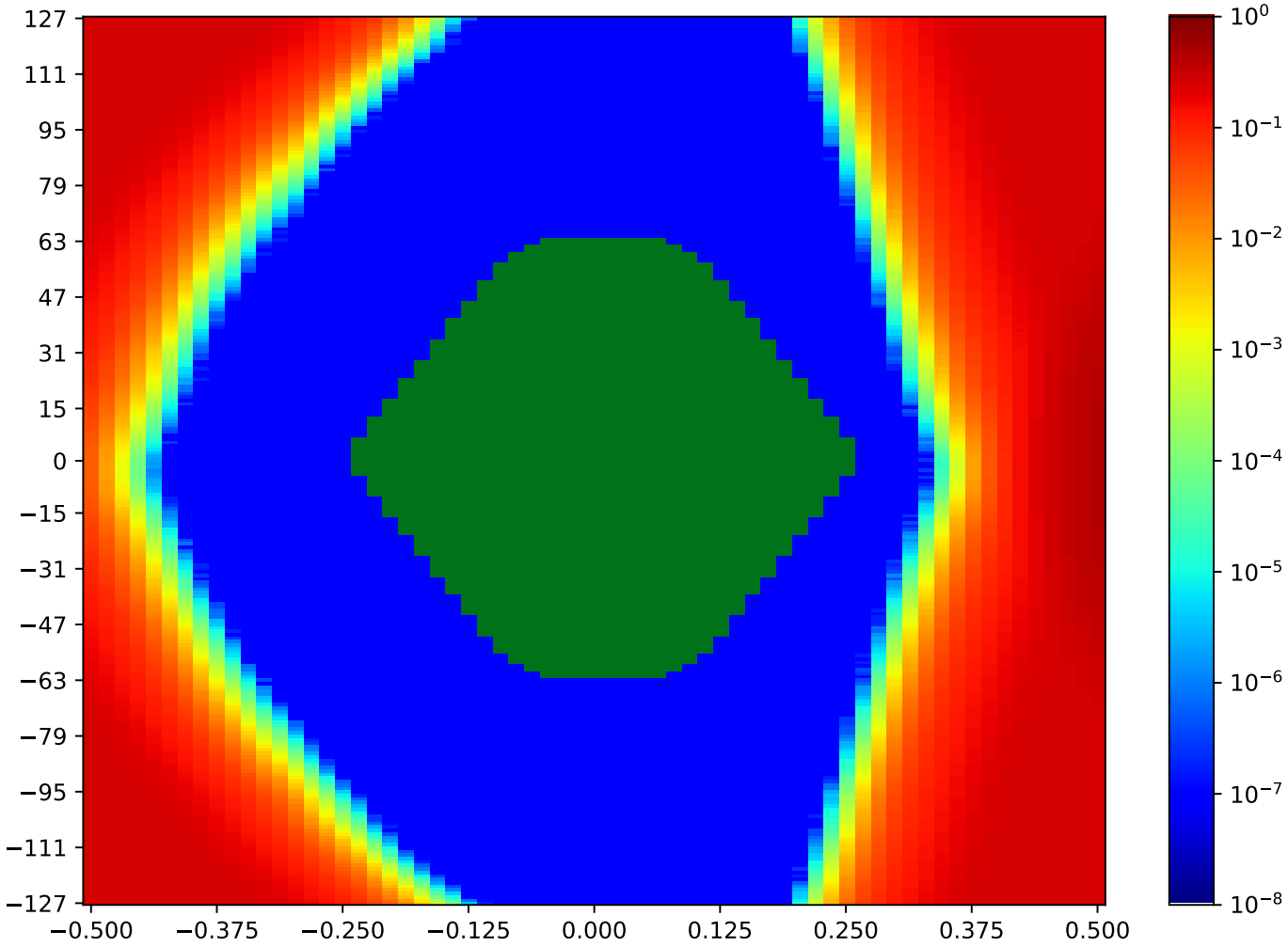


Figure 6.114: MSP_C_FPGA-IC39-15–IC15-15-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.17 MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Table 6.106: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:58:10		2019-Nov-26 17:58:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8772	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

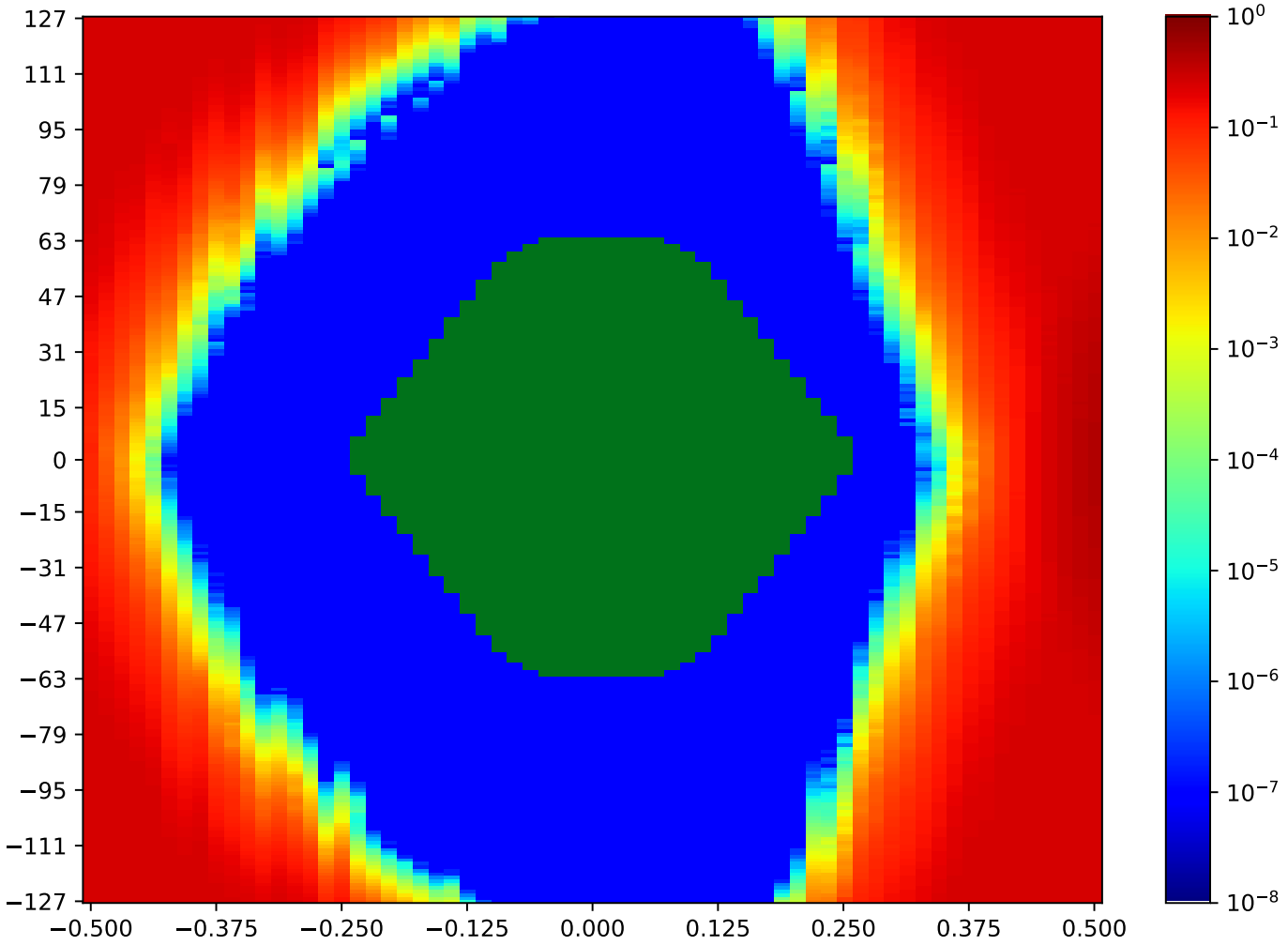


Figure 6.115: MSP_C_FPGA-IC39-16–IC15-16-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.18 MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Table 6.107: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:58:30		2019-Nov-26 17:58:49	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8769	48	73.85%	253	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

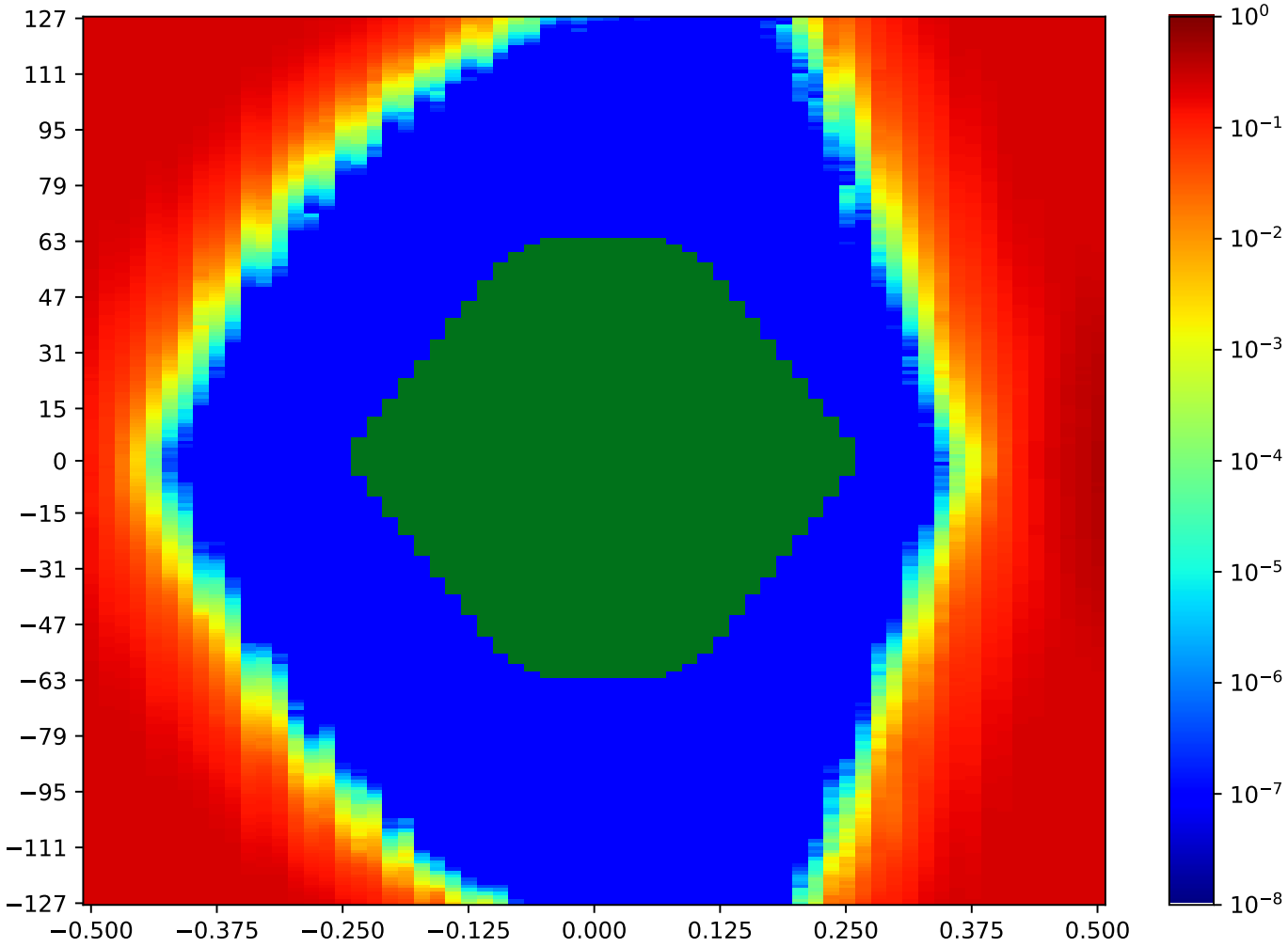


Figure 6.116: MSP_C_FPGA-IC39-17–IC15-17-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.19 MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Table 6.108: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:58:49		2019-Nov-26 17:59:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9143	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

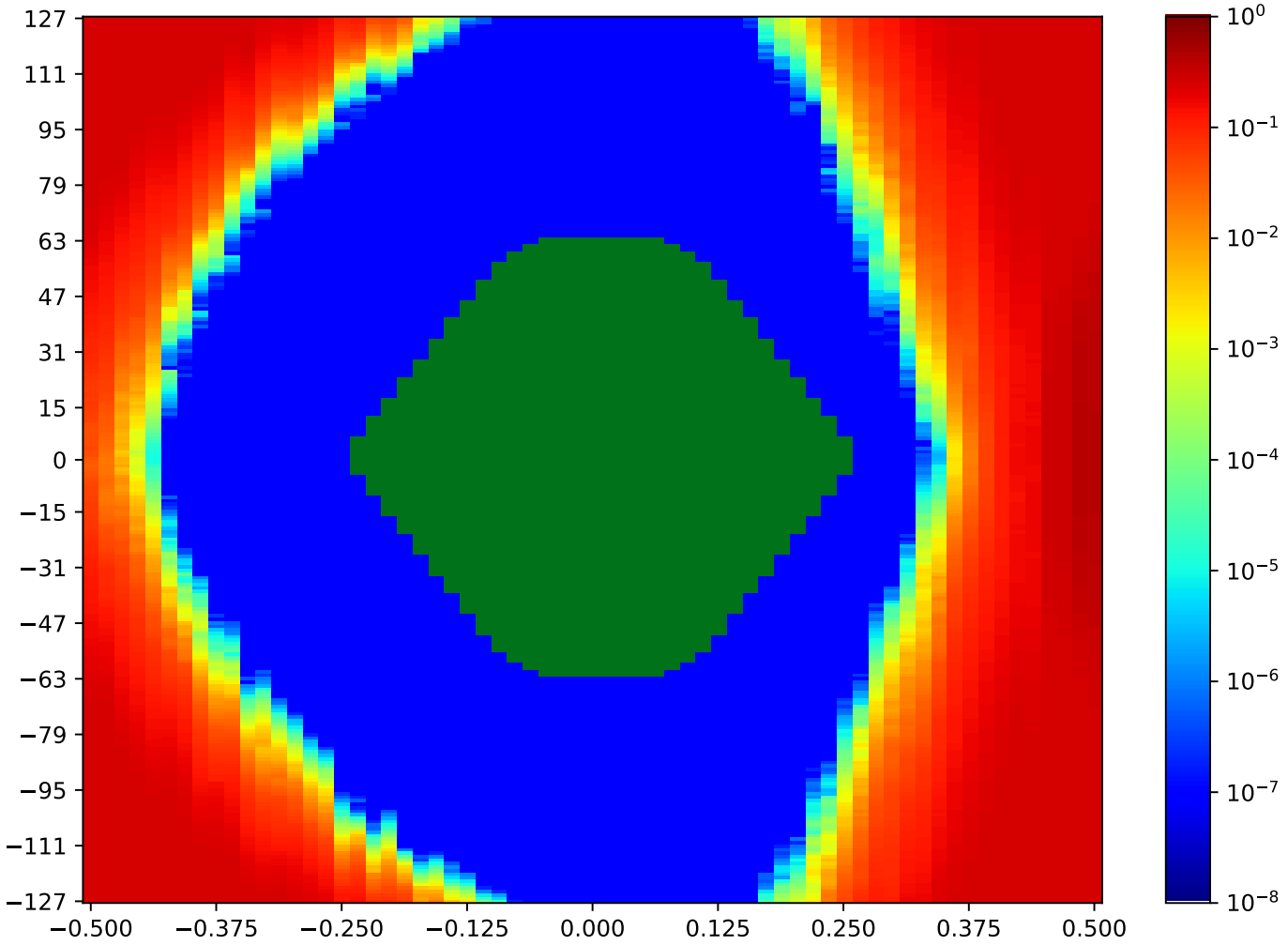


Figure 6.117: MSP_C_FPGA-IC39-18–IC15-18-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.20 MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Table 6.109: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:59:08		2019-Nov-26 17:59:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9240	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

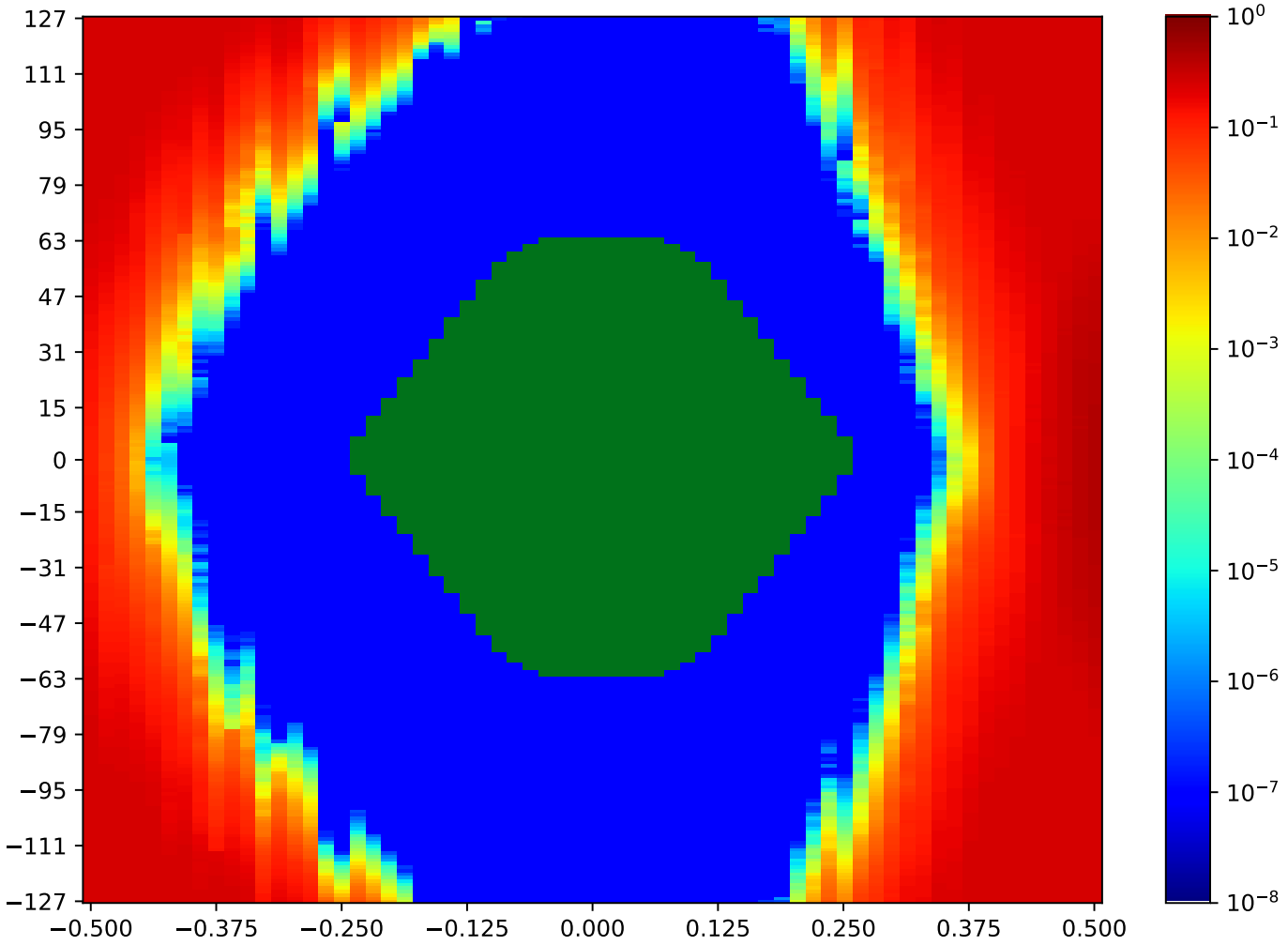


Figure 6.118: MSP_C_FPGA-IC39-19–IC15-19-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.21 MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Table 6.110: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:59:33		2019-Nov-26 17:59:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8980	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

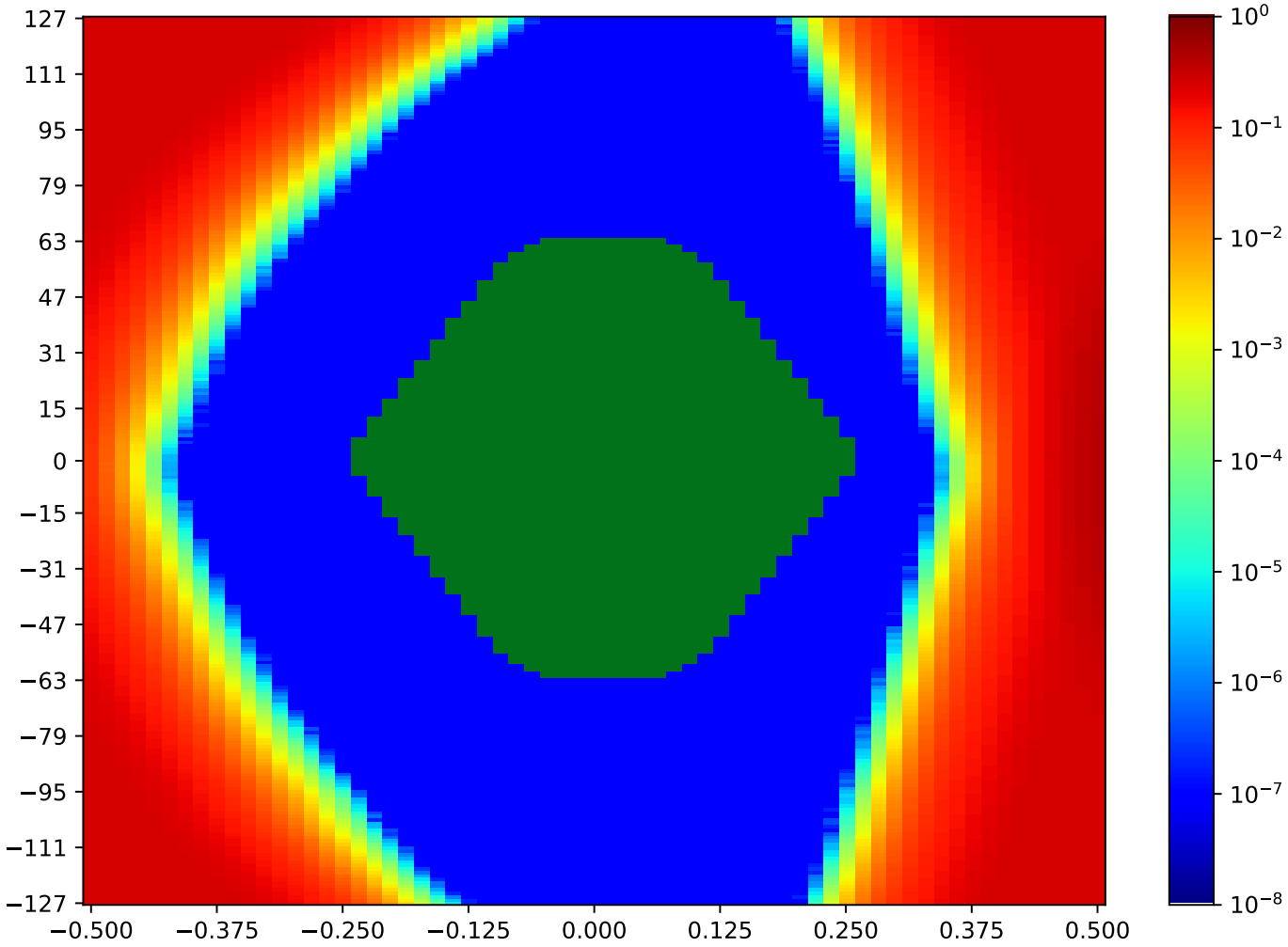


Figure 6.119: MSP_C_FPGA-IC39-20–IC15-20-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.22 MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Table 6.111: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 17:59:52		2019-Nov-26 18:00:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9363	48	73.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

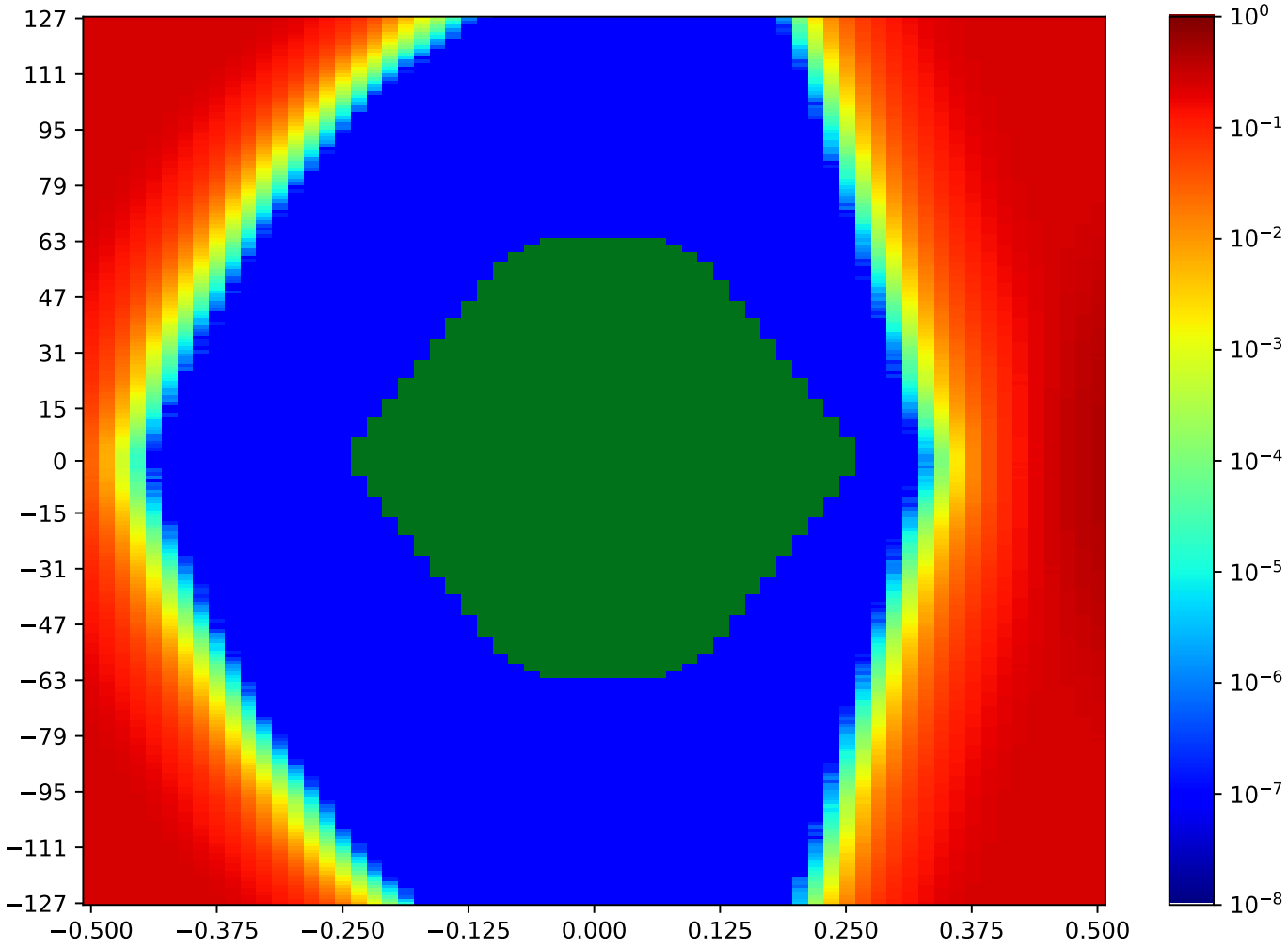


Figure 6.120: MSP_C_FPGA-IC39-21–IC15-21-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.23 MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Table 6.112: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 18:00:17		2019-Nov-26 18:00:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9246	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

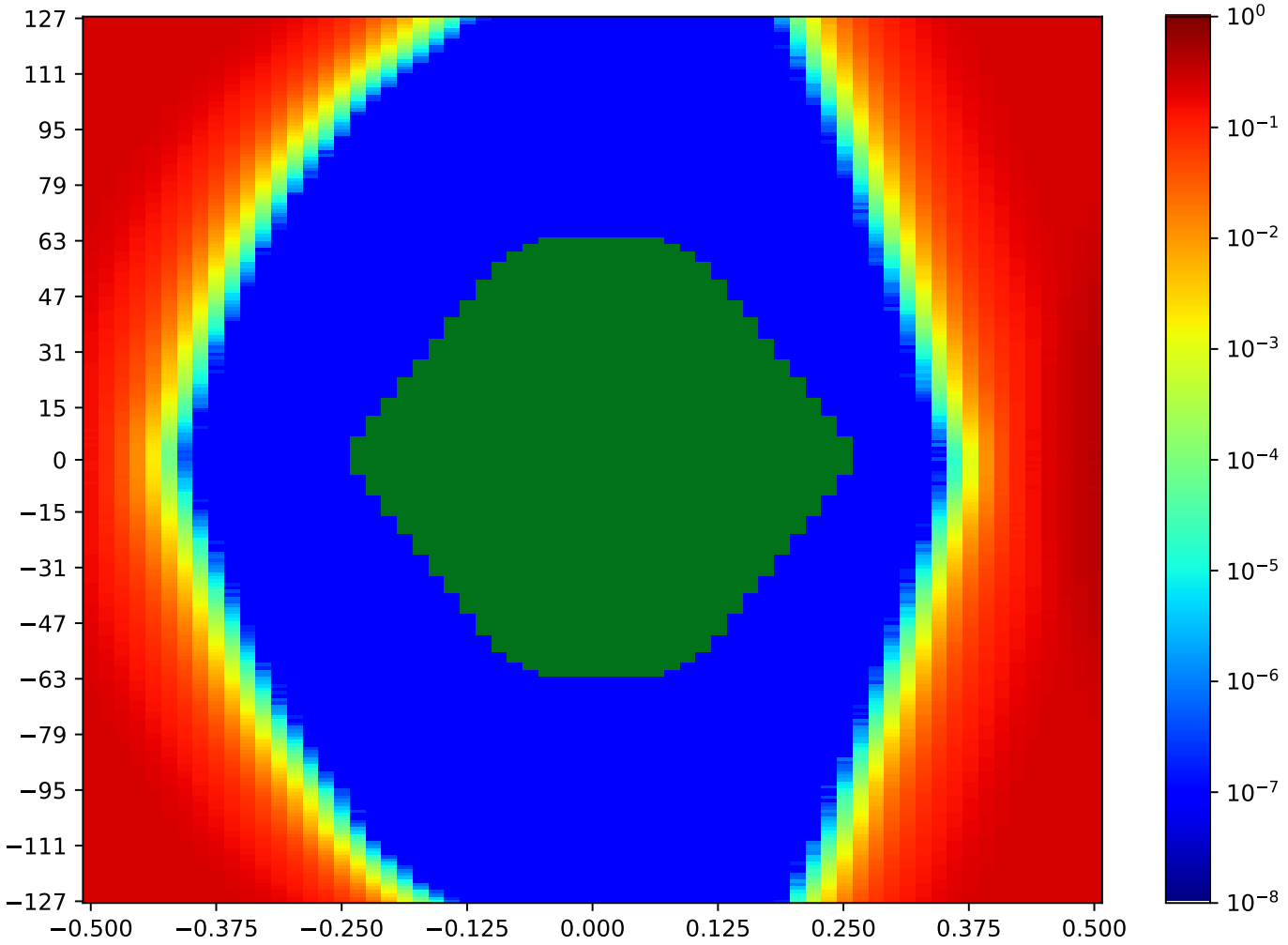


Figure 6.121: MSP_C_FPGA-IC39-22–IC15-22-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.24 MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Table 6.113: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 18:00:36		2019-Nov-26 18:00:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9163	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

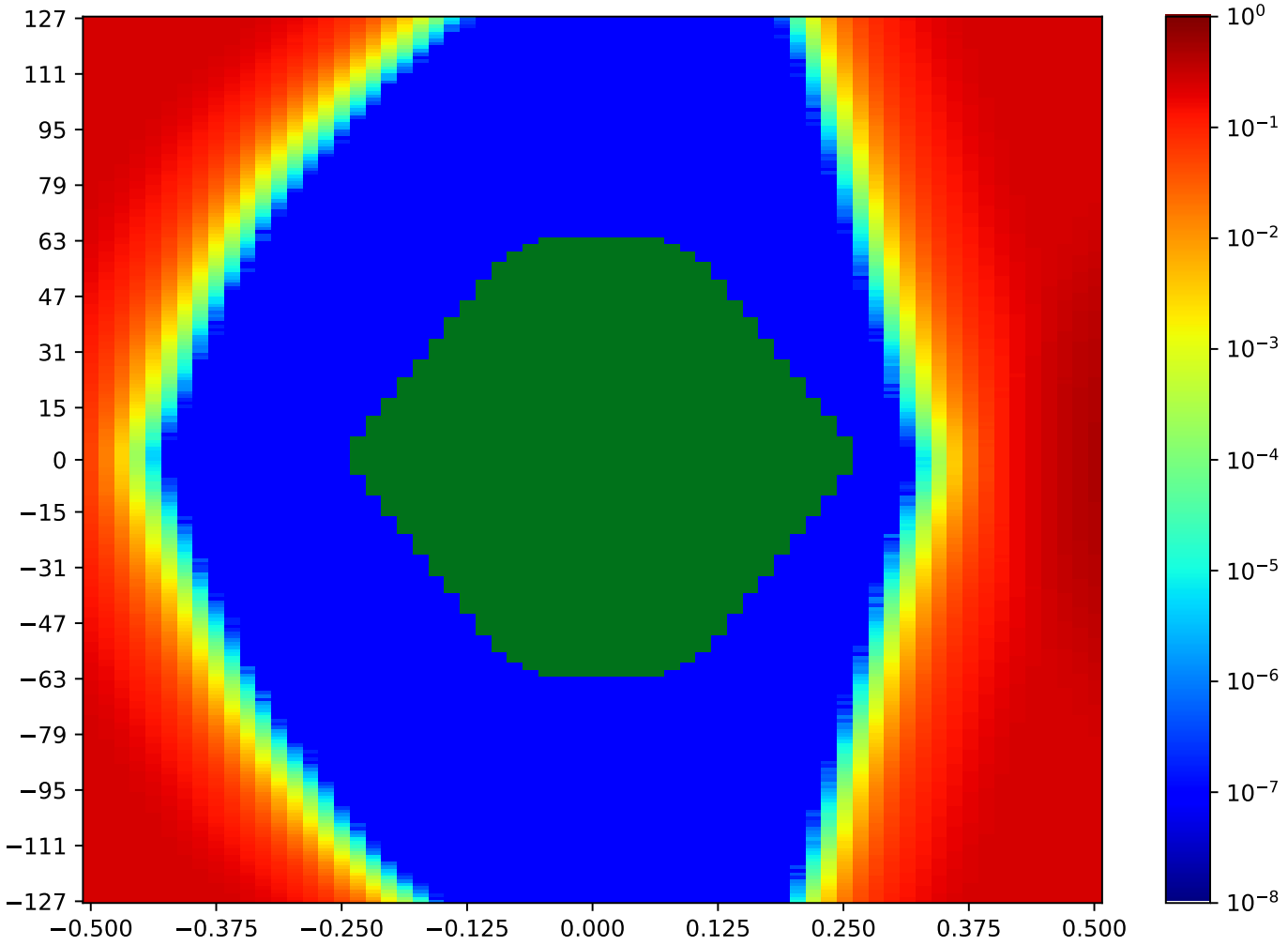


Figure 6.122: MSP_C_FPGA-IC39-23–IC15-23-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.25 MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Table 6.114: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 18:00:56		2019-Nov-26 18:01:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9302	50	76.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

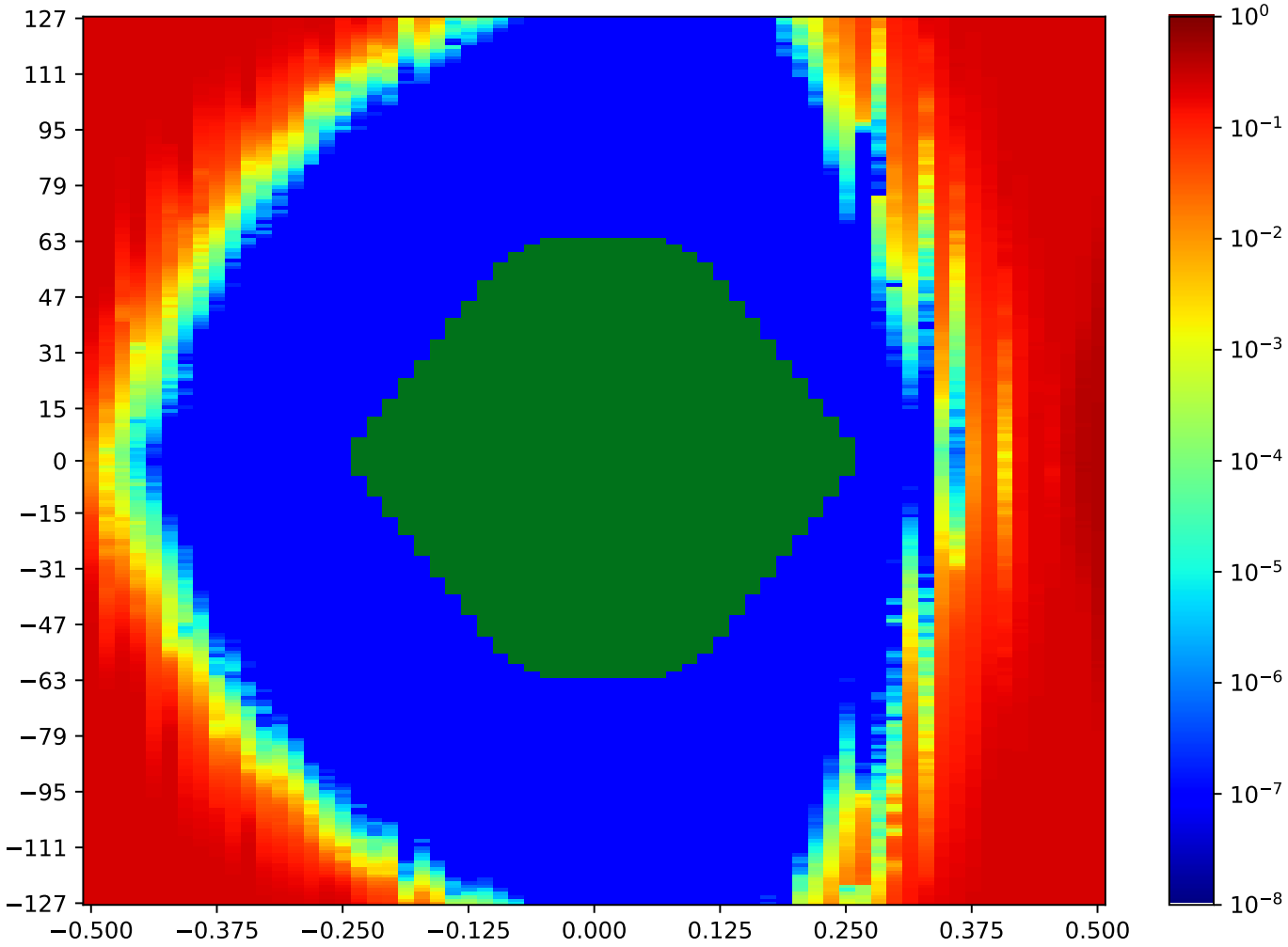


Figure 6.123: MSP_C_FPGA-IC39-24–IC15-24-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.26 MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Table 6.115: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 18:01:15		2019-Nov-26 18:01:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9210	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

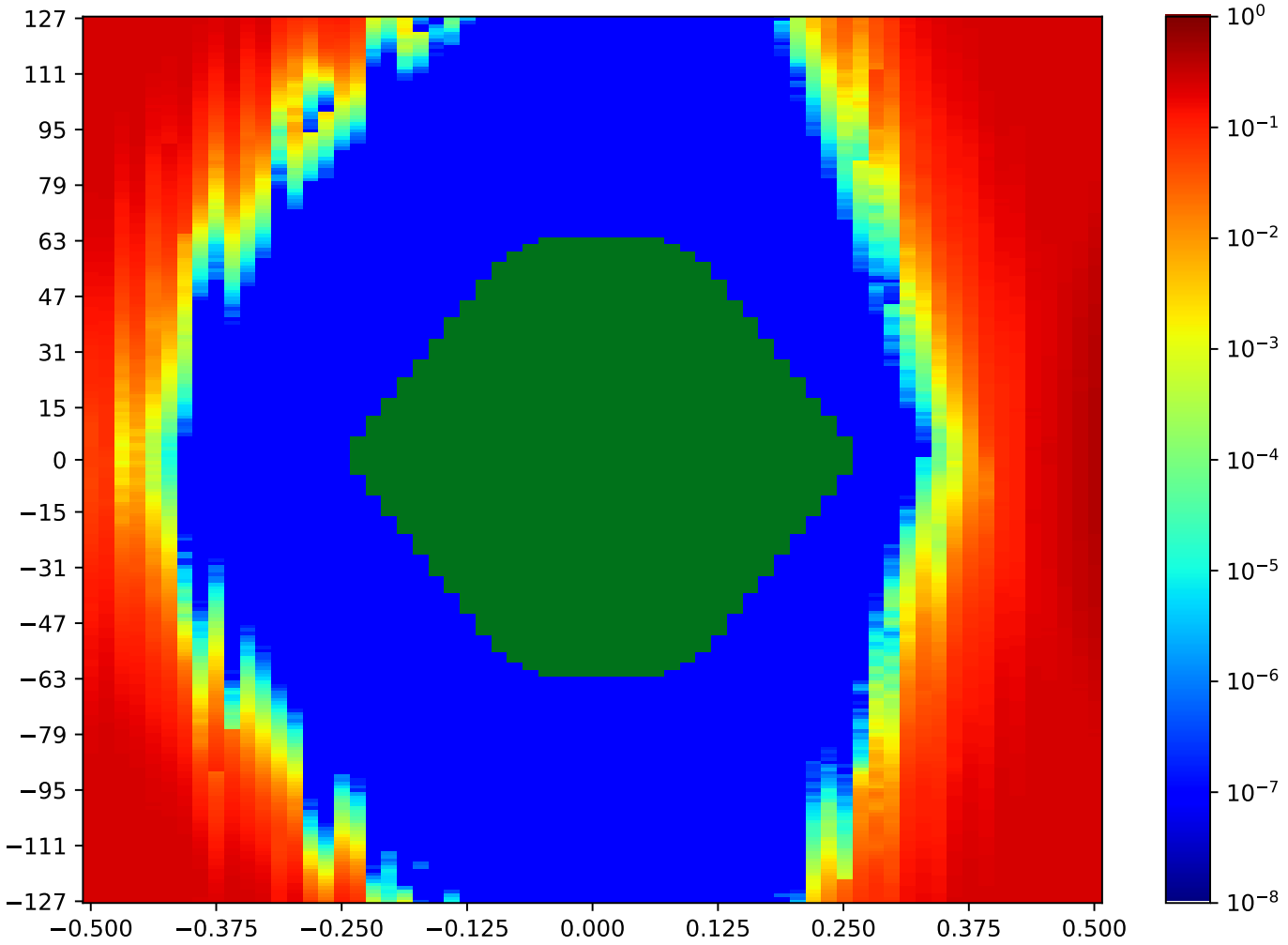


Figure 6.124: MSP_C_FPGA-IC39-25–IC15-25-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.27 MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Table 6.116: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 18:01:34		2019-Nov-26 18:01:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9353	47	72.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

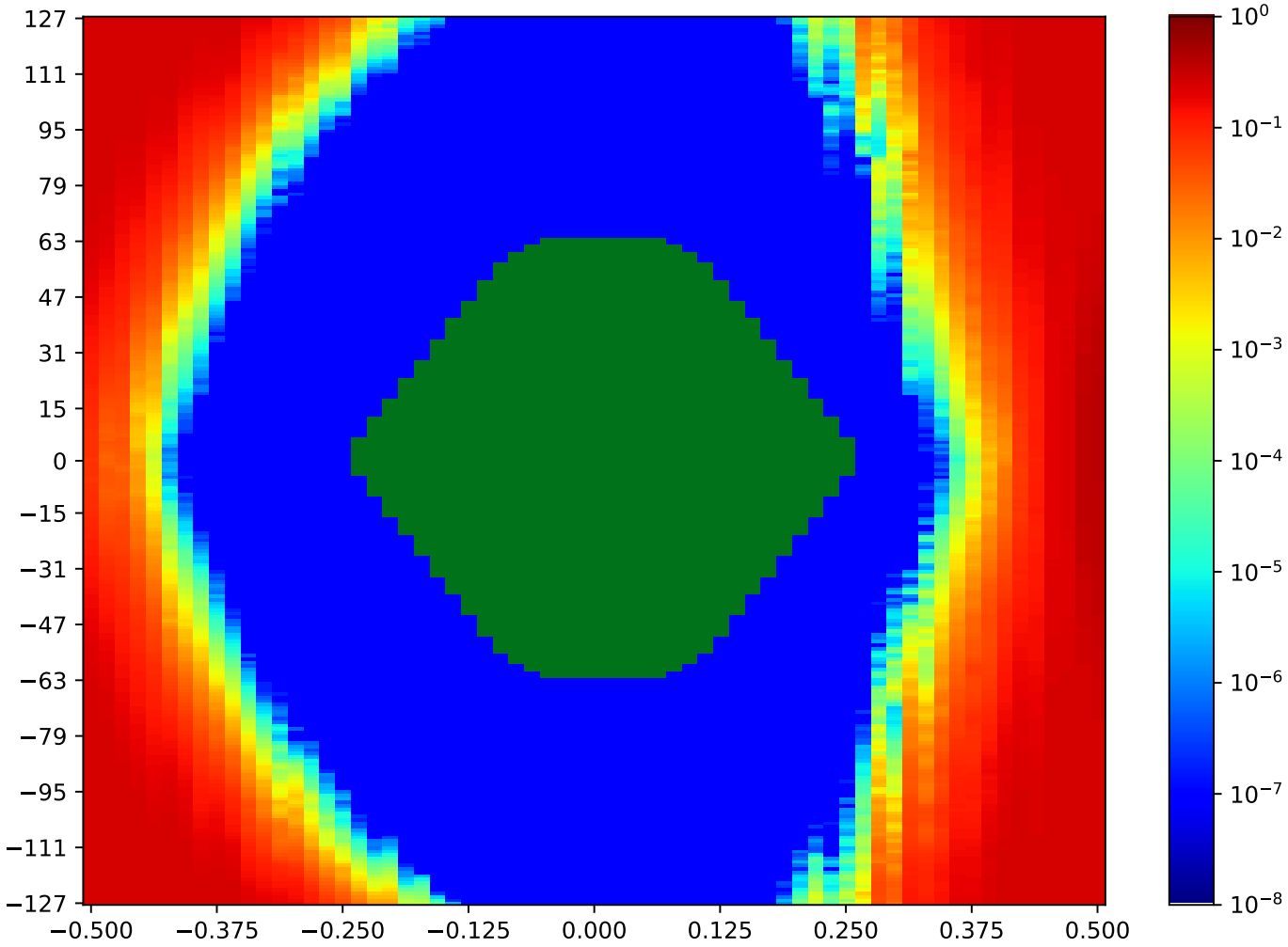


Figure 6.125: MSP_C_FPGA-IC39-26–IC15-26-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.9.28 MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Table 6.117: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale GTY	2019-Nov-26 18:01:53		2019-Nov-26 18:02:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8891	46	70.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

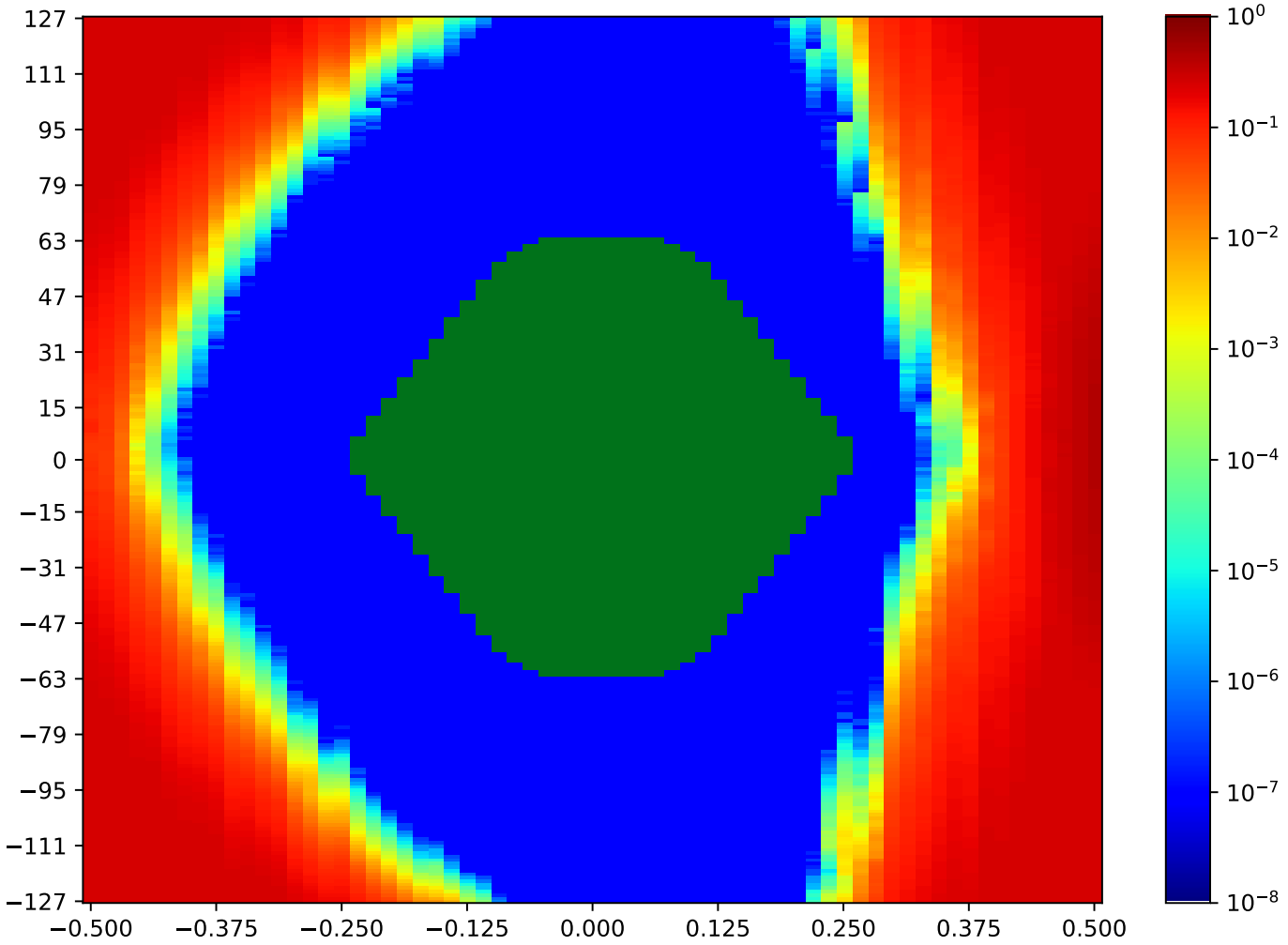


Figure 6.126: MSP_C_FPGA-IC39-27–IC15-27-TRP_FPGA

Call back to summary Figure 6.98. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10 MSP_A TX1 MSP_C RX17 Minipod Loopback

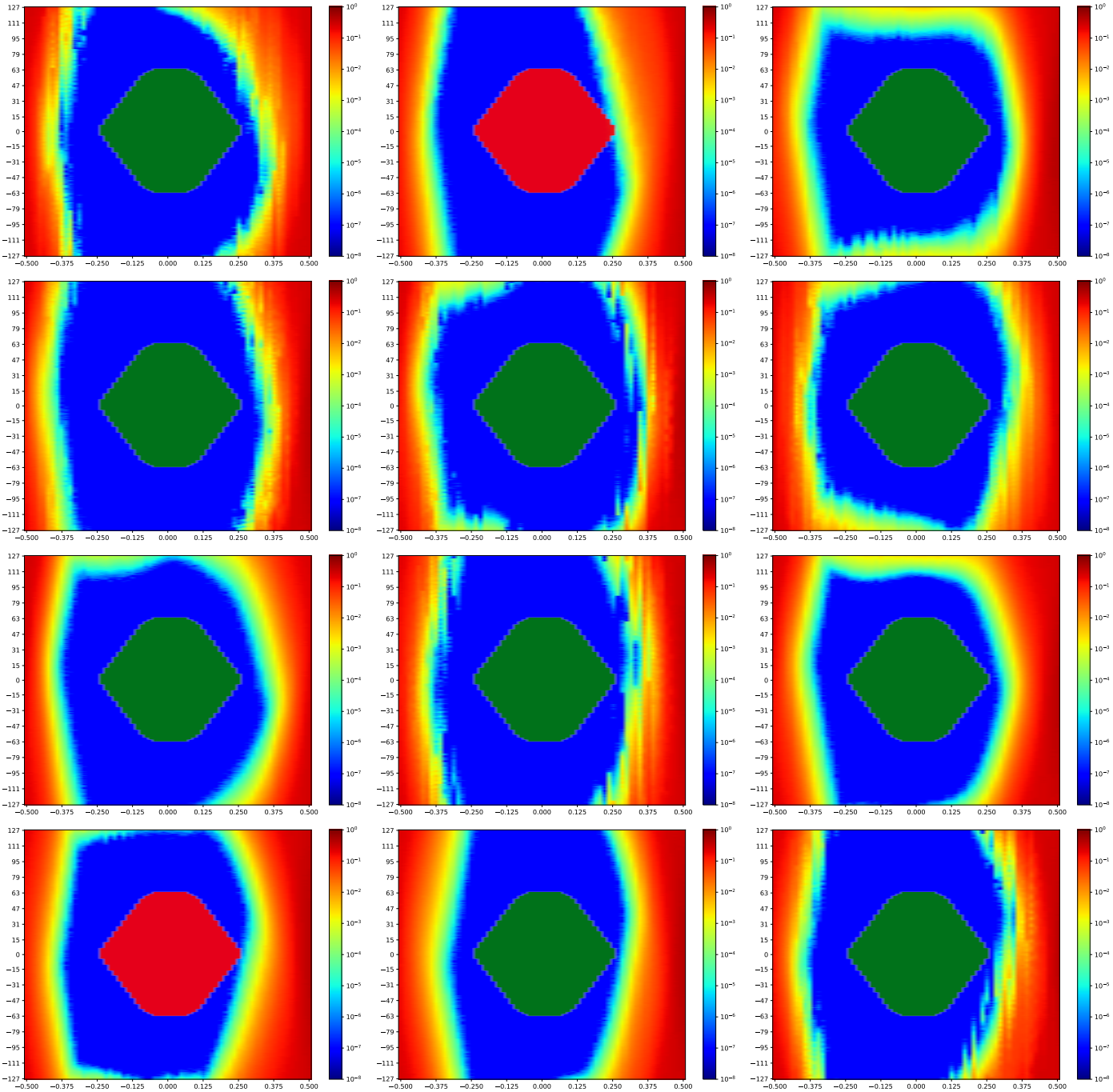


Figure 6.127: MSP_A TX1 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.140.

6.10.1 MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Table 6.118: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:28:48		2019-Nov-27 10:29:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8834	39	60.00%	245	96.08%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

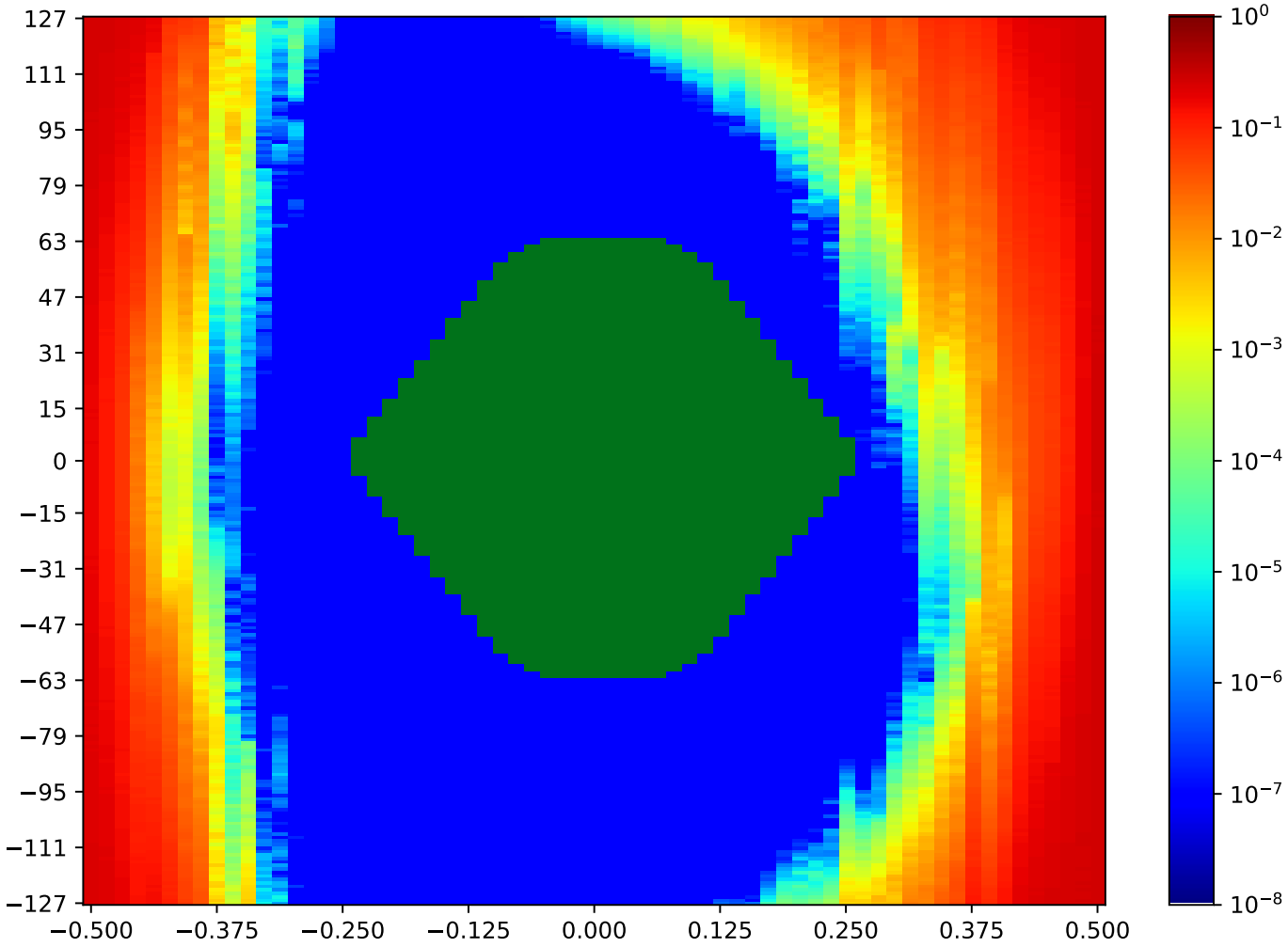


Figure 6.128: MSP_A_FPGA-TX1-00–RX17-00-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.2 MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Table 6.119: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:29:44		2019-Nov-27 10:30:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8646	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

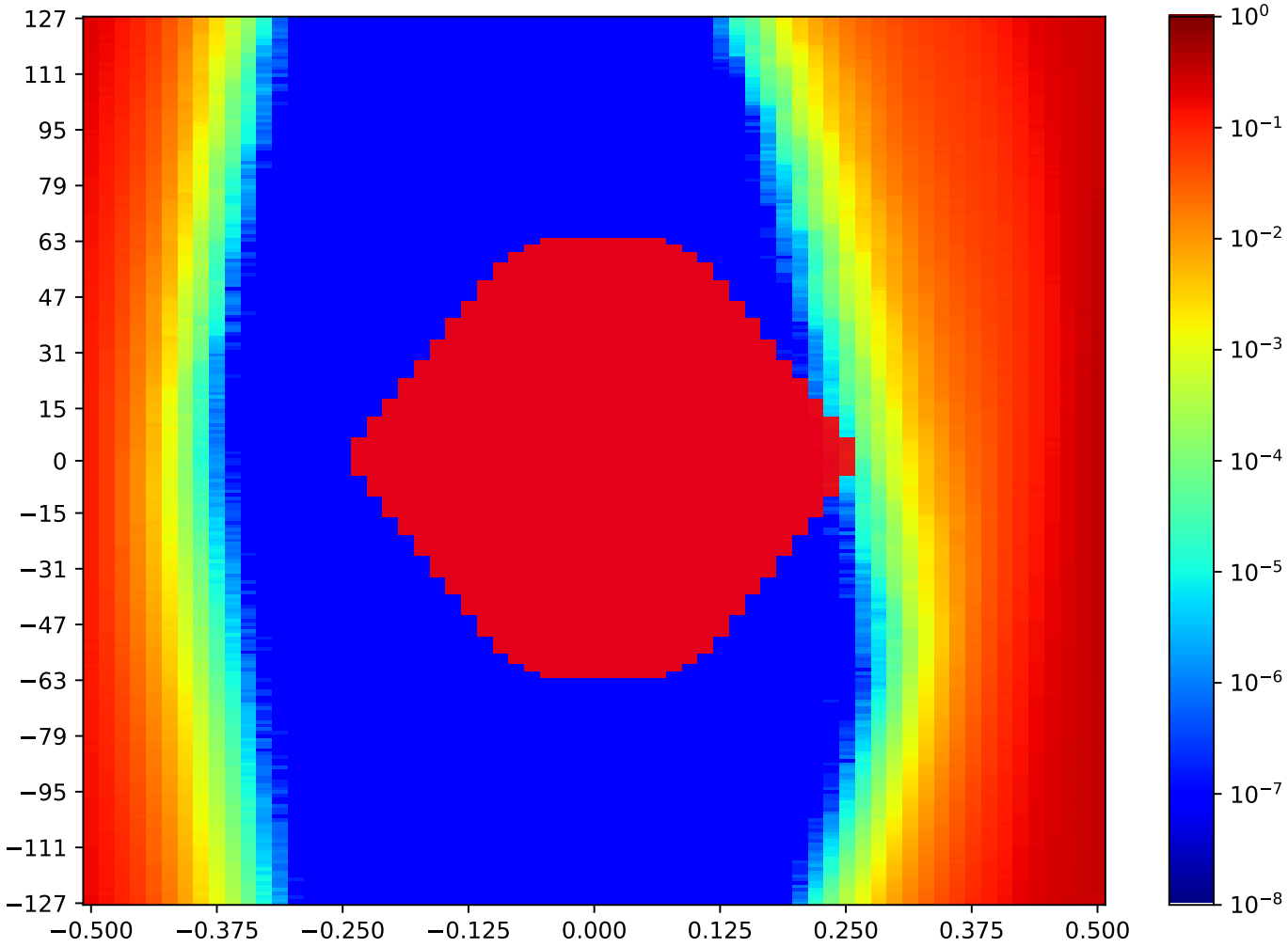


Figure 6.129: MSP_A_FPGA-TX1-01–RX17-01-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.3 MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Table 6.120: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:30:12		2019-Nov-27 10:30:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7018	41	63.08%	190	73.73%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

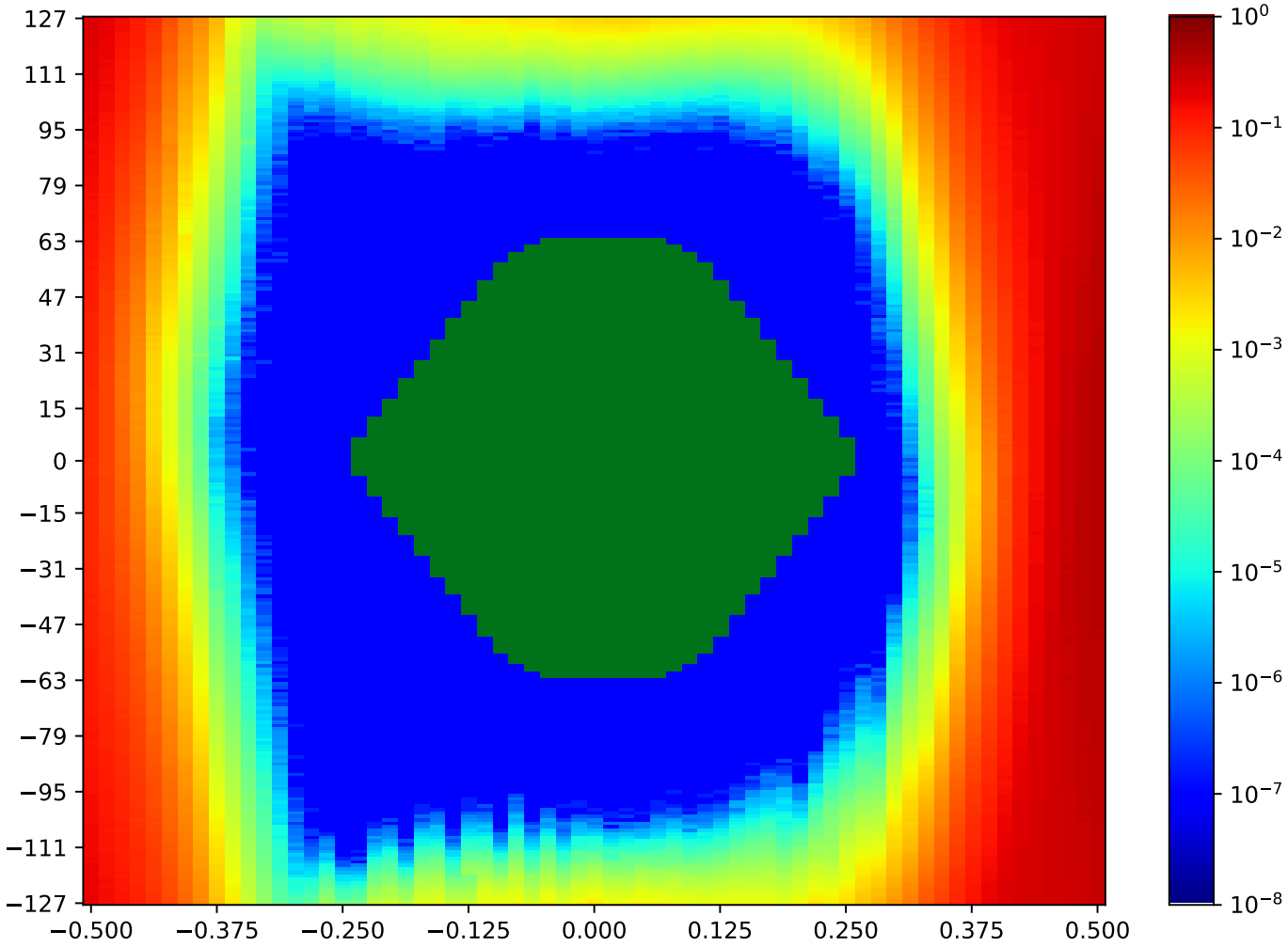


Figure 6.130: MSP_A_FPGA-TX1-02–RX17-02-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.4 MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Table 6.121: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:27:52		2019-Nov-27 10:28:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9857	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

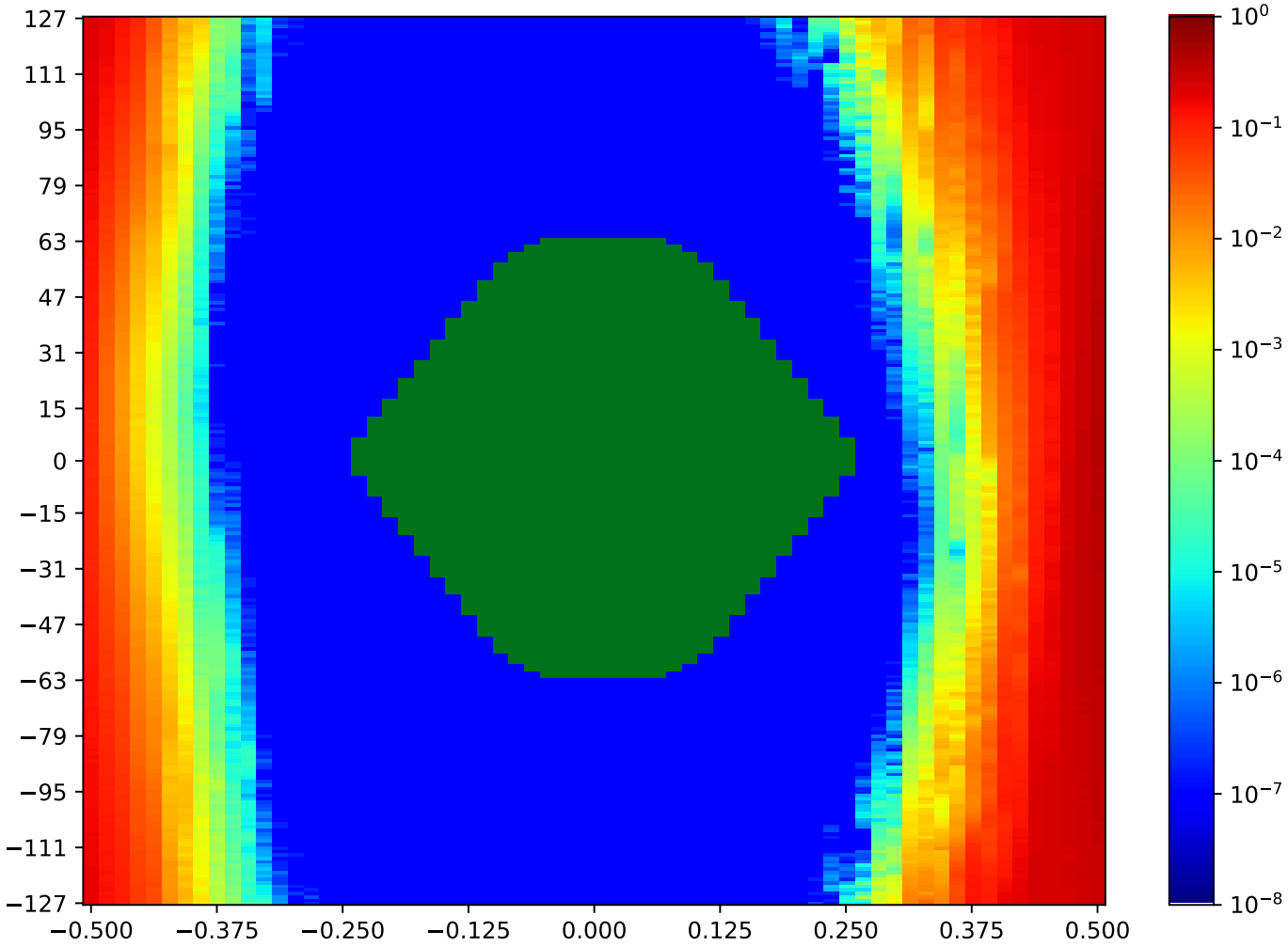


Figure 6.131: MSP_A_FPGA-TX1-03–RX17-03-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.5 MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Table 6.122: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:53:50		2019-Nov-27 10:54:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9158	44	64.62%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

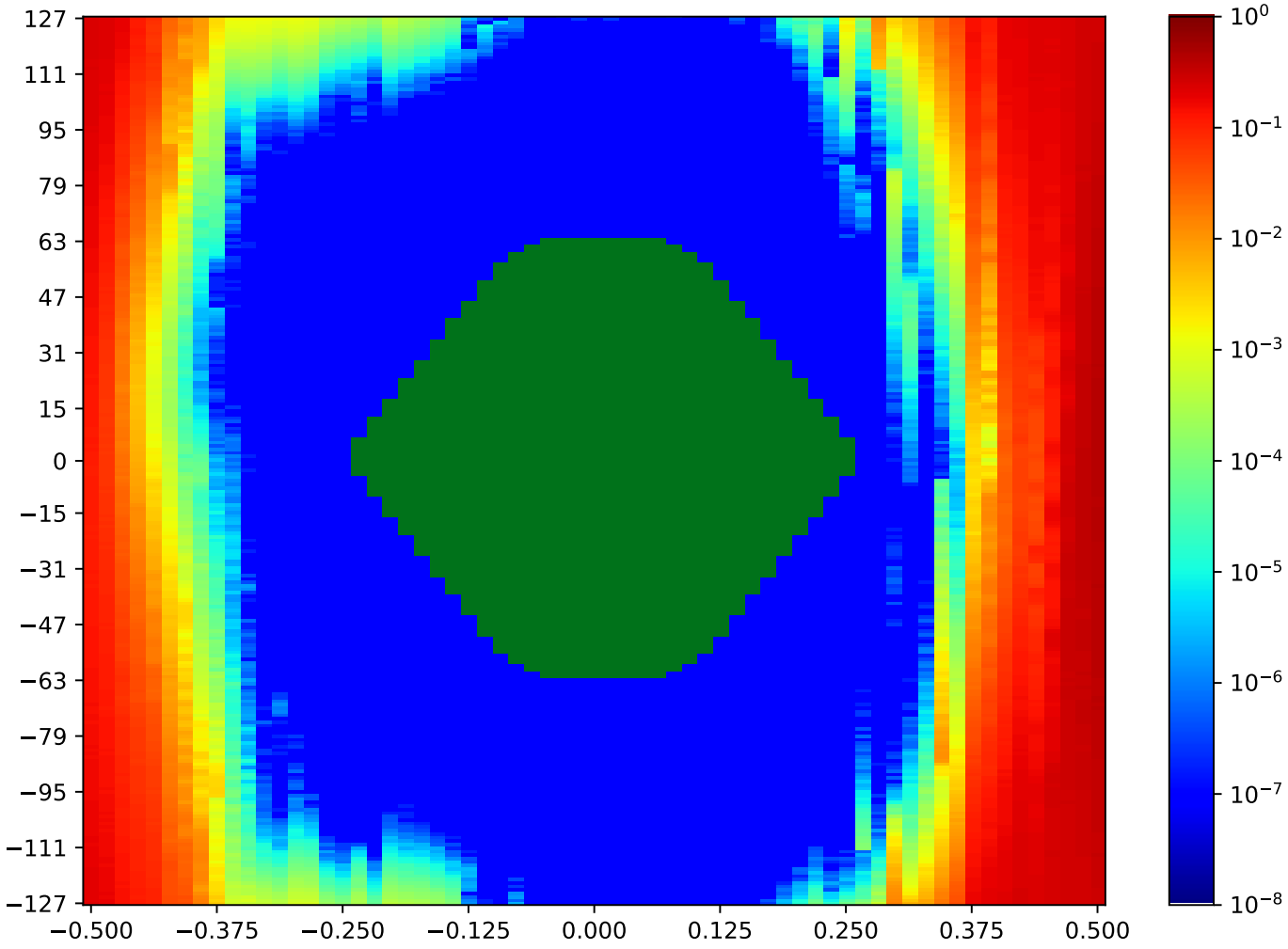


Figure 6.132: MSP_A_FPGA-TX1-04–RX17-04-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.6 MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Table 6.123: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:27:24		2019-Nov-27 10:27:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8052	40	61.54%	230	89.41%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

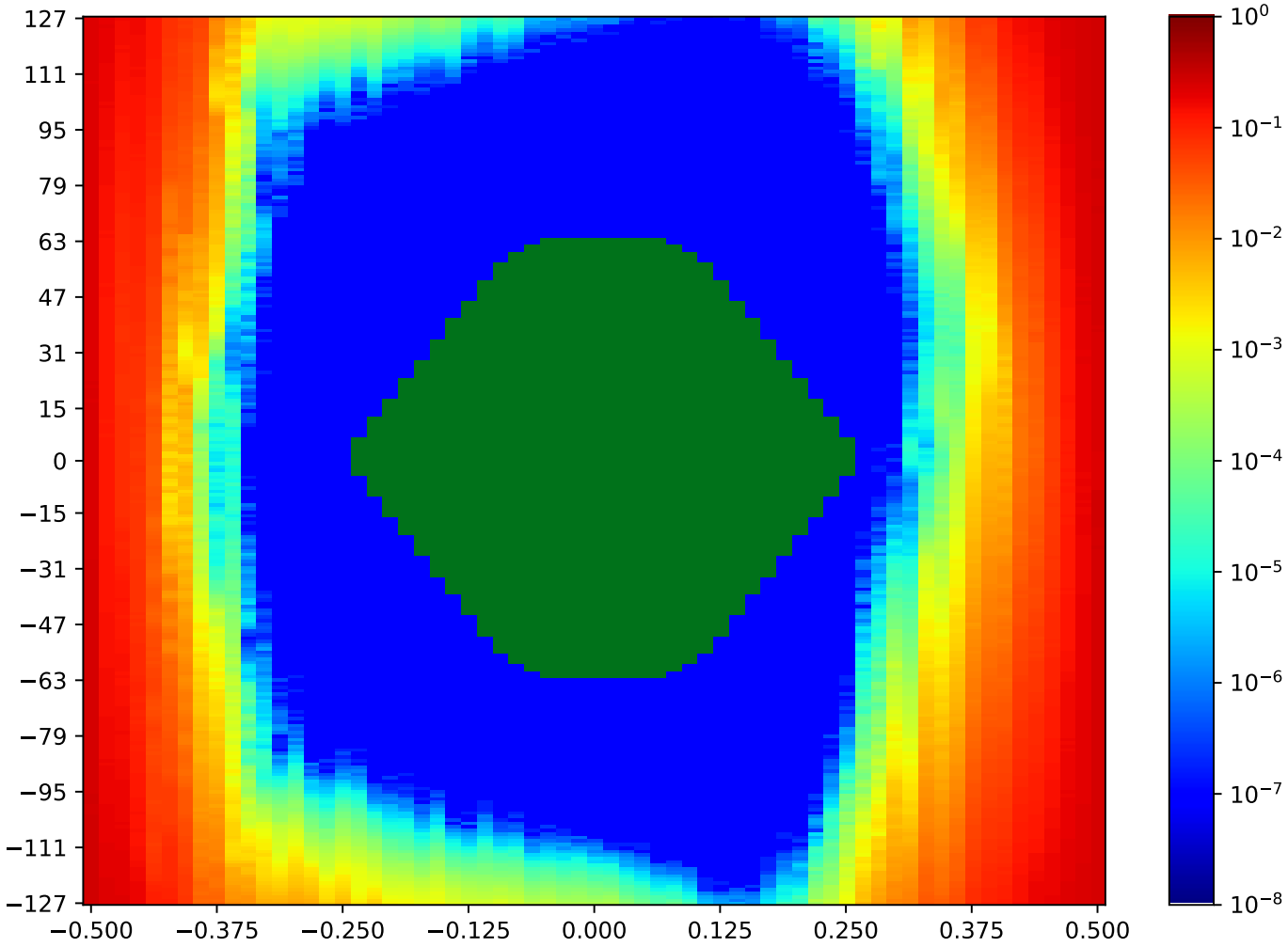


Figure 6.133: MSP_A_FPGA-TX1-05–RX17-05-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.7 MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Table 6.124: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:32:27		2019-Nov-27 10:32:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8503	43	66.15%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

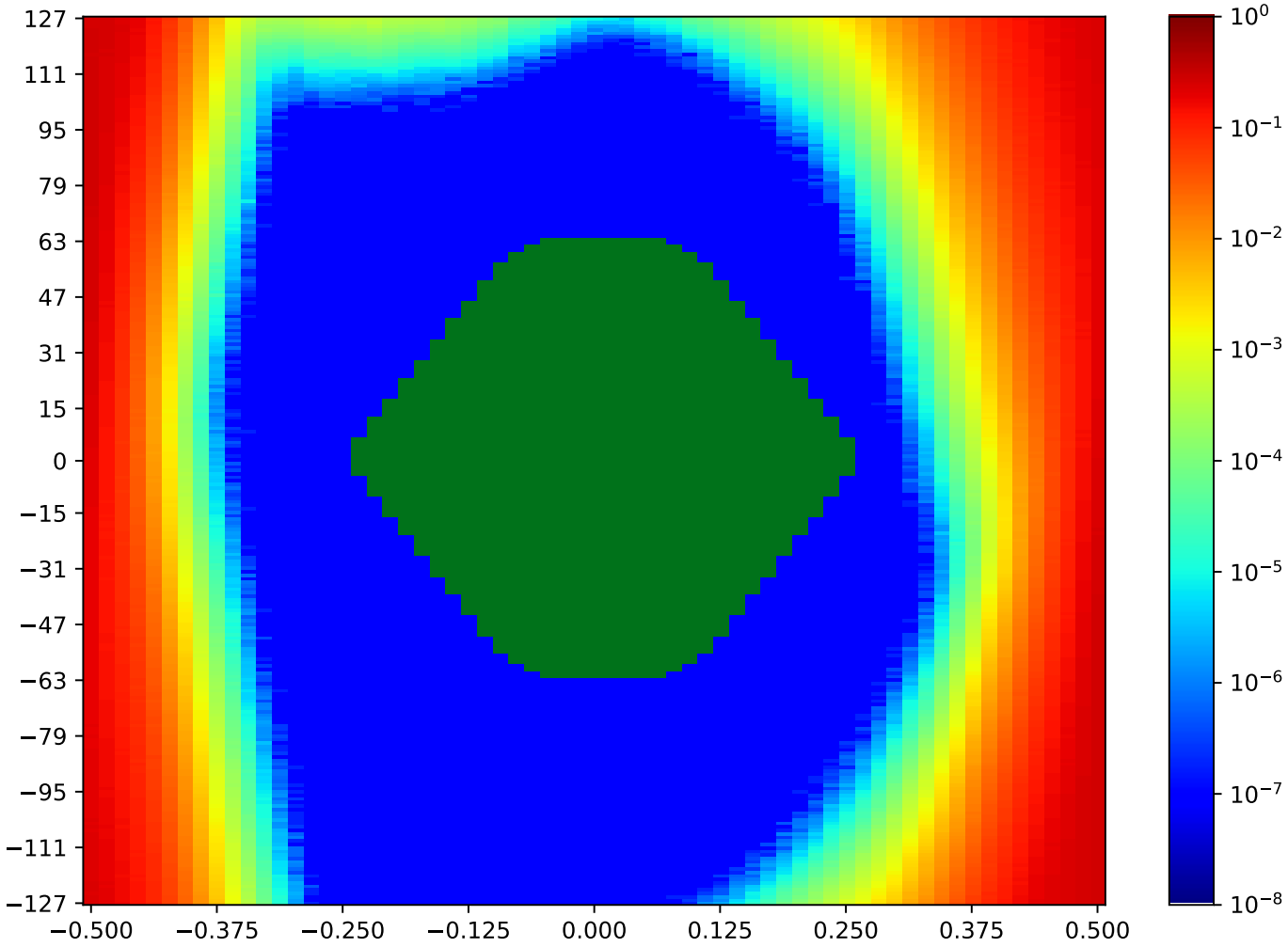


Figure 6.134: MSP_A_FPGA-TX1-06–RX17-06-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.8 MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Table 6.125: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:28:21		2019-Nov-27 10:28:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9132	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

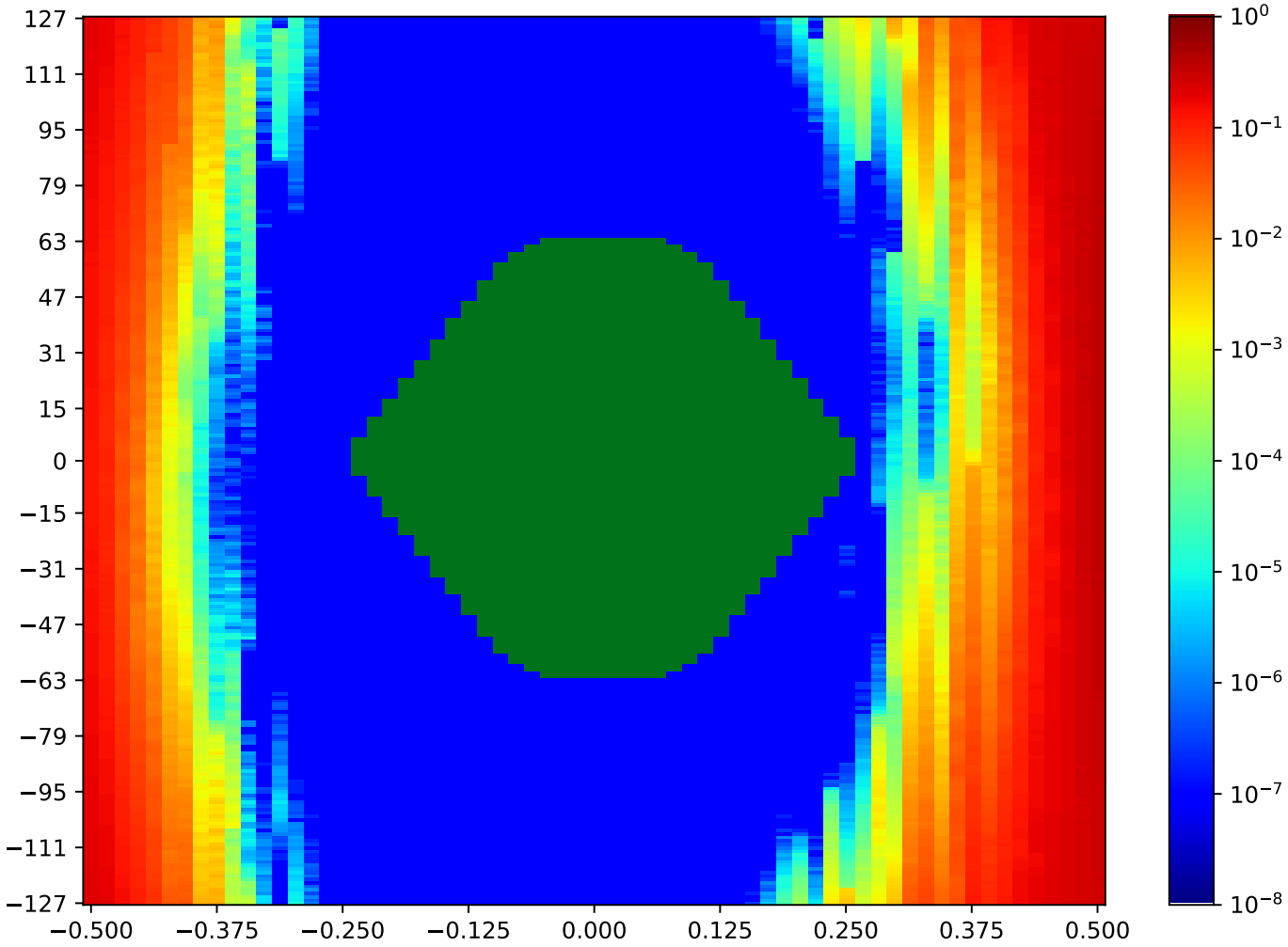


Figure 6.135: MSP_A_FPGA-TX1-07–RX17-07-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.9 MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Table 6.126: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:32:00		2019-Nov-27 10:32:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7554	38	56.92%	230	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

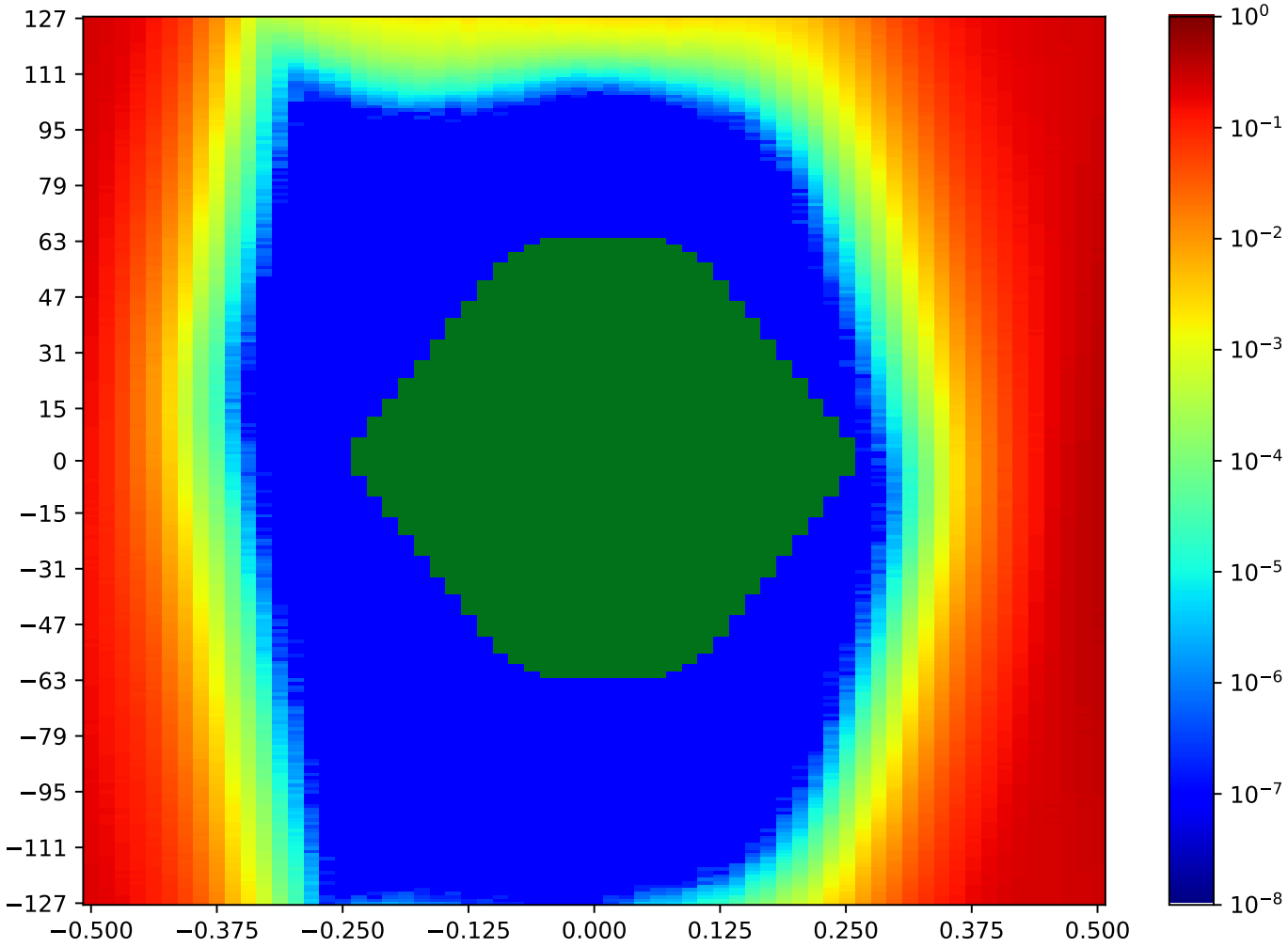


Figure 6.136: MSP_A_FPGA-TX1-08–RX17-08-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.10 MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Table 6.127: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:29:16		2019-Nov-27 10:29:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8074	38	58.46%	237	91.76%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

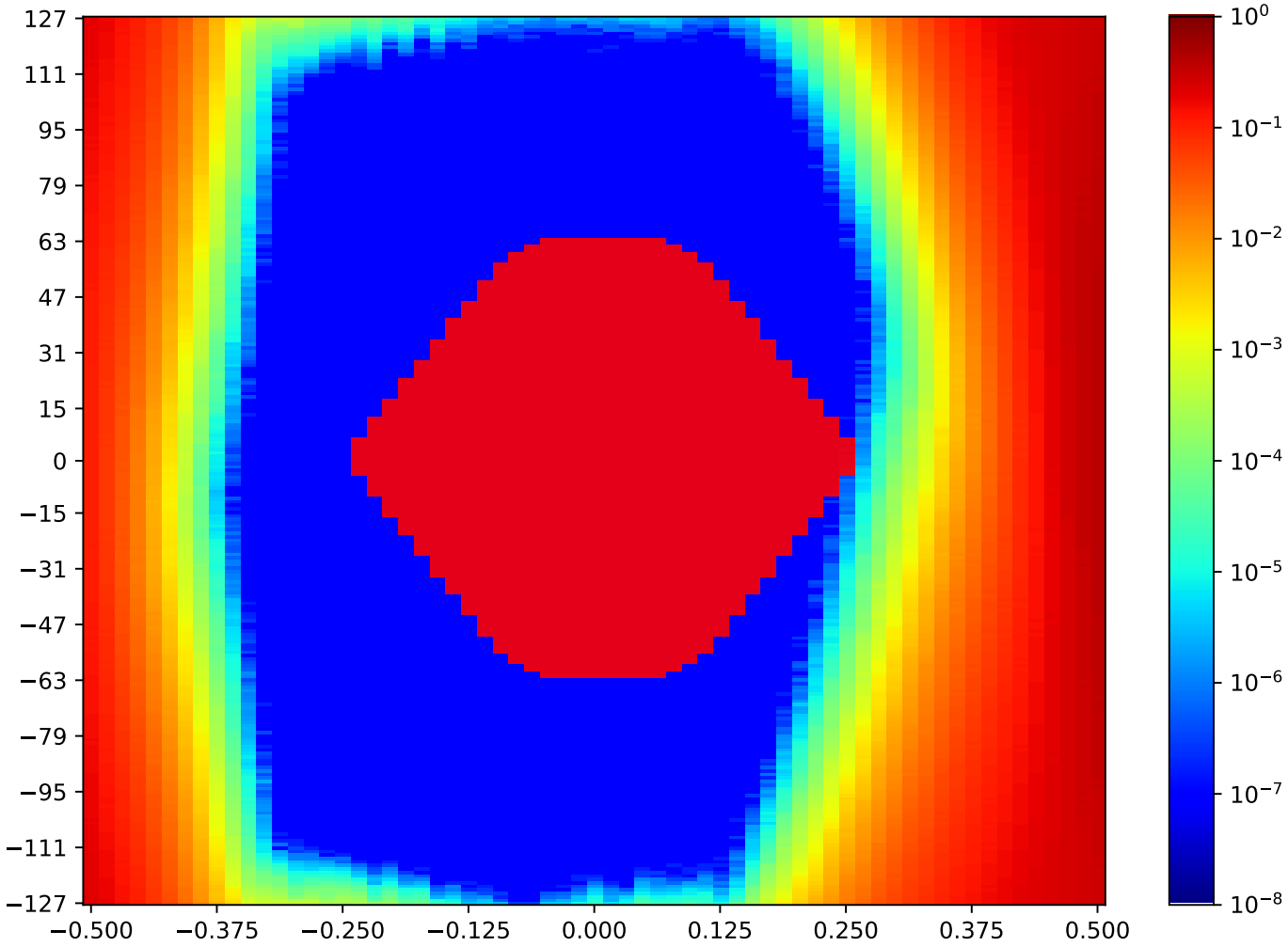


Figure 6.137: MSP_A_FPGA-TX1-09–RX17-09-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.11 MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Table 6.128: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:31:05		2019-Nov-27 10:31:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8066	35	53.85%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

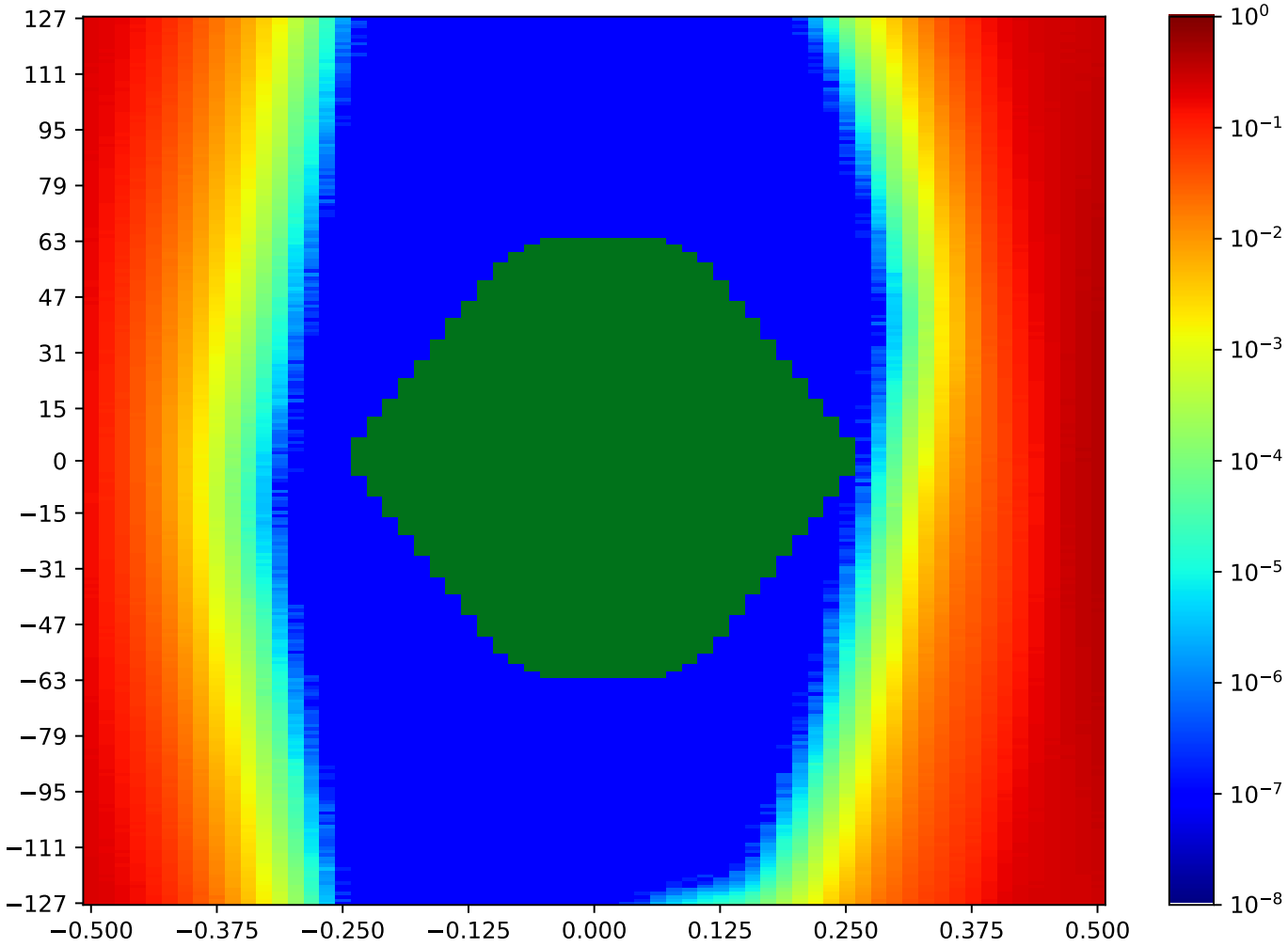


Figure 6.138: MSP_A_FPGA-TX1-10–RX17-10-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.10.12 MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Table 6.129: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:30:41		2019-Nov-27 10:31:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9219	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

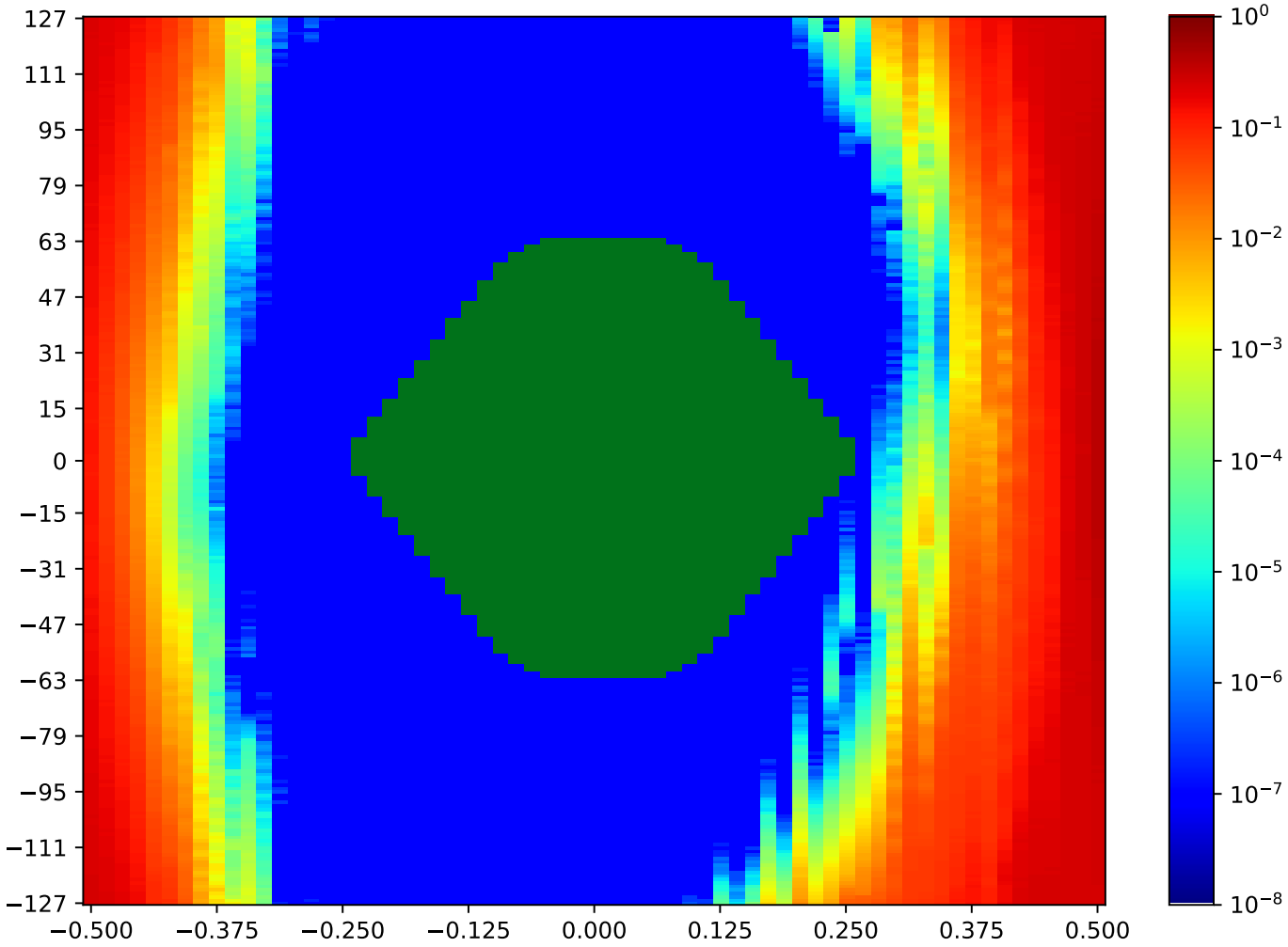


Figure 6.139: MSP_A_FPGA-TX1-11–RX17-11-MSP_C_FPGA

Call back to summary Figure 6.127. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11 MSP_A TX2 MSP_C RX18 Minipod Loopback

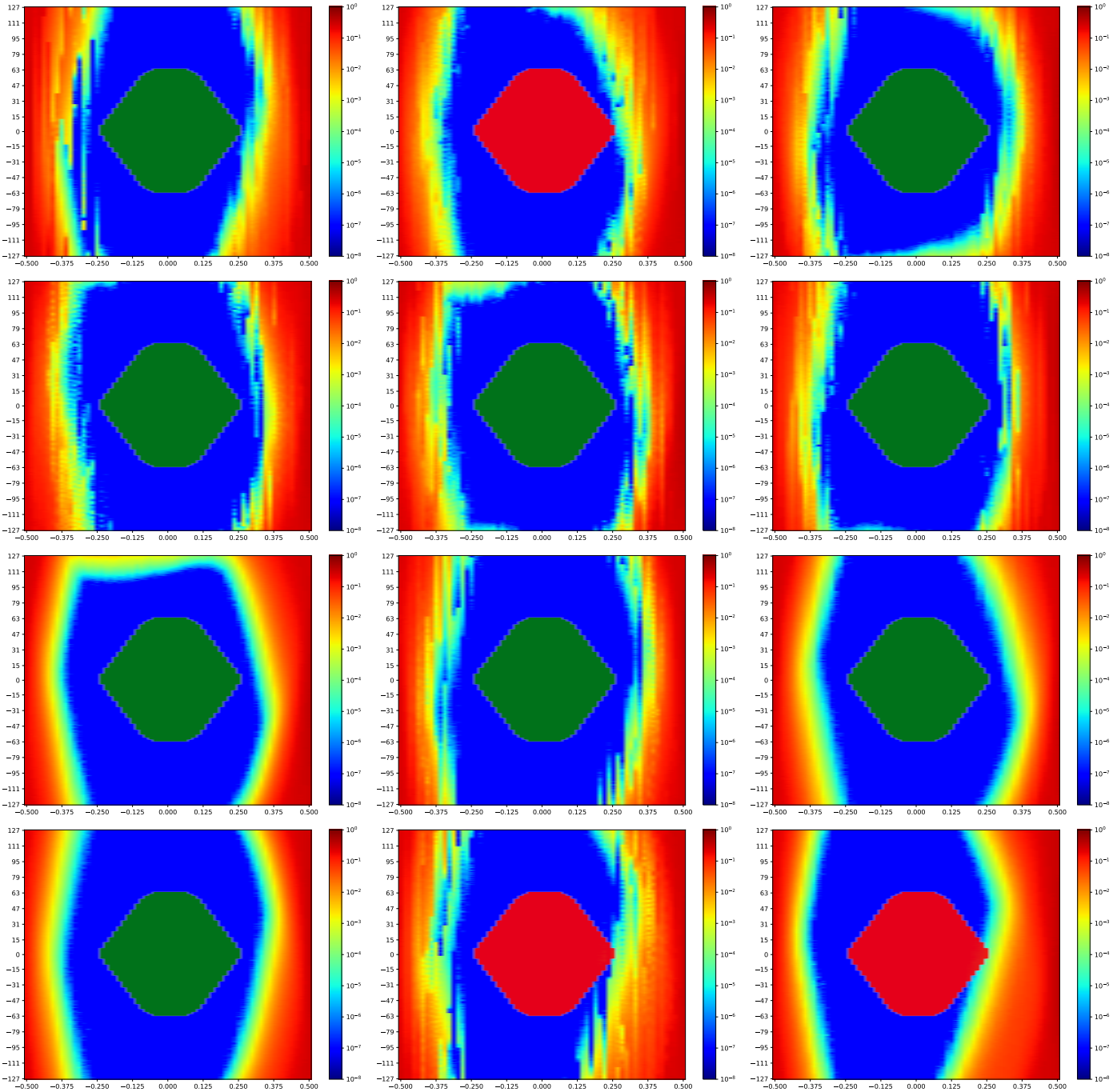


Figure 6.140: MSP_A TX2 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.153.

6.11.1 MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Table 6.130: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:34:10		2019-Nov-27 10:34:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8239	38	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

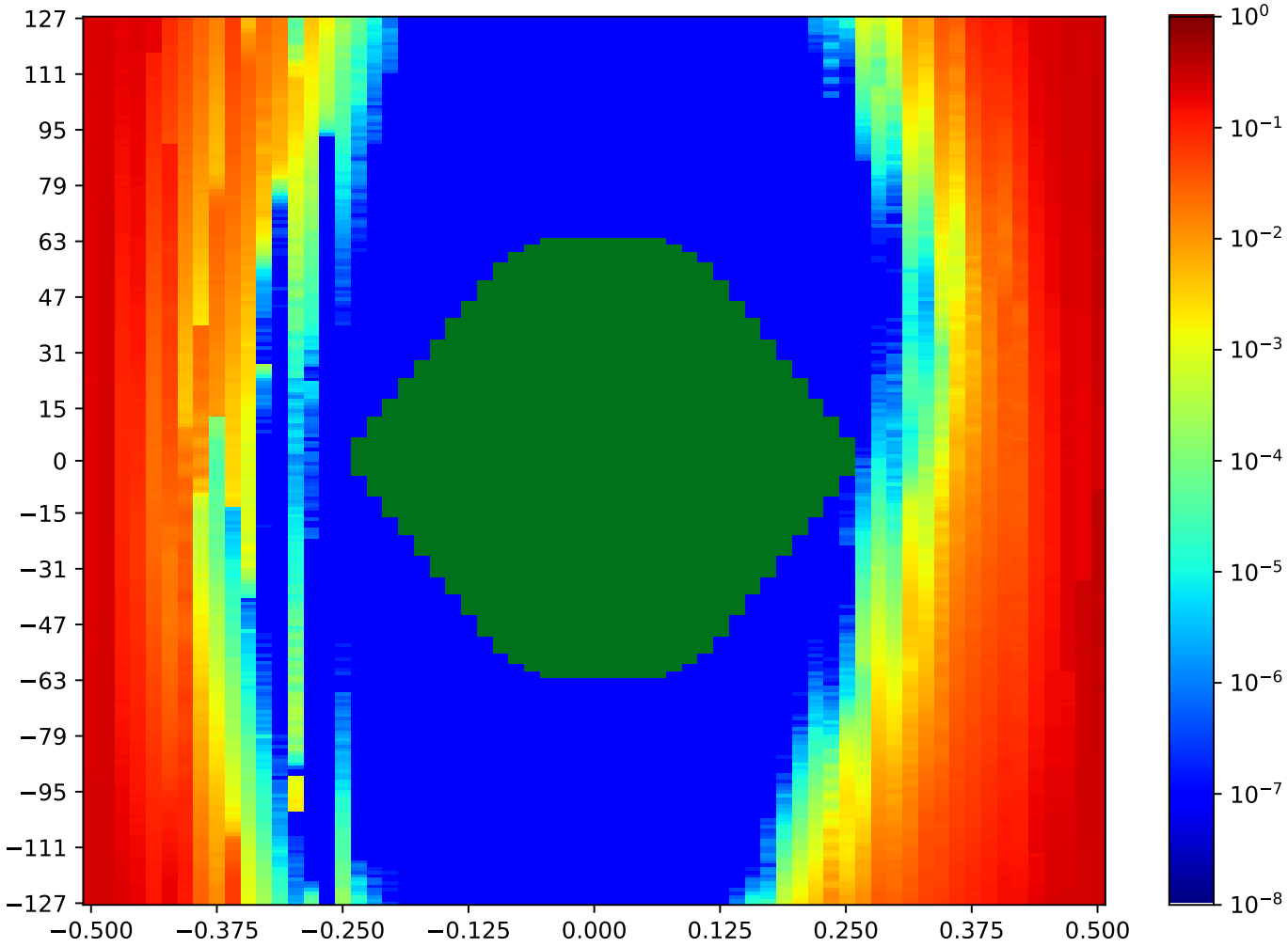


Figure 6.141: MSP_A_FPGA-TX2-00–RX18-00-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.2 MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Table 6.131: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:33:15		2019-Nov-27 10:33:42	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8078	36	55.38%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

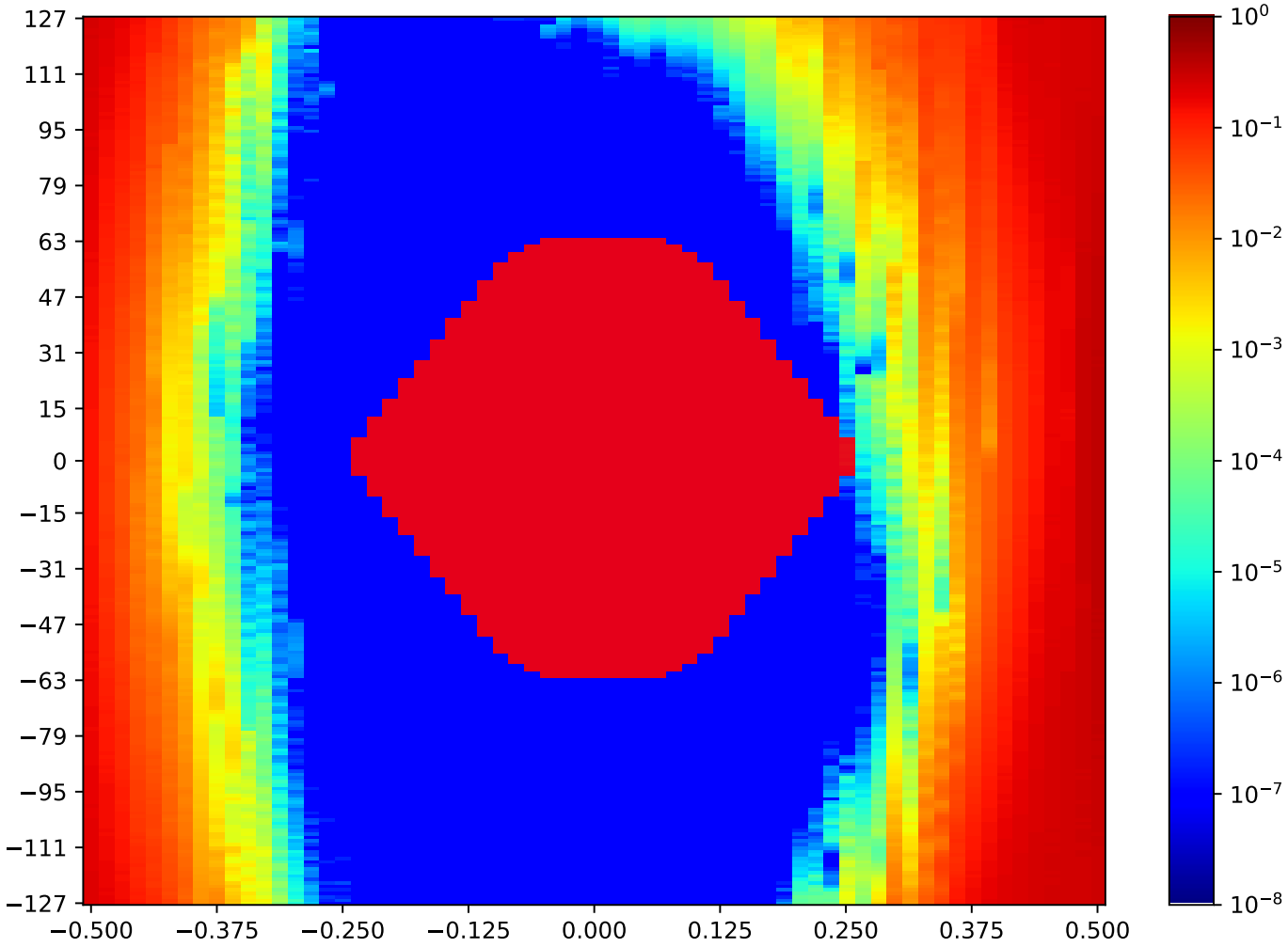


Figure 6.142: MSP_A_FPGA-TX2-01–RX18-01-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.3 MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Table 6.132: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:35:17		2019-Nov-27 10:35:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7788	37	56.92%	237	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

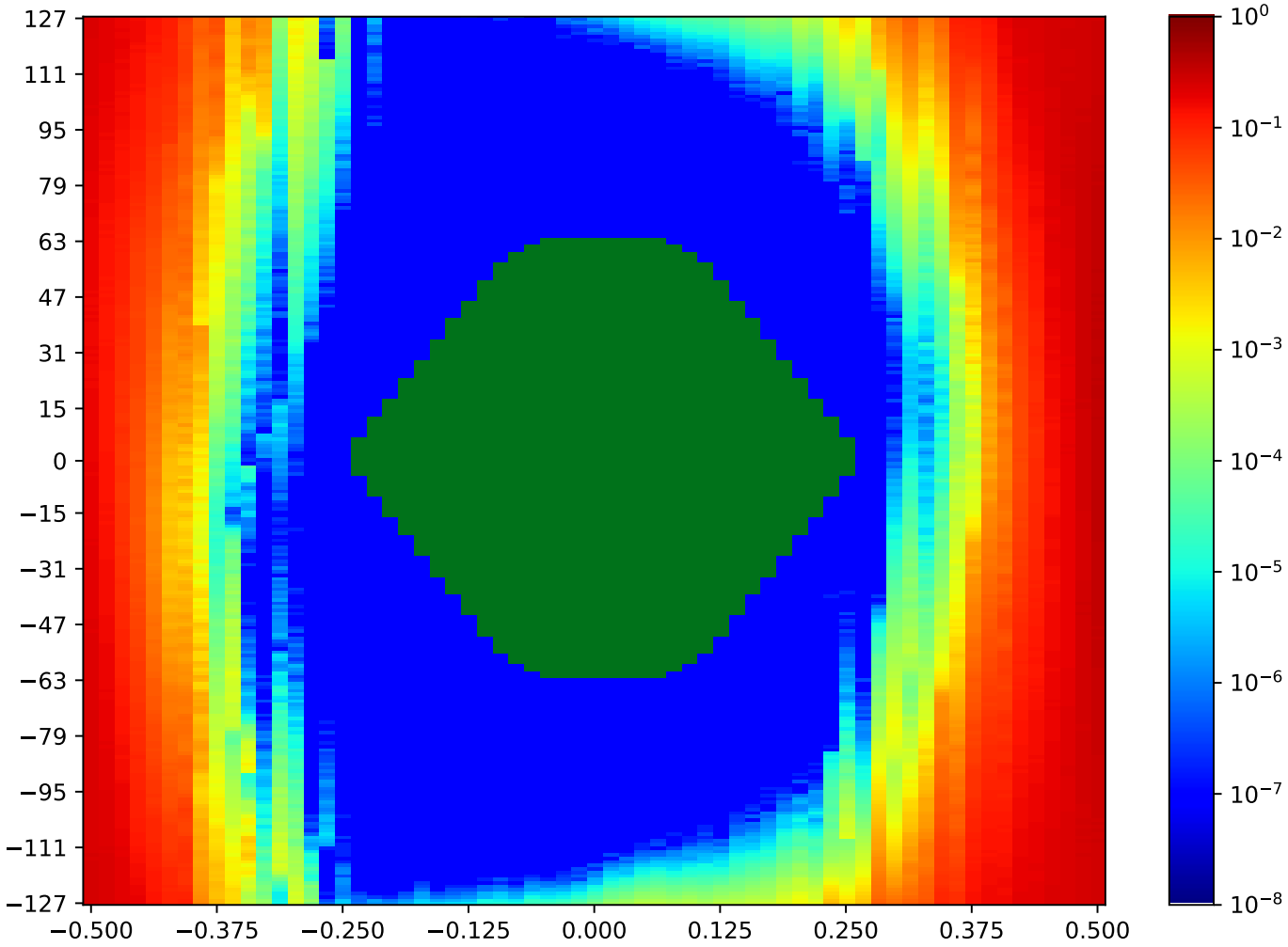


Figure 6.143: MSP_A_FPGA-TX2-02–RX18-02-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.4 MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Table 6.133: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:32:56		2019-Nov-27 10:33:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8716	42	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

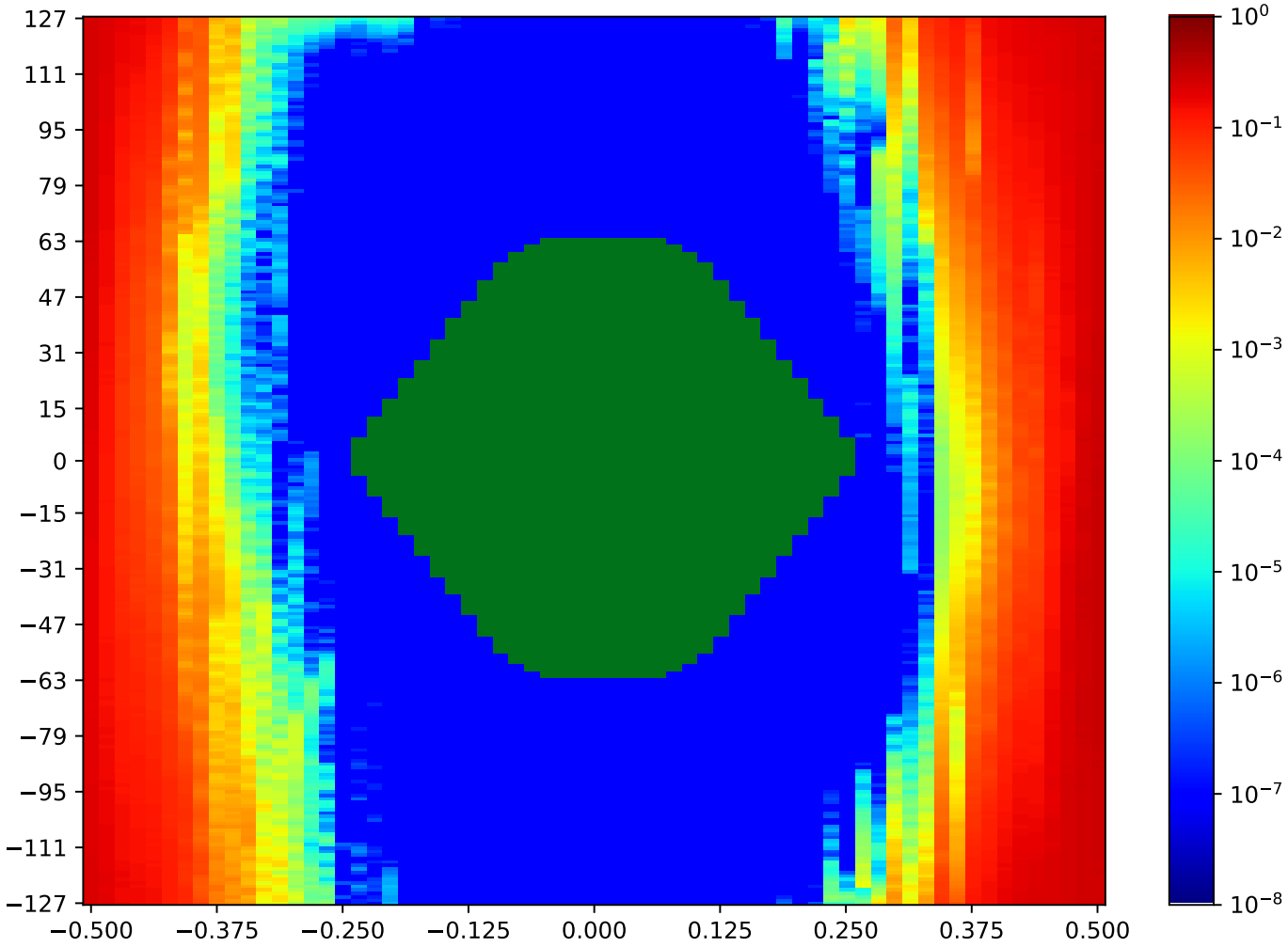


Figure 6.144: MSP_A_FPGA-TX2-03–RX18-03-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.5 MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Table 6.134: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:36:34		2019-Nov-27 10:37:03	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8527	41	60.00%	254	97.65%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

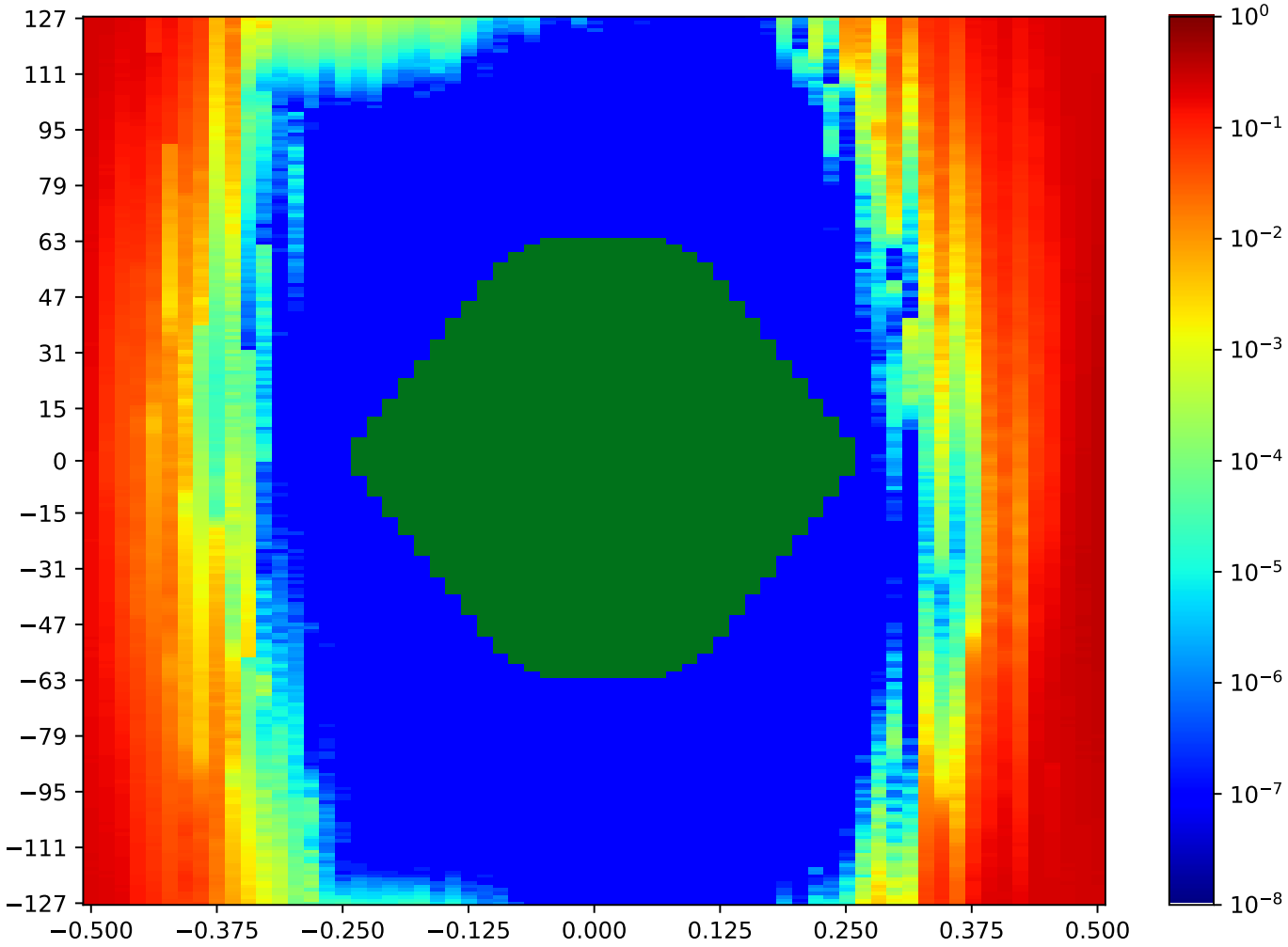


Figure 6.145: MSP_A_FPGA-TX2-04–RX18-04-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.6 MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Table 6.135: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:33:42		2019-Nov-27 10:34:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8852	40	61.54%	253	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

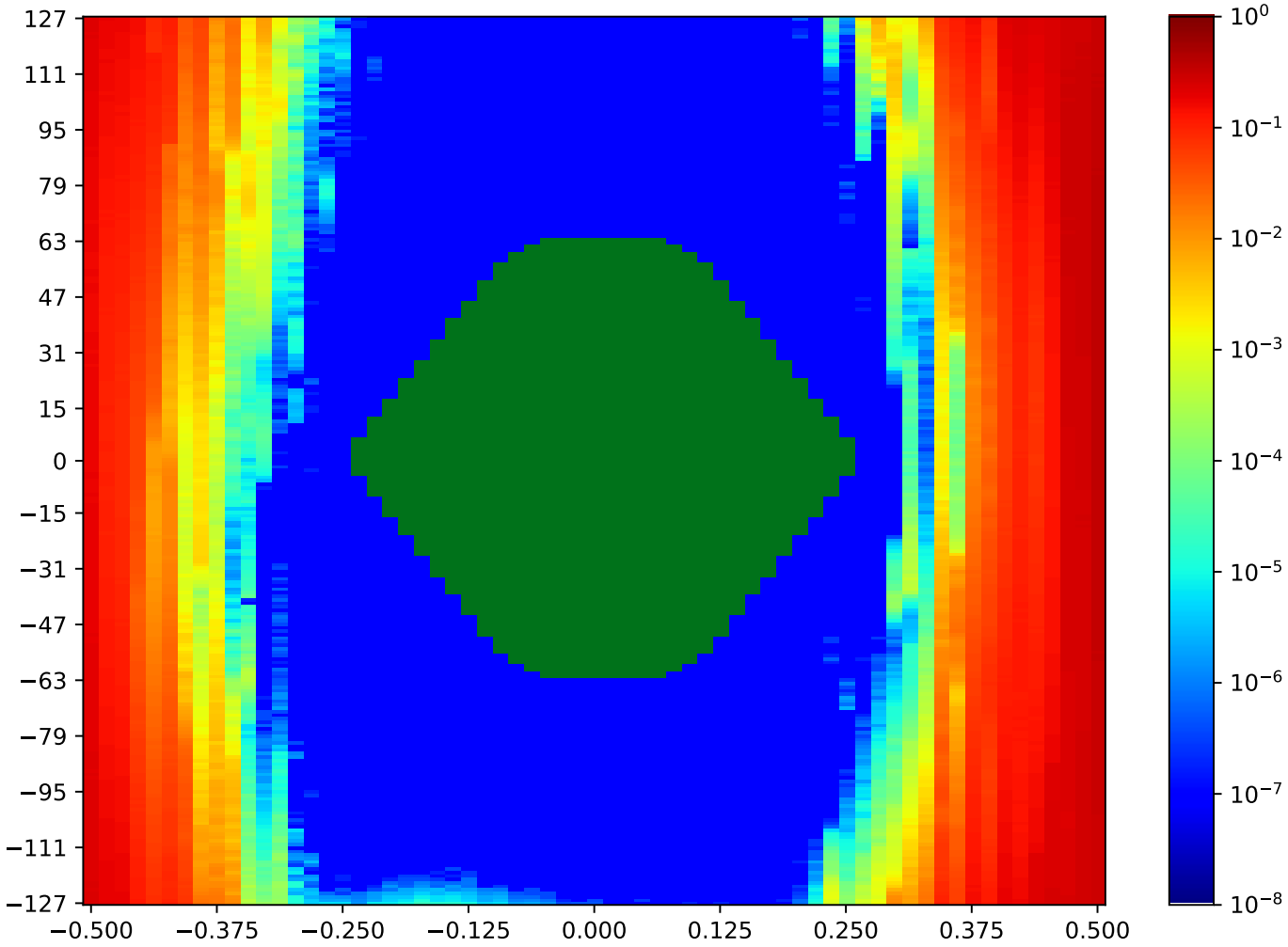


Figure 6.146: MSP_A_FPGA-TX2-05–RX18-05-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.7 MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Table 6.136: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:37:31		2019-Nov-27 10:38:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8482	40	61.54%	235	91.76%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

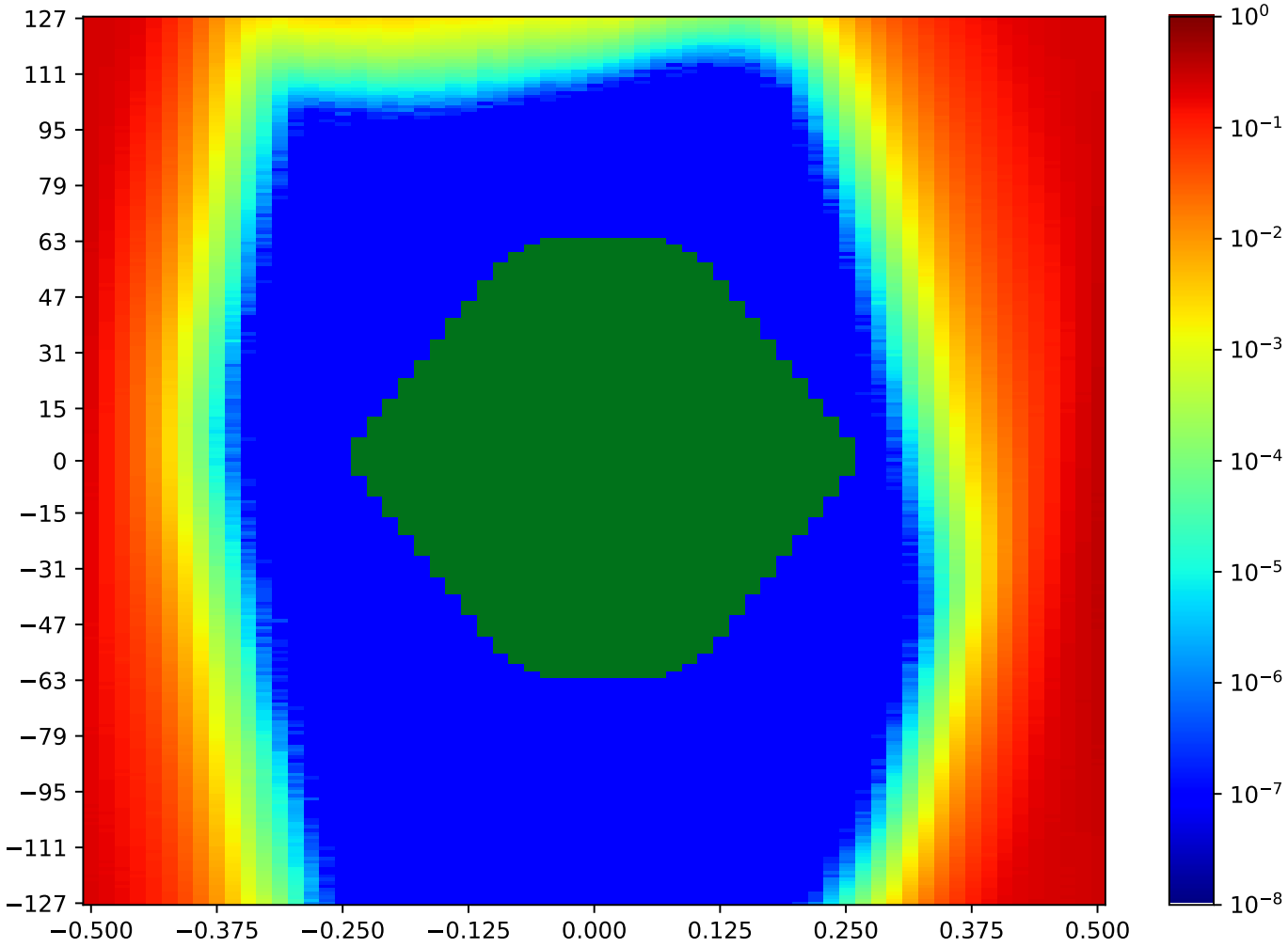


Figure 6.147: MSP_A_FPGA-TX2-06–RX18-06-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.8 MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Table 6.137: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:34:38		2019-Nov-27 10:34:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9164	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

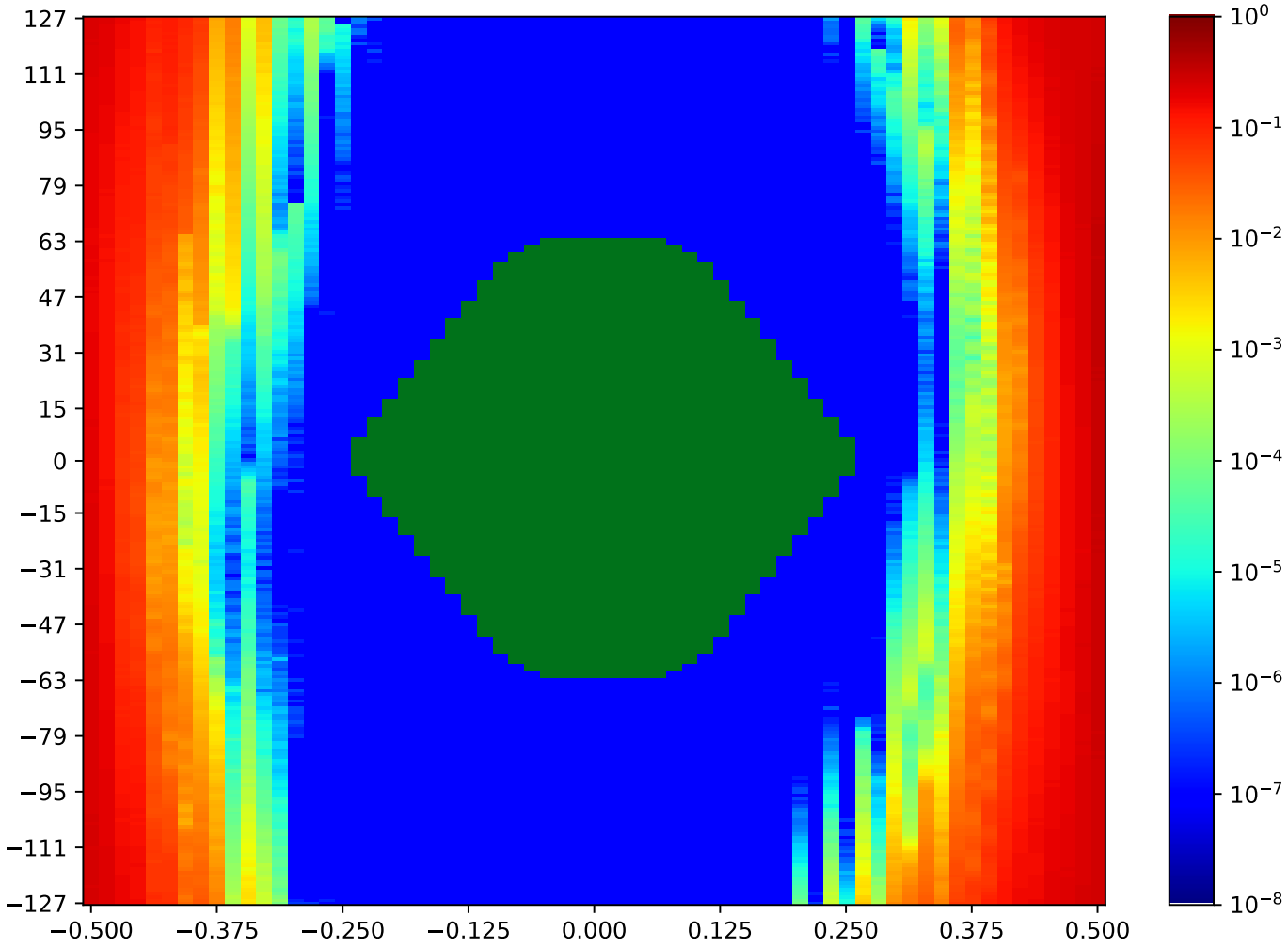


Figure 6.148: MSP_A_FPGA-TX2-07–RX18-07-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.9 MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Table 6.138: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:37:03		2019-Nov-27 10:37:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8628	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

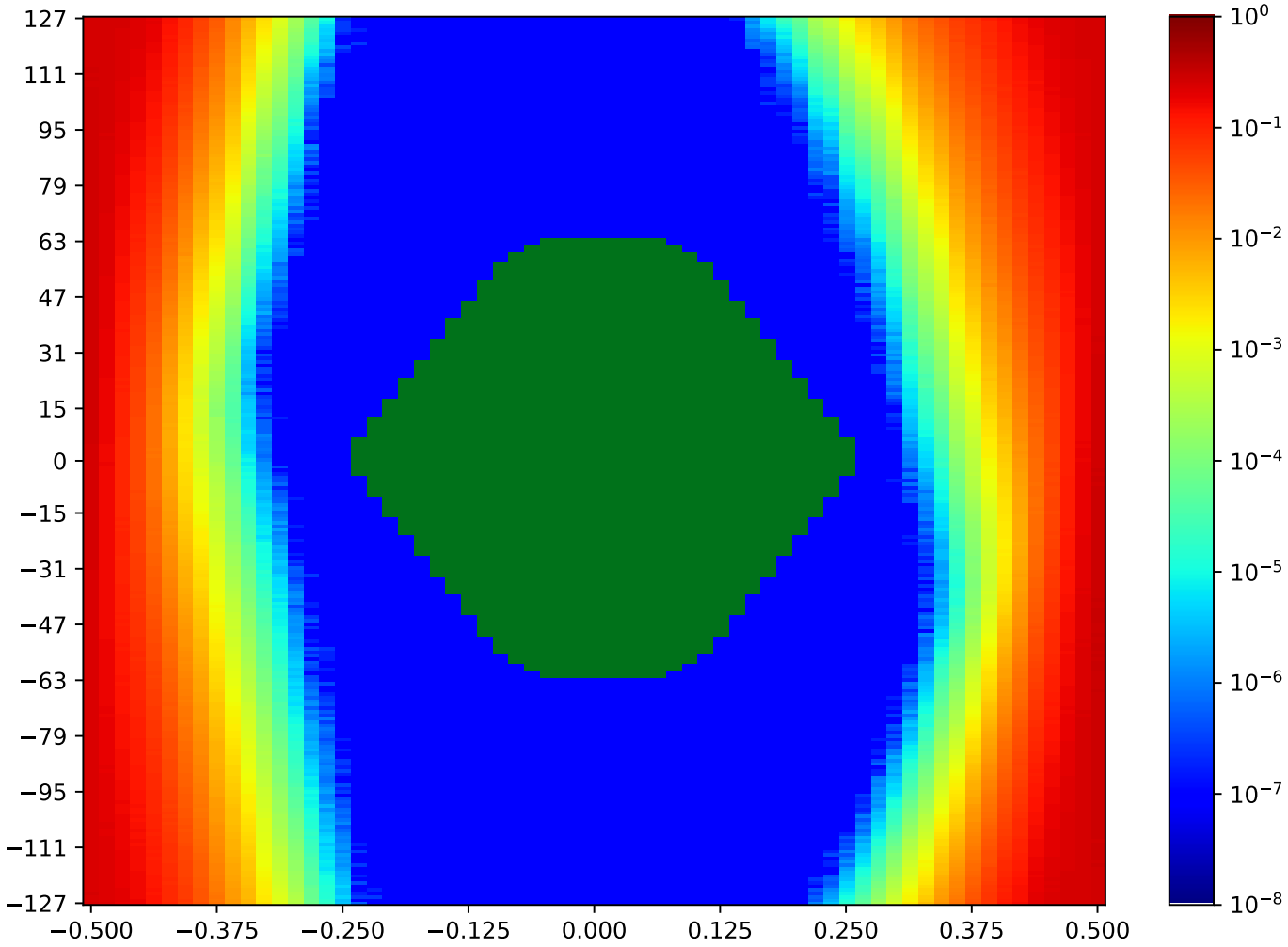


Figure 6.149: MSP_A_FPGA-TX2-08–RX18-08-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.10 MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Table 6.139: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:34:58		2019-Nov-27 10:35:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9312	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

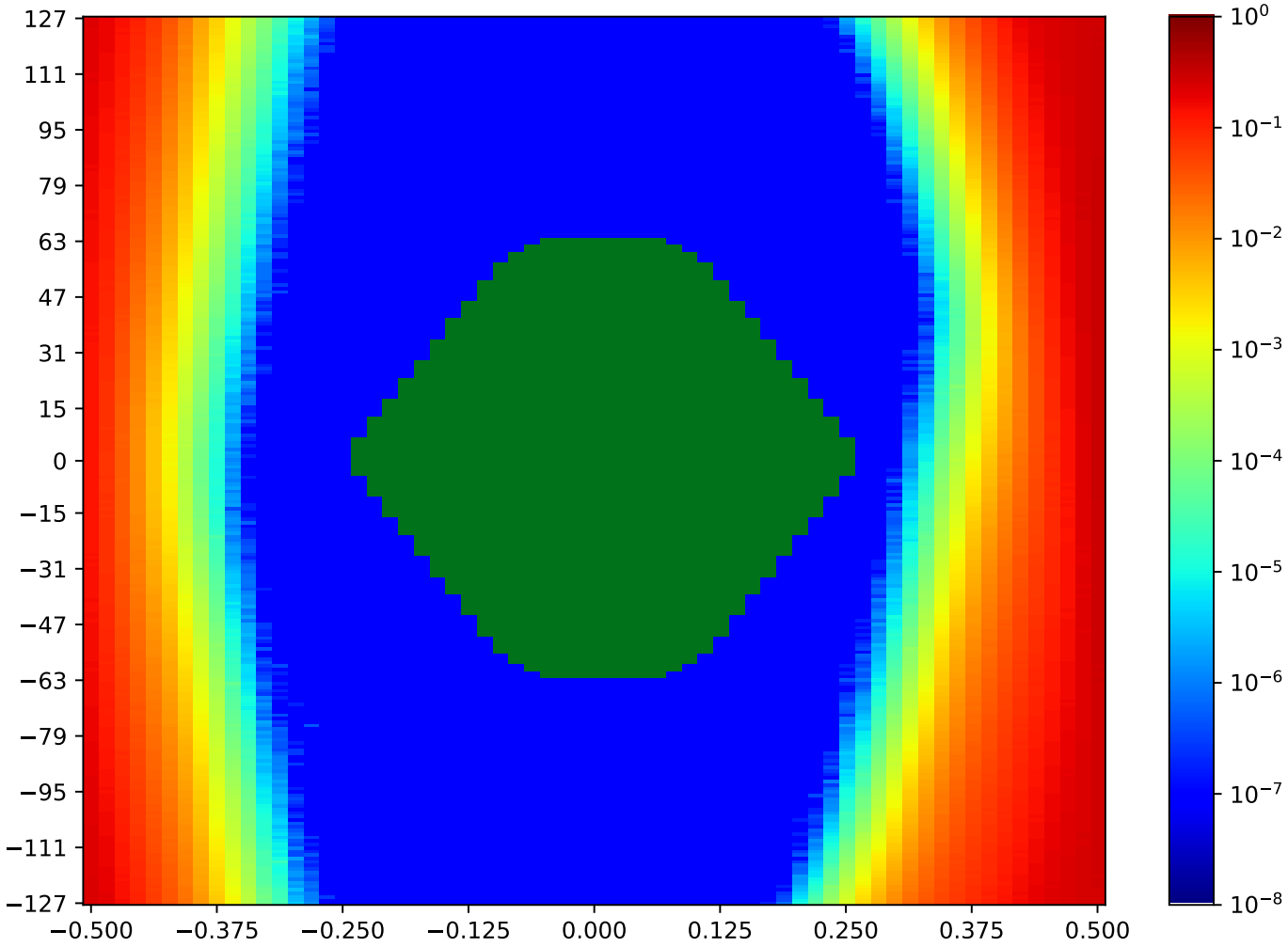


Figure 6.150: MSP_A_FPGA-TX2-09–RX18-09-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.11 MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Table 6.140: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:36:08		2019-Nov-27 10:36:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7744	36	50.77%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

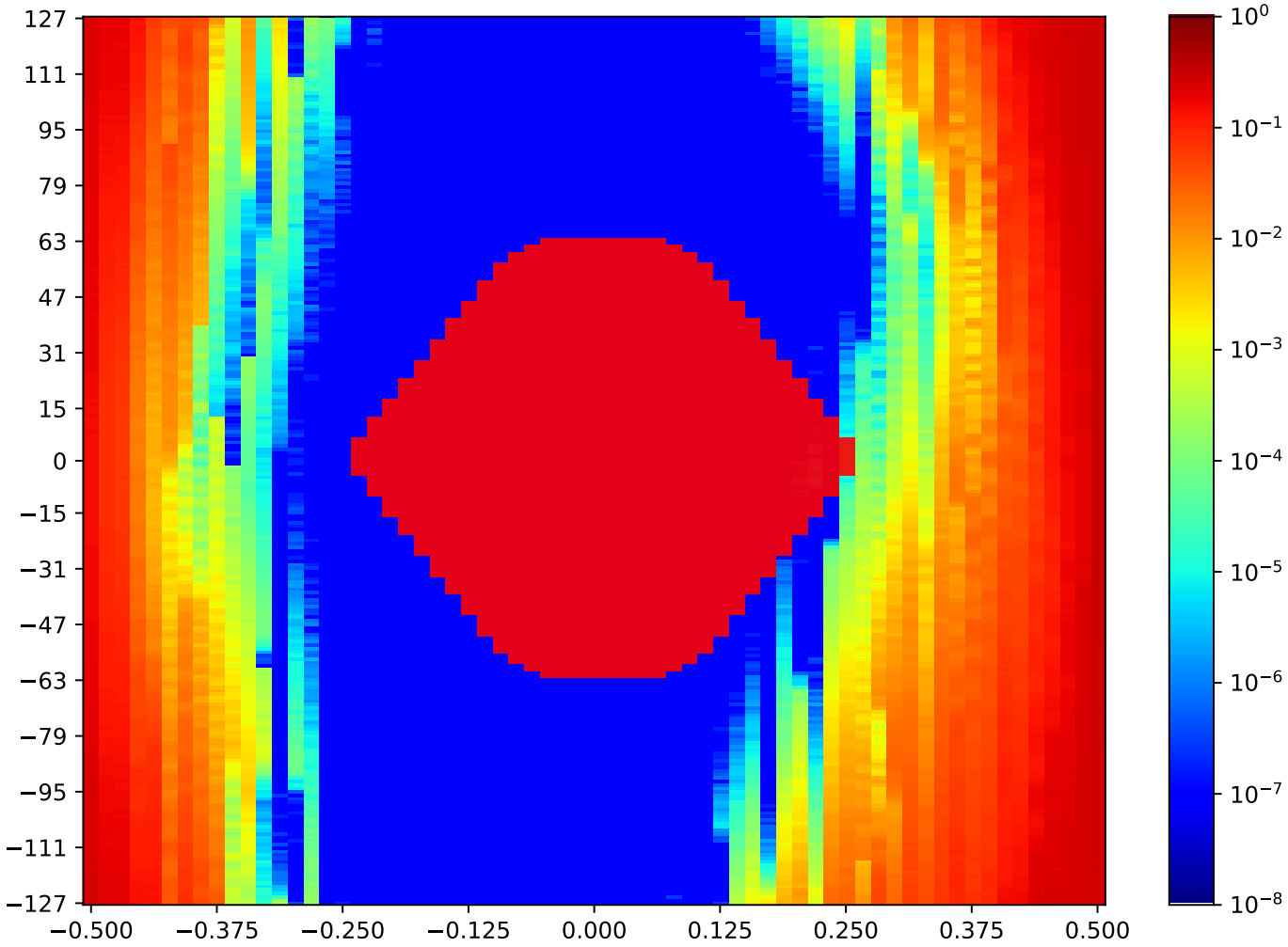


Figure 6.151: MSP_A_FPGA-TX2-10–RX18-10-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.11.12 MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Table 6.141: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:35:45		2019-Nov-27 10:36:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7946	35	53.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

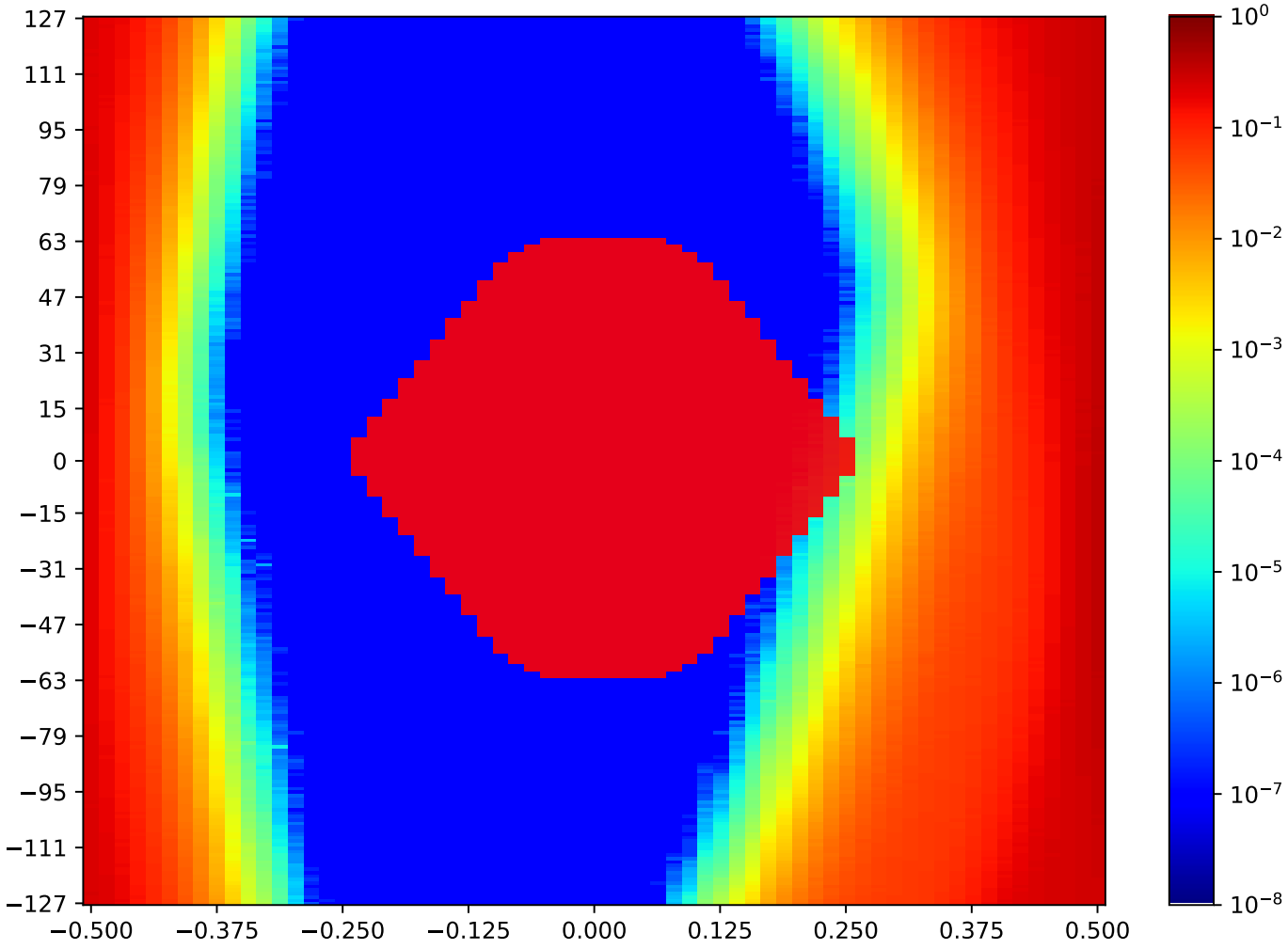


Figure 6.152: MSP_A_FPGA-TX2-11–RX18-11-MSP_C_FPGA

Call back to summary Figure 6.140. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12 MSP_C TX3 MSP_A RX8 Minipod Loopback

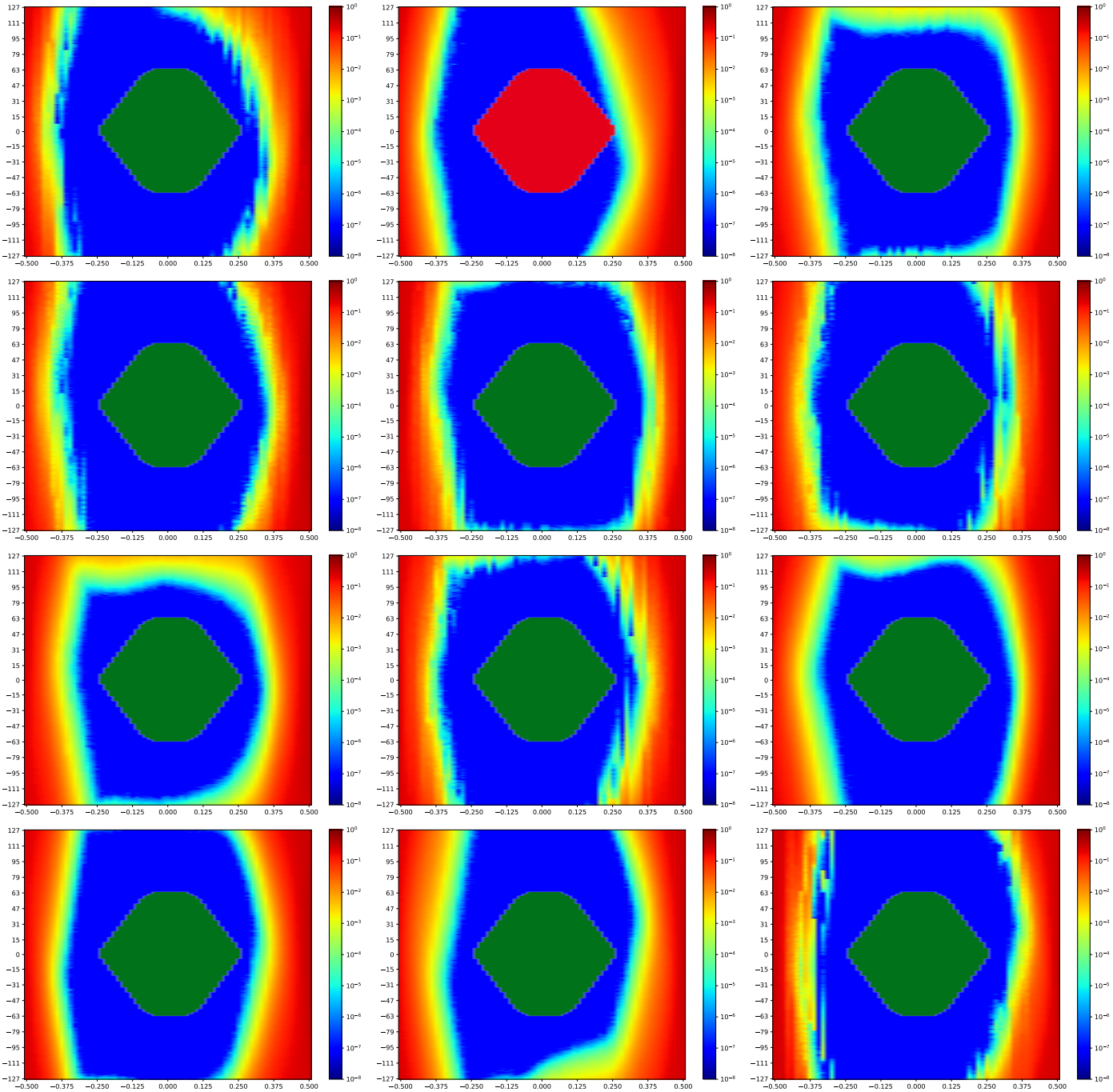


Figure 6.153: MSP_C TX3 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.166.

6.12.1 MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Table 6.142: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:39:11		2019-Nov-27 10:39:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9217	45	67.69%	241	94.12%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

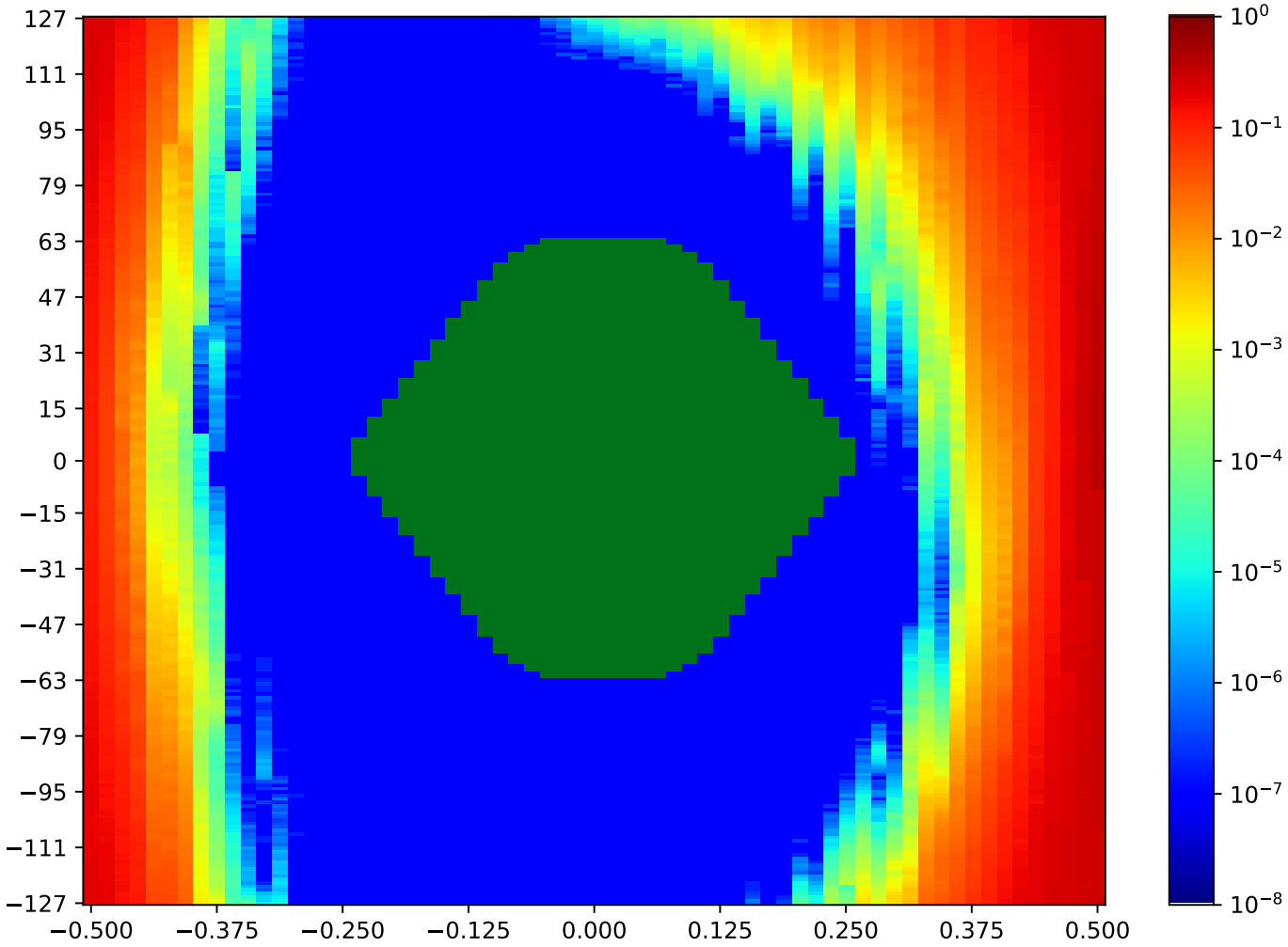


Figure 6.154: MSP_C_FPGA-TX3-00–RX8-00-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.2 MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Table 6.143: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:39:58		2019-Nov-27 10:40:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8319	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

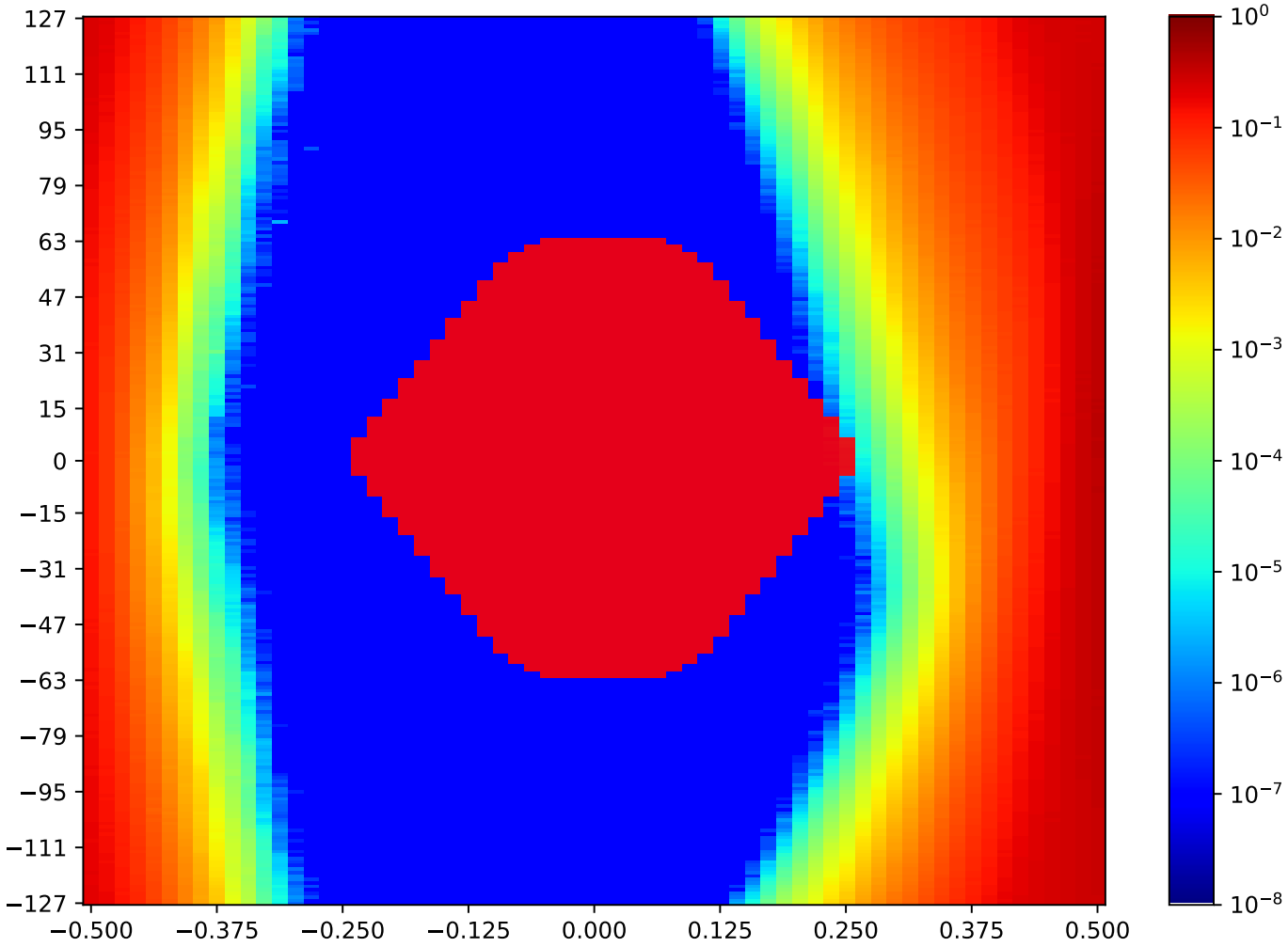


Figure 6.155: MSP_C_FPGA-TX3-01–RX8-01-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.3 MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Table 6.144: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:40:24		2019-Nov-27 10:40:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7762	40	61.54%	208	81.57%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

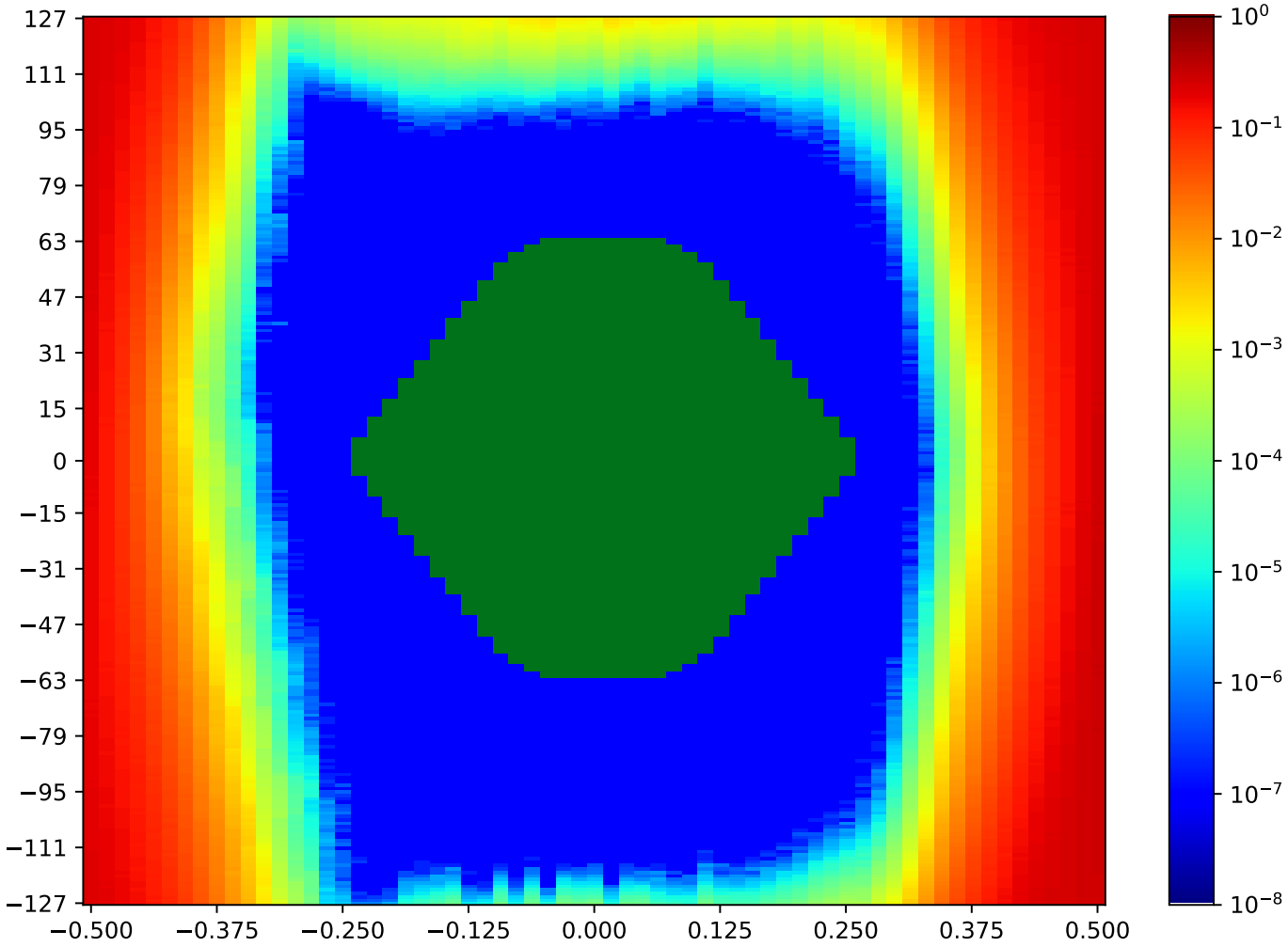


Figure 6.156: MSP_C_FPGA-TX3-02–RX8-02-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.4 MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Table 6.145: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:38:19		2019-Nov-27 10:38:44	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9517	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

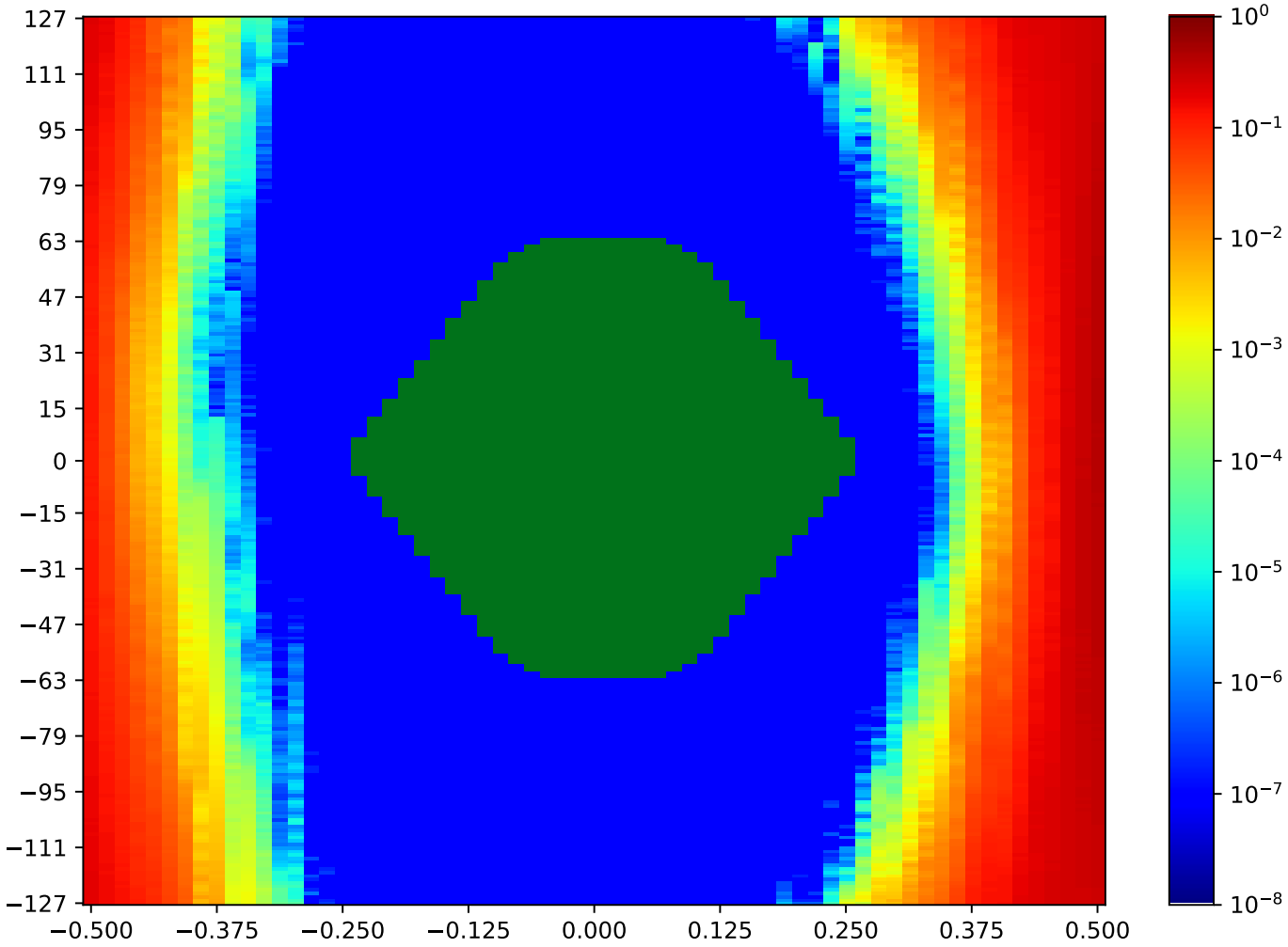


Figure 6.157: MSP_C_FPGA-TX3-03–RX8-03-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.5 MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Table 6.146: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:41:46		2019-Nov-27 10:42:15	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9074	42	64.62%	240	93.33%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

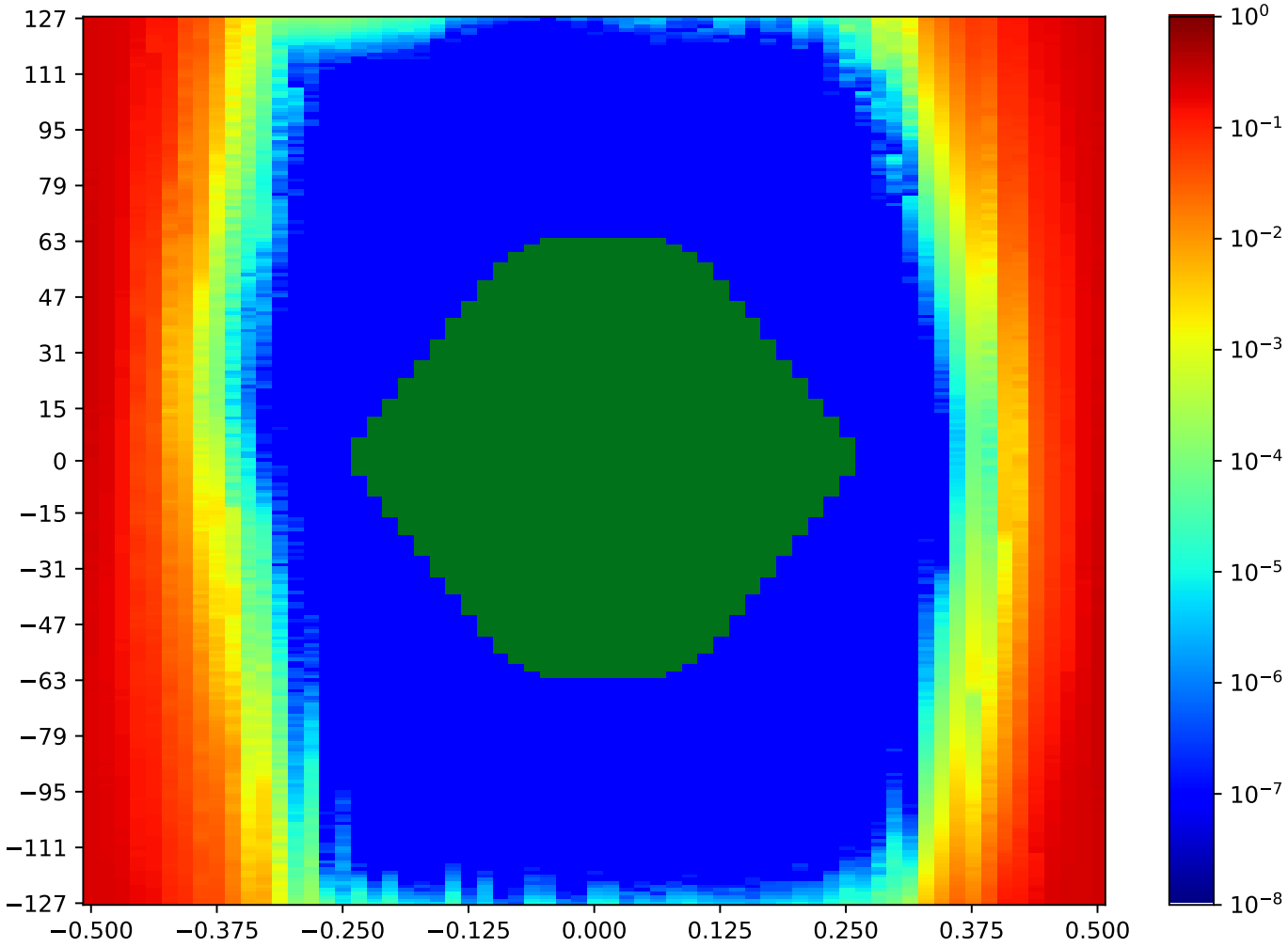


Figure 6.158: MSP_C_FPGA-TX3-04–RX8-04-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.6 MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Table 6.147: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:38:00		2019-Nov-27 10:38:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8583	39	58.46%	247	96.47%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

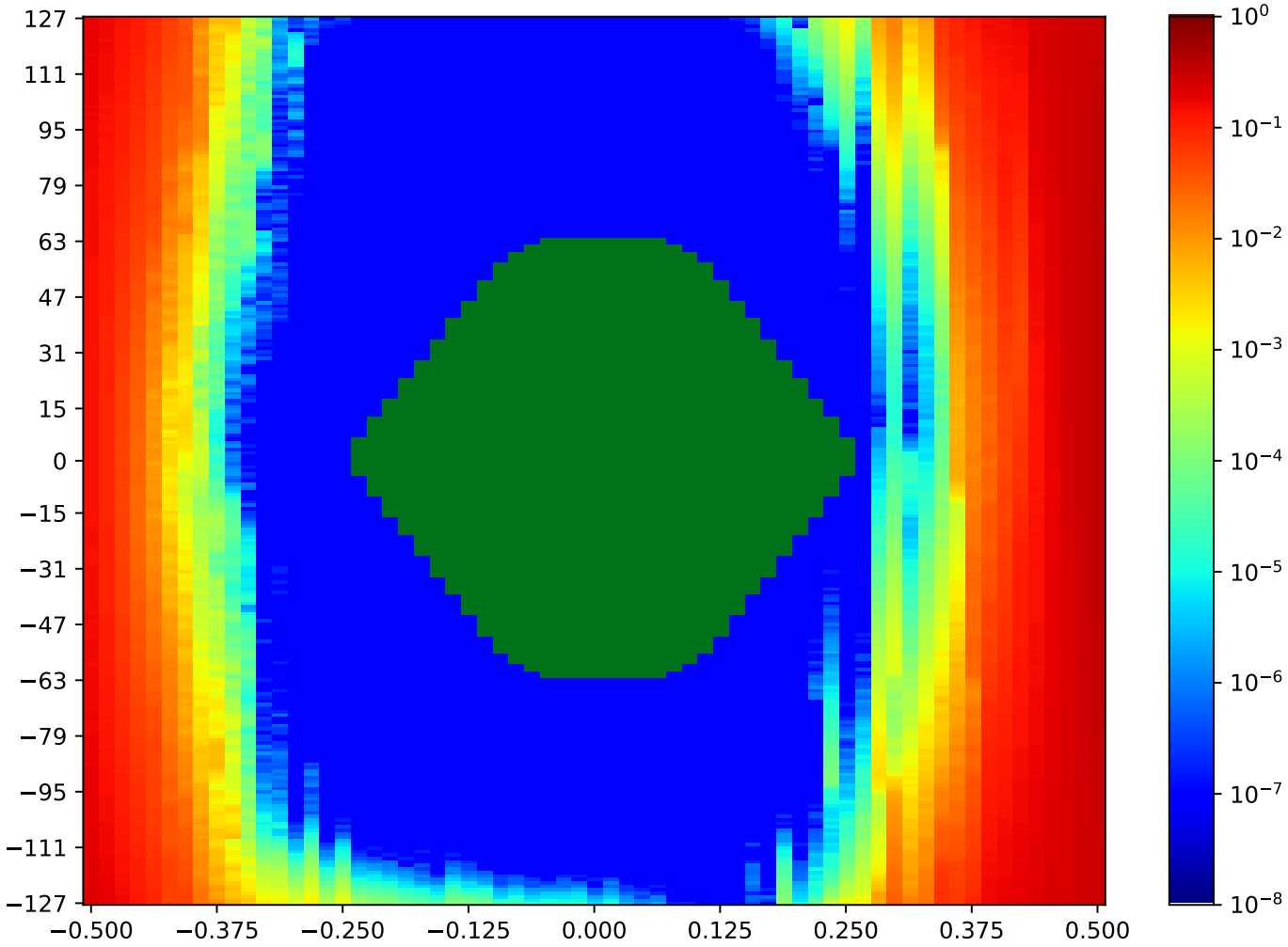


Figure 6.159: MSP_C_FPGA-TX3-05–RX8-05-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.7 MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Table 6.148: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:42:43		2019-Nov-27 10:43:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	6792	39	60.00%	209	81.96%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

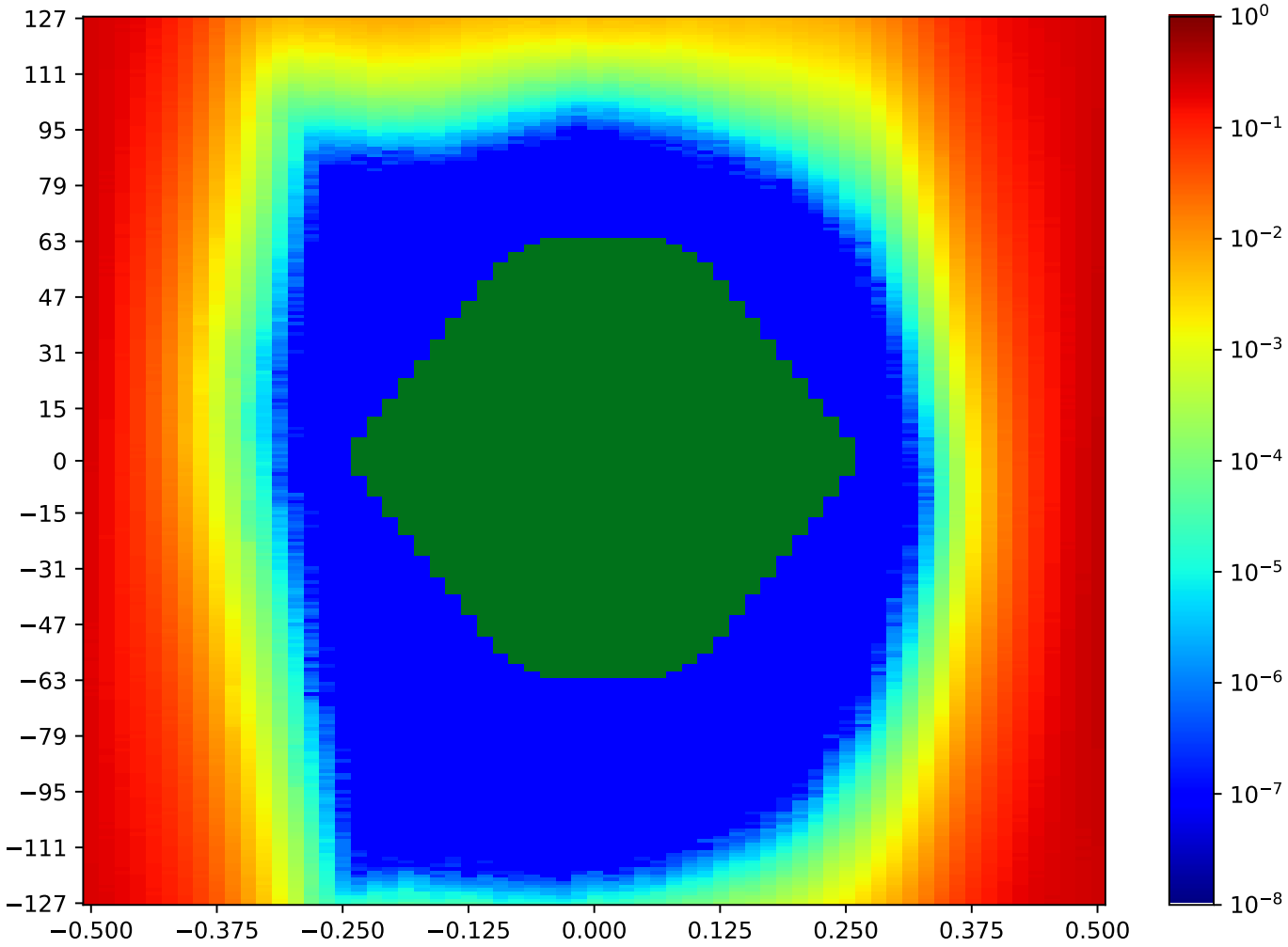


Figure 6.160: MSP_C_FPGA-TX3-06–RX8-06-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.8 MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Table 6.149: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:38:44		2019-Nov-27 10:39:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8550	40	61.54%	244	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

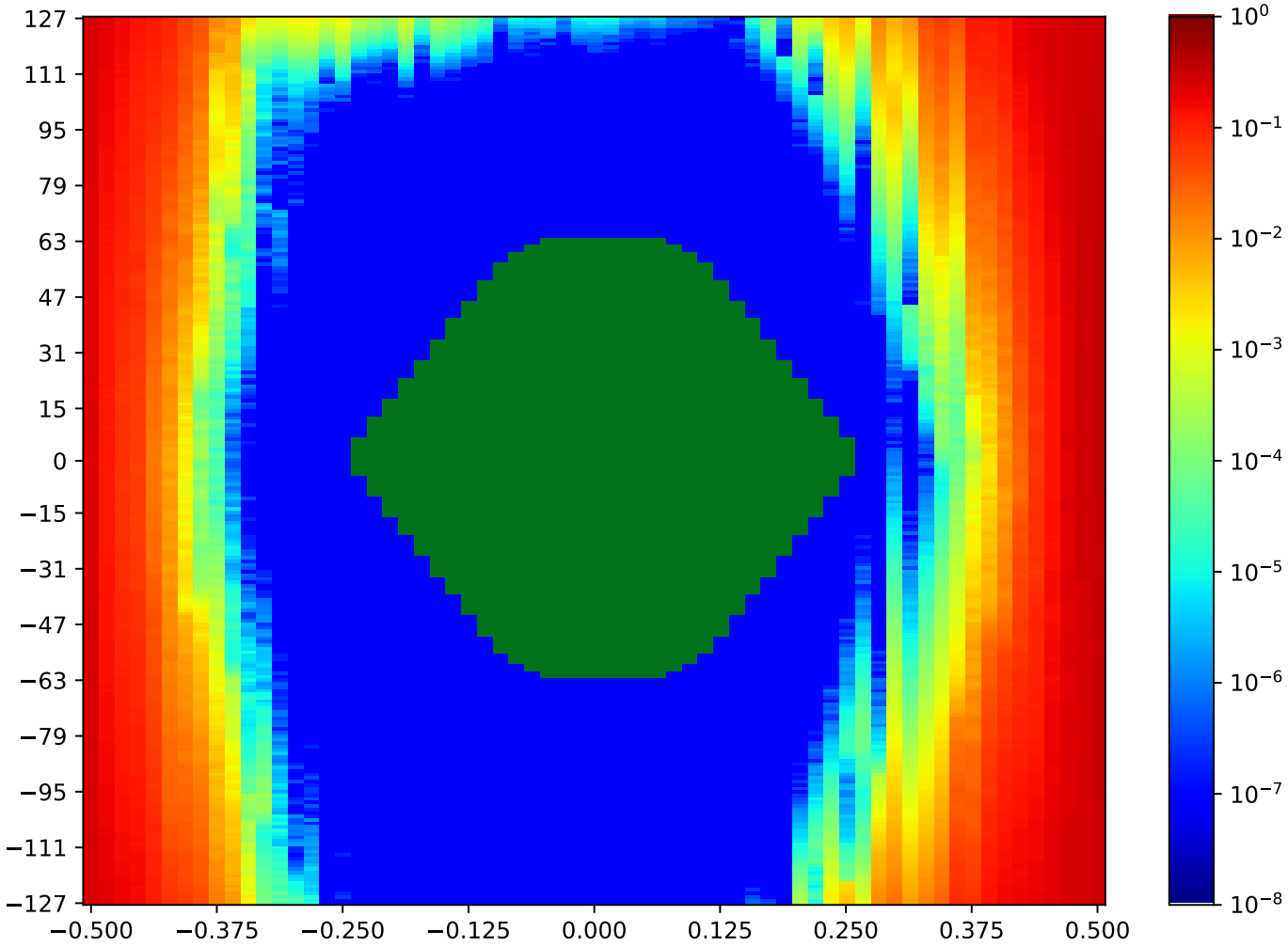


Figure 6.161: MSP_C_FPGA-TX3-07–RX8-07-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.9 MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Table 6.150: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:42:16		2019-Nov-27 10:42:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8357	41	63.08%	235	92.16%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

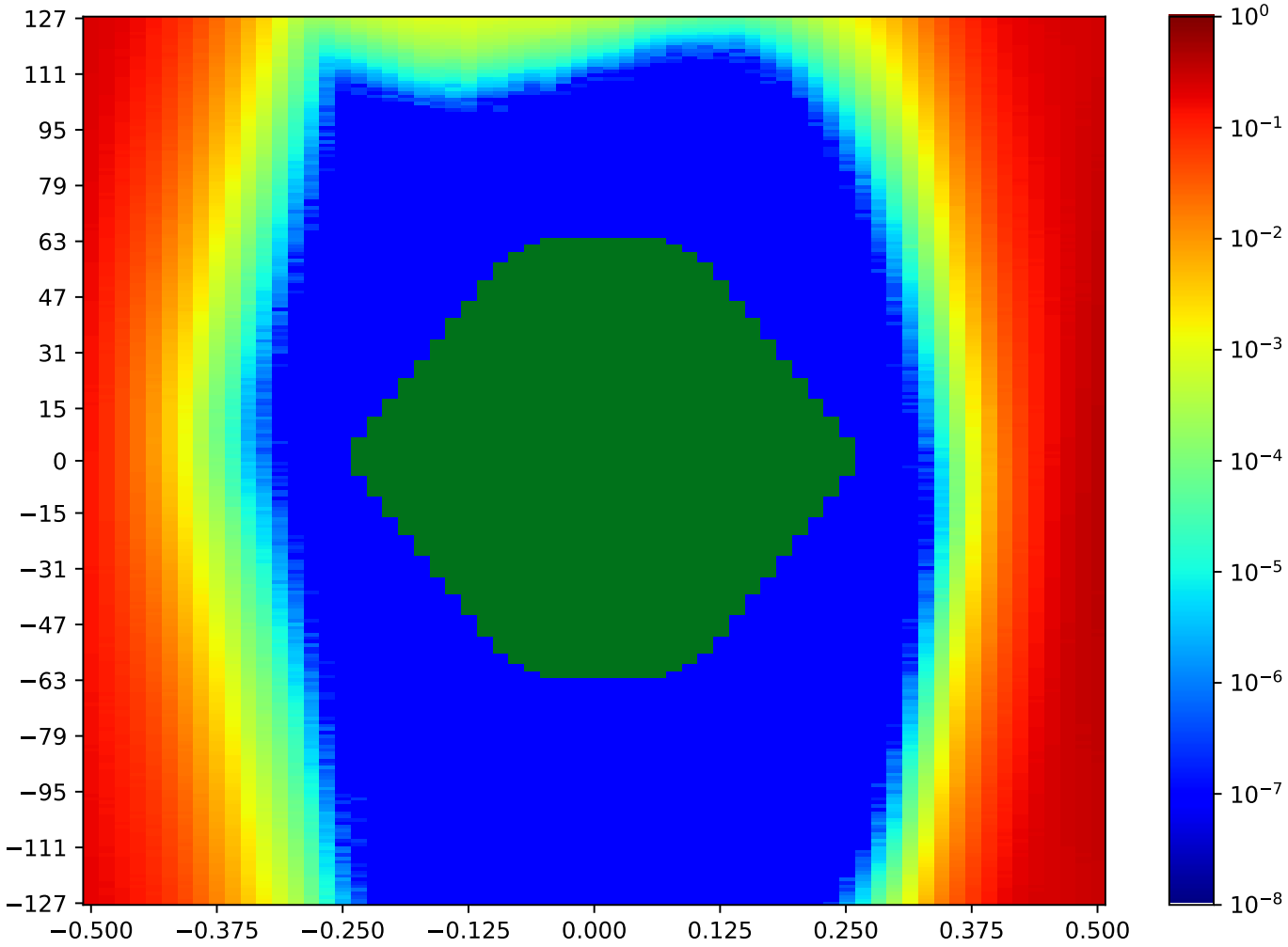


Figure 6.162: MSP_C_FPGA-TX3-08–RX8-08-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.10 MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Table 6.151: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:39:31		2019-Nov-27 10:39:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8961	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

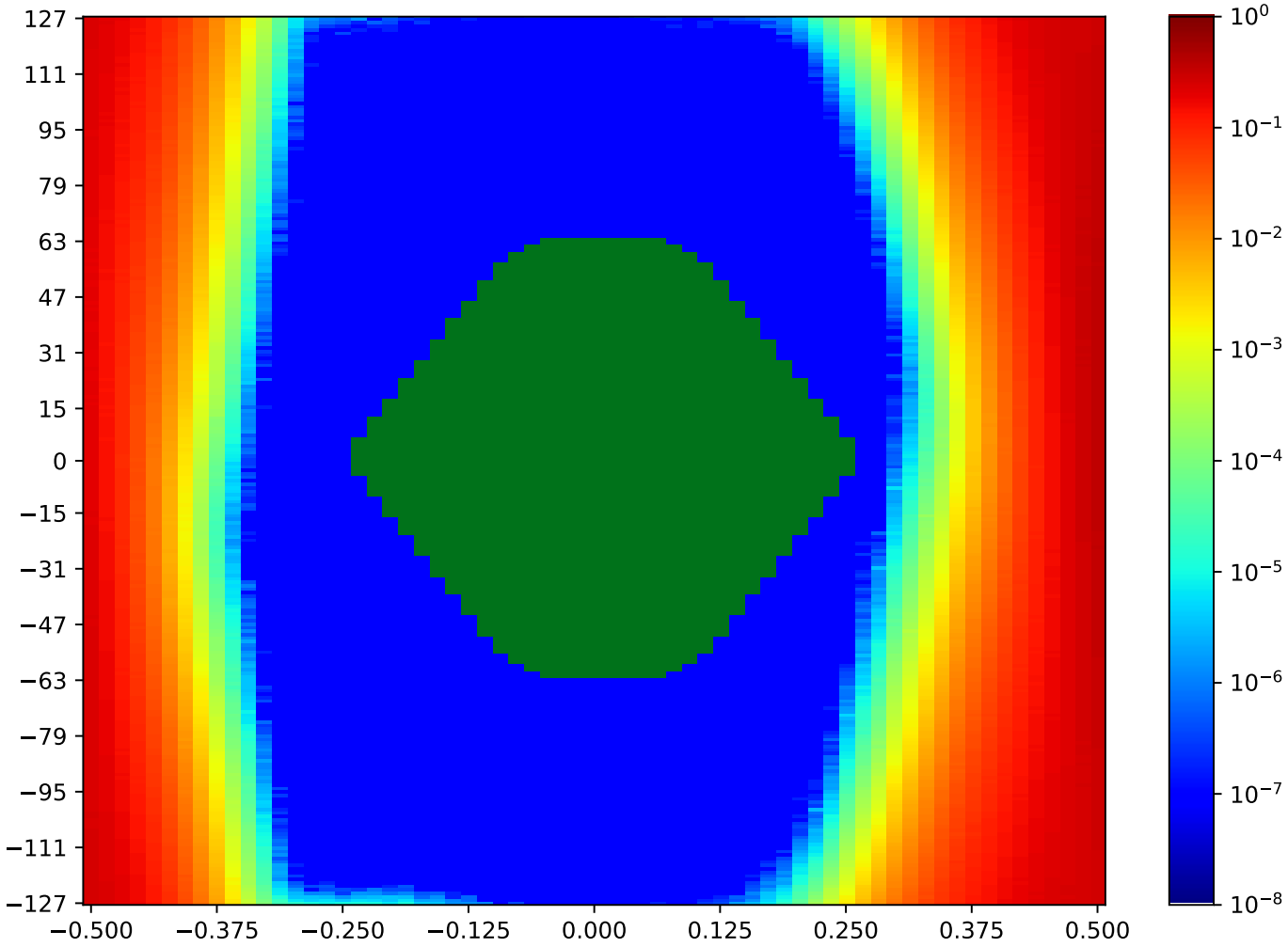


Figure 6.163: MSP_C_FPGA-TX3-09–RX8-09-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.11 MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Table 6.152: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:41:20		2019-Nov-27 10:41:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8110	38	58.46%	234	91.37%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

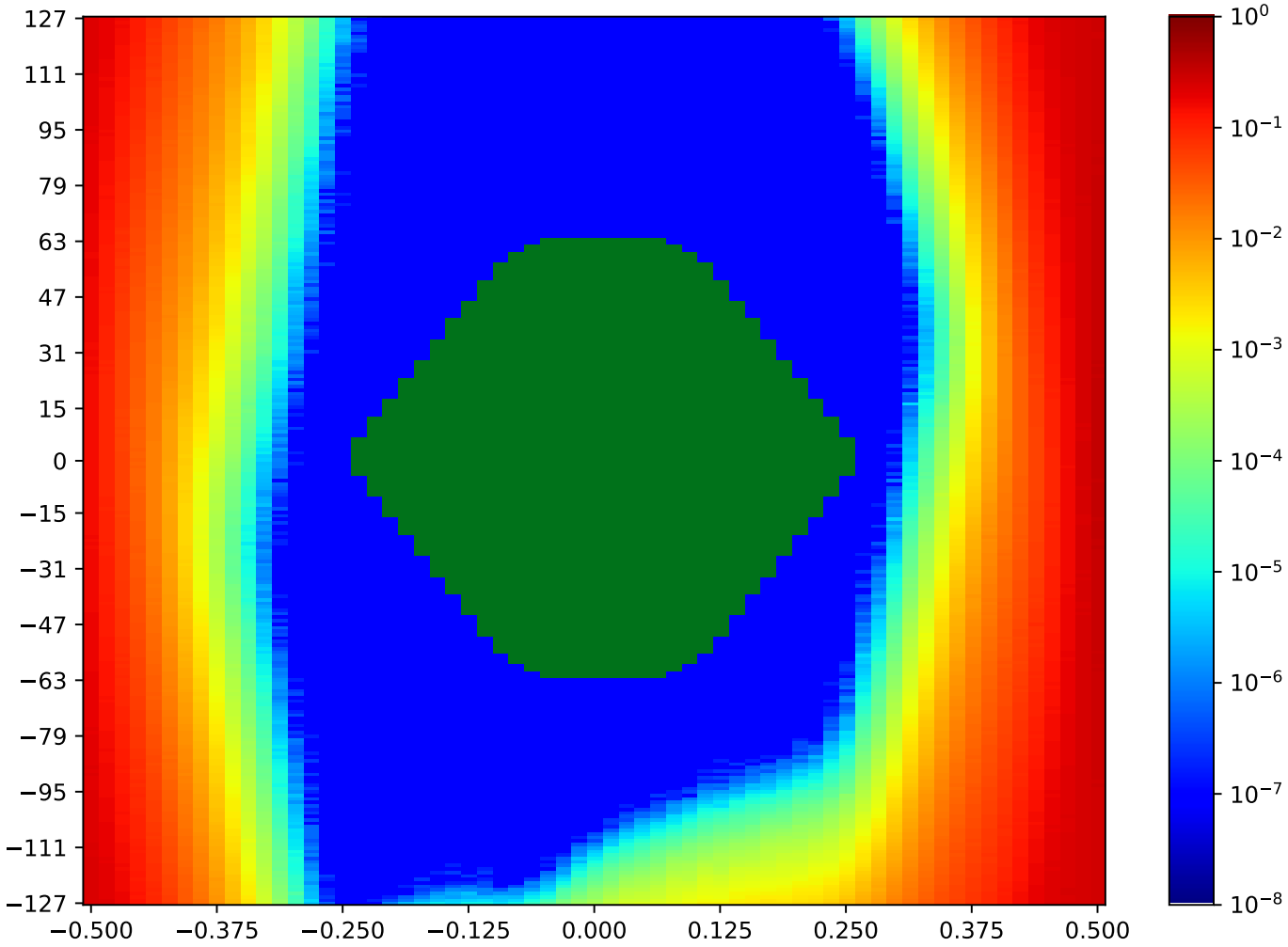


Figure 6.164: MSP_C_FPGA-TX3-10–RX8-10-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.12.12 MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Table 6.153: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:40:54		2019-Nov-27 10:41:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9824	43	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

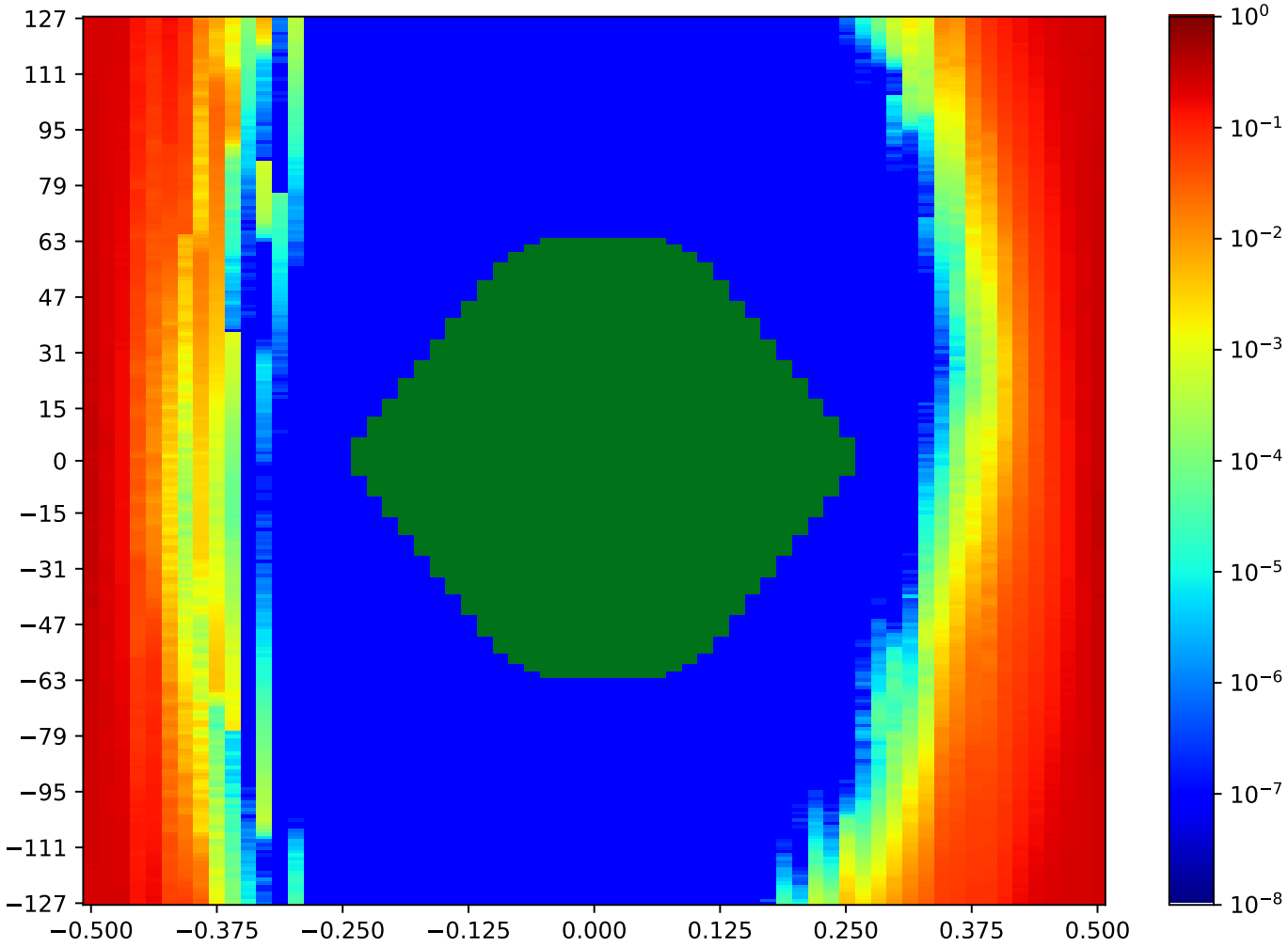


Figure 6.165: MSP_C_FPGA-TX3-11–RX8-11-MSP_A_FPGA

Call back to summary Figure 6.153. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13 MSP_C TX4 MSP_A RX9 Minipod Loopback

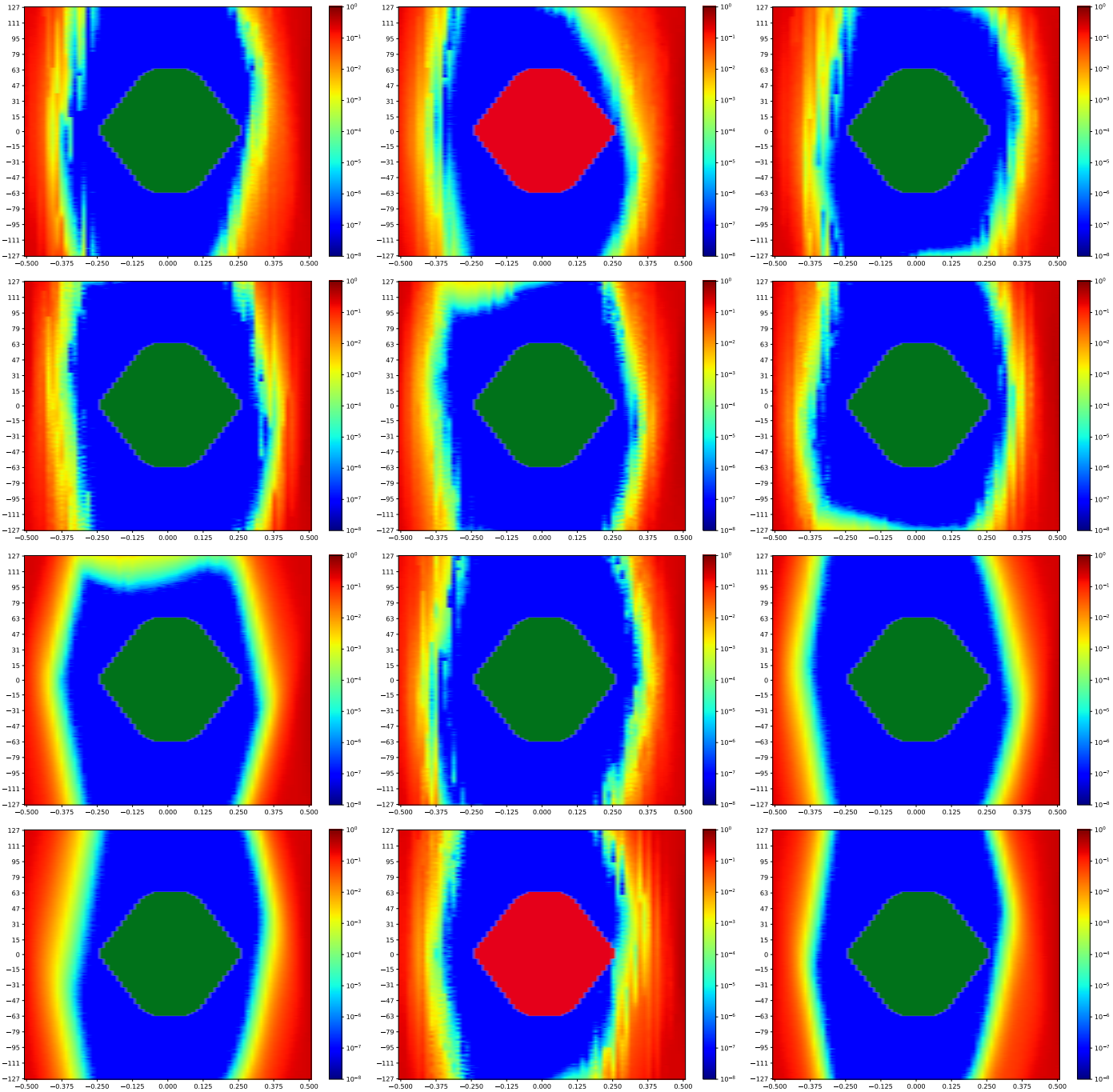


Figure 6.166: MSP_C TX4 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.179.

6.13.1 MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Table 6.154: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:44:22		2019-Nov-27 10:44:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8600	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

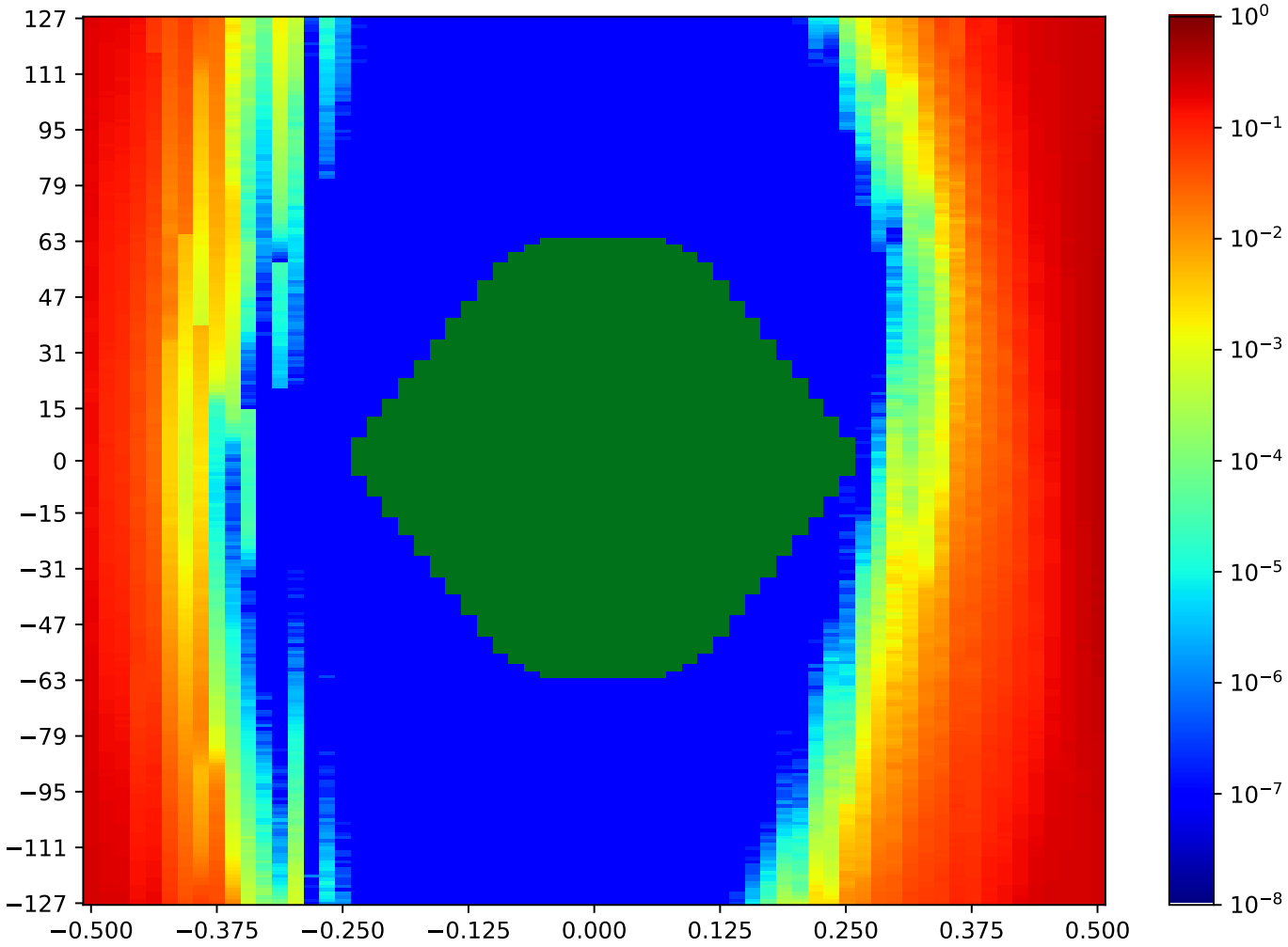


Figure 6.167: MSP_C_FPGA-TX4-00–RX9-00-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.2 MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Table 6.155: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:43:31		2019-Nov-27 10:43:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8039	38	56.92%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

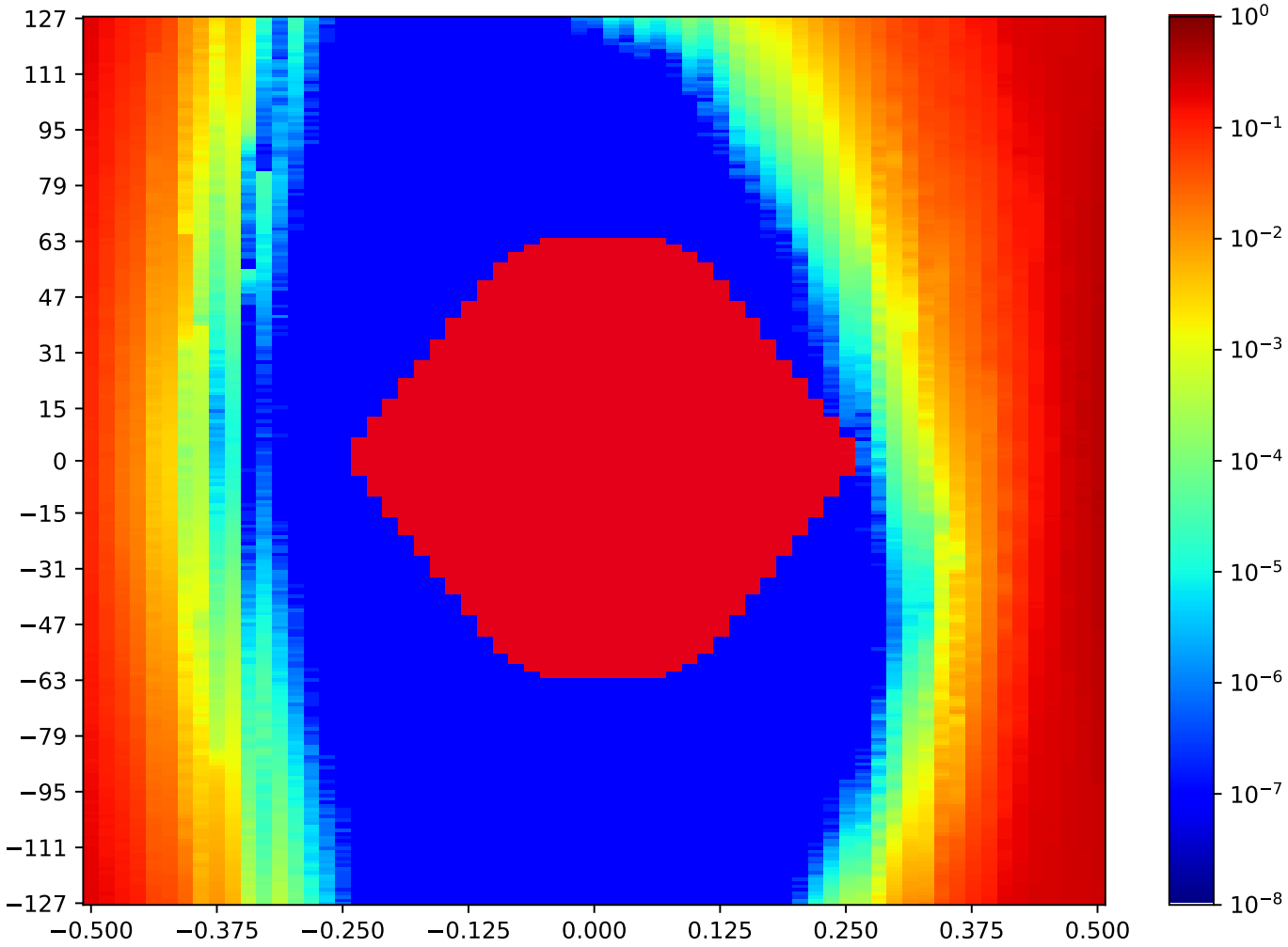


Figure 6.168: MSP_C_FPGA-TX4-01–RX9-01-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.3 MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Table 6.156: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:45:39		2019-Nov-27 10:46:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8276	40	60.00%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

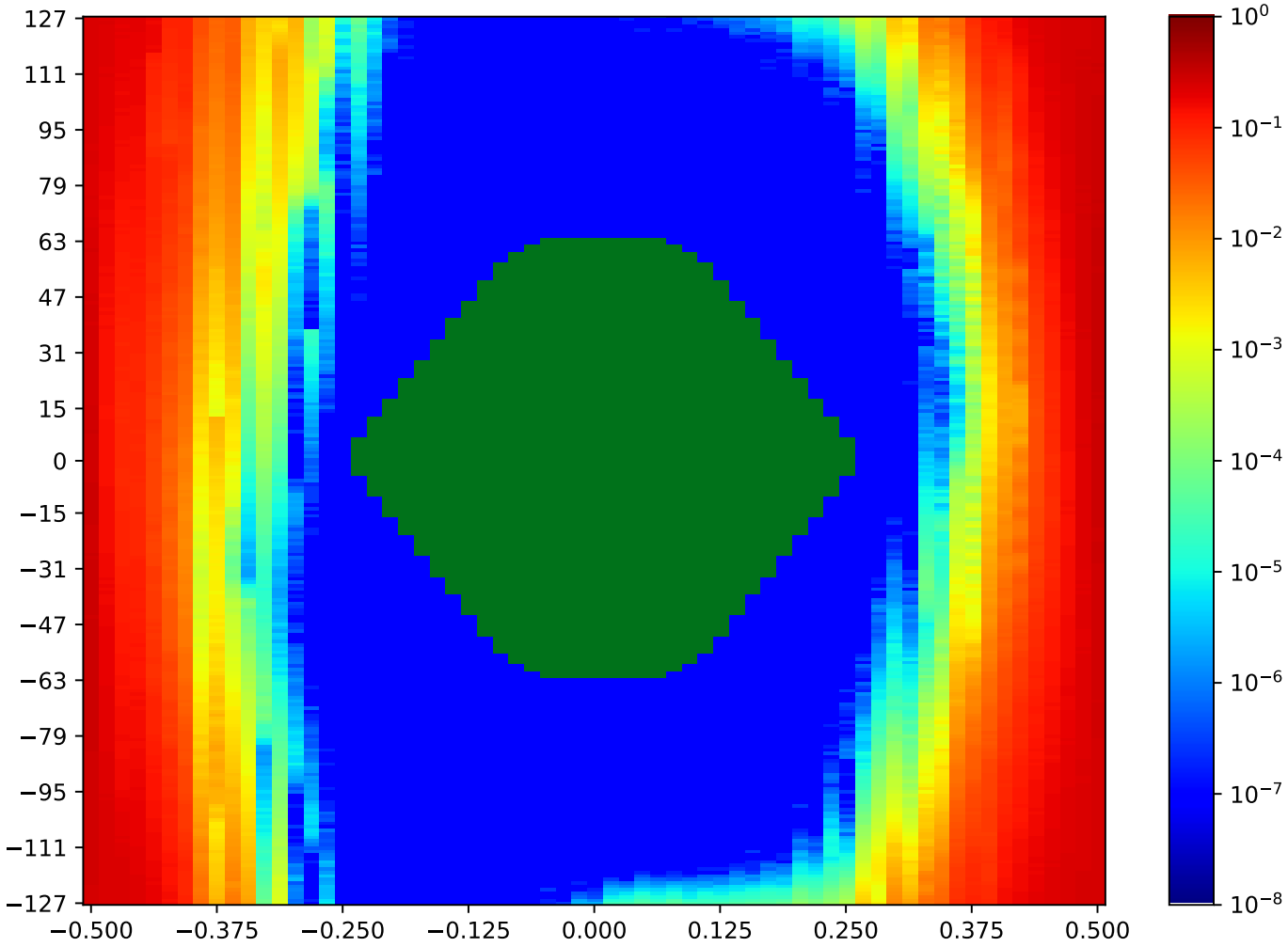


Figure 6.169: MSP_C_FPGA-TX4-02–RX9-02-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.4 MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Table 6.157: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:43:11		2019-Nov-27 10:43:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9347	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

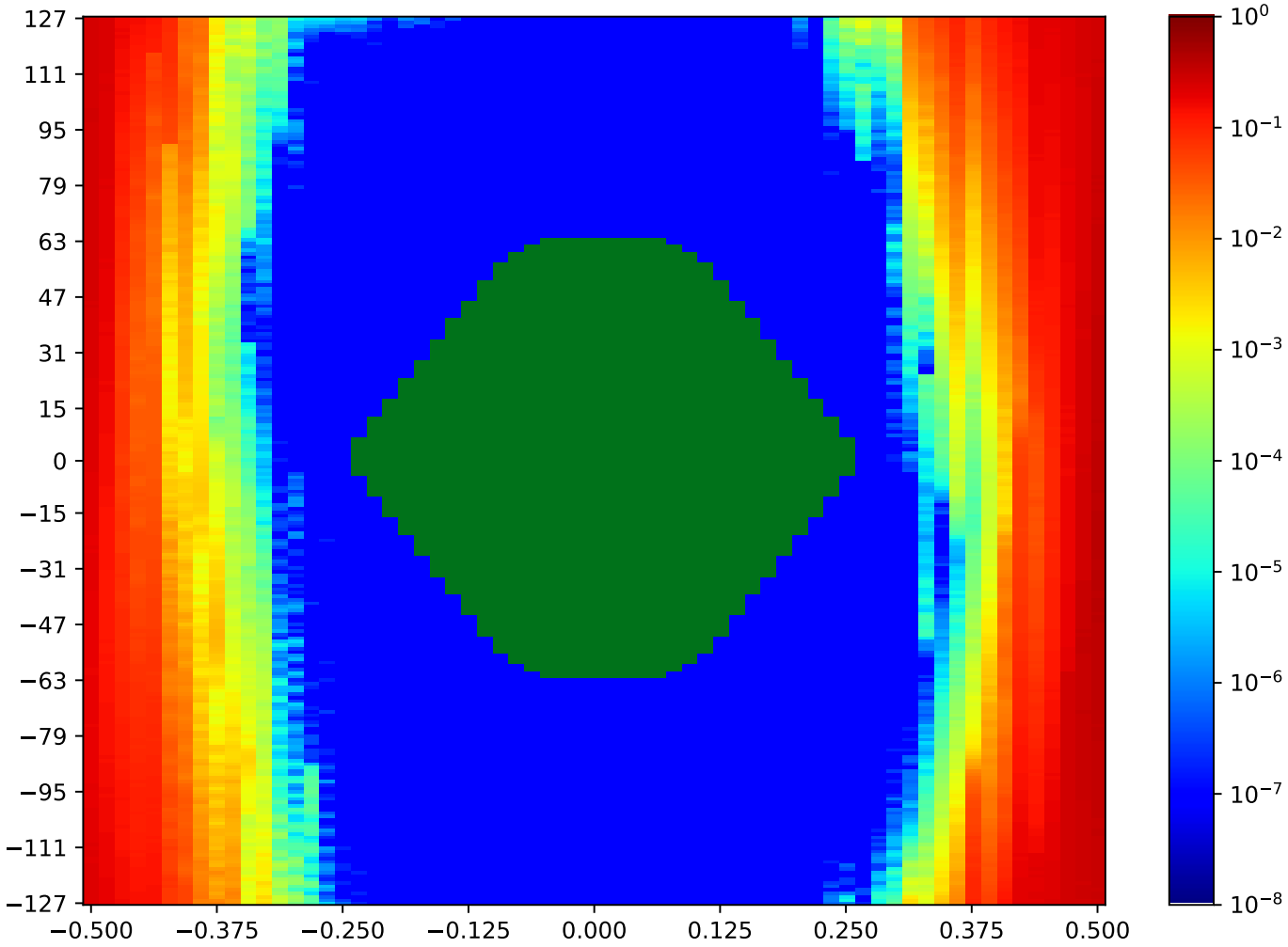


Figure 6.170: MSP_C_FPGA-TX4-03–RX9-03-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.5 MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Table 6.158: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:46:58		2019-Nov-27 10:47:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8491	39	60.00%	248	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

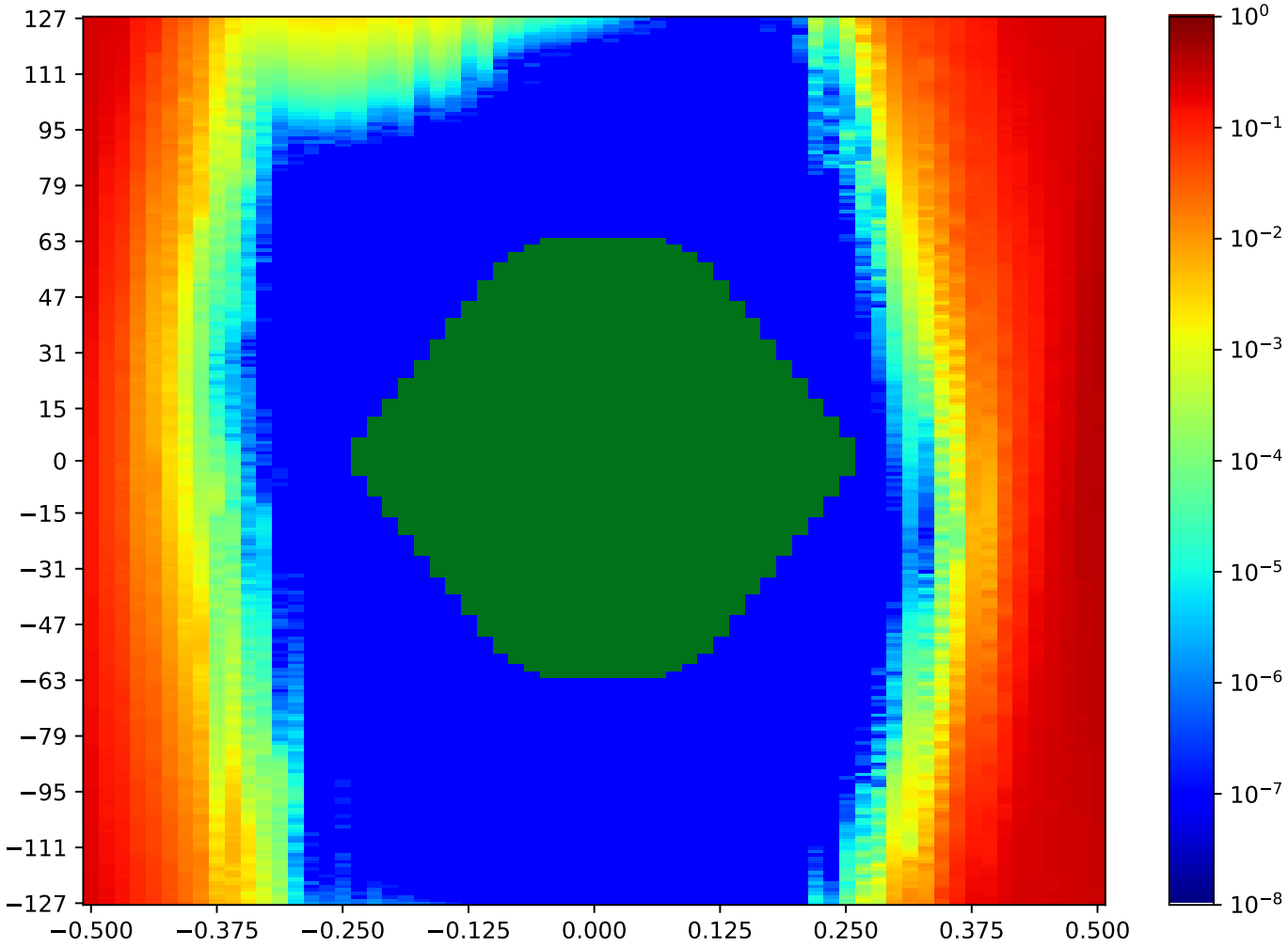


Figure 6.171: MSP_C_FPGA-TX4-04–RX9-04-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.6 MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Table 6.159: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:43:54		2019-Nov-27 10:44:22	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8664	40	61.54%	247	96.86%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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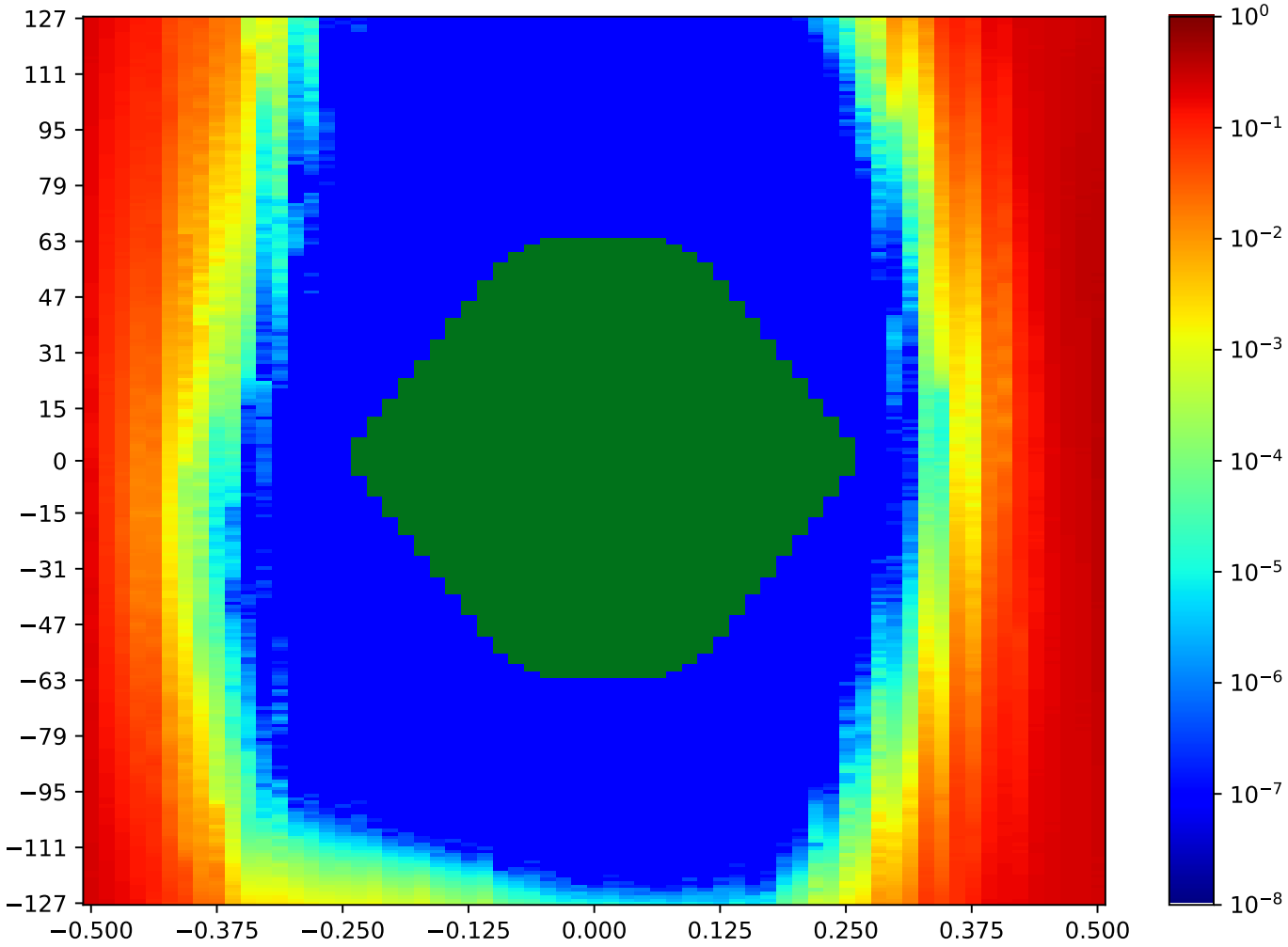


Figure 6.172: MSP_C_FPGA-TX4-05–RX9-05-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.7 MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Table 6.160: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:47:55		2019-Nov-27 10:48:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8122	41	63.08%	224	85.88%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

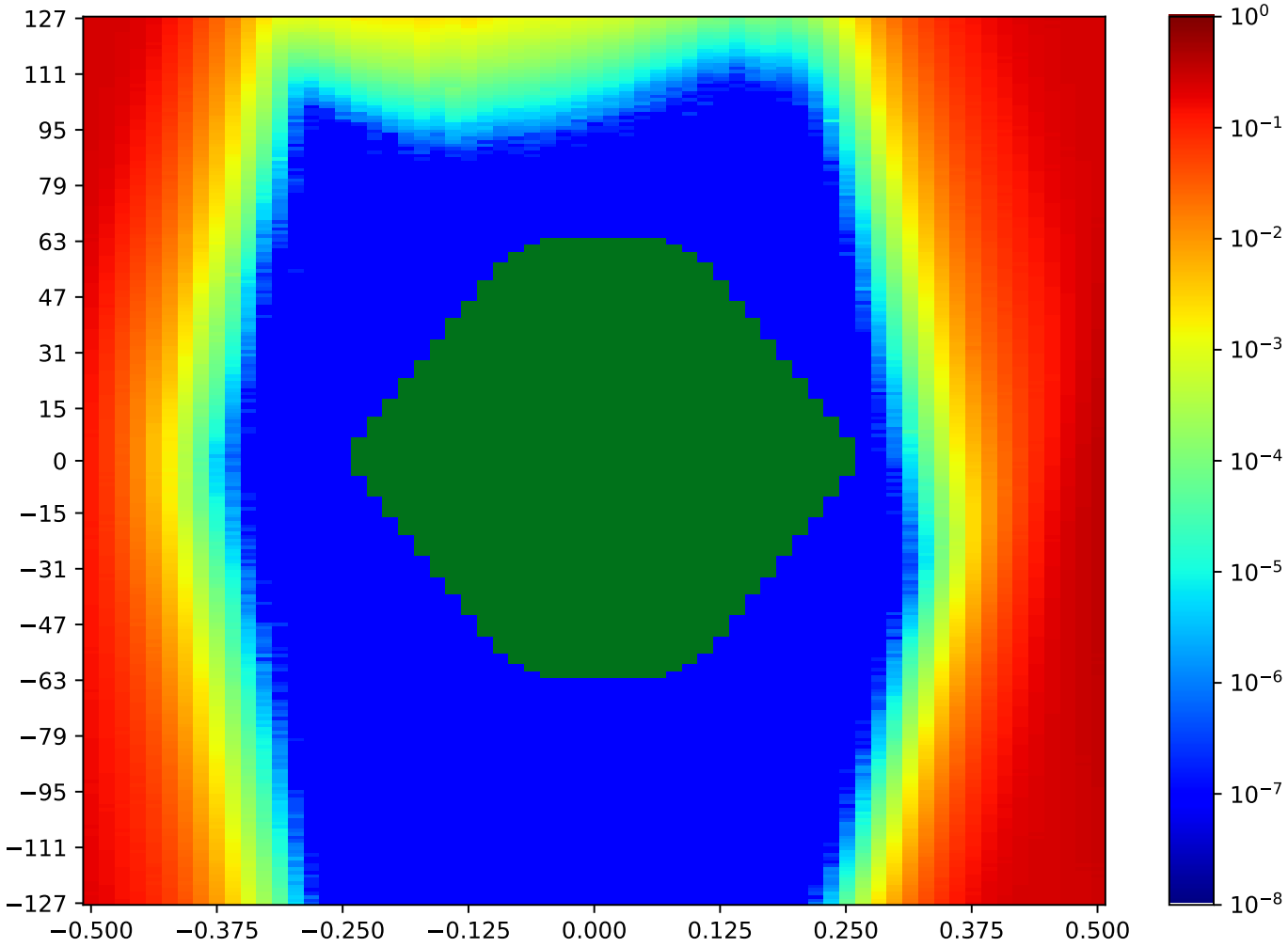


Figure 6.173: MSP_C_FPGA-TX4-06–RX9-06-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.8 MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Table 6.161: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:44:51		2019-Nov-27 10:45:20	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9449	44	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

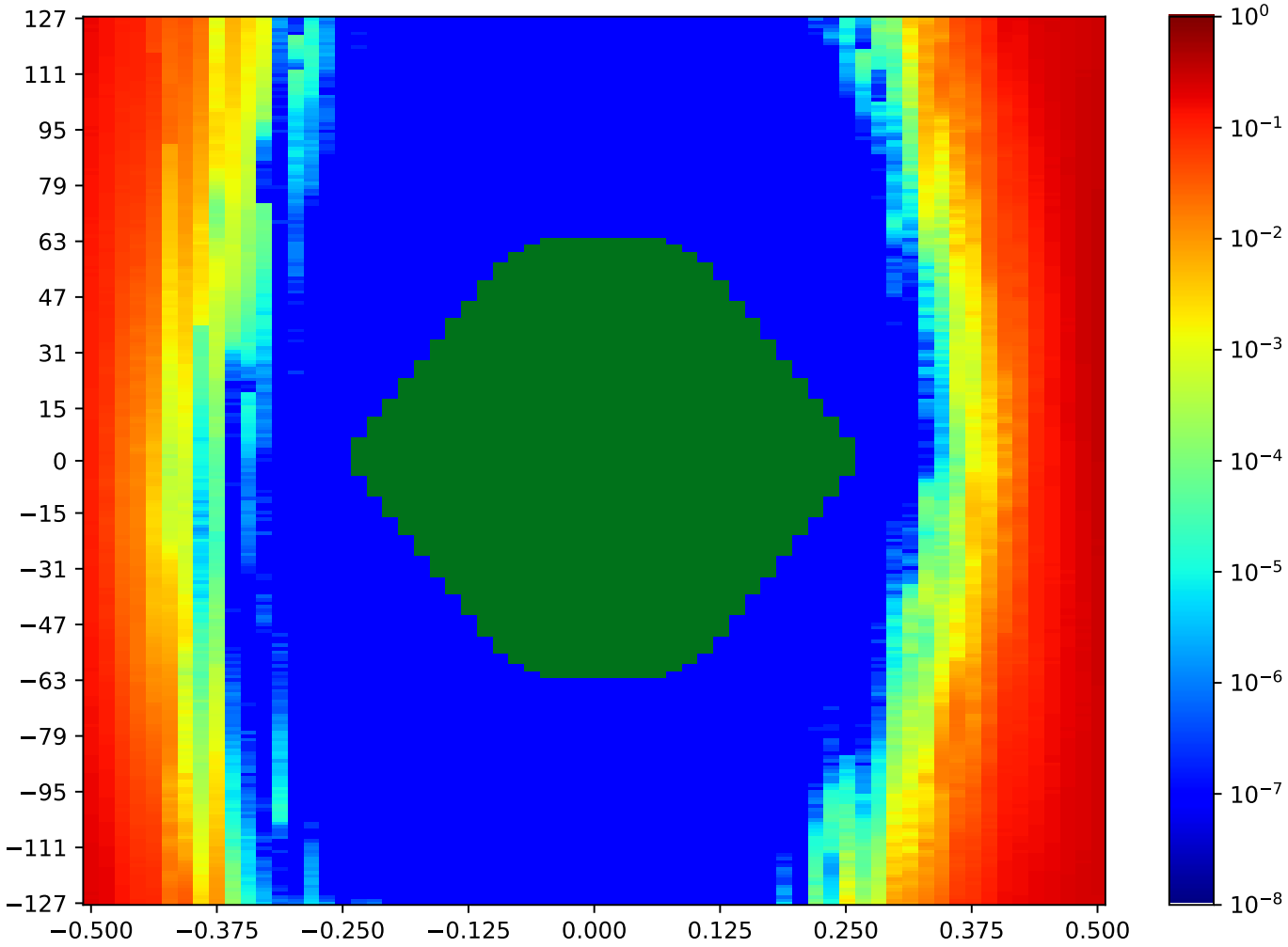


Figure 6.174: MSP_C_FPGA-TX4-07–RX9-07-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.9 MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Table 6.162: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:47:27		2019-Nov-27 10:47:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9393	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

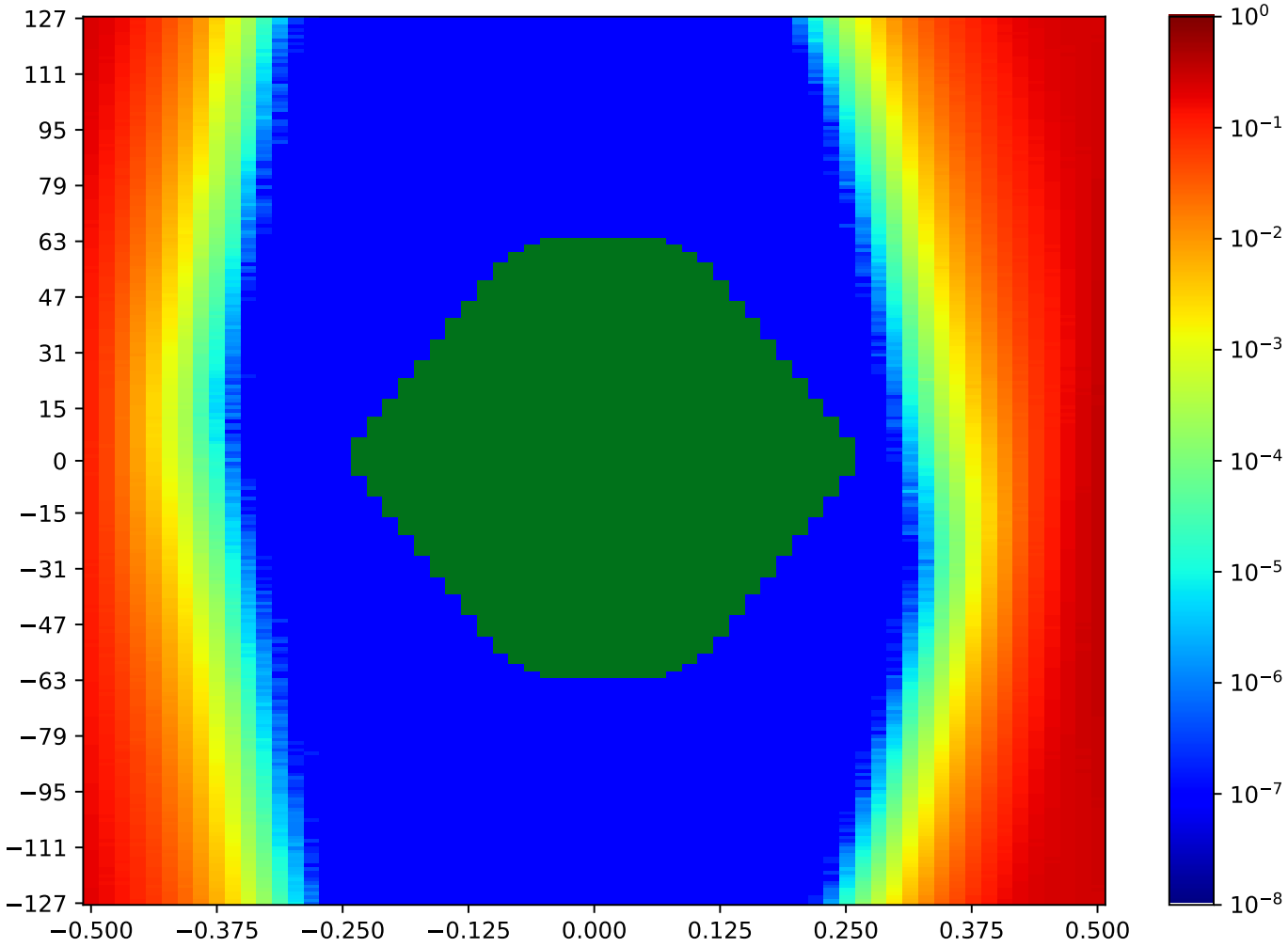


Figure 6.175: MSP_C_FPGA-TX4-08–RX9-08-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.10 MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Table 6.163: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:45:20		2019-Nov-27 10:45:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8678	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

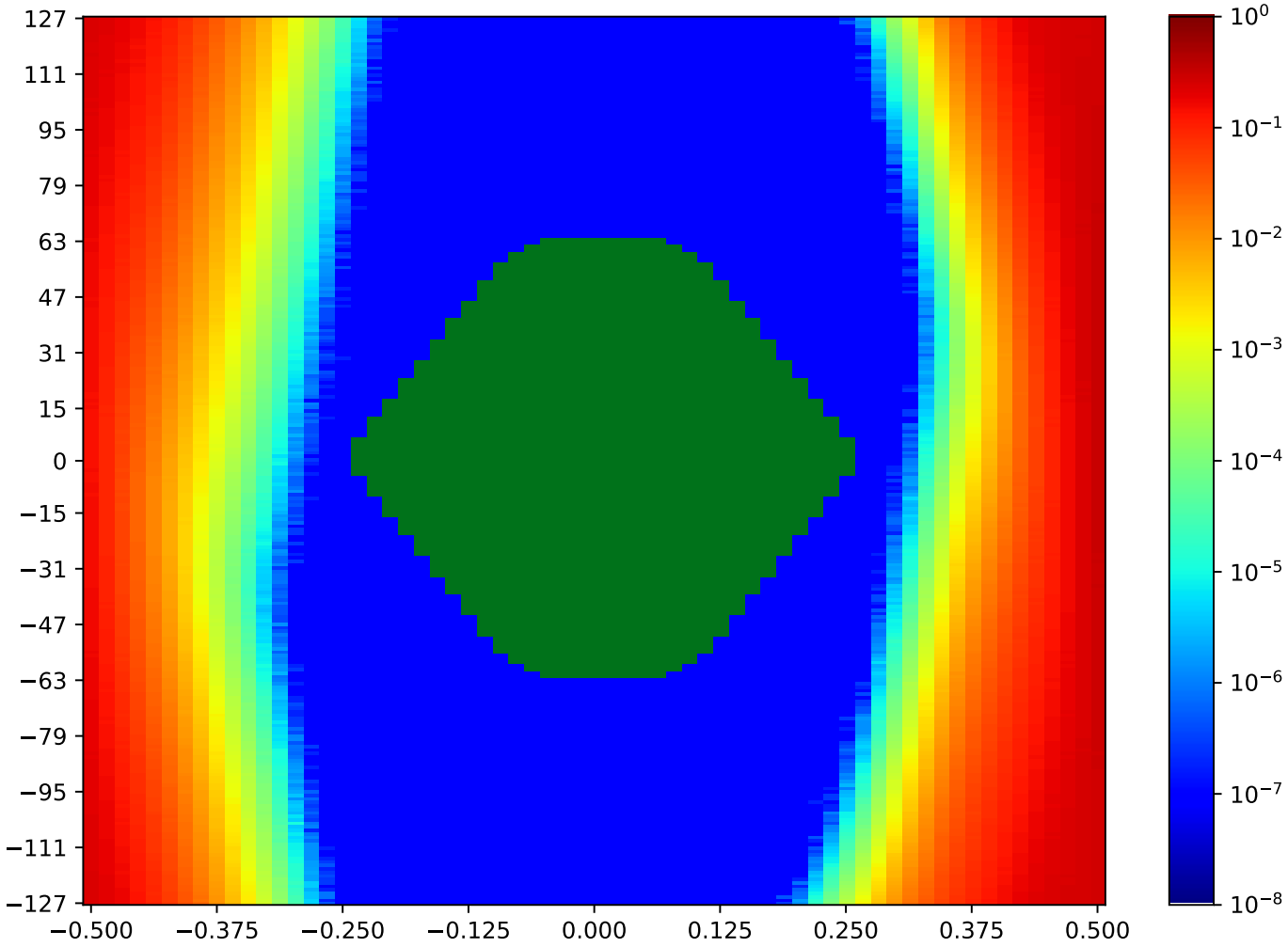


Figure 6.176: MSP_C_FPGA-TX4-09–RX9-09-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.11 MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Table 6.164: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:46:31		2019-Nov-27 10:46:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8084	35	53.85%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

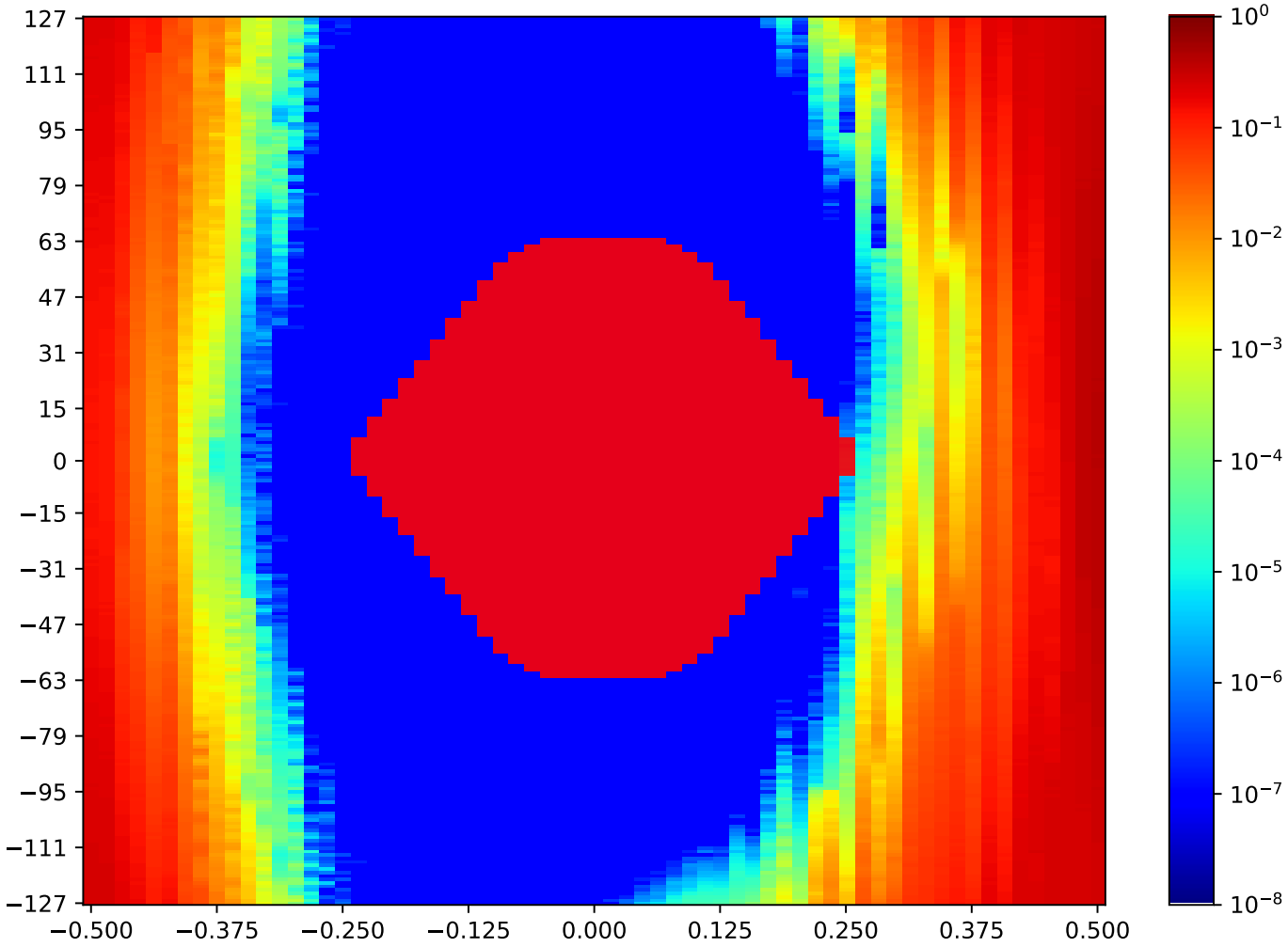


Figure 6.177: MSP_C_FPGA-TX4-10–RX9-10-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.13.12 MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Table 6.165: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:46:07		2019-Nov-27 10:46:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8975	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

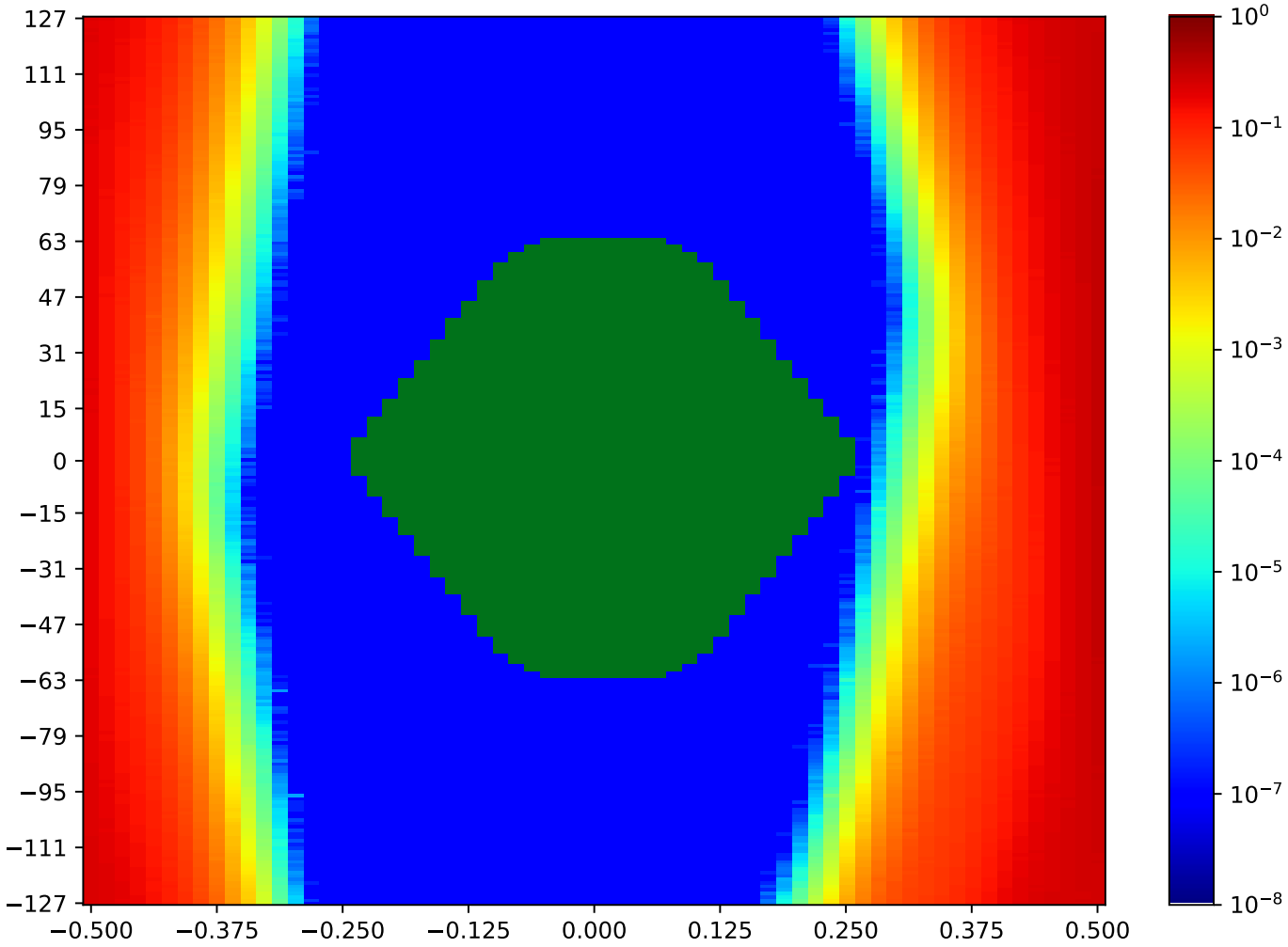


Figure 6.178: MSP_C_FPGA-TX4-11–RX9-11-MSP_A_FPGA

Call back to summary Figure 6.166. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.188.

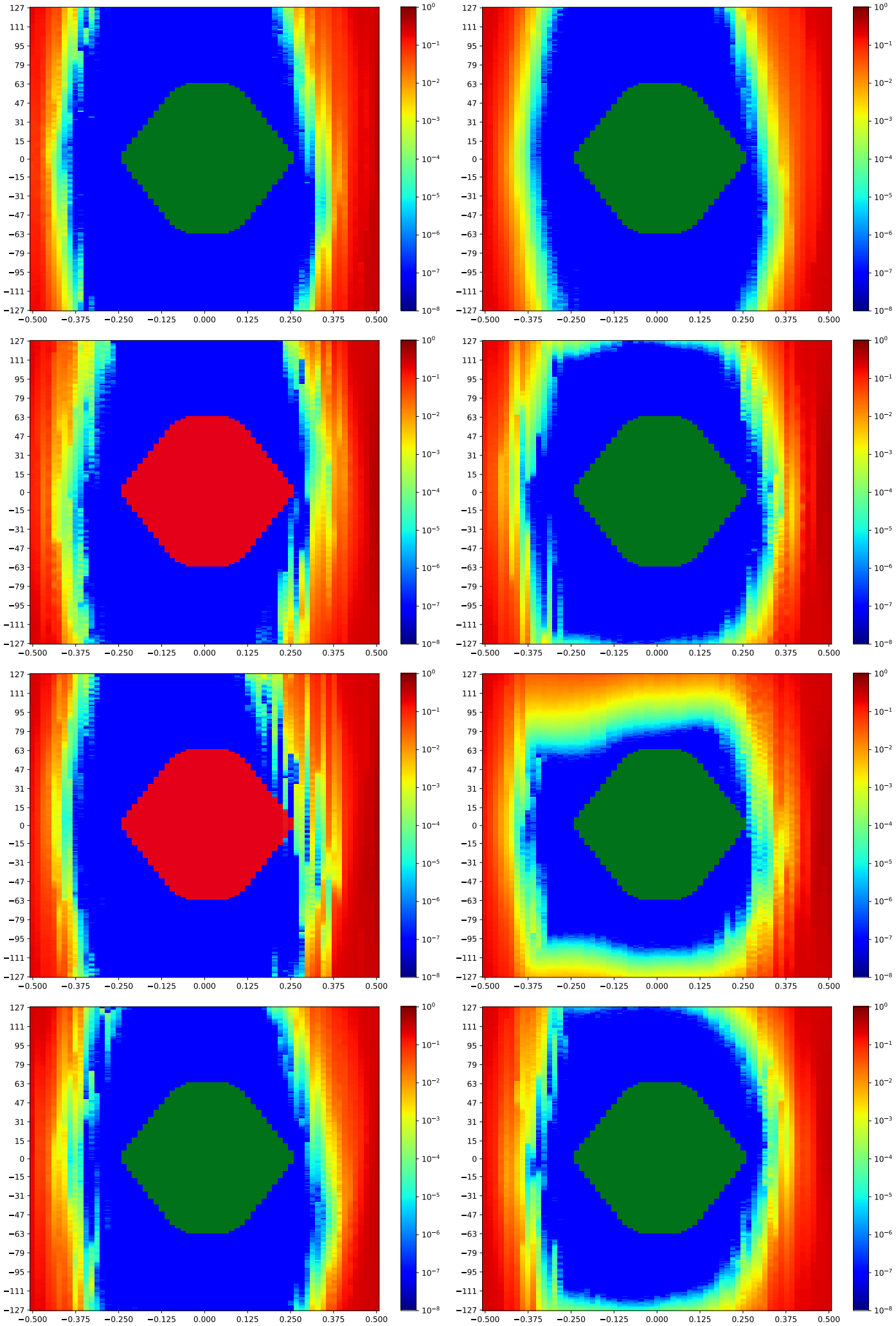


Figure 6.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback

6.14.1 TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Table 6.166: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:49:38		2019-Nov-27 10:50:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10084	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

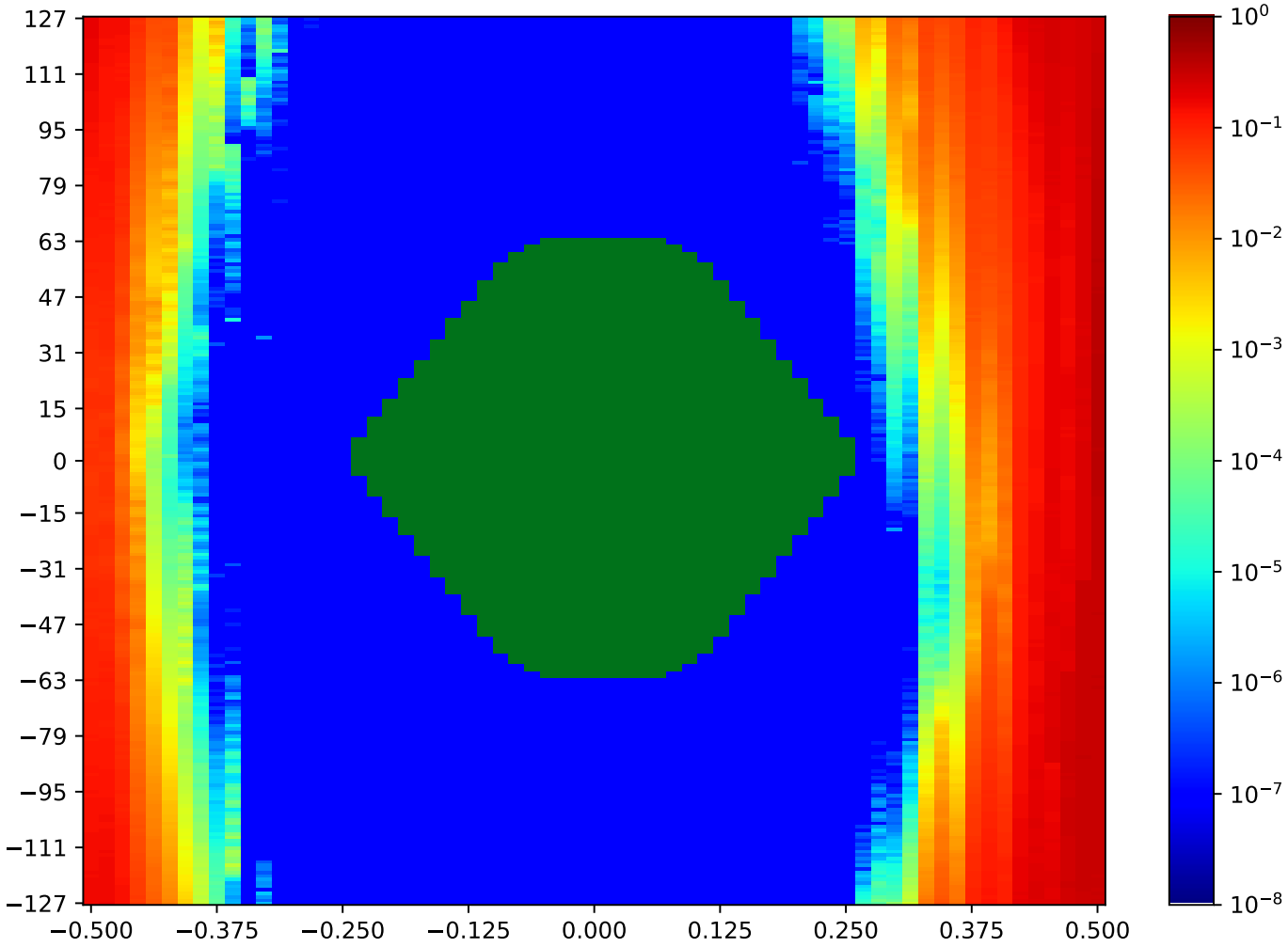


Figure 6.180: TRP_FPGA-TX5-00–RX14-00-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.2 TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Table 6.167: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:48:43		2019-Nov-27 10:49:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8963	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

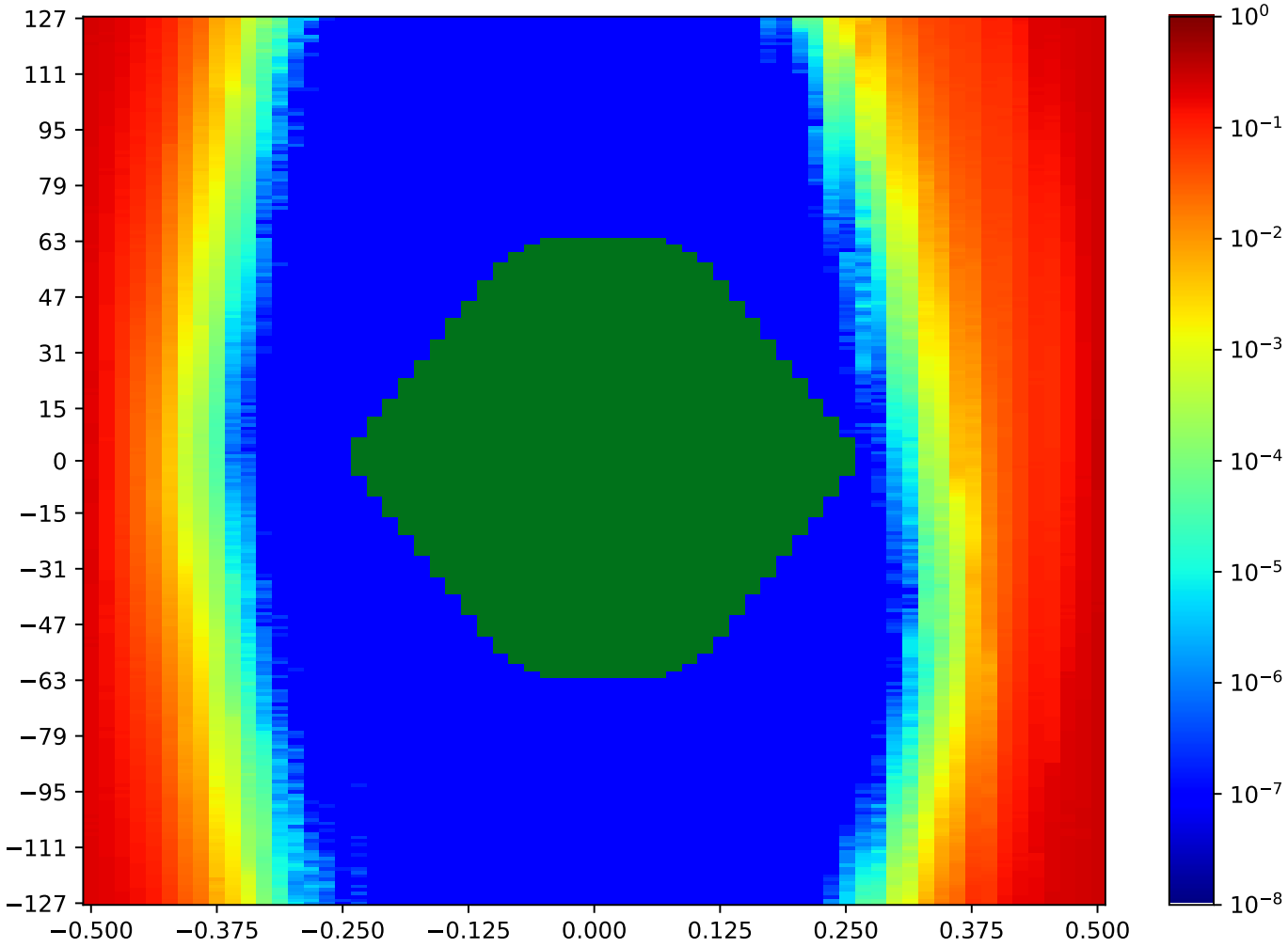


Figure 6.181: TRP_FPGA-TX5-01–RX14-01-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.3 TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Table 6.168: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:50:33		2019-Nov-27 10:51:00	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9042	41	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

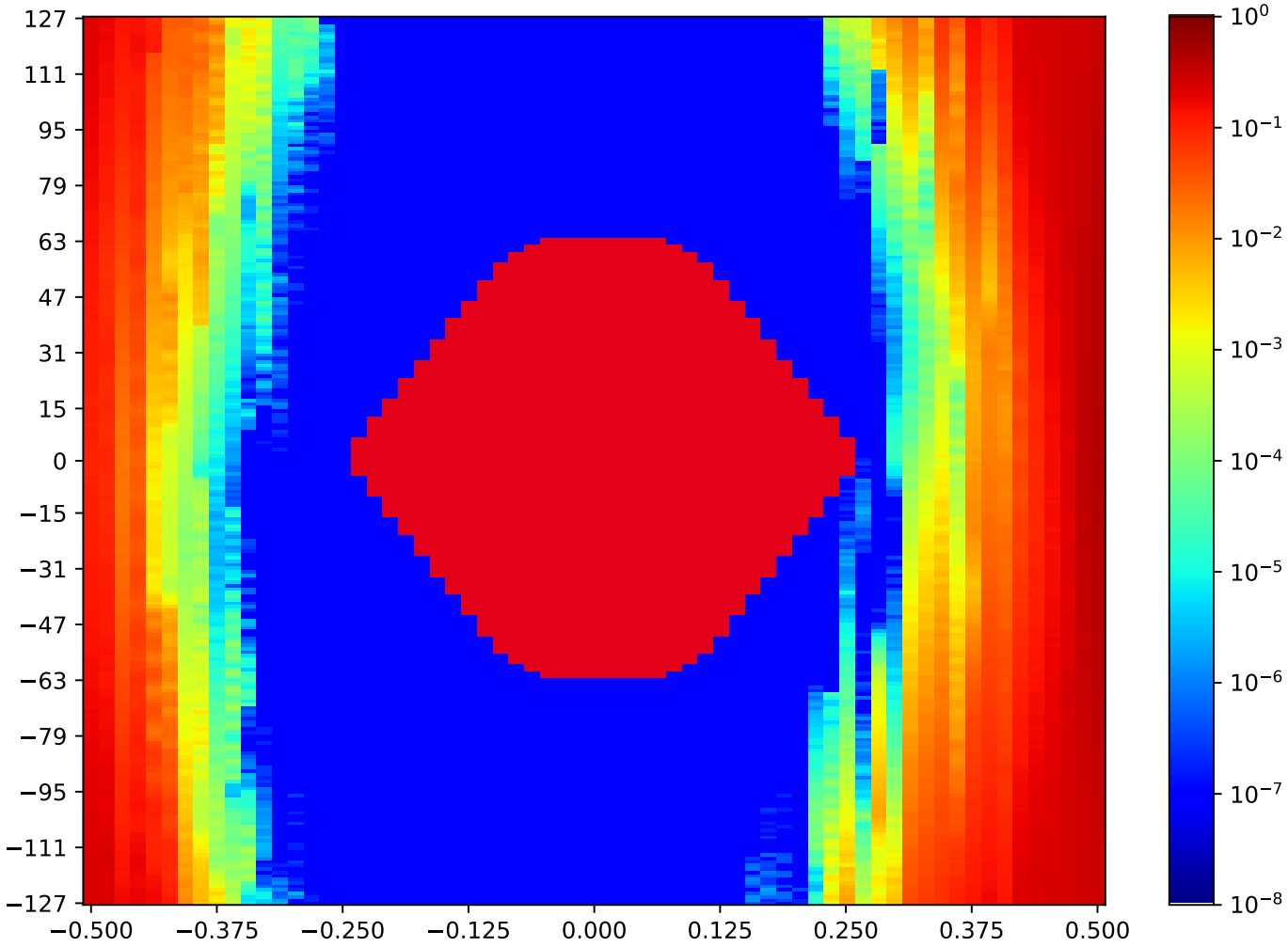


Figure 6.182: TRP_FPGA-TX5-02–RX14-02-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.4 TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Table 6.169: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:49:10		2019-Nov-27 10:49:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8512	42	63.08%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

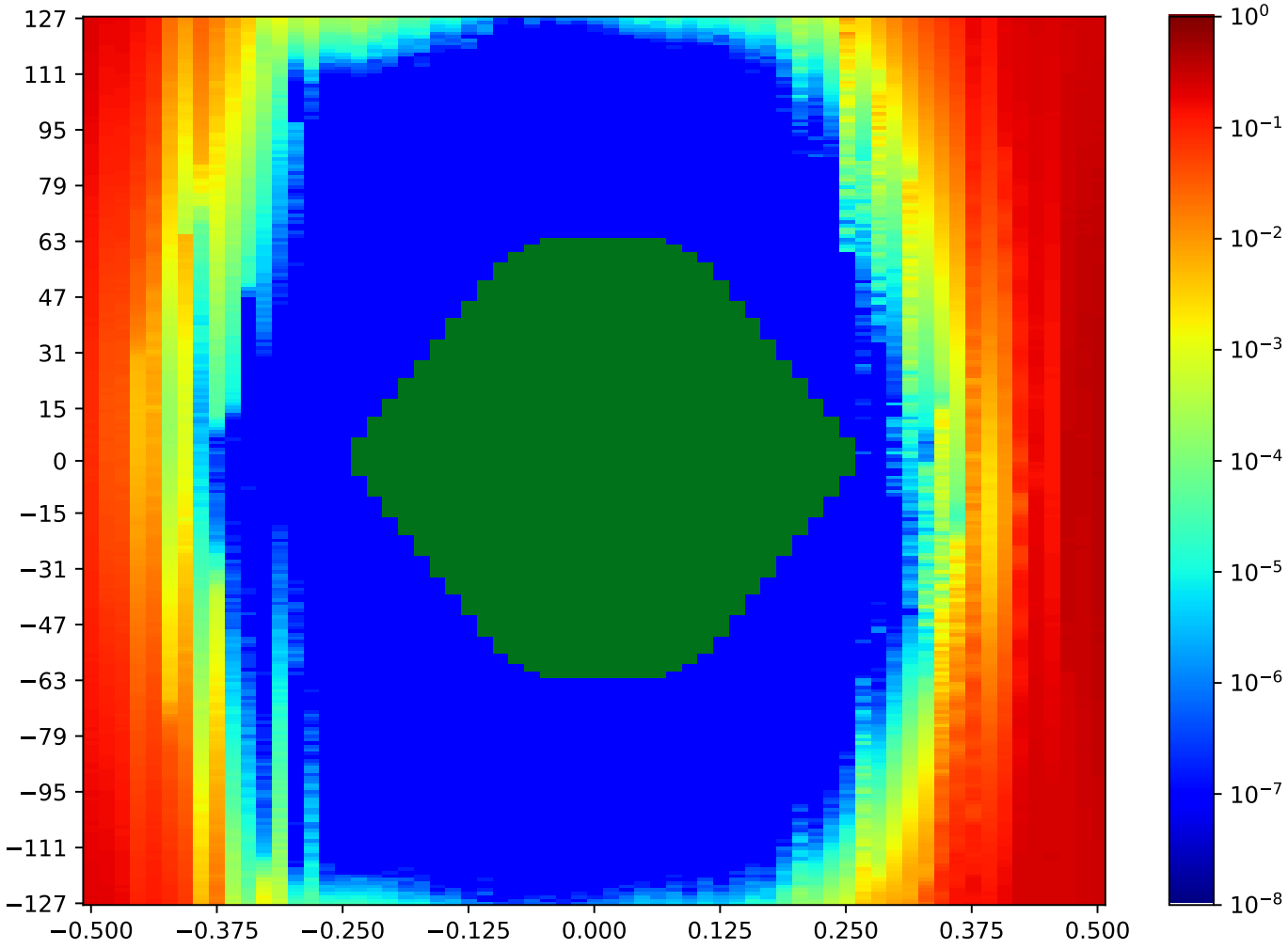


Figure 6.183: TRP_FPGA-TX5-03–RX14-03-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.5 TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Table 6.170: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:51:29		2019-Nov-27 10:51:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9103	40	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

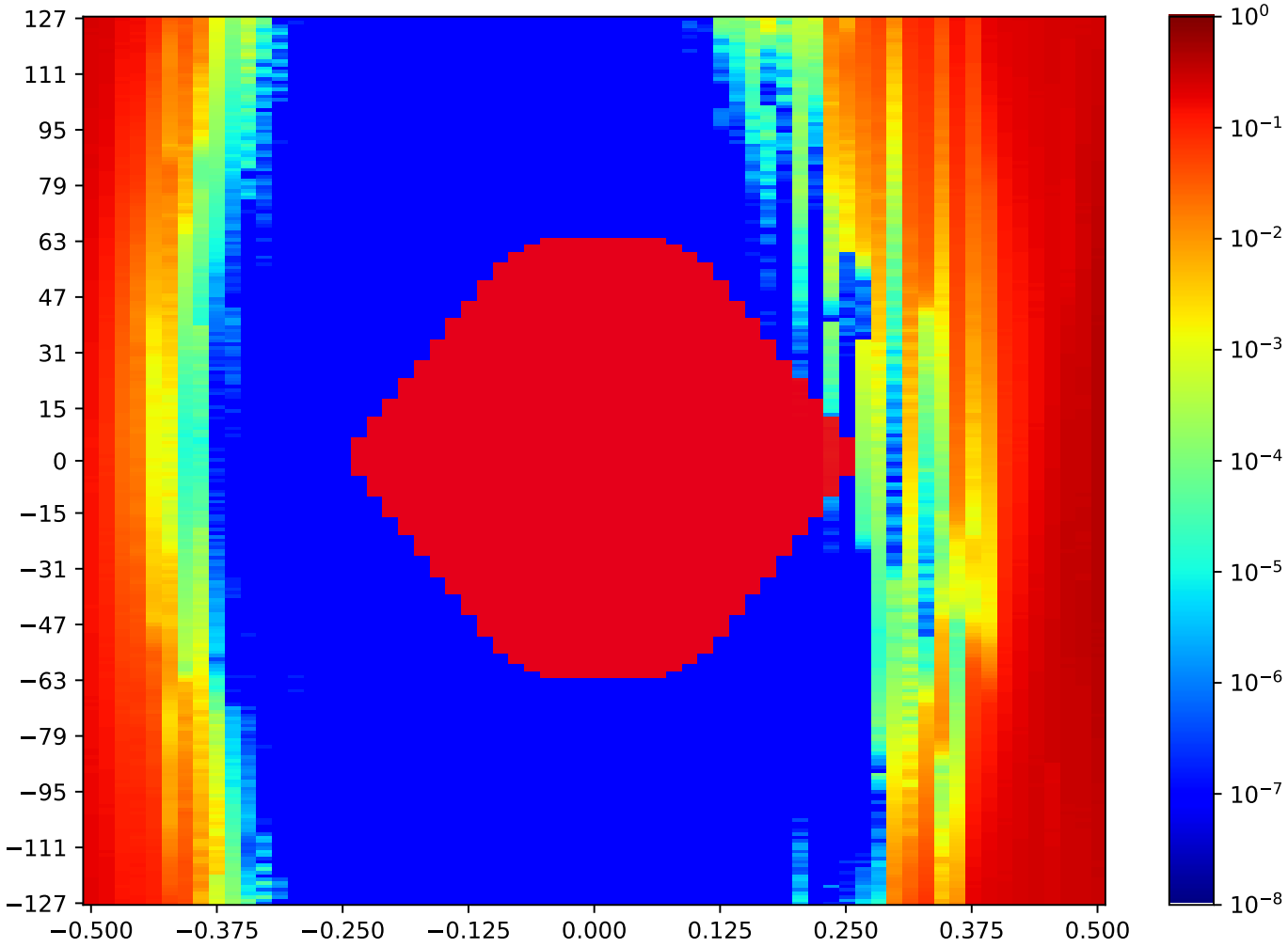


Figure 6.184: TRP_FPGA-TX5-04–RX14-04-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.6 TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Table 6.171: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:48:23		2019-Nov-27 10:48:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	5904	39	60.00%	171	67.06%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

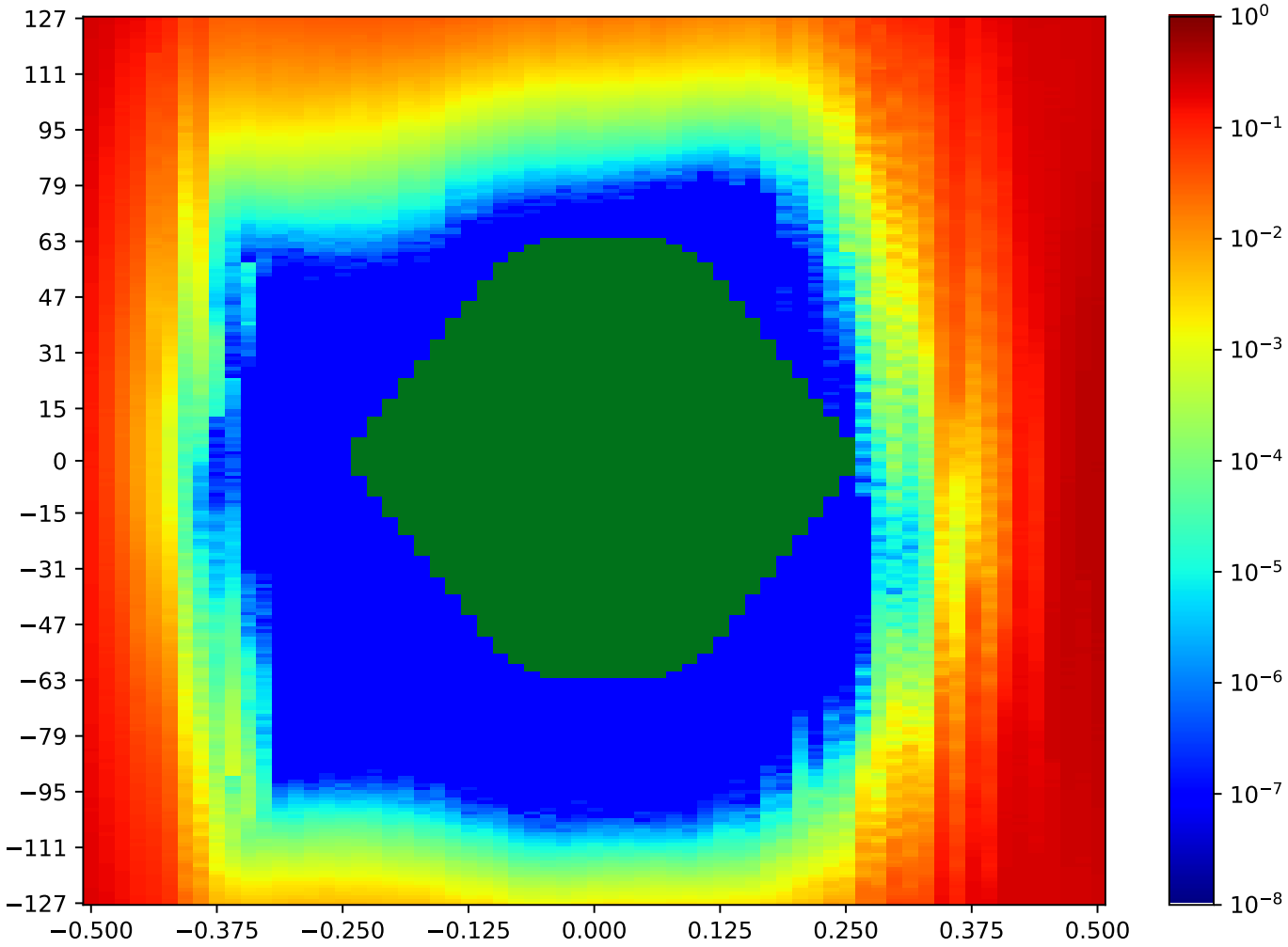


Figure 6.185: TRP_FPGA-TX5-05–RX14-05-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.7 TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Table 6.172: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:50:07		2019-Nov-27 10:50:33	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9167	41	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

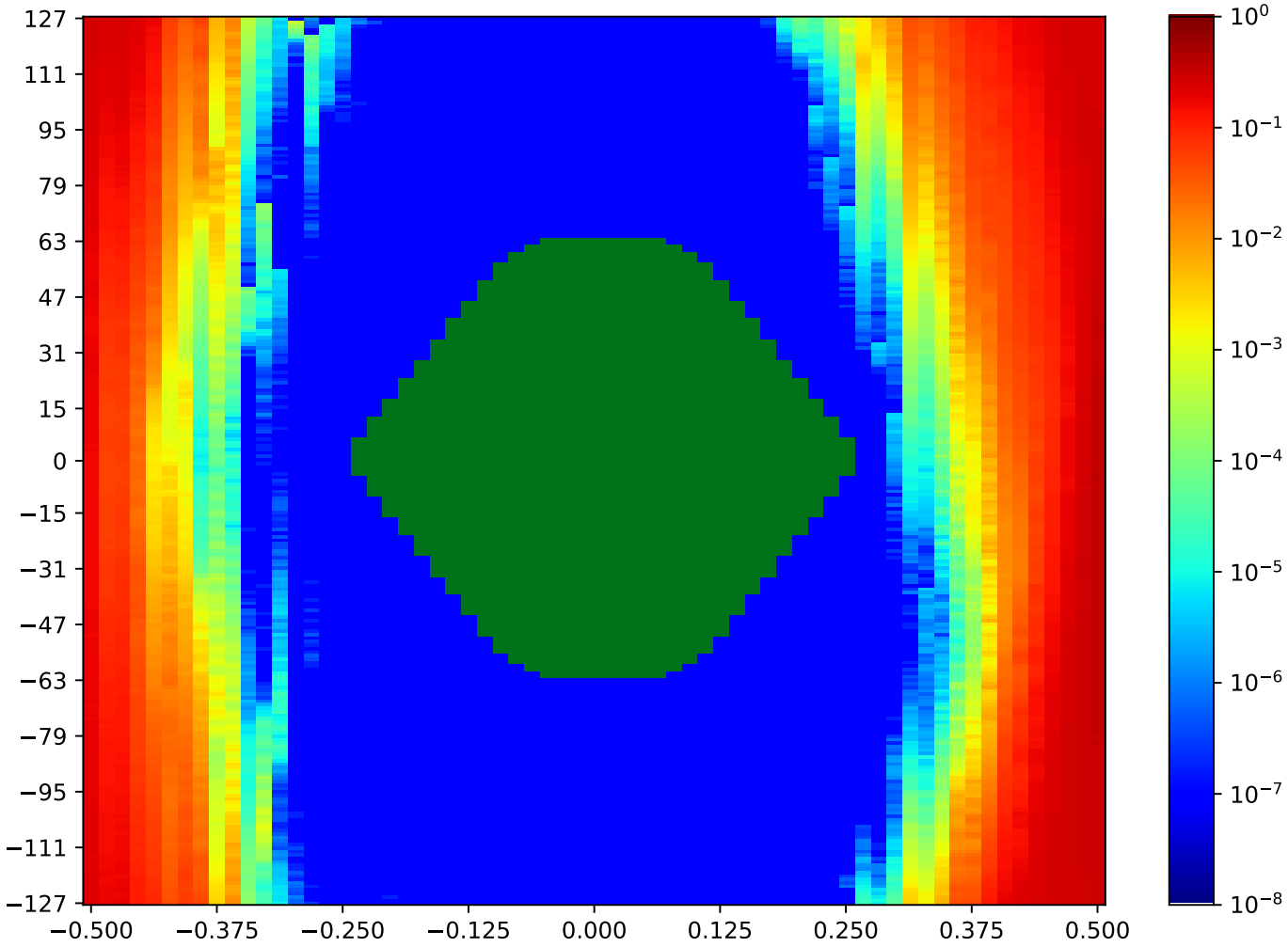


Figure 6.186: TRP_FPGA-TX5-06–RX14-06-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.14.8 TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Table 6.173: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:51:01		2019-Nov-27 10:51:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7817	41	61.54%	237	91.76%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

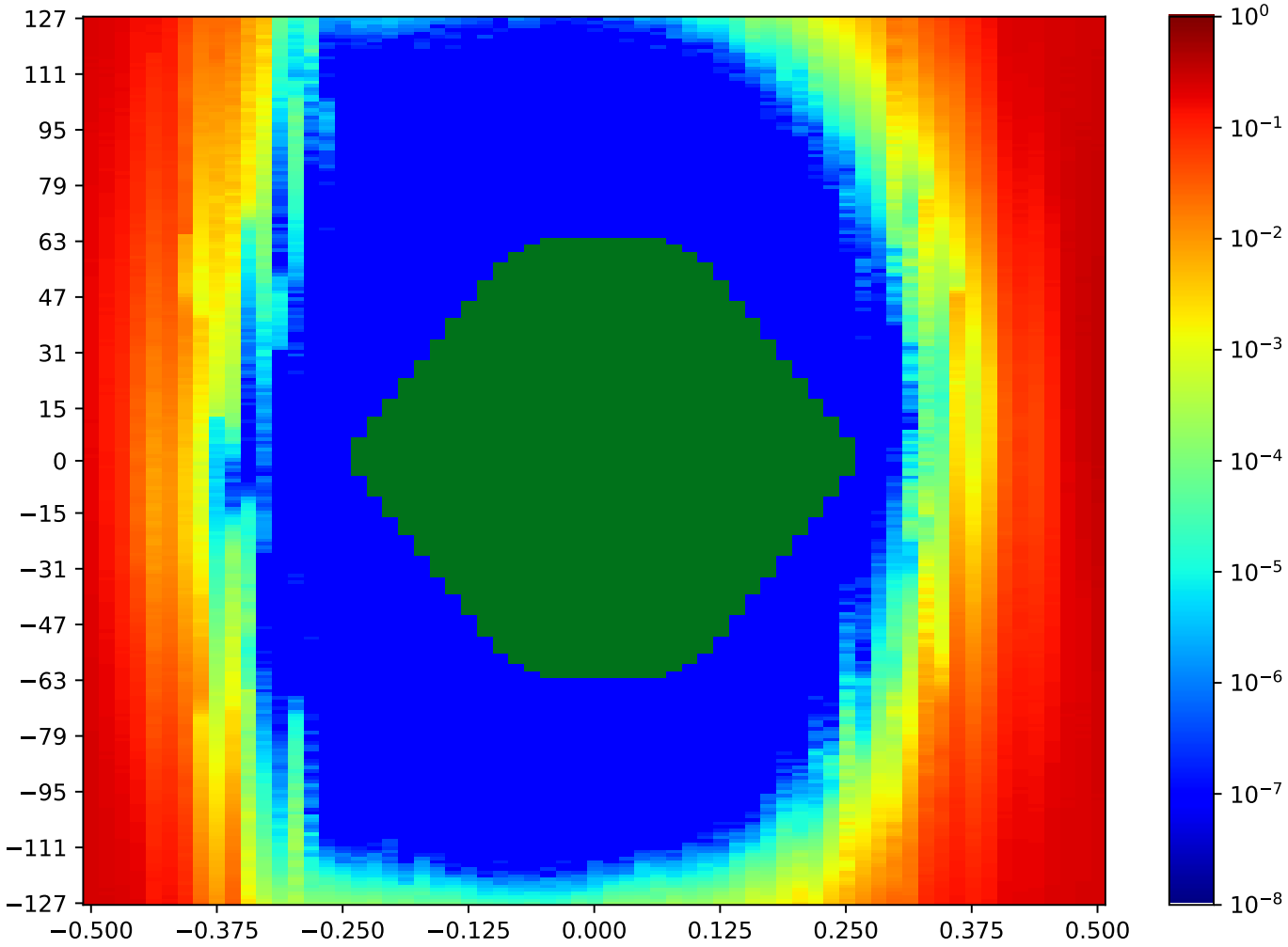


Figure 6.187: TRP_FPGA-TX5-07–RX14-07-MSP_C_FPGA

Call back to summary Figure 6.179. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15 MSP_A TX1 MSP_C RX10 Minipod Loopback

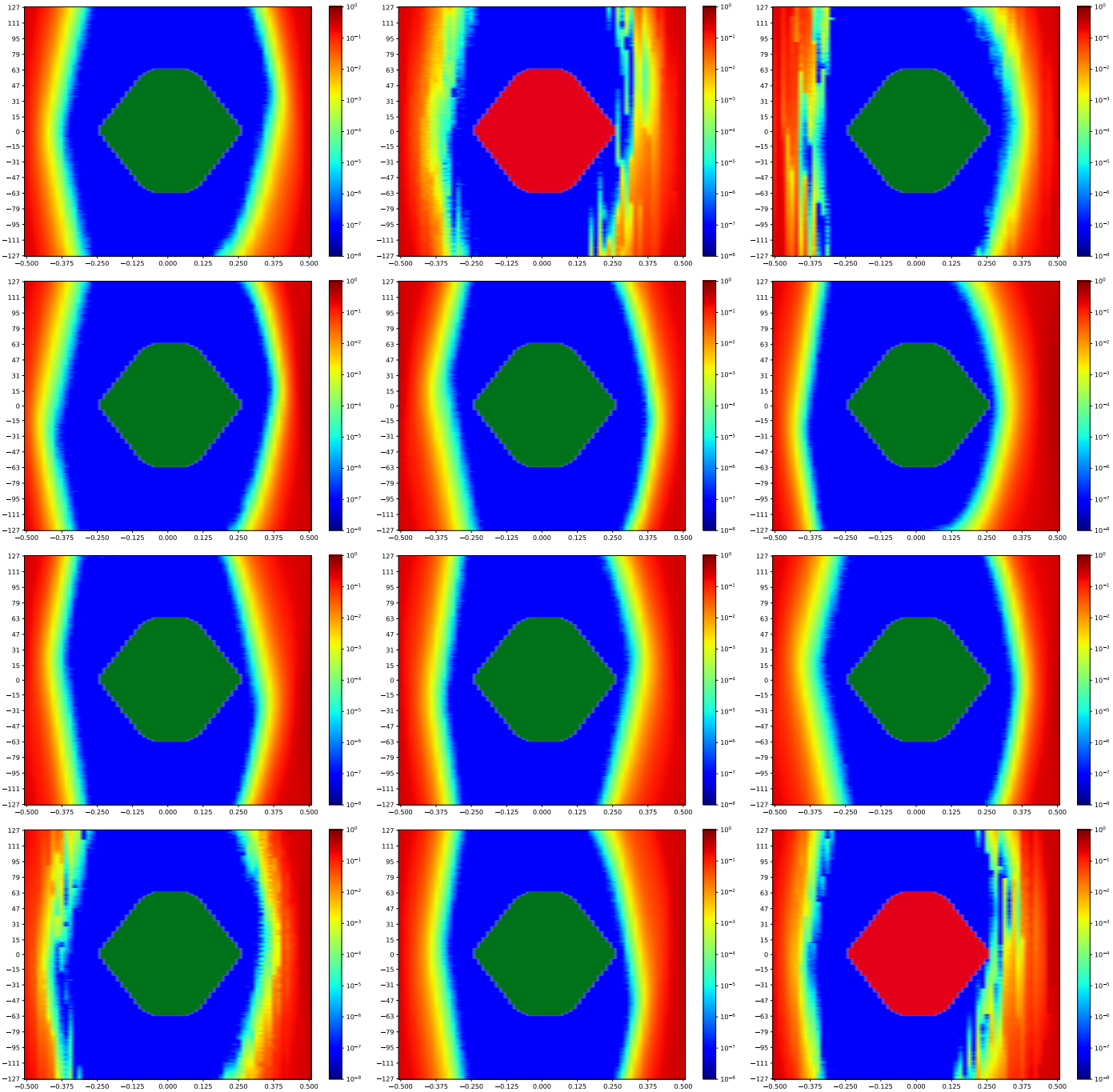


Figure 6.188: MSP_A TX1 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.201.

6.15.1 MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Table 6.174: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:59:23		2019-Nov-27 10:59:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9608	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

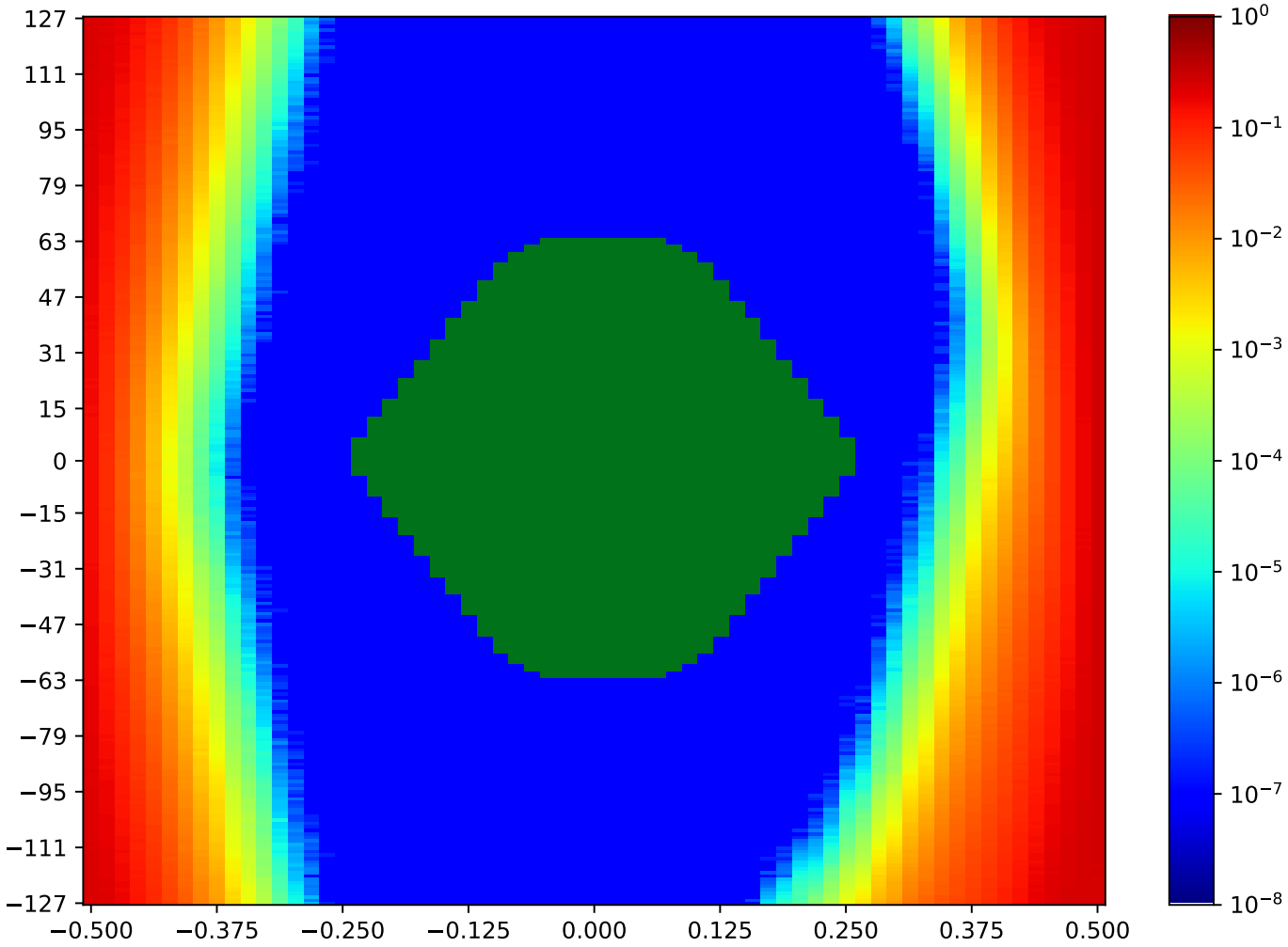


Figure 6.189: MSP_A_FPGA-TX1-00–RX10-00-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.2 MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Table 6.175: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:00:10		2019-Nov-27 11:00:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8483	39	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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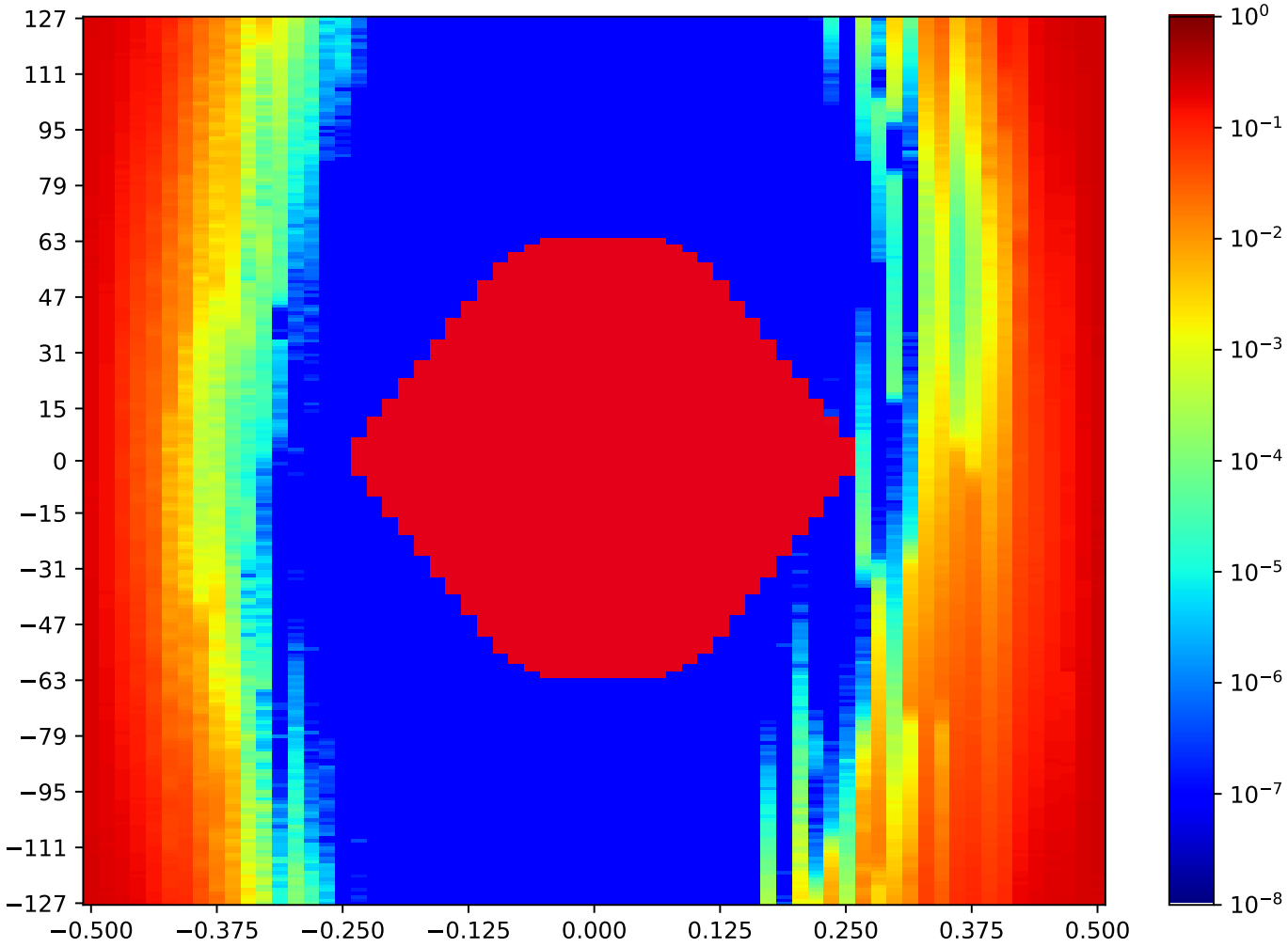


Figure 6.190: MSP_A_FPGA-TX1-01–RX10-01-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.3 MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Table 6.176: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:00:37		2019-Nov-27 11:01:05	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9333	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

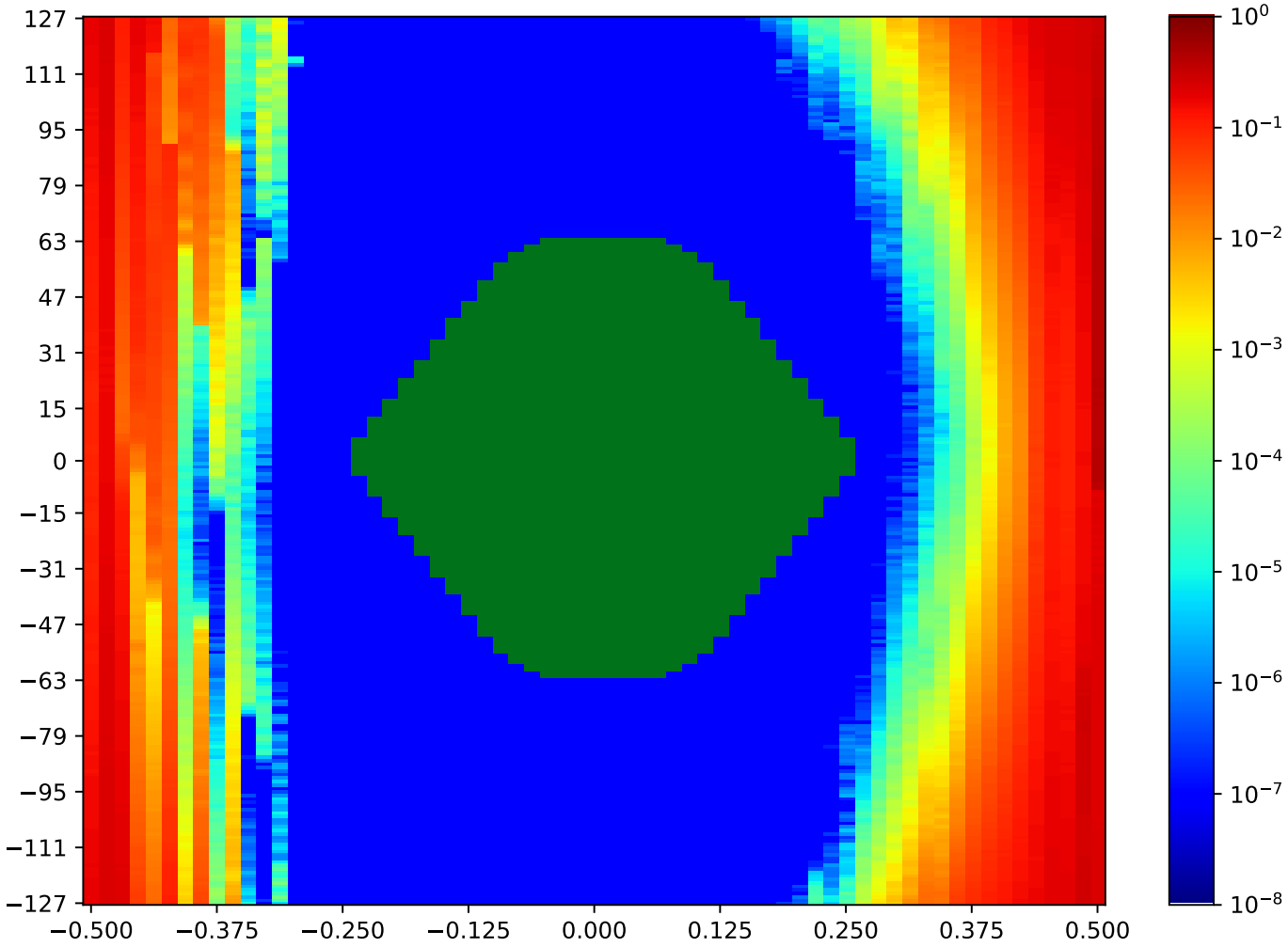


Figure 6.191: MSP_A_FPGA-TX1-02–RX10-02-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.4 MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Table 6.177: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:58:28		2019-Nov-27 10:58:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10238	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

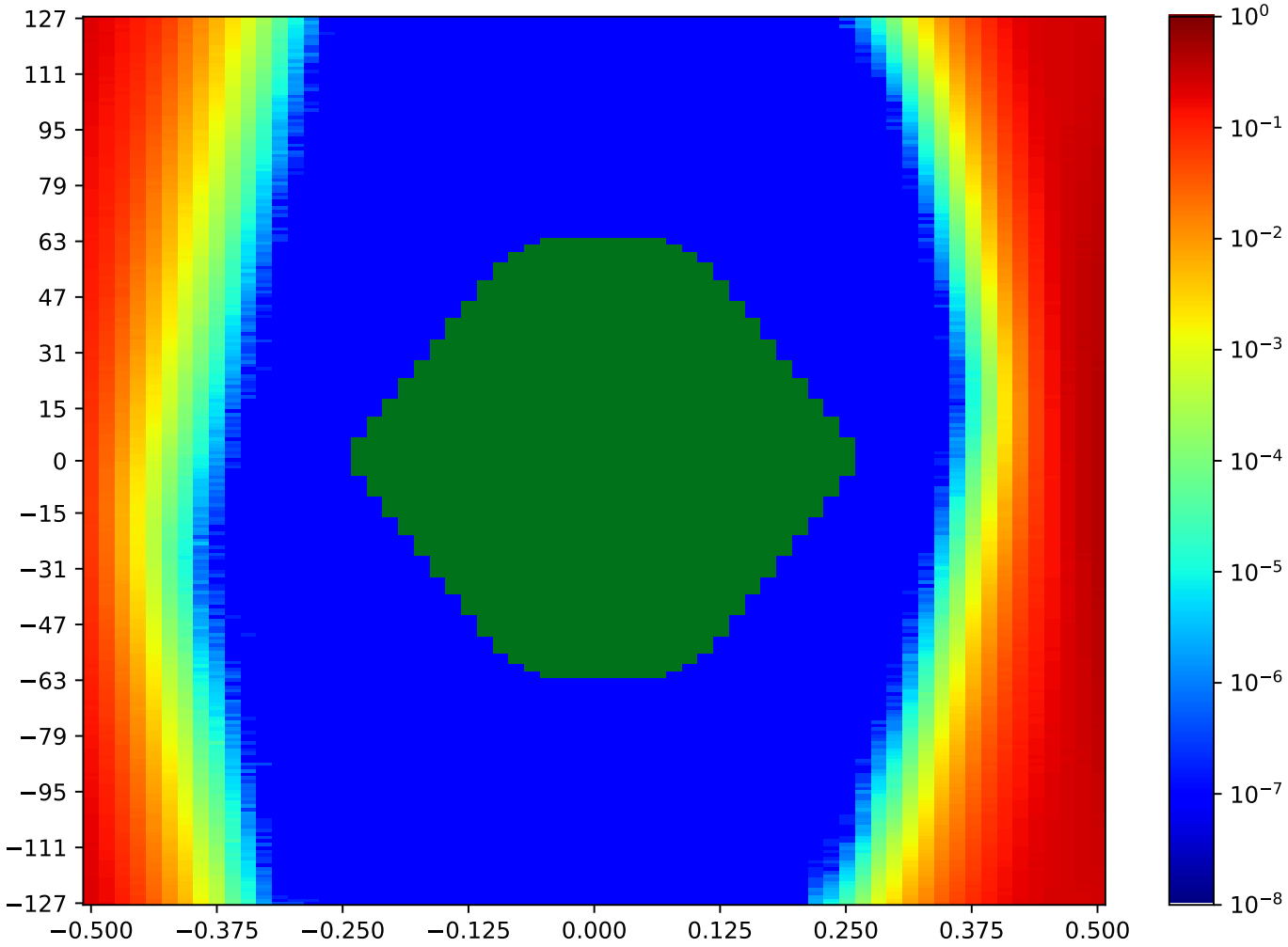


Figure 6.192: MSP_A_FPGA-TX1-03–RX10-03-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.5 MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Table 6.178: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:01:59		2019-Nov-27 11:02:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9450	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

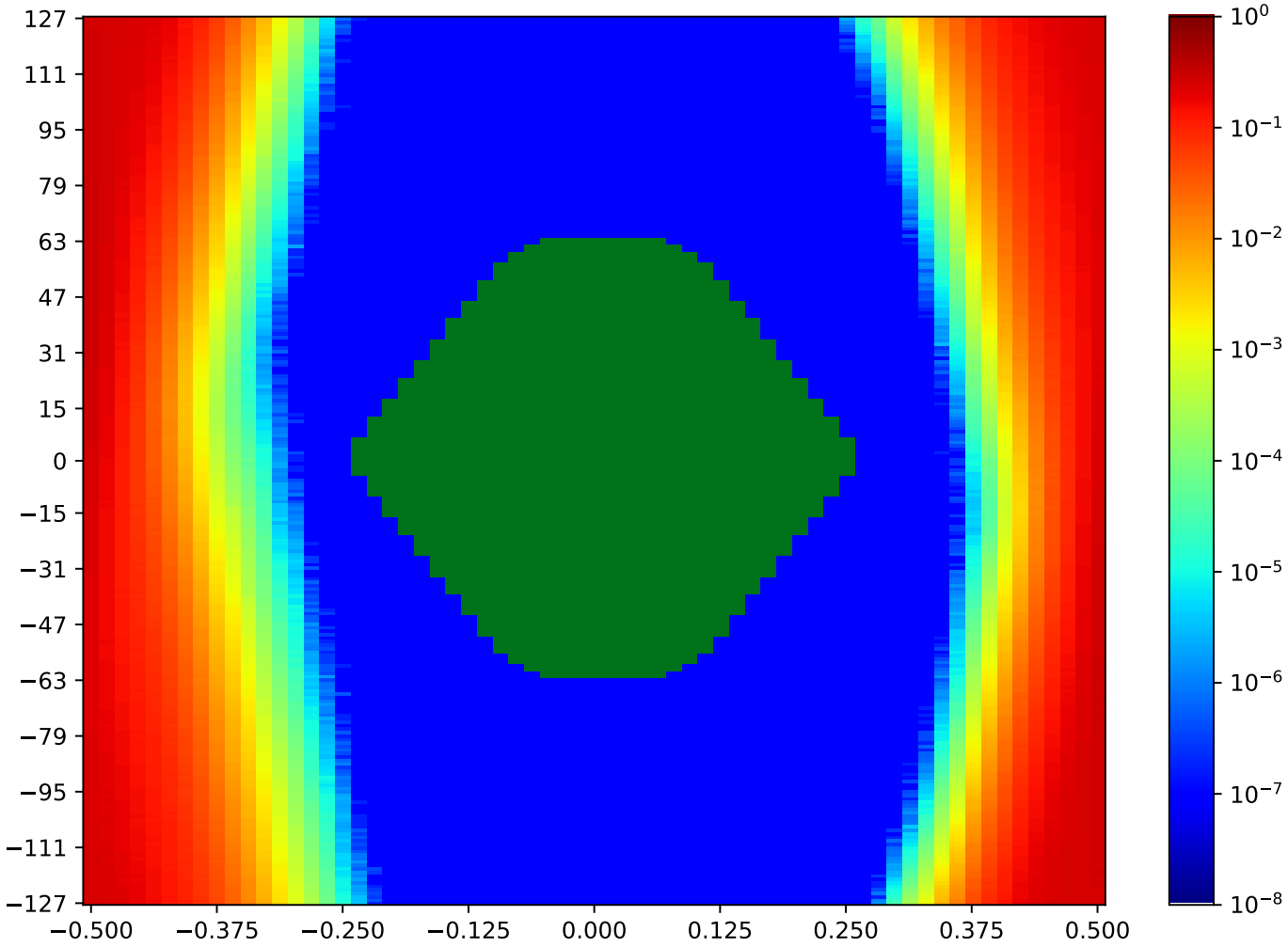


Figure 6.193: MSP_A_FPGA-TX1-04–RX10-04-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.6 MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Table 6.179: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:58:00		2019-Nov-27 10:58:28	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8873	40	61.54%	254	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

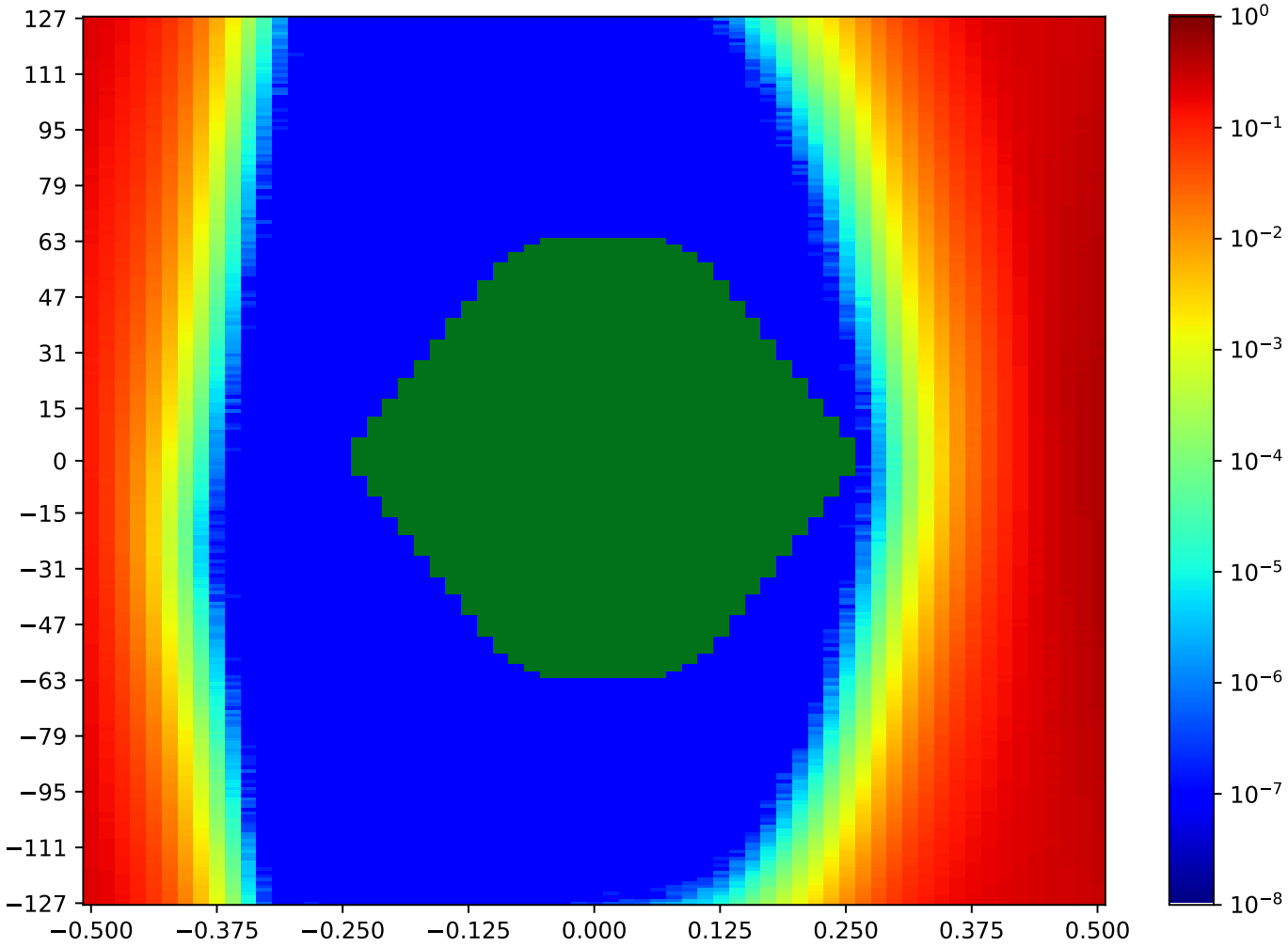


Figure 6.194: MSP_A_FPGA-TX1-05–RX10-05-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.7 MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Table 6.180: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:02:56		2019-Nov-27 11:03:24	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9182	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

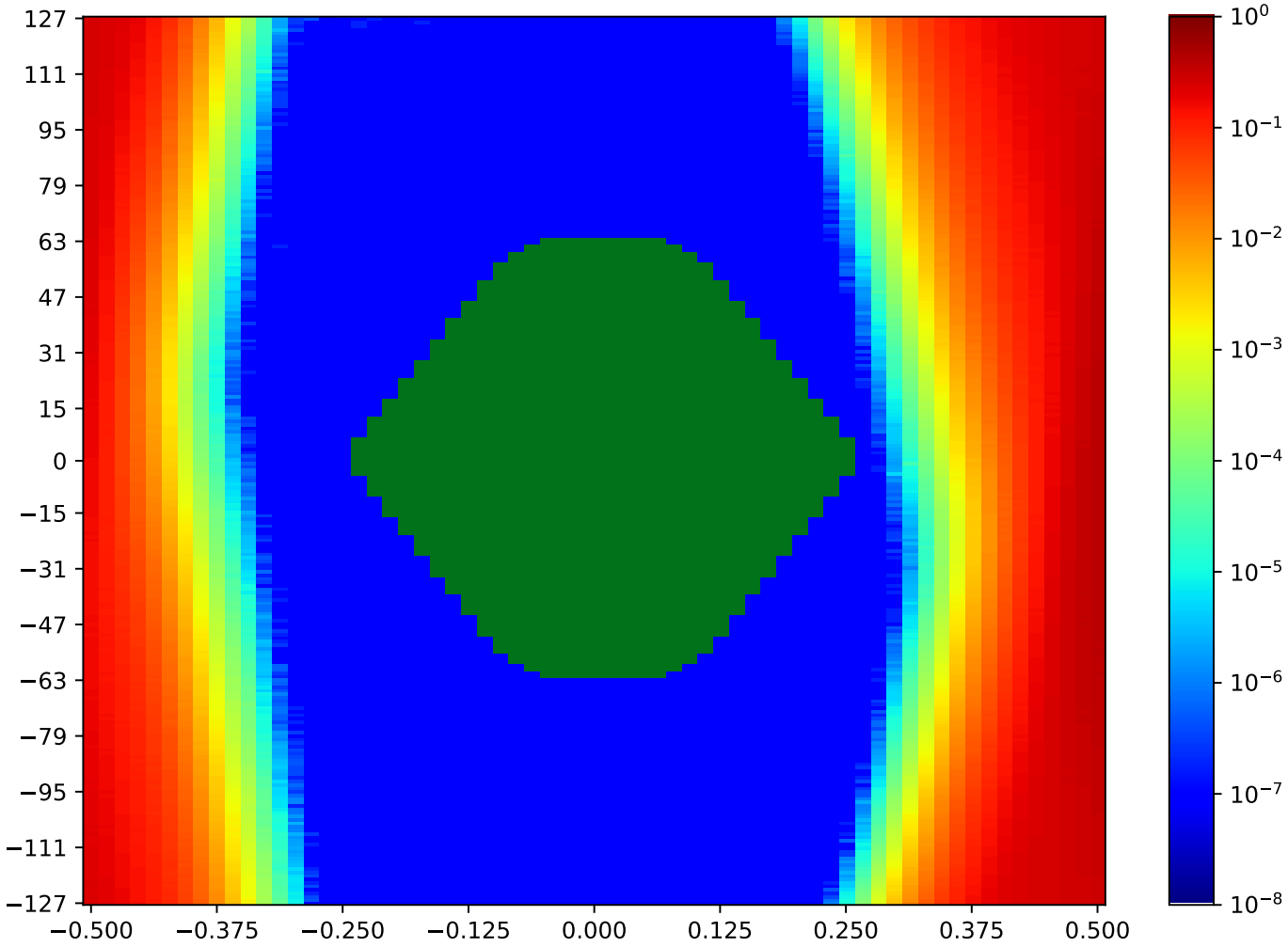


Figure 6.195: MSP_A_FPGA-TX1-06–RX10-06-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.8 MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Table 6.181: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:58:57		2019-Nov-27 10:59:23	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8815	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

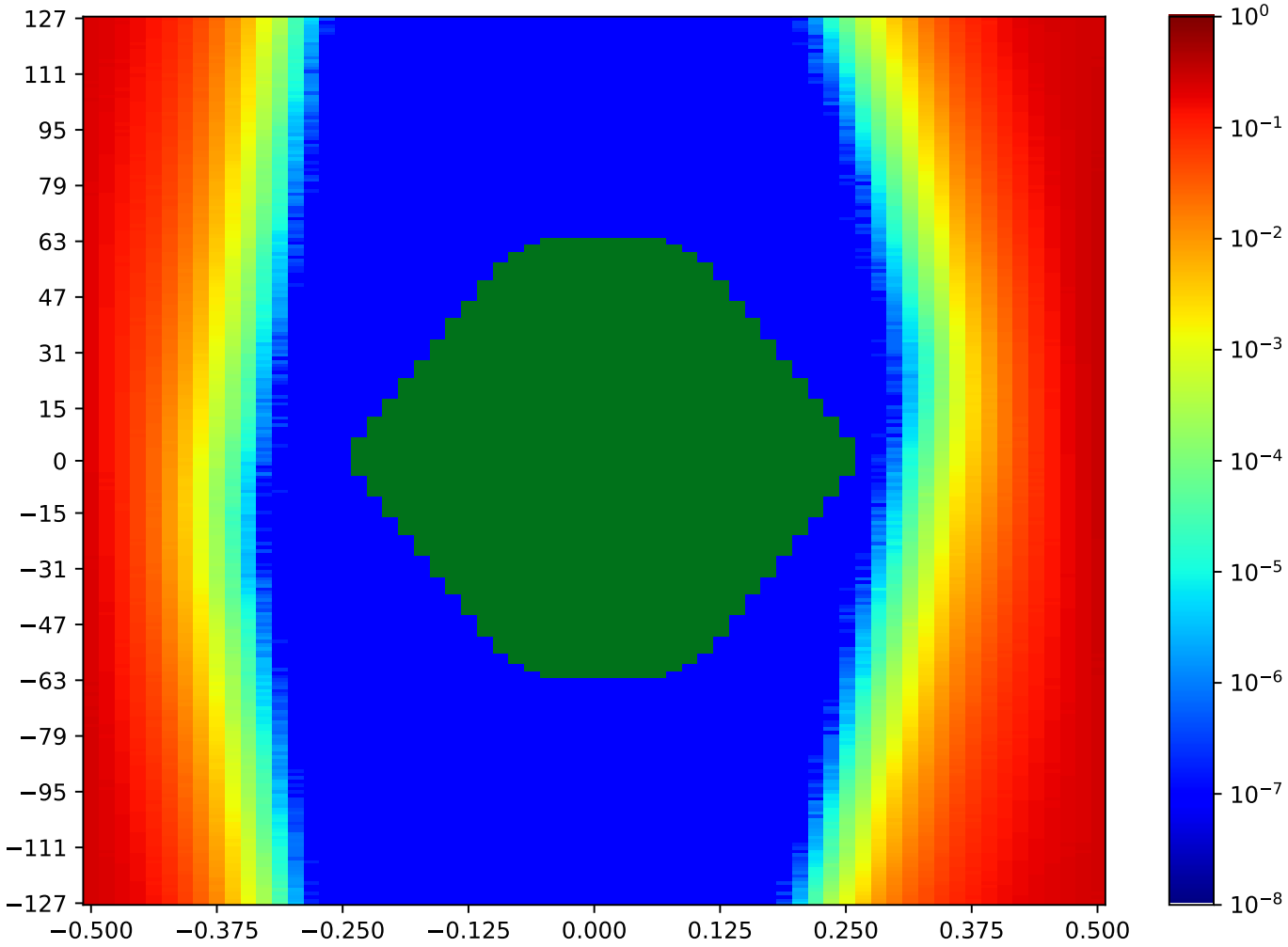


Figure 6.196: MSP_A_FPGA-TX1-07–RX10-07-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.9 MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Table 6.182: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:02:27		2019-Nov-27 11:02:56	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9101	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

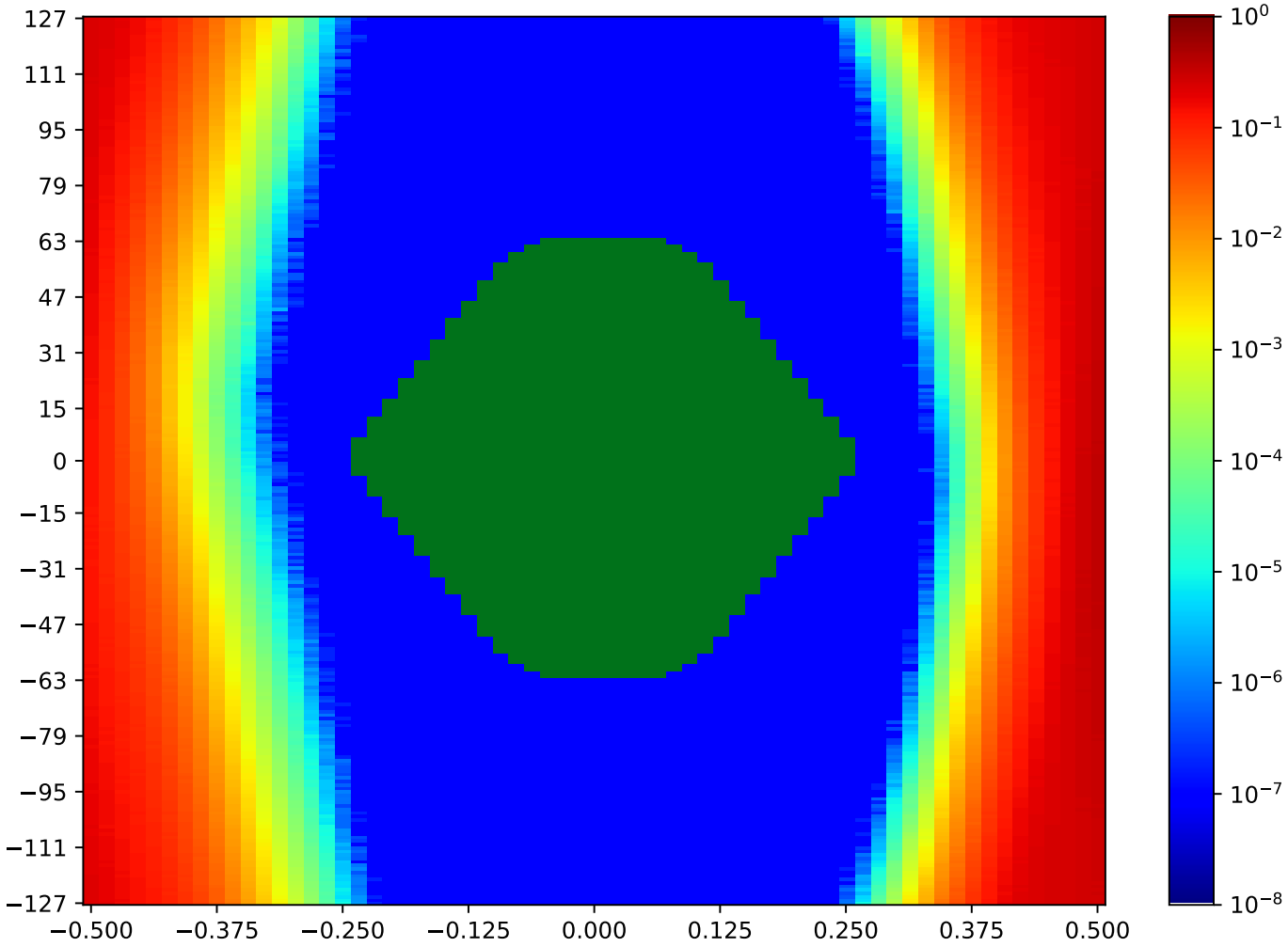


Figure 6.197: MSP_A_FPGA-TX1-08–RX10-08-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.10 MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Table 6.183: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 10:59:43		2019-Nov-27 11:00:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9646	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

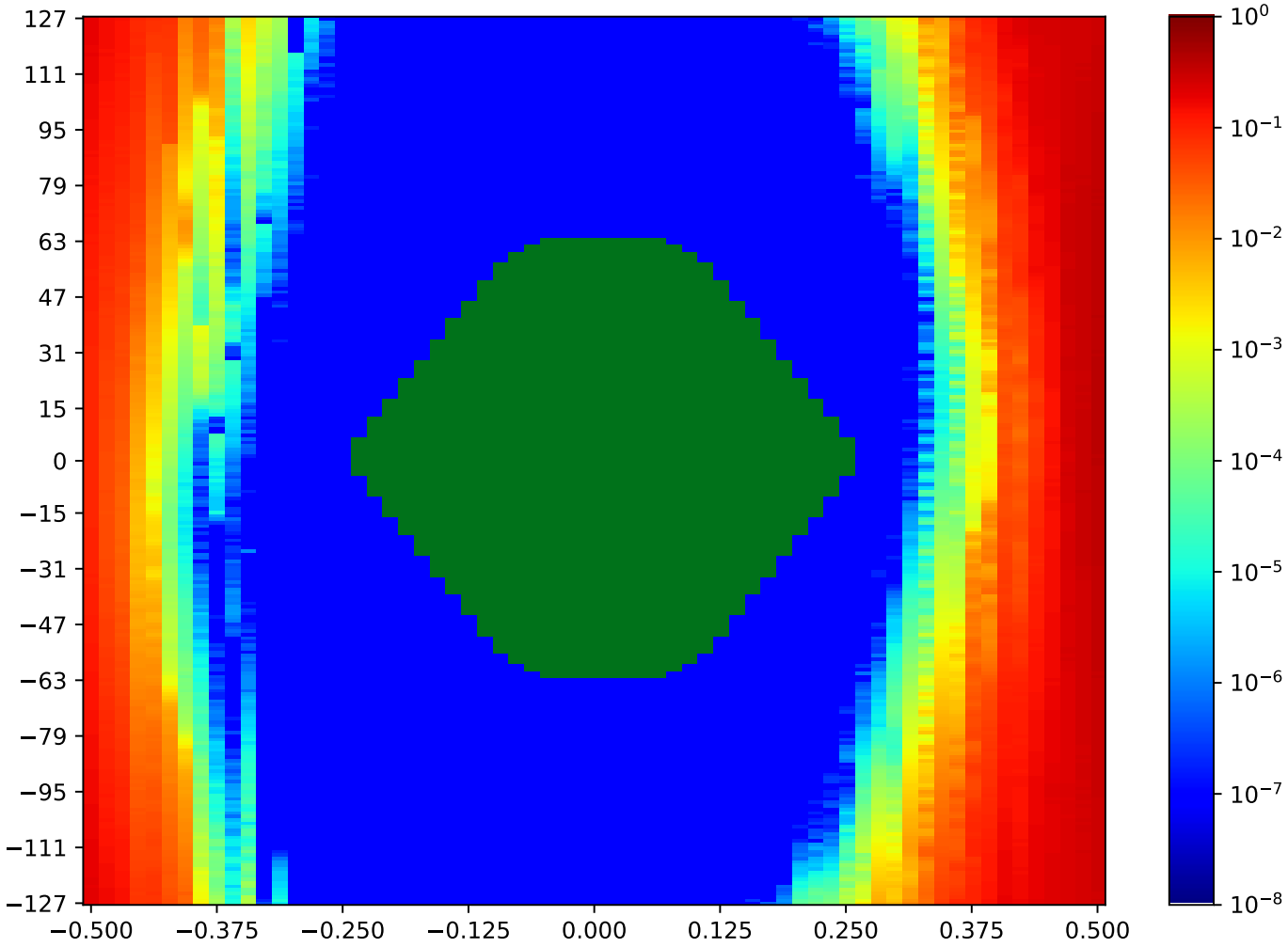


Figure 6.198: MSP_A_FPGA-TX1-09–RX10-09-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.11 MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Table 6.184: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:01:32		2019-Nov-27 11:01:59	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8888	39	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

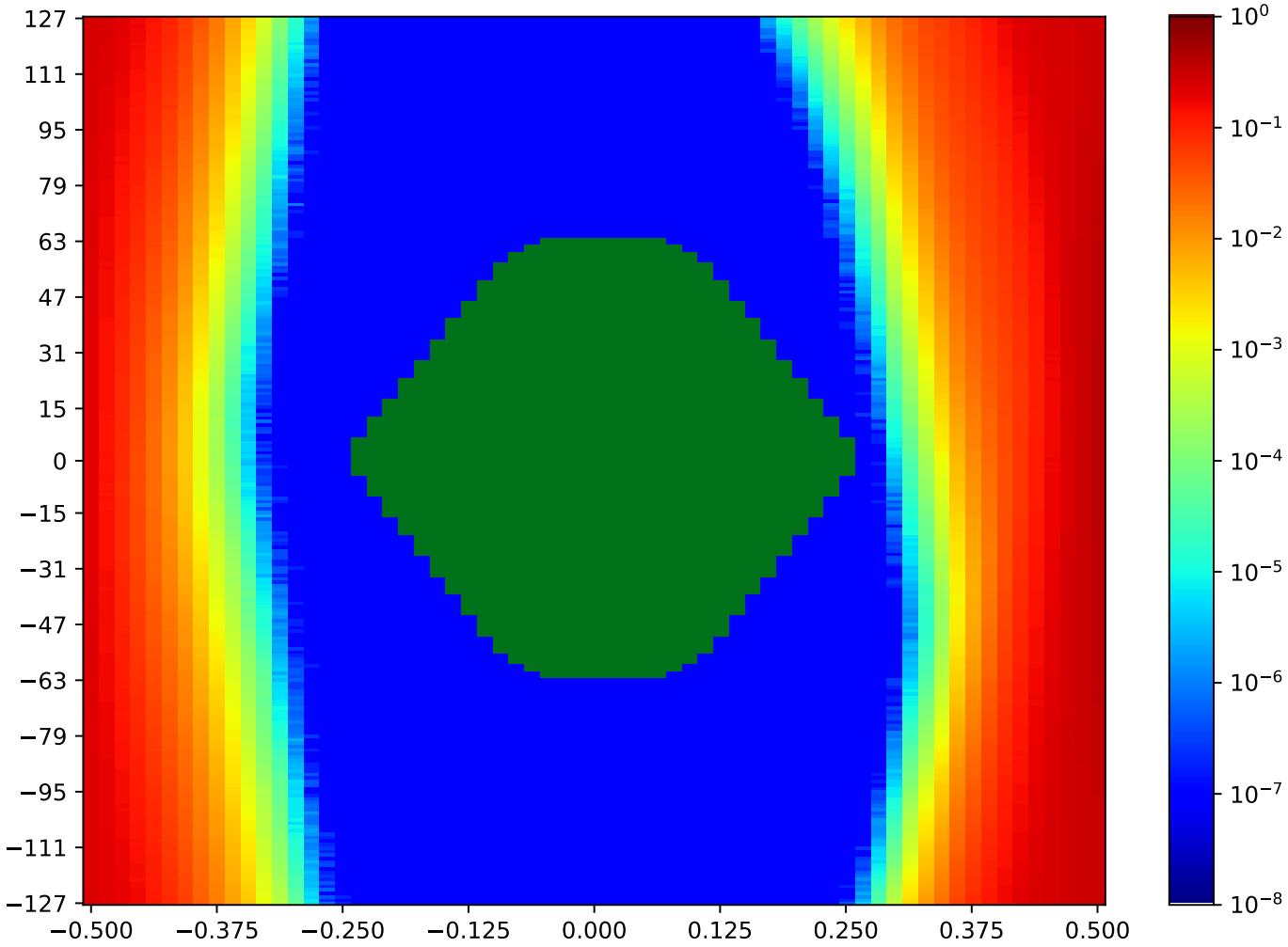


Figure 6.199: MSP_A_FPGA-TX1-10–RX10-10-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.15.12 MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Table 6.185: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:01:05		2019-Nov-27 11:01:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9027	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

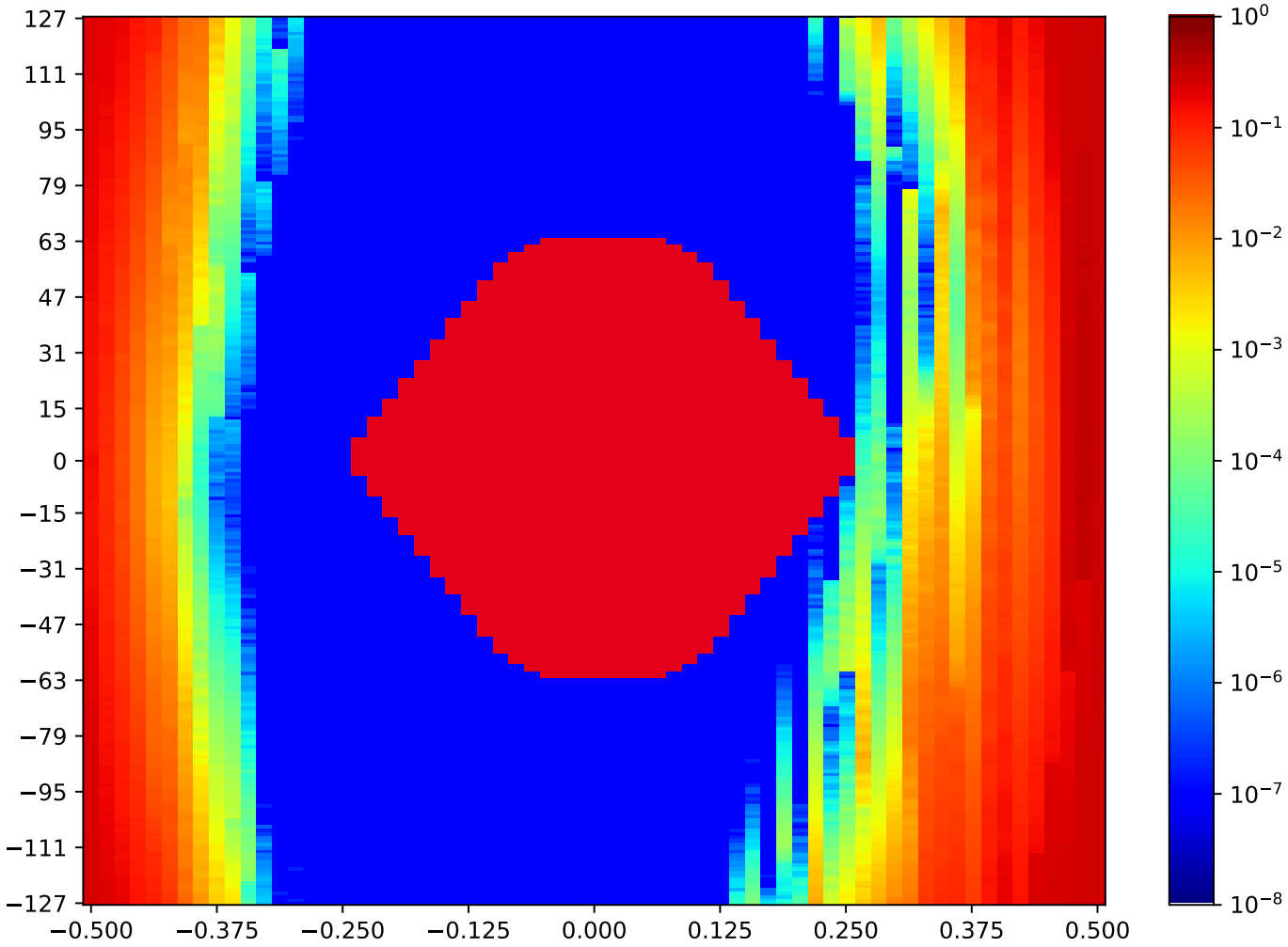


Figure 6.200: MSP_A_FPGA-TX1-11–RX10-11-MSP_C_FPGA

Call back to summary Figure 6.188. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16 MSP_A TX2 MSP_C RX11 Minipod Loopback

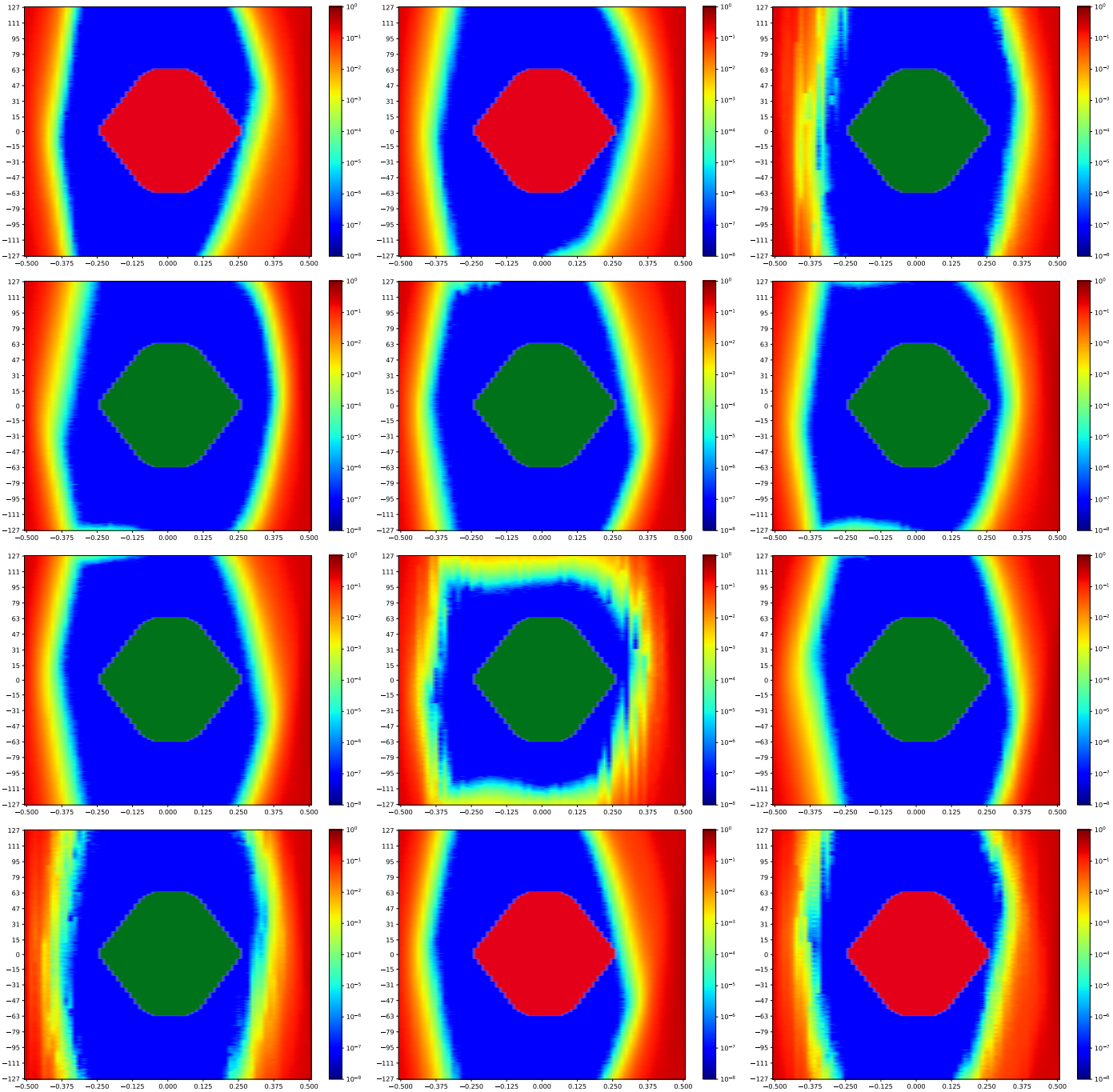


Figure 6.201: MSP_A TX2 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.214.

6.16.1 MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Table 6.186: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:04:43		2019-Nov-27 11:05:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9016	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

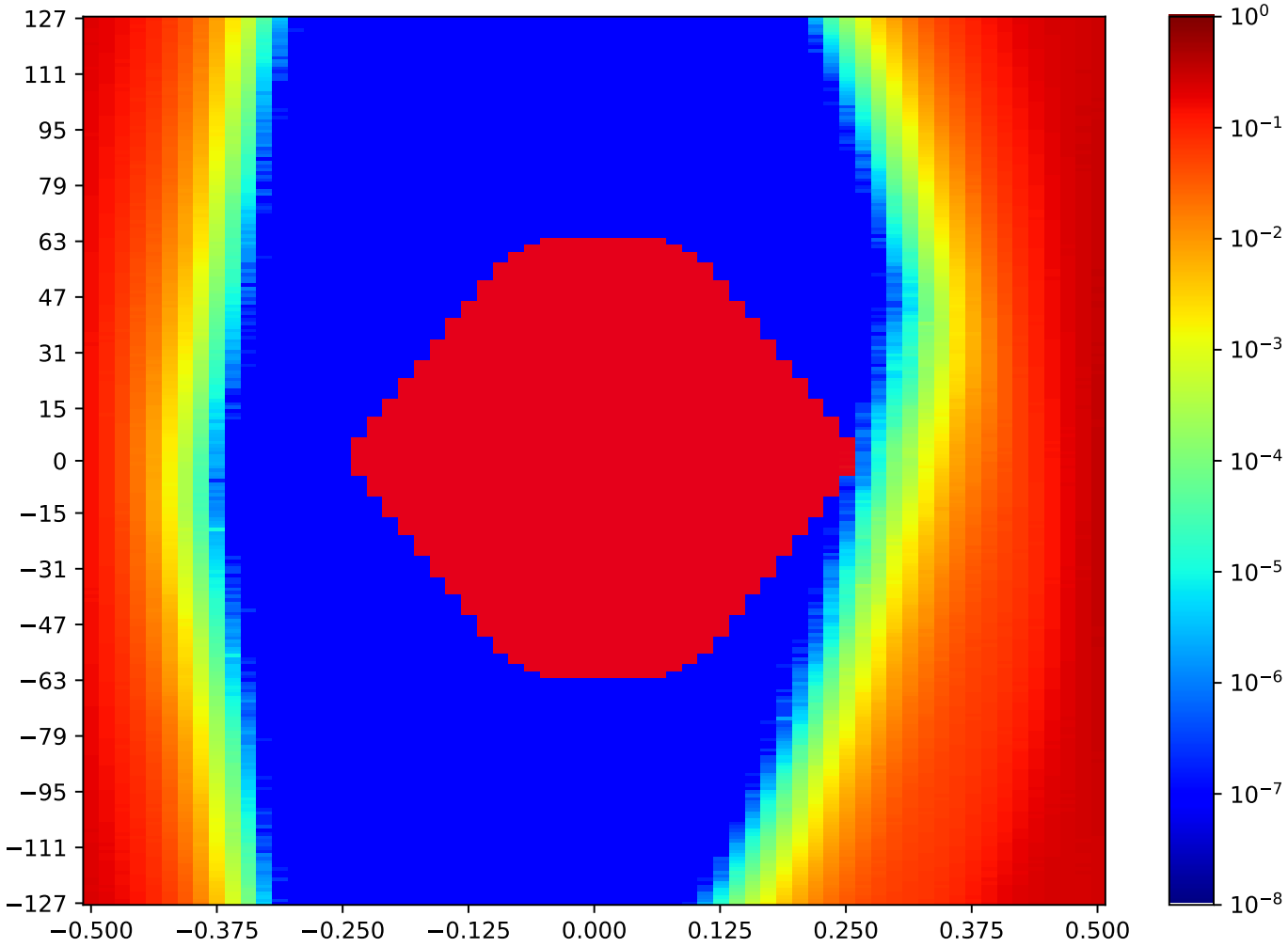


Figure 6.202: MSP_A_FPGA-TX2-00–RX11-00-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.2 MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Table 6.187: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:03:51		2019-Nov-27 11:04:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8608	39	60.00%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

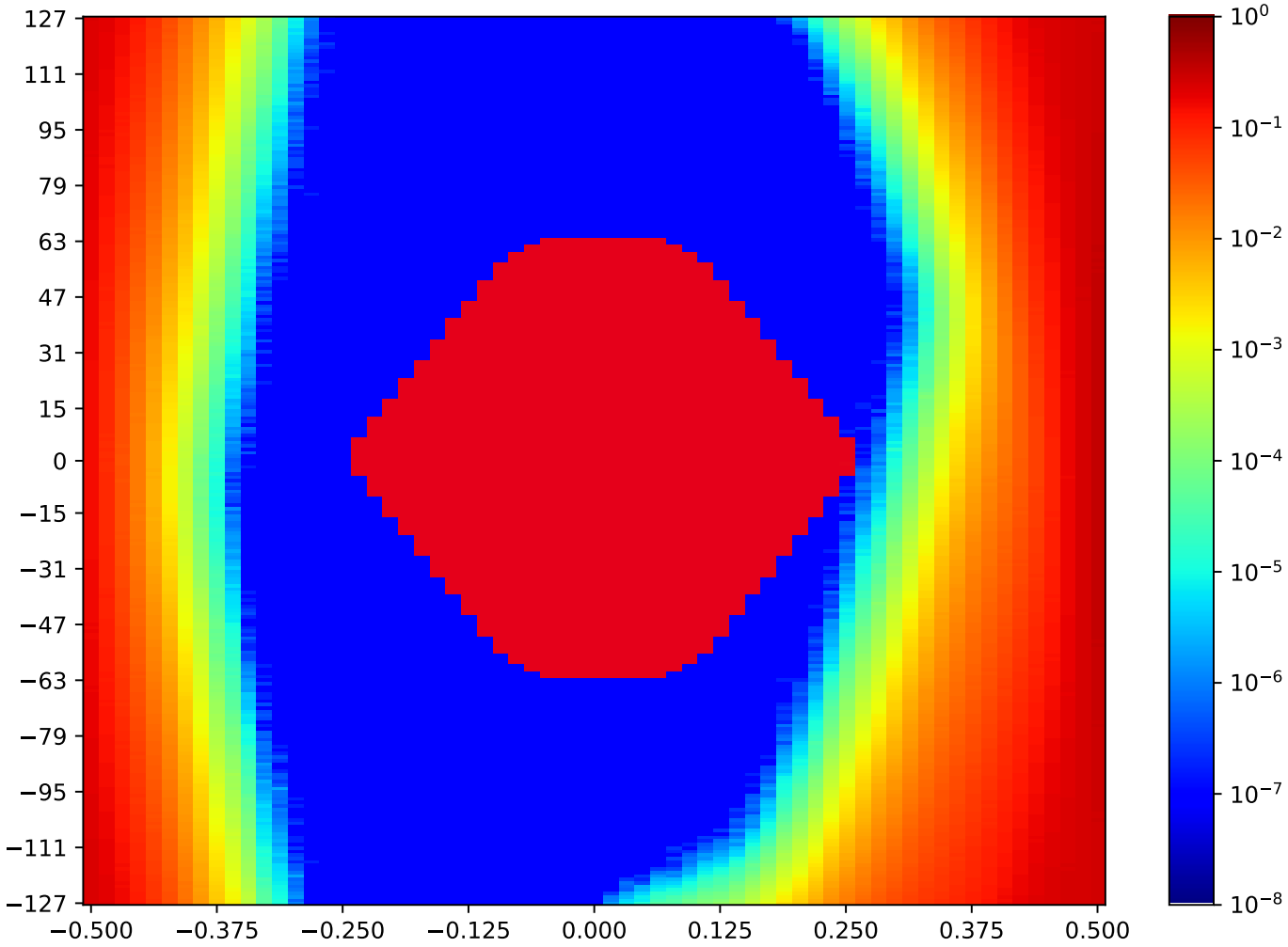


Figure 6.203: MSP_A_FPGA-TX2-01–RX11-01-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.3 MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Table 6.188: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:05:58		2019-Nov-27 11:06:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9157	41	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

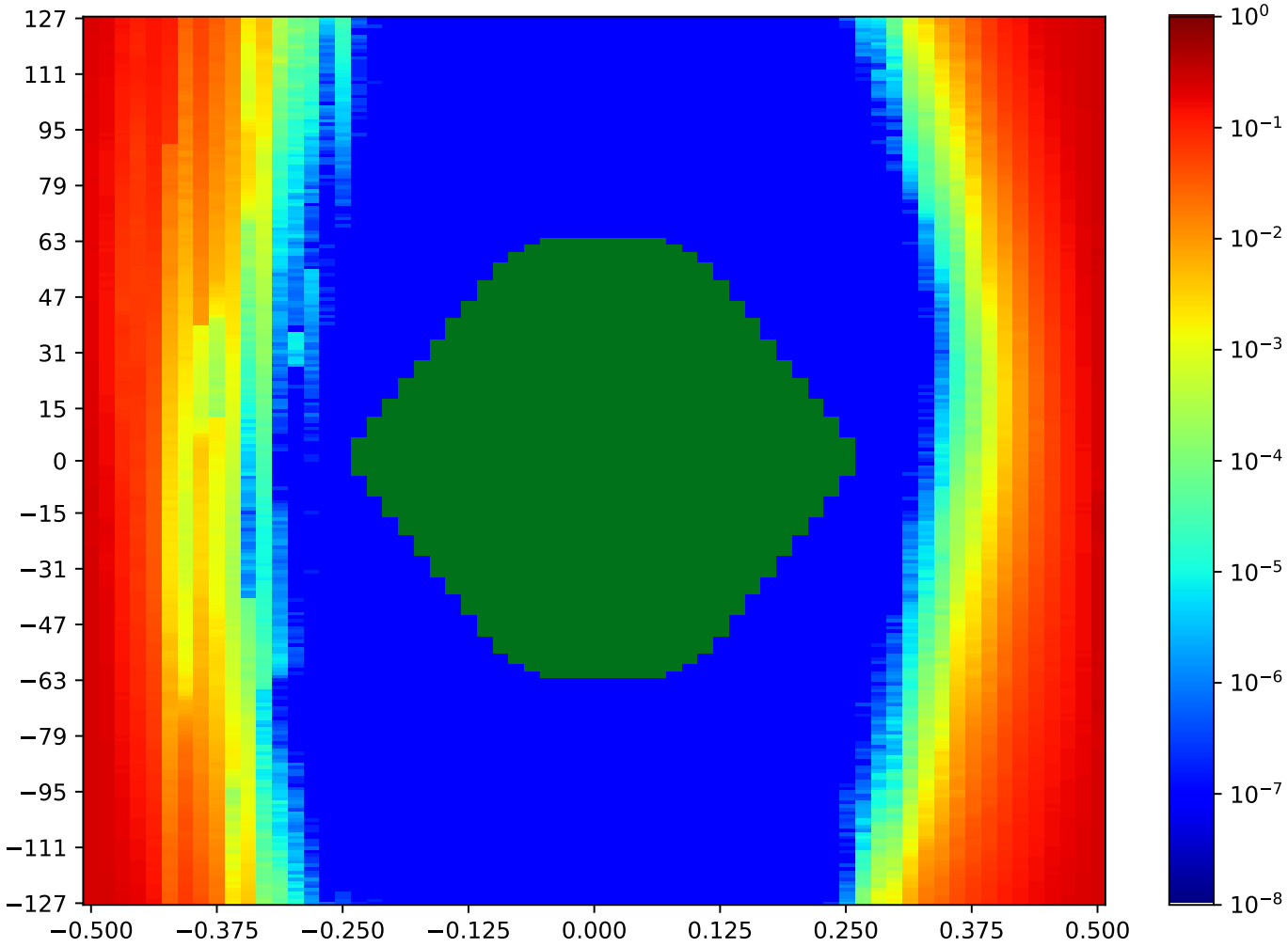


Figure 6.204: MSP_A_FPGA-TX2-02–RX11-02-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.4 MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Table 6.189: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:03:24		2019-Nov-27 11:03:50	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9685	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

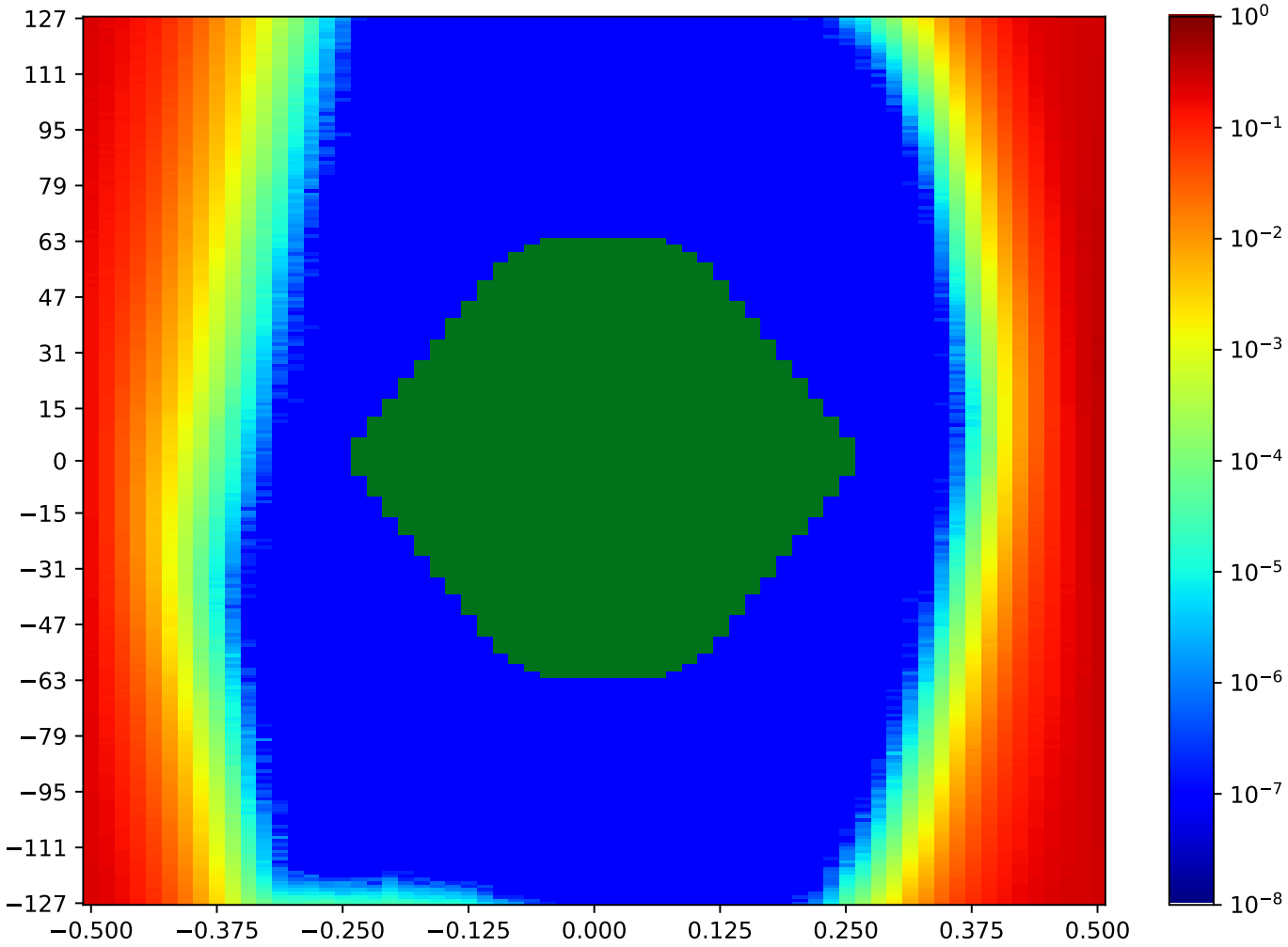


Figure 6.205: MSP_A_FPGA-TX2-03–RX11-03-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.5 MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Table 6.190: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:07:10		2019-Nov-27 11:07:35	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9164	40	61.54%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

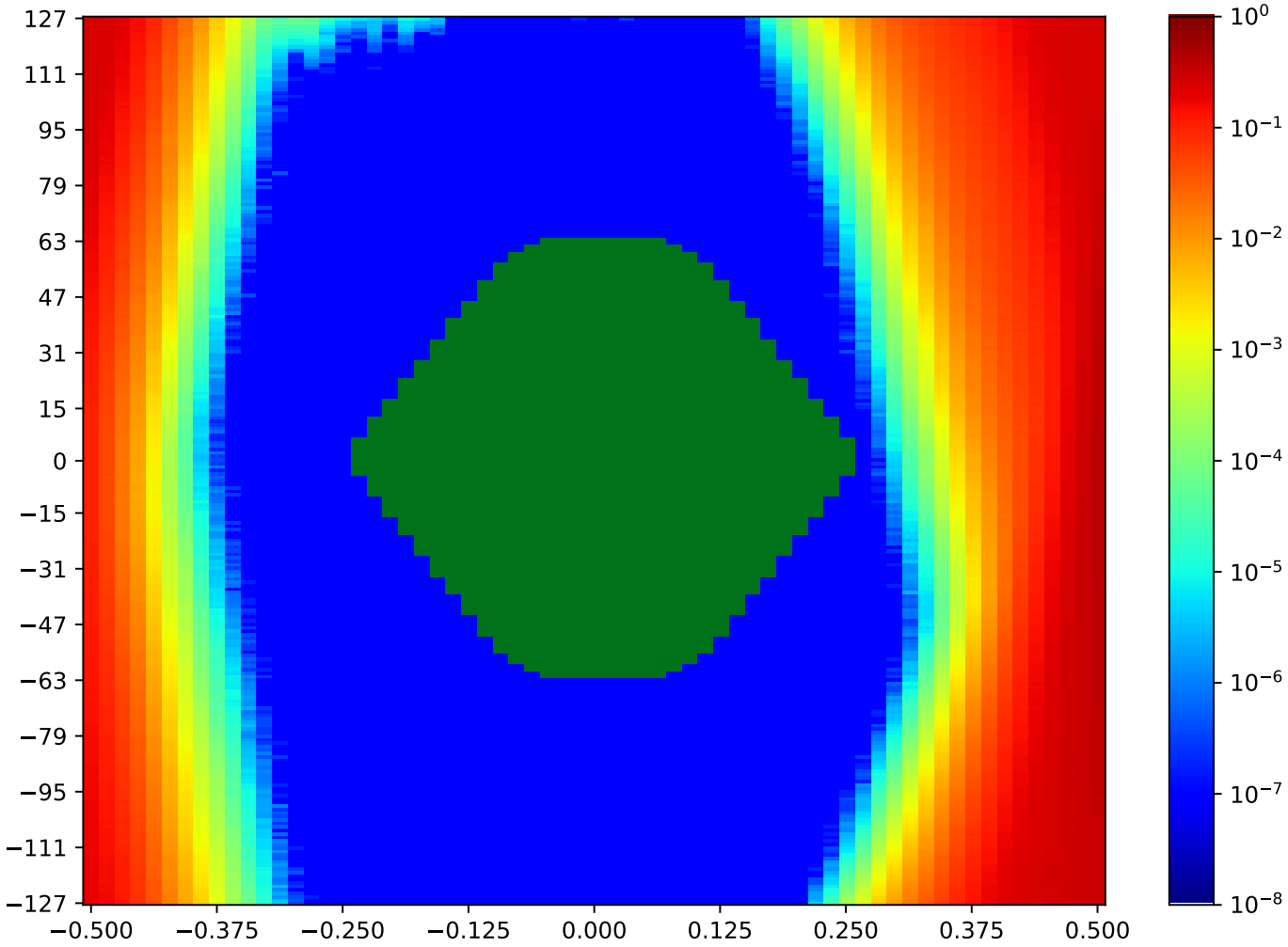


Figure 6.206: MSP_A_FPGA-TX2-04–RX11-04-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.6 MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Table 6.191: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:04:16		2019-Nov-27 11:04:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8822	41	63.08%	251	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

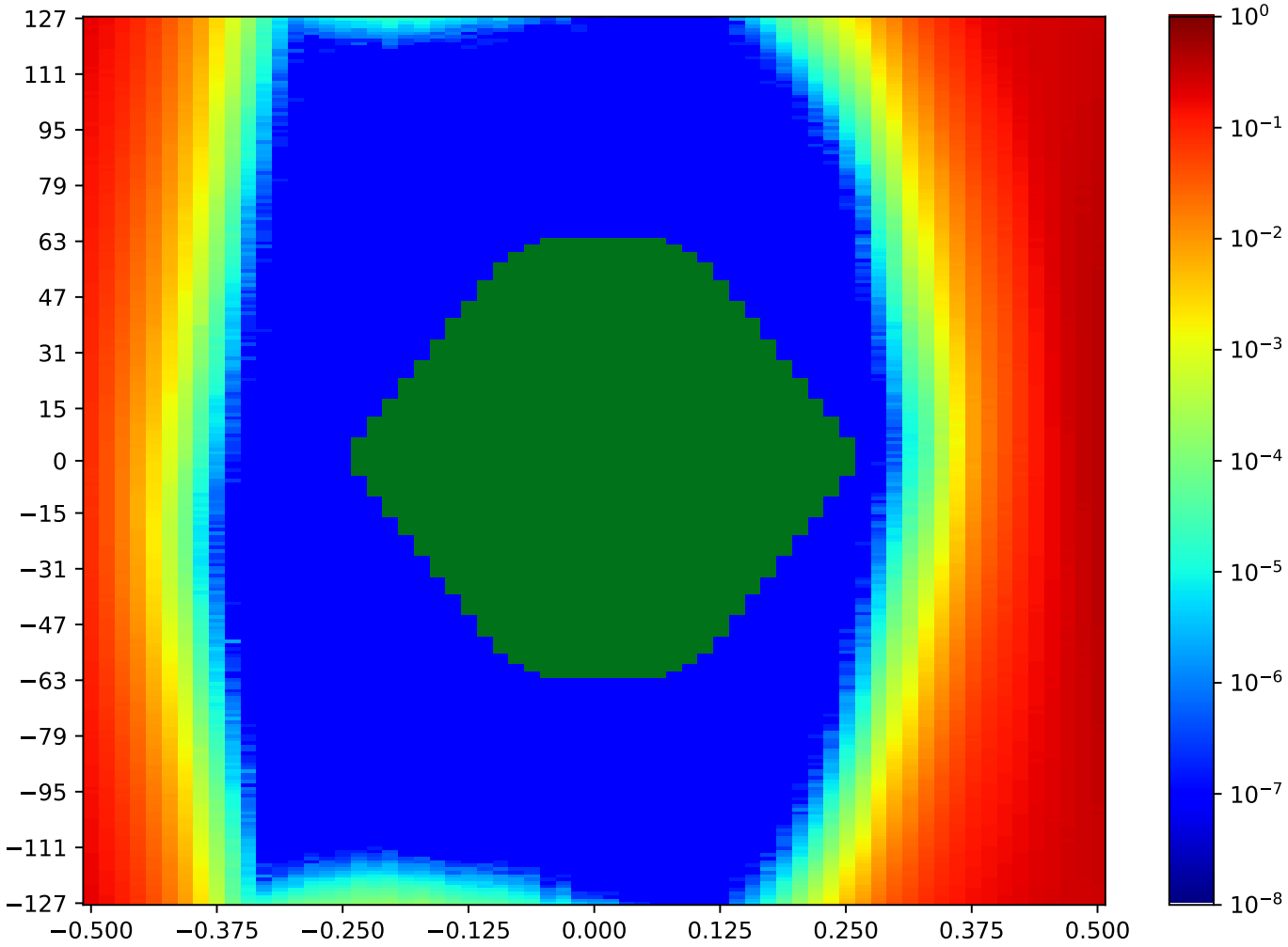


Figure 6.207: MSP_A_FPGA-TX2-05–RX11-05-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.7 MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Table 6.192: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:08:03		2019-Nov-27 11:08:31	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9017	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

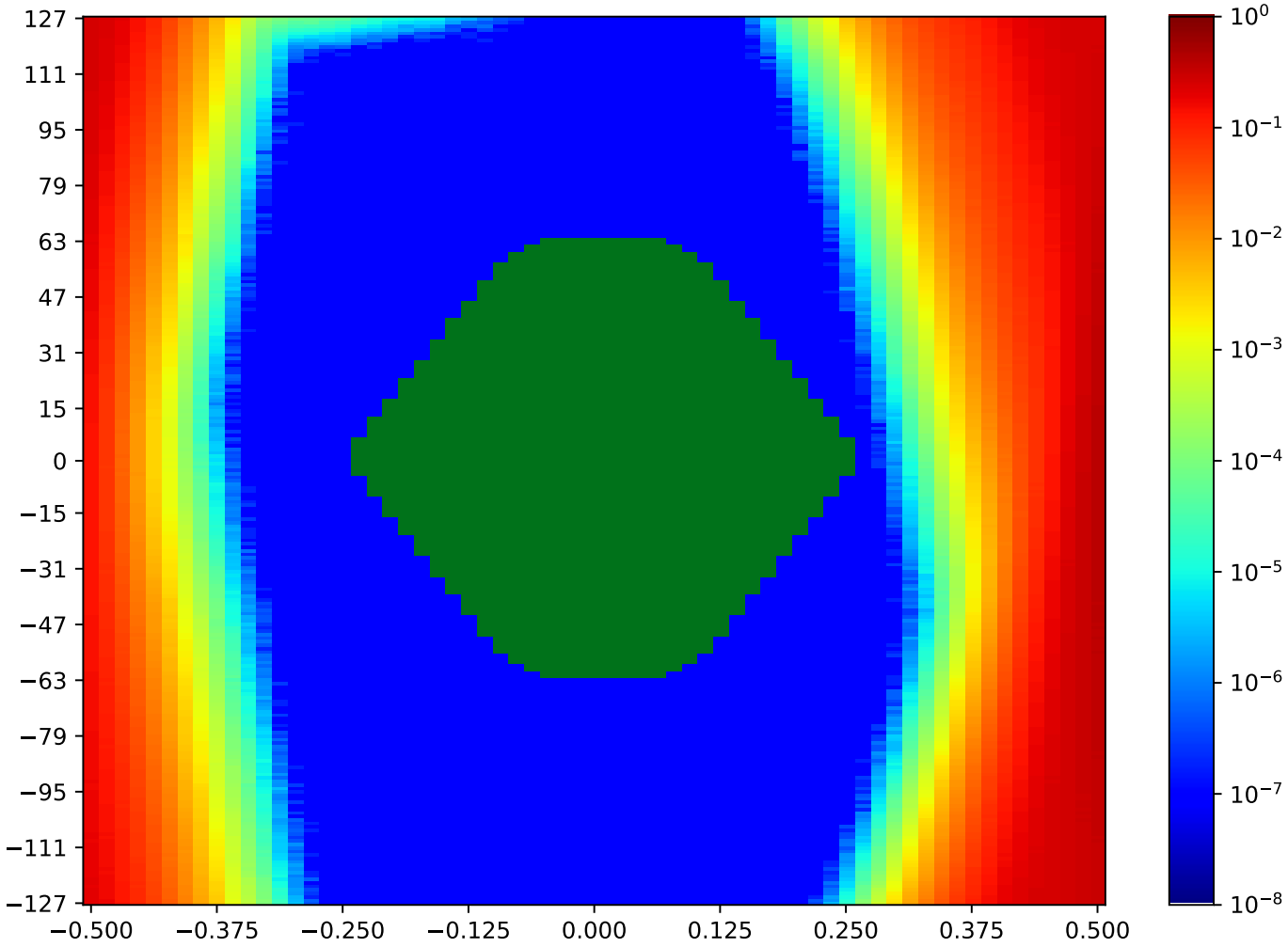


Figure 6.208: MSP_A_FPGA-TX2-06–RX11-06-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.8 MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Table 6.193: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:05:11		2019-Nov-27 11:05:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7040	41	61.54%	202	78.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

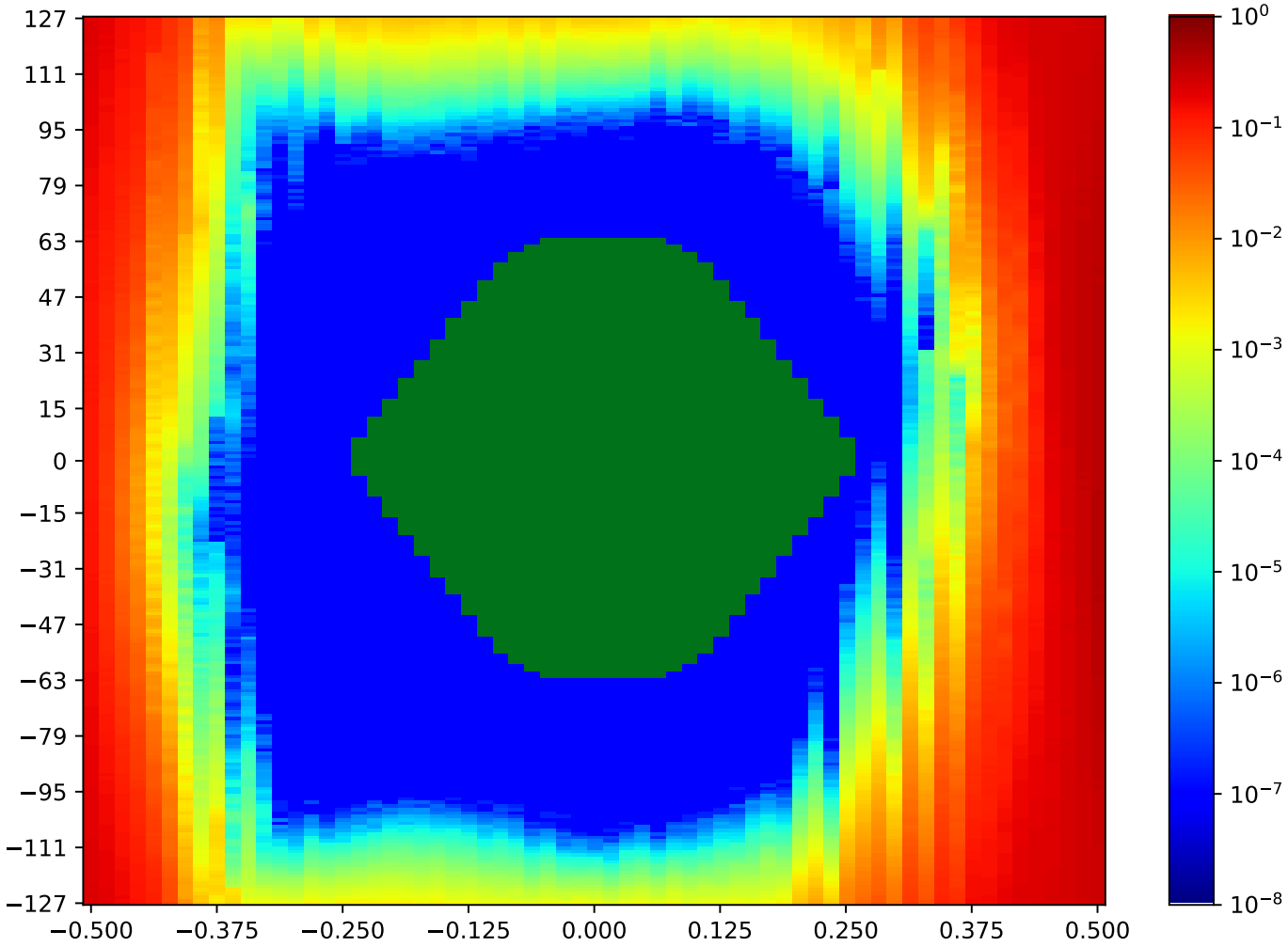


Figure 6.209: MSP_A_FPGA-TX2-07–RX11-07-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.9 MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Table 6.194: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:07:35		2019-Nov-27 11:08:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8941	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

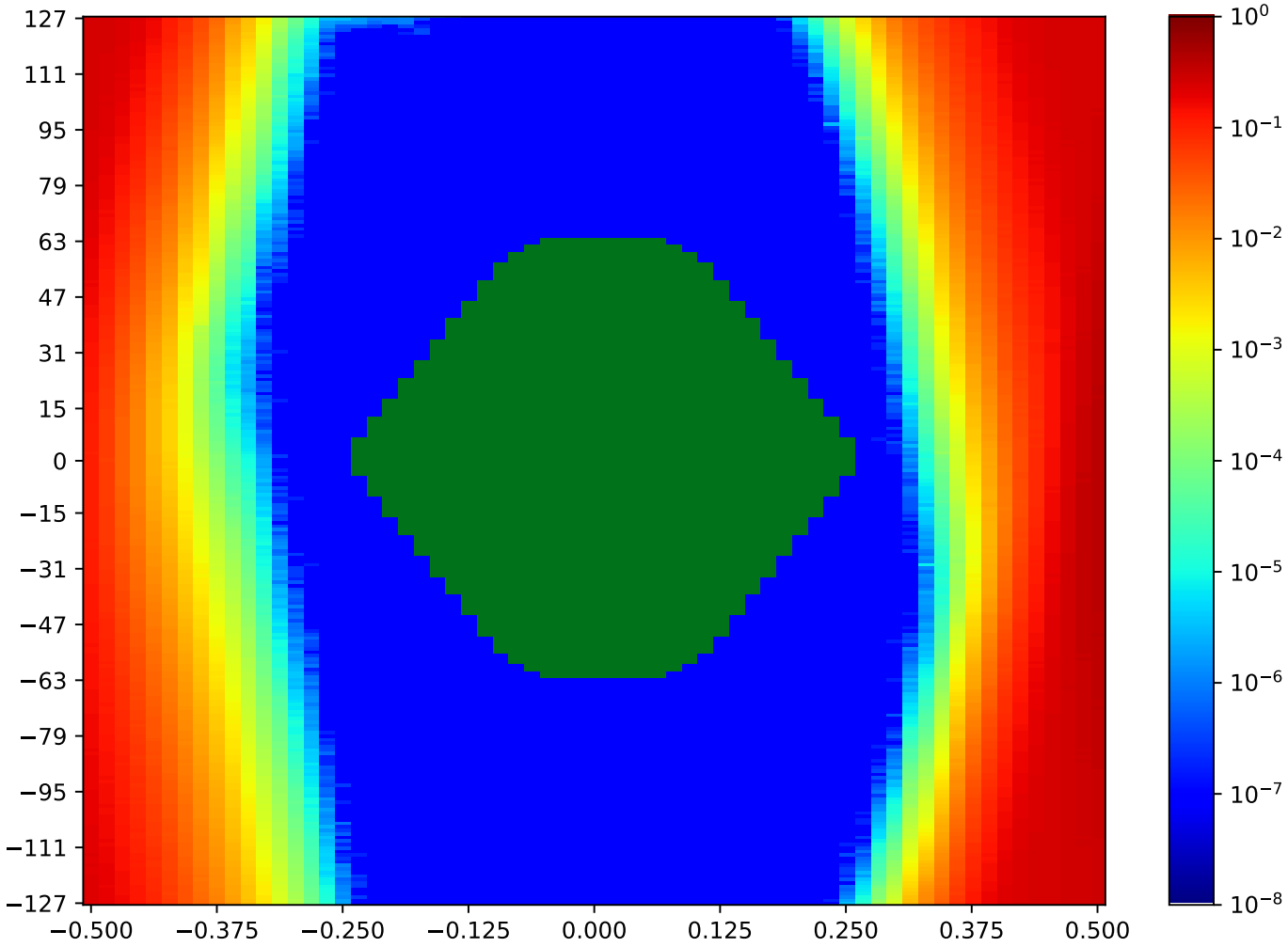


Figure 6.210: MSP_A_FPGA-TX2-08–RX11-08-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.10 MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Table 6.195: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:05:30		2019-Nov-27 11:05:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9294	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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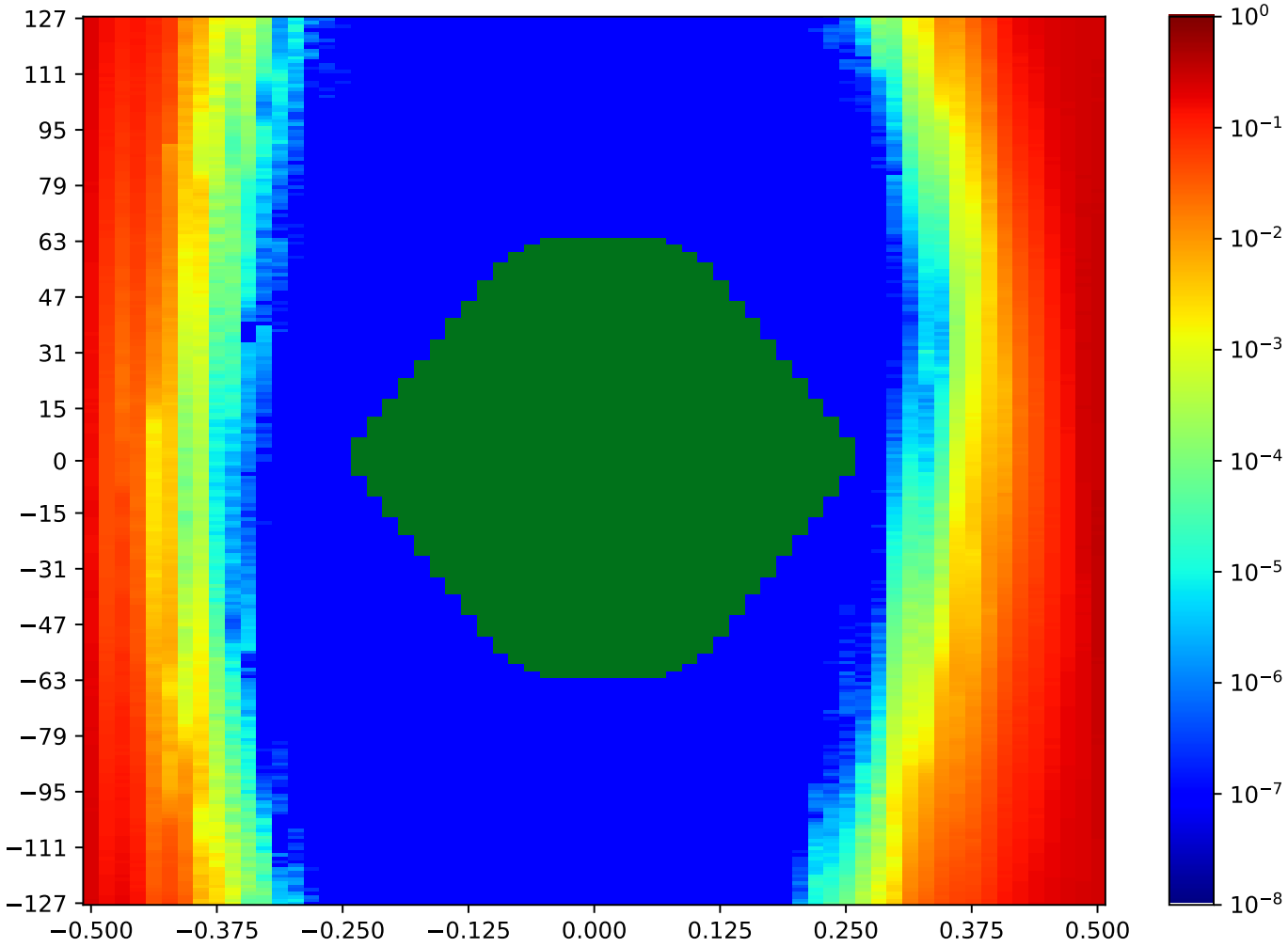


Figure 6.211: MSP_A_FPGA-TX2-09–RX11-09-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.11 MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Table 6.196: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:06:43		2019-Nov-27 11:07:10	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8916	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

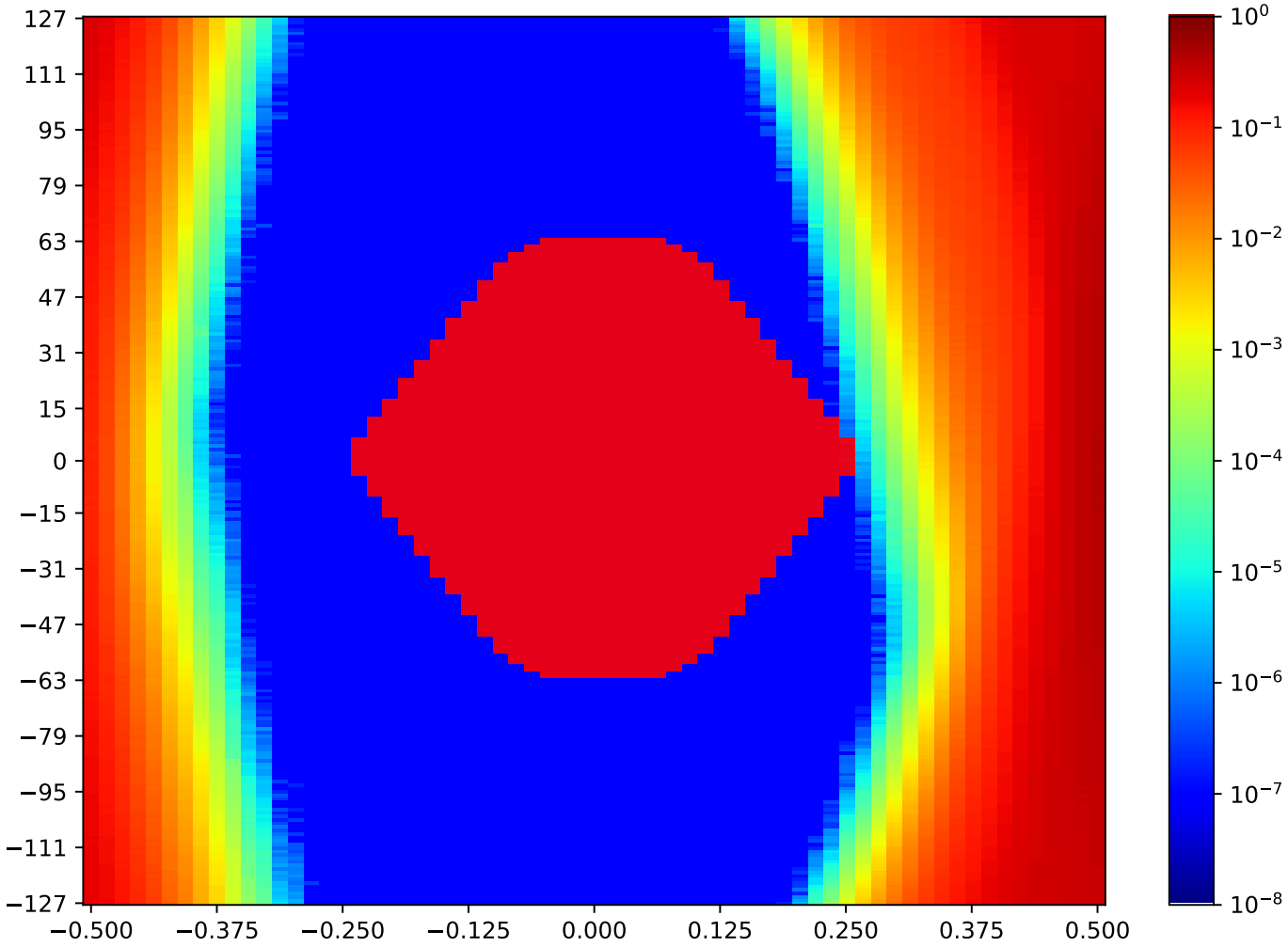


Figure 6.212: MSP_A_FPGA-TX2-10–RX11-10-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.16.12 MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Table 6.197: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:06:17		2019-Nov-27 11:06:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8716	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

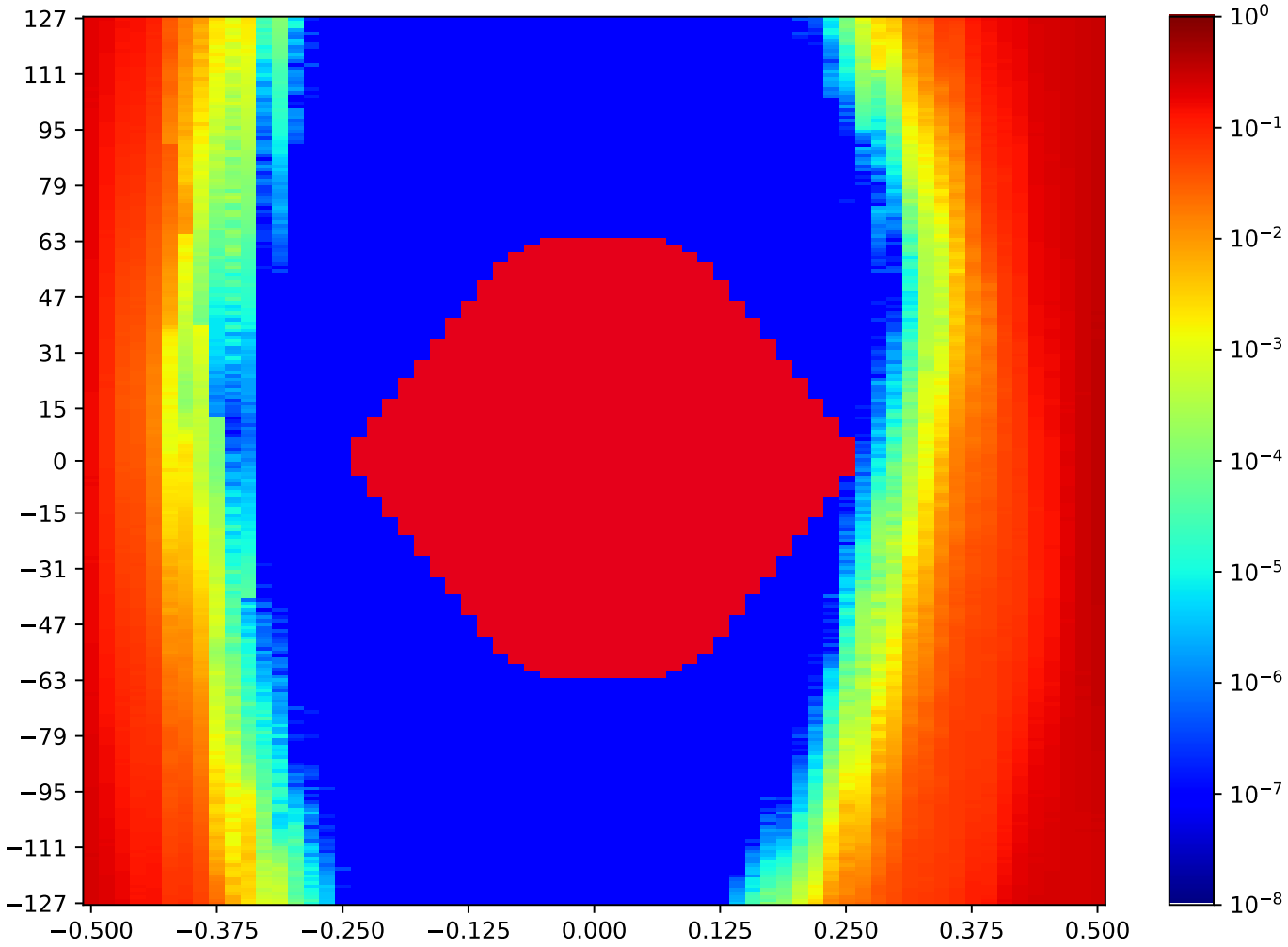


Figure 6.213: MSP_A_FPGA-TX2-11–RX11-11-MSP_C_FPGA

Call back to summary Figure 6.201. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17 MSP_C TX3 MSP_A RX1 Minipod Loopback

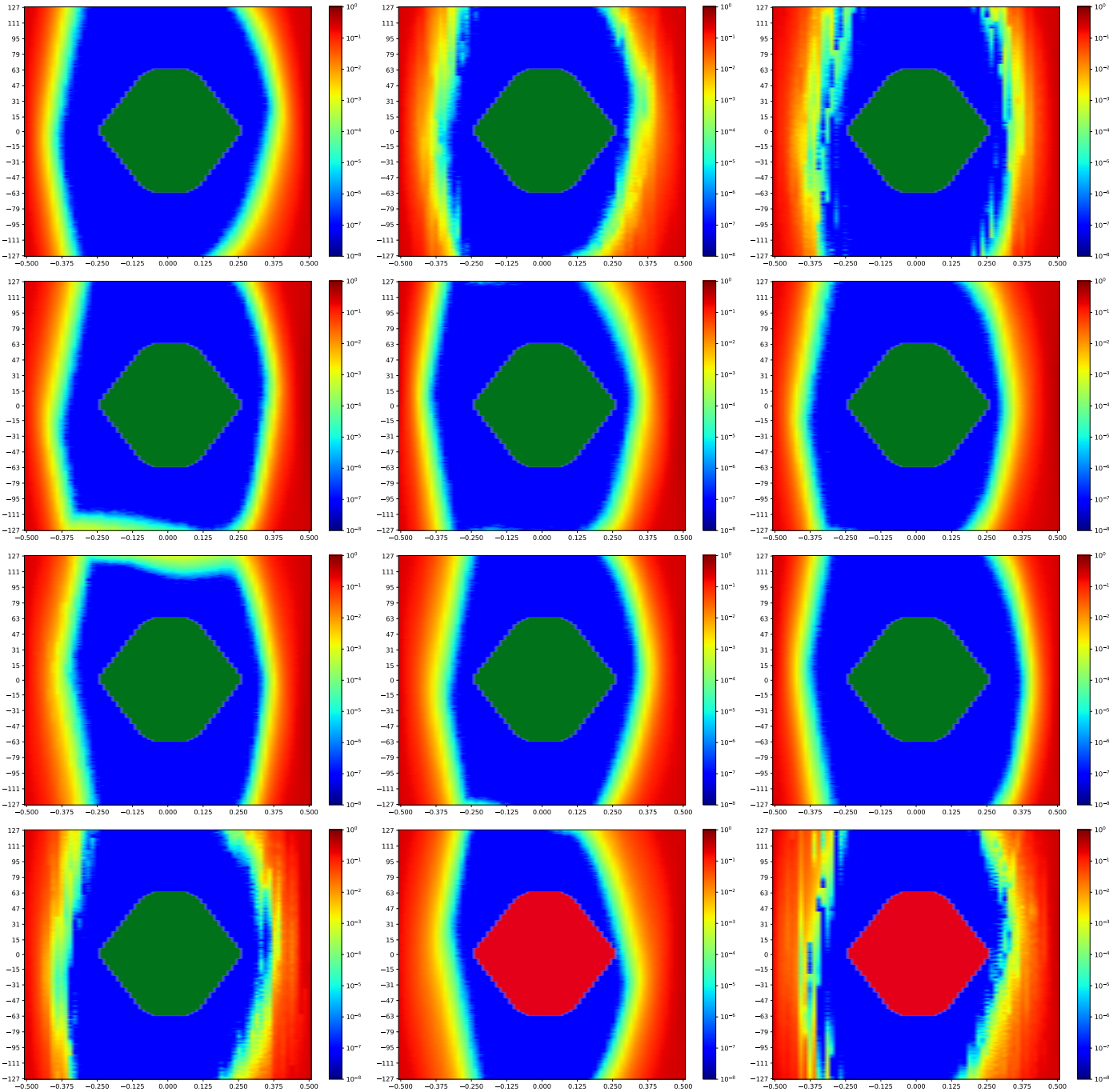


Figure 6.214: MSP_C TX3 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.227.

6.17.1 MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Table 6.198: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:09:44		2019-Nov-27 11:10:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9726	44	67.69%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

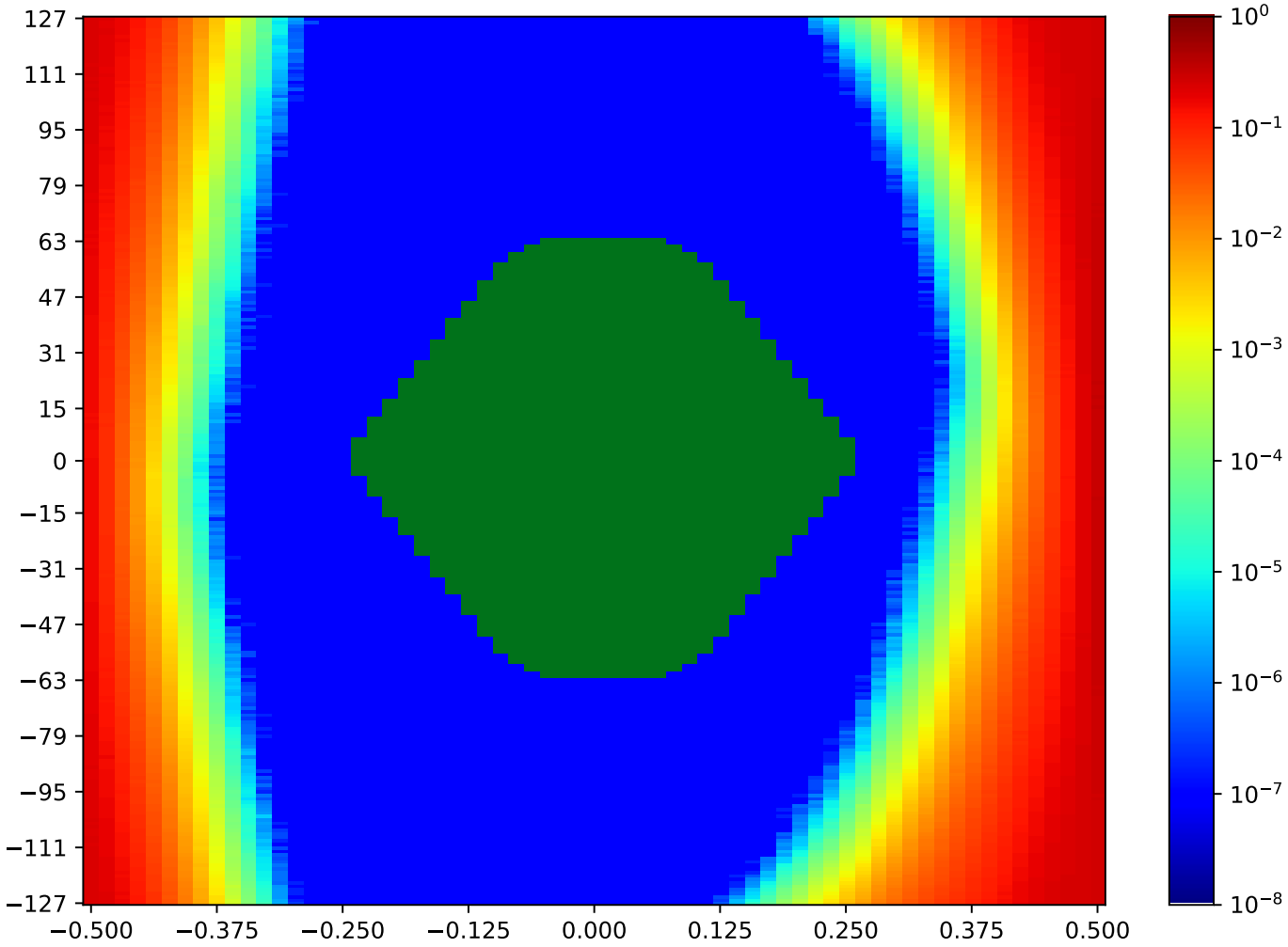


Figure 6.215: MSP_C_FPGA-TX3-00–RX1-00-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.2 MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Table 6.199: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:10:39		2019-Nov-27 11:11:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8519	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

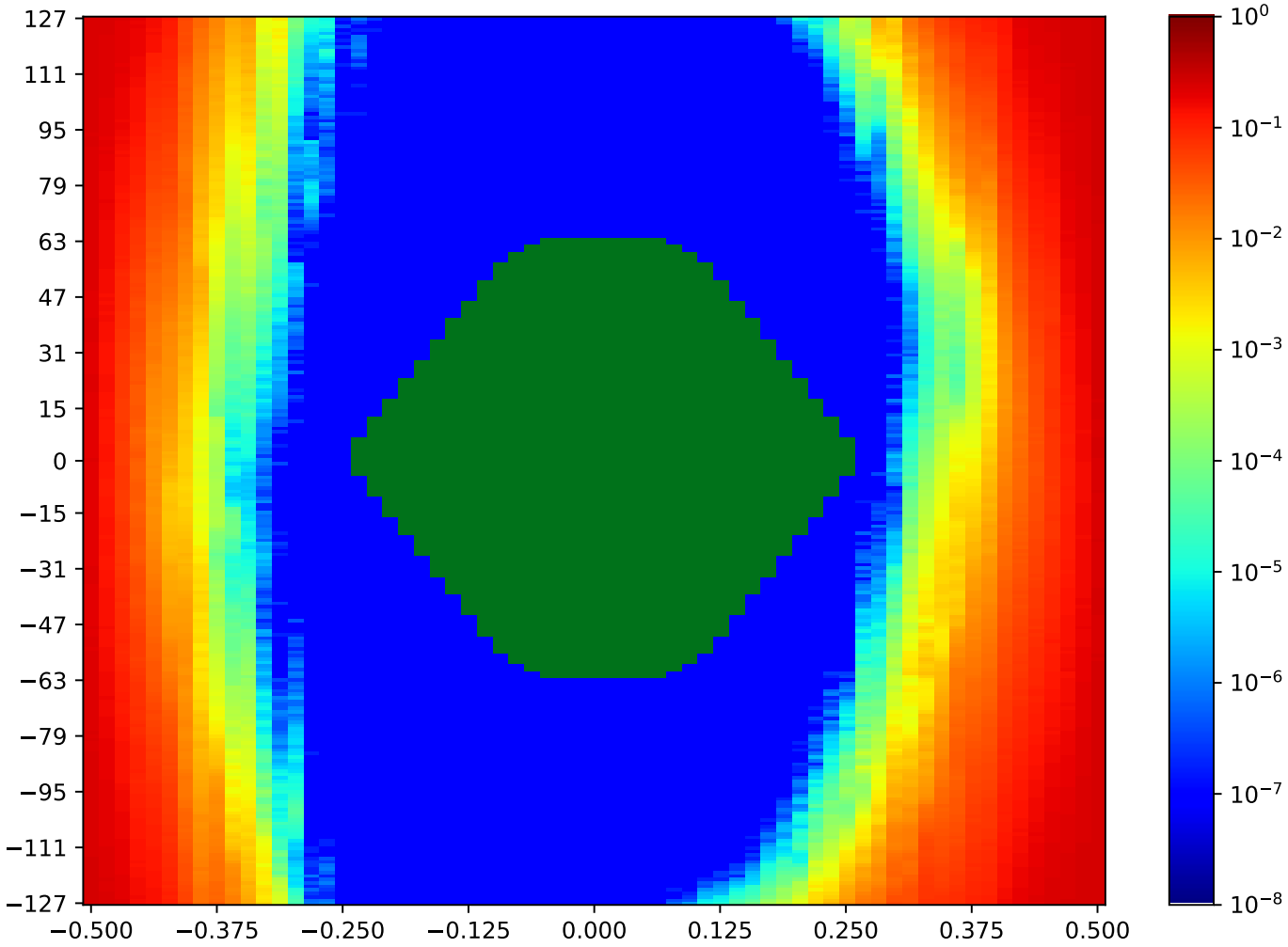


Figure 6.216: MSP_C_FPGA-TX3-01–RX1-01-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.3 MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Table 6.200: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:11:06		2019-Nov-27 11:11:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8612	39	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

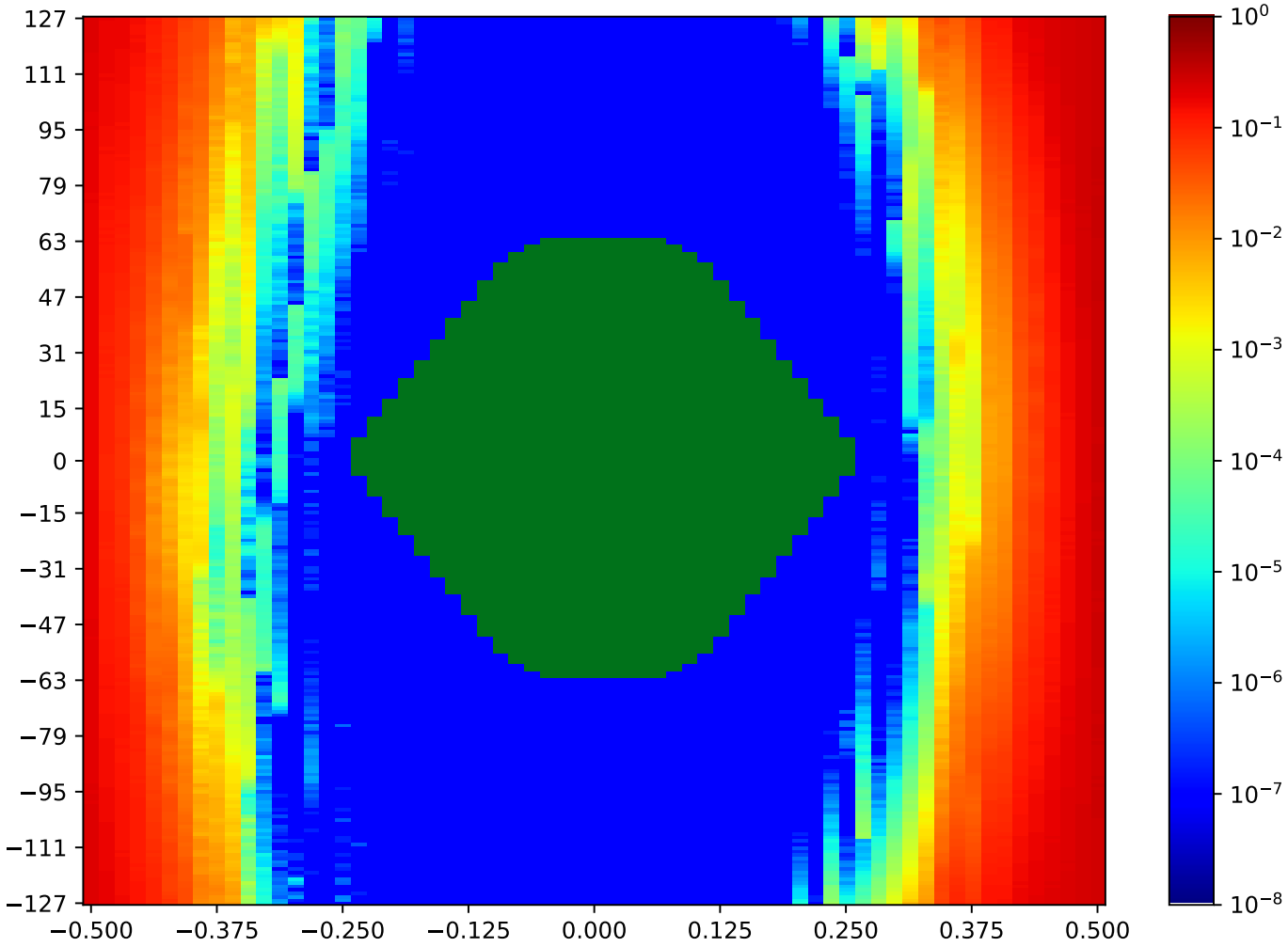


Figure 6.217: MSP_C_FPGA-TX3-02–RX1-02-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.4 MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Table 6.201: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:08:51		2019-Nov-27 11:09:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9242	43	66.15%	242	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

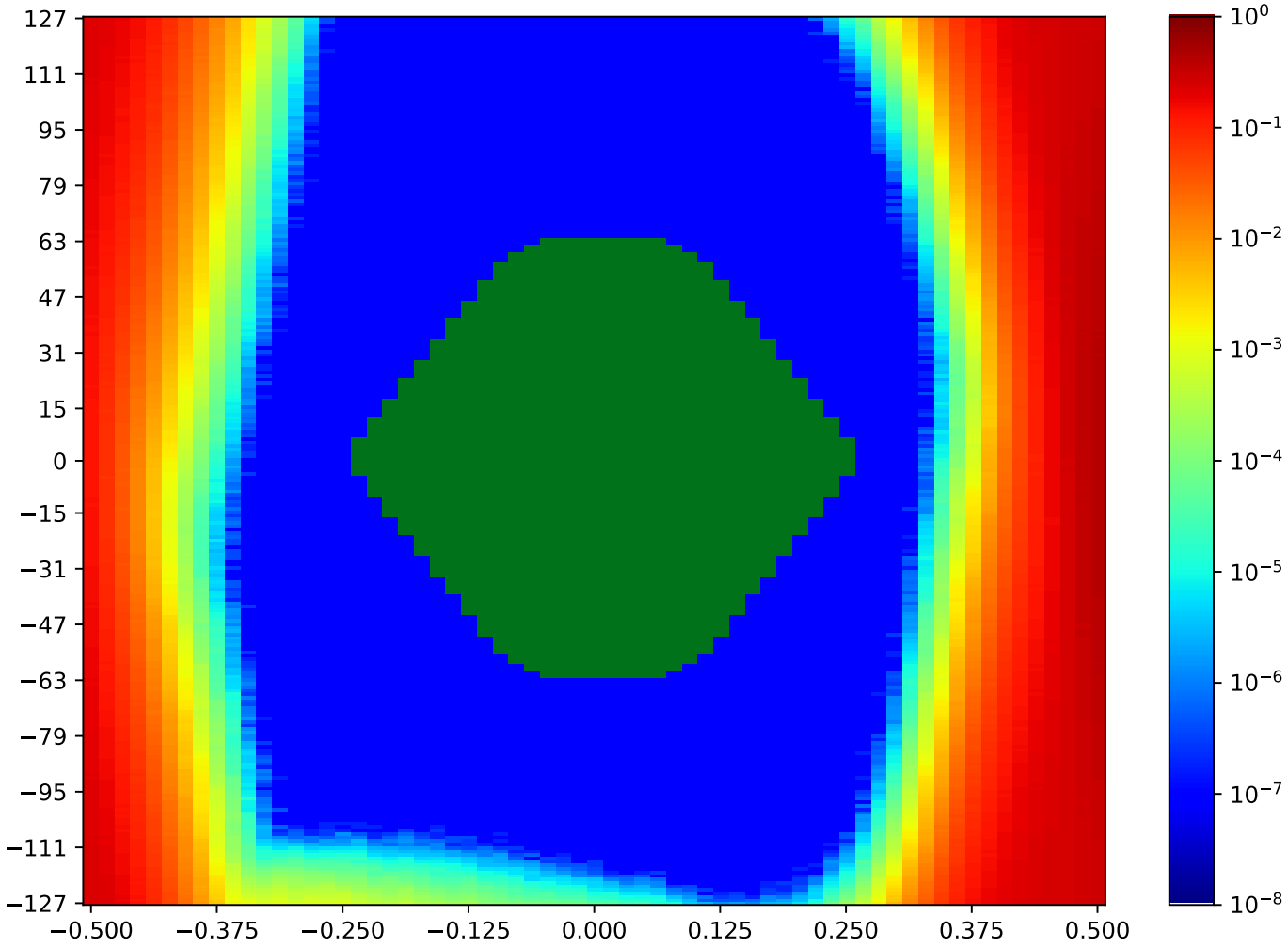


Figure 6.218: MSP_C_FPGA-TX3-03–RX1-03-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.5 MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Table 6.202: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:12:29		2019-Nov-27 11:12:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9055	43	66.15%	255	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

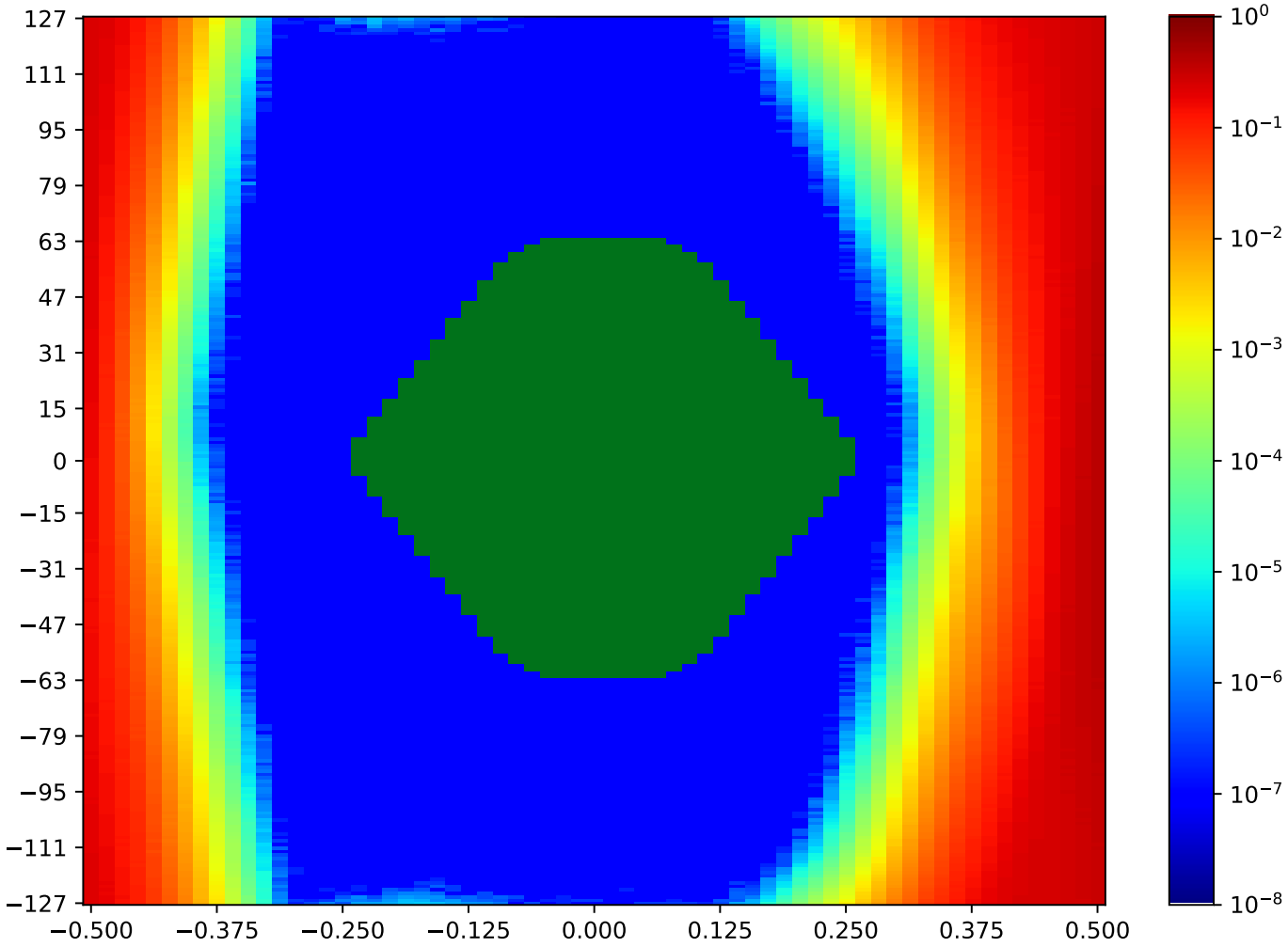


Figure 6.219: MSP_C_FPGA-TX3-04–RX1-04-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.6 MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Table 6.203: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:08:31		2019-Nov-27 11:08:51	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8977	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

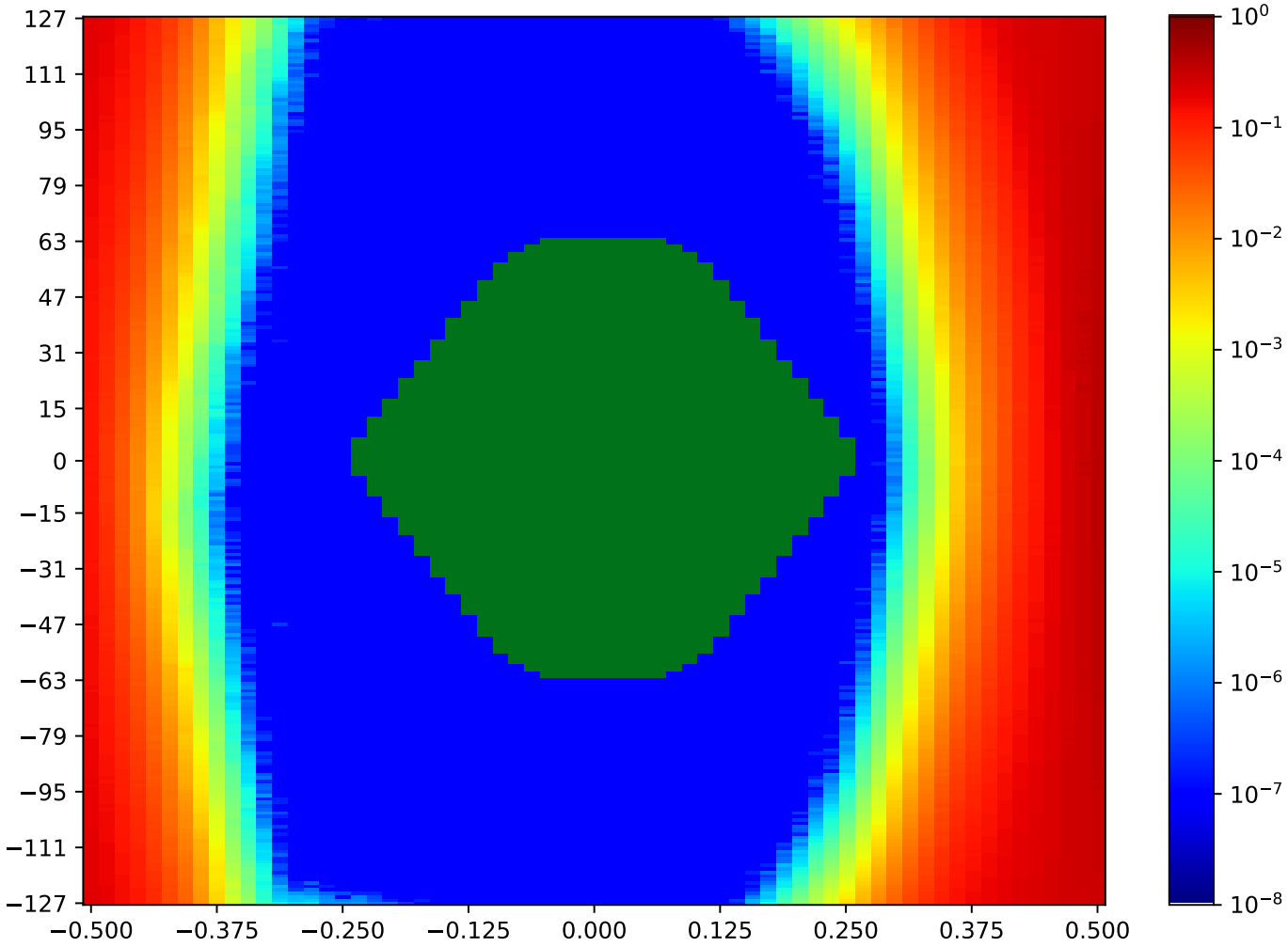


Figure 6.220: MSP_C_FPGA-TX3-05–RX1-05-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.7 MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Table 6.204: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:13:27		2019-Nov-27 11:13:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8381	40	61.54%	229	89.80%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

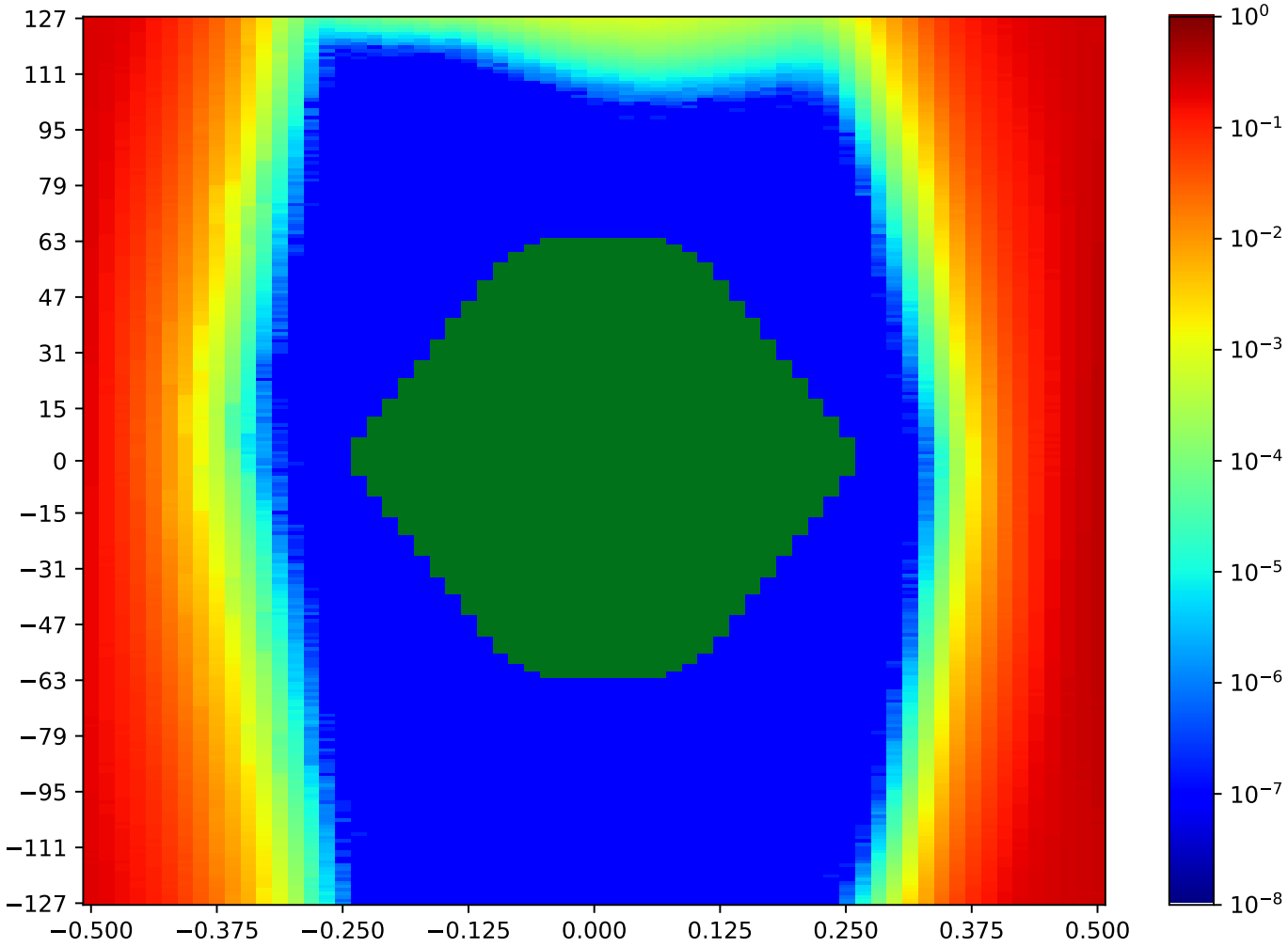


Figure 6.221: MSP_C_FPGA-TX3-06–RX1-06-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.8 MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Table 6.205: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:09:18		2019-Nov-27 11:09:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8605	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

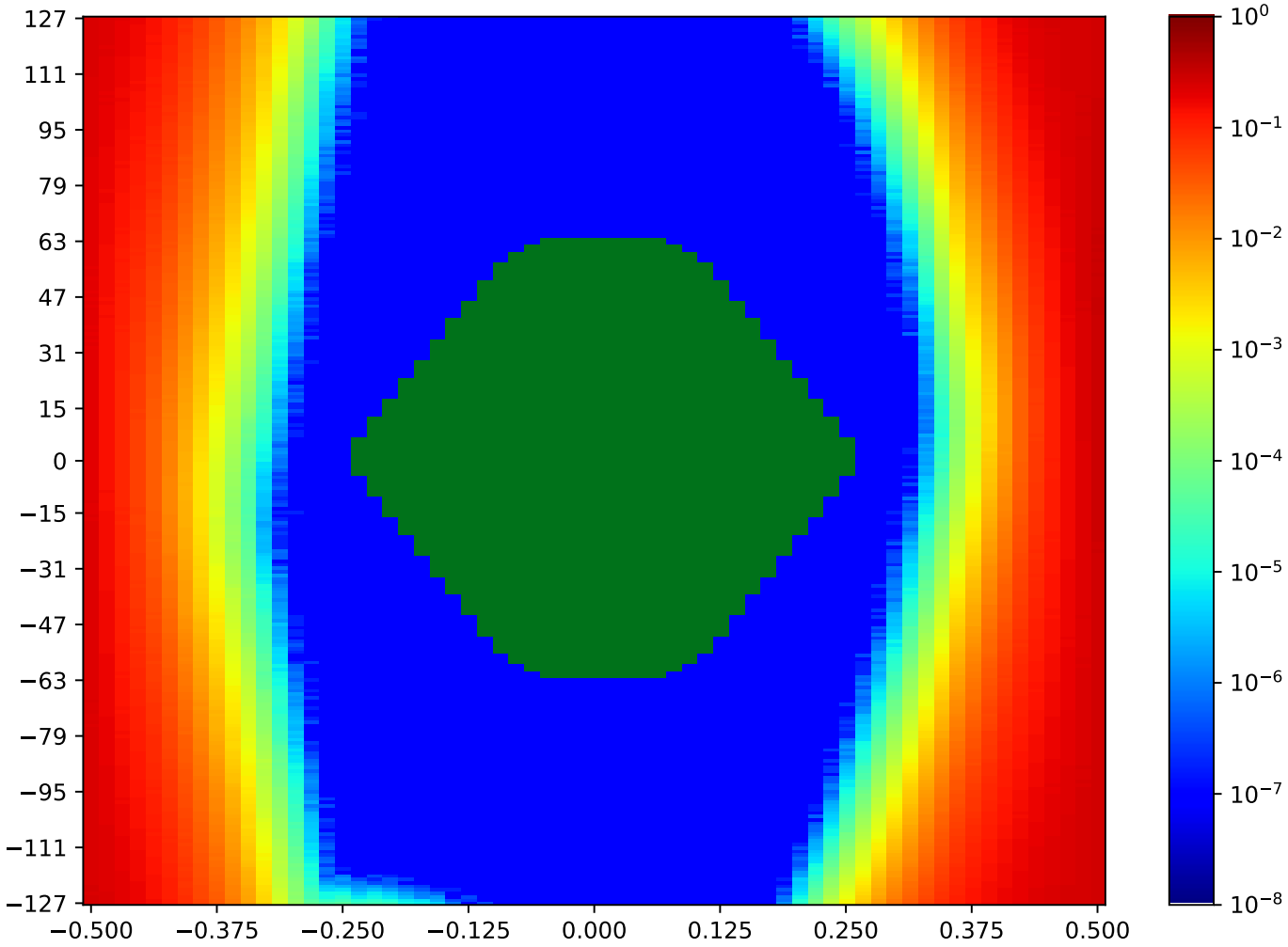


Figure 6.222: MSP_C_FPGA-TX3-07–RX1-07-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.9 MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Table 6.206: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:12:57		2019-Nov-27 11:13:27	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	10238	45	69.23%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

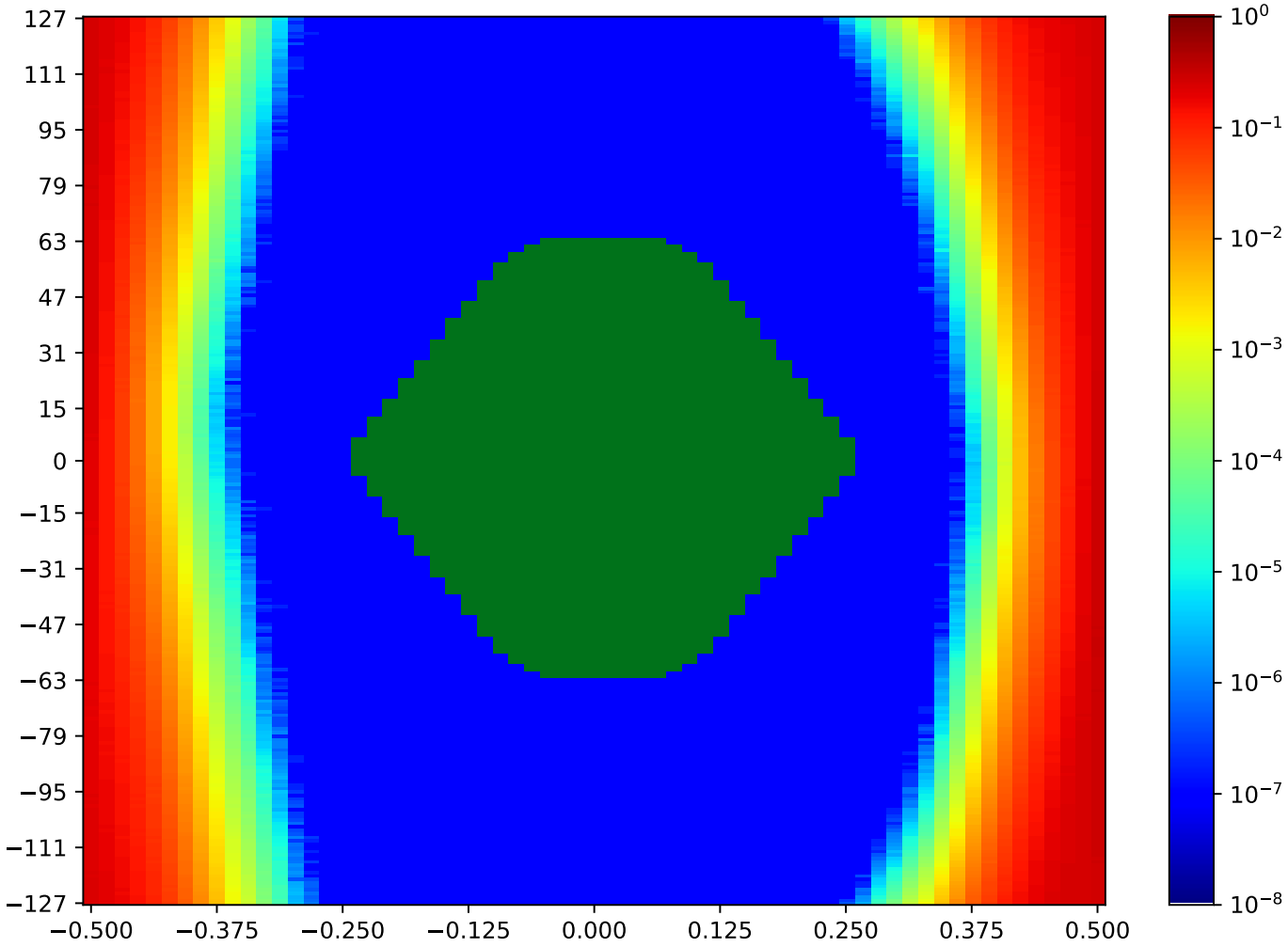


Figure 6.223: MSP_C_FPGA-TX3-08–RX1-08-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.10 MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Table 6.207: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:10:11		2019-Nov-27 11:10:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9281	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

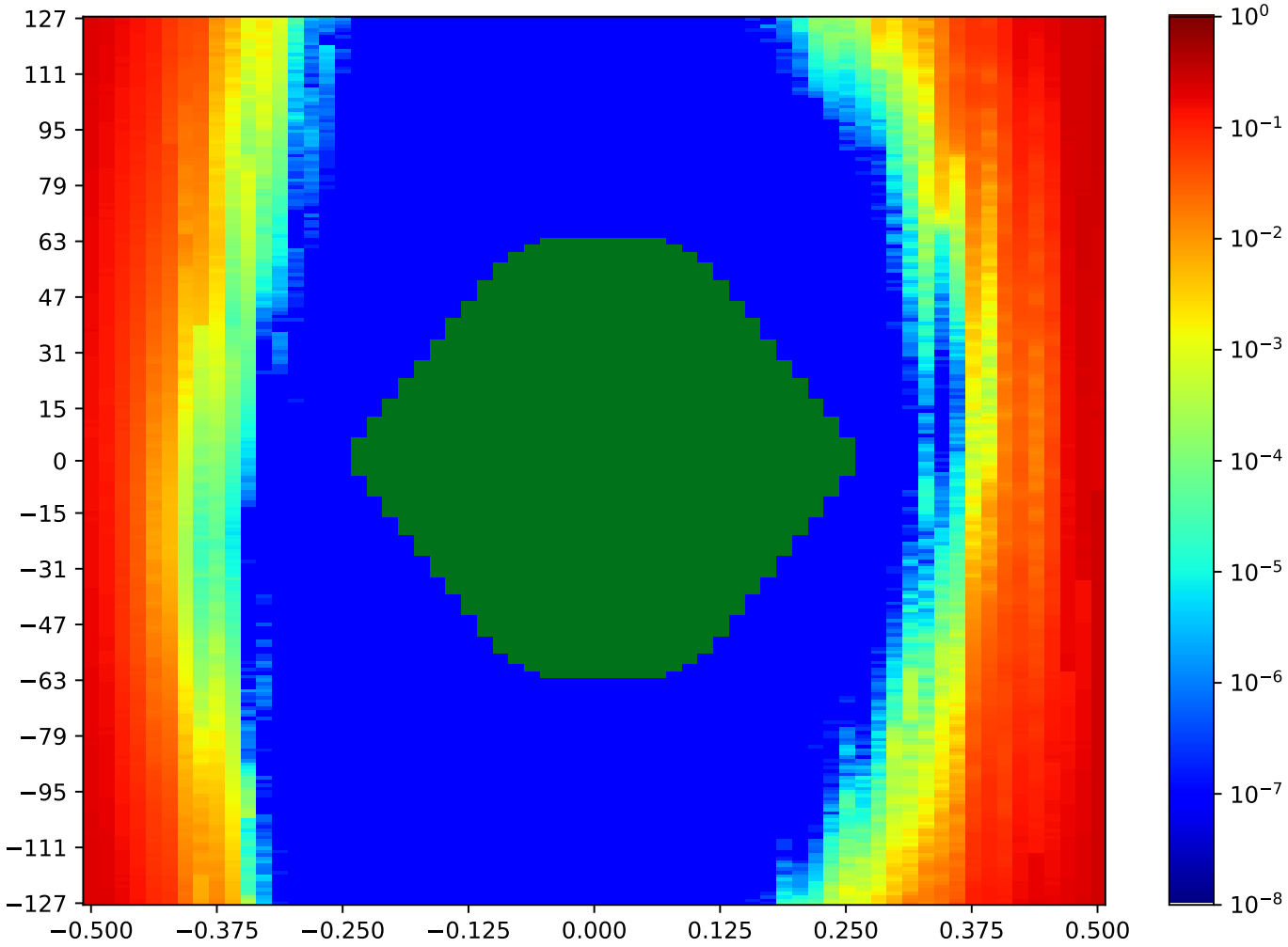


Figure 6.224: MSP_C_FPGA-TX3-09–RX1-09-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.11 MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Table 6.208: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:12:02		2019-Nov-27 11:12:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7537	34	52.31%	255	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

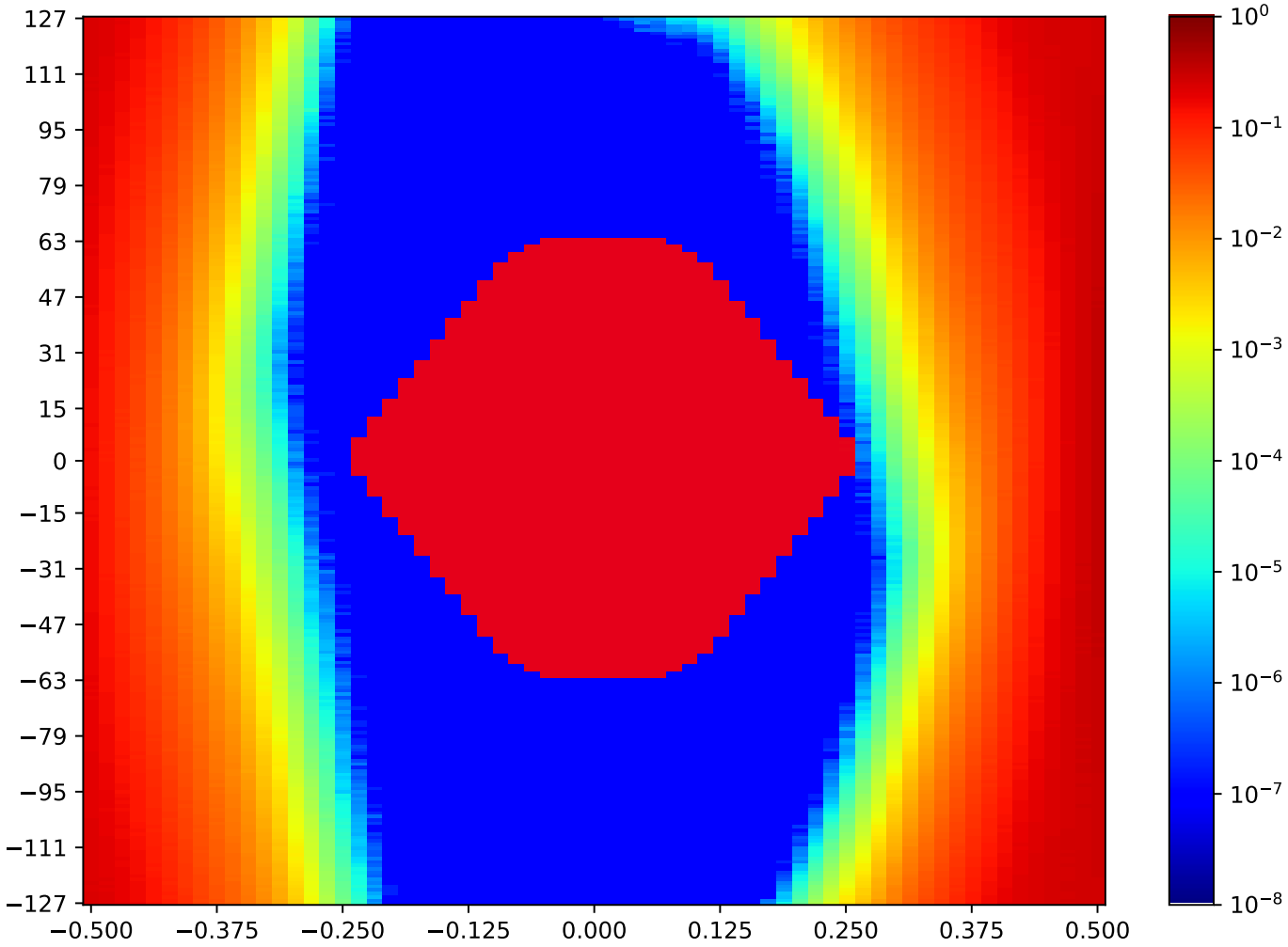


Figure 6.225: MSP_C_FPGA-TX3-10–RX1-10-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.17.12 MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Table 6.209: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:11:34		2019-Nov-27 11:12:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8775	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

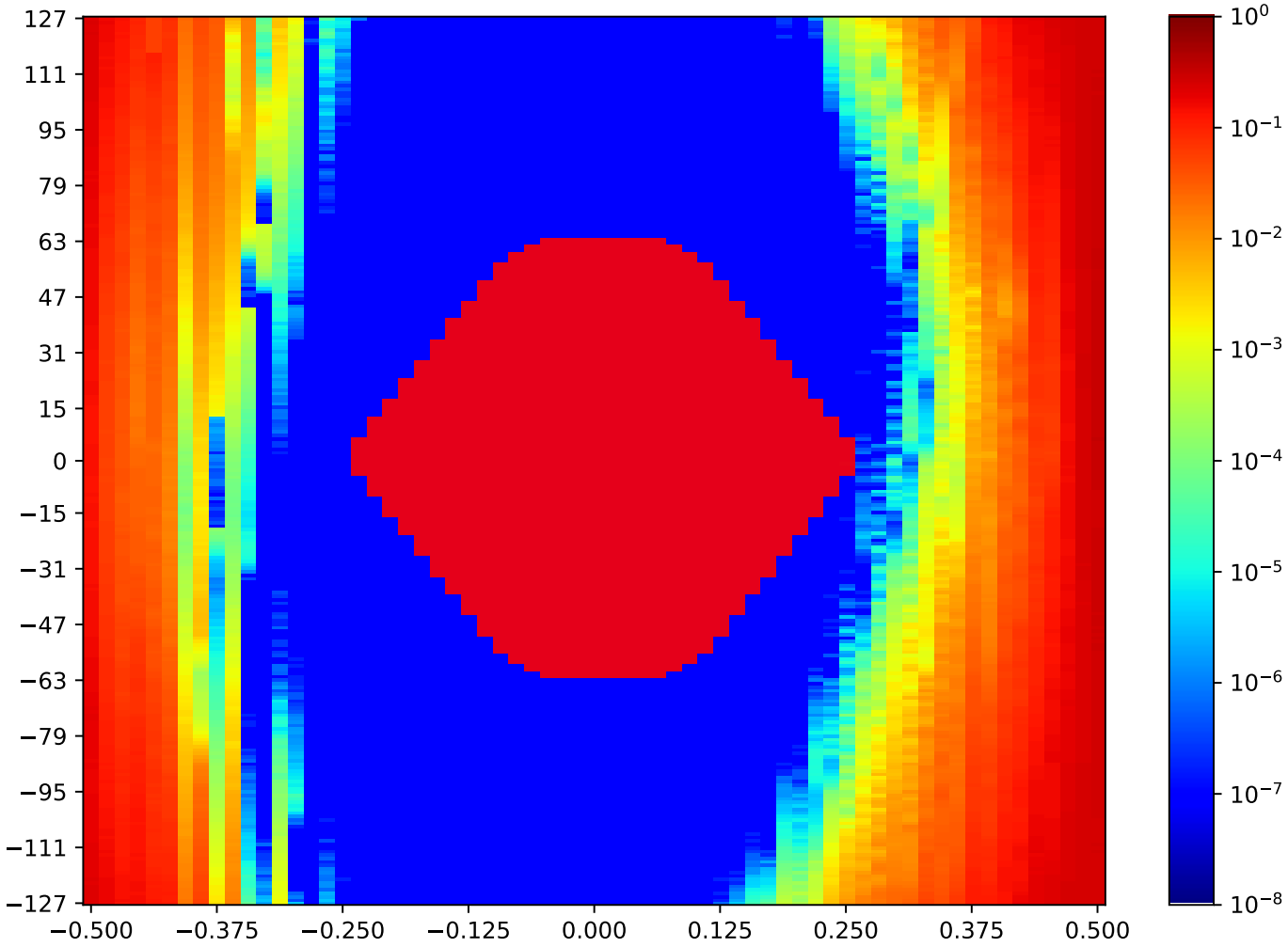


Figure 6.226: MSP_C_FPGA-TX3-11–RX1-11-MSP_A_FPGA

Call back to summary Figure 6.214. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18 MSP_C TX4 MSP_A RX2 Minipod Loopback

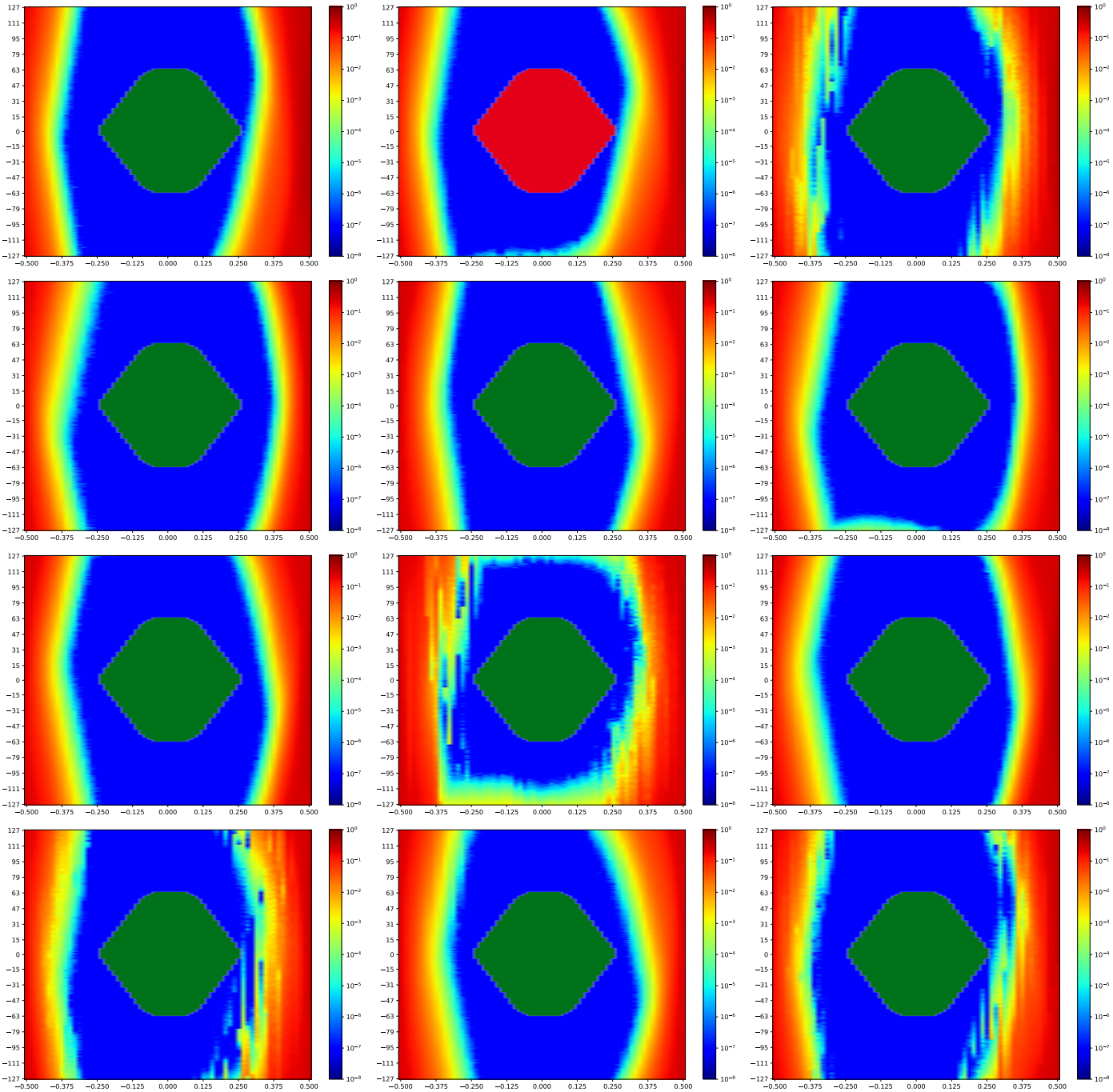


Figure 6.227: MSP_C TX4 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.240.

6.18.1 MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Table 6.210: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:15:07		2019-Nov-27 11:15:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9208	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

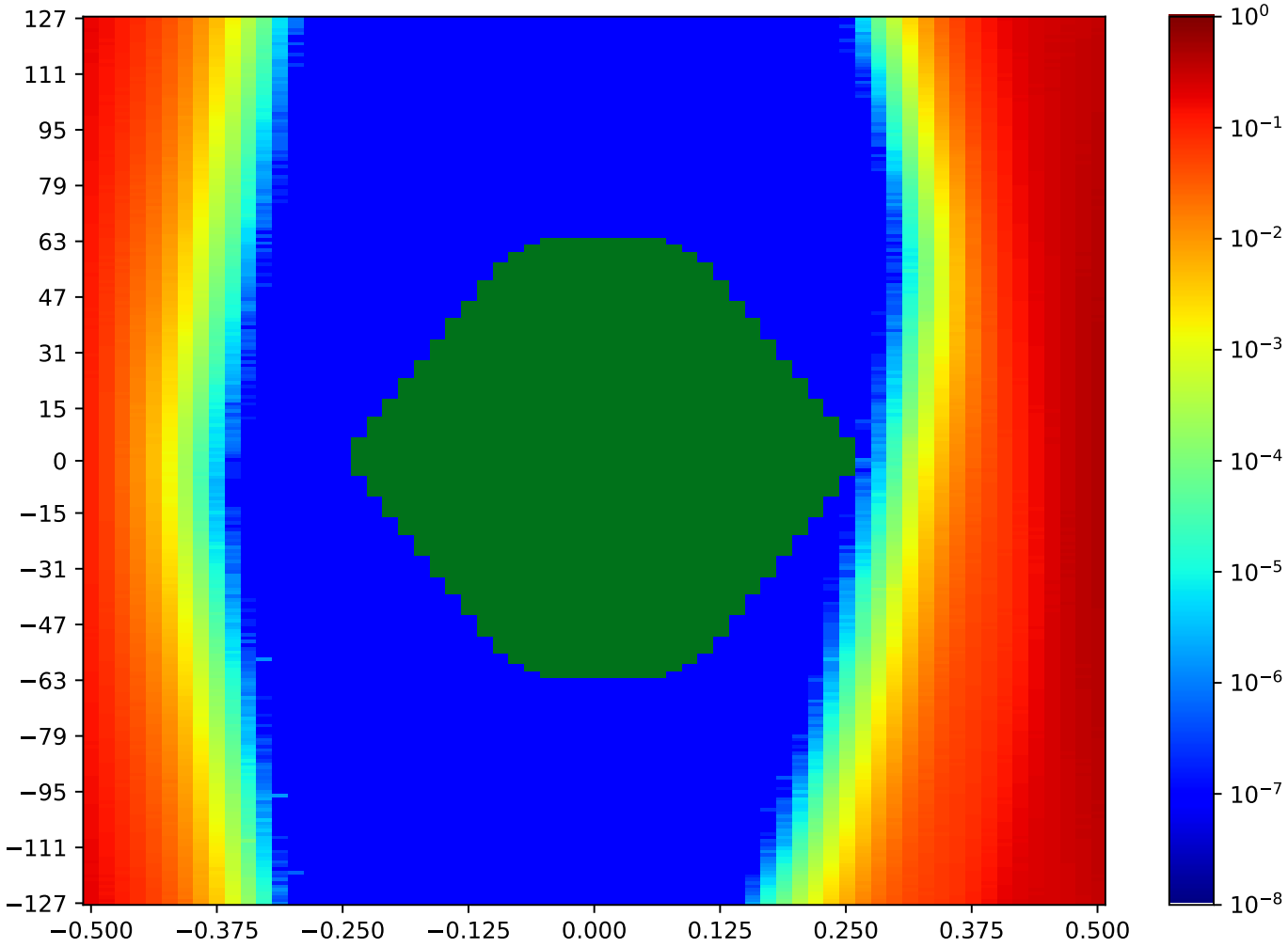


Figure 6.228: MSP_C_FPGA-TX4-00–RX2-00-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.2 MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Table 6.211: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:14:14		2019-Nov-27 11:14:38	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8509	37	56.92%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

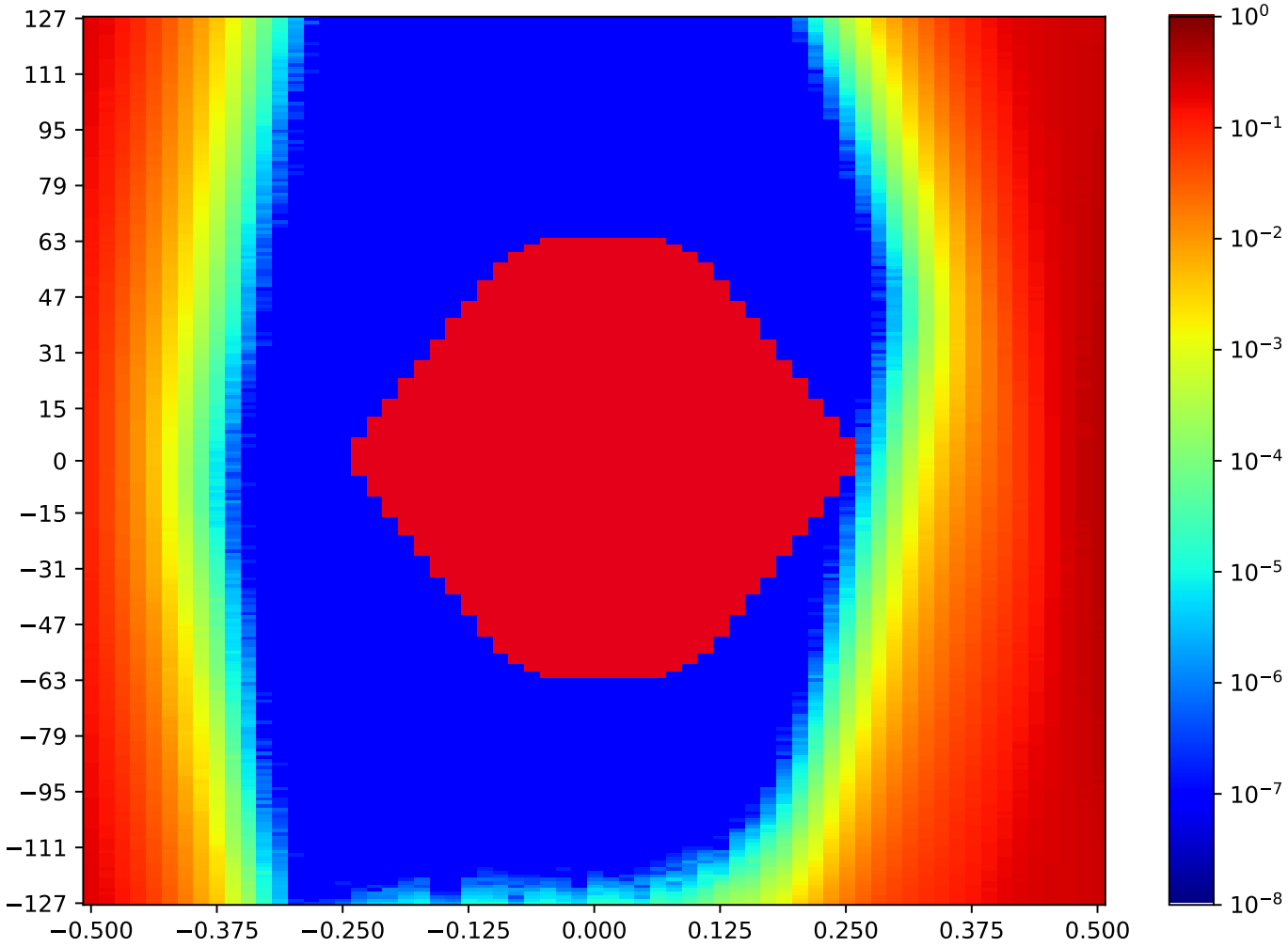


Figure 6.229: MSP_C_FPGA-TX4-01–RX2-01-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.3 MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Table 6.212: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:16:29		2019-Nov-27 11:16:48	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8362	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

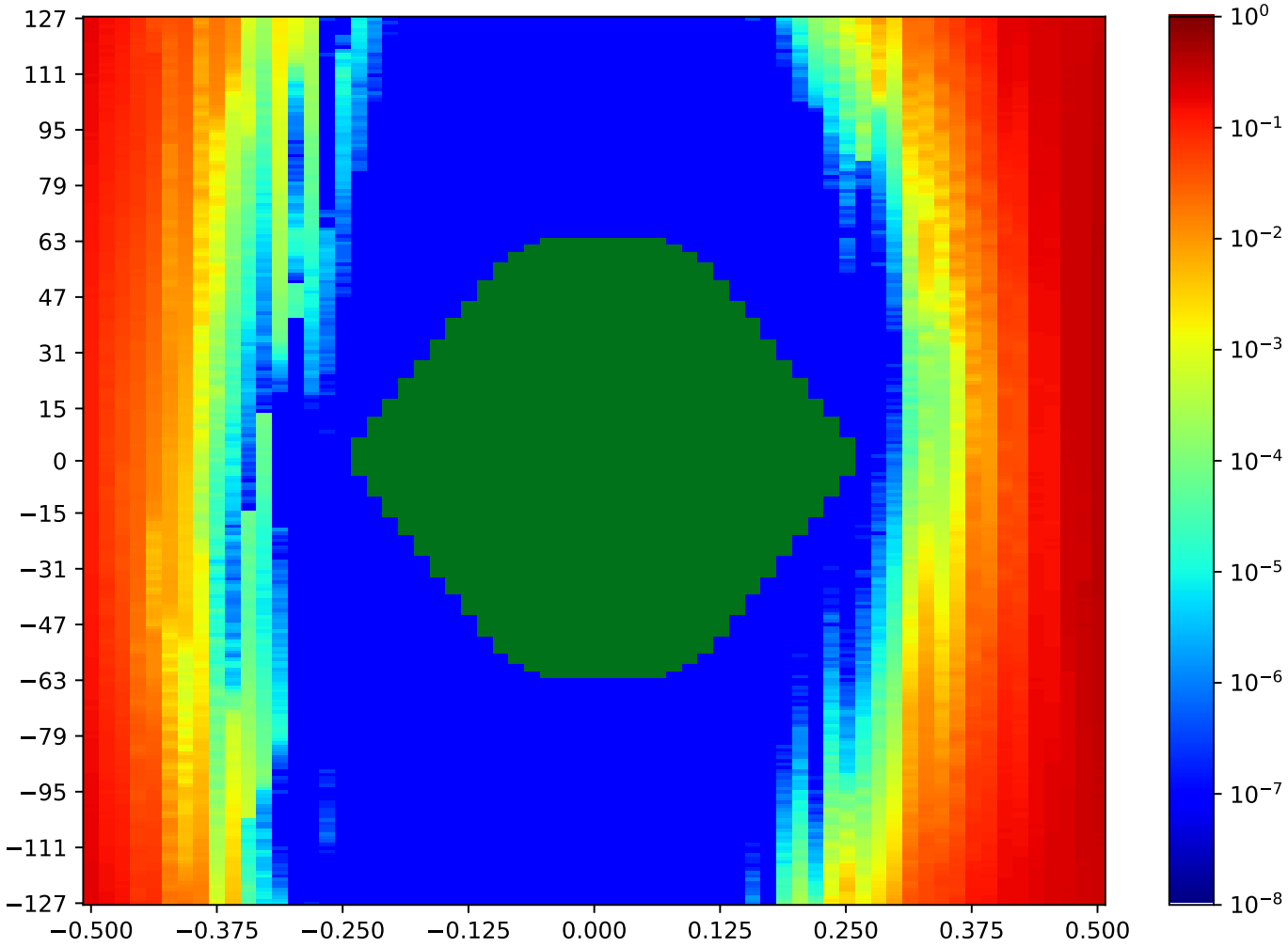


Figure 6.230: MSP_C_FPGA-TX4-02–RX2-02-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.4 MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Table 6.213: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:13:55		2019-Nov-27 11:14:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9714	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

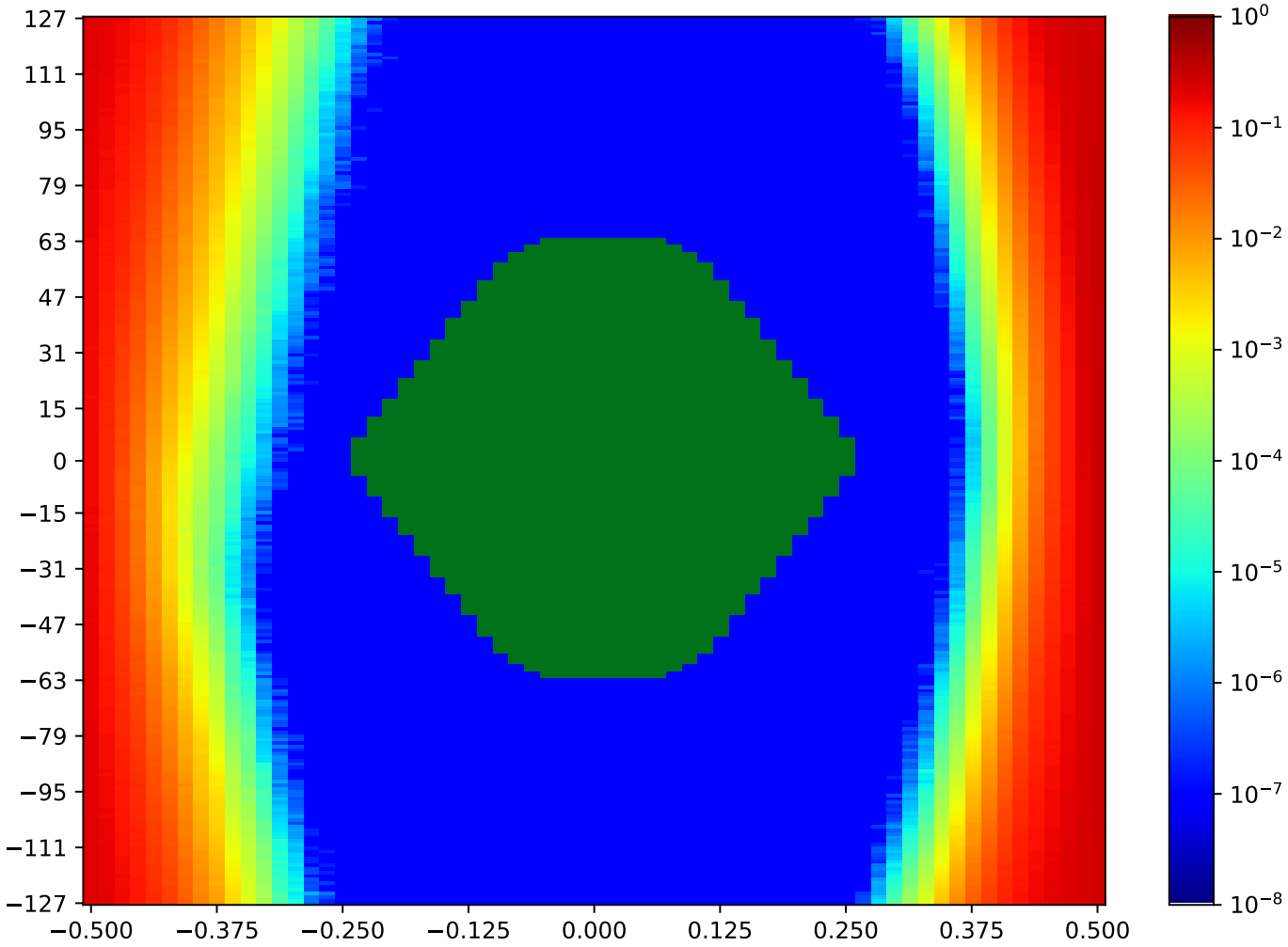


Figure 6.231: MSP_C_FPGA-TX4-03–RX2-03-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.5 MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Table 6.214: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:17:45		2019-Nov-27 11:18:11	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8719	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

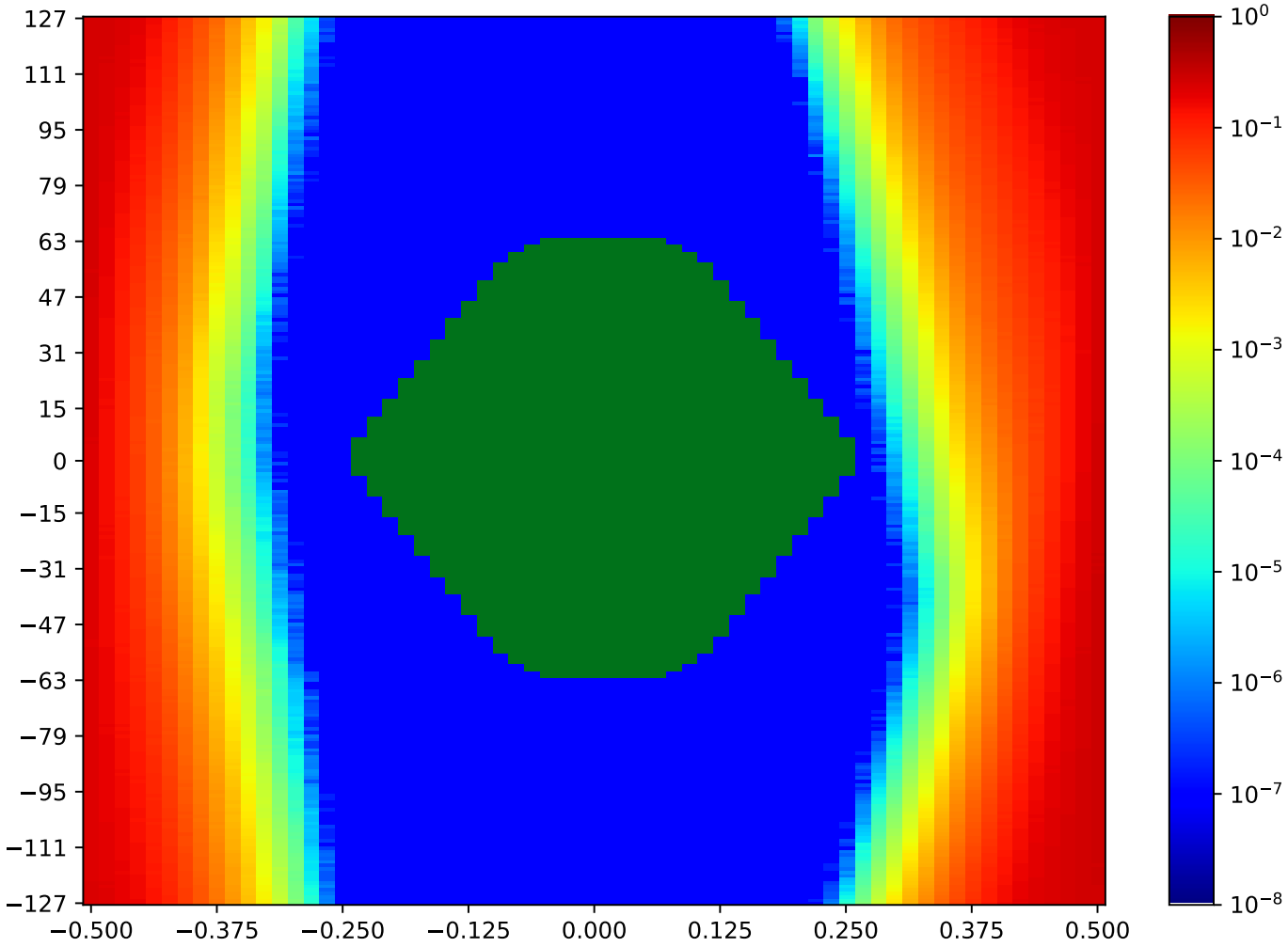


Figure 6.232: MSP_C_FPGA-TX4-04–RX2-04-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.6 MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Table 6.215: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:14:38		2019-Nov-27 11:15:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9196	42	64.62%	245	95.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

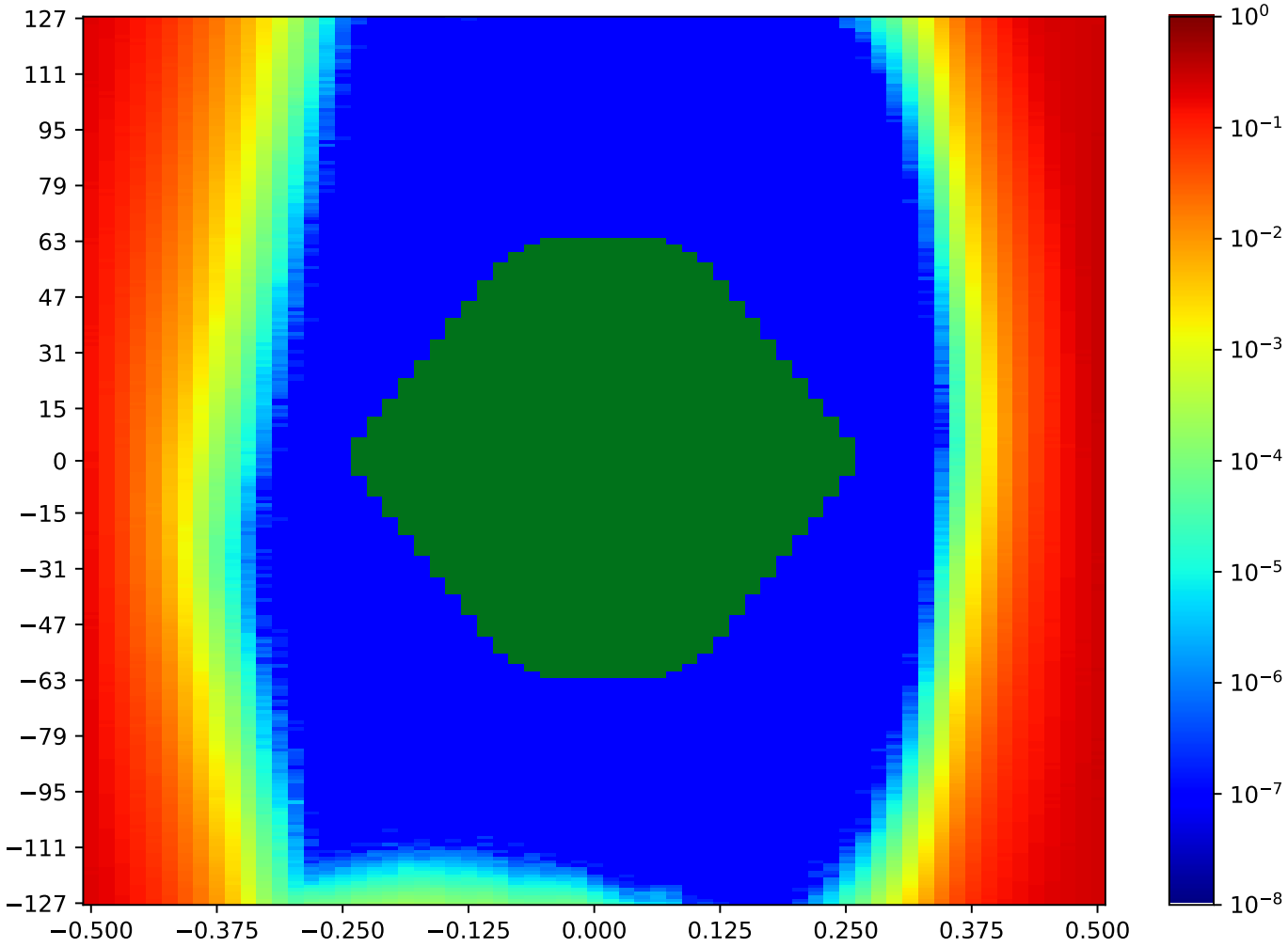


Figure 6.233: MSP_C_FPGA-TX4-05–RX2-05-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.7 MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Table 6.216: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:18:39		2019-Nov-27 11:19:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9317	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

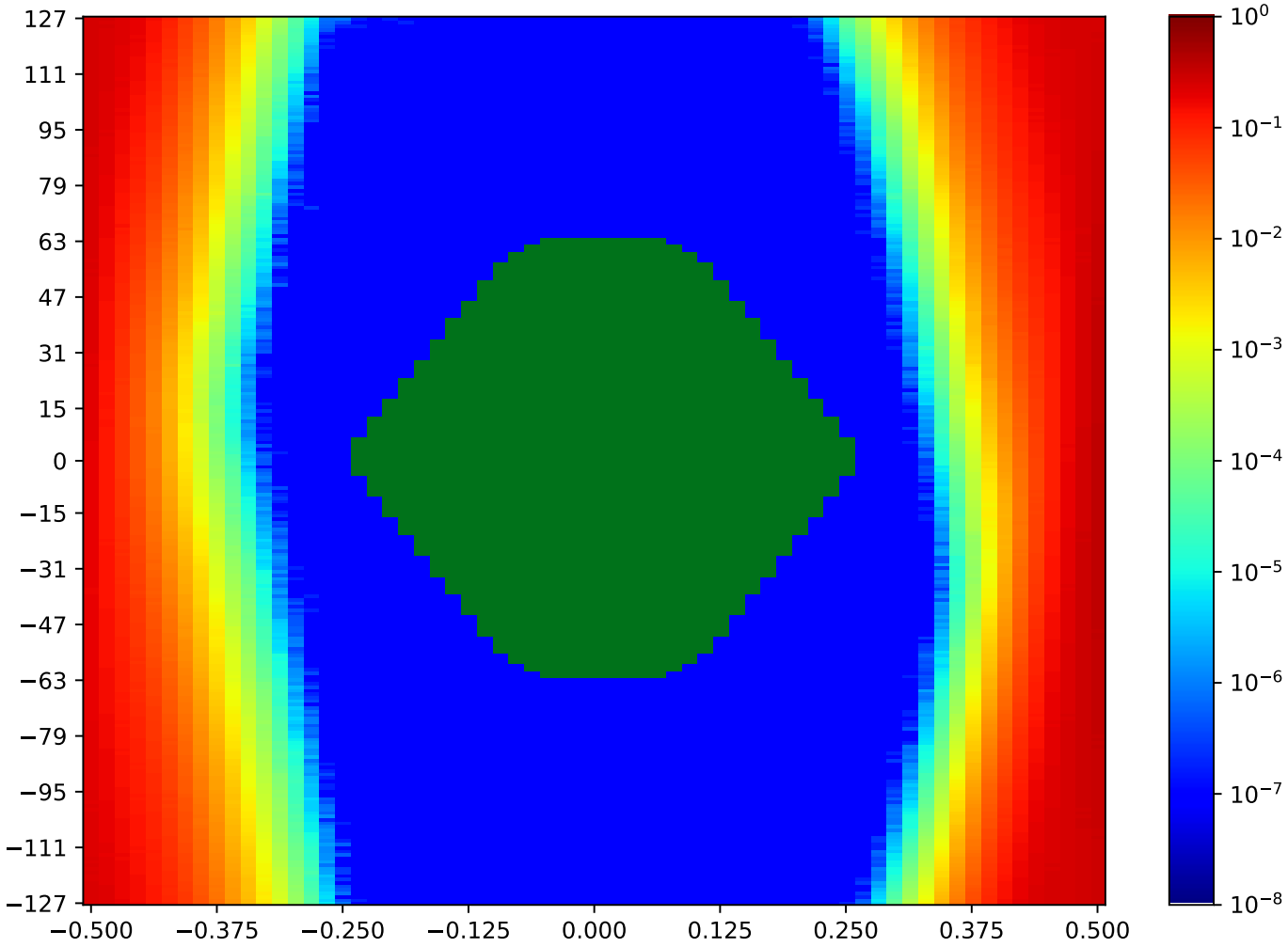


Figure 6.234: MSP_C_FPGA-TX4-06–RX2-06-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.8 MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Table 6.217: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:15:35		2019-Nov-27 11:16:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7104	40	58.46%	224	87.45%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

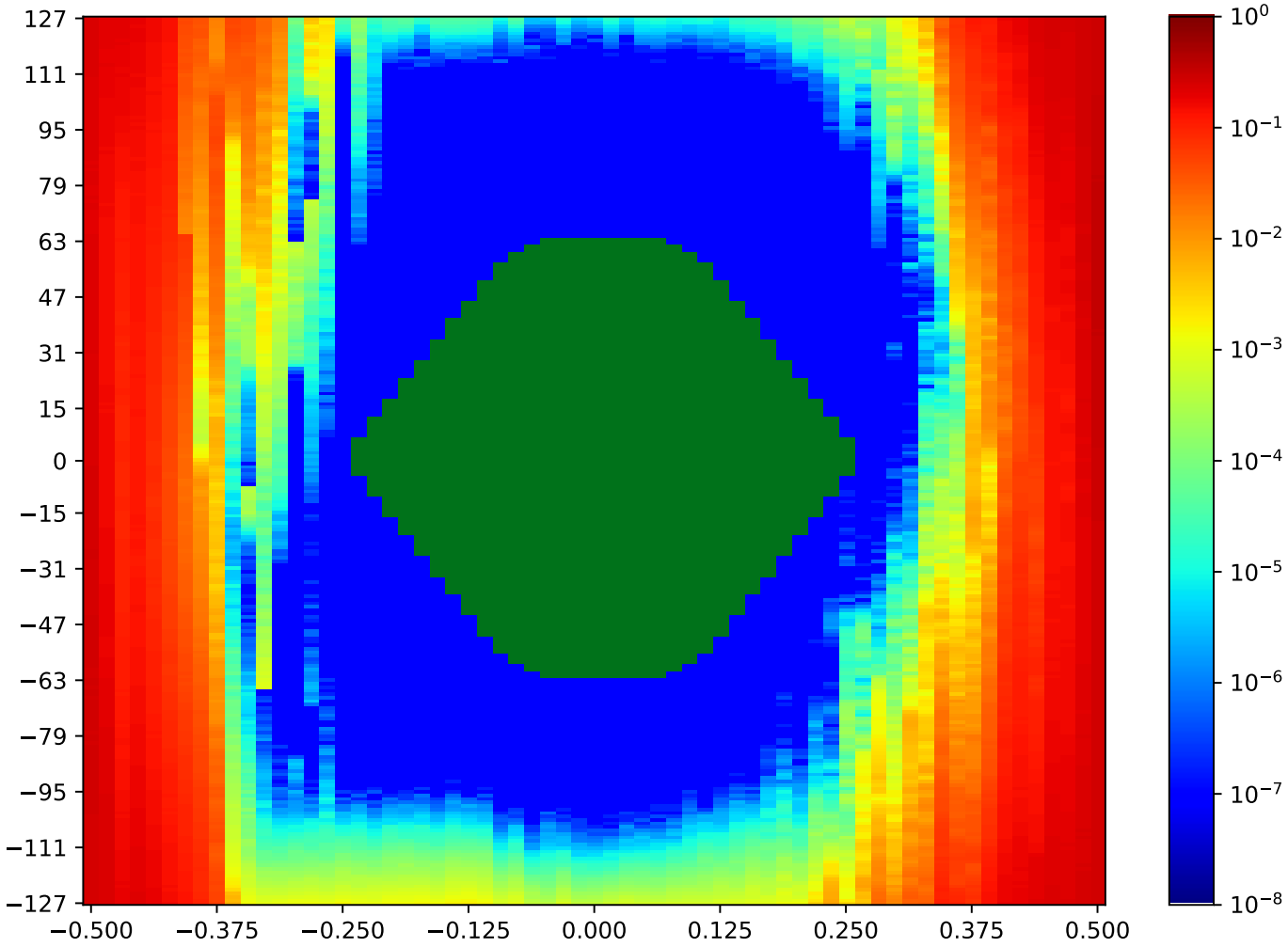


Figure 6.235: MSP_C_FPGA-TX4-07–RX2-07-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.9 MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Table 6.218: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:18:12		2019-Nov-27 11:18:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9331	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

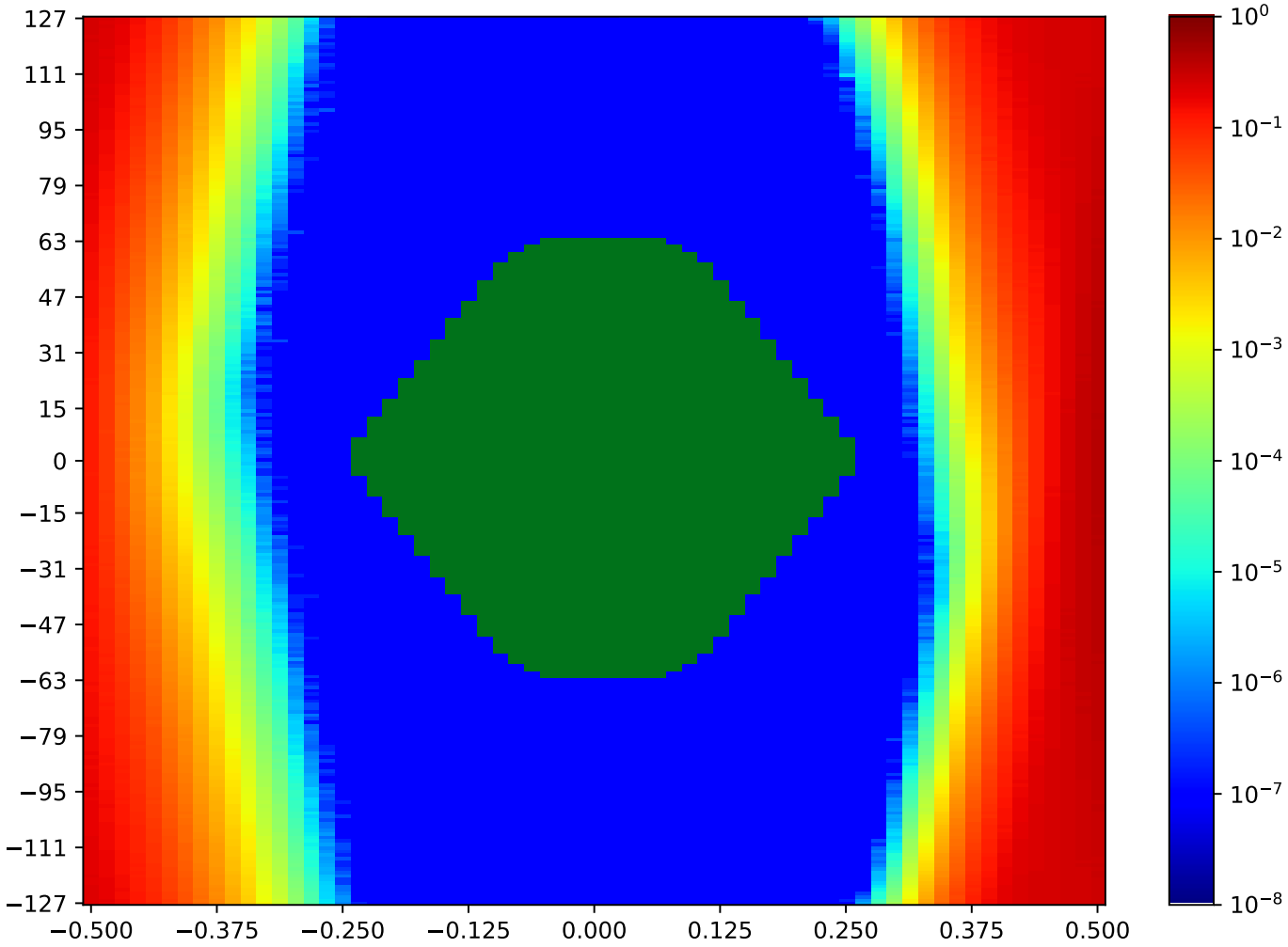


Figure 6.236: MSP_C_FPGA-TX4-08–RX2-08-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.10 MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Table 6.219: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:16:01		2019-Nov-27 11:16:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8901	40	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

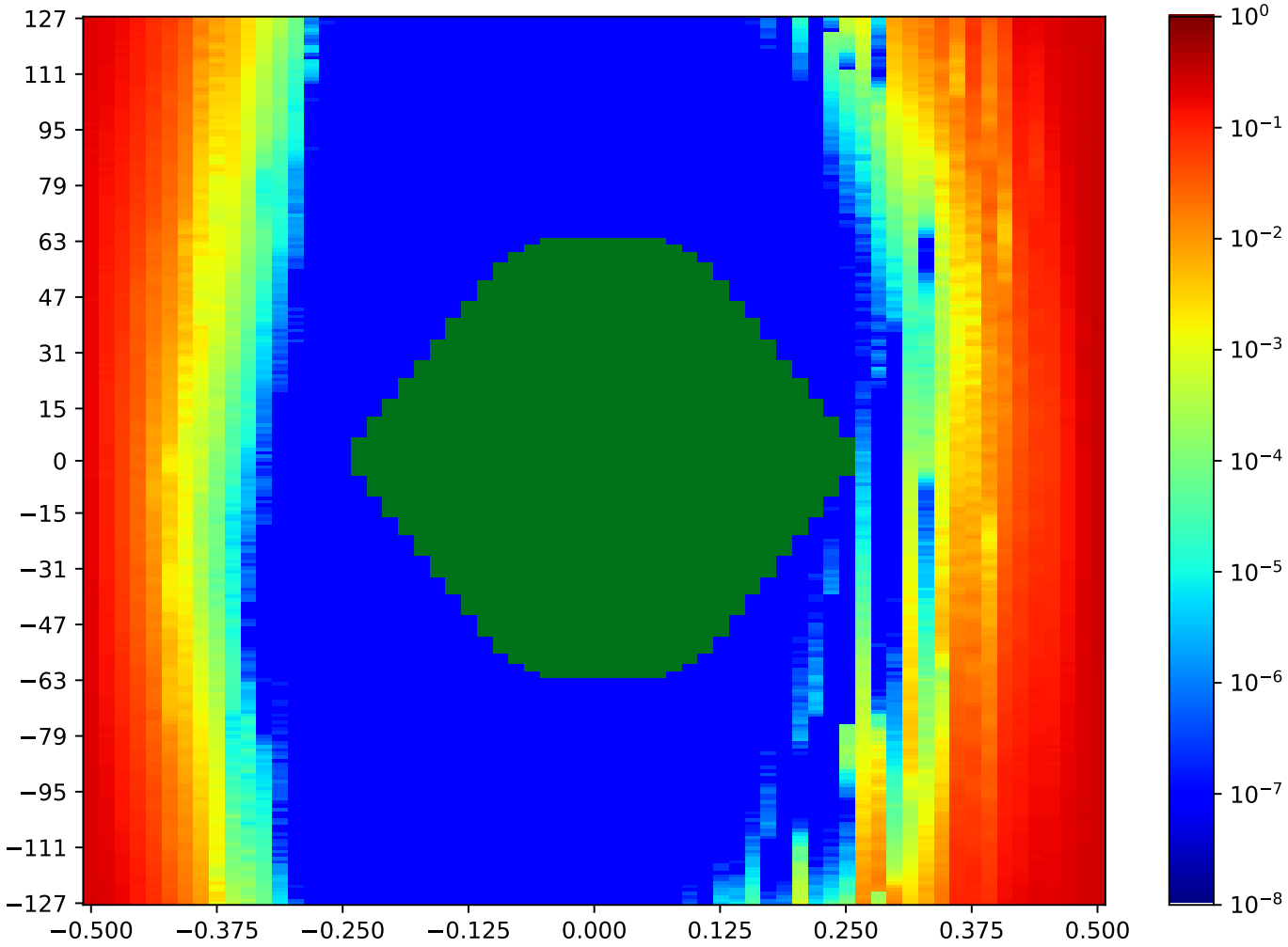


Figure 6.237: MSP_C_FPGA-TX4-09–RX2-09-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.11 MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Table 6.220: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:17:17		2019-Nov-27 11:17:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8590	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

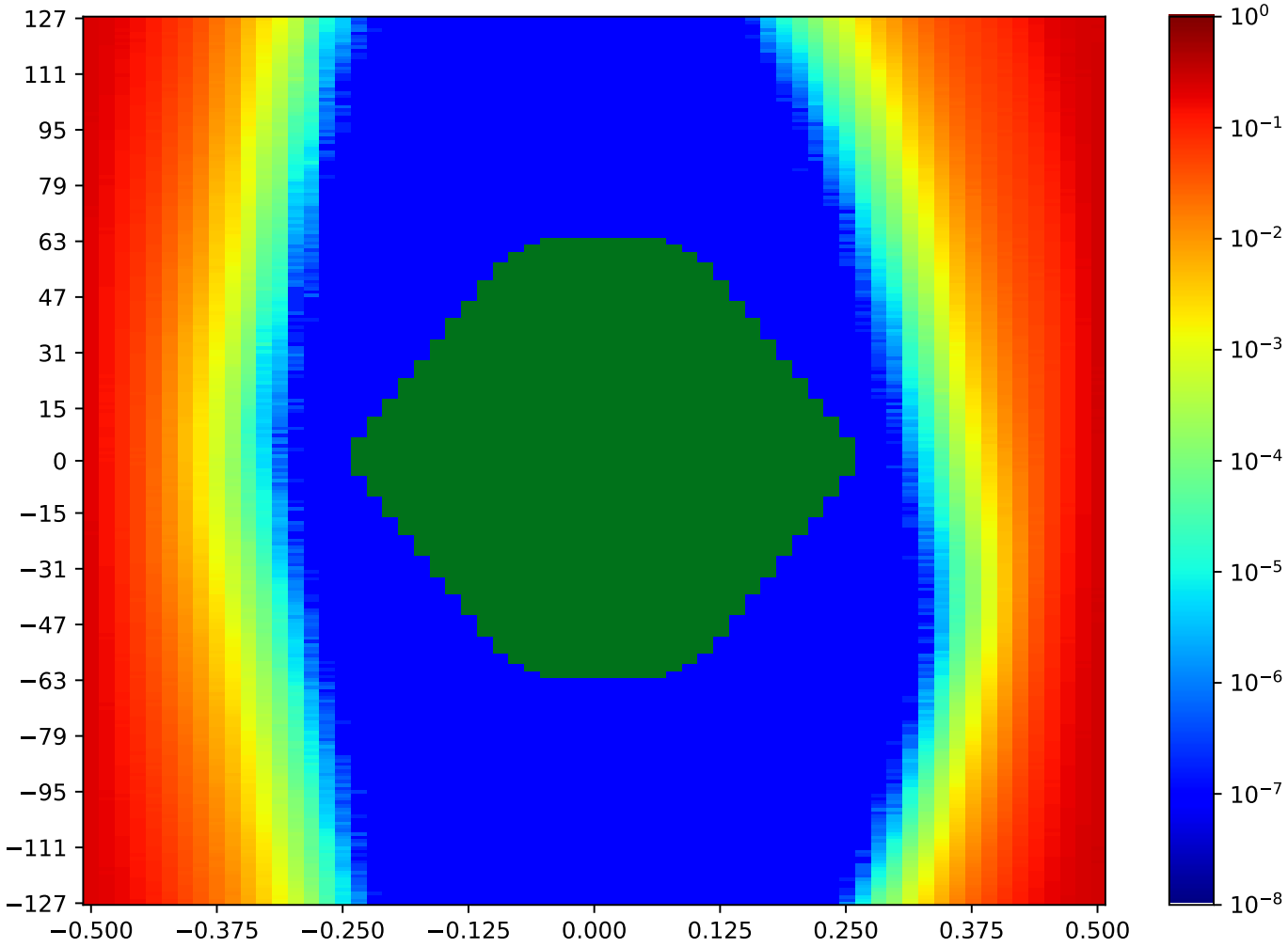


Figure 6.238: MSP_C_FPGA-TX4-10–RX2-10-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.18.12 MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Table 6.221: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:16:48		2019-Nov-27 11:17:16	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9192	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

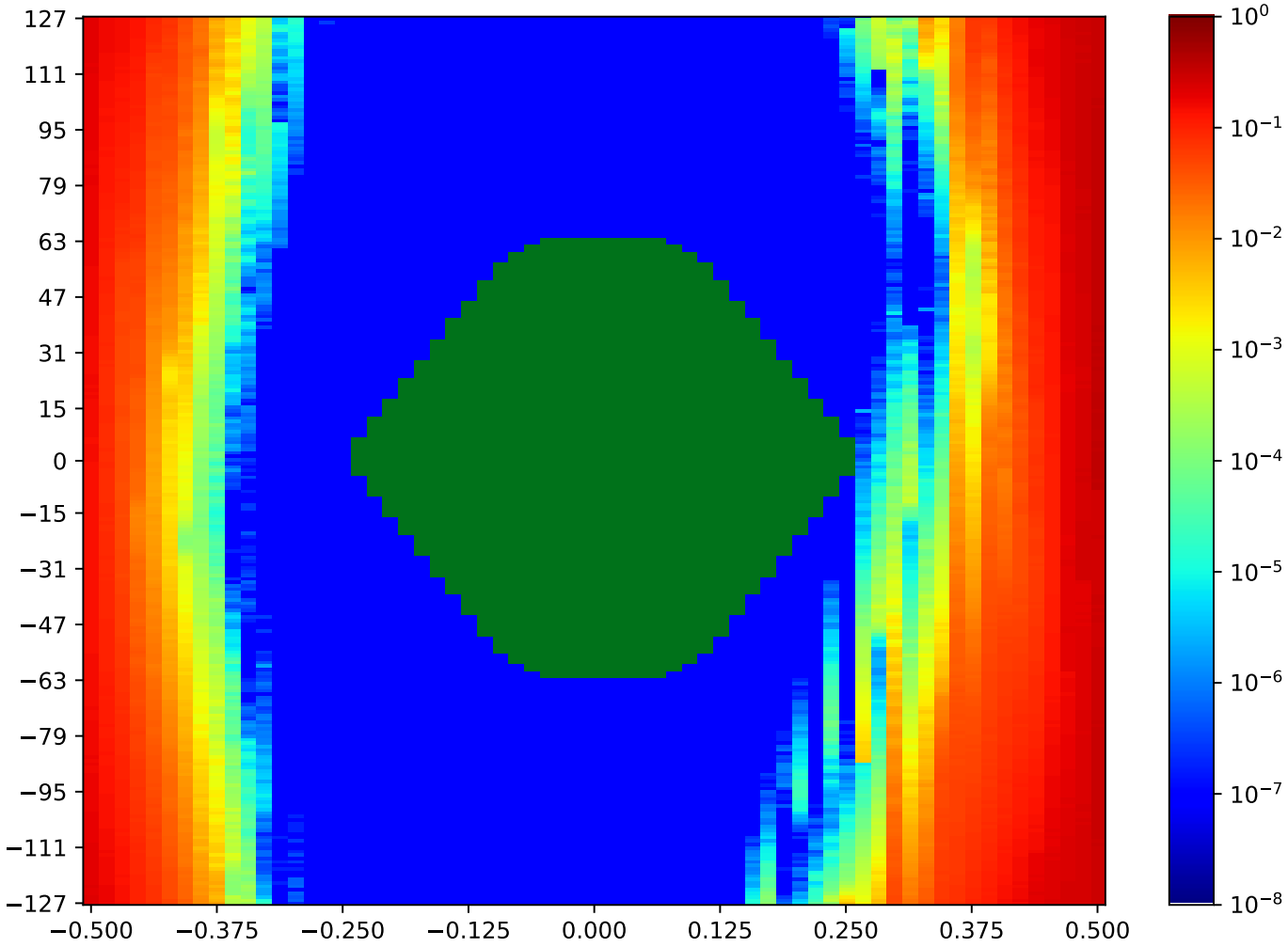


Figure 6.239: MSP_C_FPGA-TX4-11–RX2-11-MSP_A_FPGA

Call back to summary Figure 6.227. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19 MSP_A TX1 MSP_C RX12 Minipod Loopback

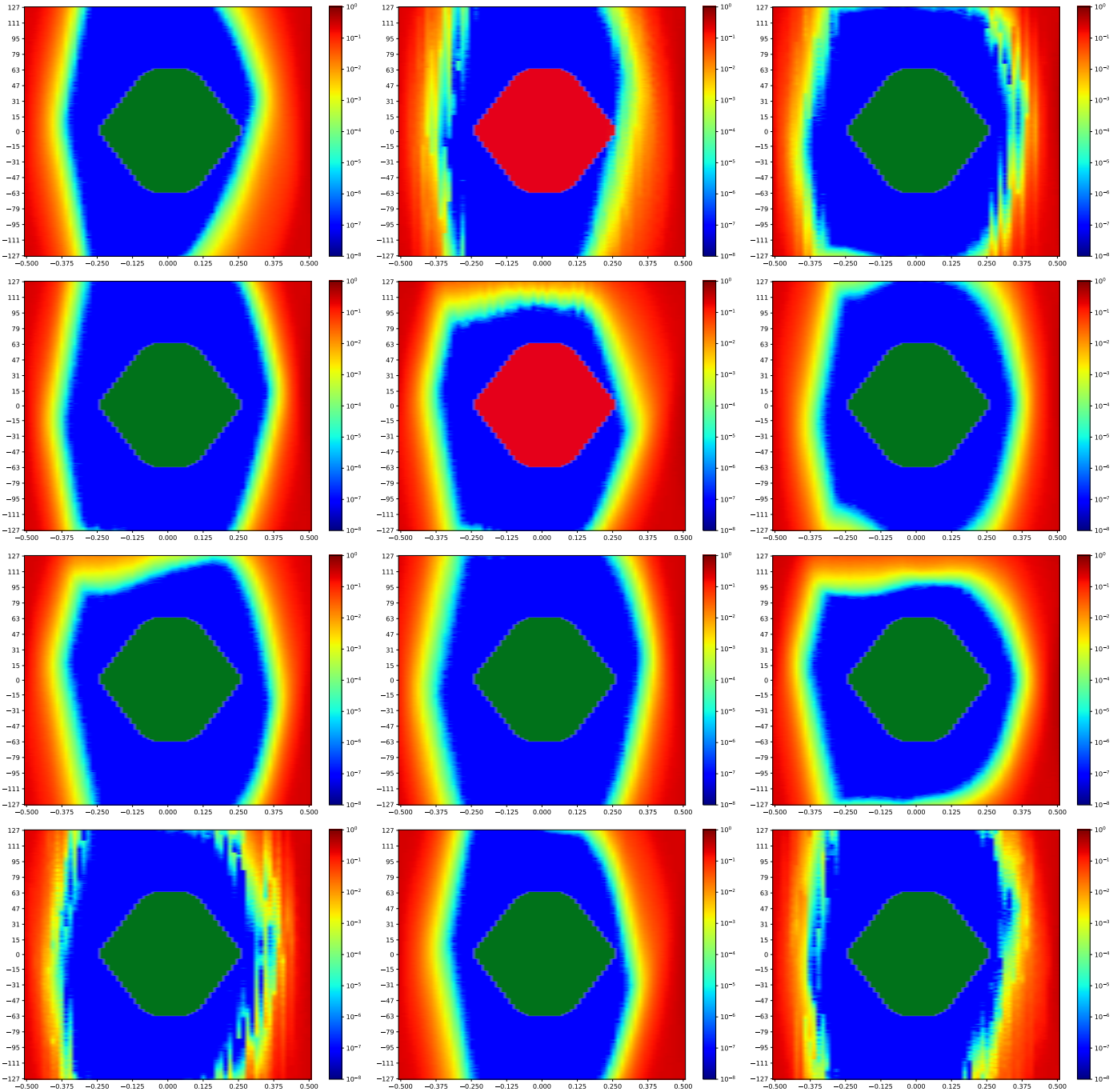


Figure 6.240: MSP_A TX1 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.253.

6.19.1 MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Table 6.222: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:35:04		2019-Nov-27 11:35:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8279	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

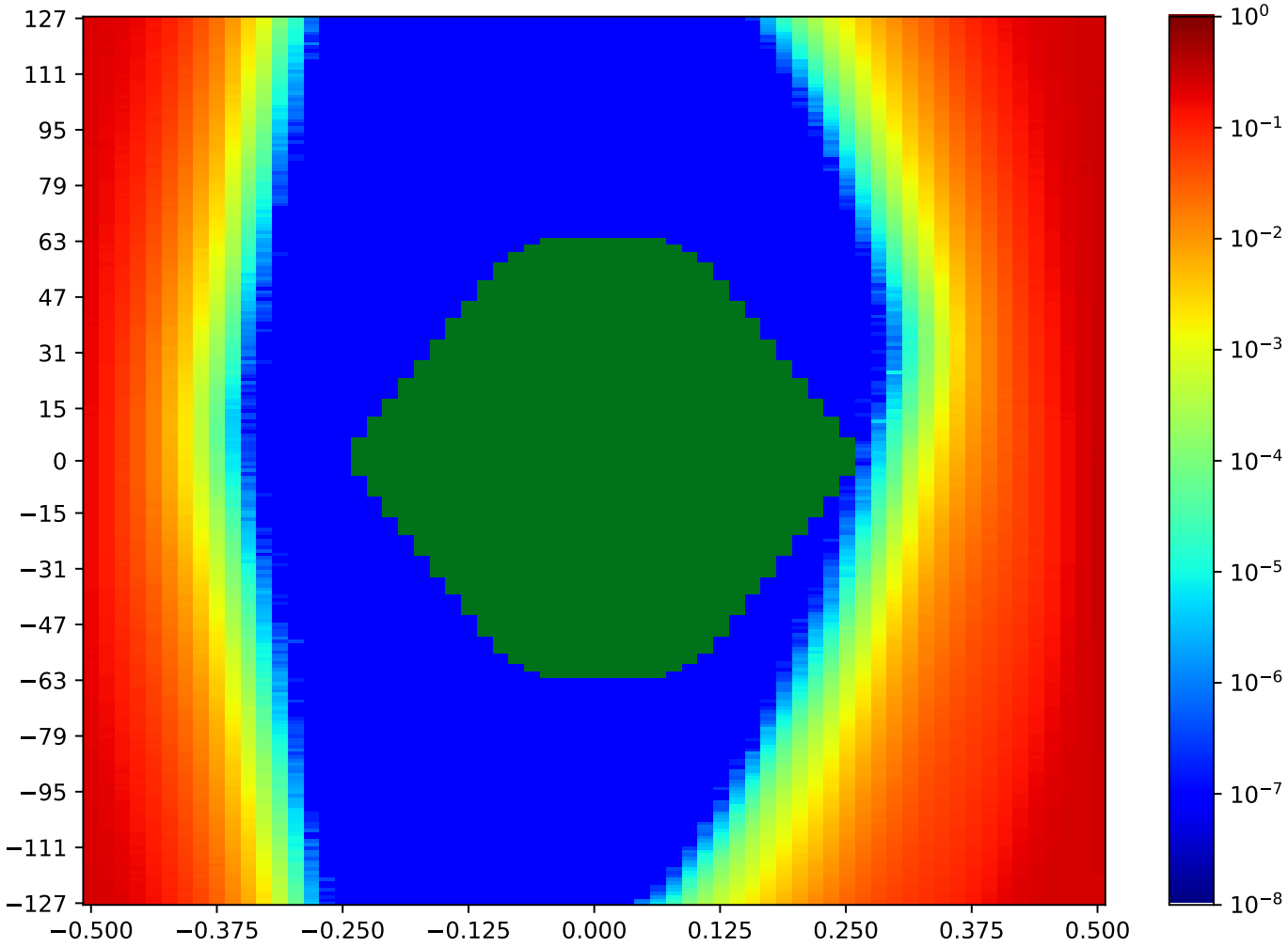


Figure 6.241: MSP_A_FPGA-TX1-00–RX12-00-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.2 MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Table 6.223: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:35:58		2019-Nov-27 11:36:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8063	35	53.85%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

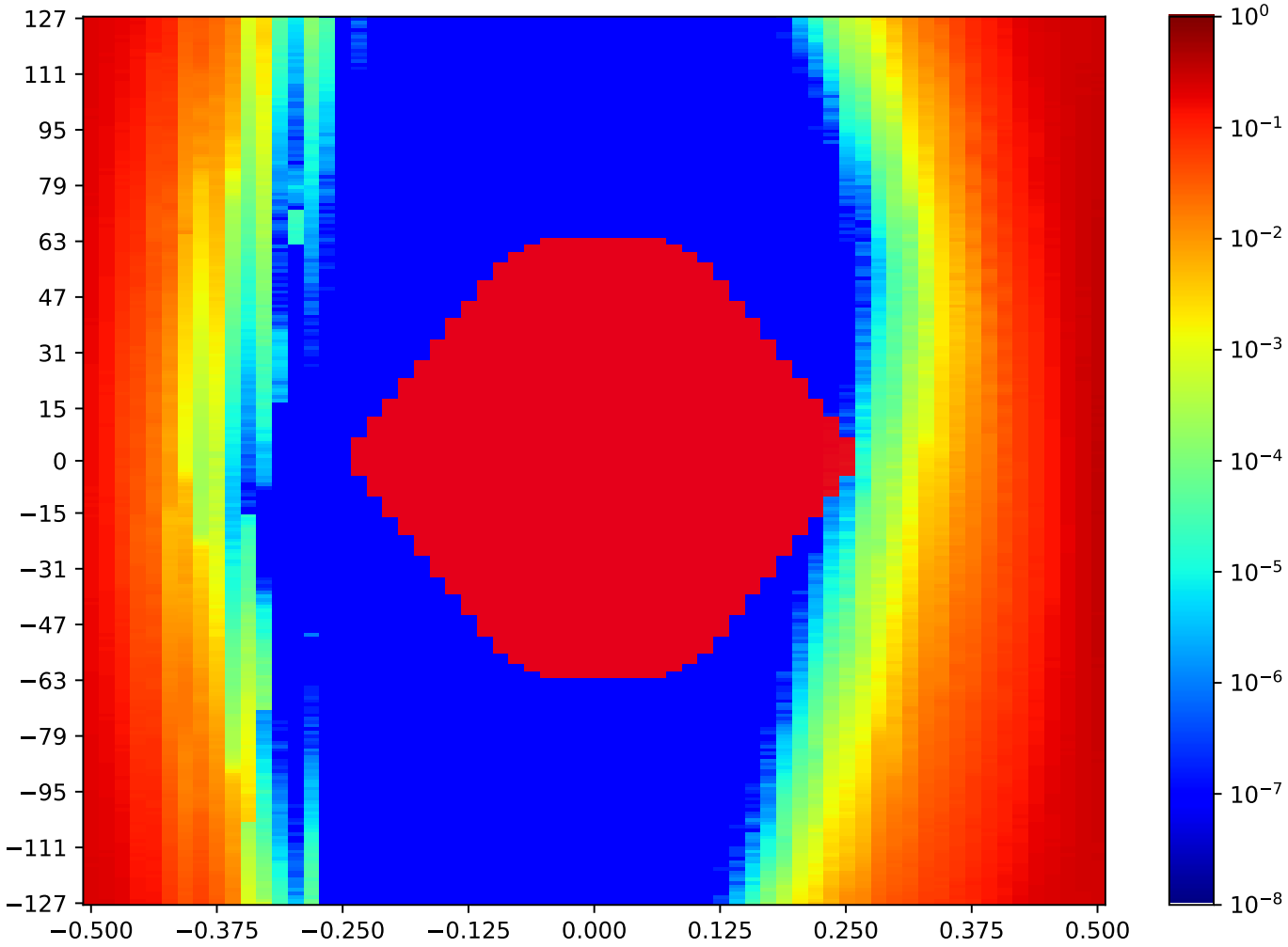


Figure 6.242: MSP_A_FPGA-TX1-01–RX12-01-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.3 MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Table 6.224: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:36:26		2019-Nov-27 11:36:53	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9172	44	66.15%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

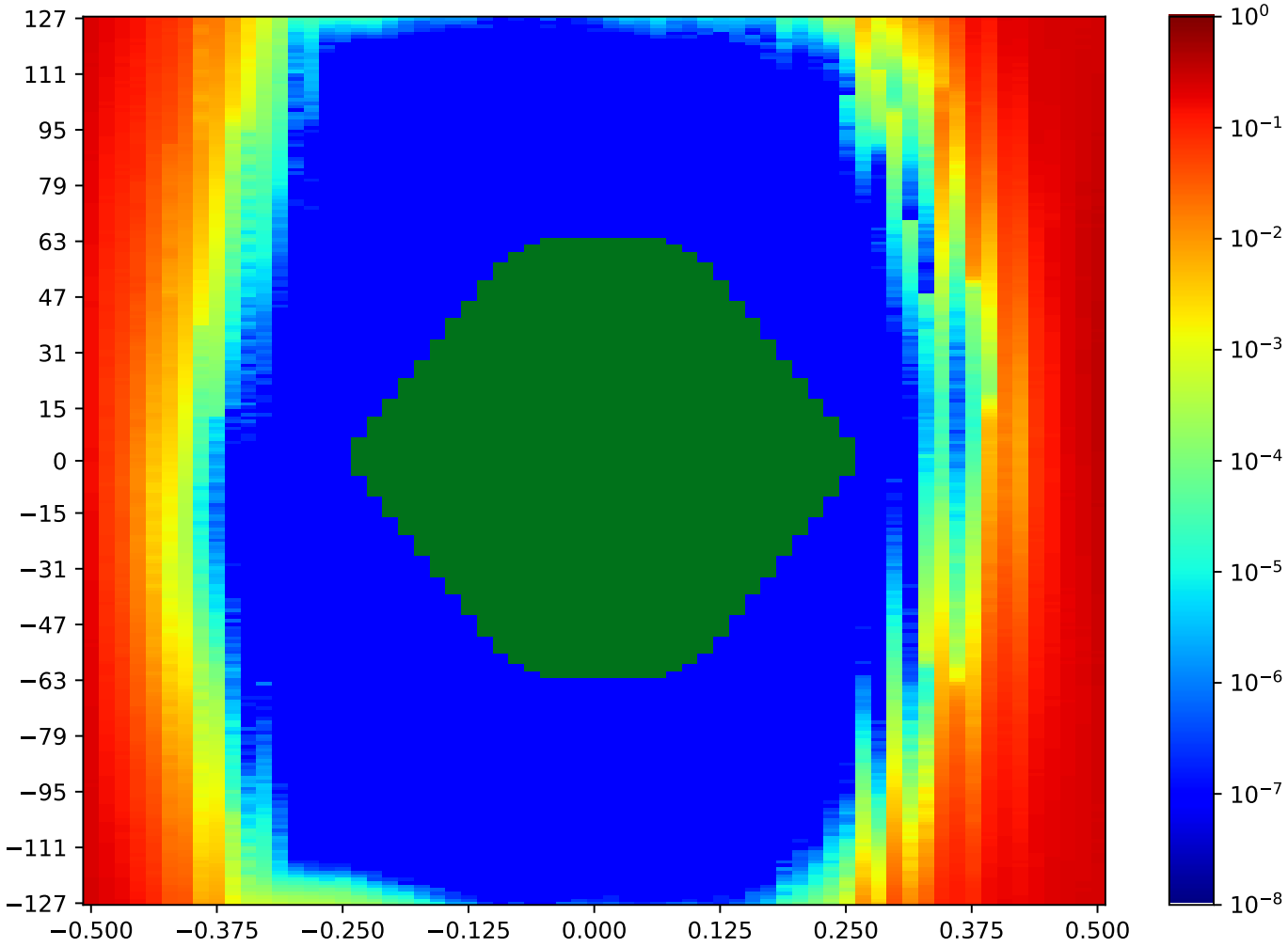


Figure 6.243: MSP_A_FPGA-TX1-02–RX12-02-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.4 MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Table 6.225: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:34:14		2019-Nov-27 11:34:43	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9639	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

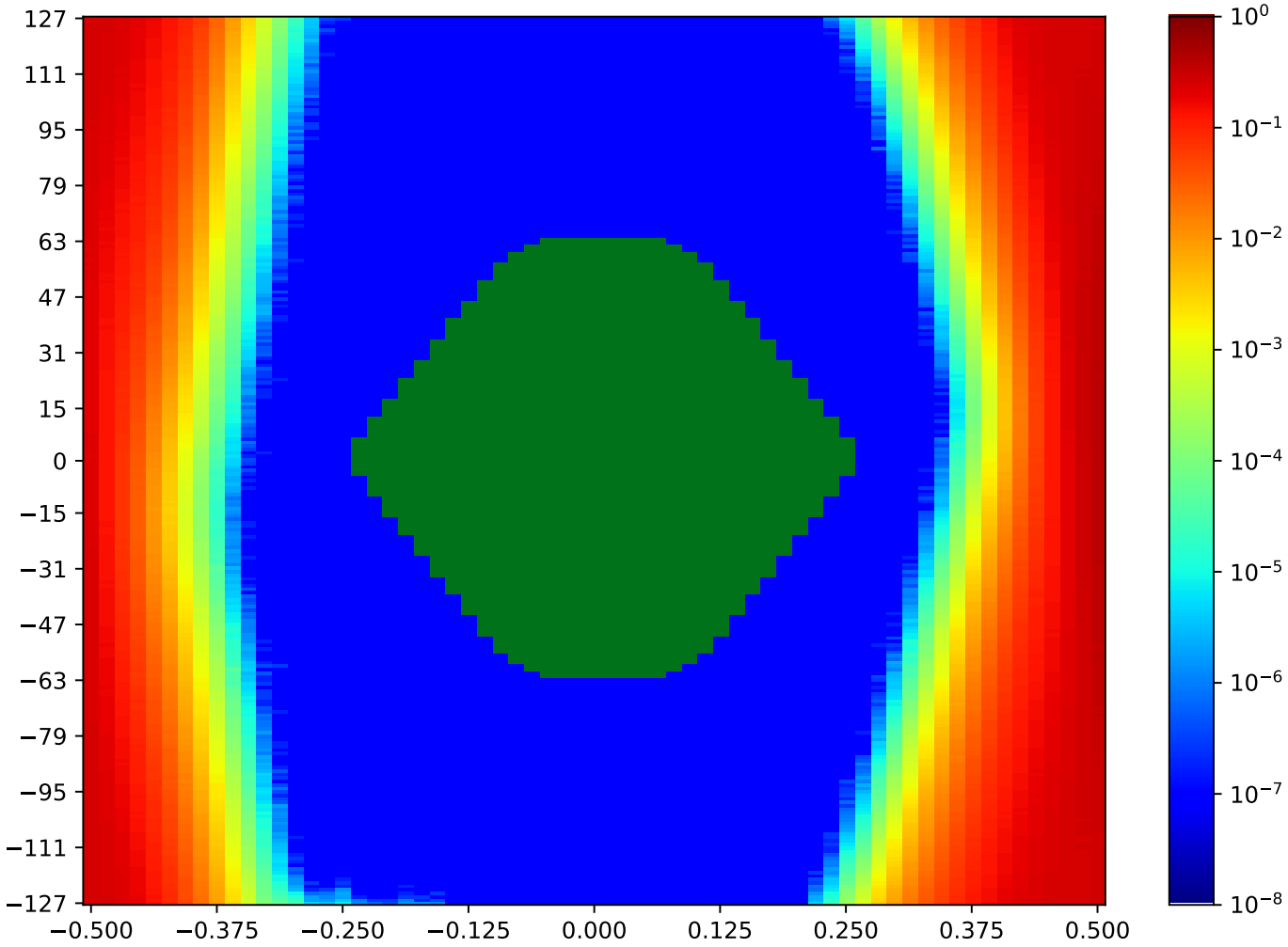


Figure 6.244: MSP_A_FPGA-TX1-03–RX12-03-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.5 MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Table 6.226: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:37:47		2019-Nov-27 11:38:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7207	37	56.92%	225	87.06%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

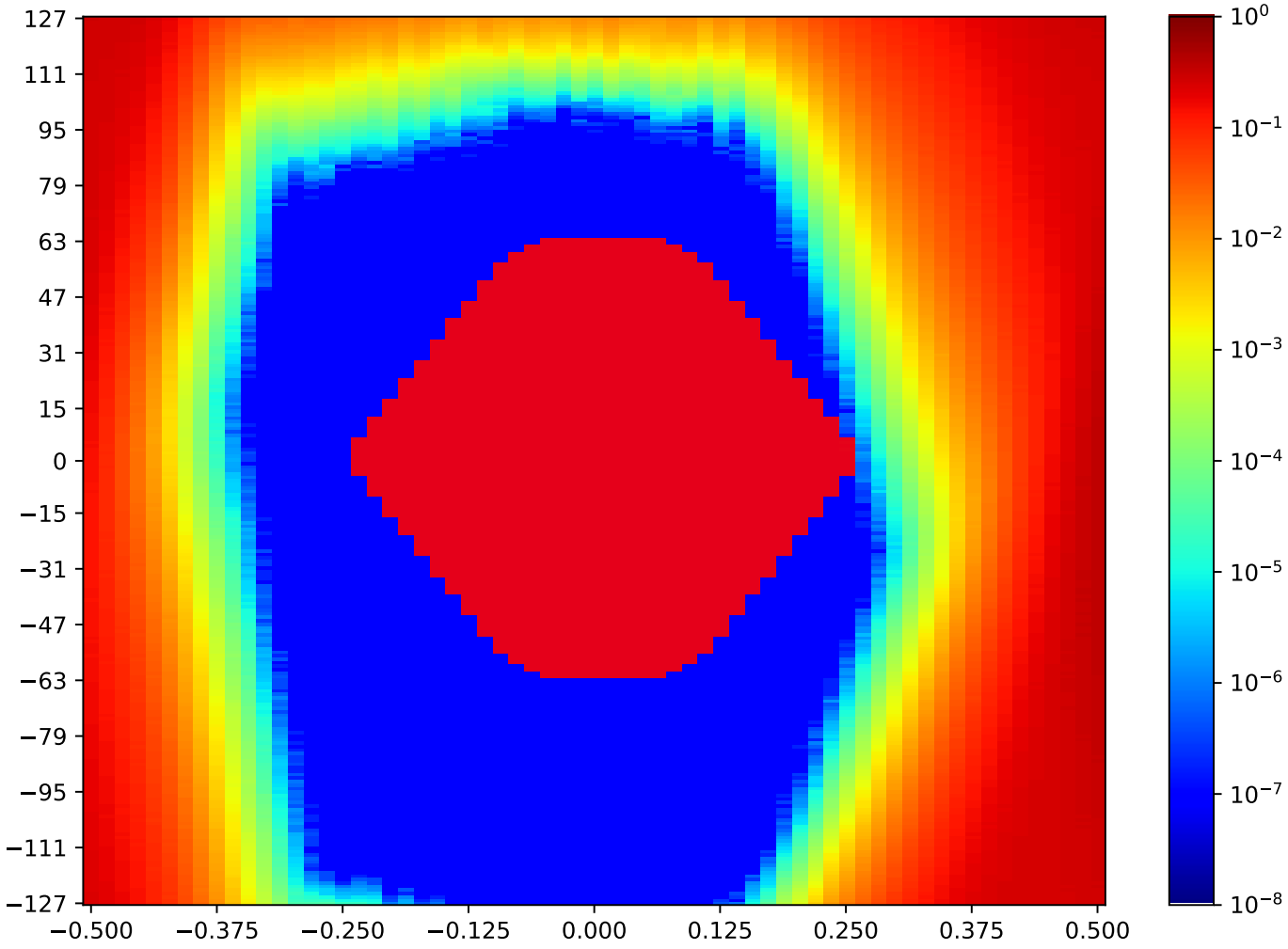


Figure 6.245: MSP_A_FPGA-TX1-04–RX12-04-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.6 MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Table 6.227: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:33:47		2019-Nov-27 11:34:14	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8241	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

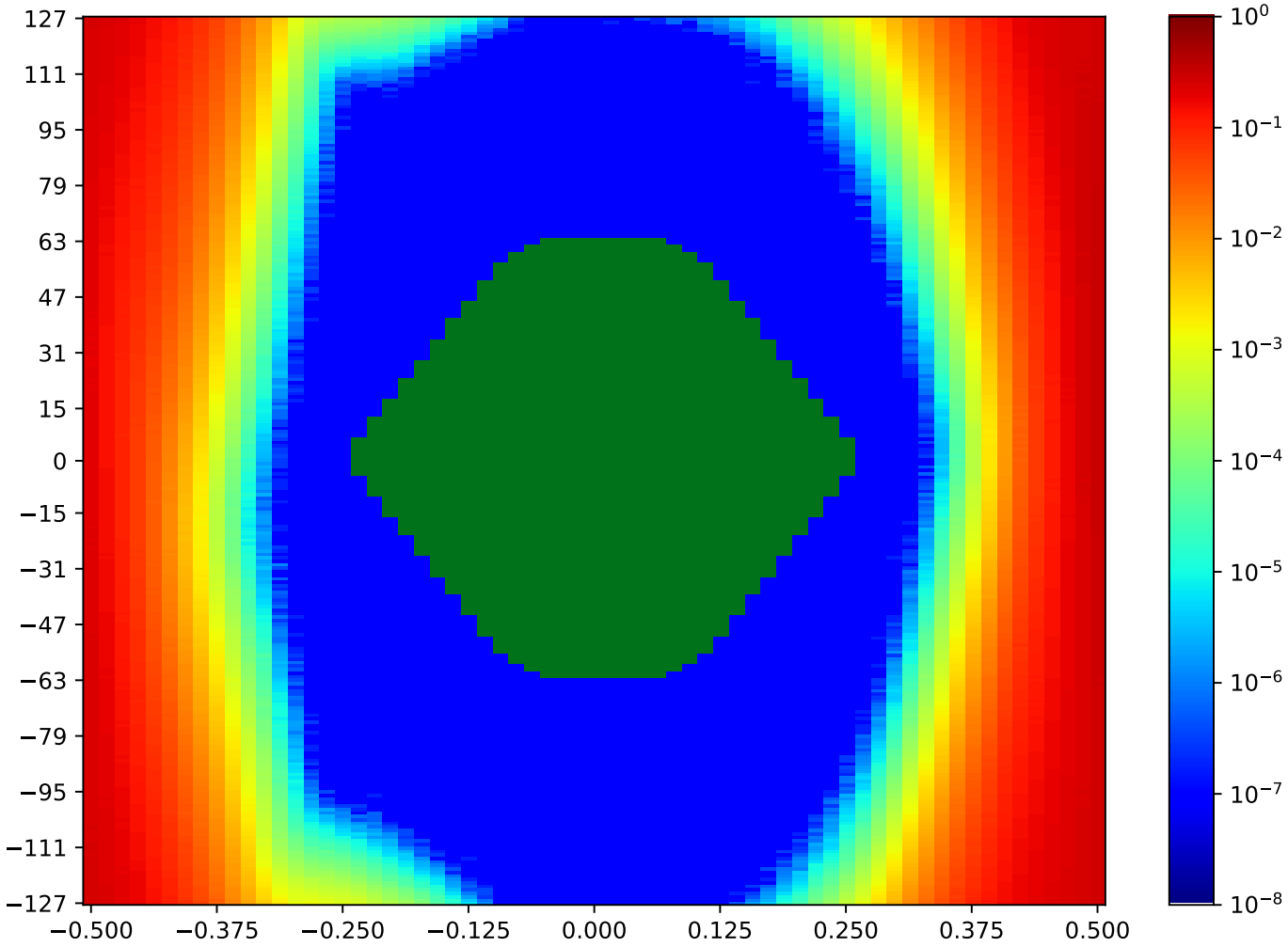


Figure 6.246: MSP_A_FPGA-TX1-05–RX12-05-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.7 MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Table 6.228: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:38:40		2019-Nov-27 11:39:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8481	42	64.62%	232	90.59%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

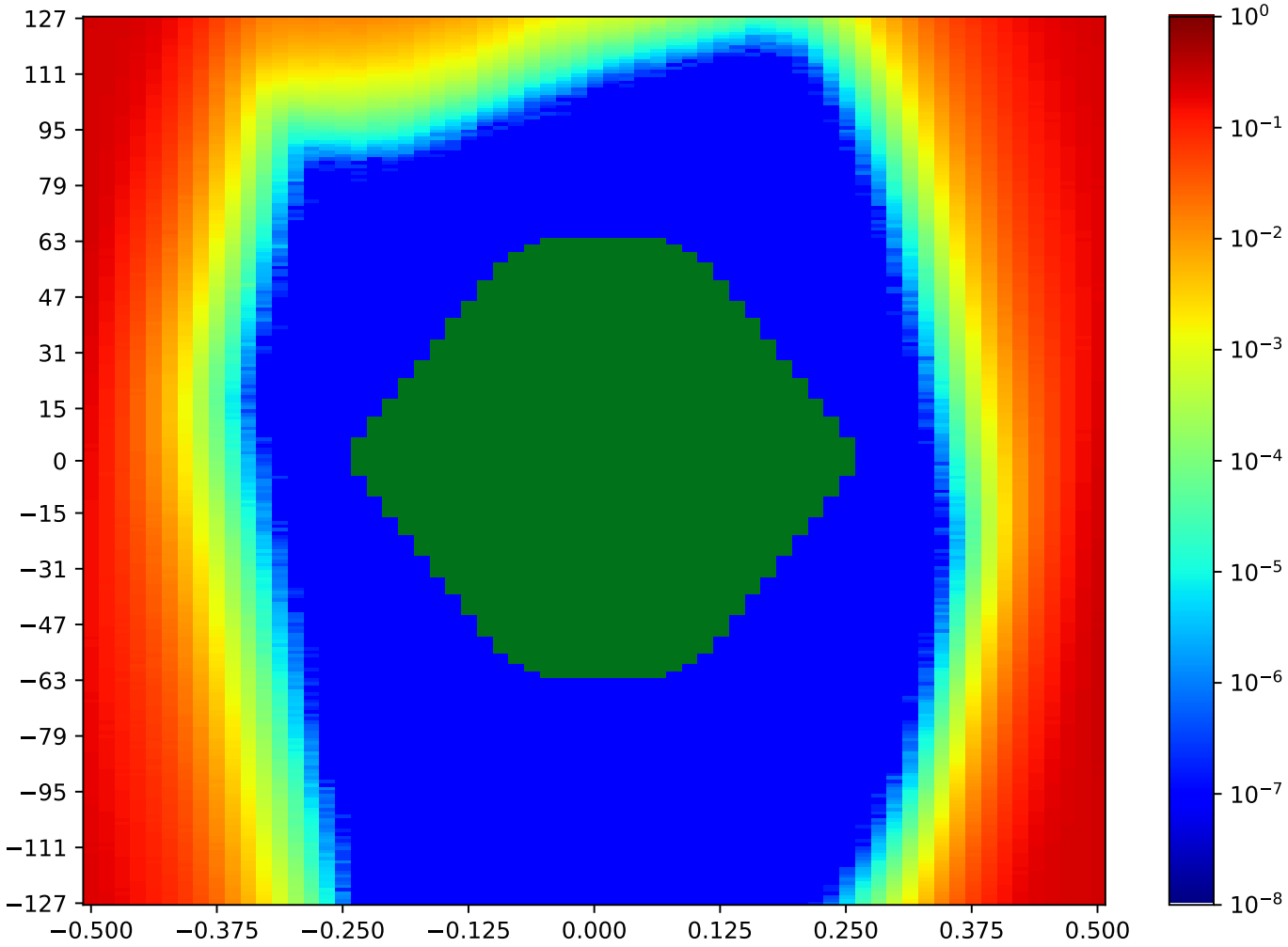


Figure 6.247: MSP_A_FPGA-TX1-06–RX12-06-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.8 MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Table 6.229: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:34:43		2019-Nov-27 11:35:04	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9359	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

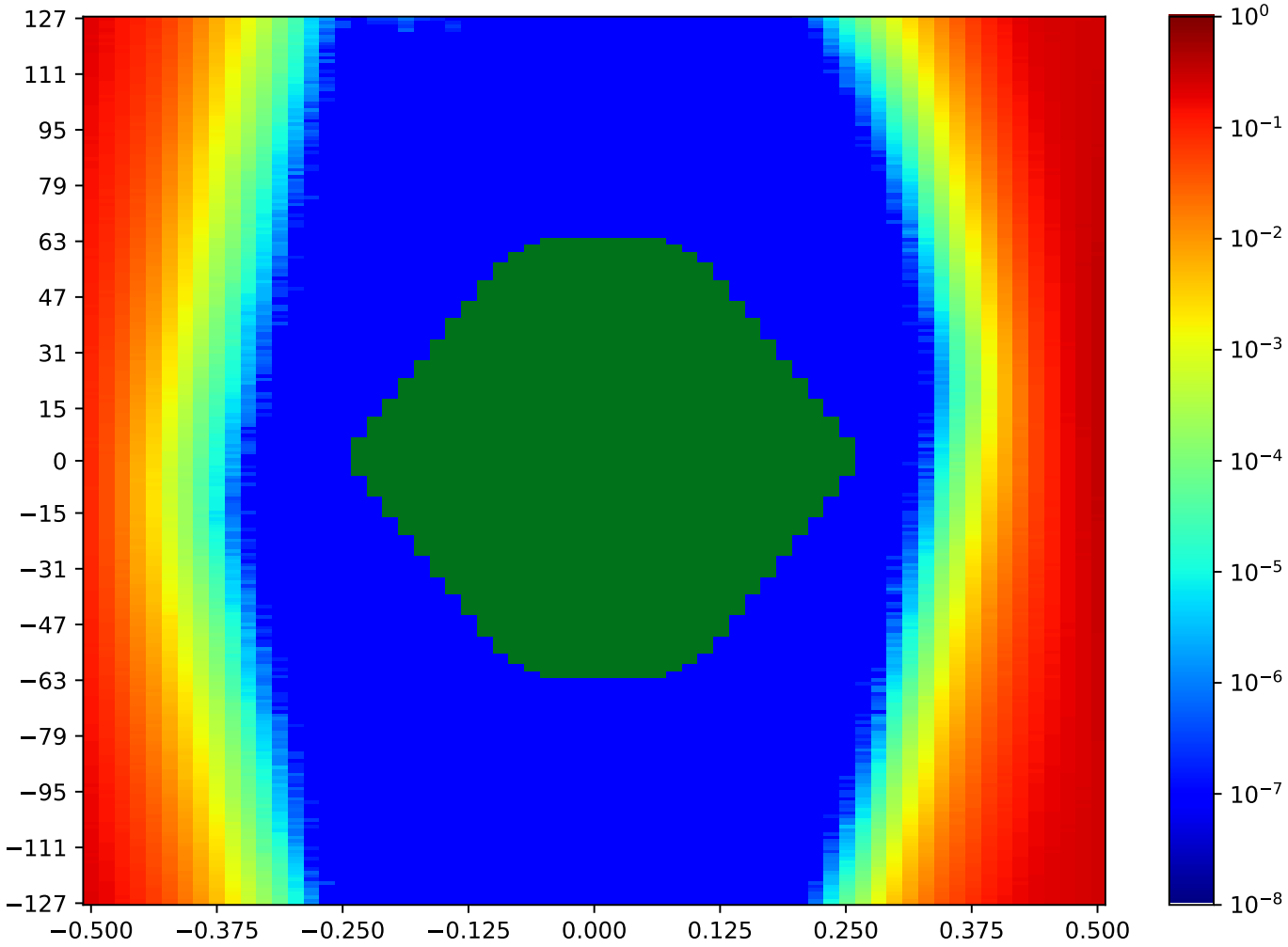


Figure 6.248: MSP_A_FPGA-TX1-07–RX12-07-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.9 MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Table 6.230: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:38:14		2019-Nov-27 11:38:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7493	44	67.69%	207	81.18%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
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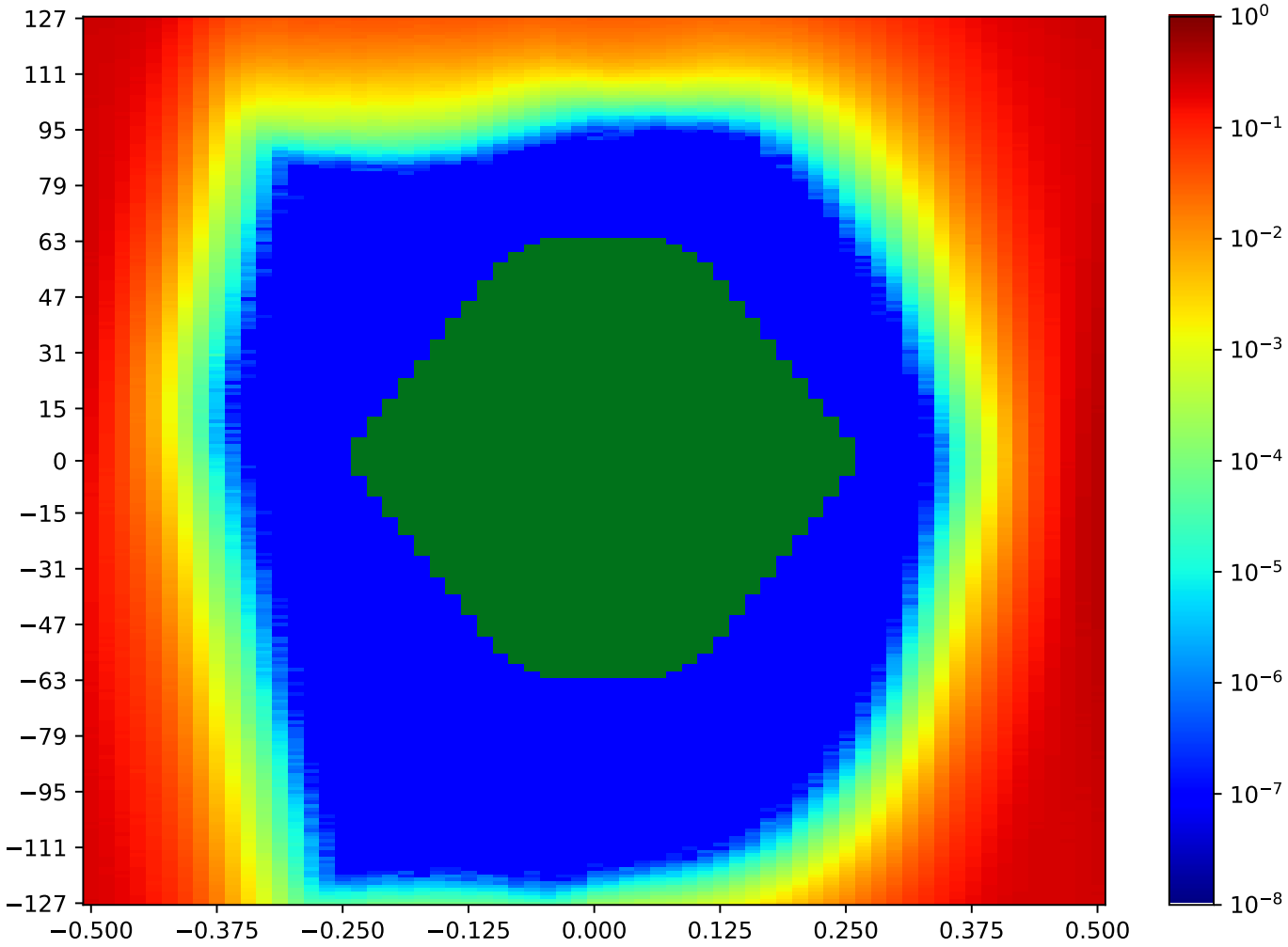


Figure 6.249: MSP_A_FPGA-TX1-08–RX12-08-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.10 MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Table 6.231: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:35:30		2019-Nov-27 11:35:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9111	41	63.08%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

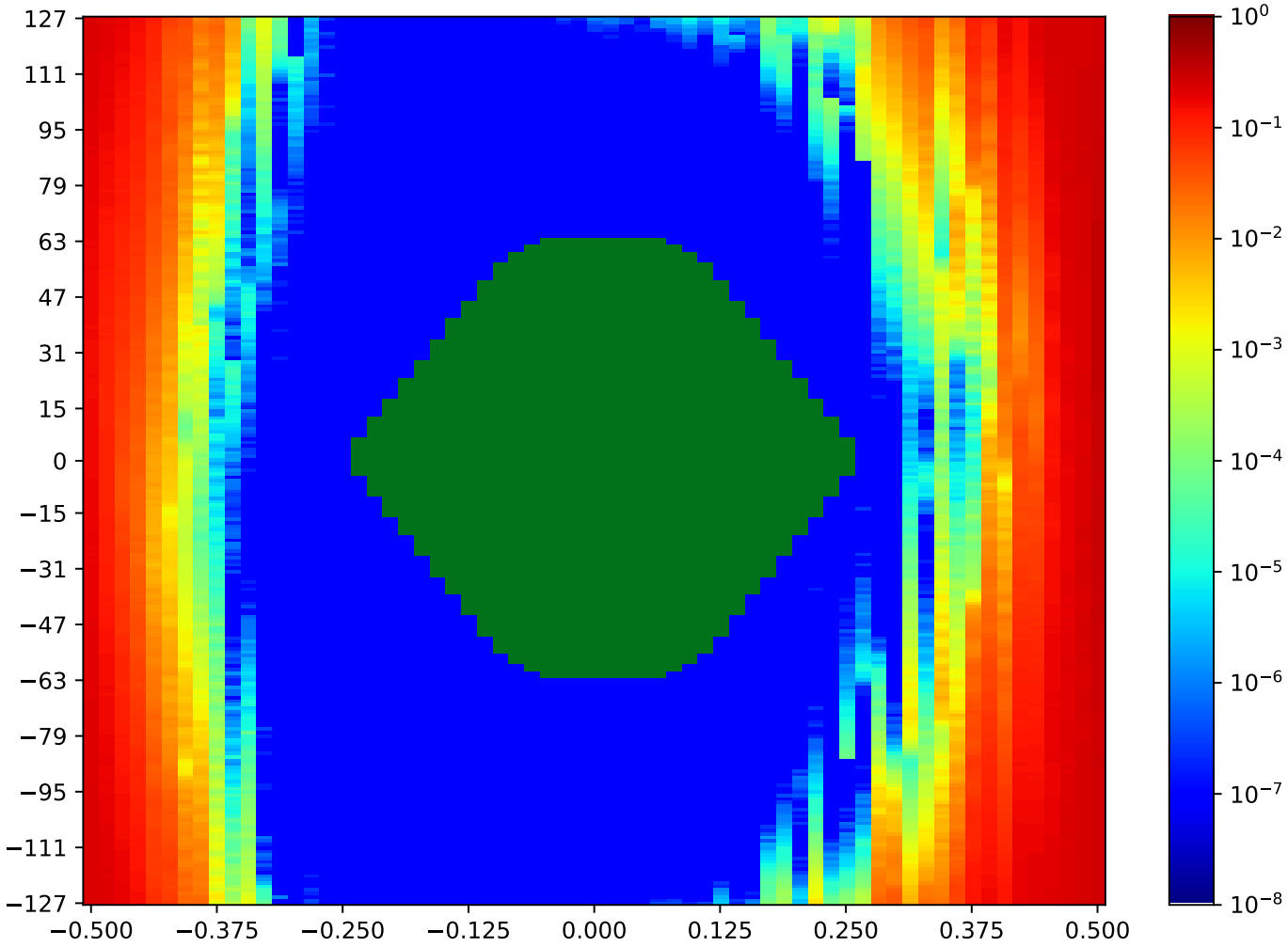


Figure 6.250: MSP_A_FPGA-TX1-09–RX12-09-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.11 MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Table 6.232: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:37:21		2019-Nov-27 11:37:47	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8087	36	55.38%	253	98.82%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

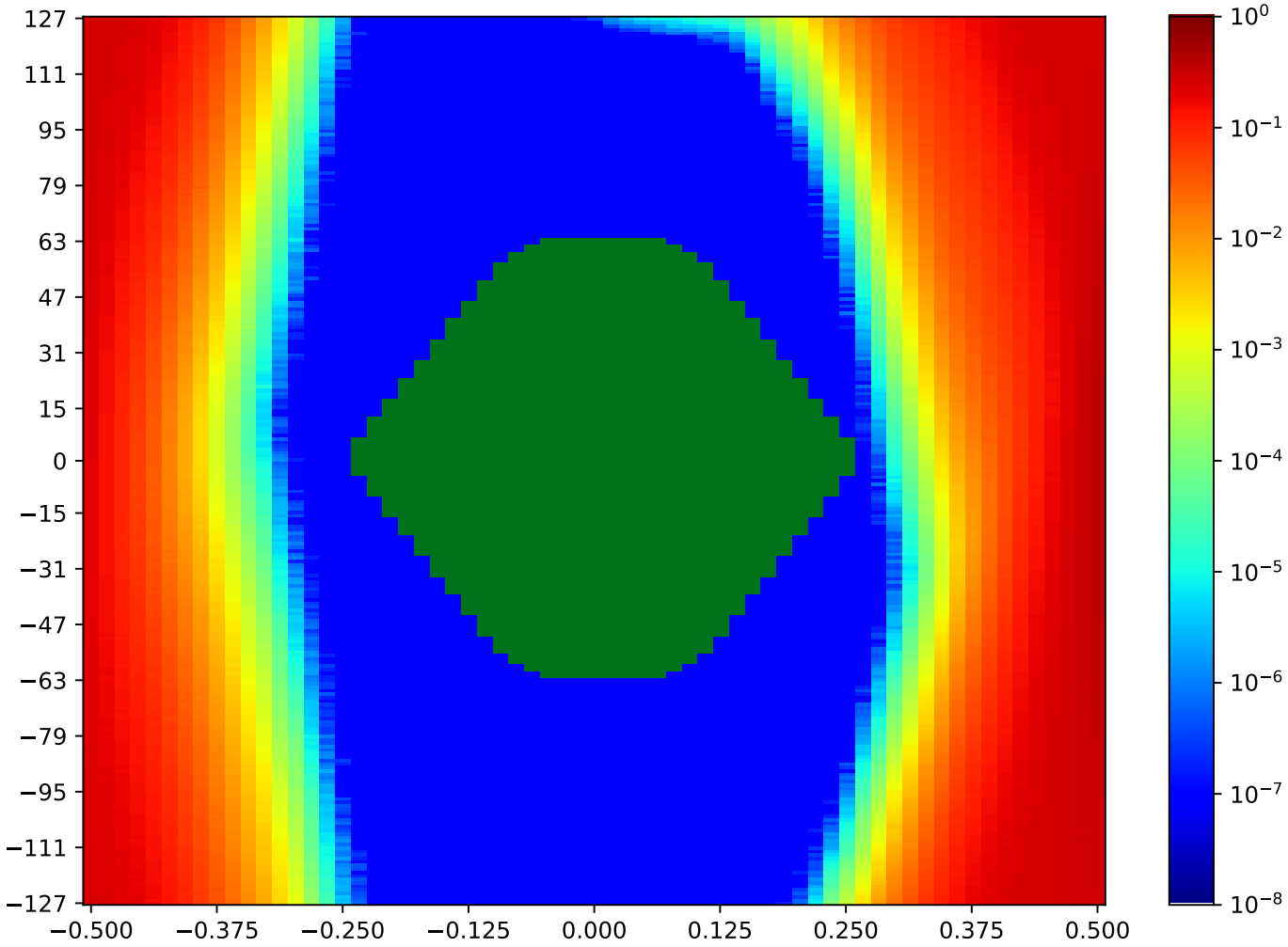


Figure 6.251: MSP_A_FPGA-TX1-10–RX12-10-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.19.12 MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Table 6.233: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:36:53		2019-Nov-27 11:37:21	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9233	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

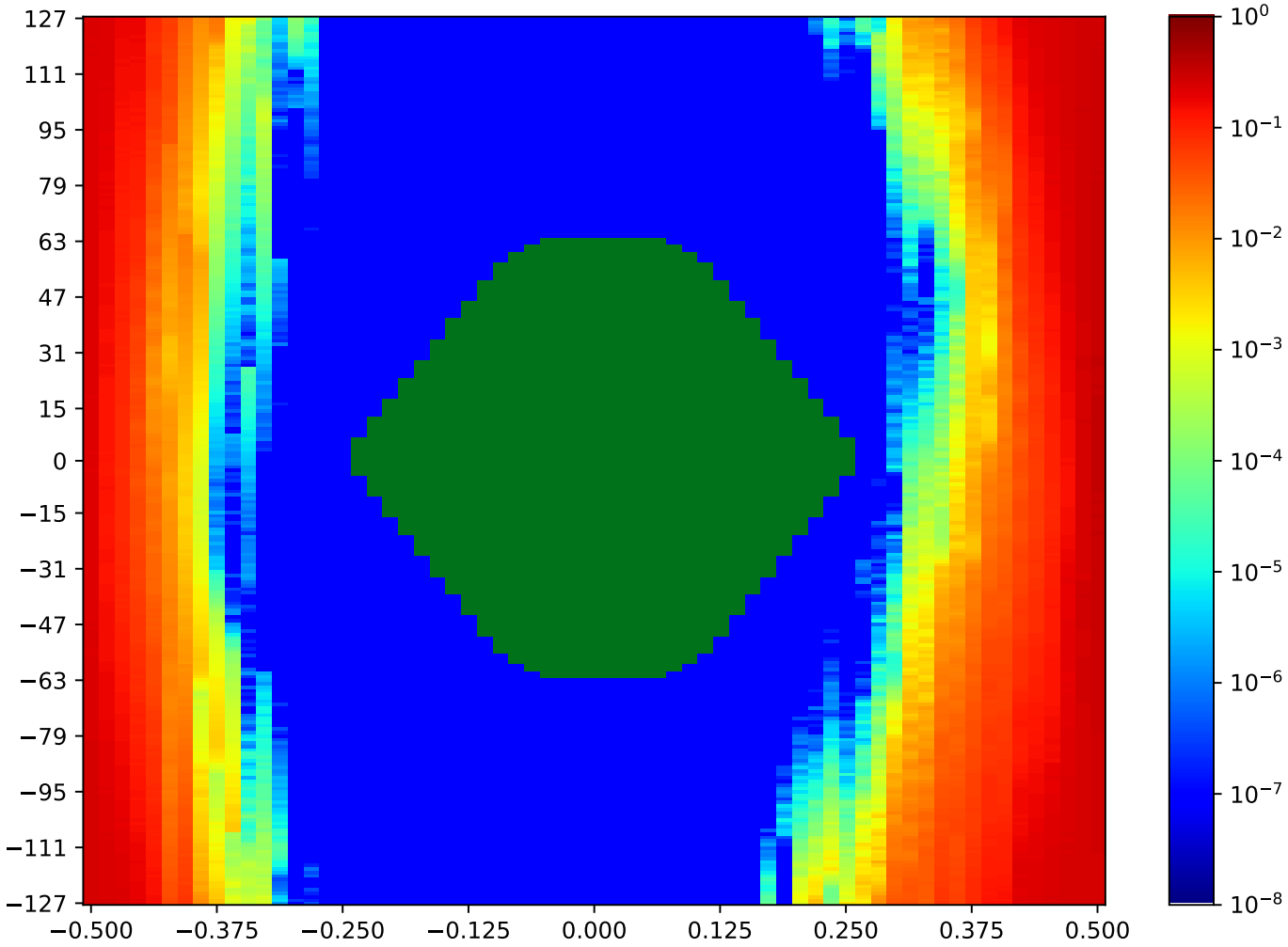


Figure 6.252: MSP_A_FPGA-TX1-11–RX12-11-MSP_C_FPGA

Call back to summary Figure 6.240. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20 MSP_A TX2 MSP_C RX13 Minipod Loopback

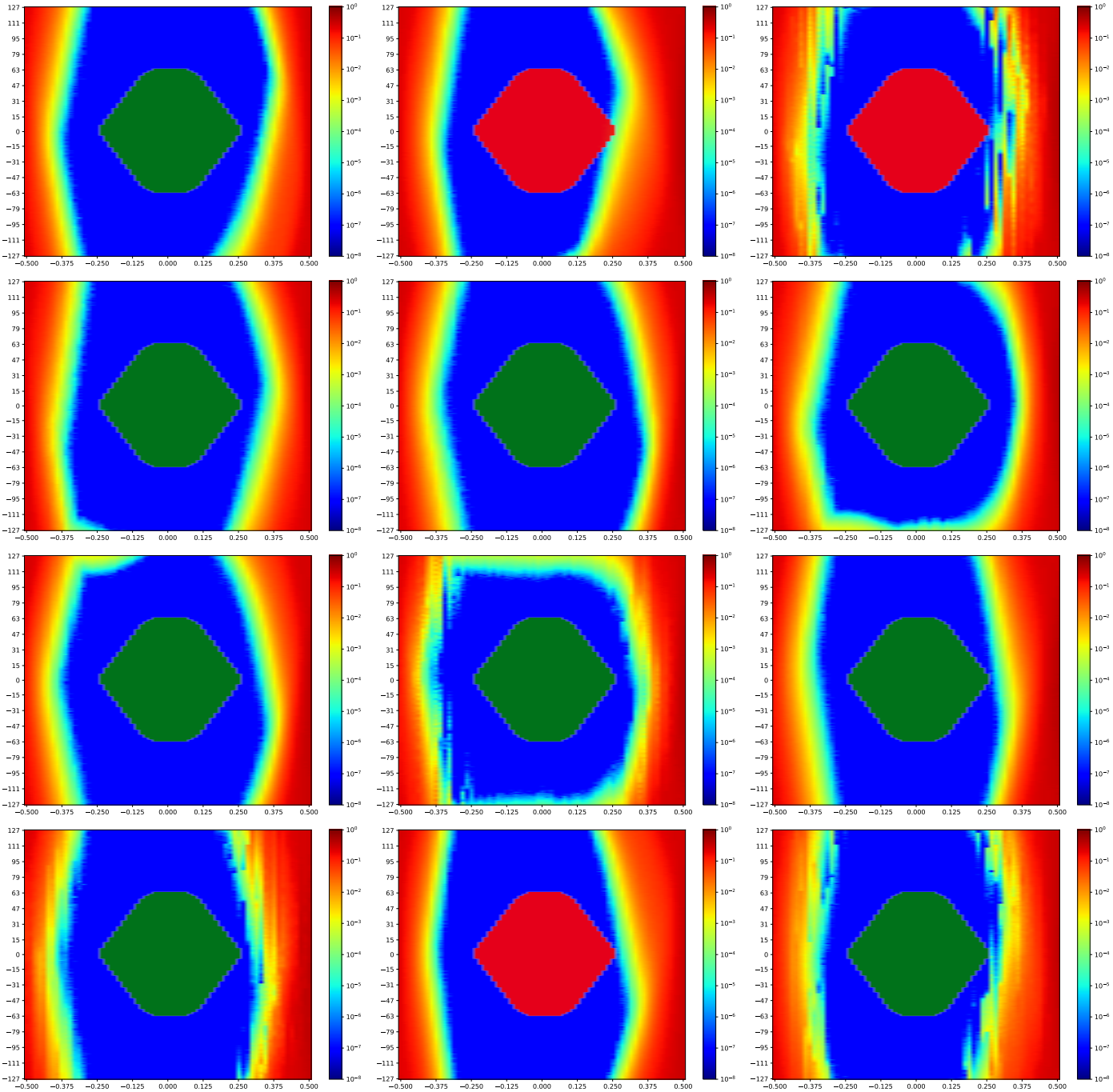


Figure 6.253: MSP_A TX2 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.266.

6.20.1 MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Table 6.234: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:40:30		2019-Nov-27 11:40:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9608	42	64.62%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

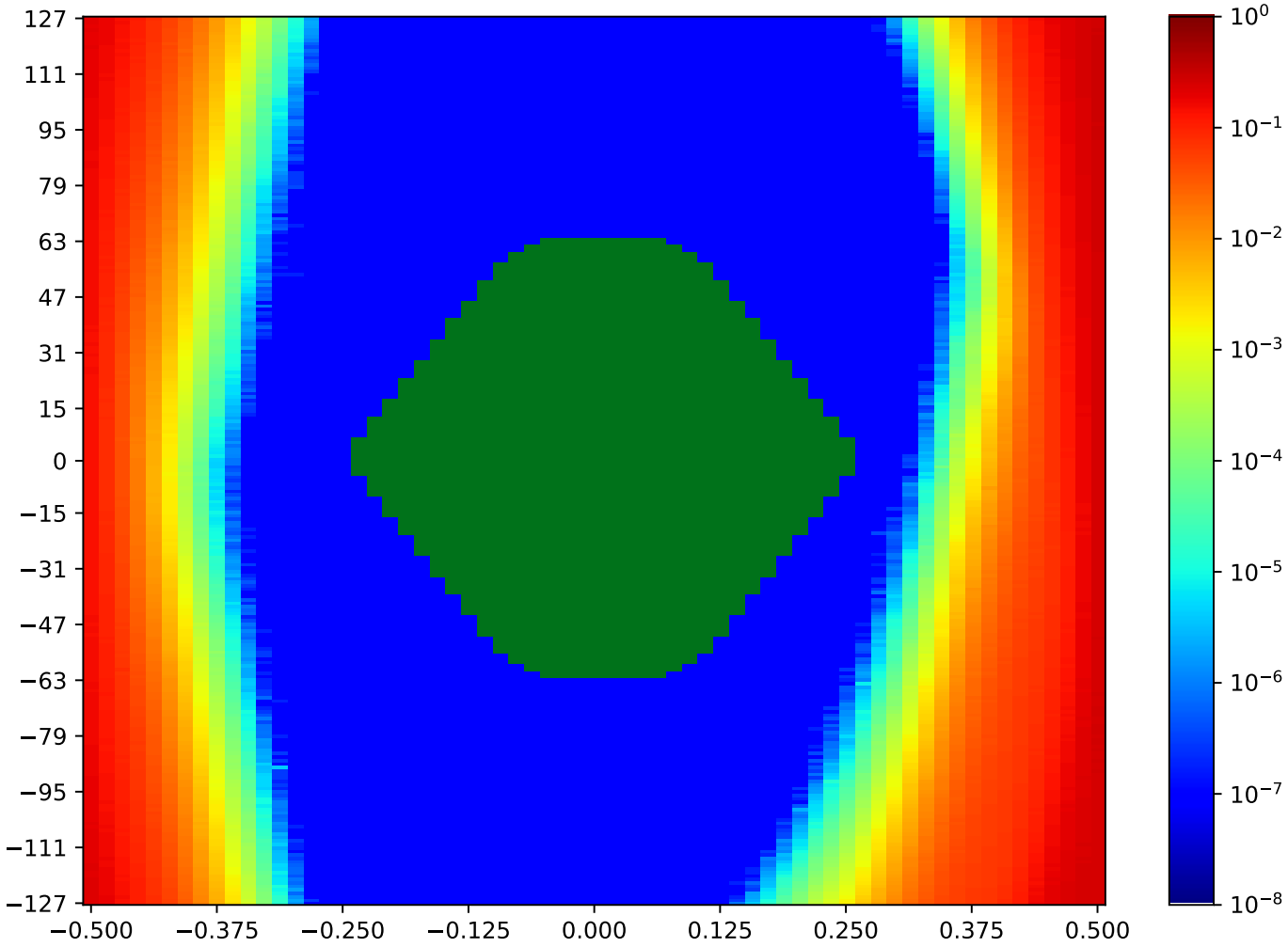


Figure 6.254: MSP_A_FPGA-TX2-00–RX13-00-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.2 MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Table 6.235: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:39:36		2019-Nov-27 11:40:02	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7768	34	52.31%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

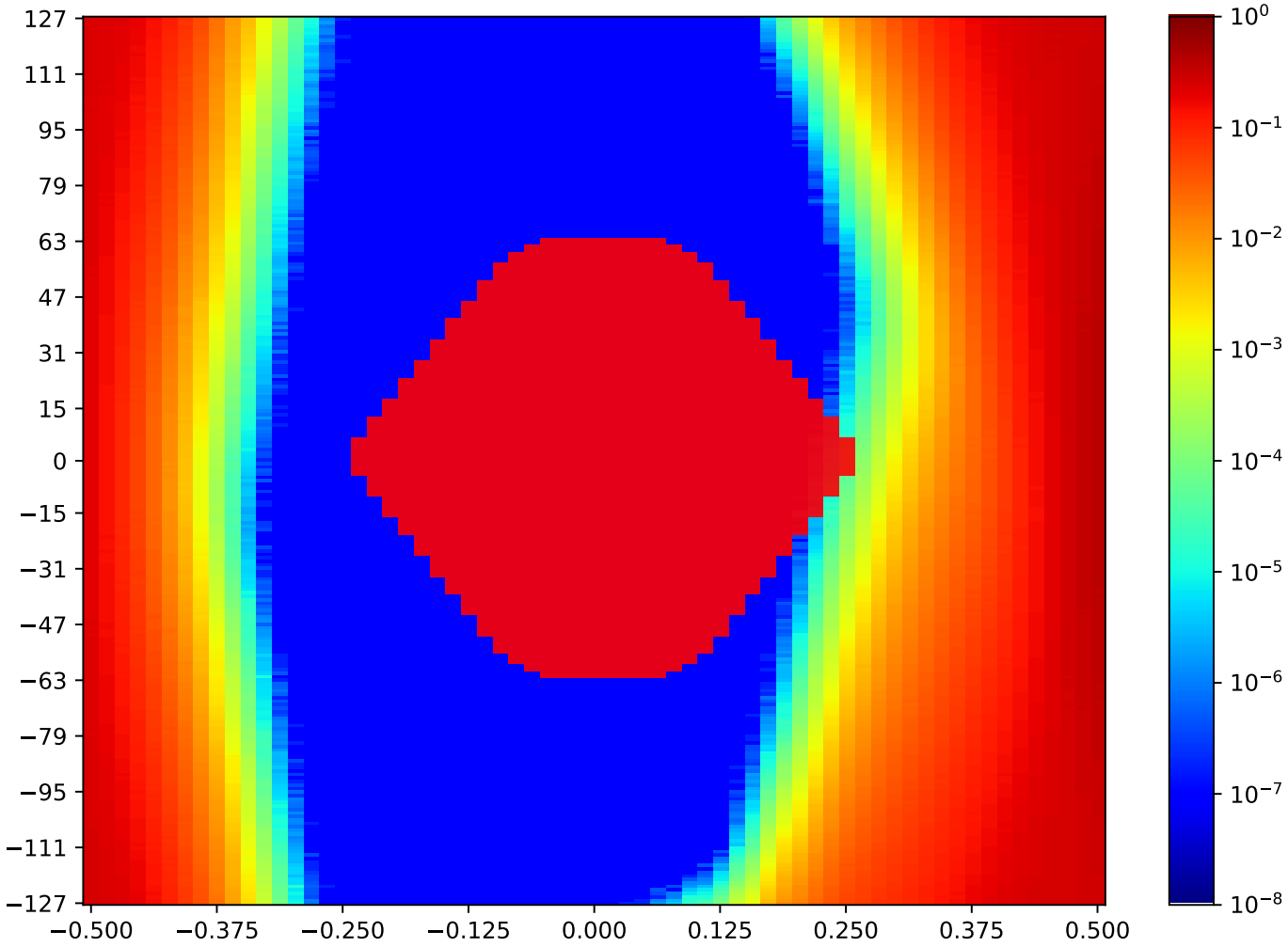


Figure 6.255: MSP_A_FPGA-TX2-01–RX13-01-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.3 MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Table 6.236: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:41:53		2019-Nov-27 11:42:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8709	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

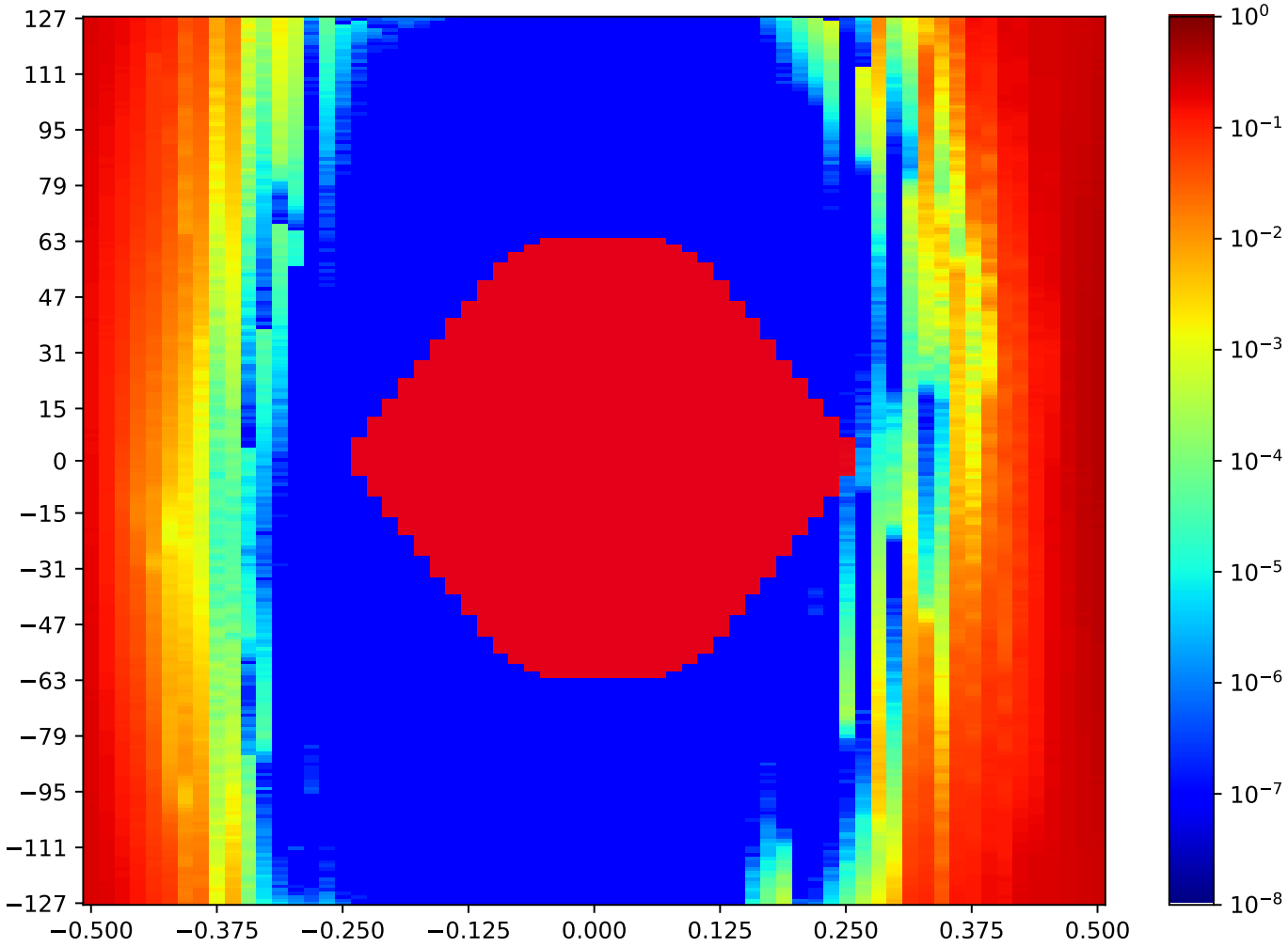


Figure 6.256: MSP_A_FPGA-TX2-02–RX13-02-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.4 MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Table 6.237: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:39:09		2019-Nov-27 11:39:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9067	39	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

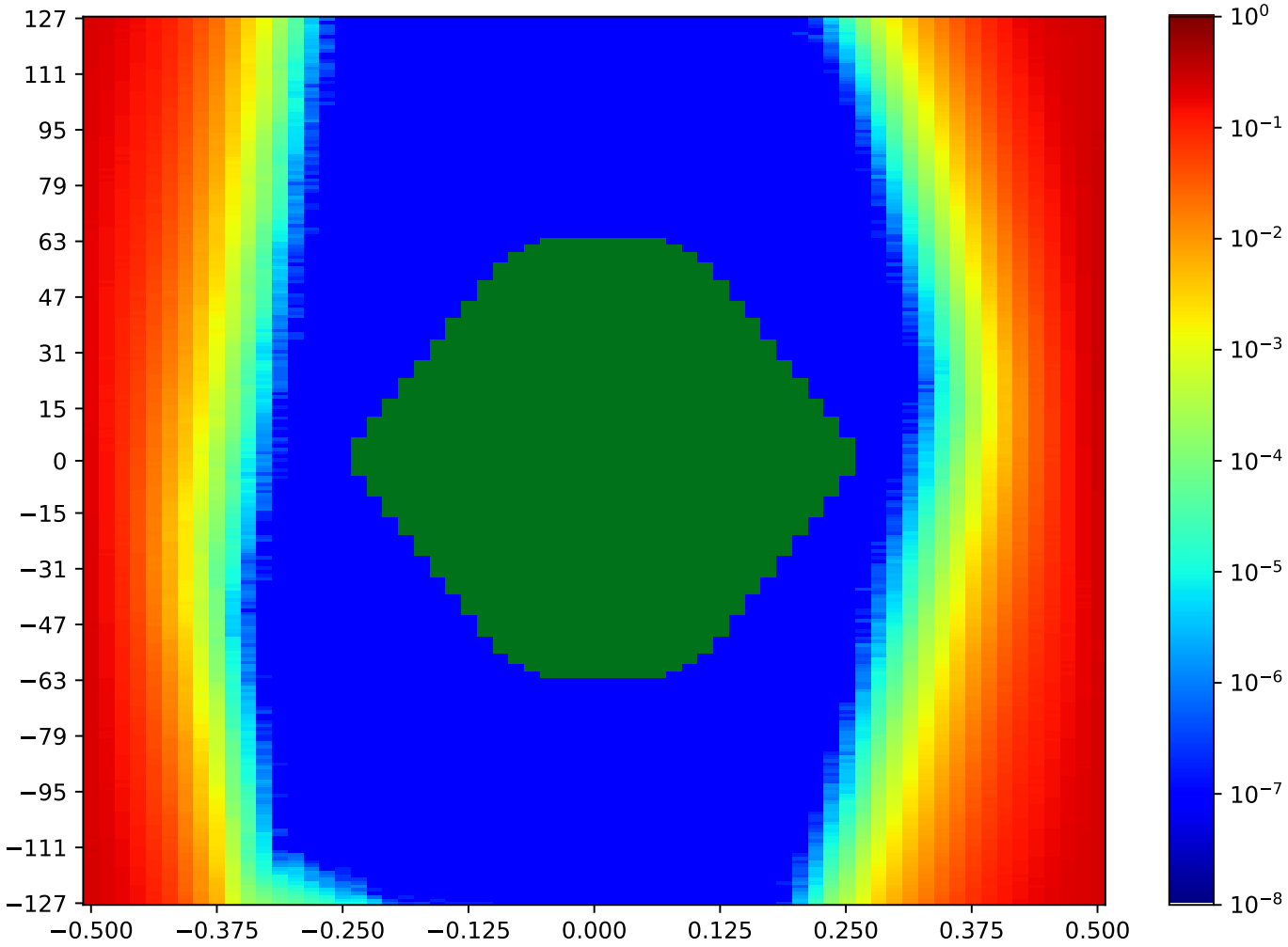


Figure 6.257: MSP_A_FPGA-TX2-03–RX13-03-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.5 MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Table 6.238: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:43:12		2019-Nov-27 11:43:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9359	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

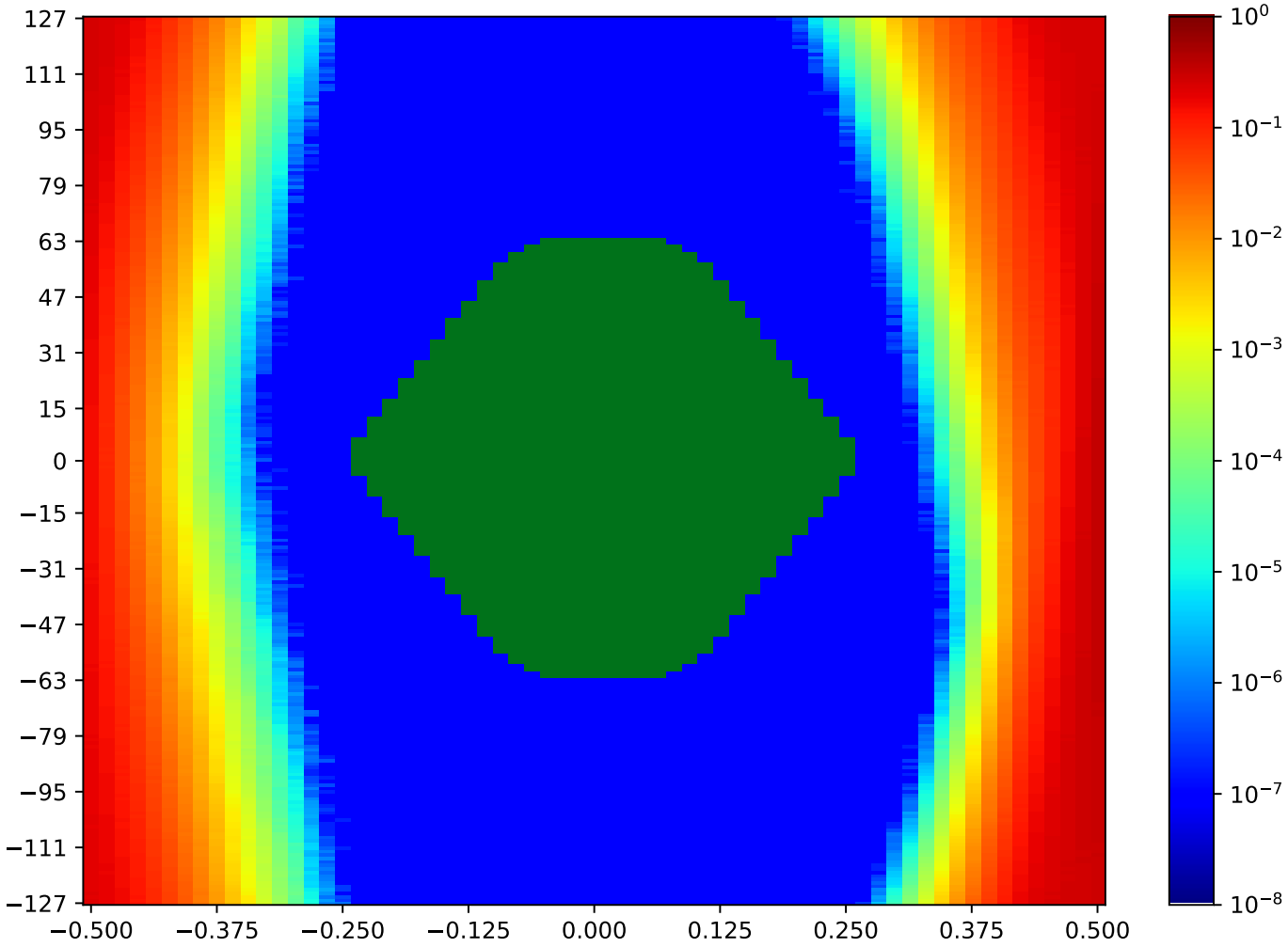


Figure 6.258: MSP_A_FPGA-TX2-04–RX13-04-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.6 MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Table 6.239: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:40:02		2019-Nov-27 11:40:30	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8535	41	63.08%	242	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

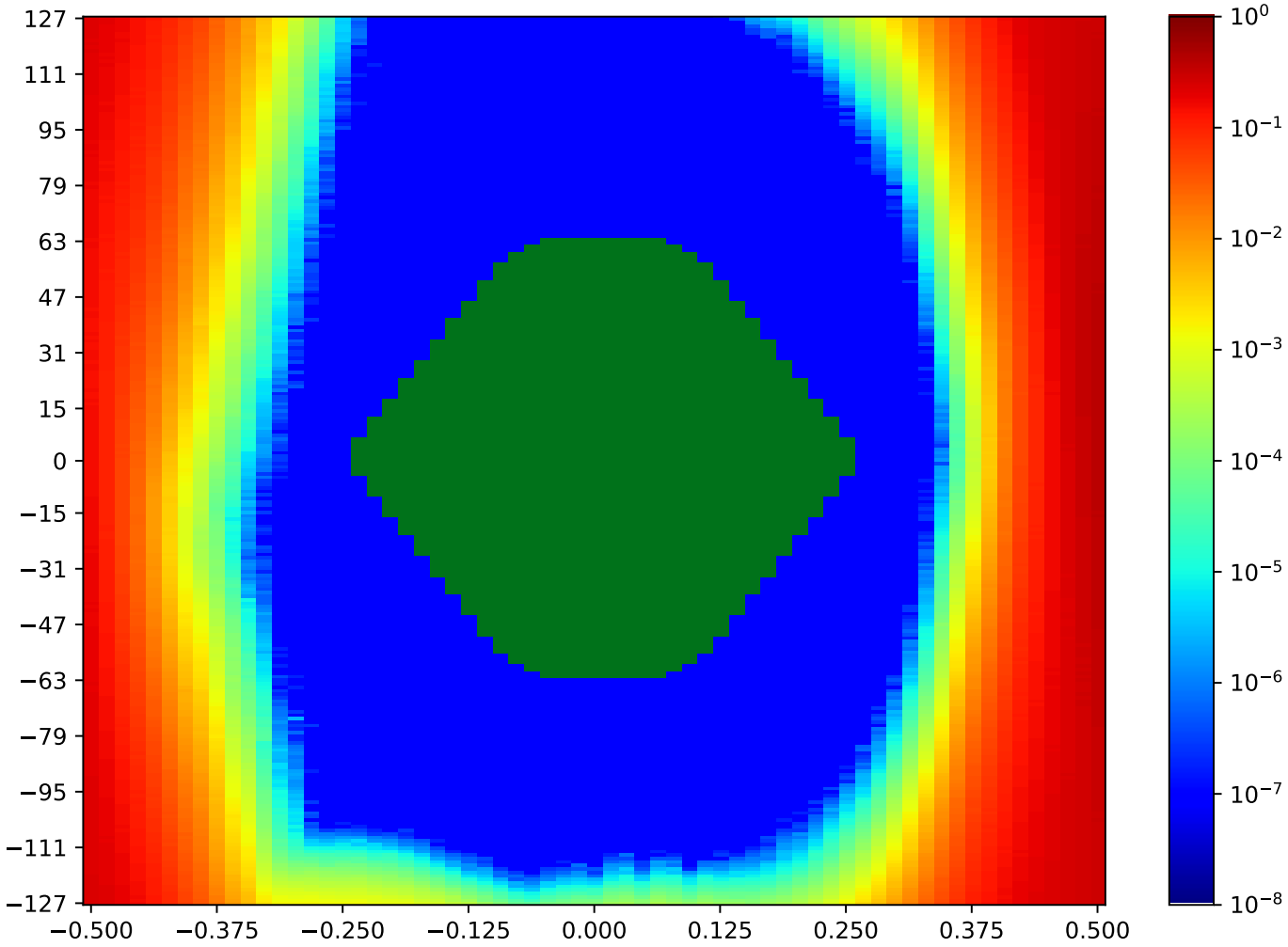


Figure 6.259: MSP_A_FPGA-TX2-05–RX13-05-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.7 MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Table 6.240: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:44:07		2019-Nov-27 11:44:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9145	42	64.62%	255	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

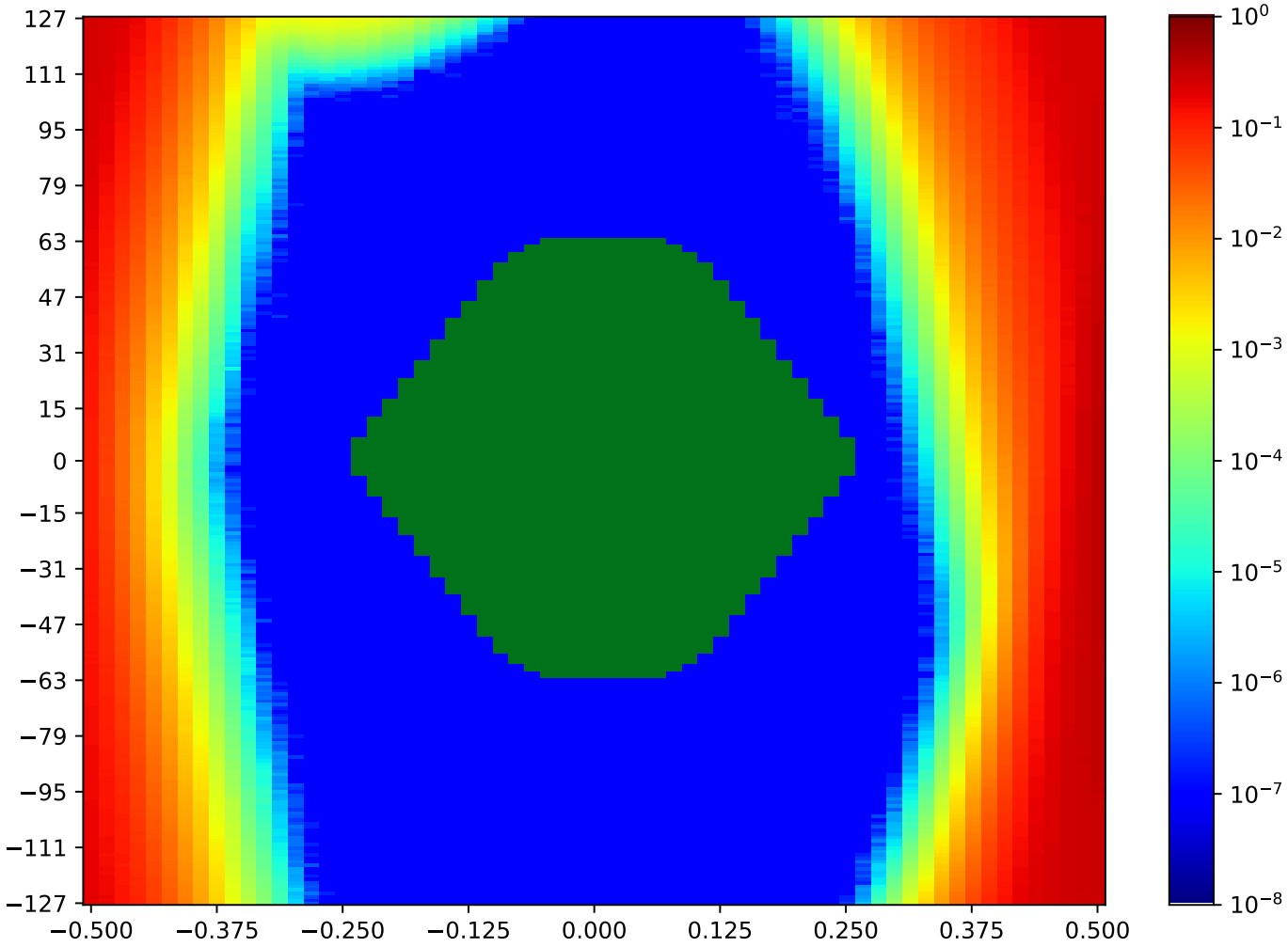


Figure 6.260: MSP_A_FPGA-TX2-06–RX13-06-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.8 MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Table 6.241: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:40:58		2019-Nov-27 11:41:25	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8077	41	63.08%	210	81.96%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

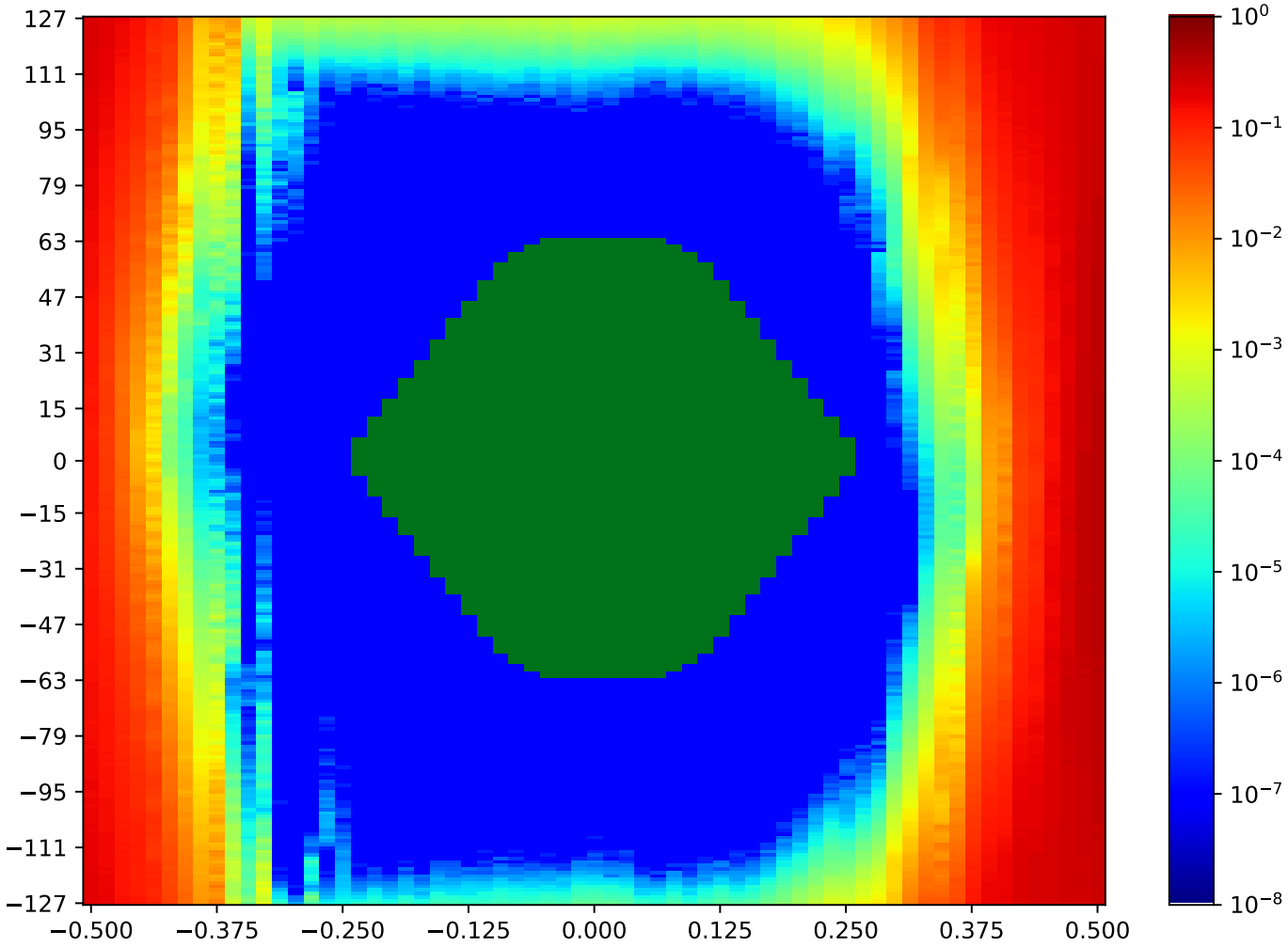


Figure 6.261: MSP_A_FPGA-TX2-07–RX13-07-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.9 MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Table 6.242: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:43:40		2019-Nov-27 11:44:07	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8726	36	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

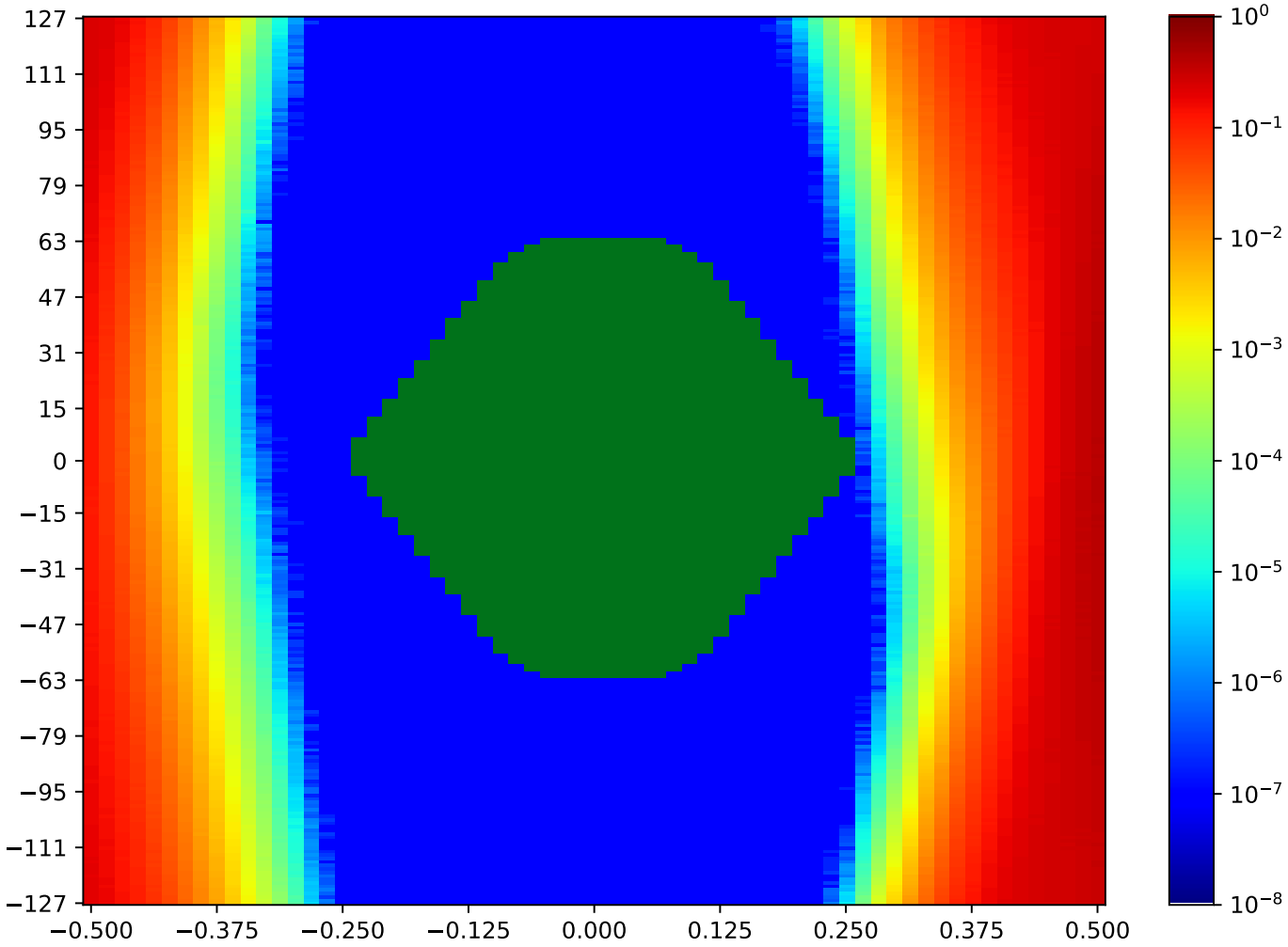


Figure 6.262: MSP_A_FPGA-TX2-08–RX13-08-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.10 MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Table 6.243: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:41:25		2019-Nov-27 11:41:52	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9232	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

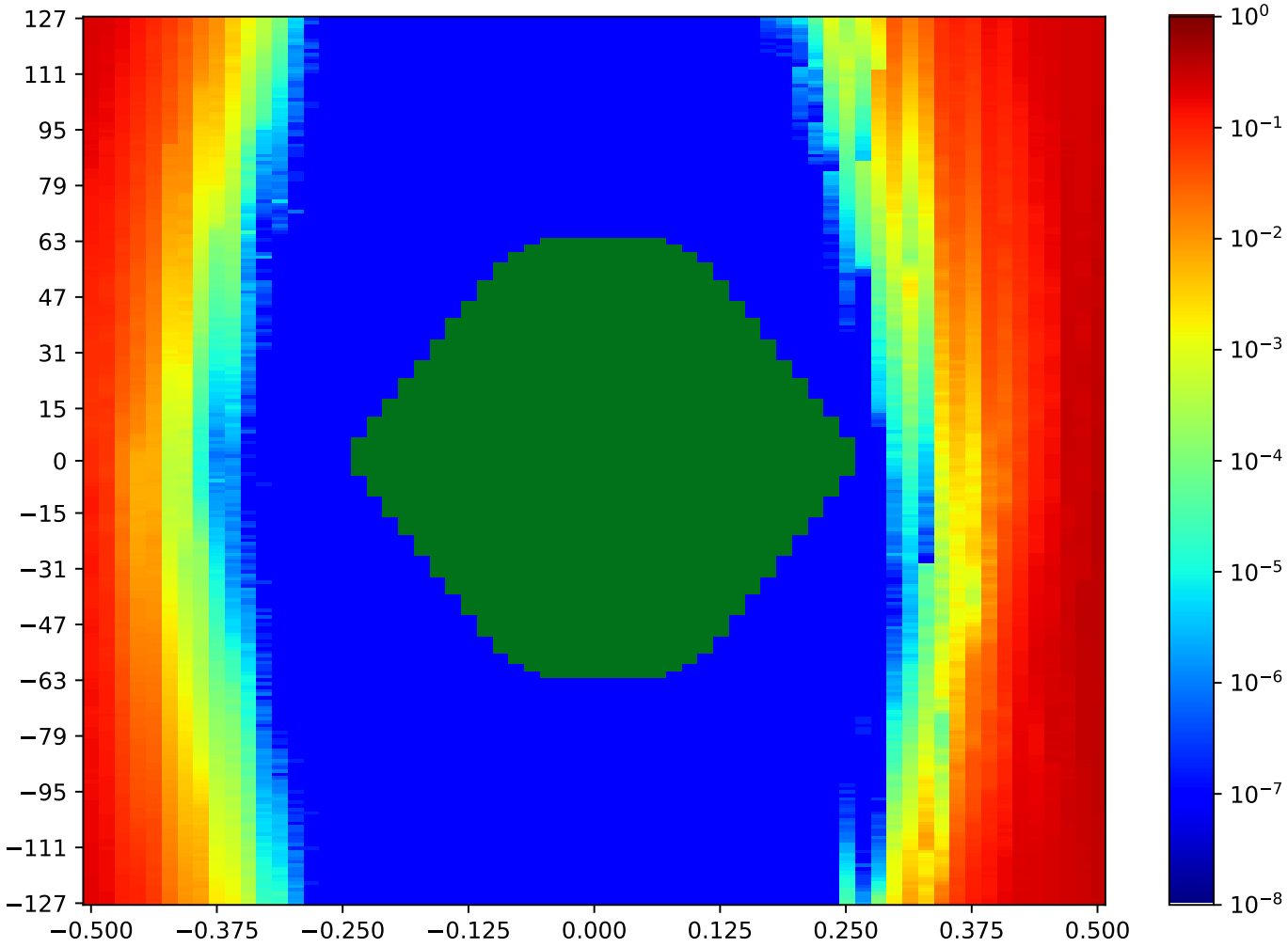


Figure 6.263: MSP_A_FPGA-TX2-09–RX13-09-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.11 MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Table 6.244: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:42:45		2019-Nov-27 11:43:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9126	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

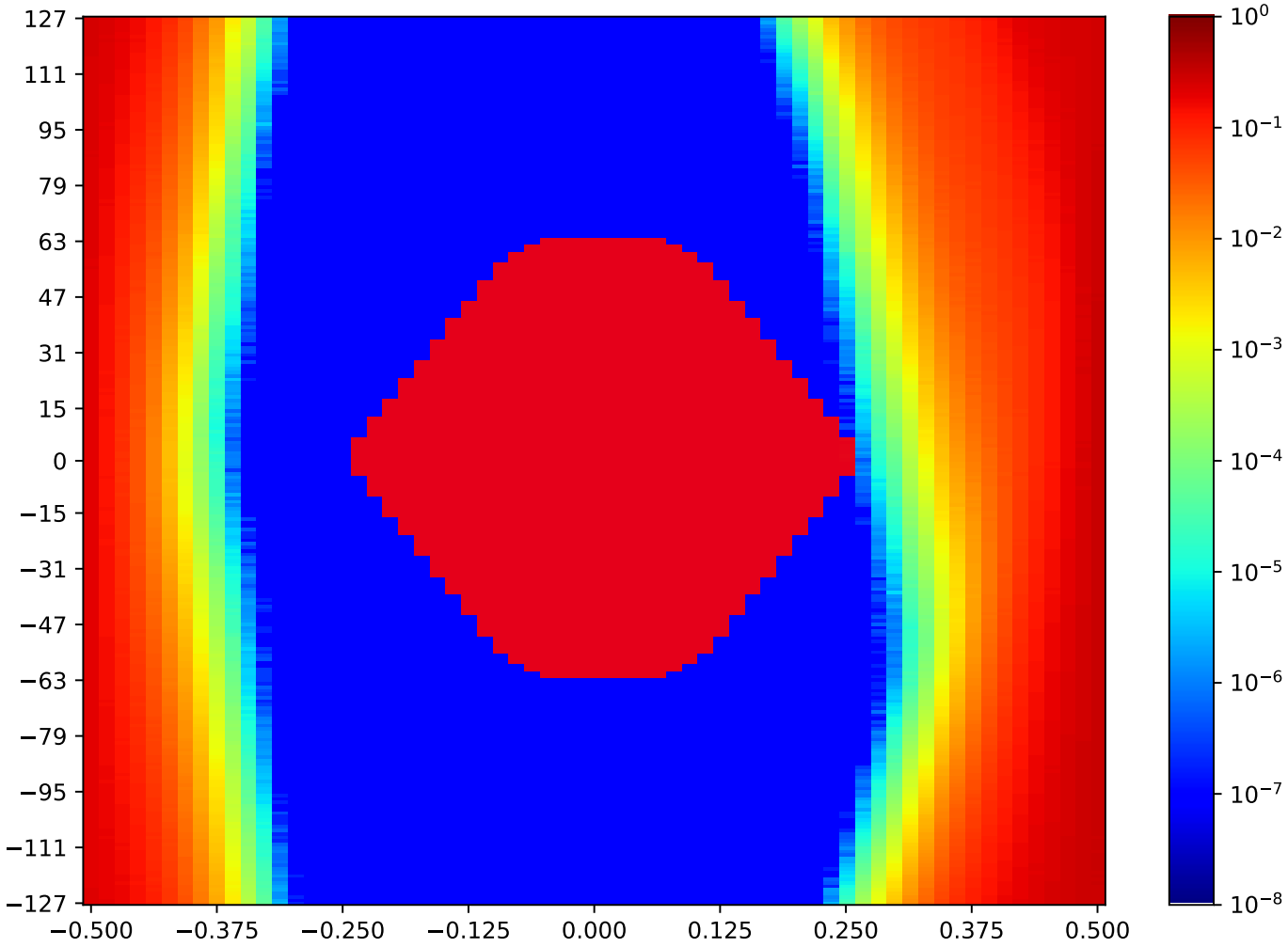


Figure 6.264: MSP_A_FPGA-TX2-10–RX13-10-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.20.12 MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Table 6.245: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:42:19		2019-Nov-27 11:42:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8465	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

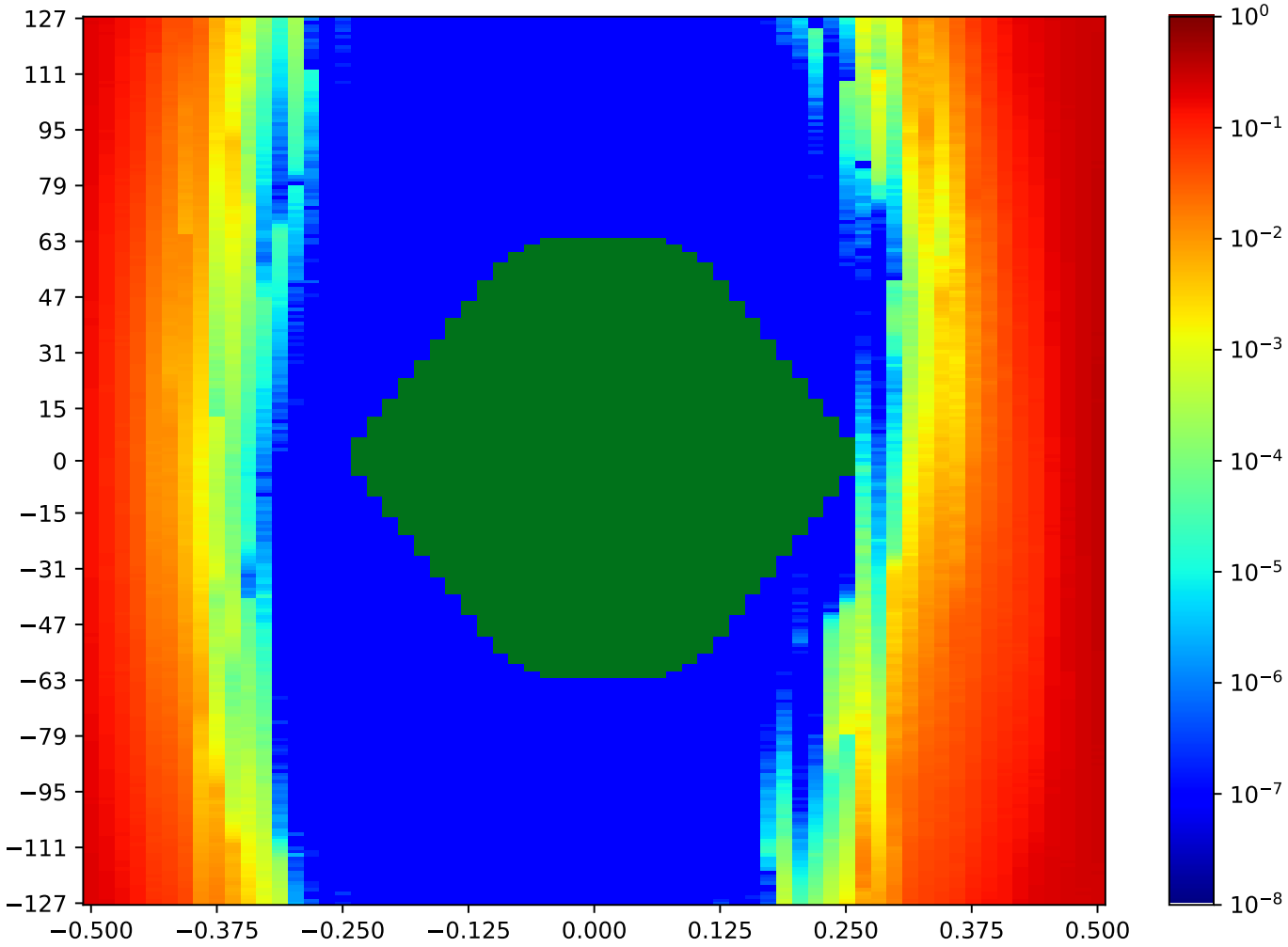


Figure 6.265: MSP_A_FPGA-TX2-11–RX13-11-MSP_C_FPGA

Call back to summary Figure 6.253. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21 MSP_C TX3 MSP_A RX3 Minipod Loopback

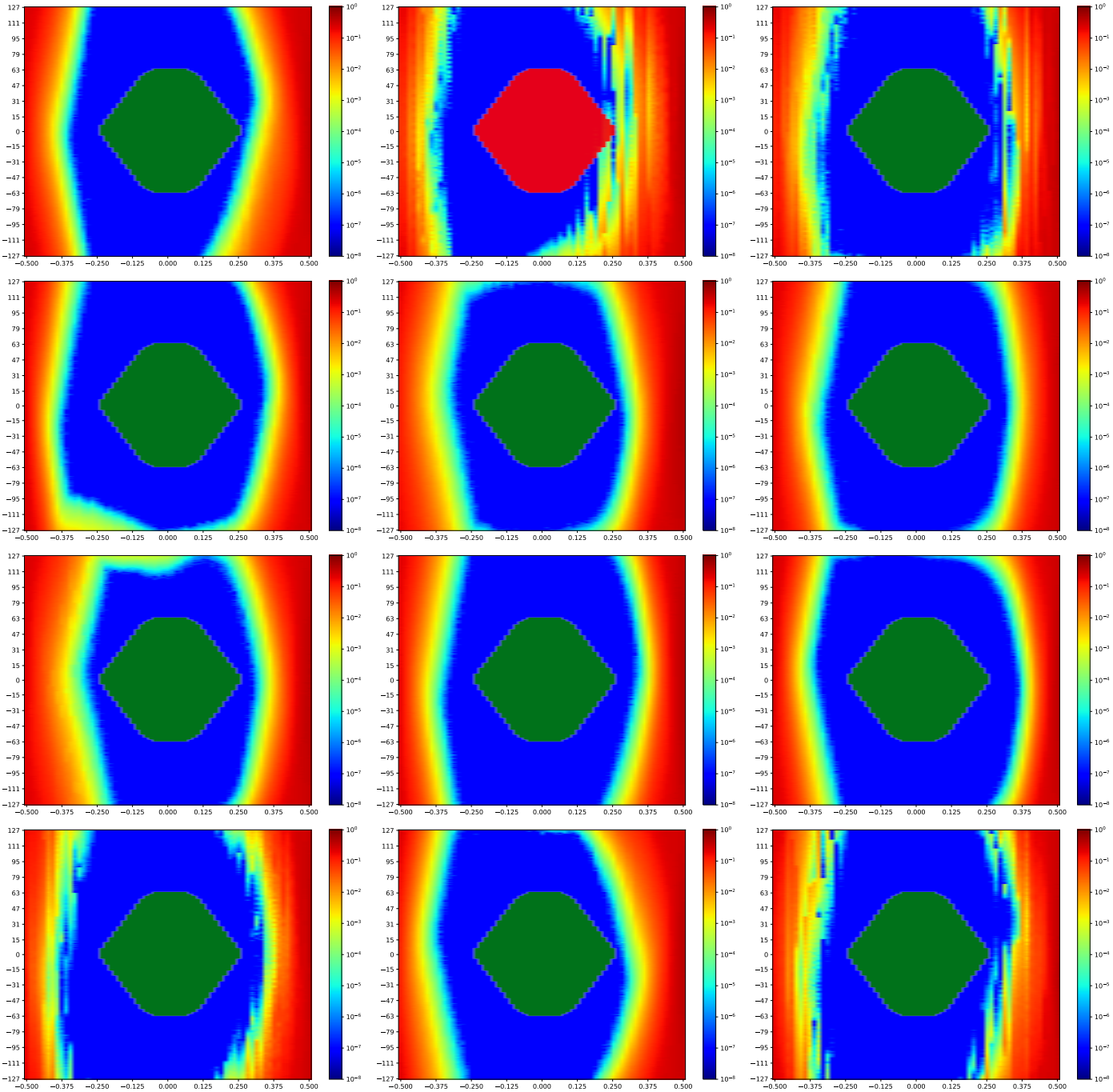


Figure 6.266: MSP_C TX3 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.279.

6.21.1 MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Table 6.246: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:45:39		2019-Nov-27 11:46:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8496	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

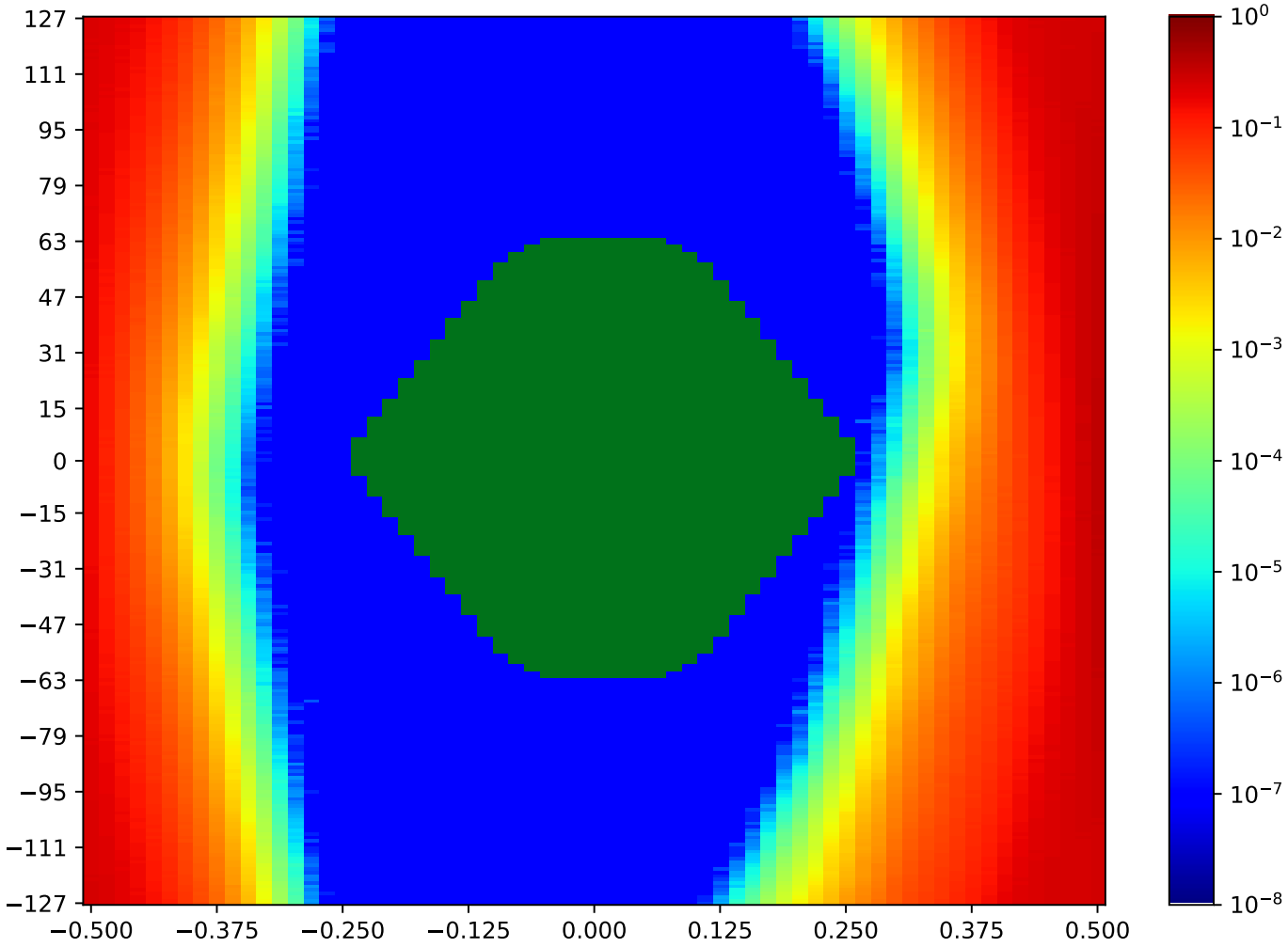


Figure 6.267: MSP_C_FPGA-TX3-00–RX3-00-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.2 MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Table 6.247: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:46:32		2019-Nov-27 11:46:58	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7924	39	55.38%	242	94.90%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

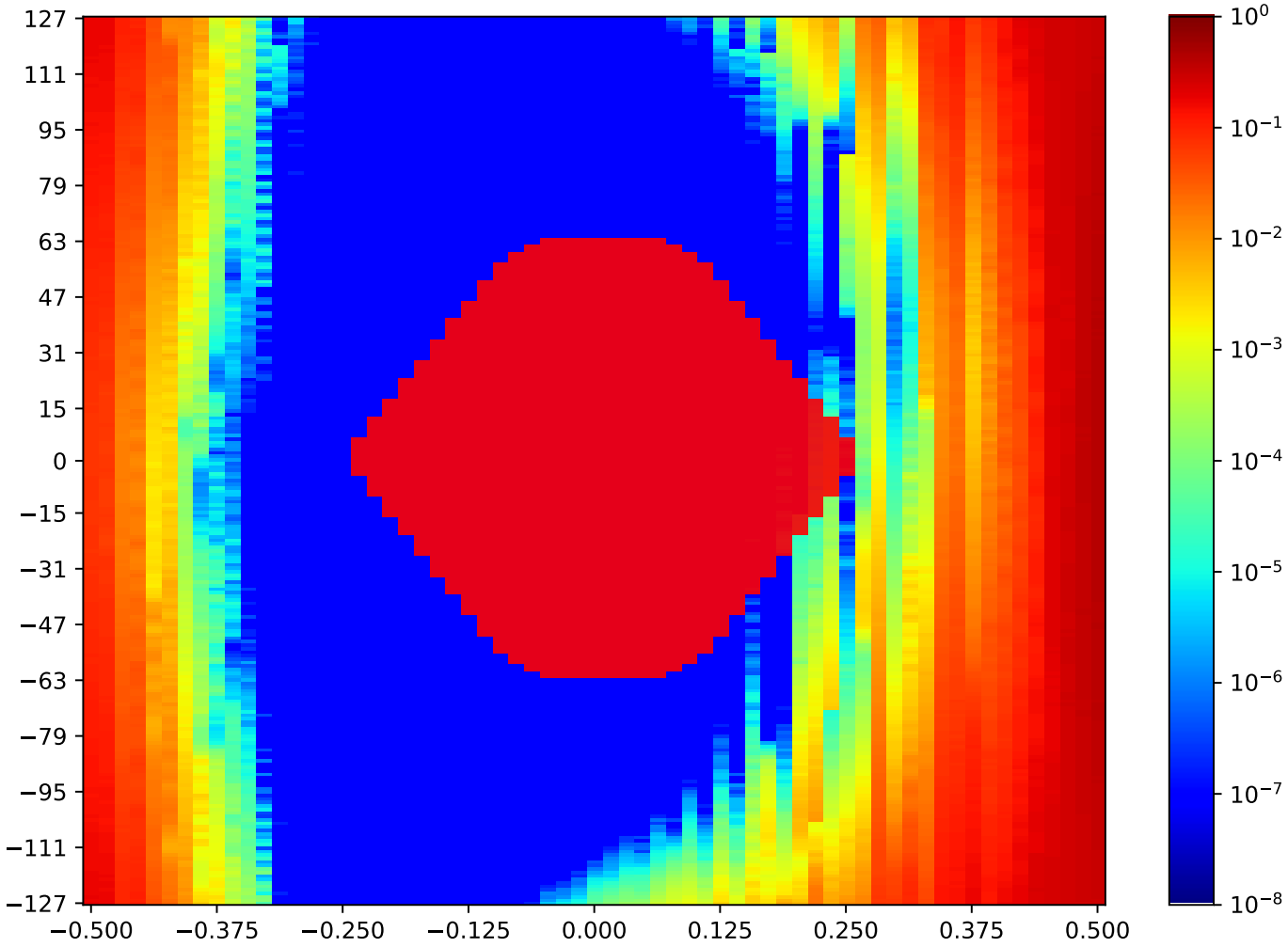


Figure 6.268: MSP_C_FPGA-TX3-01–RX3-01-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.3 MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Table 6.248: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:46:58		2019-Nov-27 11:47:17	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8830	39	58.46%	254	99.61%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

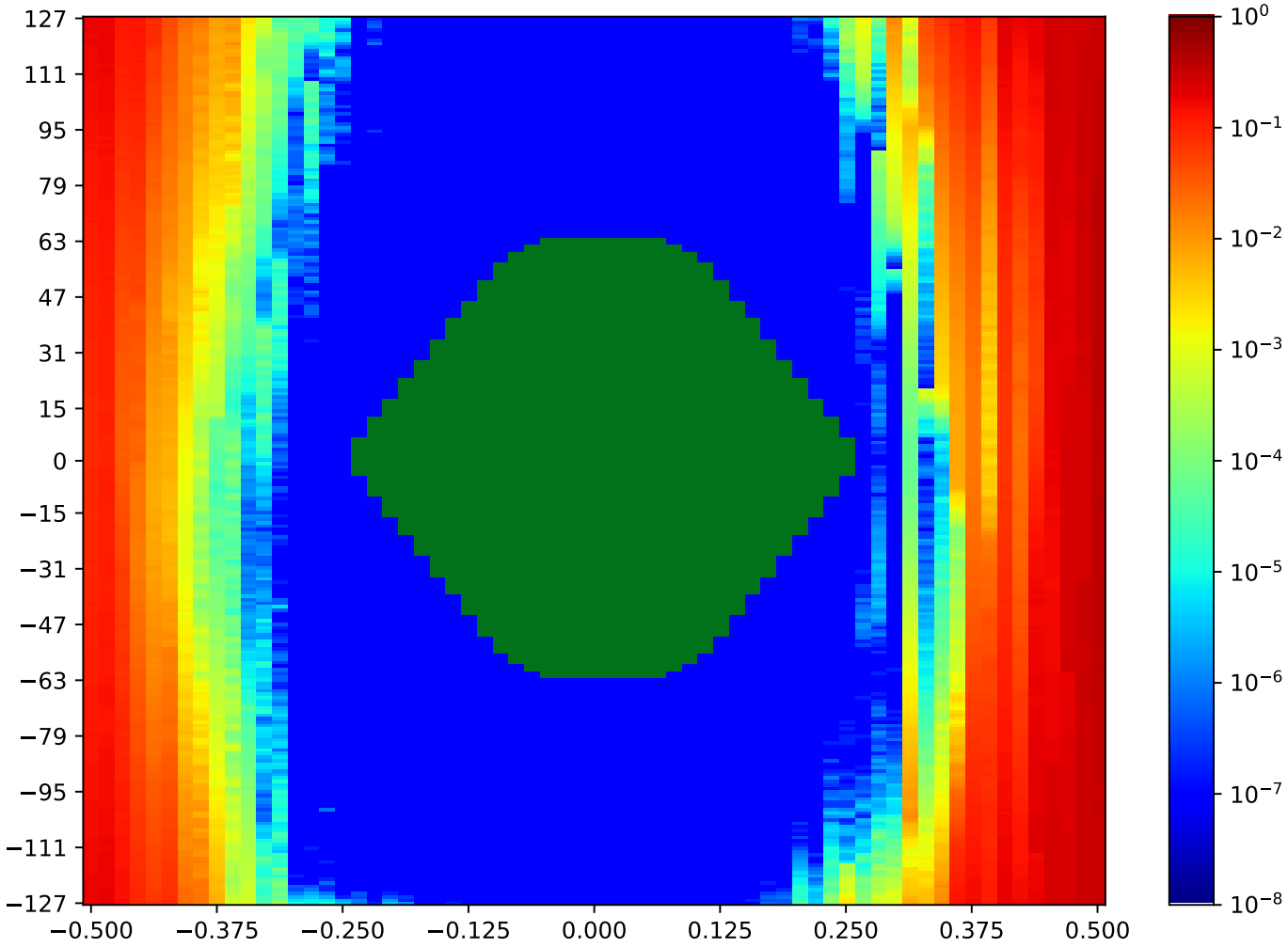


Figure 6.269: MSP_C_FPGA-TX3-02–RX3-02-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.4 MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Table 6.249: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:44:56		2019-Nov-27 11:45:19	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9239	43	66.15%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

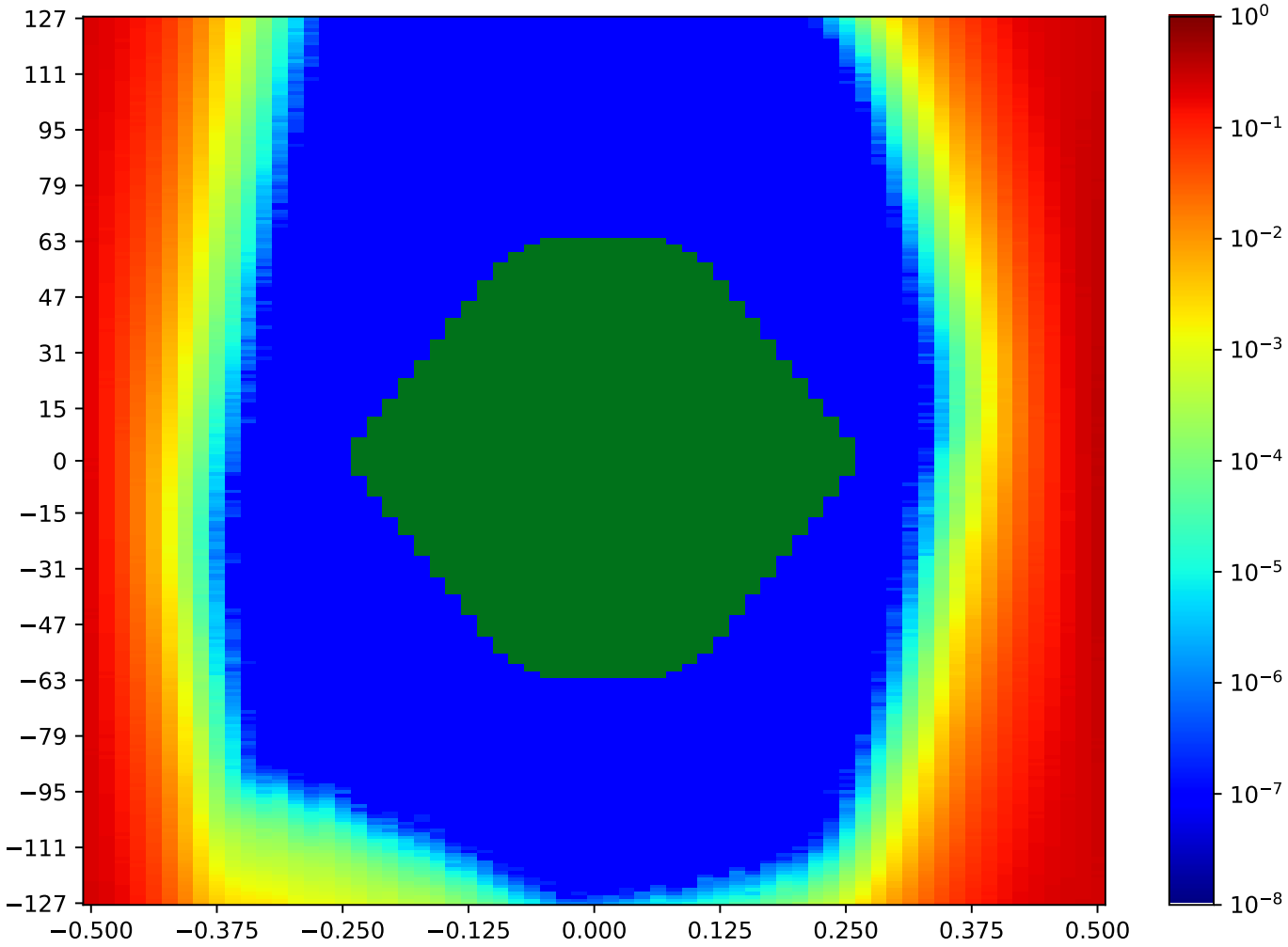


Figure 6.270: MSP_C_FPGA-TX3-03–RX3-03-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.5 MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Table 6.250: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:48:12		2019-Nov-27 11:48:37	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7505	35	53.85%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

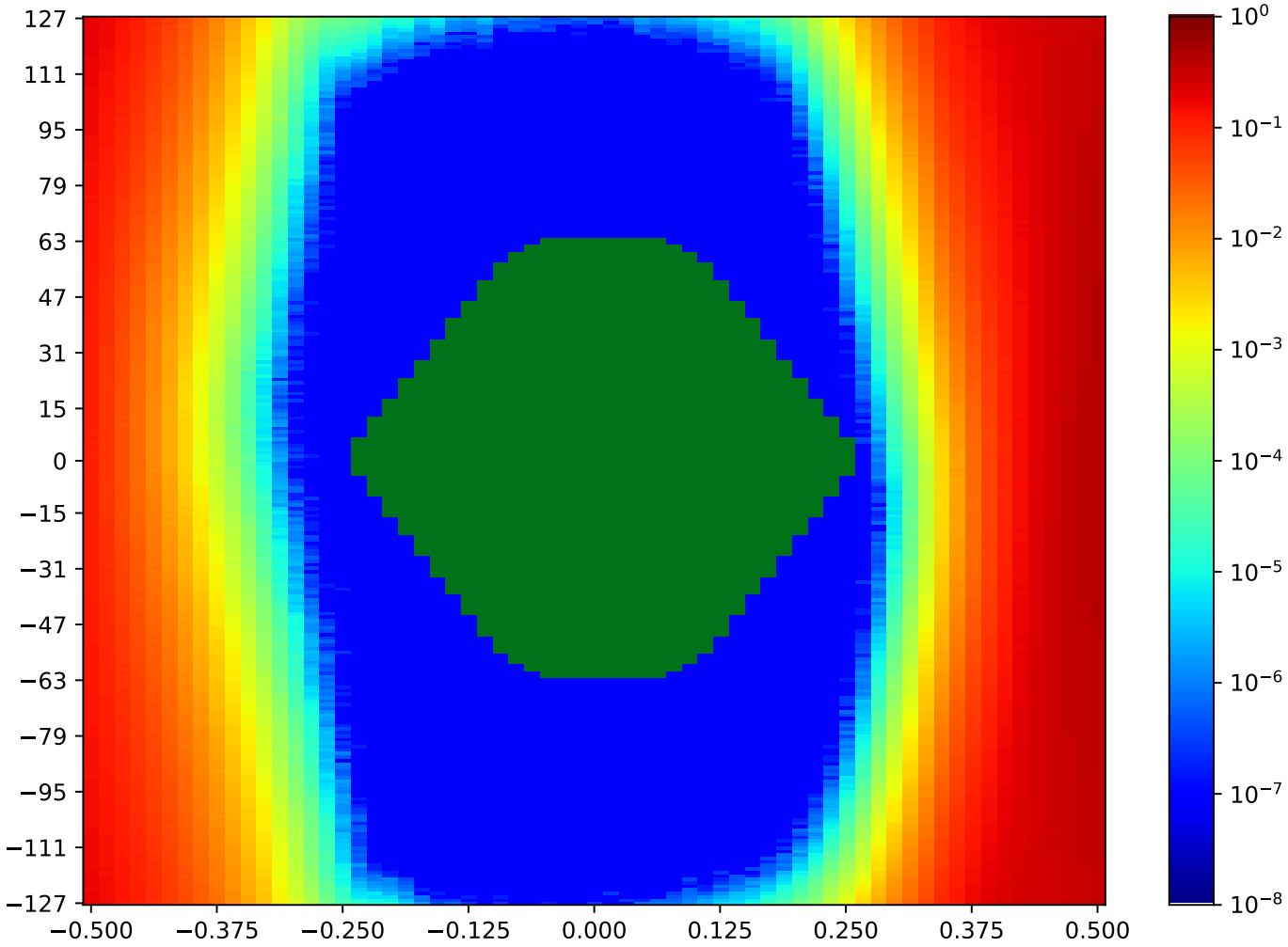


Figure 6.271: MSP_C_FPGA-TX3-04–RX3-04-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.6 MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Table 6.251: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:44:36		2019-Nov-27 11:44:55	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8711	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

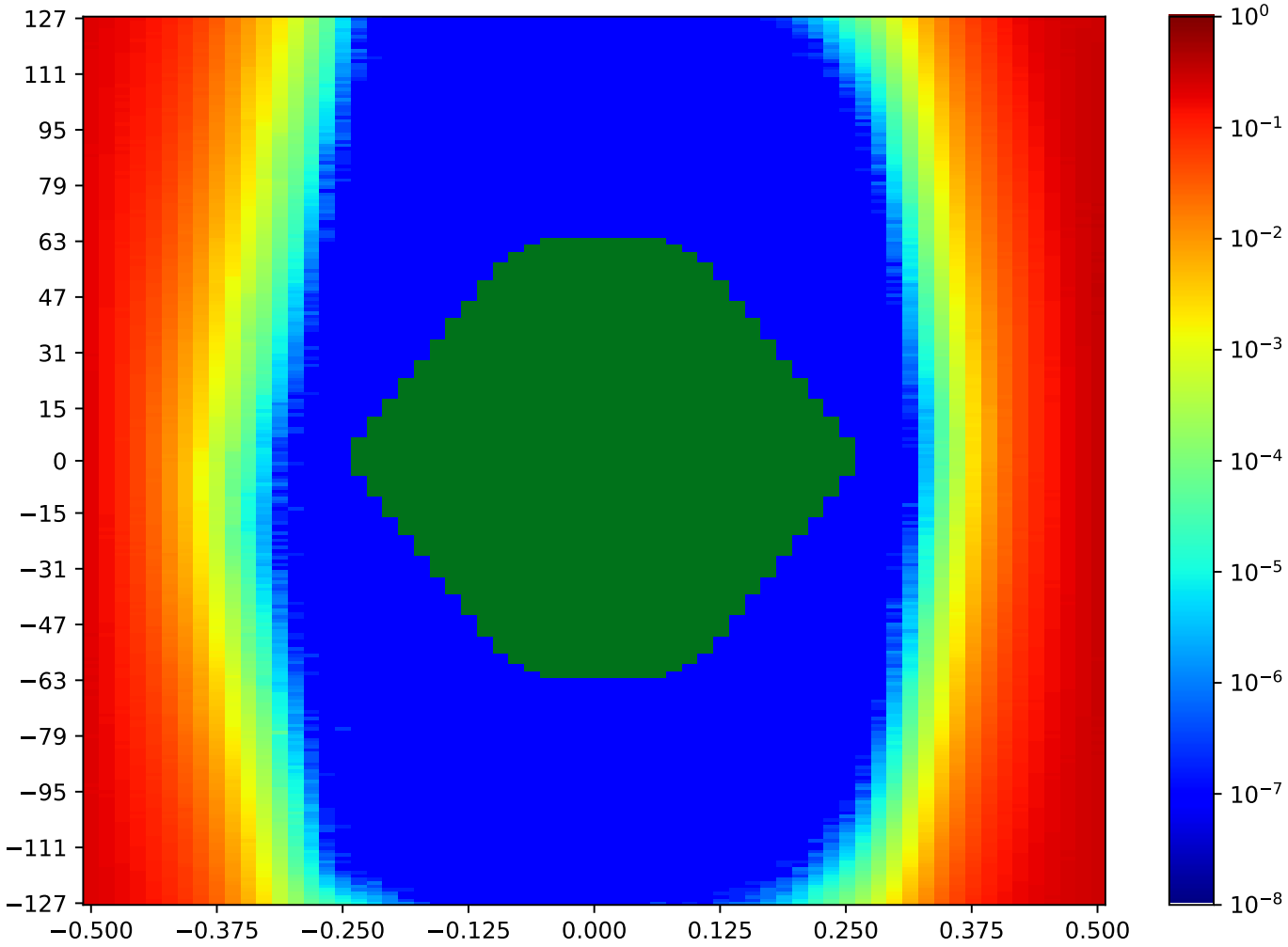


Figure 6.272: MSP_C_FPGA-TX3-05–RX3-05-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.7 MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Table 6.252: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:49:06		2019-Nov-27 11:49:34	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7195	36	55.38%	228	89.41%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

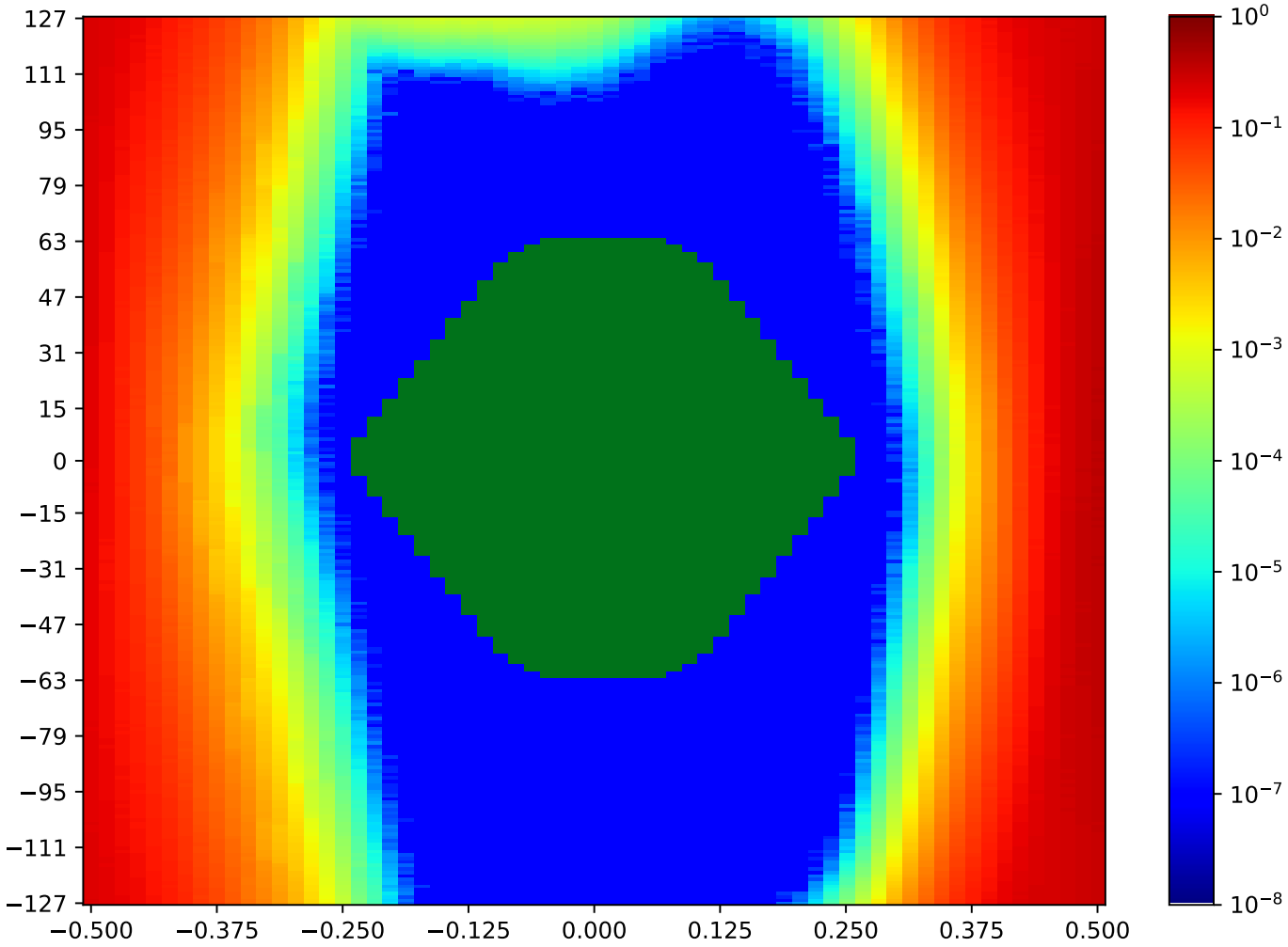


Figure 6.273: MSP_C_FPGA-TX3-06–RX3-06-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.8 MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Table 6.253: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:45:20		2019-Nov-27 11:45:39	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9348	41	63.08%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

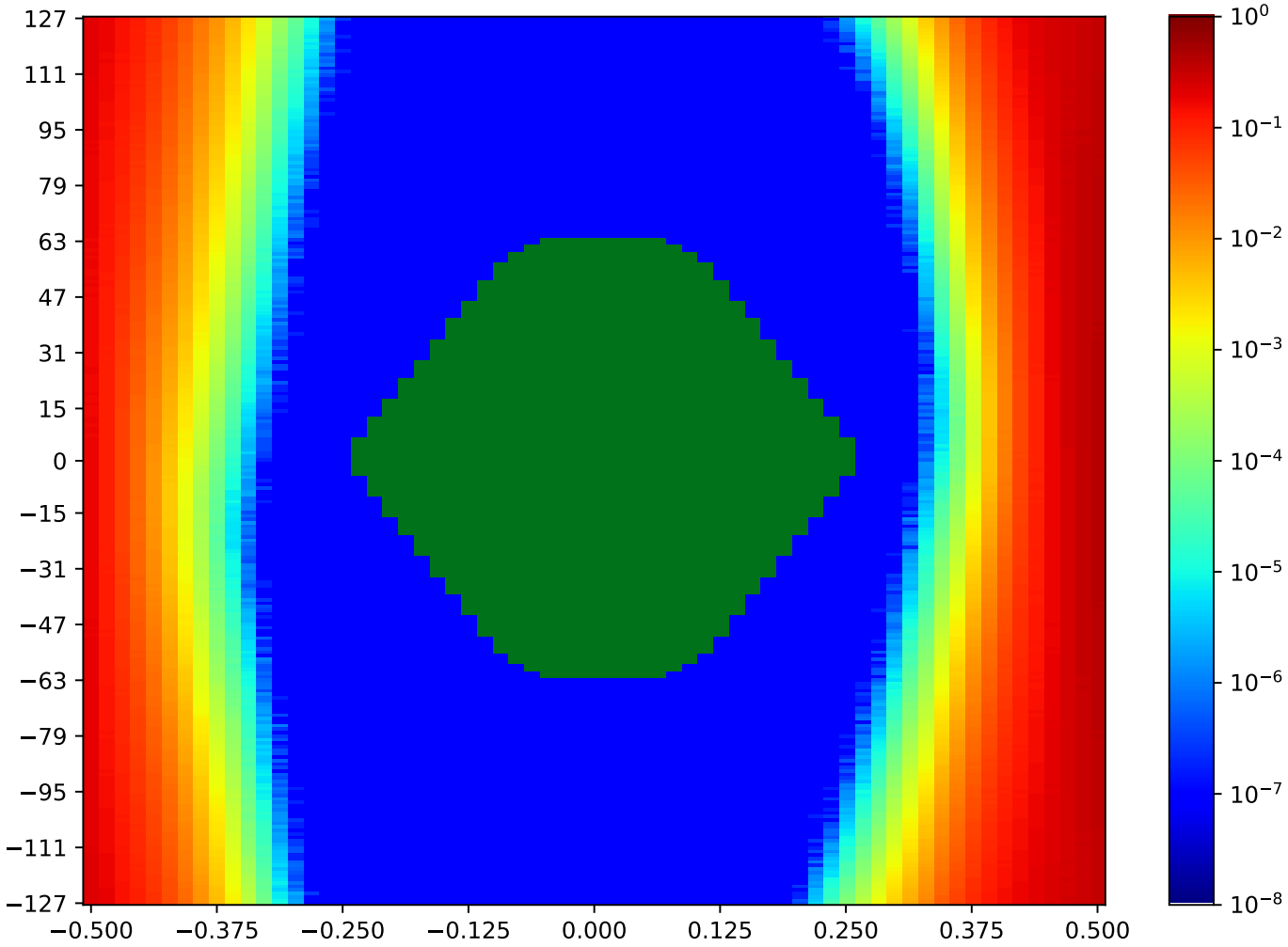


Figure 6.274: MSP_C_FPGA-TX3-07–RX3-07-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.9 MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Table 6.254: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:48:37		2019-Nov-27 11:49:06	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9751	44	67.69%	251	98.04%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

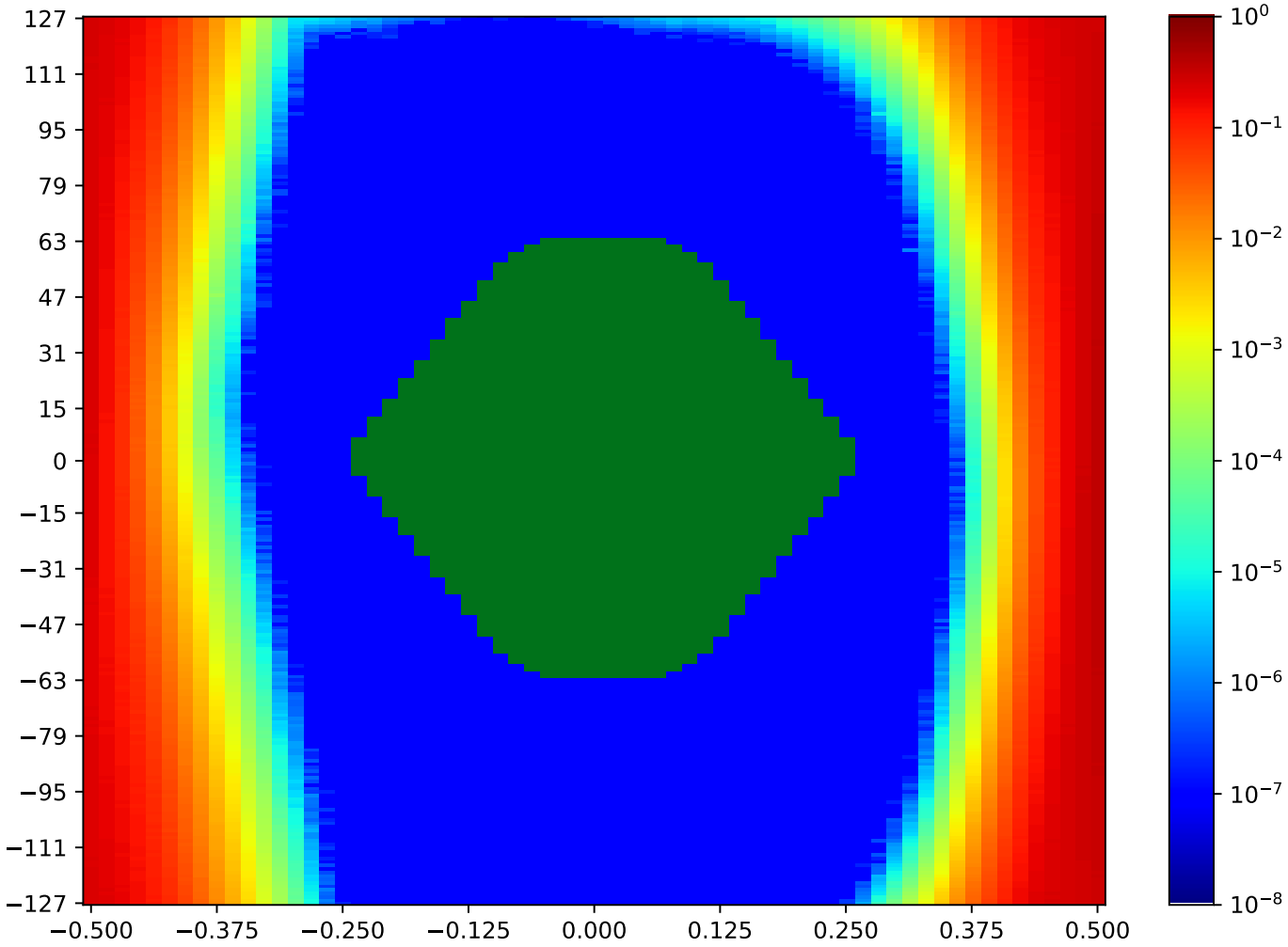


Figure 6.275: MSP_C_FPGA-TX3-08–RX3-08-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.10 MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Table 6.255: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:46:06		2019-Nov-27 11:46:32	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9527	43	66.15%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

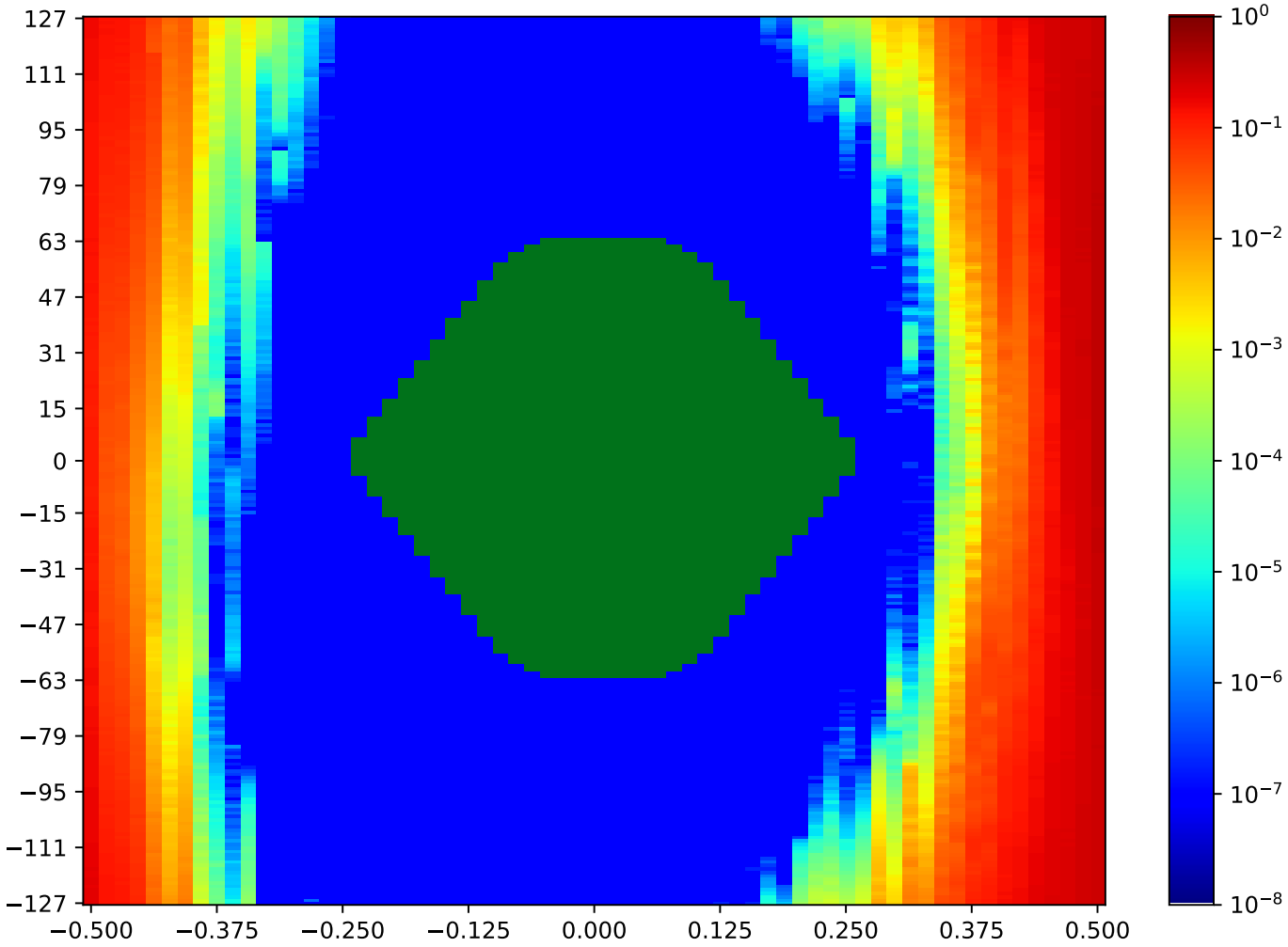


Figure 6.276: MSP_C_FPGA-TX3-09–RX3-09-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.11 MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Table 6.256: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:47:45		2019-Nov-27 11:48:12	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8583	38	58.46%	248	97.25%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

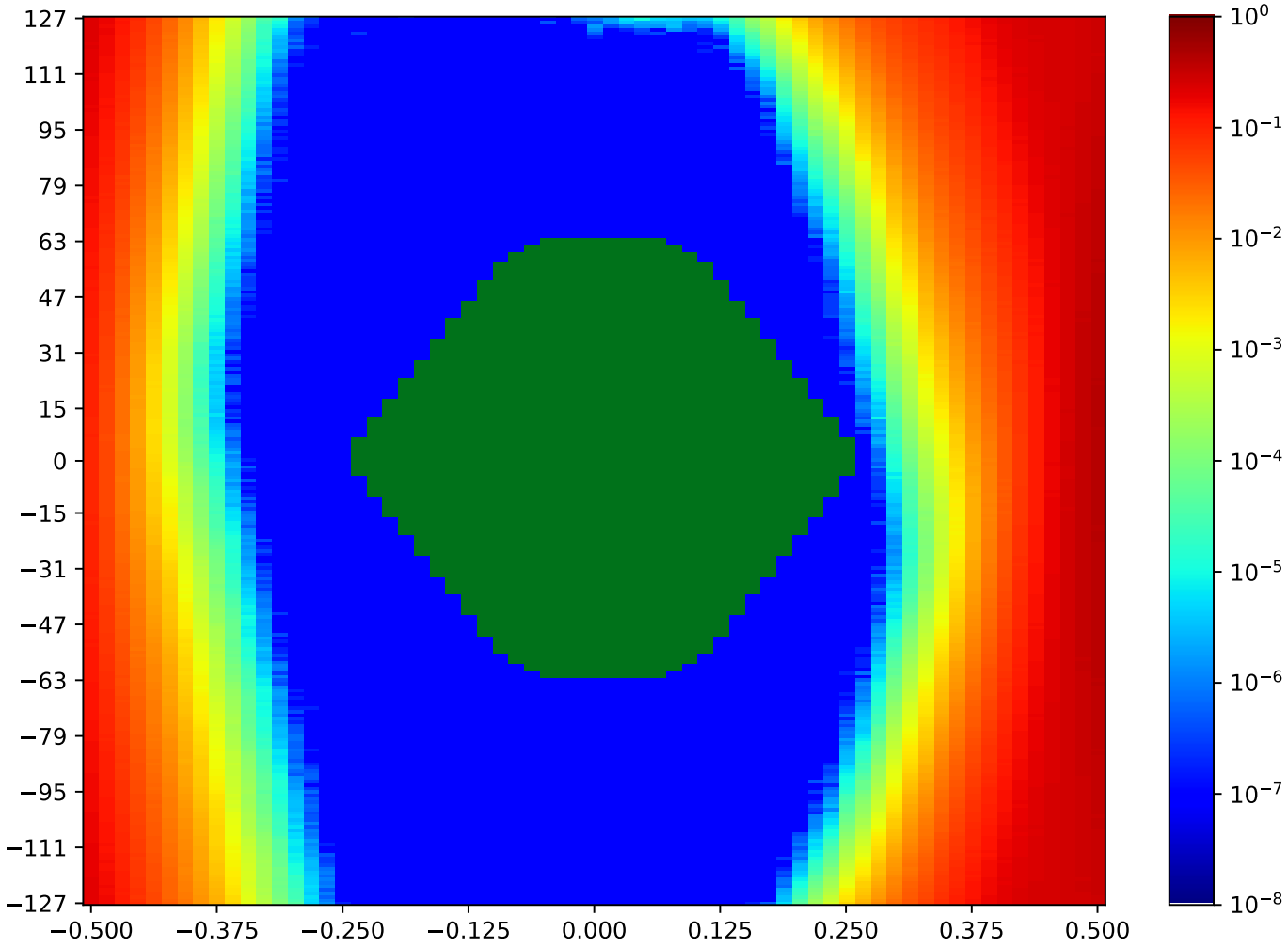


Figure 6.277: MSP_C_FPGA-TX3-10–RX3-10-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.21.12 MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Table 6.257: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:47:18		2019-Nov-27 11:47:45	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9114	41	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

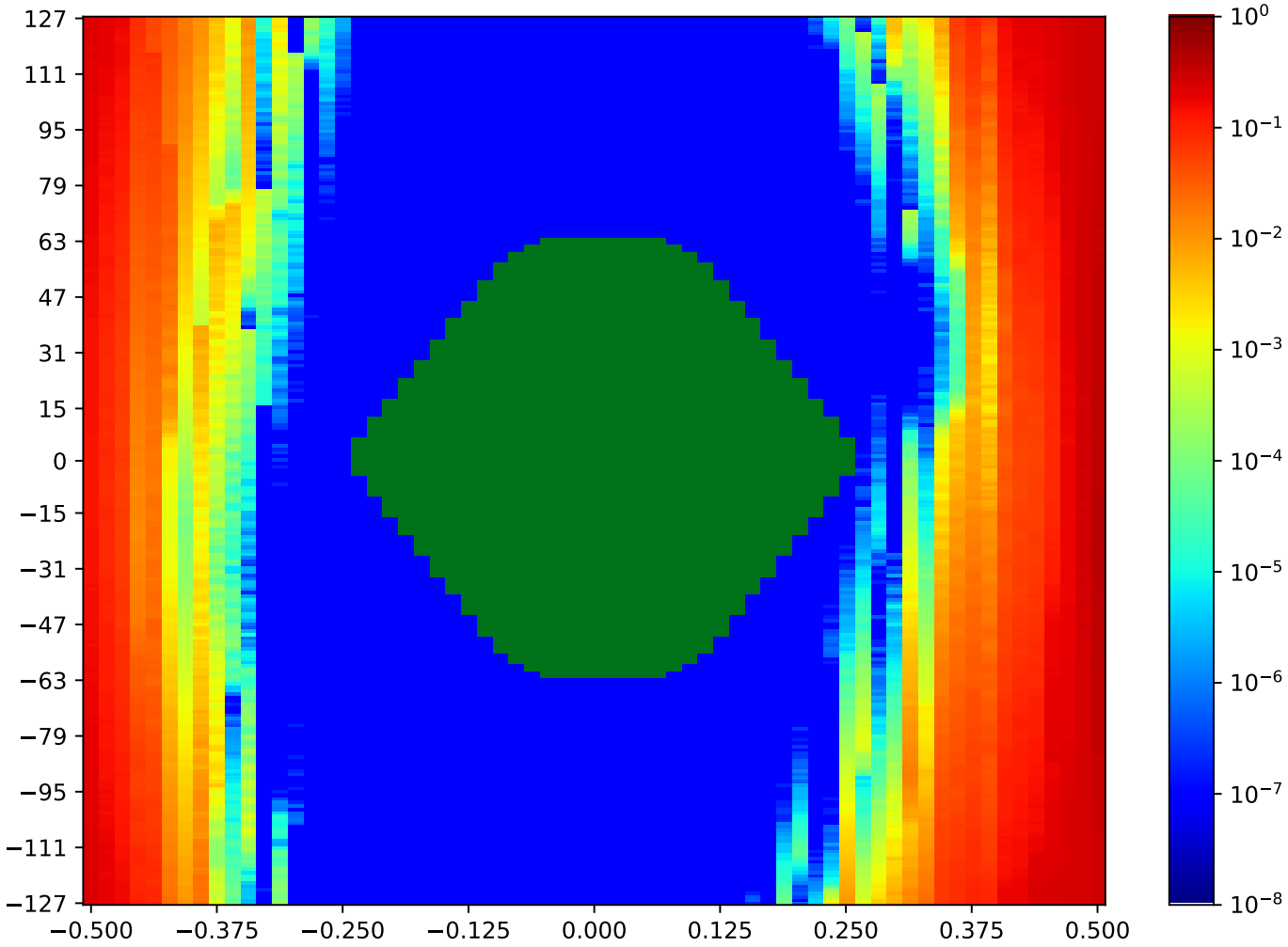


Figure 6.278: MSP_C_FPGA-TX3-11–RX3-11-MSP_A_FPGA

Call back to summary Figure 6.266. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22 MSP_C TX4 MSP_A RX4 Minipod Loopback

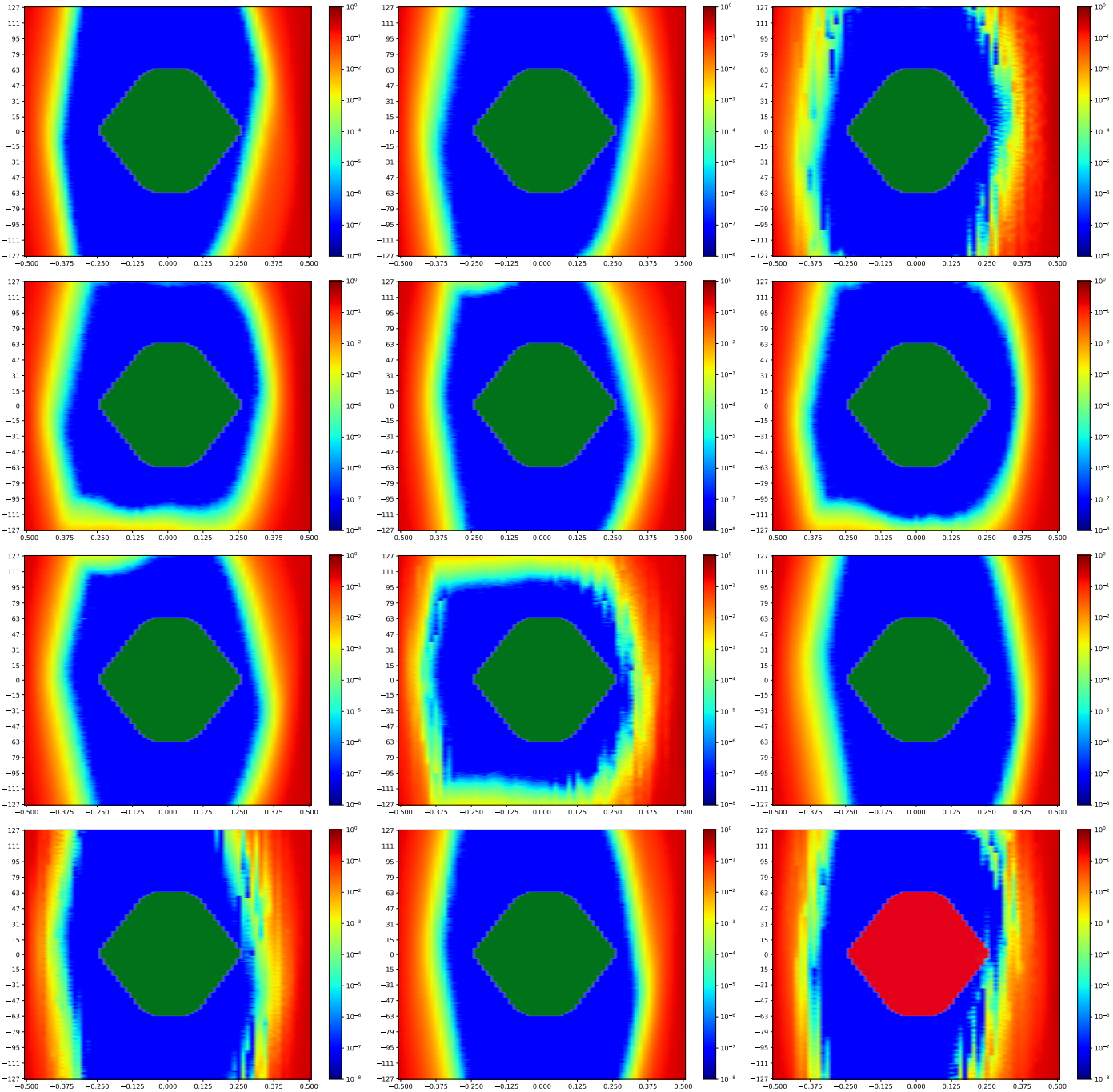


Figure 6.279: MSP_C TX4 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.
Next summary Figure 6.279.

6.22.1 MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Table 6.258: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:50:46		2019-Nov-27 11:51:13	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9264	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

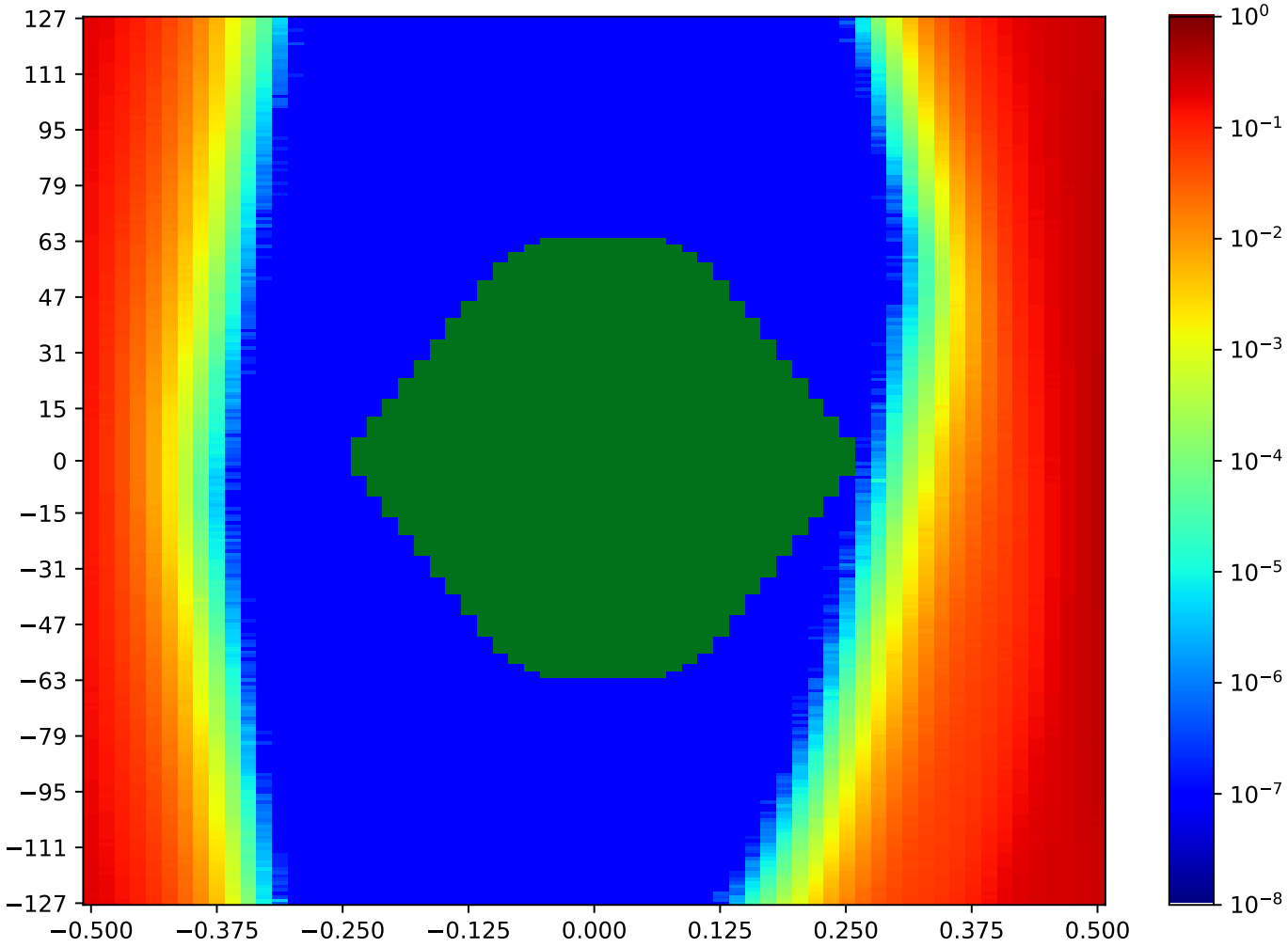


Figure 6.280: MSP_C_FPGA-TX4-00–RX4-00-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.2 MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Table 6.259: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:49:54		2019-Nov-27 11:50:18	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8755	38	58.46%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

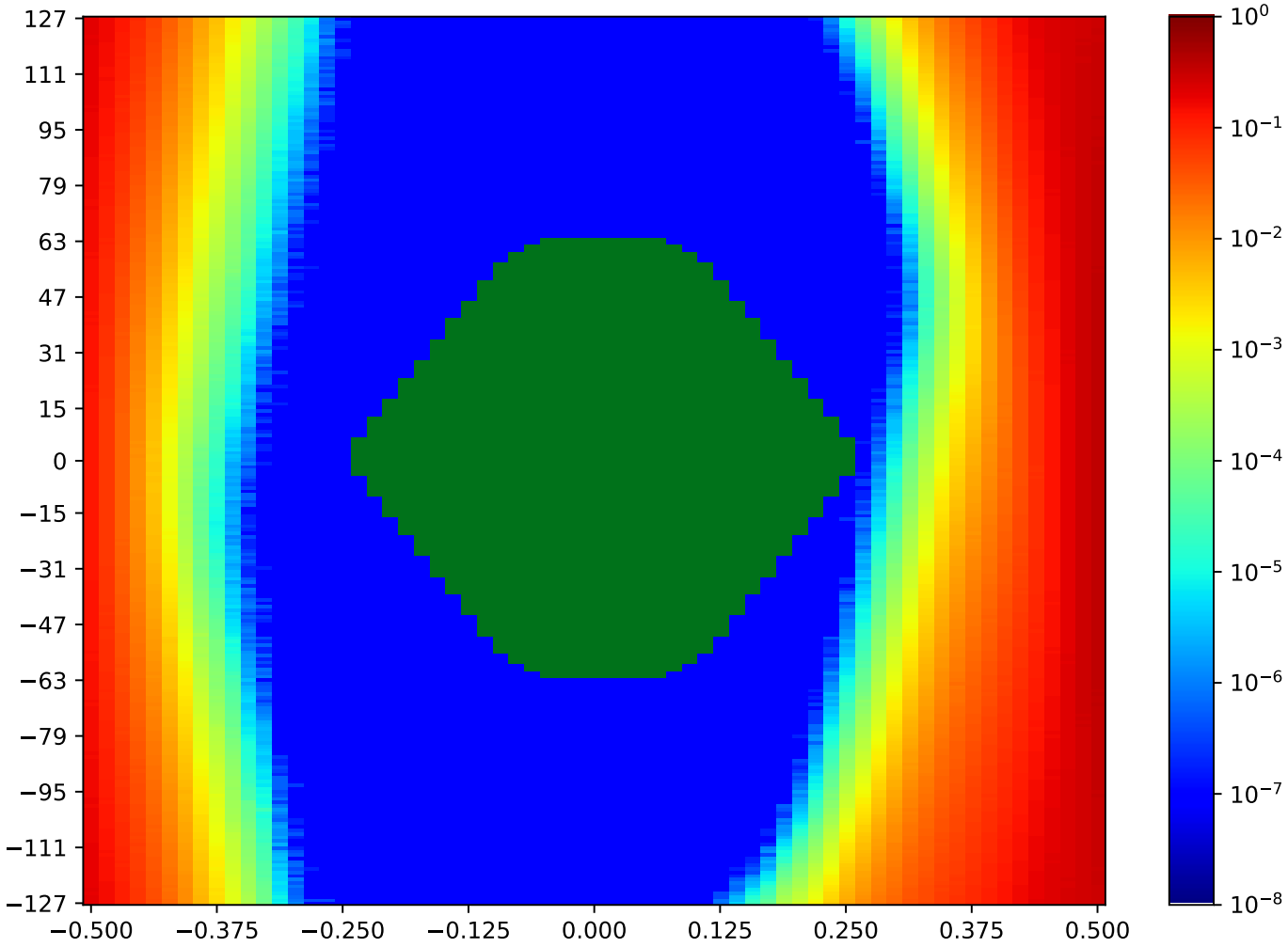


Figure 6.281: MSP_C_FPGA-TX4-01–RX4-01-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.3 MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Table 6.260: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:52:08		2019-Nov-27 11:52:36	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8448	37	56.92%	252	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

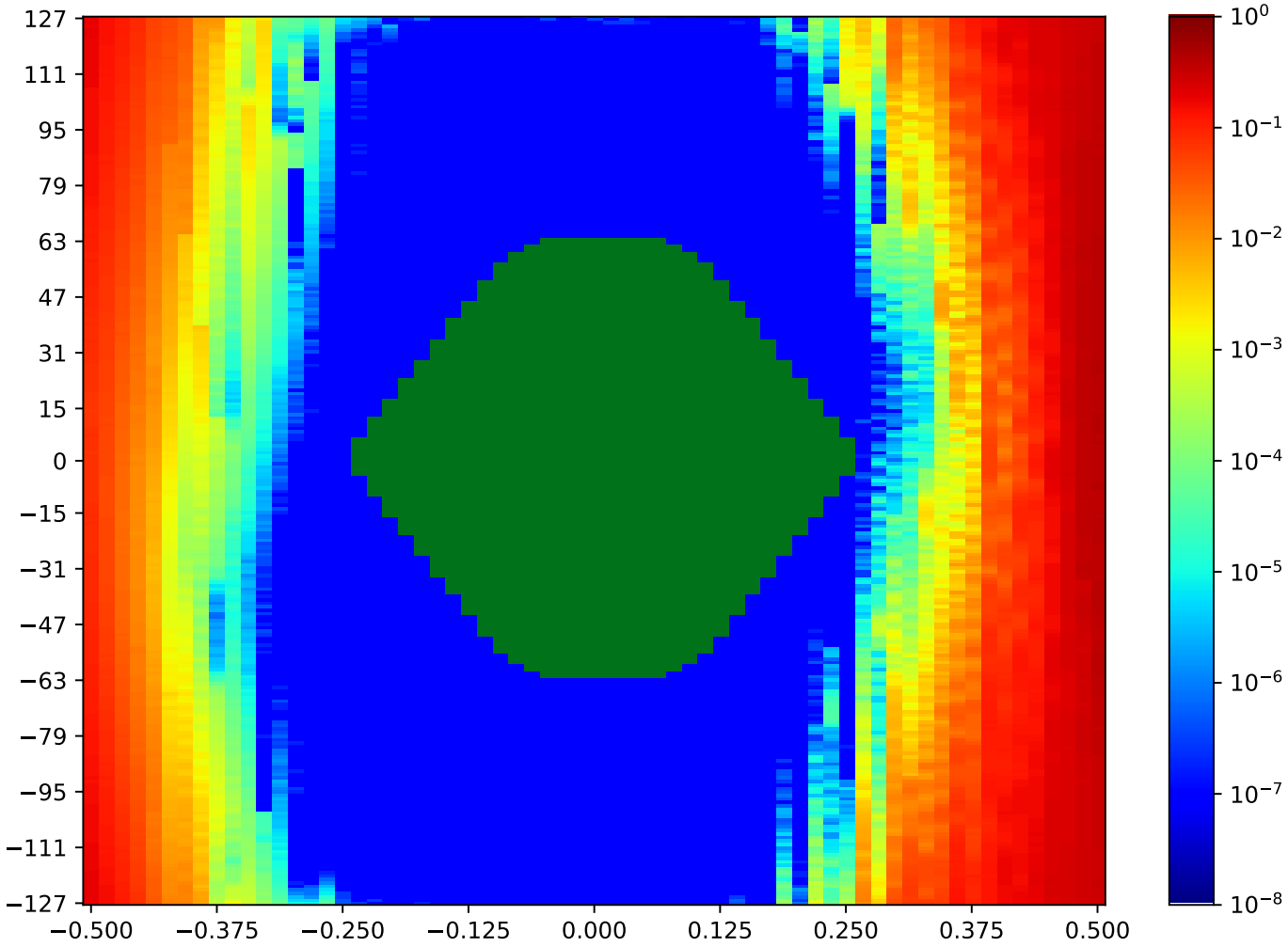


Figure 6.282: MSP_C_FPGA-TX4-02–RX4-02-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.4 MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Table 6.261: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:49:34		2019-Nov-27 11:49:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7834	40	61.54%	216	84.31%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

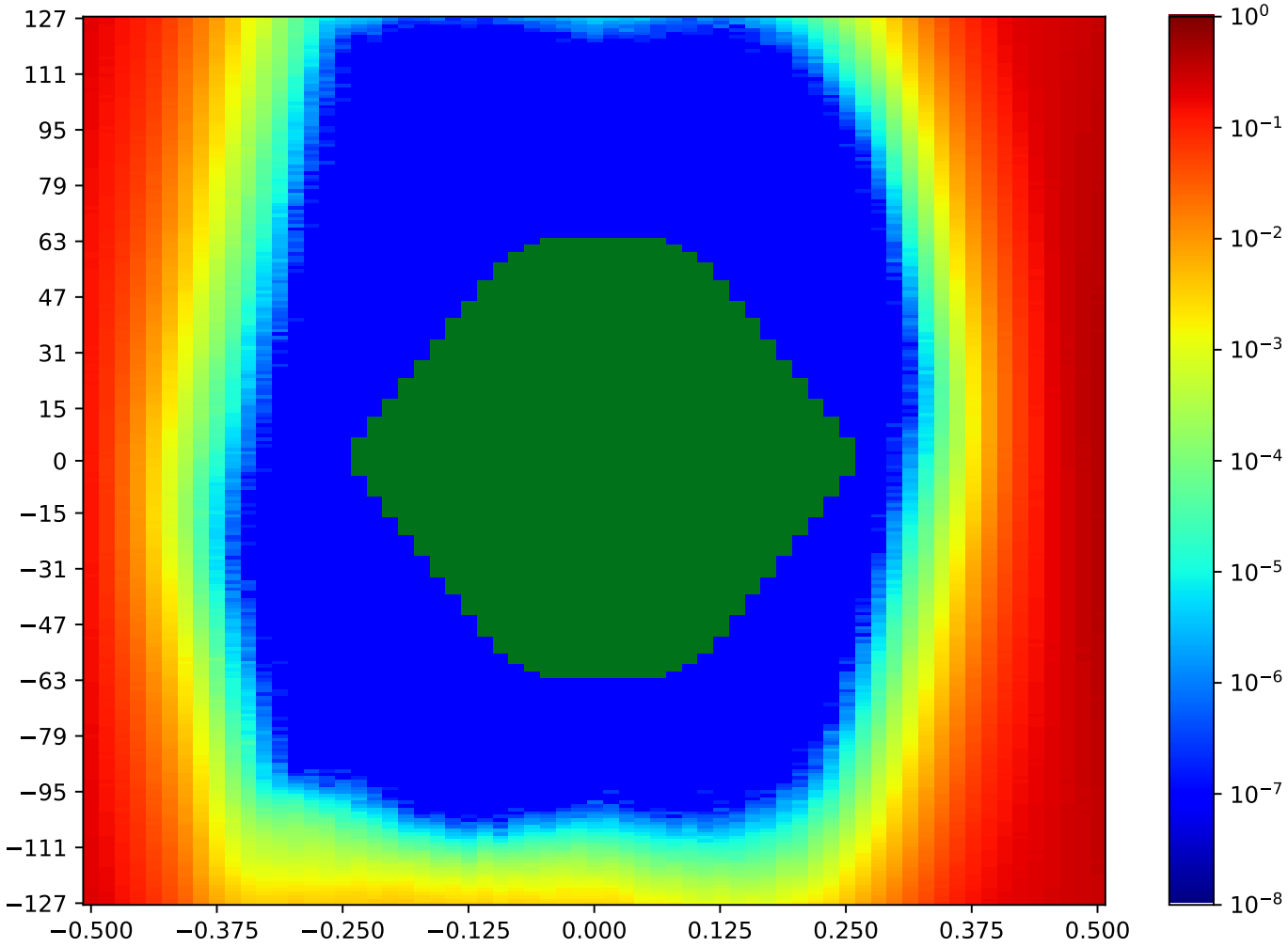


Figure 6.283: MSP_C_FPGA-TX4-03–RX4-03-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.5 MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Table 6.262: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:53:29		2019-Nov-27 11:53:57	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8299	37	56.92%	253	99.22%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

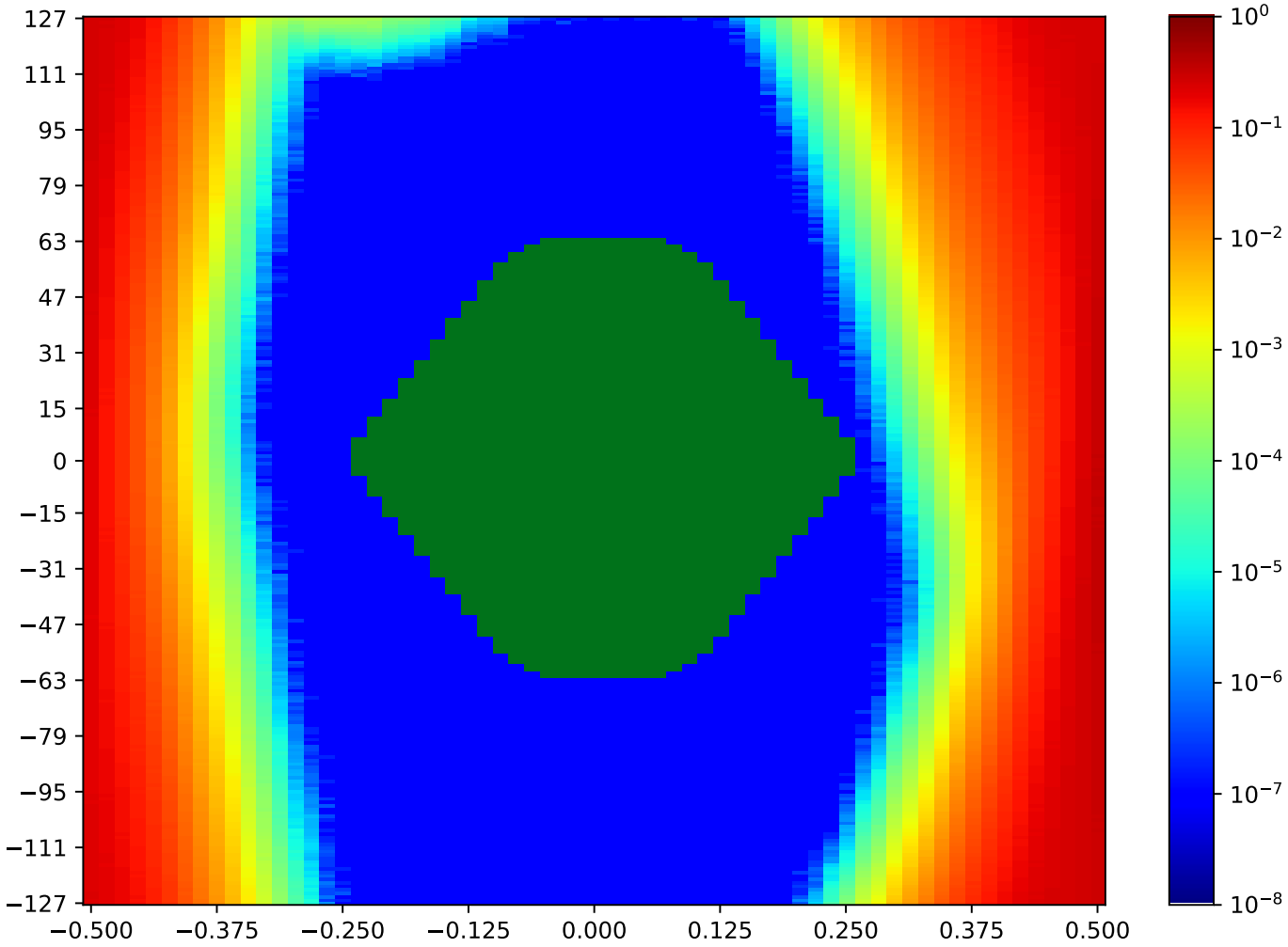


Figure 6.284: MSP_C_FPGA-TX4-04–RX4-04-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.6 MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Table 6.263: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:50:18		2019-Nov-27 11:50:46	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8697	43	66.15%	238	92.94%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

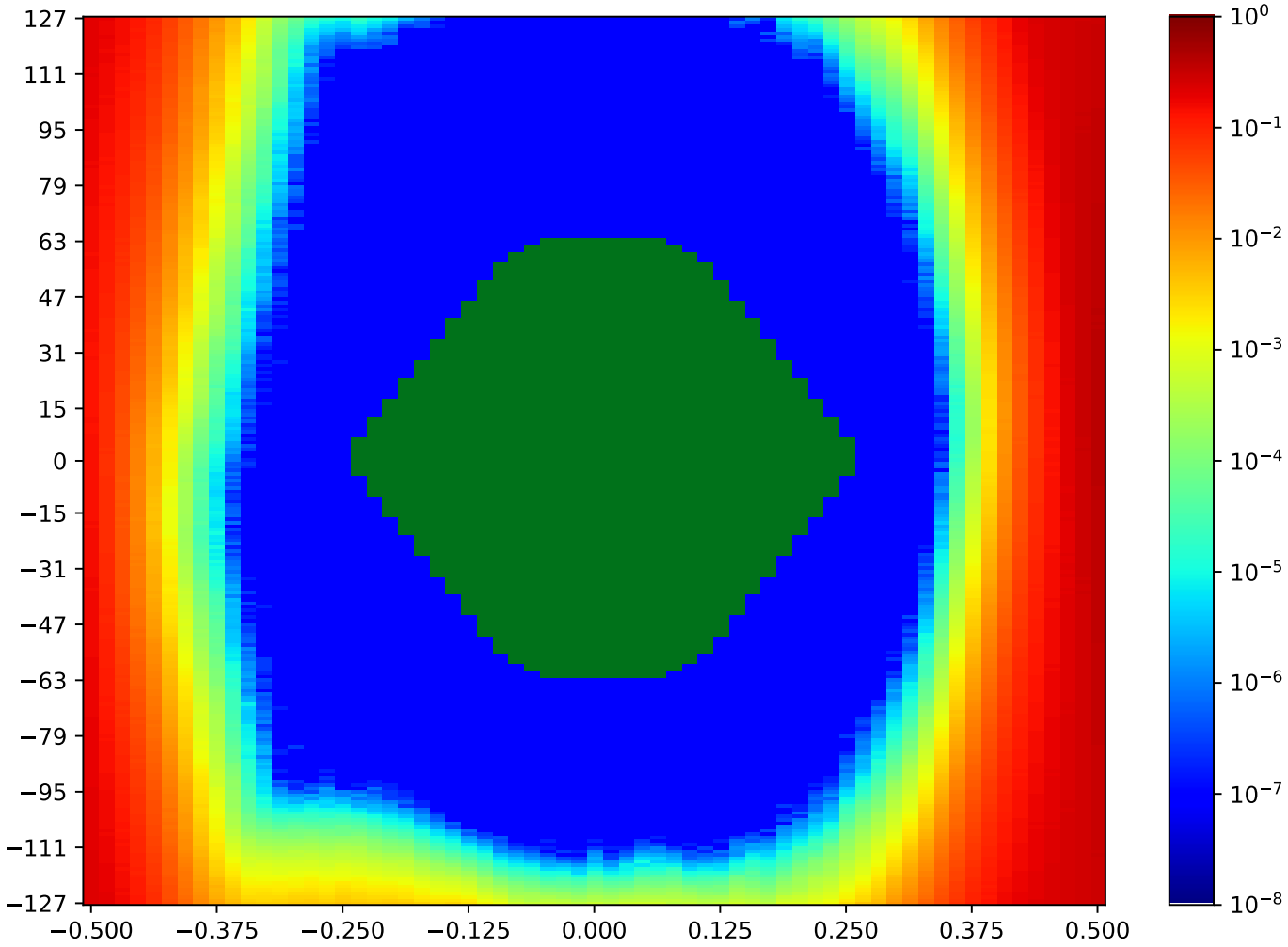


Figure 6.285: MSP_C_FPGA-TX4-05–RX4-05-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.7 MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Table 6.264: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:54:26		2019-Nov-27 11:54:54	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8483	39	60.00%	251	98.43%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

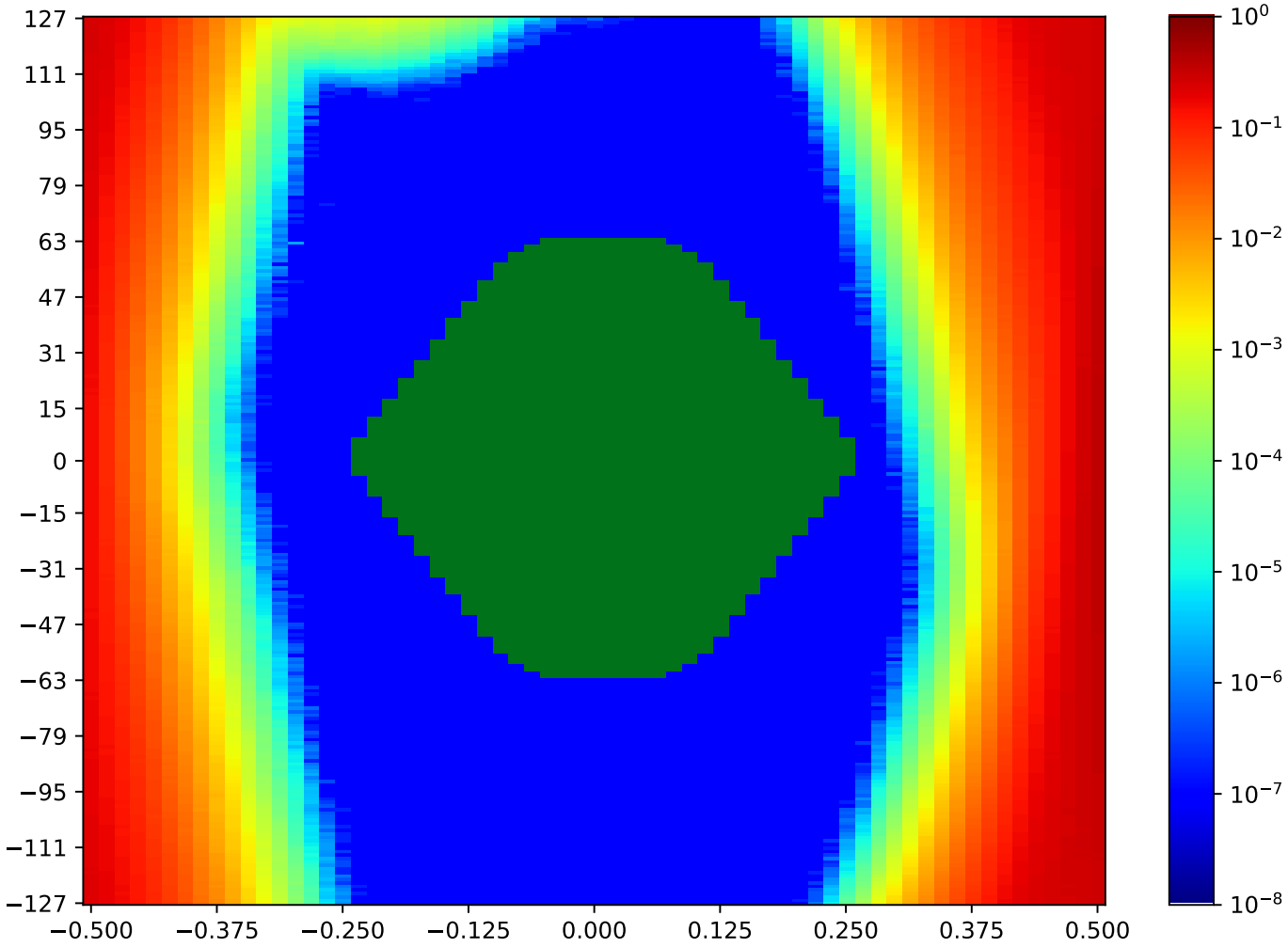


Figure 6.286: MSP_C_FPGA-TX4-06–RX4-06-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.8 MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Table 6.265: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:51:13		2019-Nov-27 11:51:40	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	7044	42	63.08%	200	75.69%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

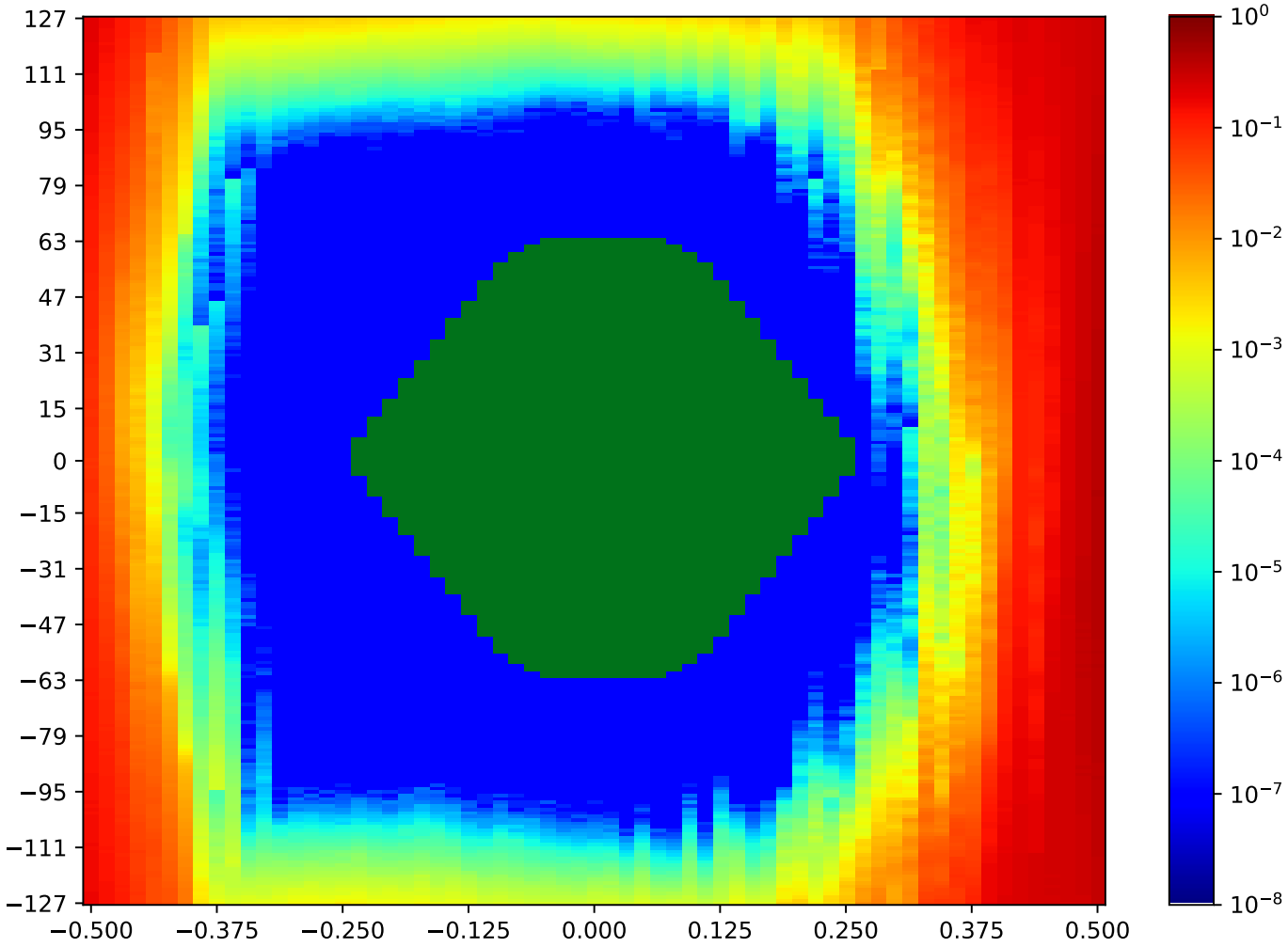


Figure 6.287: MSP_C_FPGA-TX4-07–RX4-07-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.9 MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Table 6.266: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:53:58		2019-Nov-27 11:54:26	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8928	37	56.92%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

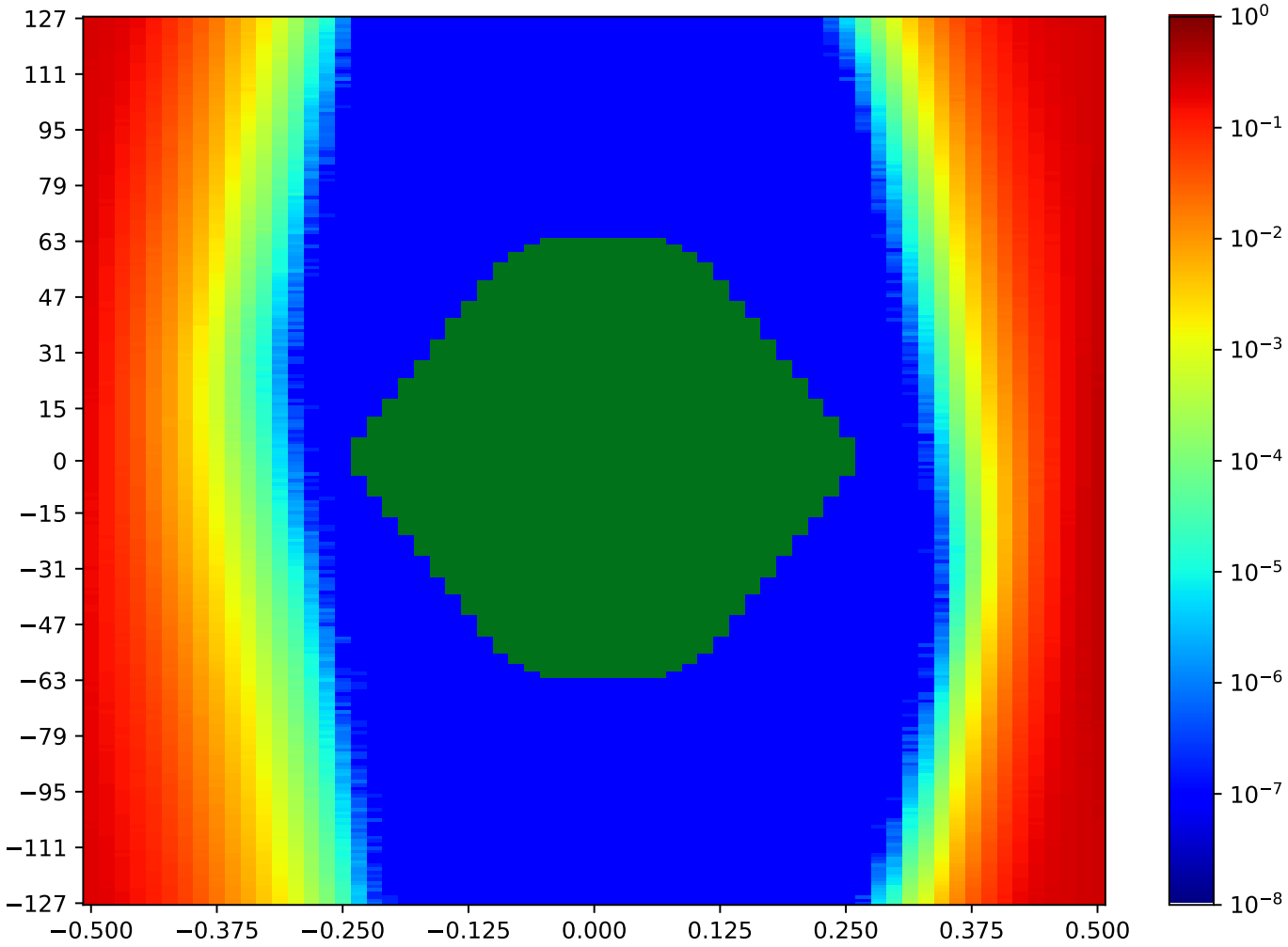


Figure 6.288: MSP_C_FPGA-TX4-08–RX4-08-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.10 MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Table 6.267: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:51:40		2019-Nov-27 11:52:08	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9086	39	60.00%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

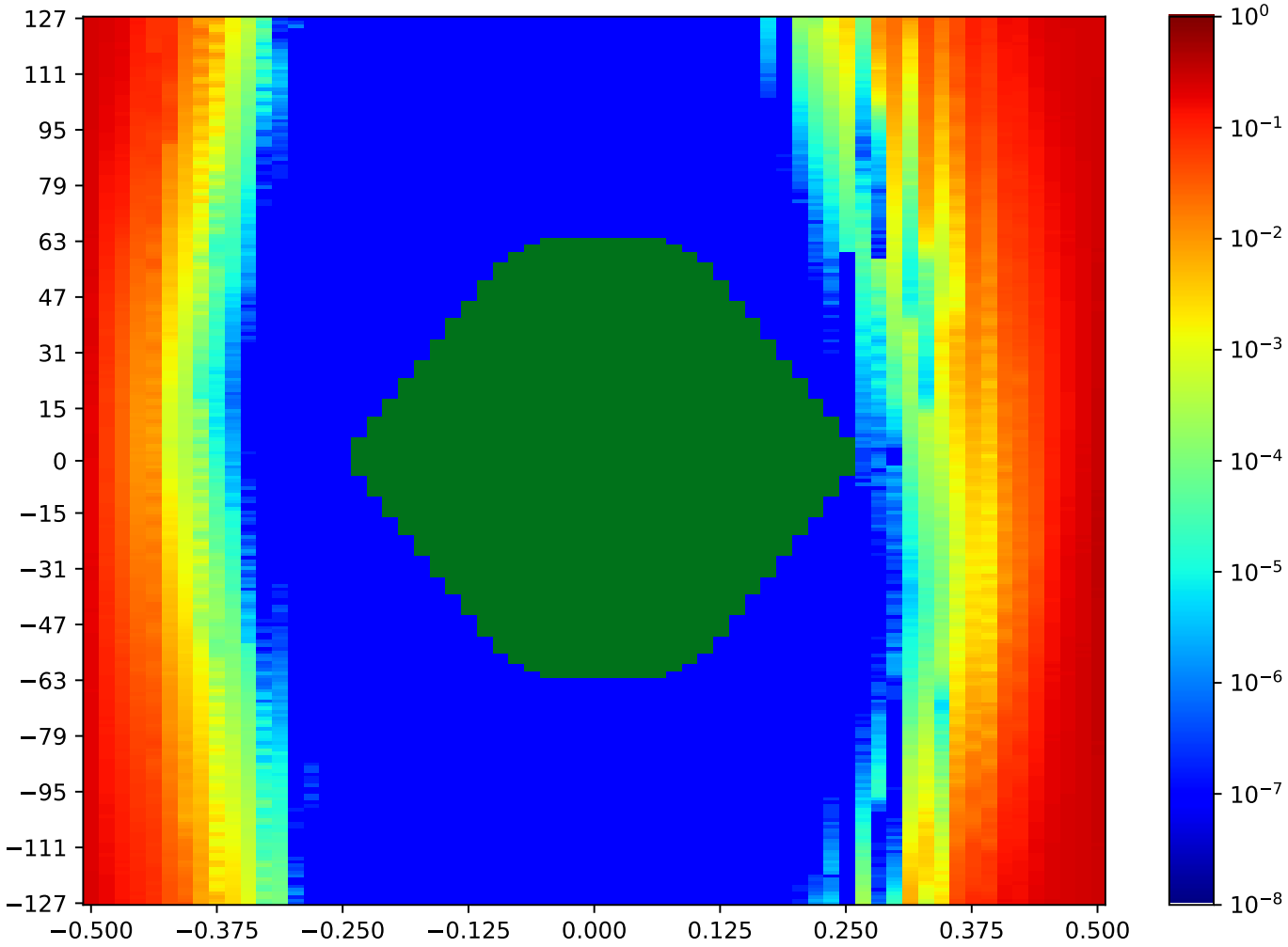


Figure 6.289: MSP_C_FPGA-TX4-09–RX4-09-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.11 MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Table 6.268: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:53:01		2019-Nov-27 11:53:29	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	9395	40	61.54%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

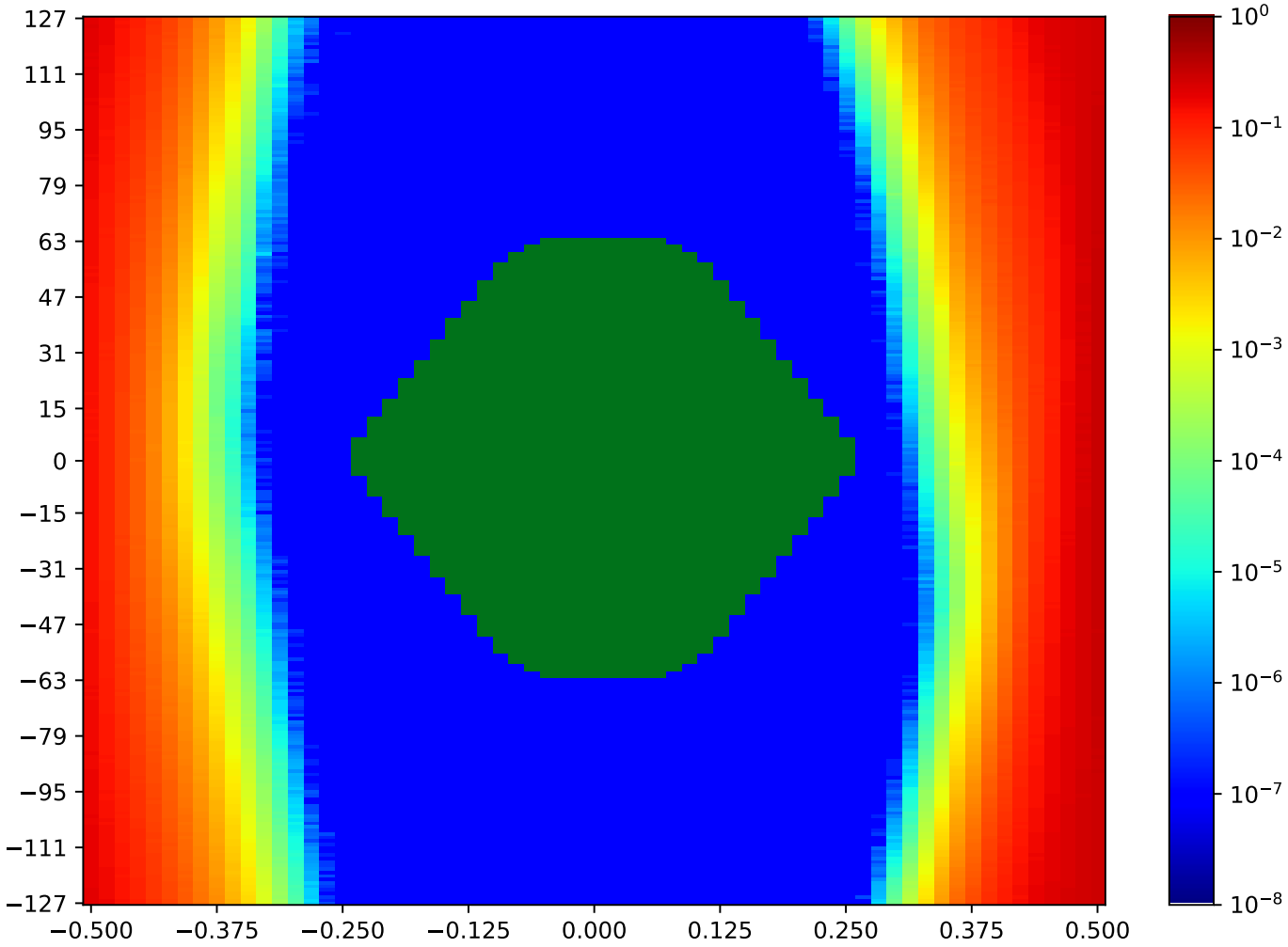


Figure 6.290: MSP_C_FPGA-TX4-10–RX4-10-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.

6.22.12 MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Table 6.269: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2018.2	UltraScale+ GTY	2019-Nov-27 11:52:36		2019-Nov-27 11:53:01	
Reset RX	**OA**	**HO**	**HO (%)**	**VO**	**VO (%)**
true	8742	39	55.38%	255	100.00%
Dwell Type	**Dwell BER**	**Horizontal Increment**	**Vertical Increment**	**Misc Info**	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

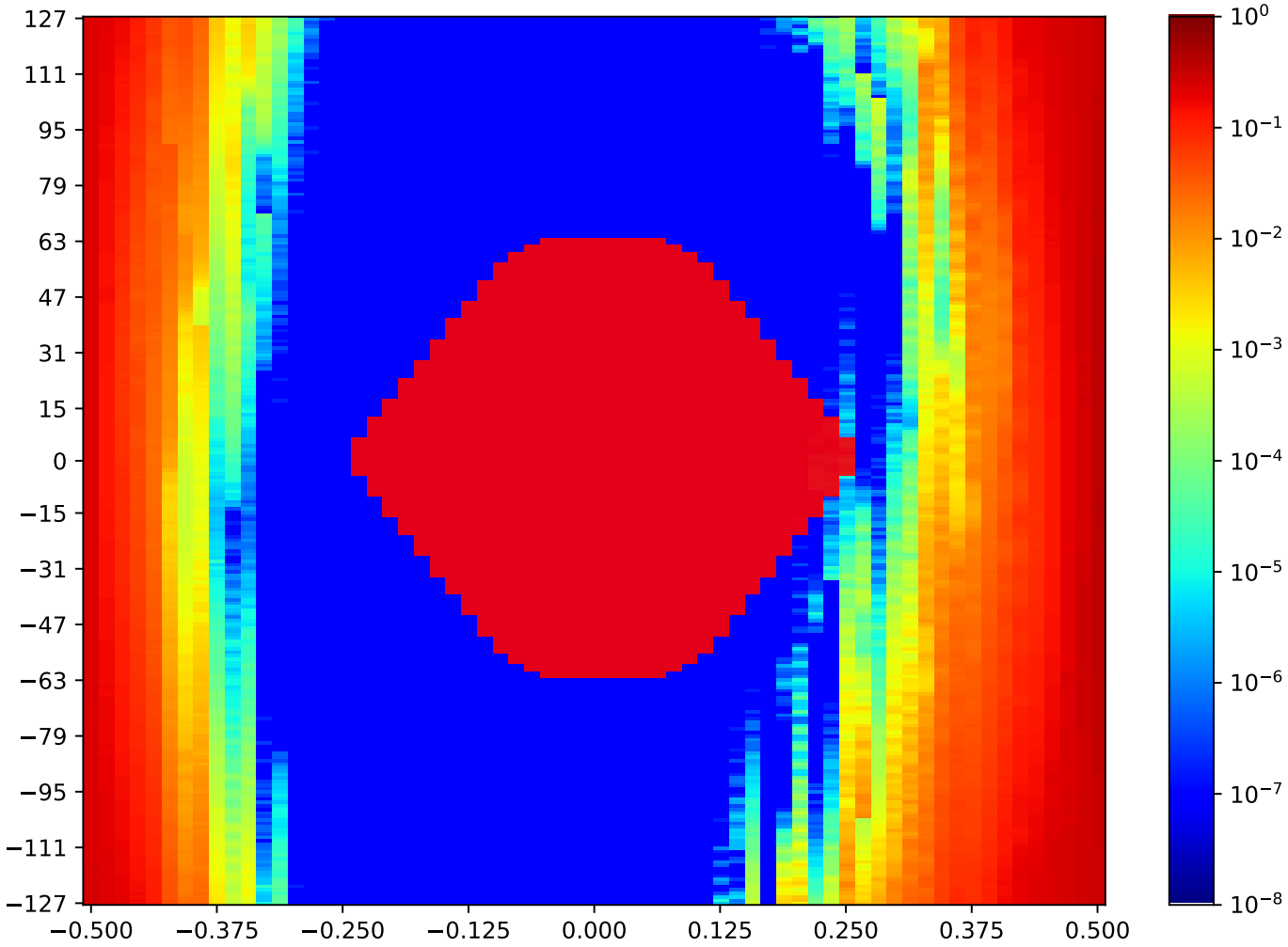


Figure 6.291: MSP_C_FPGA-TX4-11–RX4-11-MSP_A_FPGA

Call back to summary Figure 6.279. Sibling eye diagrams: V2-6.4, V2-12.8, V3-6.4.