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Programa de Pós-Graduação em Engenharia Elétrica

**Marcos Vinícius Silva Oliveira**

# The ATLAS Level-1 Muon Topological Trigger Information for Run 2 of the LHC

Juiz de Fora

2015

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Dissertação apresentada ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Juiz de Fora, na área de concentração em Sistemas Eletrônicos, como requisito parcial para obtenção do título de Mestre em Engenharia Elétrica.

Orientador: Augusto Santiago Cerqueira

Coorientador: Stefan Ludwig Haas

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**Marcos Vinícius Silva Oliveira**

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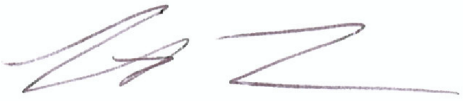
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# THE ATLAS LEVEL-1 MUON TOPOLOGICAL TRIGGER INFORMATION FOR RUN 2 OF THE LHC

Marcos Vinícius Silva Oliveira

Fevereiro/2015

Orientadores: Augusto Santiago Cerqueira
Stefan Ludwig Haas

Programa: Engenharia Elétrica

Experimentos modernos de física de altas energias têm demandando cada vez mais a utilização de técnicas avançadas de instrumentação eletrônica, devido principalmente ao grande número de sensores e a alta taxa de eventos gerados nesses experimentos, como é o caso do LHC (*Large Hadron Collider*), o maior e mais energético acelerador de partículas do mundo. Para a segunda tomada de dados do LHC, o sistema de primeiro nível de seleção *on-line* de eventos do ATLAS, um dos maiores detectores do LHC, irá adicionar informação de posição (informação topológica) dos sinais detectados pelo detector para aumentar a eficiência de seleção de eventos para variados processos de física, como o decaímento de hádron B em um par de múons de baixo momento e os decaímentos originados de processos de violação de sabor leptónico. Um dedicado Processador Topológico (L1Topo) foi desenvolvido para selecionar eventos baseados em sua topologia e fornecer o resultado para o CTP (Processador Central de Seleção de Eventos). Esta dissertação aborda o trabalho desenvolvido na atualização da Interface de Múon para o Processador Central de Seleção de Eventos (MUCTPI), que irá transmitir informação de posição de múons para o processador topológico através de saídas elétricas originalmente desenvolvidas para teste e monitoração. Portanto, um sistema de testes foi desenvolvido e resultados gerados pelo dispositivo demonstraram a viabilidade de atualização do sistema MUCTPI para que dados sejam enviados através de suas saídas elétricas com uma taxa de transmissão (320 MHz) 8 vezes maior que a taxa inicialmente prevista em projeto. Em seguida, são abordados os desenvolvimentos em FPGA do programa embarcado do sistema MUCTPI para a codificação de informação topológica de múon, bem como os desafios para o desenvolvimento de um sistema de baixa

latência. Esta inclui ainda, simulações computacionais da operação do programa embarcado desenvolvido para o sistema MUCTPI, testes no equipamento através de interfaces de monitoração e testes de integração com o processador L1Topo, que demostraram a eficácia do desenvolvimento.

Palavras-chave: MUCTPI, Seleção Topológica de Eventos, ATLAS, Primeiro Nível de Seleção de Eventos, Física de Altas Energias.

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THE ATLAS LEVEL-1 MUON TOPOLOGICAL TRIGGER INFORMATION FOR RUN 2 OF THE LHC

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Modern high-energy physics experiments, such as those taking place at the LHC (Large Hadron Collider), require the use of advanced electronic instrumentation to cope with the high number of sensor channels operating at a high rate. During the first data taking run of the LHC, the proton-proton luminosity delivered to ATLAS and CMS, two of its four detectors, made possible the discovery of the Higgs boson. For the second LHC data-taking run, the first level trigger of ATLAS will use the geometry of particle tracks (topological information) aiming at the increase of the trigger efficiency of several physics processes, such as the B-hadrons decaying to two low-$p_T$ muons and lepton flavor violation $\tau$ decays. For this purpose, a dedicated Topological Processor (L1Topo) was developed to process topological algorithms and provide additional trigger inputs to the CTP (Central Trigger Processor), which is in charge of reducing the collision rate of 40 MHz to a Level-1 event rate of 75 kHz based on event information from the calorimeters and muon spectrometer.

This dissertation presents the upgrade of the existing Muon-to-Central-Trigger-Processor Interface (MUCTPI) with the objective of transmitting muon topological information to L1Topo through electrical trigger outputs initially intended, solely, for testing and monitoring purposes. As a first step, an error-rate test system has been developed and its results have demonstrated the possibility of reliably transmitting data through the trigger outputs at 320 MHz, eight times the nominal transmission rate (40 MHz). In addition, here is presented the FPGA firmware developments for the MUCTPI to encode and transmit the muon topological information. Furthermore, this work includes computer simulations of the MUCTPI firmware operation, hardware tests using the debugging interface, and integration

tests with L1Topo processor, which have demonstrated the functionality of the upgraded MUCTPI system.

Keywords: MUCTPI, Topological Trigger, ATLAS, Level-1 Trigger, High Energy Physics.

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# Acronyms

**API** Application Programming Interface

**ATCA** Advanced Telecommunications Computing Architecture

**ATLAS** A Toroidal LHC AparatuS

**BER** Bit Error Rate

**CERN** European Organization for Nuclear Research

**CMS** Compact Muon Solenoid

**CPLD** Complex Programmable Logic Device

**CSC** Cathode Strip Chambers

**CTP** Central Trigger Processor

**DAQ** Data Acquisition

**DDR** Double Data Rate

**DDR3** $3^{rd}$ generation of Double Data Rate DRAM

**ECL** Emitter-Coupled Logic

**FIFO** First In First Out

**FMC** FPGA Mezzanine Card

**FPGA** Field Programmable Gate Array

**FSM** Finite State Machine

**HEP** High Energy Physics

**HL-LHC** High Luminosity LHC

**HLT** High-Level Trigger

**HTML** HyperText Markup Language

**ILA** Integrated Logic Analyzer

**IP** Internet Protocol

**L1Calo** Level-1 Calorimeter Trigger

**L1Muon** Level-1 Muon Trigger

**L1Topo** Level-1 Topological Trigger Processor

**LFSR** Linear Feedback Shift Register

**LHC** Large Hadron Collider

**LTP** Local Trigger Processor

**LUT** Look up Table

**LVDS** Low-Voltage Differential Signaling

**MAC** Media Access Control layer

**MDT** Monitored Drift Tubes

**MIBAK** Muon Interface Backplane

**MICTP** Muon Central Trigger Processor Interface Module

**MIOCT** Muon Interface Octant Module

**MIROD** Muon Interface Readout Driver Module

**MIRODCTP** Muon Interface ROD & CTP

**MSB** Most Significant Bit

**MTCA** Micro Telecommunications Computing Architecture

**MUCTPI** Muon-to-Central-Trigger-Processor Interface

**MuCTPiToTopo** MUCTPI-to-Level-1-Topological-Processor interface

**Nikhef** National Institute for Subatomic Physics

**NIM** Nuclear Instrumentation Module

**PLL** Phase-Locked Loop

**PRBS** Pseudo Random Bit Sequence

**QDR** Quad-Data Rate

**ROD** Readout Driver

**RoI** Region-of-Interest

**ROL** Readout Link

**ROS** Readout Subsystem

**RPC** Resistive Plate Chamber

**SBC** Single-Board Computer

**SODIMM** Small Outline Dual In-line Memory Module

**SONET** Synchronous Optical Networking

**SRAM** Static Random-Access Memory

**TCDS** Trigger, Control and Distribution System

**TDAQ** Trigger and Data Acquisition

**TGC** Thin Gap Chamber

**TTC** Timing, Trigger and Control

**UDP** User Datagram Protocol

**USB** Universal Serial Bus

**VHDL** VHSIC Hardware Description Language

**VME** Versa Module Europa

# Chapter 1

# Introduction

Modern High Energy Physics (HEP) Experiments require advanced electronic instrumentation systems to acquire and process physics event data at high rates from thousands of channels that receive signals generated by sensors on the detector. Such processing requires on-line filtering, also known as triggering, in order to select the potentially interesting events. This filtering process performed by trigger systems has to be carried out in a short period. Hence, algorithms to choose these events are implemented in hardware.

The digital processing of the off-detector electronics systems is primarily implemented using Field Programmable Gate Array (FPGA) devices, given that FPGAs offers high processing capacity and re-programmability, i.e. the capability of changing the logic.

This work will present the upgrade of the existing muon trigger interface (MUCTPI) for the trigger system of the A Toroidal LHC AparatuS (ATLAS) experiment, one of the detectors at the world's largest and most powerful particle collider, the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN).

The ATLAS trigger system is segmented into three levels: the first level is implemented using custom electronics, while the second and third levels, the so-called High-Level Trigger (HLT), is built with commercial computers, network switches, and custom software.

At the LHC, the rate of bunches of particles crossing at the interaction point is 40 MHz. Each bunch contains approximately 115,000 million protons and, on average, only 25 of them collide at the interaction point, resulting in an interaction rate of $\approx 1\,\text{GHz}$. The first level trigger reduces the rate down to 75 kHz with a very short latency budget of only $2.5\,\mu\text{s}$. Therefore, a very fast selection of the potentially interesting events is required at this level.

## 1.1 Goals

In the ATLAS experiment, the Level-1 trigger decision is based on information about trigger objects coming from the calorimeters and the muon spectrometer. The muon trigger system sends information about muon candidates to the MUCTPI, which, in its turn, counts the number of muon candidates in each bunch crossing and sends it to the central trigger processor (CTP). The MUCTPI also stores the full information about muon candidates and makes it available to the HLT in case the Level-1 trigger accepts the event. The geometry of all particle tracks from one event (topological information) is available only for the HLT, however physics analysis indicated that the trigger efficiency for several physics processes could be significantly improved by using the topological information already in the Level-1 trigger system.

The MUCTPI firmware was then upgraded in order to transmit muon topological information to a new trigger processor (L1Topo). L1Topo selects events using algorithms based on the topological information by performing cuts on the effective masses or the angle between particle tracks. Events passing the topological trigger criteria are flagged and sent to the CTP, which takes the final Level-1 decision.

This work began with a technical feasibility study of the MUCTPI upgrade, an essential step to determine the maximum speed at which the MUCTPI was able to transmit data reliably through the electrical trigger outputs.

For this purpose, an error rate test system has been developed to check the reliability of data transmission from the MUCTPI. Using this test system, a high-resolution phase scan was performed on the transmitted data, showing a very low Bit Error Rate (BER) and a significant timing margin.

After reliable data transmission had been demonstrated, the firmware of the MUCTPI was upgraded in order to deliver muon topological information to L1Topo. The firmware upgrade consisted of extracting and encoding the muon candidates information according to their geometric coordinates $\eta$ and $\phi$ and transverse momentum $p_T$, and serializing the encoded information at a bit rate of 320 Mbps.

In addition, control and monitoring interfaces were added to the MUCTPI. Using these interfaces, hardware tests were performed to check the functionality of the upgraded system.

Moreover, the error rate test system was upgraded in order to receive the muon-encoded information from the MUCTPI and write it into a high-speed memory. Using the test system, the data transmission and reception of the encoded muon information was checked, comparing the data written to memory to the reference data.

The first integration test with the L1Topo was performed and successful data

transmission was established. The results of the integration tests show that the MUCTPI is ready for commissioning tests in the ATLAS experiment.

## 1.2 Document structure

In Chapter 2, CERN, the LHC, ATLAS, and the Level-1 trigger will be presented in more detail. The muon trigger detectors and the MUCTPI system will be introduced in Chapter 3. Chapter 4 introduces the error rate test system that was developed to investigate the technical feasibility of the MUCTPI upgrade. Chapter 5 presents the MUCTPI firmware upgrade and the verification tests. In Chapter 6, results from the integration tests are shown. Finally, the conclusion is given in Chapter 7.

# Chapter 2

# Context

This chapter introduces CERN, the LHC accelerator, and the ATLAS experiment. A brief description of the ATLAS subsystems is presented, focusing on the Level-1 trigger system.

In addition, The ATLAS Level-1 trigger system upgrade program for the Run 2 of the LHC is described, as well as the motivation for the MUCTPI upgrade.

## 2.1 CERN and the LHC accelerator

CERN [1] is a European research organization that operates the world's largest particle physics laboratory. CERN has 21 member states and directly employs around 2500 people, but approximately 10.000 scientists join the collaboration through the participation of more than 600 universities and institutes from 113 nations worldwide.

Since 1954, CERN scientists have been conducting research studies and experiments to understand the basic constituents of matter. In 1957, CERN built its first accelerator to provide beam for CERN‘s first experiments in particle and nuclear physics. Nowadays, the last addition to CERN‘s accelerator complex [1–3] is the LHC [4–6], the world's largest and most powerful particle accelerator.

The LHC is built inside a circular tunnel 100 meters beneath the ground and consists of a 27-kilometer ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles. Figure 2.1 [7] shows the LHC and the four main detectors of the LHC collider.

During the first run of the LHC (2010-2013), the collision energy reached 8 TeV [8] with a time between bunch crossings (bunch spacing) of 50 ns [9]. Analysis of the data acquired during the first run confirmed the existence of the Higgs boson 40 years after its theoretical prediction [10–12]. This discovery consolidated the Standard Model since it proved the existence of the last unobserved fundamental particle.

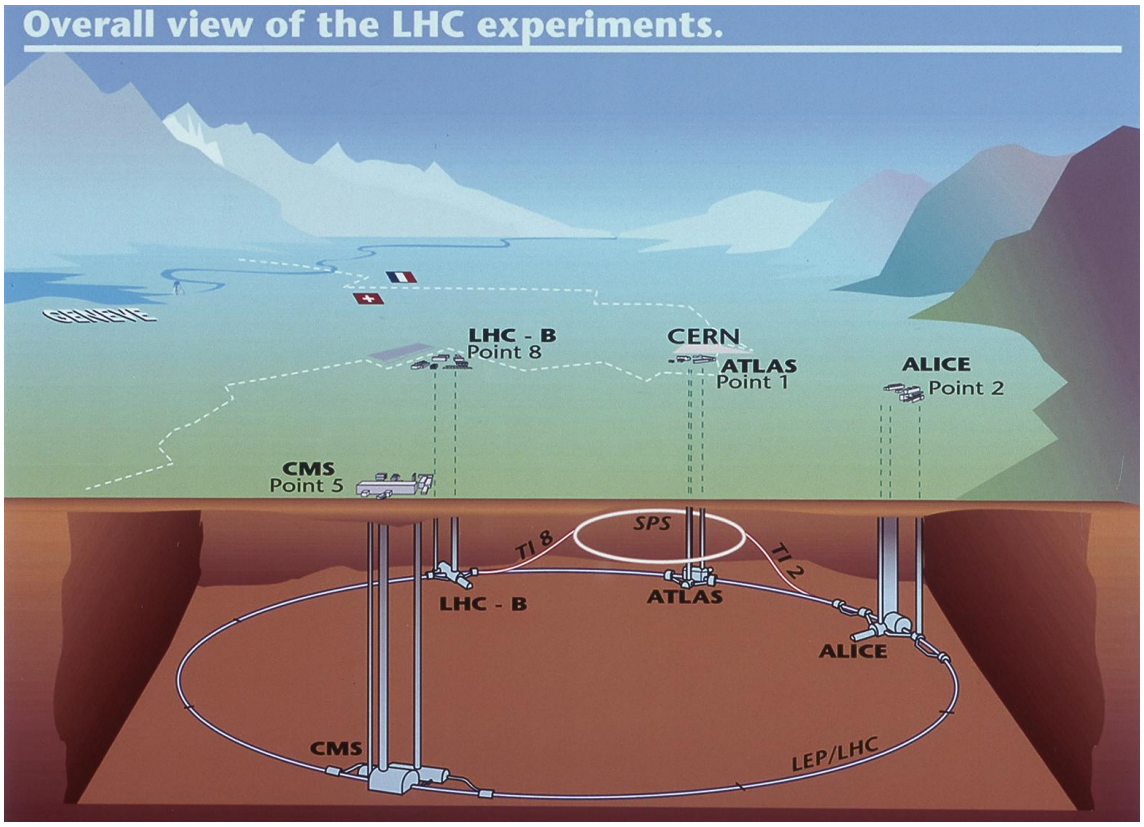



Figure 2.1: The LHC tunnel and its four main experiments

After these unprecedented results, the LHC accelerator and its experiments are currently being consolidated and upgraded for the next run of the LHC. For the second LHC run (Run 2), the collision energy is going to be increased to 13 TeV [8], and the bunch spacing reduced to the nominal value of 25 ns. This scenario brings new challenges for the operation of the LHC and its four detectors.

The LHC operation foresee three Long Shut downs (LS) until 2023 [13]. The first long shut down (LS1) is on-going, preparing the detectors for Run 2, where the peak luminosity[1] reaches $1.7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [9]. A second long shut down (LS2) is planned for 2018-2019 to prepare for peak luminosity of $2.3 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [9] corresponding to 55 to 80 interactions per bunch crossing during Run 3. Finally, a third long shut down (LS3) is foreseen for 2022-2023 after which the luminosity will stay in a constant level of $5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (High Luminosity LHC (HL-LHC)) [14–16].

[1]Luminosity is one of the most important parameters of an accelerator. It measures the number of collisions produced in the interaction point per $\mathrm{cm}^2$ and per second.

## 2.2 The ATLAS experiment

The ATLAS [17, 18] collaboration is composed of 38 countries, with 3000 physicists including more than 1000 students from more than 177 universities and laboratories.

ATLAS is the largest particle physics experiment at the LHC, and is helping the scientific community to understand the basic forces that have shaped our universe.

Figure 2.2 [7] shows an overview of the ATLAS detector highlighting its proportions when compared to a human being. ATLAS is about 45 meters long, more than 25 meters high, and weighs about 7,000 tons.

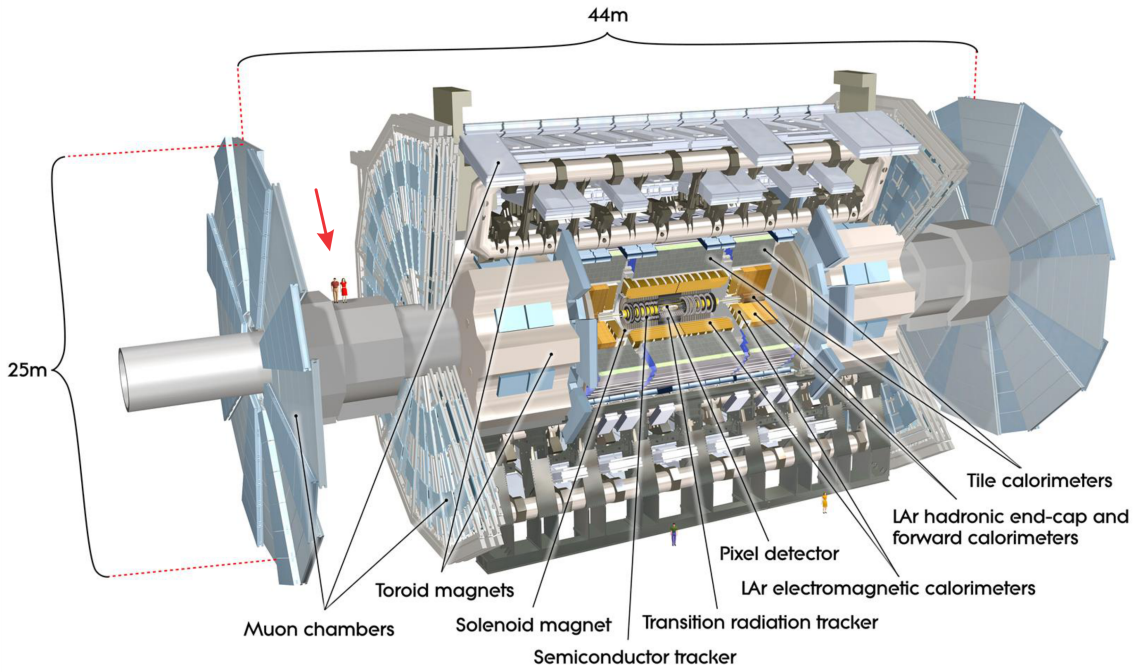



Figure 2.2: Overview of the ATLAS experiment

In order to identify all particles produced by the interaction, the detector is designed in layers. The layers consist of different types of detectors designed to observe specific types of particles. The various tracks that the particles leave in each layer of the detector allow particle identification and measurements of energy and momentum.

The Inner detector [19, 20] (pixel detector, semiconductor tracker, and transition radiation tracker) observes charged particles such as electrons or charged pions. It is enclosed within a solenoid magnet that bends charged particles depending on their momentum and it reconstructs tracks from a series of hits left by the particle.

After the particles have crossed the tracking system, they reach the calorimeters, where their energy is deposited and measured by the electromagnetic and hadronic

calorimeter systems. The Electromagnetic (EM) Calorimeter [21–24] measures the energy of electrons and photons as they interact with the electrically charged particles in matter [18].

The Hadronic Calorimeter [25–28] measures the energy of hadrons, such as protons, neutrons, and pions by reading the deposited energy on an absorbent material.

Calorimeters absorb the energy of most particles except muons and neutrinos. In order to track muons that pass through the detector, the Muon Spectrometer [29–32] is installed in the outermost layer of ATLAS. Muons are detected by measuring a series of hits left in muon chambers. A chambers is consisted of thousands of metal tubes equipped with a central wire within a gas volume. When a muon or any charged particle passes through the volume, it knocks electrons off the atoms of the gas. By measuring the time it takes for these electrons to drift from the starting point, it is possible to determine the position of the muon as it passes through.

The muon detector features separate trigger and high-precision tracking chambers. The precision measurement of the tracking coordinates is provided by the Monitored Drift Tubes (MDT) and the Cathode Strip Chambers (CSC) systems while the trigger information is generated by the Resistive Plate Chamber (RPC) and Thin Gap Chamber (TGC) systems described in Chapter 3.

## 2.3 The trigger and data acquisition system

Figure 2.3 [33] shows an overview of the Trigger and Data Acquisition (TDAQ) system.

The trigger system of ATLAS is structured in a 3-level architecture in order to reduce the event rate from an interaction rate of 1 GHz down to a few 100 Hz written to permanent storage. The first level (Level-1 trigger) is implemented with custom electronics, while the second level (Level-2 trigger) and third level (event builder), collectively known as HLT [34, 35], are built from commercial computers, network switches, and custom software.

The Data Acquisition (DAQ) system receives and buffers the event data from the detector specific readout electronics at the Level-1 trigger accept rate.

The first level trigger reduces the rate to less than 75 kHz with a latency budget of only $2.5\,\mu$s. It combines information from the calorimeter and muon trigger processors and makes the final Level-1-Accept (L1A) decision. The time between the collision and the arrival of the L1A at the sub-detectors is referred to as the Level-1 latency [36]. The first level of trigger also supplies information on the region where the object that passed the trigger threshold was located in the detector, Region-of-Interest (RoI), to the Level-2 trigger.

To ensure that the event data can be read out when the L1A arrives, each

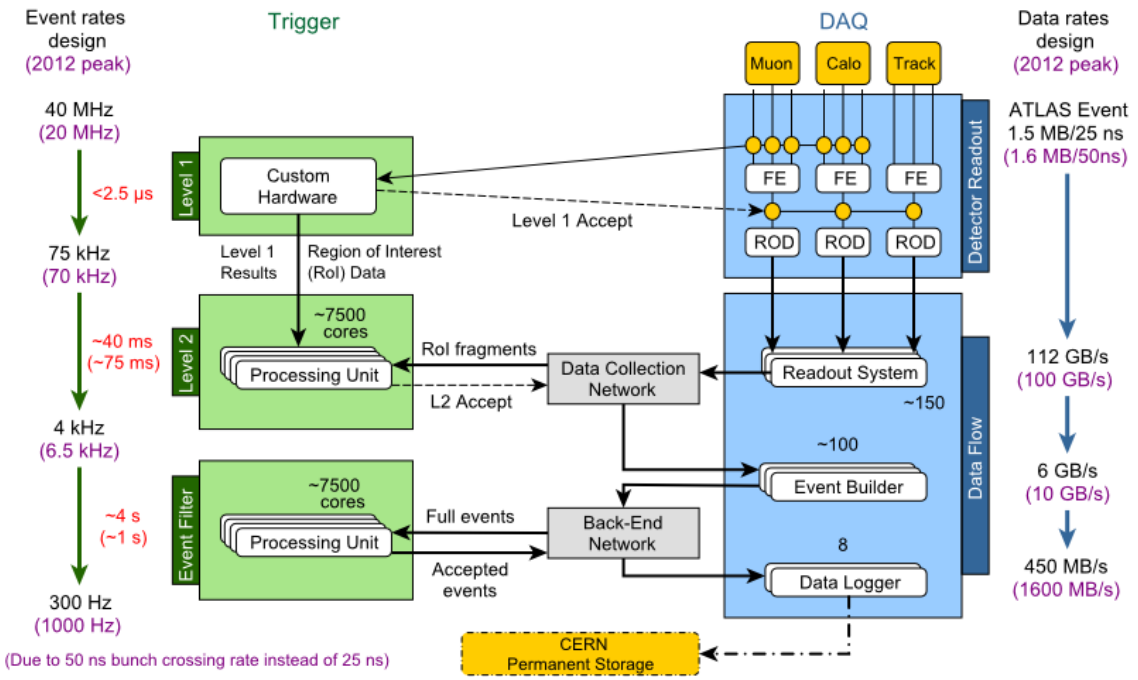



Figure 2.3: Overview of the TDAQ system

sub-detector has to store the event data for a fixed time. This time depends on the Level-1 latency and arrival time of the event data to the readout electronics. The detector specific pipeline memories implemented in the front-end electronics are used to store the data until the L1A arrives. If the Level-1 trigger accepts an event, all the data associated with the event is read out for all components of the detector. The so-called Readout Driver (ROD) receives event information from the pipeline memories, performs data compression and zero suppression, and makes the data available to be read out by the Readout Subsystem (ROS) via optical fibre Readout Links (ROLs) using the S-LINK protocol [37]. Then, the ROS provides RoI fragments to the Level-2 trigger and holds the event data in a custom memory buffer [33, 38] for the entire HLT latency period [33].

The Level-2 trigger reduces the rate of 75 kHz to 4 kHz with an average latency of 40 ms [33]. It applies additional selection criteria, based on the Level-1 RoI information and full-granularity data, by using software algorithms with emphasis on early rejection. Once the Level-2 trigger accepts an event, event fragments from all ROSes are read out by the event builder, which merges these event fragments into full ones. Then the full events enter the event filter farm, where they are processed using offline-type algorithms with access to full calibration and alignment information. The event filter reduces the rate from 4 kHz to 300 Hz[33] with a latency of a few seconds. Events selected by the event filter are moved to the permanent storage at the CERN computer center [39]. The event size is approximately 1.3 MB, resulting in final data storage rate of approximately 450 MB/s [33].

## 2.4 The Level-1 trigger system

The Level-1 trigger system [40] performs fast event selection based on information from the calorimeters and muon detectors. Figure 2.4 [17] shows an overview of the Level-1 trigger system used during the Run 1. The paths to the detector front-ends, Level-2 trigger, and DAQ system are shown in red, blue and black, respectively.

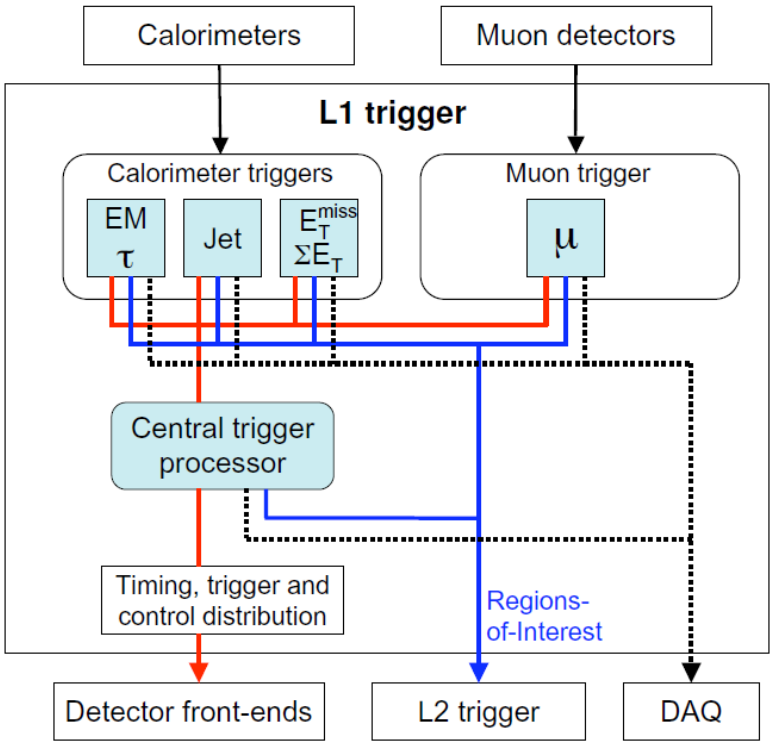



Figure 2.4: Overview of the Level-1 trigger system

The calorimeter selection is based on information from the electromagnetic and hadronic calorimeters grouped into a single sub-system, the Level-1 Calorimeter Trigger (L1Calo). The L1Calo trigger system identifies high-$E_t$ objects, such as electrons and photons, jets, and $\tau$-leptons decaying into hadrons, as well as events with large $E_T^{miss}$[1] and large total transverse energy. The calorimeter information used in the Level-1 trigger decision is the multiplicity of hits for each $E_t$ threshold per object type and energy flags.

The Level-1 Muon Trigger (L1Muon) system searches for patterns of hits consistent with muon with high transverse momentum $p_T$ coming from the interaction point. The transverse momentum $p_T$ represents the component of momentum in

[1] $E_T^{miss}$ measures the energy which is not detected in ATLAS, but it was expected due to the laws of conservation of energy and conservation of momentum. The energy imbalance is caused by particles escaping detection, unaccounted physics processes and detector characteristics such as the noise and dead or hot cells.)

the XY-plane. The muon information used in the Level-1 trigger decision is the multiplicity of muons for each of six programmable $p_T$ thresholds.

The L1A signal is generated by the Central Trigger Processor (CTP) [41] which combines the information from the L1Calo and L1Muon systems and performs the event selection based on physics signatures found in the event, such as energetic jets, leptons or large missing transverse energy [42]. The L1A signal is distributed to the detector front-ends, synchronously with the bunch clock at a fixed time after the collision through the Timing, Trigger and Control (TTC) system [40].

While the Level-1 trigger decision is based only on the multiplicity of trigger objects, the position information of the trigger objects is available in the muon and calorimeter trigger processors. For each event being accepted by the Level-1 trigger, the RoI information is sent to the Level-2 trigger and is used to seed the HLT selection.

The Level-1 latency has to be kept as short as possible due to the limited storage availability in the front-end pipelined memories. The design of the on-detector front-end electronics requires the Level-1 latency to be less than 2.5 $\mu$s. Due to the experiment dimensions and the distance to the underground counting room, the cable propagation delays take about 1 $\mu$s of this time. Leaving 0.5 $\mu$s for contingency, a latency budget of only 1 $\mu$s remains to be shared between the subsystems of the Level-1 trigger for processing and data transfer.

## 2.5 The Level-1 trigger system upgrade

The ATLAS Level-1 trigger system operated successfully during the entire data taking in Run 1. However, for Run 2, the ATLAS experiment has to efficiently trigger and record data at instantaneous luminosities that are up to two times higher than those of the original LHC design. This requires the Level-1 trigger to improve the selection efficiency by using additional information from the detector.

The ATLAS coverage can be improved increasing the trigger efficiency for several physics processes, such as the B-hadrons decaying to two low-$p_T$ muons and lepton flavor violation $\tau$ decays. The improvement in the trigger efficiency is achieved by complementing inclusive selections with more exclusive ones, such as the selections based on angles and effective masses using the geometry of all particle tracks from one event (topological information). Therefore, the so-called Level-1 Topological Trigger Processor (L1Topo) [43, 44] is being added to the trigger system.

Figure 2.5 shows an overview of the Level-1 trigger system that will operate during Run 2 with emphasis on the muon trigger system. The new trigger system components are shown in green, such as the L1Topo processor and the MuCTPiTo-Topo interface while the upgraded systems, such as the L1Calo, MUCTPI and CTP

are shown in blue.

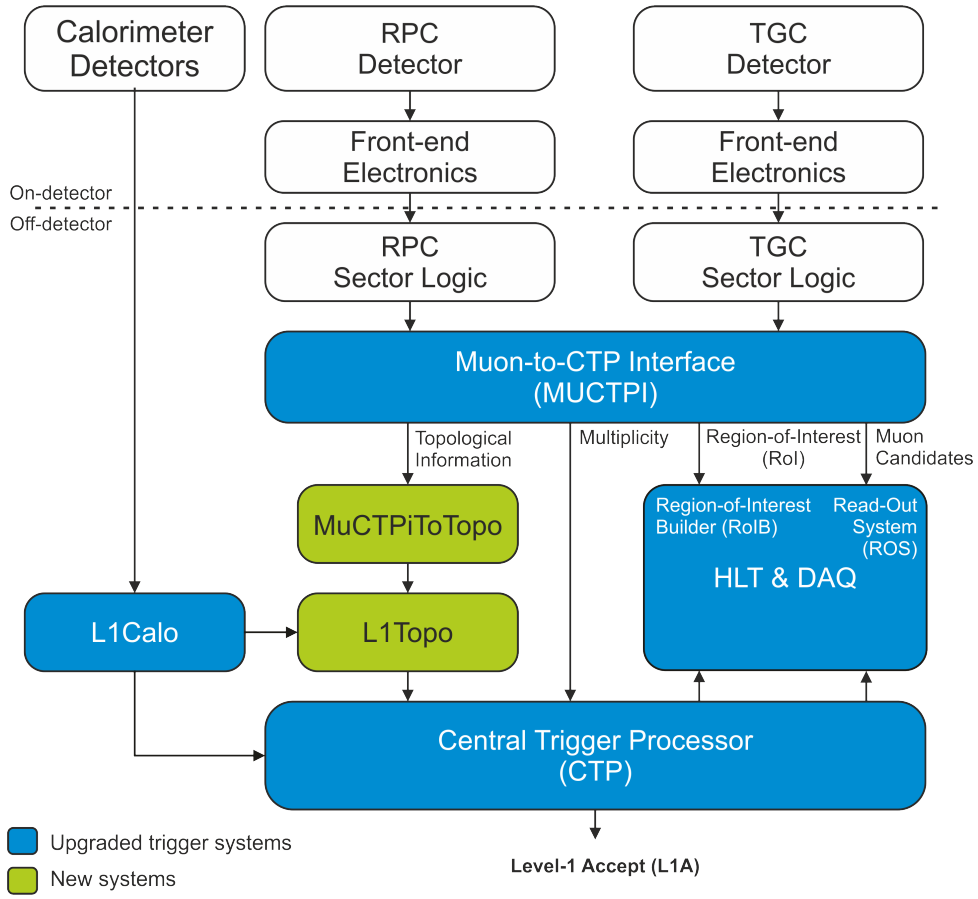



Figure 2.5: Overview of the Level-1 trigger for the Run 2 with emphasis on the muon trigger system

The trigger information from the calorimeters and muon trigger detectors is processed by dedicated trigger processors (L1Calo and MUCTPI system), which provides multiplicity of trigger objects to the CTP and topological information to L1Topo. This information is then combined in the CTP, that takes the final level-1 decision.

The L1Calo system has been upgraded in view of the increased pile-up[1] and to be able to provide topological information to L1Topo.

The primary goal of this work is the firmware upgrade of the MUCTPI system so as to provide coarse-grained muon topological information to L1Topo already in Run 2 [45]. The firmware upgrade allowed the MUCTPI to collect, encode and transmit topological information of muon candidates to L1Topo through the existing electrical trigger outputs. Full granularity muon topological information will only be available when the MUCTPI system is entirely replaced.

The MUCTPI-to-Level-1-Topological-Processor interface (MuCTPiToTopo) has

[1]Pile-up interactions increase with luminosity and are associated with collisions in addition to the collision of interest.

been implemented by National Institute for Subatomic Physics (Nikhef) to connect the muon topological information from the MUCTPI electrical outputs to the L1Topo processor optical inputs. This interface is described in more detail on Chapter 6.

The CTP has also been upgraded to increase the number of trigger inputs by doubling the internal backplane data transfer rate and adding direct inputs to the processing unit, which are used to receive trigger signals from L1Topo.

## 2.6 Summary

In an effort to increase the trigger efficiency for several physics processes, a topological trigger processor (L1Topo) has been introduced to the ATLAS Level-1 trigger system. The trigger processors had to be upgraded in order to provide position information of trigger objects to L1Topo, which will select events based on its topology.

The next chapter will present the Level-1 muon trigger system including the MUCTPI which its firmware upgrade to transmit topological information to L1Topo is the primary goal of this work.

# Chapter 3

# Level-1 muon trigger system

This chapter gives an overview of the muon trigger detectors and the MUCTPI system, describing the principle of operation and their application on the Level-1 trigger system.

## 3.1 Muon trigger detectors

The muon trigger detectors provides track information within 15-25 ns [17] after the passage of a particle, allowing to identify the beam crossing. The trigger information is provided by RPC detectors in the barrel region ($|\eta| < 1.05$) [46], and TGC detectors in the end-cap region ($1.05 < |\eta| < 2.4$) [47]. These chambers can measure both coordinates of the track, one in the bending RZ-plane, and one in the non-bending $\phi$Z-plane [17, 32]. The ATLAS coordinate system is described in Appendix A.

The RPC and TGC trigger detectors provide the multiplicity and approximate energy range of the muon tracks traversing the detector. They also complement the high-precision tracking measurement by providing a second coordinate measurement in the non-bending plane, as the purpose of the MDT detectors is to determine the coordinate of the track in the bending plane. After matching of the MDT and trigger chamber hits in the bending plane, the coordinate on the non-bending plane from the trigger chamber is adopted in the MDT measurement.

The momentum of the muons is estimated using a coincidence scheme that measures the bending[1] of muon tracks in the magnetic field of the large superconducting air-core toroid magnets [48, 49].

Figure 3.1 [32] shows a schematic view of the muon detectors. The lines in magenta indicate the muon trigger chambers (RPC and TGC trigger detectors). The low-$p_T$ and high-$p_T$ trigger coincidences are indicated in red and blue respectively. As

[1]The smaller the momentum, the stronger the bending, and the higher the momentum, the stiffer the track becomes.

the bending is greater for low-$p_T$ trigger objects, the estimation of the approximate energy range of low-$p_T$ trigger objects is performed using chambers located close to each other, such as the pairs RPC1 & RPC2 and TGC3 & TGC2. In the other hand, tracks detected at chambers distant to each other, such as the pairs RPC1 & RPC3 and TGC3 & TGC1 (inside the regions indicated in blue), are classified as high-$p_T$ trigger objects. The larger distance between RPC1 & RPC3 and TGC3 & TGC1 enables the estimation of the approximated energy range of high-$p_T$ trigger objects without the need of high-precision tracking information.

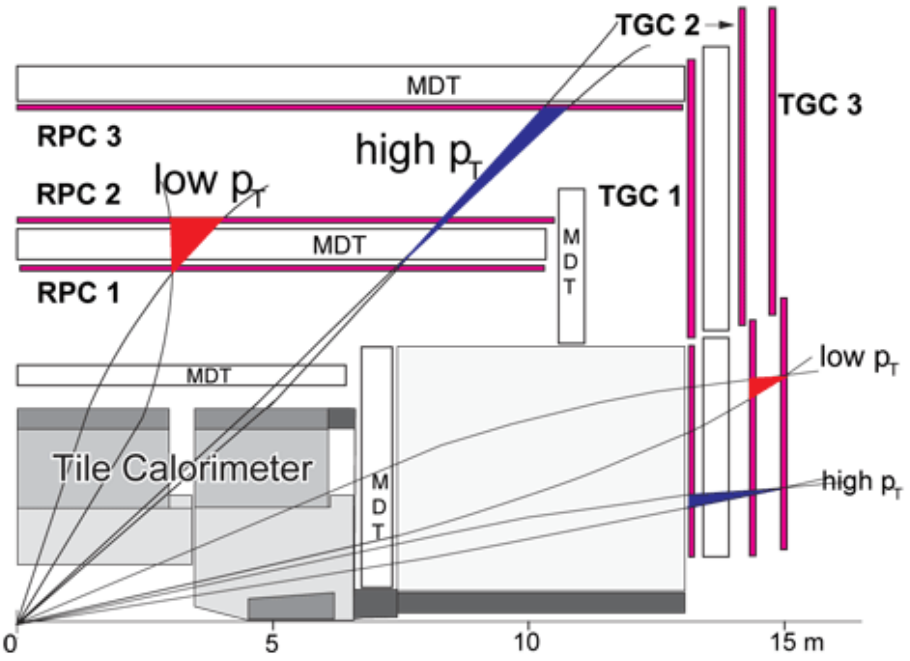



Figure 3.1: Schematic view of the muon detector

Figure 3.2 shows the segmentation of the muon trigger subsystems.

The RPC system divided in two halves (forming two barrels), each half is then segmented in 32 trigger sectors in $\phi$ and each trigger sector is divided into 24 sub-sectors[32, 50].

The TGC system is also segmented in two in $\eta$, each half is segmented into two regions: the forward (inner) and the end-cap (outer) regions. The forward region is segmented into 24 sectors in $\phi$, and the end-cap region is segmented into 48 sectors (also in the $\phi$ direction). The on-detector electronics granularity determines the maximum number of sub-sectors. For the end-cap sectors it is limited to 148 sub-sectors, and for the forward sectors is 64 [32, 50].

The muon trigger sector logic [51–53] reconstructs muon tracks (three dimensionally) and classifies them into one of six $p_T$ threshold values. It selects the two highest-$p_T$ muon candidates for each of the 208 muon trigger sectors from RPC and TGC systems and sends the so-called sector data to the MUCTPI system. The sector

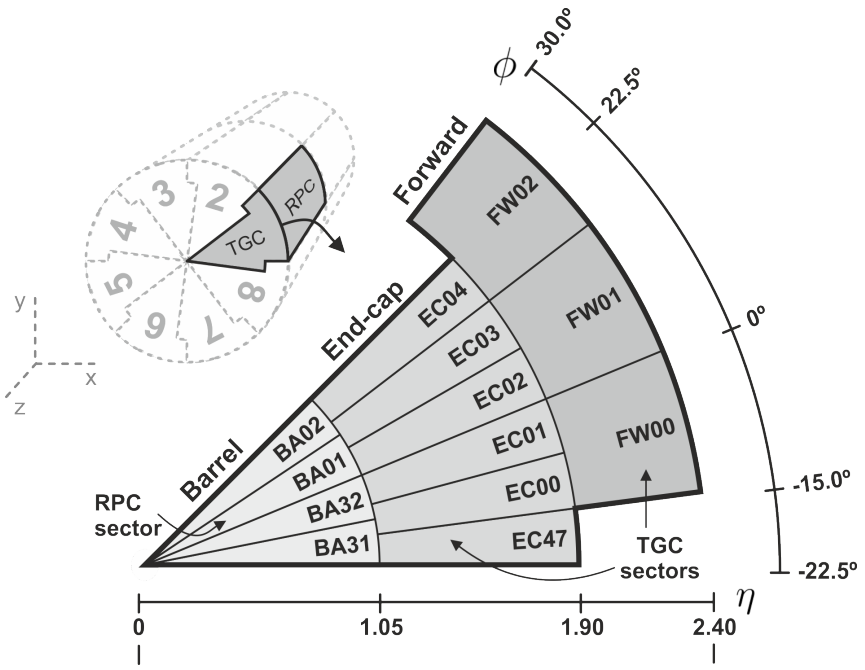



Figure 3.2: Muon trigger subsystems segmentation

data contains information, such as the position RoI and the transverse momentum $p_T$ threshold value from each candidate. The RoI value represents the sub-sector number where the hit was detected.

## 3.2 MUCTPI

At the MUCTPI, each half of the muon trigger detector is segmented into eight octants. Each octant contains thirteen sectors: four sectors from the barrel region, six sectors from the end-cap region, and three sectors from the forward region [50].

The MUCTPI combines the information delivered by the trigger sector logic modules from the three regions of the muon trigger sub-detectors (barrel, end-cap and forward) and then calculates the total number of muon candidates, the so-called multiplicity, for each of six $p_T$ thresholds.

The overlap handling algorithm [54] avoids double counting of muon candidate tracks that transverse more than one detector region by using programmable Look up Tables (LUTs) to indicate if a given candidate is located in one of the overlap regions between adjacent trigger sectors. The total multiplicity is forwarded to the CTP which takes the final Level-1 decision.

Figure 3.3 shows the block diagram of the MUCTPI system, which shows the routing of the trigger signals (multiplicity) from the 16 Muon Interface Octant Modules (MIOCTs) to the Muon Central Trigger Processor Interface Module (MICTP) through the Muon Interface Backplane (MIBAK). It also shows the distribution of

the timing signals from the MICTP module and the shared bus over which the Muon Interface Readout Driver Module (MIROD) module receives the readout data.

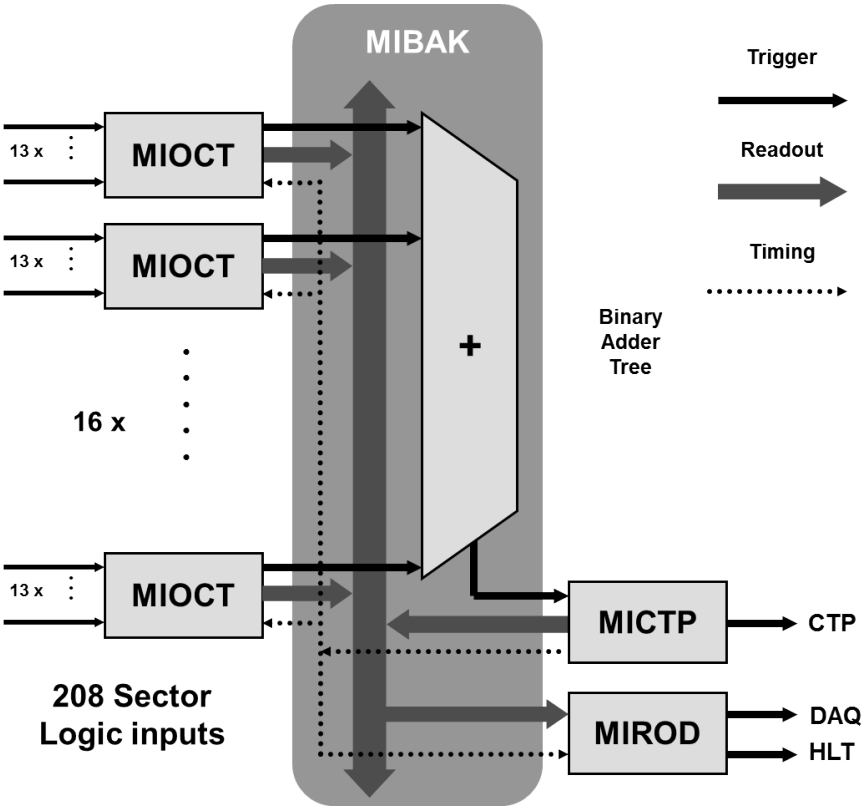



Figure 3.3: MUCTPI system block diagram

The MIOCT module combines the data from the 13 trigger sectors of one octant and calculates the octant multiplicity values. The custom active MIBAK backplane distributes the timing and control signals, implements a shared bus for the readout, and calculates the overall multiplicity, which is latched by the MICTP. The MICTP module receives trigger and timing signals and forwards the overall multiplicity values to the CTP. When an L1A is received from the CTP, the MIROD module collects the readout data from the 16 octants and the overall multiplicity value from the MICTP and sends them to the HLT and DAQ systems.

The MICTP and MIROD modules are implemented using the same card design with only few differences in the assembly of components. For example, the MIROD module hosts S-LINK mezzanine cards to implement the optical link communication to the DAQ and HLT systems, whereas the MICTP does not need them.

Figure 3.4 shows the MUCTPI crate, which hosts 16 MIOCT modules, one MICTP module, one MIROD module and one custom MIBAK backplane in a 9U Versa Module Europa (VME) crate. The MUCTPI crate also hosts one Local Trigger Processor (LTP) [55] module that receives trigger and timing signals from the CTP system and forwards a busy flag from the MICTP module to the CTP system whenever the readout logic is unable to accept further events. The

LTP also allows stand-alone operation of the MUCTPI system for test purposes by supplying locally generated trigger and timing signals. In addition, a Single-Board Computer (SBC) [56] is installed in the system for controlling and configuring the modules through the VME bus [57] backplane.

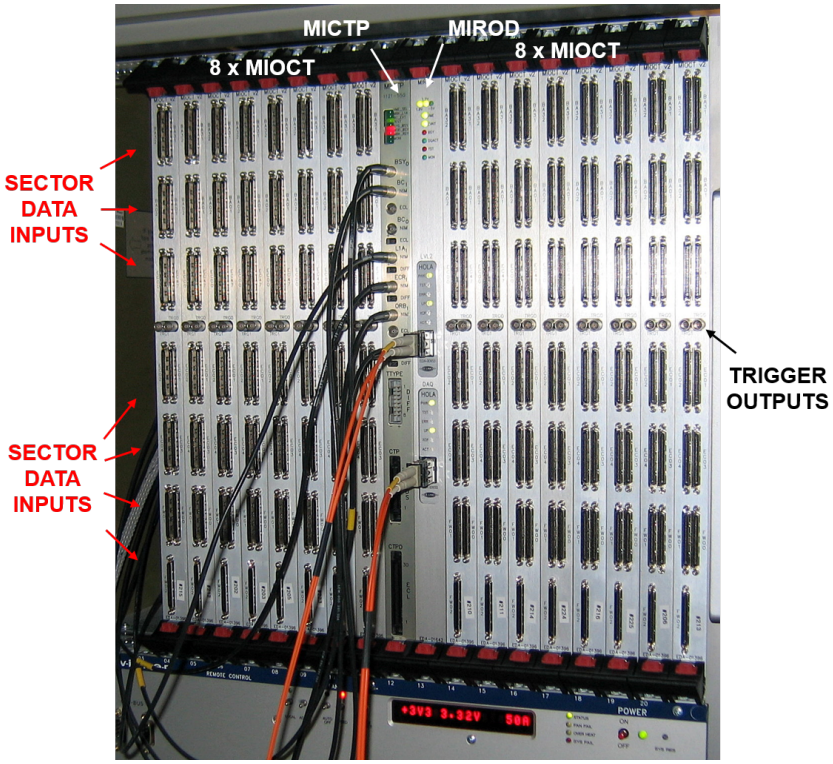



Figure 3.4: MUCTPI crate

### 3.2.1 MIOCT

The MIOCT card calculates the candidate multiplicities taking into account the possible overlap of muon tracks in the detector. There are two FPGAs on the module. Most of the functionality is implemented in the MIOCT FPGA which performs the trigger and readout functionality. The MIOCT FPGA is an Altera Stratix II EP2S90 FPGA device [58]. A second smaller FPGA (Altera Cyclone II EP2C5 [59]) is used to implement the VME bus interface and to control peripherals on the card.

The block diagram of the MIOCT FPGA logic is shown in Figure 3.5. Programmable length pipelines are used to synchronize the sector data from 13 trigger sectors. Then, double counting of muons is avoided by the overlap handling unit. The octant multiplicity is calculated and sent to the MIBAK backplane for summing with the values from the other octants. The readout logic stores the sector data in pipeline memories until the L1A arrives. Then, the data from accepted events are read out through the MIBAK backplane. The QDR-II Static Random-Access Mem-

ory (SRAM) memory can be used for validation of the functionality and to capture sector input data. The MIOCT module also features two electrical trigger outputs, originally foreseen for testing purposes, but later used during Run 1 to indicate the existence of at least one muon candidate in selected regions of the detector.

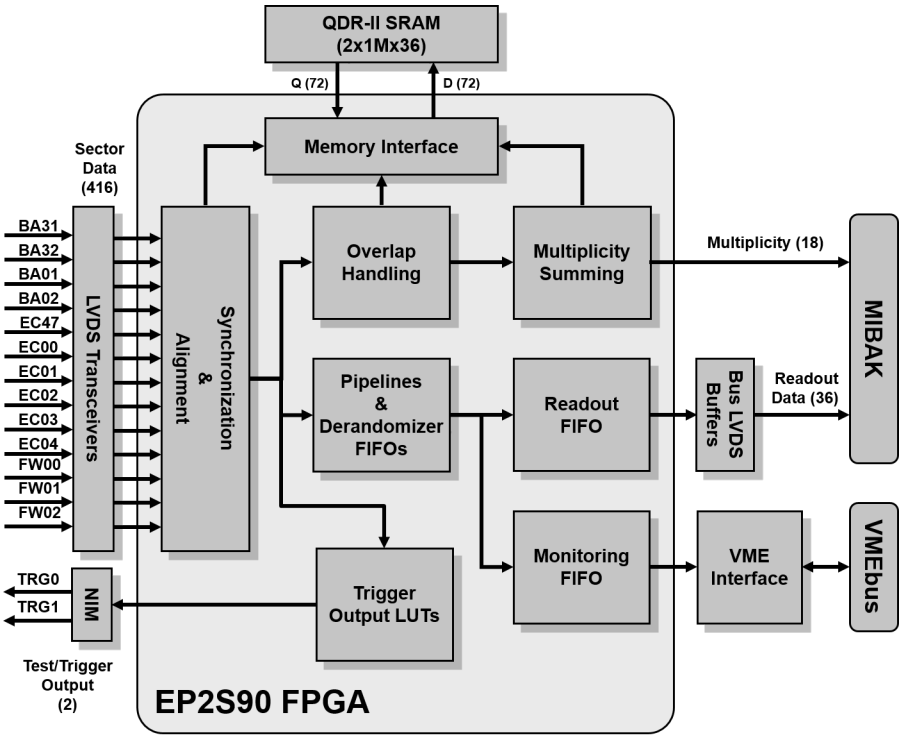



Figure 3.5: MIOCT block diagram

#### 3.2.1.1 MIOCT sector data

The sector data contains information from the two highest-$p_T$ muon candidates, including the sub-sector number where the hit was detected (RoI), the transverse momentum $p_T$ threshold value, the charge sign, overlap flags, and a flag which indicates the existence of more than one candidate in a given RoI. In addition, it carries information about the lower three bits of the bunch crossing identification (BCID) number and a flag, which indicates the existence of more than two candidates in a sector. The lower bits of the BCID are used for checking if the data from all 13 trigger sector inputs are aligned with respect to the same bunch crossing. Table 3.1 gives an overview of the MIOCT sector data format for the different trigger regions.

#### 3.2.1.2 Synchronization & alignment

Each of the 13 sector inputs has one programmable synchronization and alignment unit. This unit synchronizes the data with one of the 8 phases derived from the bunch clock. It then delays the data using programmable-length pipelines in

Table 3.1: Sector data format for barrel, end-cap and forward

| **Meaning** | | **Barrel** | **End-Cap** | **Forward** |
|---|---|---|---|---|
| Information for each of the two candidates | Region Of Interest (RoI) | 5 bits | 8 bits | 6 bits |
| | $> 1$ candidate in the RoI | 1 bit | N.A. | N.A. |
| | Sector overlap flags | 2 bits | 1 bit | N.A. |
| | $p_T$ threshold | | 3 bits | |
| | Charge sign | N.A. | 1 bit | 1 bit |
| $> 2$ candidates in a sector | | | 1 bit | |
| Bunch crossing identification (BCID) | | | 3 bits | |

order to compensate for the effect of different lengths cables and different delays from the barrel and end-cap subsystems.

#### 3.2.1.3 Overlap handling

Once the data are synchronized and aligned, double counting of muons is avoided by checking the coincidence of muon candidates in overlap regions. Figure 3.6 shows the location of the 13 trigger sectors in one octant of the detector. The zones highlighted in gray indicate the overlap regions handled in the MIOCT module. The overlap handling unit supports every combination of overlaps between trigger sectors from the same or adjacent regions, i.e. barrel-barrel, end-cap-end-cap, forward-forward, barrel-end-cap and end-cap-forward. The front-end electronics handles overlap within a sector. Note that there is no overlap between the trigger sectors BA32 and BA01 because they use the same large chamber [50]. The MUCTPI system does not support overlap handling between adjacent octants, this was not required when the system was designed.

The overlap handling unit processes 22 overlap regions of the detector in parallel for each candidate pair. It uses LUTs to determine if a given pair of RoIs is in overlap. The RoI values of each of the candidates feed the address input of the LUTs that identifies if the candidates are in overlap. If so, the pT value of the candidates is compared and the lowest $p_T$ candidate is suppressed

The required number of LUTs to check the overlap regions for all candidates is shown in Equation (3.1),

$$N = R \times C^2, \tag{3.1}$$

where N represents the number of LUTs, R represents the number of overlap regions being considered, and C represents the number of candidates in a trigger sector. Currently, 22 overlaps region are considered and two candidates are sent by the muon detectors, resulting in 88 LUTs. The LUTs are implemented using on-chip memory blocks available in the FPGA device. The overlap definitions are loaded to the LUTs through the VME bus when the system is configured.

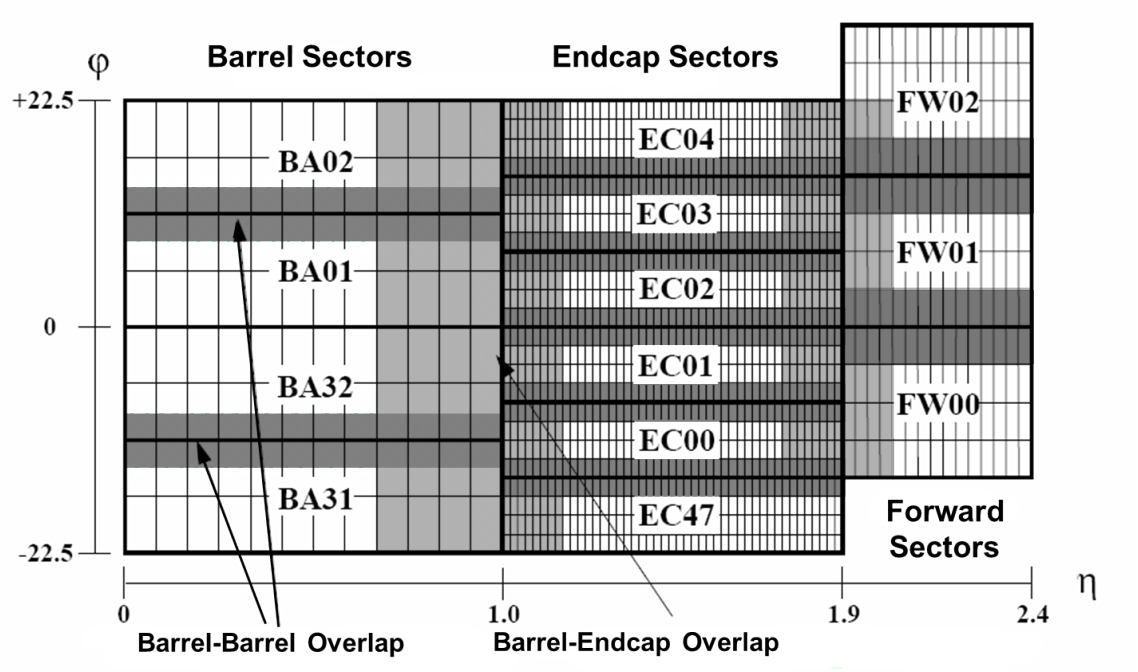



Figure 3.6: Overlap regions handled by the MIOCT module

#### 3.2.1.4 Multiplicity summing

The multiplicity summing unit counts the number of candidates for each of the 6 $p_T$ threshold values taking into account the overlap. It groups the results into an 18-bit word with a 3-bit count for each $p_T$ threshold value. The multiplicity results for each octant are then sent to the MIBAK backplane where the overall multiplicity is calculated.

#### 3.2.1.5 Trigger outputs

Two electrical trigger outputs are used to indicate the presence of at least one candidate that satisfies conditions of the sector number and $p_T$ threshold values at the bunch crossing rate. These conditions are loaded into LUTs that drive the two trigger outputs. All of the trigger outputs from the 16 MIOCT cards are connected to a NIM module that implements a logic OR of each group of 16 inputs. This module generates two inputs to the CTP that indicates the existence of at least one candidate in the barrel and end-cap regions respectively.

#### 3.2.1.6 Readout

The trigger sector data, the octant multiplicity values and the candidate veto flags are connected to programmable-length pipelines that store the data until the

L1A arrives. The so-called derandomizer[1] First In First Outs (FIFOs) latch the incoming data from the pipeline registers whenever an L1A is received and forward the data to the readout and monitoring FIFOs.

The readout controller keeps track of the status of all the FIFOs and issues the FIFO read and write requests. It adds a header and control flags to the readout data before writing them to the readout and monitoring FIFOs that are read through the MIBAK and VME bus interfaces respectively.

The MIBAK interface delivers the readout data to the MIBAK backplane whenever a read request is received from the bus.

#### 3.2.1.7 Debug & monitoring

Each of the MIOCT cards features two Quad-Data Rate (QDR)-II SRAM memories with a capacity of 1 M × 36-bit words each [60]. The memory can work in two modes:

a) Snapshot mode: the trigger sector data, the overlap flags, the candidate suppression flags, the octant multiplicity values and time monitoring data from up to 128 k bunch crossings are written to the memory.

b) Replay mode: the sector data are read from the memory and the generated results (overlap flags, multiplicity, and others) are written back to the memory.

The Snapshot mode is useful for the timing-in of the system, as well as for diagnostics and monitoring purposes. The replay mode can be used to validate the results generated by the hardware every time a new firmware version is implemented.

The MIOCT card also provides information for on-line monitoring. More than 300 counters are implemented to measure the rate of events under certain conditions. Examples are: the number of occurrences of each $p_T$ threshold for each candidate from every trigger sector; the number of veto flags of each of the 26 candidates and the number of single and multiple overlap occurrences.

### 3.2.2 MIROD

The MIROD module sequentially reads out event data from each of the MIOCT modules and the overall multiplicity data from the MICTP over the MIBAK backplane. It receives data from the MIBAK via Bus Low-Voltage Differential Signaling (LVDS) buffers. It then combines, buffers, formats, and processes the data in the on-board FPGA and sends them to the HLT and DAQ through S-LINK optical link mezzanine cards.

[1]The term derandomizer is employed in this context because the L1A requests are received randomly.

Figure 3.7 shows the block diagram of the Muon Interface ROD & CTP (MIRODCTP) module with two mezzanine cards that are installed when the board is used to implement the MIROD functionality.

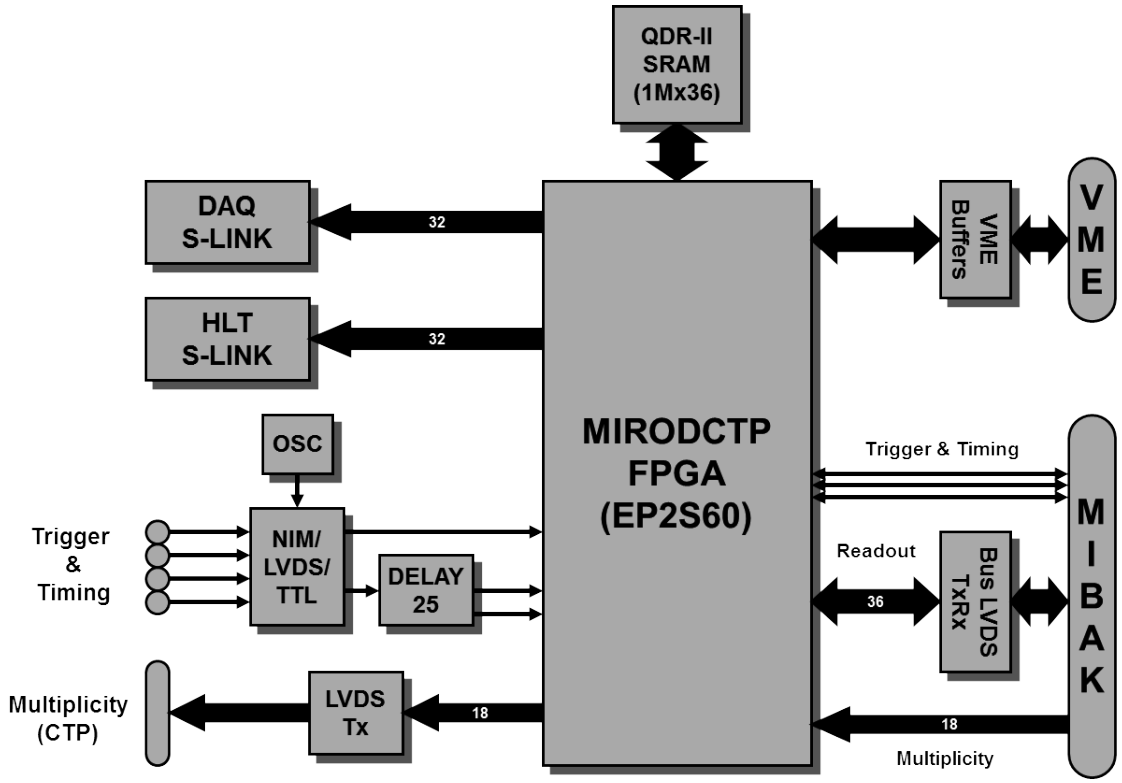



Figure 3.7: MIRODCTP module block diagram

### 3.2.3 MICTP

The MICTP receives timing and trigger signals from the front-panel using the appropriate level translators, and distributes them to the remaining cards in the system via the backplane.

The on-board FPGA receives the overall multiplicity values calculated by the adder tree on the MIBAK, latches and sends them to the CTP using LVDS buffers over a twisted-pair cable. The overall multiplicity values are then stored in a pipeline memory until the L1A arrives in order to be read out by the MIROD via the MIBAK bus. Figure 3.7 also shows the front-panel connections of the timing & trigger signals through the level converter buffers and the distribution of the signals via the MIBAK backplane.

### 3.2.4 MIBAK

The custom active backplane calculates the overall multiplicity values by summing the octant multiplicity values from each of the 16 MIOCT cards. The summing

is performed by using an adder tree implemented in Altera MAX7000 Complex Programmable Logic Device (CPLD) chips [61], in order to achieve the lowest latency.

The MIBAK also implements a bus to transfer the readout data from the MIOCT and MICTP modules to the MIROD module using a token passing protocol. The MIROD issues a token to the MICTP and, after that, to all the MIOCT modules in turn. While a module has a token it puts its readout data onto the bus. Once finished it forwards the token to the next module in the readout chain. The electrical connections on the bus are based on Bus LVDS signals.

Finally, the MIBAK also distributes trigger and timing signals with low skew to all modules in the crate.

## 3.3 Summary

This chapter provided an overview of the Level-1 muon trigger system with emphasis on the MUCTPI system and its modules.

The next chapter will discuss the technical feasibility studies performed with the MUCTPI system. The results from these studies were essential to determine the maximum bit rate at which the MIOCT trigger outputs can transmit data reliably.

# Chapter 4

# MUCTPI feasibility tests

This chapter describes the tests performed to investigate the feasibility of sending topological information at the bunch crossing rate through the MUCTPI electrical trigger outputs.

During Run 1 the MIOCT electrical outputs were operated at a rate of 40 MHz, as intended in the original design specifications. However, this rate is not sufficient even to send coarse muon topological information on individual candidates to L1Topo. In order to provide coarse-grained muon topological information in Run 2, the data rate transmitted through the MUCTPI electrical trigger outputs had to be increased significantly.

Since the electrical trigger outputs had never been tested at more than 40 MHz, a technical feasibility study was conducted to determine the maximum rate at which the data could be reliably transmitted. The MIOCT firmware was modified to generate a Pseudo Random Bit Sequence (PRBS) at a multiple of 40 MHz for all trigger outputs. Initially, an oscilloscope was used to check the quality of the transmitted signal and then a dedicated error rate test system was developed to verify and perform a phase scan of the PRBS data received from the MUCTPI.

## 4.1 Firmware modification of the MIOCT module

Depending on both the signal and the transmission channel (transmitter, receiver and cable connections) characteristics, previous data bits can affect the current value of the signal by changing the timing of the transition, consequently causing data dependent jitter [62]. To demonstrate that reliable data transmission could be achieved when the MIOCT electrical trigger outputs are over-clocked[1], the MIOCT firmware was modified to transmit PRBS data through the trigger outputs over-clocked by factors of 2, 4, 6, and 8. A PRBS pattern is used because the test

[1]The process of forcing a component to operate faster than the original clock frequency is often referred to as over-clocking

pattern must have similar properties to the trigger signal to be transmitted through the trigger outputs. An example of these characteristics is the short and long time intervals between edges, which are present in pseudo-random sequences. Therefore, a study of the degradation of the transmitted signal quality due to data dependent jitter is more realistic using pseudo-random sequence than using fixed patterns.

A 31-bit Fibonacci Linear Feedback Shift Register (LFSR) ($k = 31$) [63, 64] was chosen for the implementation of the pseudo-random sequence generator (PRBS-31). The selected random generator uses the feedback polynomial $x^{31} + x^{28} + 1$ to generate a sequence with $N = 2^k - 1 = 2^{31} - 1 = 2.147.483.647$ different states. Figure 4.1 shows the block diagram of the LFSR.

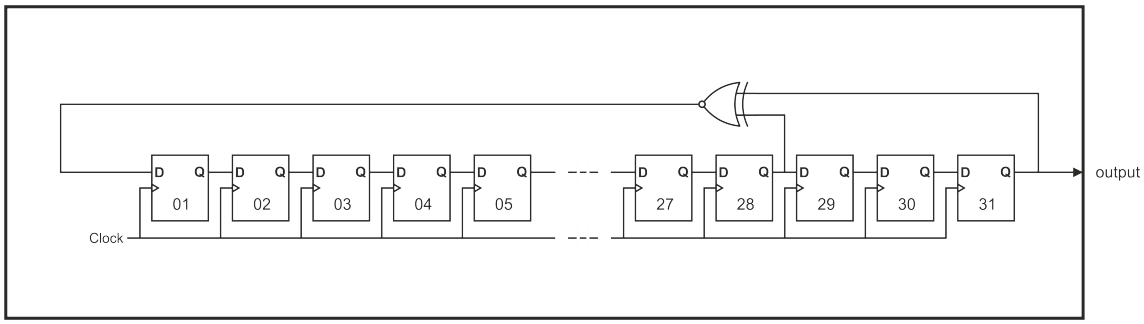



Figure 4.1: A PRBS generator of $2^{31} - 1$ bits generated as the output of a 31-bit Fibonacci linear shift register

Tests were performed configuring the MIOCT outputs to send PRBS data at 80 Mbps, 160 Mbps, 240 Mbps and 320 Mbps. The MIOCT trigger outputs and the LHC clock provided by the MICTP module were connected to the oscilloscope[1] [65] configured in infinite persistence display mode, which superimposes multiple oscilloscope acquisitions. After the accumulation of thousands of waveforms, the overlay of the samples triggered by the transmitter clock generates an so-called eye diagram, named so because the resulting image looks like the opening of an eye. If the eye diagram looks closed, it means that the edge timing is slow, and data dependent or other jitter is significant. Figure 4.2 shows an eye diagram of the data transmitted by two MIOCT outputs operating at 320 Mbps. This eye-diagram was generated from data accumulated over 30 days. The top and bottom plots represent the eye-diagram of the outputs TRG0 and TRG1 respectively. The abscissa axis represents the time in 500 ps/div and the ordinate axis indicates the signal voltage in 150 mV/div. The oscilloscope measurements show an open eye-diagram for the two electrical trigger outputs operating at 320 Mbps.

However, the test with the oscilloscope checks only the transmitter because the oscilloscope does not have the same limitations such as the setup and hold times or drift of the clock phase that the actual receiver has. Besides, the oscilloscope

[1] WaveRunner 6 Zi from LeCroy

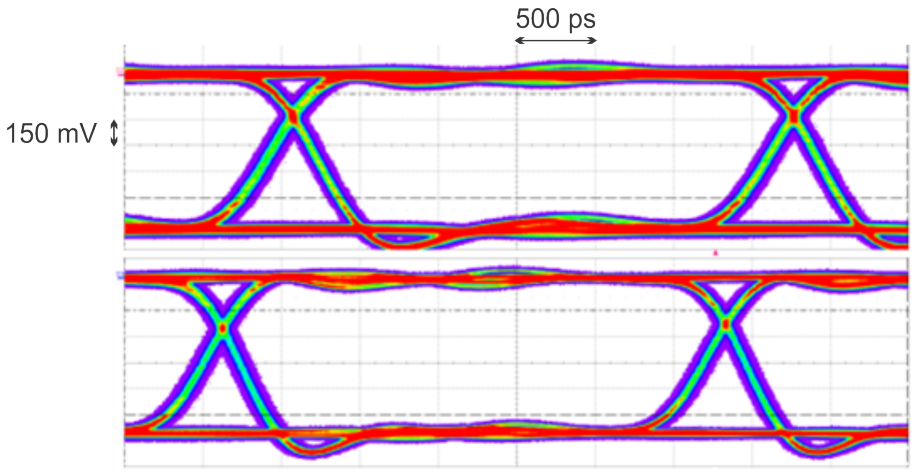



Figure 4.2: Eye-diagram of two MIOCT outputs operating at 320 Mbps

acquires samples of the signal over the time, which makes it impossible to detect errors that occur infrequently. Therefore, an dedicated error rate test system has been developed to overcome these issues and generate a phase scan of the received data.

## 4.2 Development of an error rate test system

The error rate test system estimates the BER of the received PRBS data by counting the number of errors detected in the sequence and performs jitter analysis checking the existence of transitions at various sampling points.

### 4.2.1 Hardware platform

The test system is implemented using an FPGA evaluation board[1] [66]. The chosen FPGA device[2] [67, 68] provides flexible input/output resources, such as the programmable internal delay lines and data serializers and deserializers. The evaluation board also offers connectivity for two FPGA Mezzanine Cards (FMCs), a Gigabit Ethernet interface, and a high-speed memory module[3] that are needed for the implementation of the test system. The usage of mezzanine cards enables customizing the connectivity for the specific application requirements. Figure 4.3 [66] shows a photo of the evaluation board and its peripherals, including the Kintex-7 FPGA device, the DDR3 SODIMM[4] module, the Ethernet physical interface and the FMC connectors.

[1] Xilinx KC705
[2] 7-series Kintex device
[3] $3^{rd}$ generation of Double Data Rate DRAM (DDR3)
[4] Small Outline Dual In-line Memory Module (SODIMM)

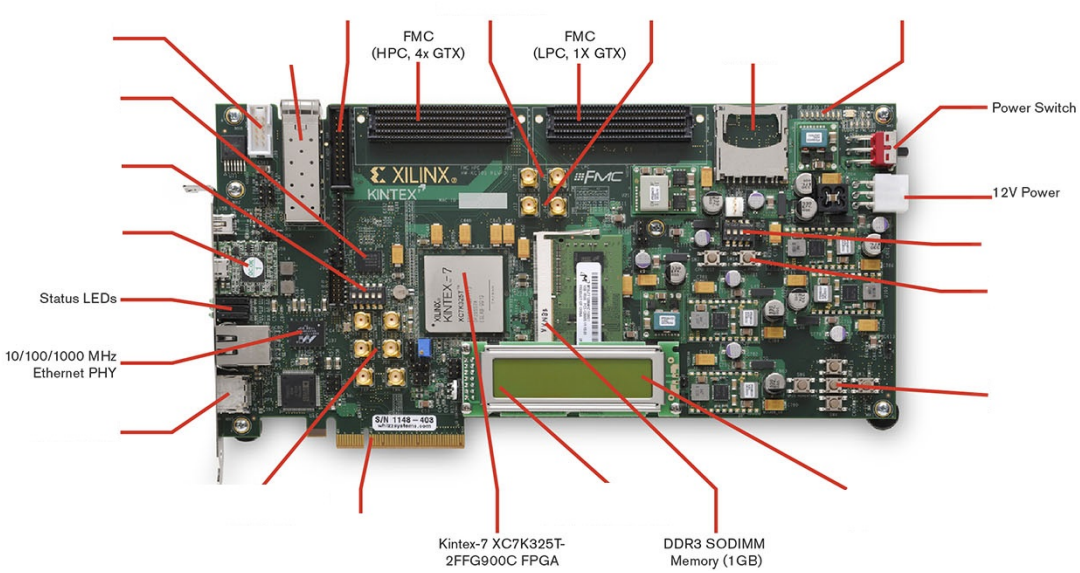



Figure 4.3: Xilinx Kintex-7 FPGA KC705 Evaluation Kit resources

The error rate test system uses a custom FMC designed and built by Nikhef for receiving clock and MUCTPI trigger outputs data. The so-called MUCTPI receiver mezzanine card consists of an input stage with 40 LEMO[1] connectors (32 inputs + 8 outputs), and the respective NIM[2] to LVDS or LVDS to NIM level converters. It also includes a clock multiplier and jitter-cleaner circuit in the clock network (Si5317 [69] and Si5324 [70]). Figure 4.4 shows a photo of the mezzanine card [71].

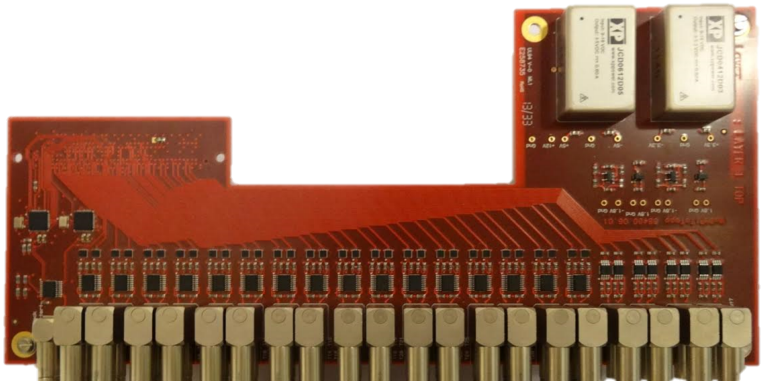


Figure 4.4: MUCTPI receiver mezzanine card

Since the input to output phase skew of the jitter-cleaner device is not controlled after the internal calibration and can assume any value according to the datasheet, a different mezzanine card is used to receive the clock in the test system.

The Trigger, Control and Distribution System (TCDS) FMC 2SFP LEMO mezzanine card [72] features a clock input followed by a level converter circuit that

[1]LEMO is push-pull connectors often used for NIM.
[2]Nuclear Instrumentation Module (NIM)

translates the input signal level from ECL[1] to LVDS with constant delay. Figure 4.5 shows a photo of the card with the LEMO connectors on the top-left and the FMC connector on the right.

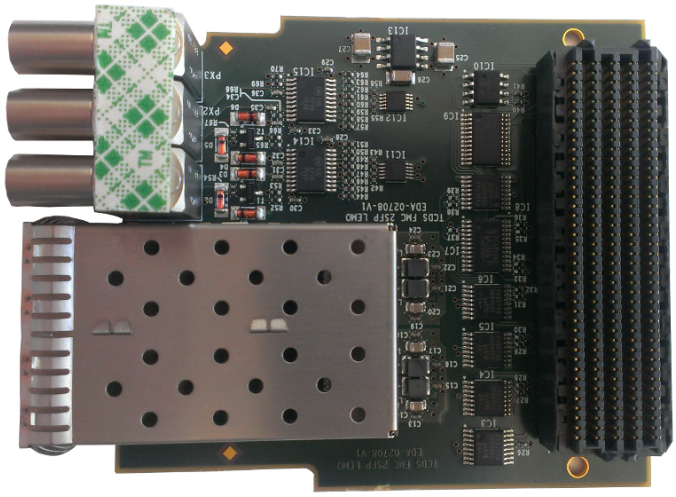


Figure 4.5: TCDS mezzanine card

The test system uses a portable computer to control the FPGA evaluation board through its Ethernet interface.

### 4.2.2 Firmware development

The error rate test system can receive and adjust the phase of the input signals with very high resolution. It checks the received data against errors and produces summary results that can be read out through the Ethernet interface. Figure 4.6 shows a block diagram of the test system with the firmware enclosed with a dashed line. The DDR input and PRBS evaluation units are replicated for each of the 32 channels. Note that the clock reception using the TCDS mezzanine card is omitted in the diagram.

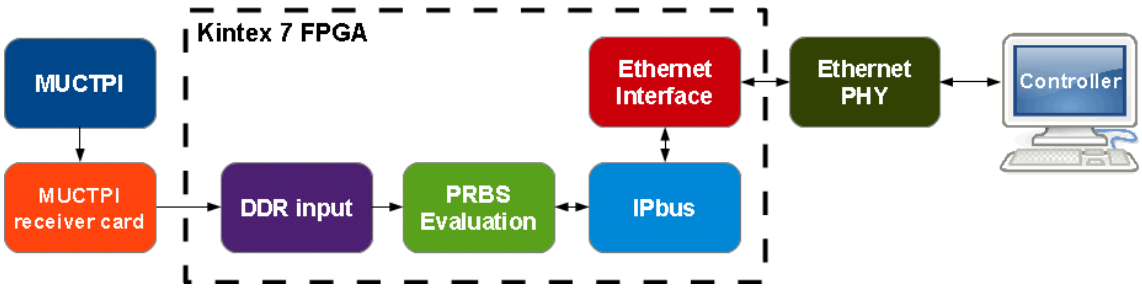



Figure 4.6: Error rate test system block diagram

[1]Emitter-Coupled Logic (ECL)

#### 4.2.2.1 DDR input

The DDR input block is in charge of receiving the data and applying a programmable delay on the data. The Xilinx 7-series family features internal delay line units, known as IDELAY blocks [73], with programmable tap selection for adjusting the required phase offset for each input. The test system controller selects the phase offset by choosing one of the 32 taps of the internal delay unit. The delay unit is calibrated to make sure the delay is constant over temperature, voltage and manufacturing process variations. The time delay per tap $\Delta_t$ is given by Equation (4.1) [73],

$$\Delta_t = \frac{1}{2N_{taps}F_{ref}}, \tag{4.1}$$

where $N_{taps}$ represents the number of taps, and $F_{ref}$ represents the reference frequency supplied to the self-calibration controller.

For the minimal reference frequency of 200 MHz, the resulting delay step is 78.125 ps. Therefore, the maximum delay of the IDELAY blocks is 2.5 ns. Since the MUCTPI system is sending data at 320 Mbps, resulting in a bit period $\Delta_{bit} =$ 3.125 ns, the delay cannot cover the full sampling window of the received data.

However, oversampling the data from the delay lines output can increase the phase offset adjusting range. For this purpose, the internal serialization/deserialization unit (ISERDES) [73] are configured in the oversampling mode (known as Networking mode in the Xilinx documentation) in order to latch the input data in four different sampling points using four orthogonal clocks. Figure 4.7 [66] shows a block diagram of the ISERDES unit in Networking interface mode.

The output signal from the IDELAY block is connected to the DDLY input port of the ISERDES block and four orthogonal (90° phase-shifted) clocks are connected to *clk* (0°), *oclk* (90°), *clkb* (180°), and *oclkb* (270°) ports. The outputs Q1-Q4 supply the data latched at the rising edge of *clk*, *clkb*, *oclk*, and *oclkb*, respectively, synchronously with the clock *clk*.

An on-chip Phase-Locked Loop (PLL) circuit [74] is used to generate two orthogonal clocks (*clk* and *oclk*), and the other two clocks are generated by inversion. Taking into account that the data are now sampled at four positions, the delay required $\Delta_r$ to cover the full sampling window is reduced as described in Equation (4.2).

$$\Delta_r = \frac{1}{4F_{clk}}, \tag{4.2}$$

where $F_{clk}$ represents the clock frequency the receiver is using to sample data.

For $F_{clk} = 320\,\text{MHz}$, $F_{clk} = 160\,\text{MHz}$, and $F_{clk} = 80\,\text{MHz}$, the respective delay

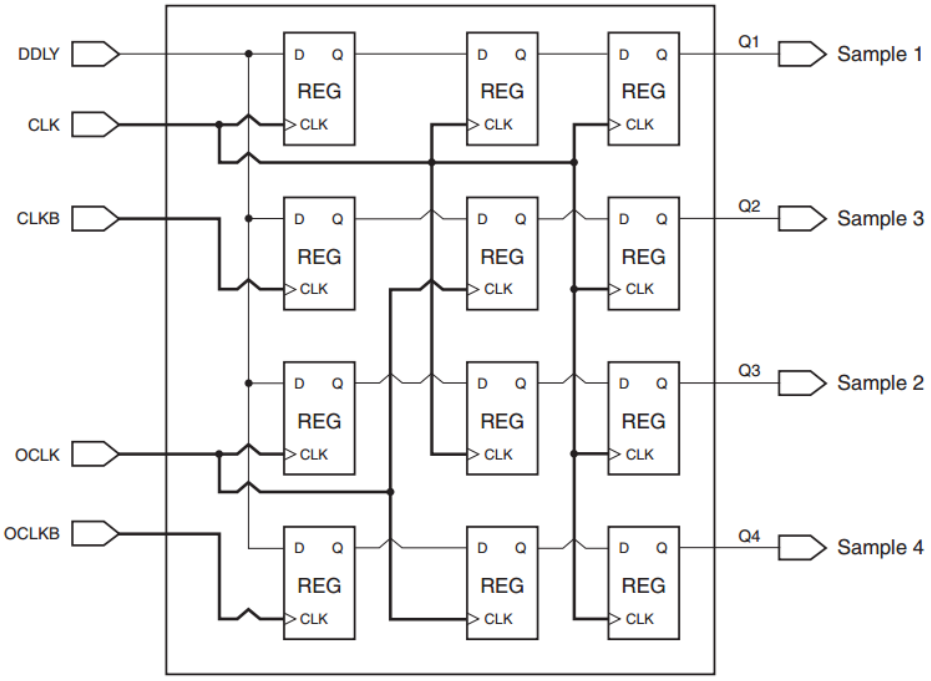



Figure 4.7: Xilinx ISERDES block diagram in Networking interface mode

required $\Delta_r$ values are described in Equation (4.3).

$$\Delta_r = \begin{cases} \frac{1}{4\times 320\,\text{MHz}} = 781.25\,\text{ps} & \text{if } F_{clk} = 320\,\text{MHz} \\ \frac{1}{4\times 160\,\text{MHz}} = 1.5625\,\text{ns} & \text{if } F_{clk} = 160\,\text{MHz} \\ \frac{1}{4\times 80\,\text{MHz}} = 3.125\,\text{ns} & \text{if } F_{clk} = 80\,\text{MHz} \end{cases} \tag{4.3}$$

Figure 4.8 shows a timing diagram of the four different sampling points using four orthogonal clocks running at three different frequencies. On the top is shown the input signal and the bit period window $\Delta_{bit}$. The bottom part shows the delay required $\Delta_r$ when the receiver logic is running in 320 MHz, 160 MHz or 80 MHz. The arrows in red, yellow, green and blue indicate the segments of the sampling window at which the signal is latched at four orthogonal clocks phases 0°, 90°, 180°, and 270°. Note that the lower is the $F_{clk}$ value, the higher $\Delta_r$ value is needed.

The reduction of the clock frequency simplifies the timing of the system, allowing the fitting tool to place and route the logic with more relaxed constraints. Considering the limitation on the maximum delay available by the IDELAY block ($\Delta_r$ has to be lower than or equal to 2.5 ns), only $F_{clk} = 320\,\text{MHz}$ and $F_{clk} = 160\,\text{MHz}$ can be used. Since both could be used, the lower frequency value is selected ($F_{clk} = 160\,\text{MHz}$) allowing the receiver logic to run at half the transmission data rate. The logic running on the slower clock is implemented using Double Data Rate (DDR) lines that transfer two bits per 160 MHz clock cycle.

Since the programmable line delay can exceed the period of each of the four

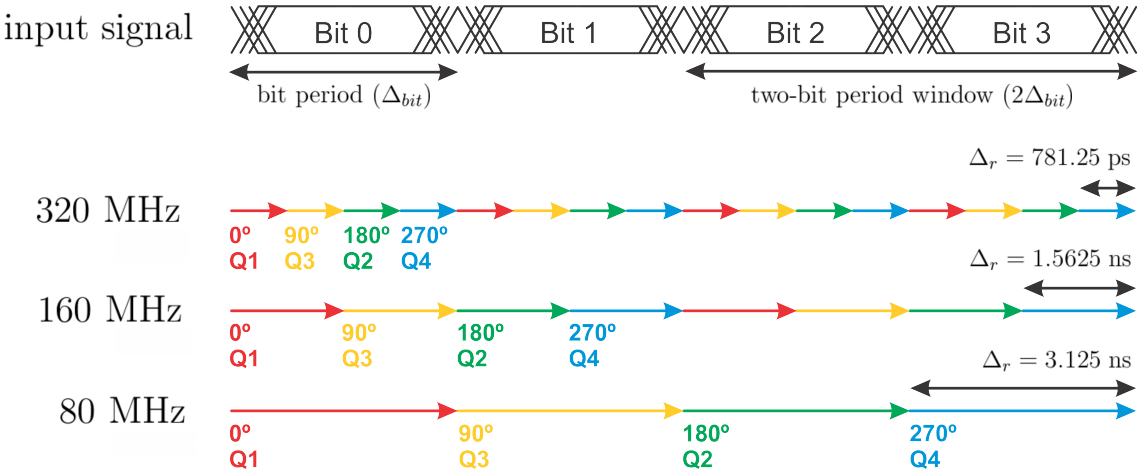



Figure 4.8: Timing diagram of the four different sampling points using four orthogonal clocks running at 320 MHz, 160 MHz, and 80 MHz

sampling window segments shown in Figure 4.8, the delay line tap selection is limited to $\Delta_r$. The maximum allowed tap value $N_{tmax}$ is given by the delay required $\Delta_r$ divided by the delay of one tap $\Delta_t$, as described in Equation (4.4).

$$N_{tmax} = \frac{\Delta_r}{\Delta_t} = \frac{1.5625\,\text{ns}}{78.125\,\text{ps}} = 20. \tag{4.4}$$

This means that for each of the four segments of $2\Delta_t$, only the taps from 0 to 19 can be selected, otherwise the delay will exceed 1.5625 ns and the data from the same time segment will be seen in more than one of the four outputs. Therefore, only $4 \times 20 = 80$ combinations of outputs and taps are permitted. Figure 4.9 shows the allowed taps values and the respective total delay obtained from each output Q1-Q4.

For instance, if data have to be sampled with a phase offset of 135°, the output Q3 (90°) and tap number 10 has to be selected.

In order to detect transitions, the test system also implements a second path to compare the actual signal with the signal delayed by a fixed number of delay taps. Figure 4.10 shows both paths followed by the respective XOR gates outputs that compares the signals from both paths.

The tap delay of the first path, the so-called master path, is set using the *delay control* input signal. The setting for the second path, the so-called slave path, is based on the master path configuration plus a programmable parameter K, as shown in Figure 4.10. For the tests, K is set to 1, allowing transitions to be detected even in a very short interval of $\approx 80\,\text{ps}$. Note that the slave path receives the inverted output of the differential input buffer and, for this reason, an XOR gate is used to provide the match result.

The *match* signal is low whenever a transition is detected. Transitions of the

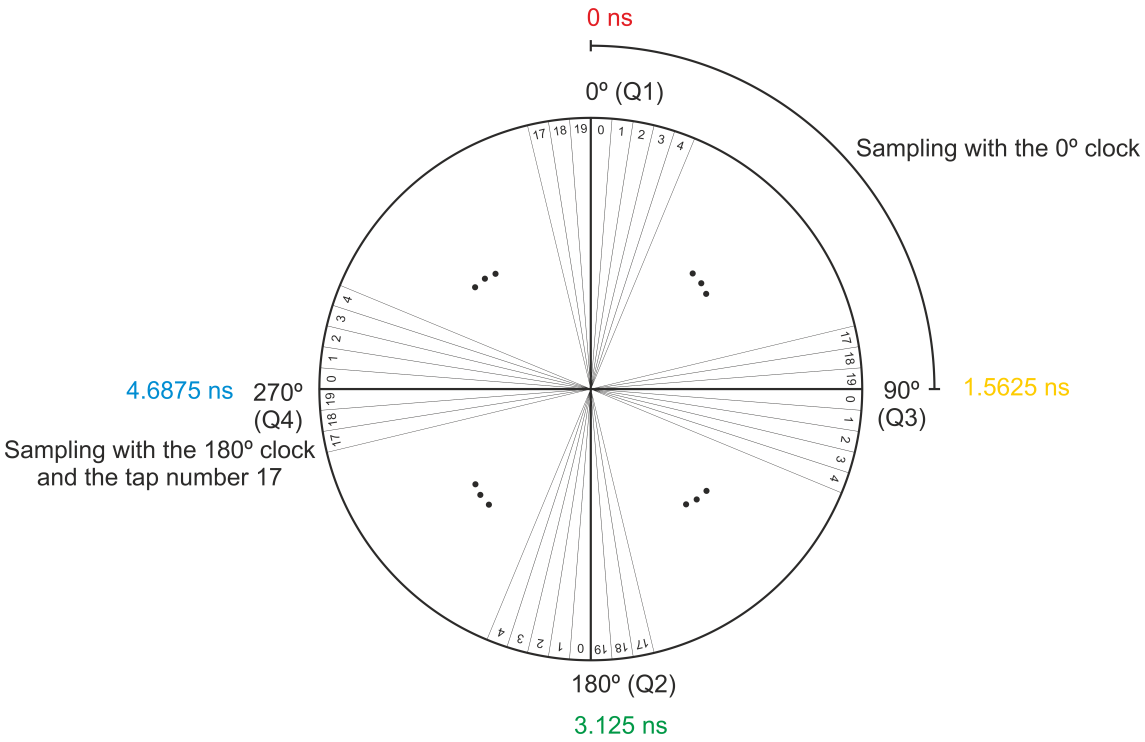



Figure 4.9: Phase coverage, when the tap delay selection is limited to 20 taps and four orthogonal phases are used to sample the input data

data close to the sampling point can result in metastability and lead to bit errors on received data. Metastability occurs whenever the setup and hold times in a flip-flop are violated. It happens because the flip-flop register enters a state where the output is unpredictable, this state is also known as the metastable state or the quasi-stable state. At the end of this state, the flip-flop outputs settles down to either '1' or '0'.

The *match* signal is set to high whenever both signals from master and slave paths are different[1].

Figure 4.11 shows a timing diagram that illustrates how transitions can be de-

[1]Because the inversion of the differential buffer output

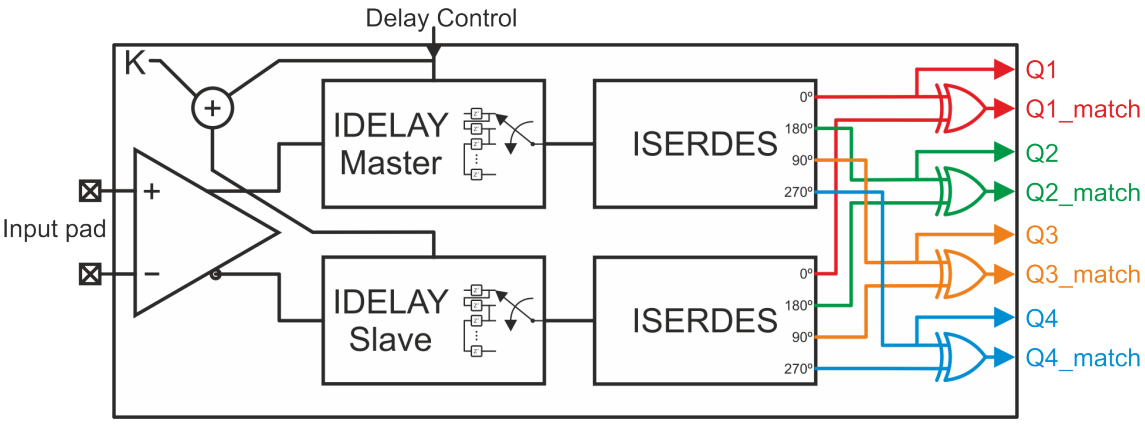



Figure 4.10: DDR input block diagram

tected using the DDR input circuit shown in Figure 4.10.

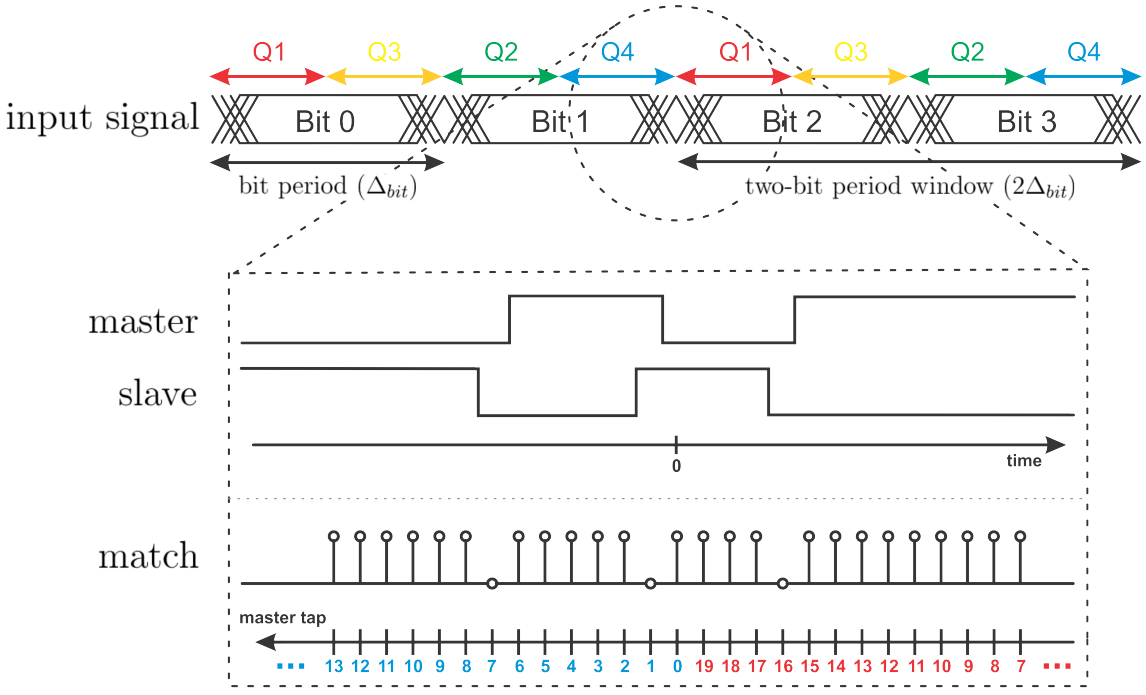



Figure 4.11: Timing diagram illustrating how transitions can be detected using the DDR input circuit

On the top of the figure, the input signal and the respective interval covered by each of the Q1-Q4 output is shown. On the bottom, the first part shows the continuous output signal from the master and slave IDELAY blocks with taps set to zero and one respectively. The second part illustrates the match value in Q4 and Q1 ports for a reduced range of their tap values. The tap values in blue and red indicates the master tap configuration for Q4 and Q1 outputs respectively.

One of the three transitions shown in Figure 4.11 is seen in the Q4 match output when the master tap is set to 7 or 1, or in the Q1 match output if the master tap is set to 16. As the output of only one tap can be seen at a time, transitions cannot be detected in every 80 positions of the $2\Delta_{bit}$ sampling window simultaneously. Therefore, the transition detection has to be divided into steps. Each step checks a maximum of four positions of the sampling window simultaneously, taking into account that four match outputs are monitored.

The test system covers the full sampling window checking two positions per step, which optimizes the usage of logic resources by splitting the measurement into two stages Figure 4.12 shows the procedure used to cover all 80 positions of the sampling window.

The first 20 steps check first and third quarters of the sampling window monitoring, at the same time, Q1 and Q2 ports, while the last twenty steps check the second and fourth quarters of the sampling window monitoring the Q3 and Q4 ports. Note

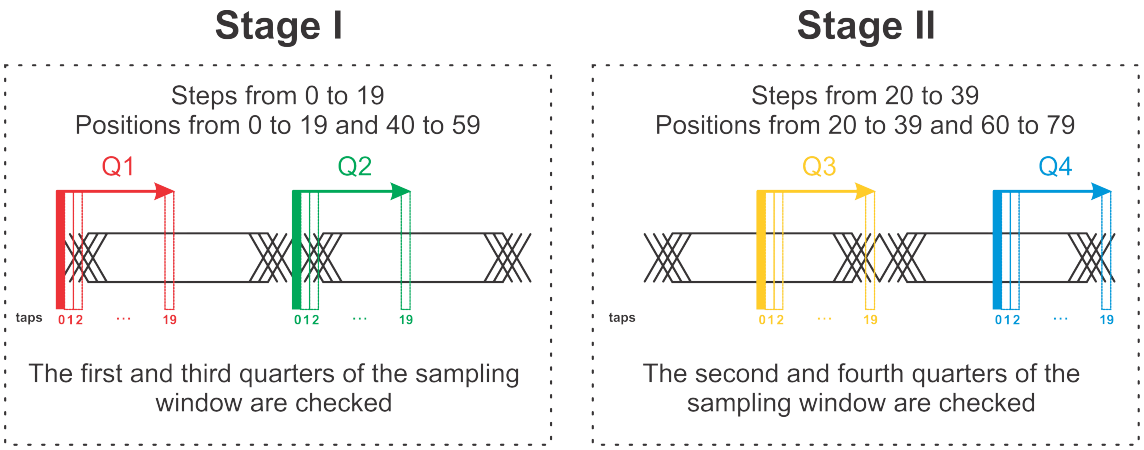



Figure 4.12: A diagram of the two stages performed to cover the full sampling window

that the outputs Q1-Q4 are grouped in such way so as to supply the data latched at the same area of the bit period window for two consecutive bits. For example, Q1 and Q2 outputs supply data from the first half of the sampling window for bits 0 and 1, then 2 and 3, and so on. Each step has to be checked for the existence of transition various times because transitions can be rare or even not exist depending on the position of the sampling window.

#### 4.2.2.2 PRBS evaluation

The PRBS evaluation unit checks the received data and produces summary results to quantify the reliability of data reception. It performs two sorts of measurements:

1. It checks for the existence of transitions at a giving sampling phase.
2. It compares the received PRBS data with a reference and counts the number of errors.

The two measurements are complementary. The first method identifies the metastable regions in the bit period window using the DDR input match ports for detecting transitions. The second method estimates the BER in a stable sampling point by counting the number of errors.

##### 4.2.2.2.1 Transition detection circuit

Figure 4.13 shows the block diagram of the transition detector circuit. Each pair of match signals from the DDR input unit are combined into a single match signal using a logic AND. The *phase selection* input port is used to select which of the match ports will be checked depending on the segment of the bit period window

being measured, as described in Figure 4.12. The *match* signal is high if both match signals from the DDR input are high.

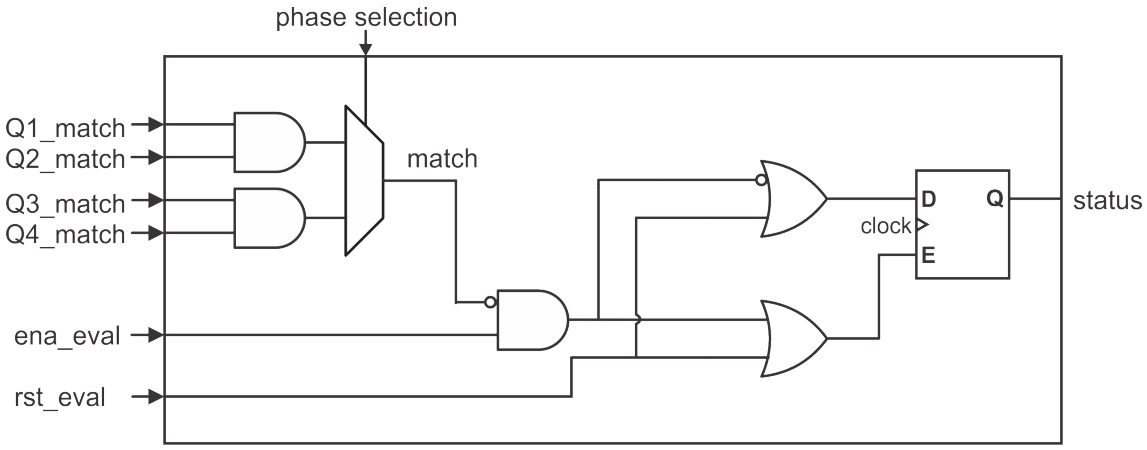



Figure 4.13: Transition detection circuit

The *status* register is set at the beginning of the test and reset when a transition occurs.

#### 4.2.2.2.2 PRBS receiver circuit

The second measurement compares the received data to an internally generated pseudo-random sequence [75] once the internal generator is synchronized with the input data.

Figure 4.14 shows the PRBS receiver circuit. The PRBS generator can operate in two modes: in the first mode the registers are initialized using the input data. In the second mode, the generator produces a free-running sequence synchronized with the input pattern.

If the synchronization is successful, the internal PRBS generator produces a sequence identical to the transmitted sequence. The internal generator in the PRBS receiver unit is the same as the generator implemented in the transmitter (MIOCT), as described in Section 4.1.

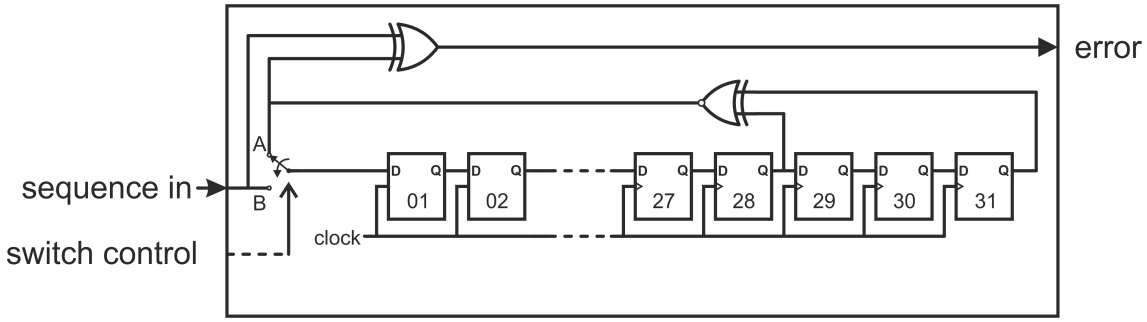



Figure 4.14: PRBS receiver circuit

When the switch is in position B, the generator loads the serial input sequence. Note that the switch has to stay for at least k[1] clock cycles in position B. Equation (4.5) describes the minimum time for loading the input sequence into the generator registers.

$$T_s = k\Delta_{bit} = 31 \times 3.125 \text{ ns} = 96.875 \text{ ns}. \tag{4.5}$$

After all the registers have been initialised, the generator is ready to generate the free-running sequence by setting the switch to position A. This sequence is synchronized with the input pattern.

The input sequence and the internally generated sequence are compared, and the *error* signal indicates whenever an mismatch occurs. If any error has occurred while loading the seed into the generator, the number of errors detected will be very high and indicates the occurrence of one of the two following scenarios:

1. The input data is sampled in the metastable region, which results in very high error rate. In this case, a new synchronization attempt will not succeed.

2. There are few bit errors in the received data. Therefore, one or more registers were loaded with corrupted data during initialisation, and the internal generator is in a different state from the transmitter. The number of detected errors will be very high because the internal generator did not receive a valid seed. The synchronization must be repeated, and the internal generator will load an error-free sequence the next time, in the case the error rate is low enough.

The phase scan results produced by the transition detection unit helps to distinguish the two cases by indicating the sampling points in the metastable region.

#### 4.2.2.2.3 PRBS evaluation unit

Figure 4.15 shows a block diagram of the PRBS evaluation unit. Two instances of the PRBS receiver unit are connected to each of the two lines of the selected DDR pair (Q1, Q2 or Q3, Q4). A pair is chosen by the *phase selection* signal, in the same way, as in the transition detector circuit.

The *error* output from both internal PRBS generators are connected to an error counter. If only one of the generators detects an error, the counter increments by one, if both detect an error, it is incremented by two. The counter is active only if the *ena_eval* signal is asserted, and the counter is reset in case the signal *rst_eval* is asserted. The counter stops incrementing when it reaches the maximum value to prevent overflow. The bit counter outputs the number of bits measured and the data from both counters are used to calculate the BER value.

[1] k represents the number of registers in the internal generator

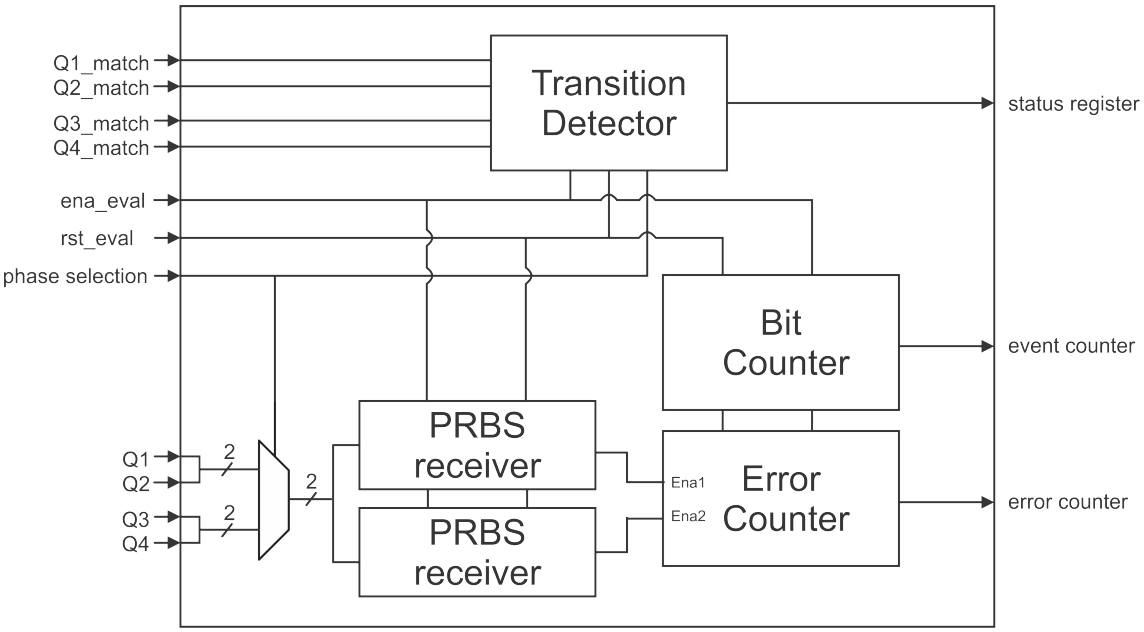



Figure 4.15: PRBS evaluation block diagram

#### 4.2.2.3 IPbus unit

The IPbus is used to control, i.e. to configure the DDR input and the transition detector circuit and to read out the test results through Ethernet.

IPbus [76] is an open-source project that was initially developed for the Compact Muon Solenoid (CMS) [77] experiment at CERN, as the control interface for the Micro Telecommunications Computing Architecture (MTCA) [78] based systems. TCA is a crate standard initially developed for telecommunication applications, which is being used in ATLAS and CMS for the upgrade of the trigger electronics, as an alternative to the VME standard. Even though IPbus was originally developed for the CMS experiment upgrade, it is foreseen to be used in many other applications, such as the ATLAS L1Calo trigger upgrade [79] and the DAQ system of the COMPASS experiment[1] [80].

Figure 4.16 shows a block diagram that describes the principle of operation of IPbus.

The IPbus software interface layer (PyChips) provides methods to perform R/W transactions requests to registers mapped into a virtual memory space. The user writes software that invokes these methods, generating so-called IPbus requests. The IPbus requests are encapsulated into an Ethernet packet and transmitted to the end-user hardware through Ethernet connection.

At the target, the Ethernet interface decodes the Ethernet packet into a User Datagram Protocol (UDP) packet that is sent to the IPbus core. The Ethernet interface implements the Ethernet Media Access Control layer (MAC) and the PHY

[1]Common Muon and Proton Apparatus for Structure and Spectroscopy

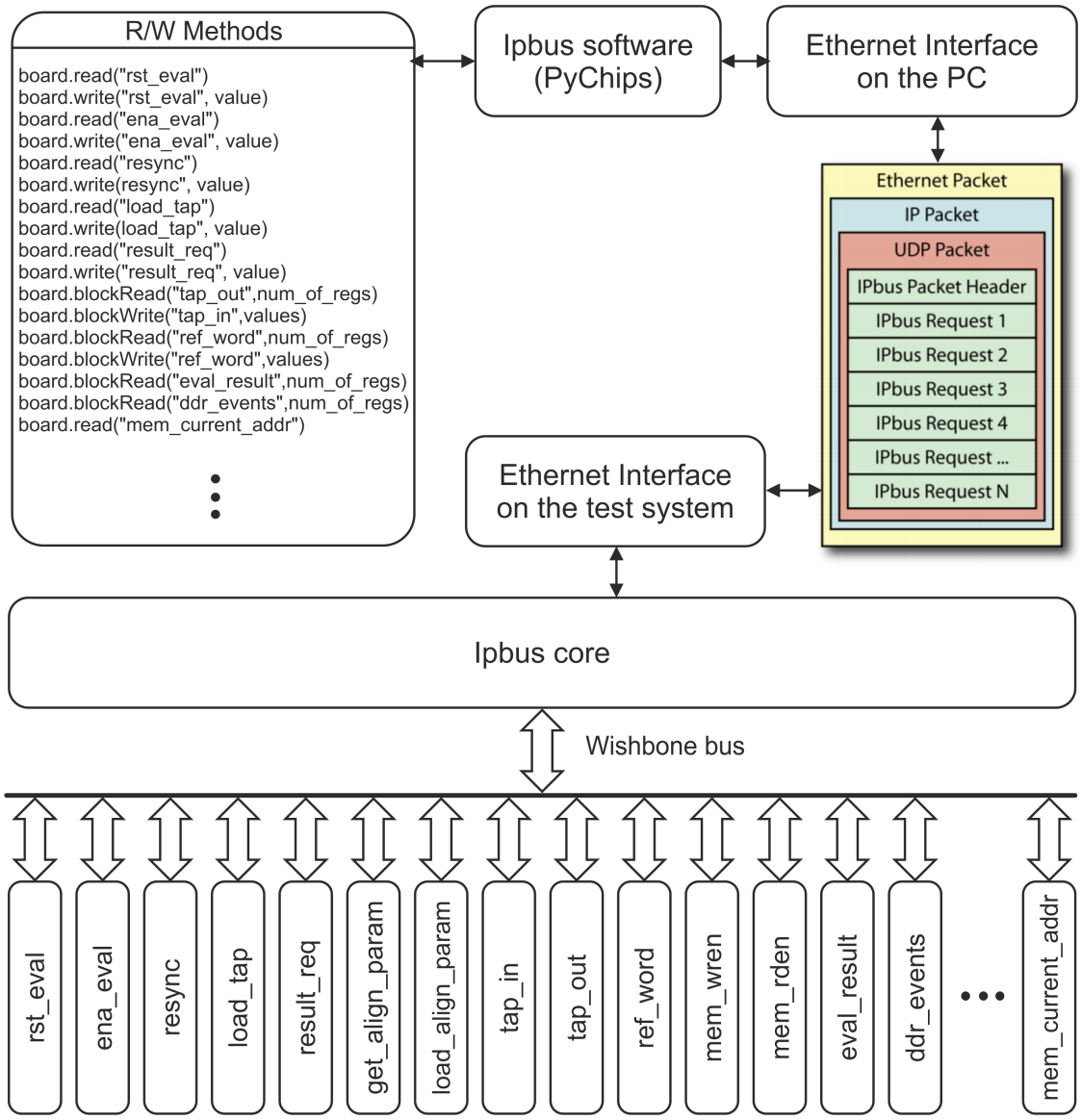



Figure 4.16: Principle of operation of the IPbus system

interface by using Intellectual Property (IP) cores from Xilinx. The IPbus core implements a UDP socket, which translates this packet into R/W bus transactions requests for a Wishbone bus [81]. The Wishbone Bus is an open source hardware computer bus intended to allow the parts of an integrated circuit to communicate with each other.

Each of the transaction requests received by the IPbus core is associated with an address position in a virtual memory space, previously defined by the user in a configuration file. The IPbus core fabric implements an address decoder that associates each of these address positions with one of the several slave units implemented by the user. These slave units implement a bridge between the Wishbone bus and the different control interfaces in the user design.

The slave units implemented for the test system allow the configuration and

monitoring of the DDR input and PRBS evaluation units, by reading and writing their respective configuration registers. Moreover, the slave units allow the controller software to generate phase scan and BER plots by reading out data from registers (for example the *status* signal from the Transition Detector circuit) that stores the test results generated by the firmware.

### 4.2.3 Software development

The test system software configures the test system and reads out results from the PRBS evaluation unit for generating a phase scan histogram and a plot of the BER of the received data. An overview of the software operation is shown bellow.

1. Load input parameters.
2. Check if the test system is available and ready.
3. Run a short-term test (every sampling position is checked).
4. Read results.
5. Run a long-term test (only selected sampling positions are checked).
6. Produce summary results and publish them on a web page.

The test system software begins by loading the input parameters defined by the user, such as the duration of the short and long-term tests, the sampling positions to be checked in the long-term test and the test system Internet Protocol (IP) address. Then, the software connects to the test system hardware through the Ethernet interface and checks if the correct firmware version is loaded and the status of the monitoring registers. The monitoring registers indicates if the on-chip PLL and the programmable delay calibration units are ready for operation and, if so, the software executes a short test to perform a phase scan of the received data. From this phase scan plot, the user selects the positions of the bit period window to be checked in the long-term test.

During a test, the software executes a test iteration for each position of the bit period window being checked. Figure 4.17 shows the Finite State Machine (FSM) diagram of the software operation during a test iteration. The short-term and long-term tests differ only in the duration of the test and the selected sampling positions being checked.

Each test iteration starts by selecting the appropriate DDR pair (Q1, Q2 or Q3, Q4), and the delay tap associated with the sampling position being checked. The selection of the DDR pair and the tap delay is performed individually for each of the 32 channels.

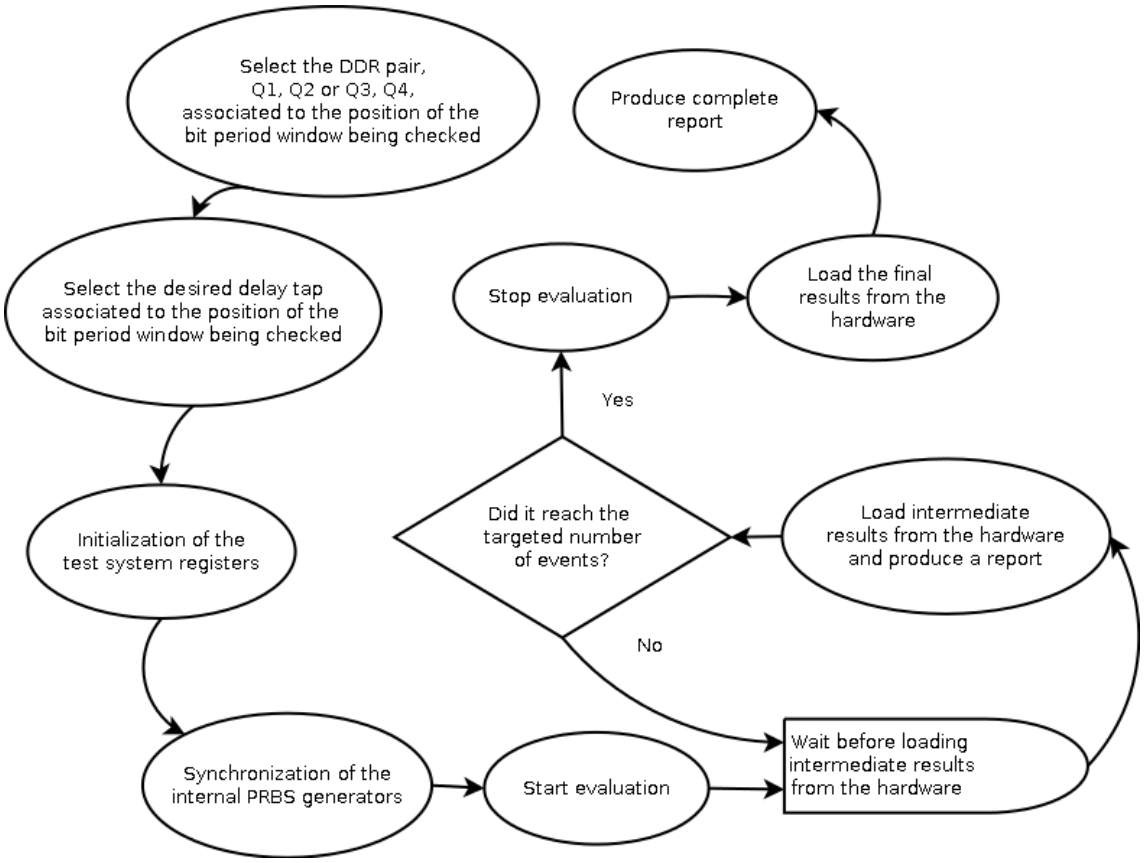



Figure 4.17: FSM diagram of the software operation of a test iteration (an iteration is executed for each position of the bit period window being checked)

Then, the software initialises the control and result registers. The software checks the status of the control registers, and then sends synchronization requests to all PRBS receiver units. The software performs the synchronization by toggling the feedback switch for about 1 ms. This is orders of magnitude longer than the required time defined in Section 4.2.2.2.2.

After the synchronization, the software starts a test for every channel in parallel. Then, the application halts for a predefined time before loading results from the transition detector status registers and the BER counters. If the bit counter reached the targeted number of bits, the test system software stops the test[1]. Otherwise, the test system enters a loop, waiting for and loading results until the bit counter reaches the desired number of bits. The application publishes intermediate results on a web page every time the loop is repeated. The publication of these so-called live results enables the user to keep track of results with the test running, which allows checking if the test was correctly set up, and avoids noticing any misconfiguration only at the end of a long-term test.

[1]The test is stopped by deasserting the *ena_eval* signal.

When the test has finished, the application loads the final results from the hardware, produces a complete report, publishes the results on a web page, and exits. The software publishes the results for each channel in the following formats:

1. A color-coded histogram with the value of the transition detector status register at each sampling point.
2. A plot of the BER as a function of the sampling position.
3. A table with the BER values and the counter values for every sampling position.
4. A complete report of the test results and the test system hardware status.

The software is written in Python, and it uses several packages in order to handle bit strings, to generate plots, to generate HyperText Markup Language (HTML) for the web page, and to produce standardized logs.

## 4.3 Test results

The tests were performed in the CTP lab, where there is a full MUCTPI system for firmware and software validation. The MUCTPI trigger outputs were configured to transmit data at a bit rate of 320 Mbps. The software was set to perform long-term tests of 120 h, and the results from the error rate test system are presented in the following sections.

### 4.3.1 Transition detection results

Figure 4.18 shows the phase scan color-coded histogram, which indicates the position of the bit period window where transitions were detected.

The abscissa and ordinate axes indicate the different positions of the sampling window points and the channel number respectively. The bins in green indicate that no transitions were detected at a given position (transition-free region) whereas the ones in red indicate that at least one transition was detected (metastable region).

The plot also shows that on average 75% of the bit period window points are transition-free while metastability is observed in only 25% of them. Also, different phase offsets for each channel can be observed due to the difference between the trace[1] length of all 32 channels in both MUCTPI receiver mezzanine card and FPGA evaluation board and the difference between the trace length of the two MIOCT trigger outputs.

[1] A printed or etched wire on a printed circuit board

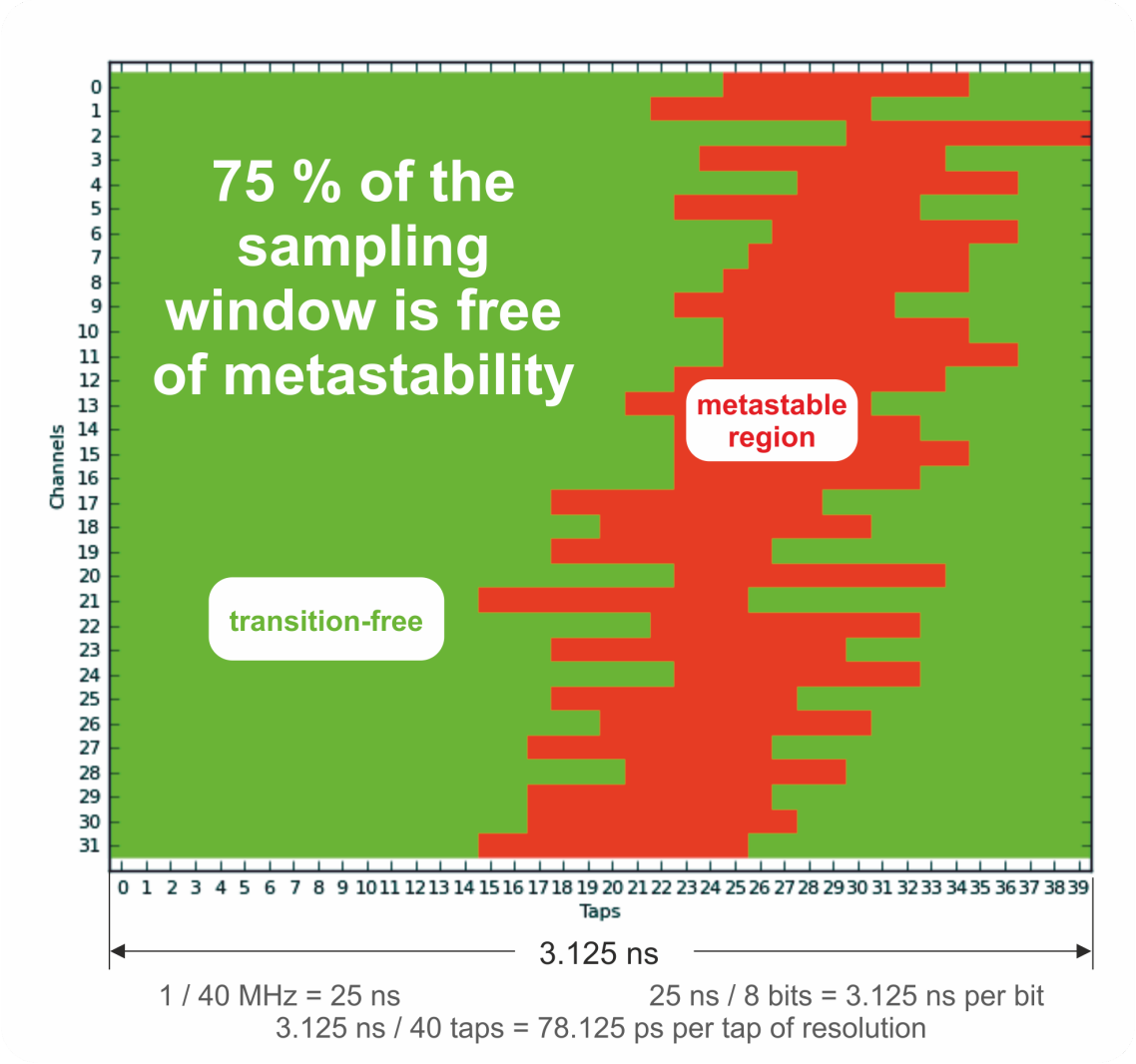



Figure 4.18: Phase scan of the received data from the MUCTPI system with the electrical trigger outputs operating at 320 Mbps

The phase scan results show that the MUCTPI system can transmit data when overclocked by a factor of 8 with a comfortable timing margin.

Reliable data transmission can be established by sampling the data at any position within the transition-free region. However, the BER can be minimized by calculating the optimal sampling point. The optimal sampling point can be estimated by finding the centre of the green region, or the position opposed to the centre of the metastable region, as indicated in Figure 4.19.

For example, the centre of the metastable region for channel 31 has been detected at the tap number 20, then the optimal sampling can be performed sampling data at phase 0. Data from position 0 is acquired by selecting the DDR pair Q1 and Q2 and setting the tap delay to 0. The same process can be repeated for every channel, and a list of the optimal sampling points is produced.

A long-term test using the taps at the border of the metastable zone was per-

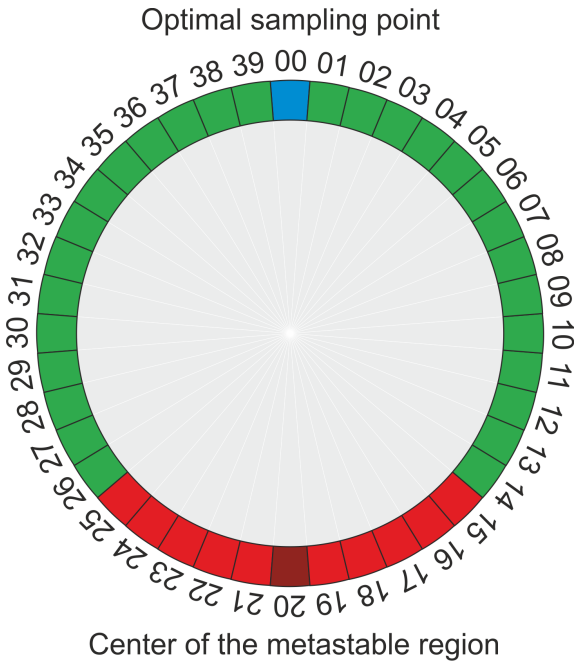



Figure 4.19: A cyclic description of the transition detector results for the channel 31

formed to check the width of the metastable region and its stability in time. The metastable region can move due jitter and drift of the clock phase, and it affects the position of the optimal sampling point. Even though the transmitter sends its clock to the receiver, the phase of the received clock can change with temperature, voltage fluctuation and process variations. The phase drift analysis is essential to guarantee that the system can operate over a long ATLAS data-taking run without the need for recalibration. Additional long-term tests of 120 h, taking into account positions of the bit period window at the boundaries of the metastable region did not indicate drift of the clock phase longer than 80 ps.

In a separate test, the firmware of one MIOCT card was modified to send pseudo-random data at 400 Mbps through only two electrical trigger outputs. Next, the firmware of the error rate test system was modified in order to be able to sample data at the same rate. Equation (4.4) defined in Section 4.2.2.1 was used to calculate the maximum tap value that prevents overlap between the different timing windows being checked. For a bit period window $\Delta_{bit} = 2.5\,\text{ns}$ the maximum tap selection is given by Equation (4.6).

$$N_{tmax} = \frac{1.25\,\text{ns}}{78.125\,\text{ps}} = 16. \tag{4.6}$$

Figure 4.20 shows the results from the transition detector circuit when two MUCTPI electrical trigger outputs are operating at 400 Mbps.

The region in green indicates the transition-free sampling points while the bins

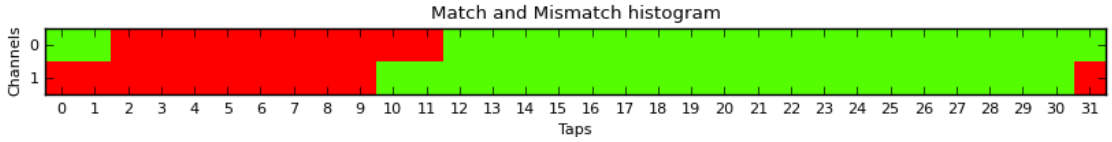



Figure 4.20: Phase scan color-coded histogram of the received data from the MUCTPI operating at 400 Mbps

in red are associated with sampling in a metastable region. The transition-free zone corresponds to $\approx 65\%$ of the bit period window.

In order to have a longer timing margin, the data rate was kept at 320 Mbps since there was no need to increase it.

### 4.3.2 PRBS evaluation results

Even in a system without any design issues, errors can still happen due to random noise from external sources, and in these cases the BER performance is limited by random noise and/or random jitter. Taking into account the measurement of the error probability is not possible, it is usually satisfactory to estimate the probability of the BER value to be lower than an upper limit with a quantifiable confidence.

Usually, it is enough to say that the BER is at least as good as a required value defined for some design constraint or standard. For example telecommunications protocols, such as Synchronous Optical Networking (SONET), require a BER of $10^{-10}$ using long pseudo-random bit sequences, such as the PRBS-15 or PRBS-23, depending on the data transmission rate [82]. Data communications protocols, such as the Fiber Channel and Ethernet commonly specify a BER performance of $10^{-12}$ using shorter bit sequences, when an 8b10b encoder is used. In some cases, system specifications require a BER of $10^{-16}$ or lower [83].

For example, being acceptable to have a single bit error in 24 h, the upper limit can be defined in the order of $1 \times 10^{-15}$ with the 32 MUCTPI electrical trigger outputs operating in parallel at a bit rate of 320 Mbps. It is possible to say that the probability of error is estimated to be lower than $1 \times 10^{-15}$ with a quantifiable confidence level (CL). Equation (4.7) [84] shows the definition of CL.

$$CL = P\left[P(\varepsilon) < \gamma | (\varepsilon, n)\right], \tag{4.7}$$

where $\gamma$ represents the specified upper limit, $\varepsilon$ represents the number of bit errors detected in a given measurement, and $n$ represents the number of bits measured.

Based on this definition, the value of the confidence level for a given test without errors is given by Equation (4.8) [84],

$$CL = 1 - e^{-\gamma n}. \tag{4.8}$$

During the long-term test, data from $\approx 1.38 \times 10^{14}$ bits were accumulated for each channel and no error occurred in any of the channels when sampling data at the optimal sampling point. Considering that the MUCTPI aggregate data rate of 10.24 Gbps (32 $\times$ 320 Mbps), the MUCTPI system sent $\approx 4.42 \times 10^{15}$ bits, through the 32 electrical trigger outputs. Thus, the confidence level CL of the BER measurement, taking into account the upper limit value $\gamma$ of $1 \times 10^{-15}$, can be expressed as in Equation (4.9).

$$CL = 1 - e^{-\gamma n} = 1 - e^{-1 \times 10^{-15} 4.42 \times 10^{15}} = 0.9880. \tag{4.9}$$

Based on the test results, the BER is estimated to be lower than $1 \times 10^{-15}$ with a confidence level of 98.80%, which implies that, if the test is repeated various times, the BER value is estimated to be at least as good as $1 \times 10^{-15}$ in 98.80% of the cases.

### 4.3.3 Demonstration of the complementarity between the phase scan and BER results

Figure 4.21 demonstrates how the phase scan and the BER results complement each other, showing together the BER plot and respective phase scan histogram of two MUCTPI trigger outputs operating at 320 Mbps during a short-term test (10 seconds per tap). As can be seen in this plot, a fairly accurate estimation of the width of the metastable region can be produced even with a quick phase scan. The test system software automatically generates this plot, and it is part of the aforementioned live results.

Note that data from only two channels are printed in this plot for improving the readability. The phase scan results are complementary to the BER plot and vice versa. The metastable region seen by the transition detector circuit is located in the same region where the PRBS receiver unit detected errors. Moreover, the metastable region lasts for 625 ps for both channels (8 taps).

As can be seen in the BER plot, the tap positions inside the metastable region show very high BER values, while the points at the edges illustrate rapidly decreasing BER values. For example, only seven errors out of 3.2 billions of bits were detected on channel one position 17, resulting in a BER $\approx 2.18 \times 10^{-9}$. As the PRBS receivers do not lock for the taps inside the metastable region (excepted the taps at the border that can eventually synchronize depending on the error rate) all the other (very high) BER values are invalid.

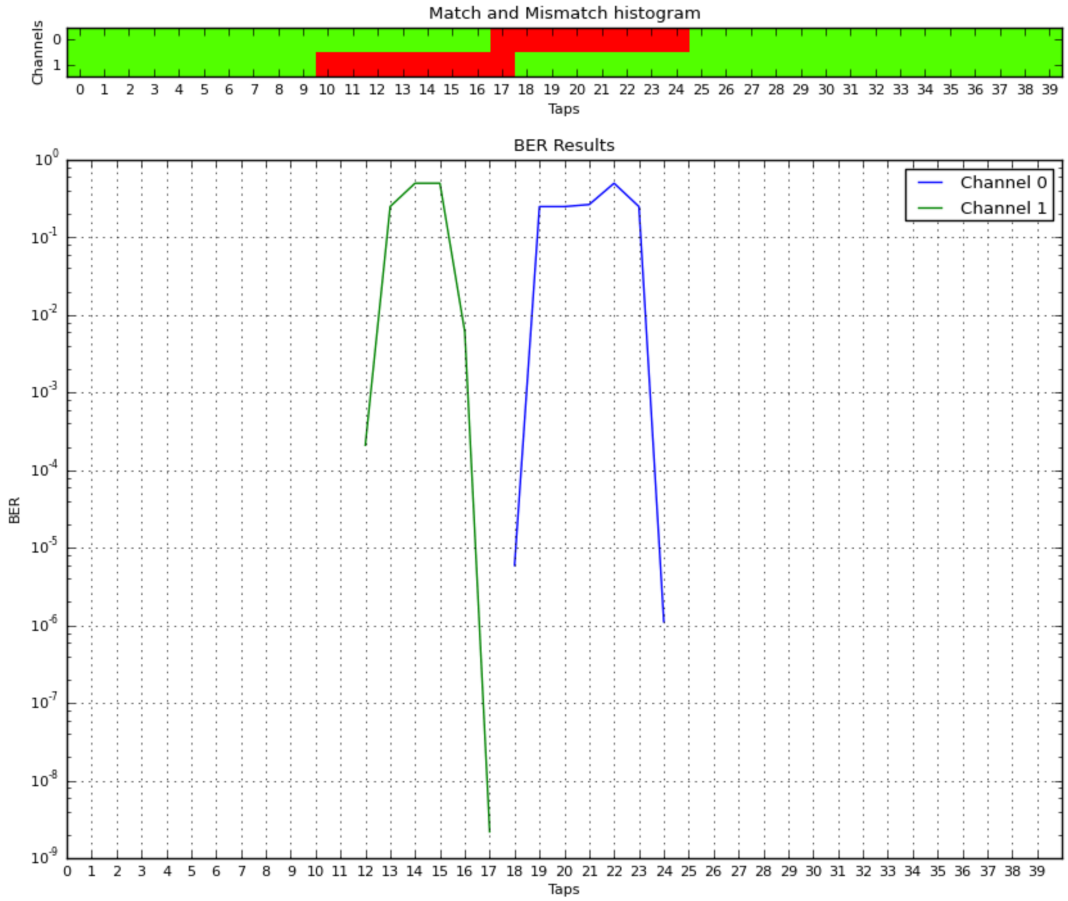



Figure 4.21: A plot of the BER of the data received from two MUCTPI electrical trigger outputs

## 4.4 Summary

An error rate test system has been developed to investigate if the transmission of data through the overclocked trigger outputs is reliable. This test system is based on an FPGA evaluation board and uses custom FMC cards for receiving data and clock from the MUCTPI. The FPGA device implements the data checking and a control interface to a portable computer. Over-clocking the signal received from the programmable on-chip input delay lines increased the phase adjustment range by a factor of 4. This approach was necessary in order to check the reliability of the data transmission and reception over the full bit period window shifting the sampling phase in 40 positions.

The phase scan results from the test system show that 75% of the bit period window is free of transitions. So, an optimal sampling point can be chosen to allow the system to transmit data with a comfortable timing margin. The BER of the received data, at the optimal sampling point, is estimated to be lower than $1 \times 10^{-15}$ with 98.80% of confidence.

The test results demonstrated that the MUCTPI system can reliably transmit data through the electrical trigger outputs operating at 320 Mbps. The next step was to upgrade the existing MIOCT firmware in order to add the topology functionality. The upgrade of the MUCTPI system firmware is described in Chapter 5.

# Chapter 5

# MUCTPI system upgrade

This chapter describes the changes on the MUCTPI system to transmit muon topological information to L1Topo. The firmware of the MIOCT module has been upgraded to extract, encode and transmit topological information through the electrical trigger outputs operating at a bit rate of 320 Mbps. In addition, this chapter presents the verification of the firmware upgrade through functional simulation and hardware tests.

Furthermore, this chapter presents the upgrade of the error rate test system presented in Chapter 4 in order to receive the serial data from the MUCTPI system and write it into a memory module, from where it can be read out for verification. The upgraded test system was used to check the muon topological information received from all 16 MIOCT modules.

## 5.1 Firmware upgrade of the MUCTPI system

In order to provide muon information to the topological processor, the MIOCT firmware has been upgraded to extract and encode topological information from the two candidates with the highest transverse momentum. The encoded data are then serialized at 320 Mbps (overclocking by a factor of 8) and transmitted to the MuCTPiToTopo interface using the electrical trigger outputs. As mentioned in Section 3.2.1.5, the trigger outputs were used to indicate the presence of at least one candidate in a selectable region of the muon trigger detectors during Run 1. The trigger output data were generated by programmable LUTs. This logic was removed from the firmware and replaced by the topological encoding unit.

Figure 5.1 shows a block diagram where the new functionality is highlighted. The topological encoding unit receives sector data from the synchronization and alignment unit and veto flags from the overlap handling unit. It extracts and encodes the topological information and sends it out through the electrical trigger outputs.

The memory interface connections were also changed to include debugging information from the topological encoding unit. In addition to the results from the overlap handling unit and multiplicity summing unit, the encoded topological information can now be written into the memory in order to verify the new firmware.

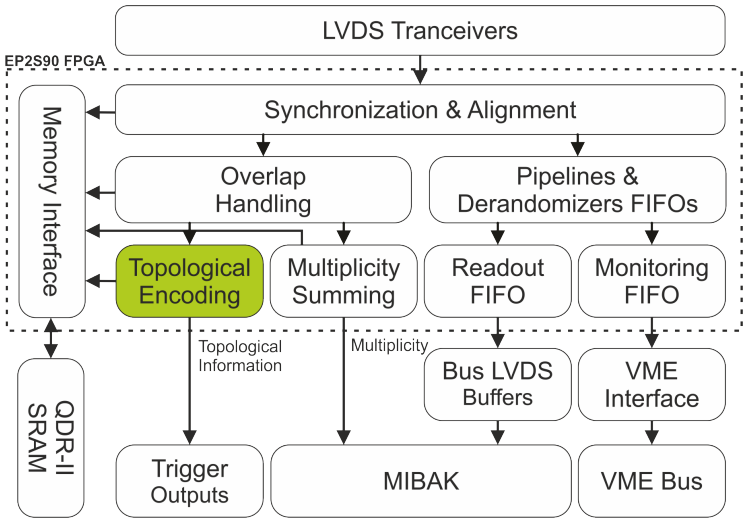



Figure 5.1: MIOCT block diagram

Figure 5.2 shows a block diagram of the topology encoding unit, the functionality is divided into four stages. In the veto unit, the muon candidates flagged by the overlap handling unit are suppressed. The remaining candidates are sorted by $p_T$ and the top two highest-$p_T$ candidates are encoded using programmable LUTs. Finally, the candidates are serialized at 320 Mbps using DDR outputs. In addition, the MIOCT module can also send PRBS-31 data for testing, as described in Section 4.1, and a 16-bit programmable pattern for phase and word alignment to the MuCTPiToTopo interface.

The LUTs and control registers of the unit are configured via VME and an internal address decoder is implemented to provide VME access to all programmable registers in the design. For instance, the LUTs are seen as memory devices on the VME bus and are configured using VME block transfers.

In addition, the topology encoding unit implements three 32-bit monitoring counters to indicate the presence of one, two, or more than two candidates. The rate at which these counters have to be read to prevent overflow is derived from the ratio between the maximum increment rate (40 MHz, the LHC clock) and the counter modulus ($2^{32}$), as shown in Equation (5.1).

$$F_{read} = \frac{40\,\mathrm{MHz}}{2^{32}} \approx 0.01\,\mathrm{Hz}. \tag{5.1}$$

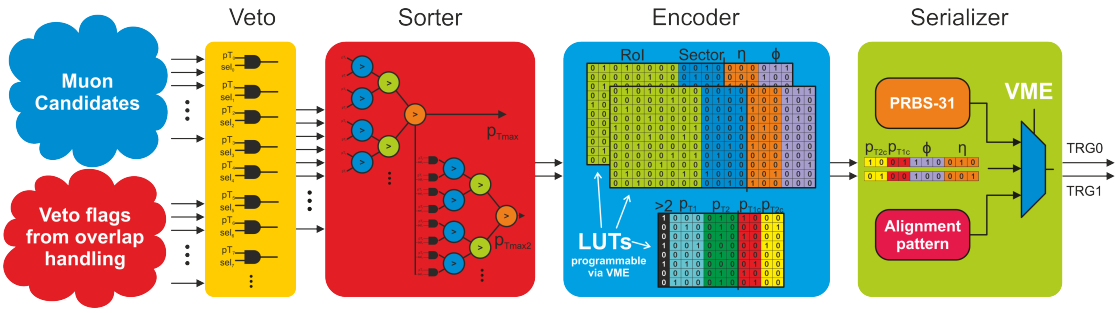



Figure 5.2: Topological encoding block diagram

### 5.1.1 Candidate veto

Pipeline registers are used to delay the sector data in order to align it with the veto flags. The veto logic suppresses the candidates that are flagged by the overlap handling unit and forwards the remaining candidates to the sorting unit.

The registers from the overlap handling unit that supply the veto flags are duplicated, in order to decouple the timing of the multiplicity and topology encoding paths. This technique is known as register duplication and improves the timing of the critical path. It also simplifies the placing and routing, by reducing the fan-out of the registers in the critical path.

### 5.1.2 Sorting

The sorting unit sorts the muon candidates according to their $p_T$ values and outputs the sector number, RoI and $p_T$ value of the $1^{st}$ and $2^{nd}$ highest-$p_T$ candidates.

For the design of this latency-critical path, different implementation approaches had to be evaluated in an effort to achieve optimal timing results. Sequential sorting algorithms can perform the functionality with very low usage of logic resources. For instance, a sequential sorting algorithm working in 160 MHz with a single comparator would take 26 clock cycles, the number of muon candidates in an octant, to find the highest-$p_T$ candidate. The latency $\Delta_{ss}$ for the sequential sorting algorithm is described in Equation (5.2).

$$\Delta_{ss} = 26 \times \frac{1}{160\,\mathrm{MHz}} = 162.5\,\mathrm{ns}. \tag{5.2}$$

This latency is too long when compared to the overall MUCTPI latency of $\approx 125\,\mathrm{ns}$ [85], hence not acceptable for the sorting implementation. In order to minimize the latency of this path, the sorting unit therefore implements a parallel processing approach by instantiating every necessary comparison as to find the highest-$p_T$ candidate in parallel. An example with five elements is shown in Table 5.1.

Table 5.1: Comparison matrix for sorting five elements using a parallel processing approach

| | **b** | **c** | **d** | **e** |
|---|---|---|---|---|
| **a** | $p_{Ta} \geq p_{Tb}$ | $p_{Ta} \geq p_{Tc}$ | $p_{Ta} \geq p_{Td}$ | $p_{Ta} \geq p_{Te}$ |
| **b** | $\overline{(p_{Ta} \geq p_{Tb})}$ | $p_{Tb} \geq p_{Tc}$ | $p_{Tb} \geq p_{Td}$ | $p_{Tb} \geq p_{Te}$ |
| **c** | $\overline{(p_{Ta} \geq p_{Tc})}$ | $\overline{(p_{Tb} \geq p_{Tc})}$ | $p_{Tc} \geq p_{Td}$ | $p_{Tc} \geq p_{Te}$ |
| **d** | $\overline{(p_{Ta} \geq p_{Td})}$ | $\overline{(p_{Tb} \geq p_{Td})}$ | $\overline{(p_{Tc} \geq p_{Td})}$ | $p_{Td} \geq p_{Te}$ |

The number of comparators needed to find the highest-$p_T$ candidate is derived from the number of different combinations of 2 elements chosen from a set of E elements, as described in Equation (5.3).

$$N = \binom{E}{2} = \frac{E(E-1)}{2}, \tag{5.3}$$

where $N$ corresponds to the number of comparators and $E$ corresponds to the number of elements to be sorted. For the example of five elements shown above, only ten comparators are required. For the topological encoding, 26 muon candidates have to be sorted, so 325 comparators are needed. Note that the comparisons that can be derived by inversion are not counted. For example, $\overline{(p_{Ta} \geq p_{Tb})}$ is equivalent to a logic NOT of the first comparison in the row above ($p_{Ta} \geq p_{Tb}$).

The highest-$p_T$ value can be found by checking the comparison results in every row of the comparison matrix. The element with the highest-$p_T$ value is given by the row where every comparison result is true and, if there are no rows with all comparisons result true, the highest-$p_T$ candidate is the last element.

The output of the logical AND of the comparison results of each row flags the position of the candidate with the highest-$p_T$ value in a one-hot encoding scheme. Consequently, a one-hot multiplexor is implemented. This multiplexer consists of the output connected to a logical OR between all the inputs, and an enabling flag, as can be seen in Figure 5.3.

Only the $p_T$ value is used in the sorting process. However, the multiplexer outputs the full information from the selected candidate, consisting of the sector number, RoI, and the $p_T$ value.

After finding the highest-$p_T$ candidate, the second highest-$p_T$ candidate is derived by using a modified copy of the original matrix of comparisons shown in Table 5.1. The highest-$p_T$ candidate is ignored in the modified matrix by negating its comparison results.

Likewise, as the top candidate, the second highest-$p_T$ candidate is selected based

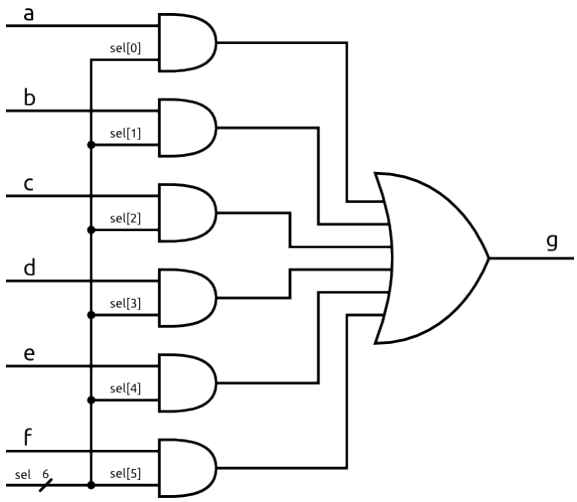



Figure 5.3: Logic diagram for a 6-input one-hot multiplexer

on the second matrix of comparisons. Again a second multiplexer selects the sector number, RoI and $p_T$ values and forwards it to the encoding unit.

The sorting algorithm works in a clock domain of 160 MHz ($T_{clk} = 6.25\,\text{ns}$). Initially, the logic path was pipelined in four stages in order to estimate the propagation delay of each step. Figure 5.4 shows a simplified timing diagram of the sorting unit pipelined in four stages.

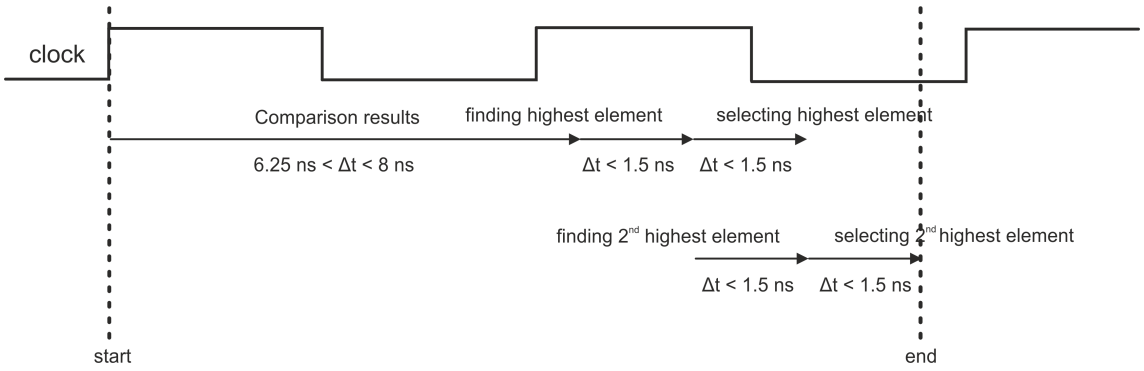



Figure 5.4: Simplified timing diagram of the sorting unit pipelined in four stages

The latency information for each stage is generated from the timing analysis performed by the static timing analysis tool[1].

As shown in Figure 5.4, the comparison process (first stage) accounts for the longest part of the propagation delay. The remaining operations, such as finding and selecting the $1^{st}$ and $2^{nd}$ highest-$p_T$ candidates, add only a small delay.

Since the first stage requires more than one 160 MHz clock cycle, it is necessary to increase the acceptable propagation delay for this stage or break this stage into two new stages using register pipelining.

[1]Altera TimeQuest application. TimeQuest is part of the Quartus II software and produces timing report of the firmware implementation for a selected Altera device.

Due to the complexity of employing manual pipelining technique, the acceptable propagation delay for the first stage of the sorting unit was increased to two clock cycles, which was also enough to include the logic from the other three stages into the same path. Therefore, the full sorting process is performed in a path with propagation delay of 12.5 ns. When compared to the sequential sorting approach, the latency achieved with the parallel processing is 13 times lower. The increase of the acceptable propagation delay is implemented by setting a timing exception in the synthesis tool known as a multi-cycle path constraint. The multi-cycle path constraint indicates to the synthesizer that the acceptable propagation delay between two registers can be increased to $n \times T_{clk}$, where n indicates the number of clock cycles set in the timing constraint and $T_{clk}$ indicates the period of the clock.

In addition to the timing exception implemented, the design also has to ensure that the data from the sorting output register will be read only two clock cycles after the input data arrives. This is implemented by controlling the clock enable port of the registers in the data path.

A very simple protocol implements the data flow control using a *source_valid* signal at the output of each unit. Every unit indicates the existence of new data in the output, by asserting the signal *source_valid* for one clock cycle. A second unit expects a *sink_valid* signal before latching and processing the input data.

Figure 5.5 shows the data flow control connections between the sector data input, the candidate veto unit and the sorting unit.

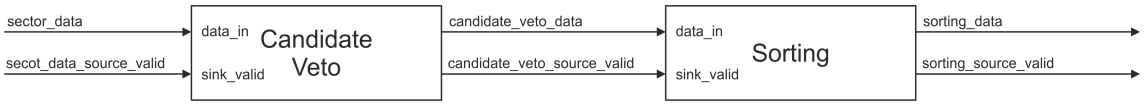



Figure 5.5: Block diagram of the data flow control signals of the candidate veto and sorting units

Figure 5.6 shows the timing diagram of the data flow control signals for the candidate veto and sorting units.

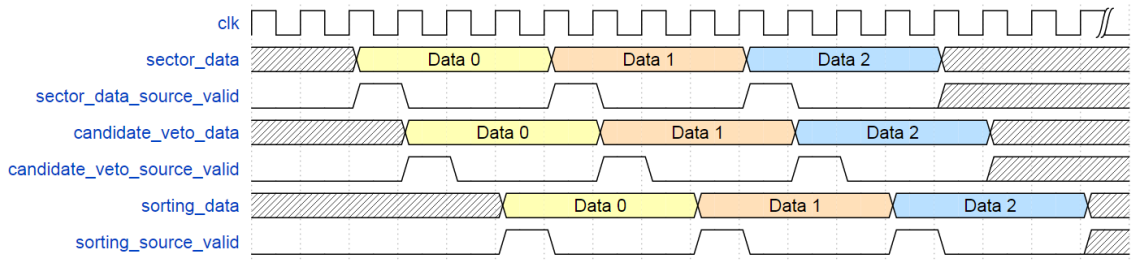



Figure 5.6: Timing diagram of the data flow control signals of the candidate veto and sorting units

The *sector_data* signal represents the sector data from the 13 trigger sectors and the *sector_data_source_valid* signal is asserted for one 160 MHz clock cycle

whenever new sector data are available. Then the candidate_veto unit delivers candidate information after one 160 MHz clock cycle, and the *candidate_veto_source_valid* signal is used to indicate when new data are available. Finally, the sorting algorithm receives the input data and the source_valid flag and delivers the highest and second highest-$p_T$ candidates after two 160 MHz clock cycles. Then, the *sorting_source_valid* signal is asserted.

The use of control flags being propagated through the units (instead of being locally generated) simplifies the control of the data flow. Each unit carries the information of its delay and it does not need to know the delay of other units to operate properly. For instance, if one unit needs to be removed from or included into the circuit, no changes are required on the remaining units.

### 5.1.3 Encoding

The eight bits of topological information were allocated based on a compromise between the available bandwidth, derived from the feasibility test results shown in Chapter 4, and the best trigger efficiency from physics simulations [86]. The pseudorapidity $\eta$, the polar angle $\phi$ and the transverse momentum $p_T$ are encoded according to Table 5.2.

Table 5.2: The MIOCT trigger outputs data format

| Bit position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Trigger output | $\eta$ | | | $\phi$ | | | $p_T$ | |

The topological information of the two highest-$p_T$ muon candidates is encoded in $\eta$ and $\phi$ with an average bin size $\Delta\eta \times \Delta\phi \approx 0.3 \times 0.1$.

#### 5.1.3.1 Encoding of the geometric coordinate $\eta$

Three bits are used for encoding $\eta$, seven out of eight possible codes are available since one code ("111") is reserved to indicate the absence of any candidate. The mapping between the $\eta$ codes and the detector granularity is shown in Figure 5.7.

This plot was generated from information about the geometry and size of each RoI of the muon trigger detectors, using an object-oriented data analysis framework (ROOT [87, 88]). The outline of each RoI was plotted, and its color indicates the proposed $\eta$ code that the MUCTPI system will send to the L1Topo processor whenever the given RoI appears in one of the two muon candidates.

The encoder assigns six codes to the barrel and end-cap regions, resulting in a bin size $\Delta\eta \approx 0.3$. In the forward region, a greater bin size of $\Delta\eta = 0.53$ is used. The topological code assignment can still be changed by generating a new file with the

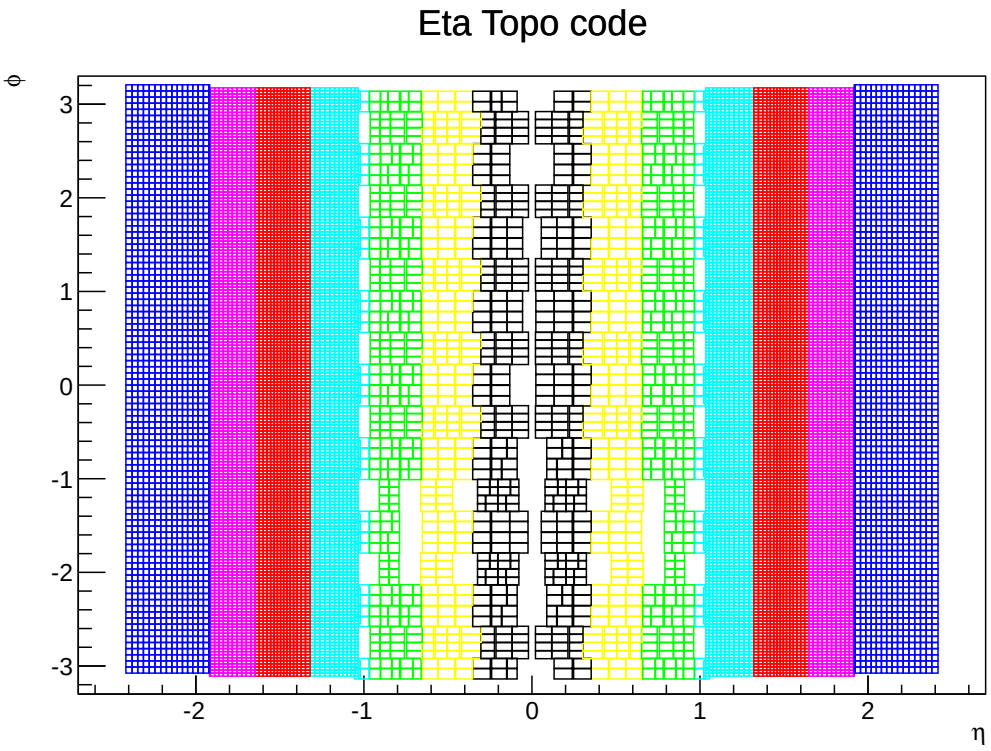



Figure 5.7: Sector and RoI Encoded in $\eta$

new encoding scheme and loading its content into programmable LUTs implemented in the MIOCT firmware.

#### 5.1.3.2 Encoding of the geometric coordinate $\phi$

Three bits are used to encode the polar angle $\phi$. The eight codes are uniformly distributed within the three regions (barrel, end-cap and forward) resulting in a unique bin size $\Delta\phi < 0.1$. This is shown in Figure 5.8 where the color of each RoI indicates the proposed $\phi$ code that the MUCTPI system will send to the L1Topo processor whenever the given RoI appears in the one of the muon candidates.

#### 5.1.3.3 Encoding of the transverse momentum $p_T$

Two bits are used to encode the $p_T$ threshold, three of four codes are used to map the original six $p_T$ thresholds onto three programmable $p_T$ threshold values ($p_{T_I}$, $p_{T_{II}}$, $p_{T_{III}}$) for each candidate. For the second candidate, the remaining code is reserved to indicate the existence of more than two candidates, while the $p_T$ bits of the first candidate still carry only information about the highest $p_{\mathrm{T}}$ threshold. The remaining code of the $p_T$ bits of the first candidate is not used to map a fourth threshold value in order to allow L1topo to treat the first and second candidate transparently. Table 5.3 shows the transverse momentum $p_T$ encoding scheme.

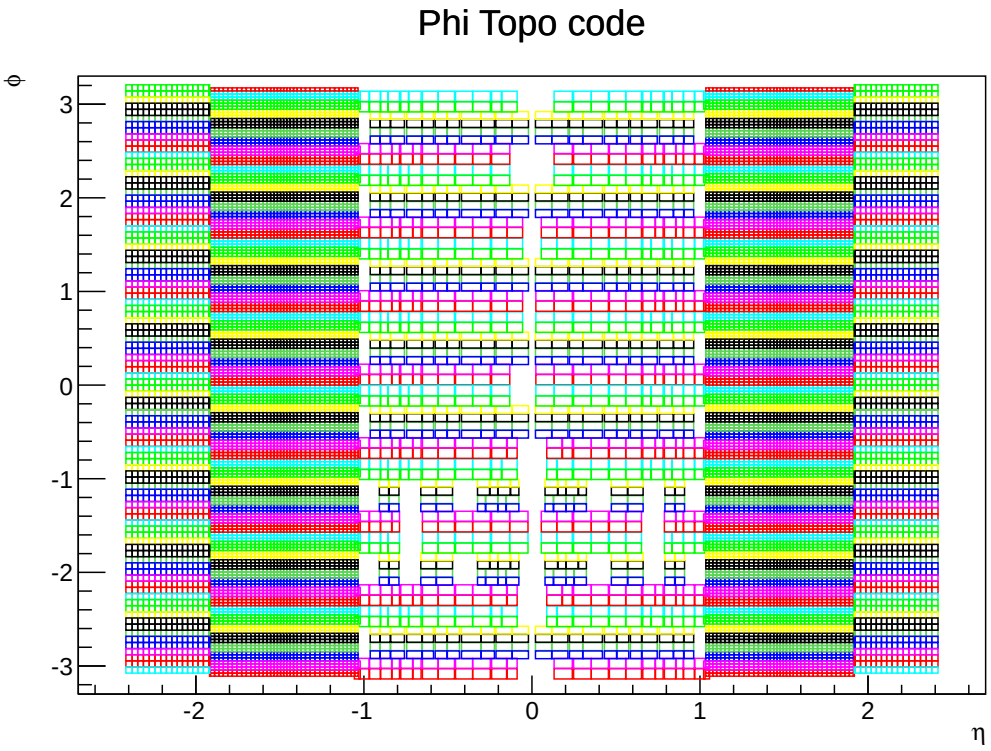



Figure 5.8: Sector and RoI Encoded in $\phi$

Table 5.3: Encoding of the transverse momentum $p_T$

| | **First candidate** | **Second candidate** |
|---|---|---|
| **00** | $p_{T_I}$ | $p_{T_I}$ |
| **01** | $p_{T_{II}}$ | $p_{T_{II}}$ |
| **10** | $p_{T_{III}}$ | $p_{T_{III}}$ |
| **11** | not used | more than two candidates |

#### 5.1.3.4 No-candidate code assignment

The code indicating the absence of a candidate must start with the 3-bit reserved code in the $\eta$ encoding. However, the five remaining bits can be assigned to any desired value. This programmable word has been agreed upon to be 0xE8 since it offers short and long time intervals between transitions. The short and long time intervals can be seen in the frequency domain as high and low-frequency components. This allows to have a more precise phase alignment because it assists the MuCTPiToTopo interface to spot data dependent jitter.

#### 5.1.3.5 Encoding summary

Additional position information is defined by the cable connections from the MUCTPI system to the MuCTPiToTopo interface. For instance, the octant number (from 1 to 16) and consequently the detector side (A or C) is used to define a extended $\eta, \phi$ coordinate. Each MIOCT can encode $7 \times 8 = 56$ geometric locations explicitly extracted from the MUCTPI topology encoding data format. Taking into account 16 octants, the MUCTPI system can encode and send to L1Topo $16 \times 56 = 896$ geometric locations of muon candidates.

### 5.1.4 Serializer

In the last stage of the topology unit, the 8-bit word from the encoder unit is serialized at 320 Mbps and transmitted using DDR outputs. A separated serializer for each output is implemented using a shift register that first outputs the Most Significant Bit (MSB). The two electrical trigger outputs carry the information from the $1^{st}$ and $2^{nd}$ highest-$p_T$ candidates respectively.

Besides, the serializer unit can also generate a fixed 16-bit training pattern to be used for phase and word alignment to MuCTPIToTopo. The pattern is programmable via VME and is set during the system configuration.

For test purposes, the serialization unit also features a PRBS generator, which is the same one described in Chapter 4.

A multiplexor is used to select one of the following outputs:

1. PRBS data
2. 16-bit fixed pattern
3. Topology encoded data

## 5.2 Firmware verification

The firmware upgrade of the MIOCT module was verified against errors in two stages. Firstly, VHSIC Hardware Description Language (VHDL) functional simulation of the MIOCT firmware was performed and, then, the actual hardware was tested using the test memory to verify the generated topological information.

### 5.2.1 VHDL functional simulation

The VHDL functional simulation test bench consists of a VHDL behavioural reference model and a VHDL code of the firmware. Figure 5.9 shows the connection

between the reference model and the VHDL firmware code. The verification uses the Mentor Graphics ModelSim simulator.

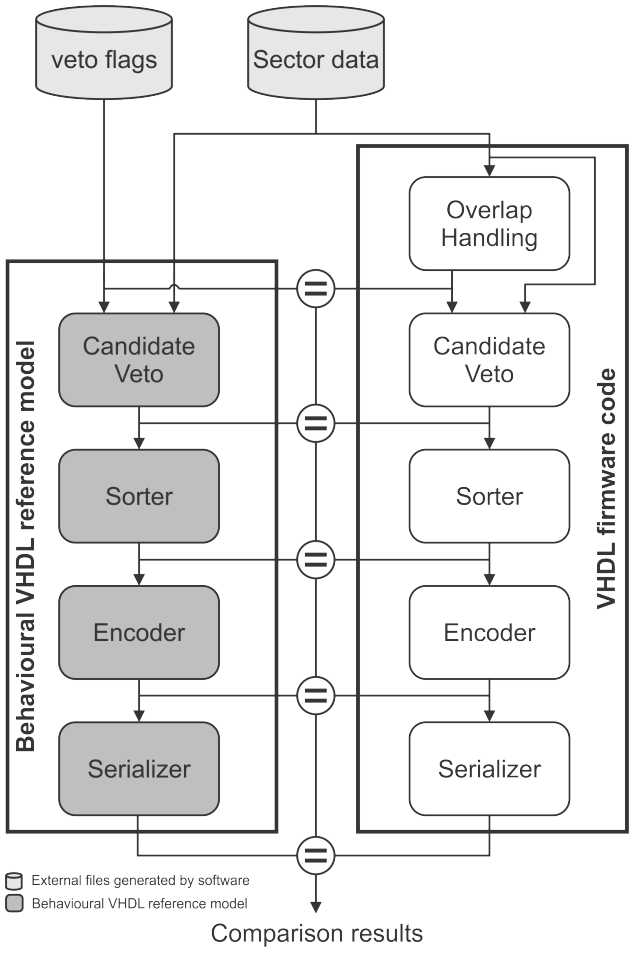



Figure 5.9: Functional simulation flow

The results from the VHDL firmware code simulation are compared to results from the reference model. The VHDL firmware code represents the functionality of the overlap handling and topology encoder units. The reference model implements the functionality of the Candidate Veto, Sorter, Encoder and Serializer units and takes the sector data and veto flags from external files. Four sector data pattern and veto flags files based on candidates with overlap or without overlap, and candidates based on a random distribution or based on a multiplicity counter were generated. Each of these files contains sector data equivalent to 13 orbits[1], resulting in $4 \times 13 \times 3564 \approx 185$ k test patterns.

The VHDL firmware code is verified by comparing the output of each unit to the output from the corresponding unit in the reference model. In the case a mismatch is detected, a complete report is generated. This simplifies debugging because it allows to determine easily which of the units in the VHDL simulation model generated the

[1]One orbit corresponds to one LHC turn, equivalently to 3564 bunch crossings.

error.

The VHDL firmware code was verified through functional simulation using sector data information from ≈ 185 k bunches without errors. However, the functional simulation does not check if the firmware is properly implemented in the hardware. Therefore, in a next step, in-system verification was used to check the firmware loaded in the FPGA of the MIOCT module.

### 5.2.2 In-system design verification

The in-system design verification checks the behaviour of the MIOCT hardware in operation, comparing results from the hardware using a software-based reference. The results from the hardware are produced by writing random generated sector data to a test memory, which supplies sector data to the overlap handling unit and reads back the generated veto flags and topology information. Figure 5.10 shows a block diagram of the in-system verification.

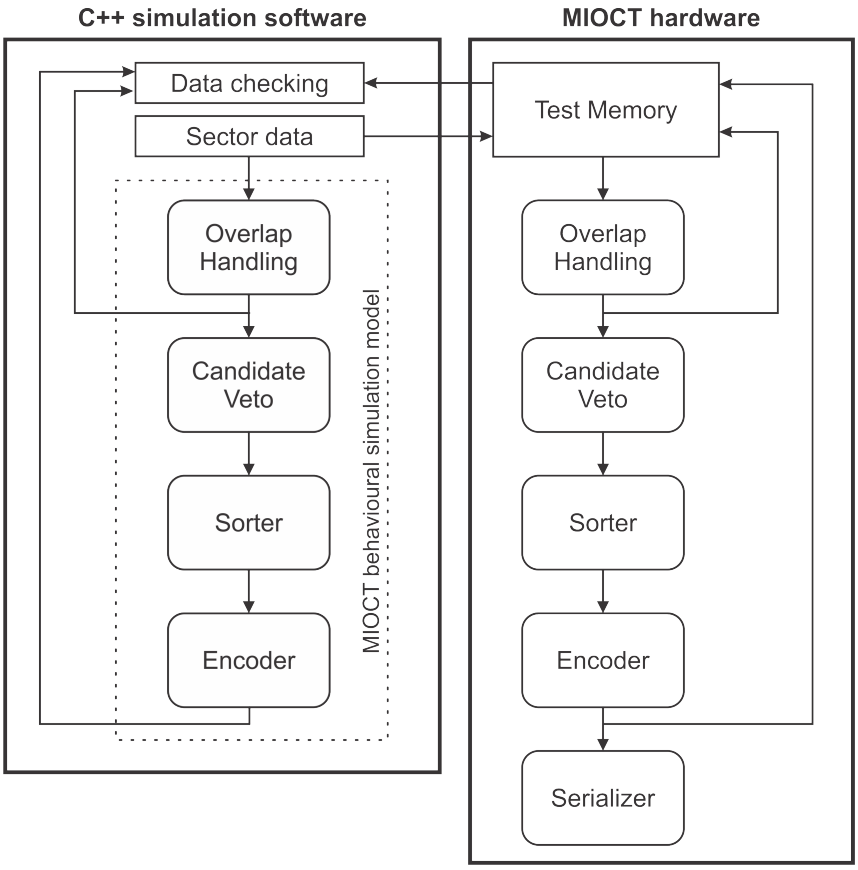



Figure 5.10: In-system Verification flow only results from the overlap handling and the topology encoder are checked)

First, the C$^{++}$ simulation software generates random sector data[1] and writes

[1]The sector data used here have the same characteristics as the data used in the VHDL simulation.

them into the test memory module. Then, it configures the memory to inject sector data into the overlap handling unit input at the same time that the generated veto flags and the topological encoded data are written back to the memory. After that, the memory data are read out and compared to a software-based reference generated by the so-called MIOCT behavioural reference model.

The MIOCT behavioural reference model is implemented in the existing simulation software. In order to interface with the MIOCT test memory, the software uses a low-level software layer that provides an Application Programming Interface (API) to ease the control of registers in the hardware via the VME bus and a suite of test programs for systematic testing.

This test was performed using sector data from $\approx 1.4$ billions of bunches without errors. However, the in-system verification did not verify the serialization and data transmission, as can be seen in Figure 5.10. For this reason, the error rate test system was upgraded to receive the encoded data from the MUCTPI system and write it into a memory module for verification.

## 5.3 Upgrade of the error rate test system

The error rate test system, described in Chapter 4, was upgraded to receive the serialized data from the 32 MUCTPI electrical trigger outputs, align them, and write the information into a memory module in order to be read out by a computer for verification.

Figure 5.11 shows the block diagram of the upgraded test system. The word alignment and the memory interface units were added to the firmware described in Section 5.1. Initially, the input signal is phase-aligned using the PRBS data pattern and word-aligned using a know 8-bit value generated in each of the MIOCT modules.

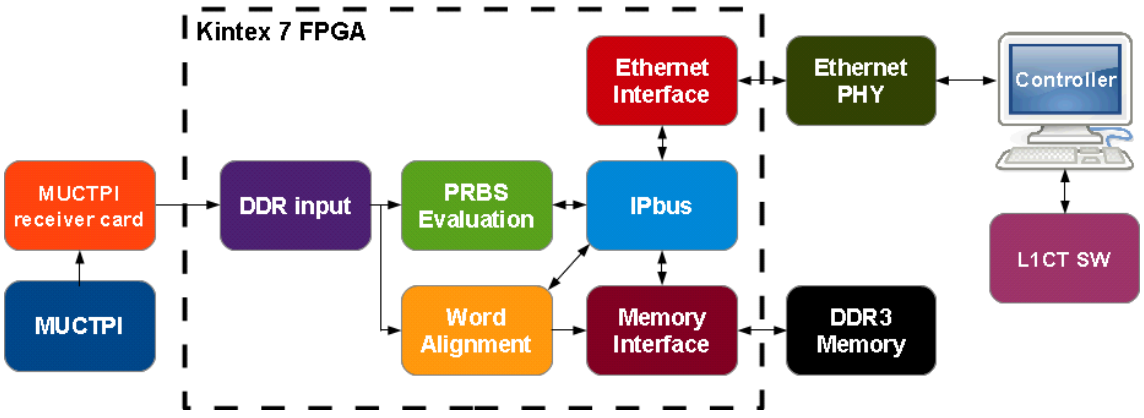



Figure 5.11: Block diagram of the upgraded error rate test system

For every 160 MHz clock cycle, the word alignment circuit compares the input data to the predefined 8-bit alignment reference value. When both match, the circuit

loads the bit position into a monitoring register.

The word alignment circuit aligns the data by latching the input at the position defined in a configuration register. The configuration register can be set externally by software or can be set internally by loading the value of the monitoring register. In case the timing of the system is unchanged, the values of the configuration register for each channels can be stored in a database and loaded using the IPbus control interface. The aligned data from all 32 MUCTPI channels are then sent to the memory interface shown in Figure 5.12.

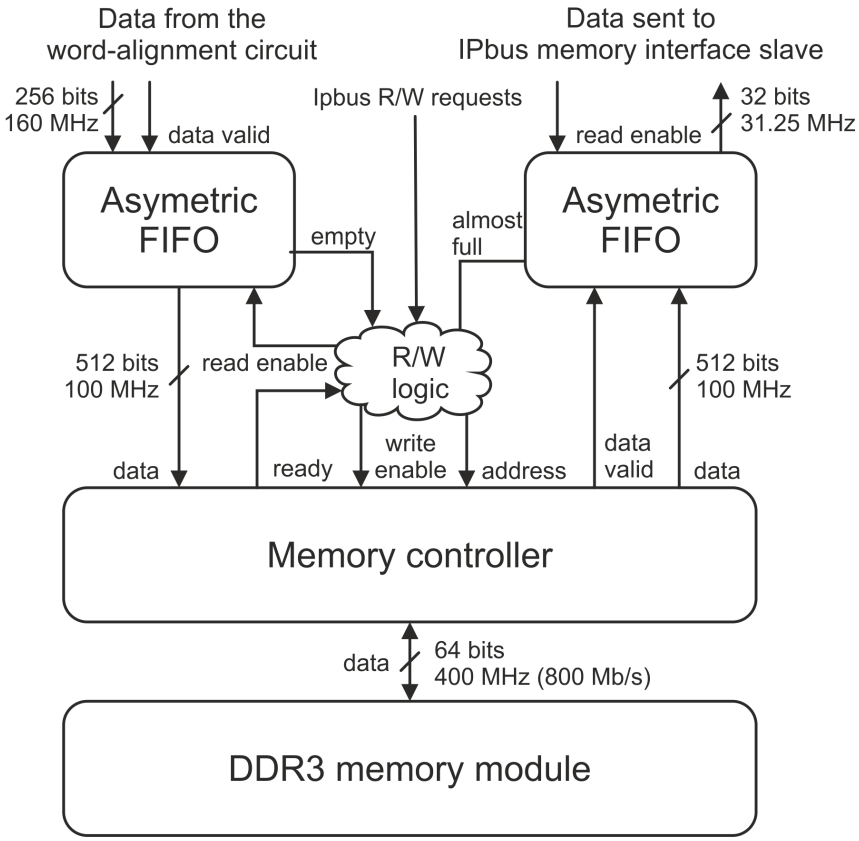



Figure 5.12: Memory interface block diagram

The input data are written into an asymmetric FIFO that receives 256 bits (32 $\times$ 8 bits) of data per bunch clock and sends 512-bit words to the memory controller. Similarly, a second asymmetric FIFO reads the data from the memory controller and sends them to the Ethernet interface. The readout FIFO has a 512-bit input and 32-bit output interfaces since the memory controller and the Ethernet interface operate with 512-bit and 32-bit ports respectively.

The two FIFOs are also used for clock domain crossing since the data input works in a clock domain of 160 MHz, the memory controller works at 100 MHz and the Ethernet interface operates at 31.25 MHz. The control logic makes sure that the data are read only after the writing process is finished.

The memory controller is connected to a 1GB DDR3 SODIMM memory module

operating at a bit-rate of 800 Mbps. This device can store data from 31.25M bunches.

## 5.4 Verification using the upgraded error rate test system

The verification of the serialization and transmission of the data through the MUCTPI electrical trigger outputs was performed by checking the data received by the test system after deserialization and alignment. This test checks the data received from all 16 MIOCT modules, and the test procedure is described below.

Firstly, all 32 MUCTPI trigger outputs are configured to send PRBS data and the optimal sampling point for each of the channels is measured as shown in Section 4.3.1. Secondly, all 32 MUCTPI trigger outputs are configured to send a known 8-bit value to perform the word alignment described in Section 5.3. Then, after the word alignment has been found, the bit position is stored on the computer and loaded to the test system configuration registers. Next, all 32 MUCTPI trigger outputs are configured to send a test pattern in a loop using the test memory described in Section 3.2.1.7.

Python scripts have been created to generate different data patterns based on randomly generated seeds for each of the 16 MIOCT modules. The maximum depth of the memories was used. Then, data equivalent to 36 LHC orbits were generated and written to text files. The same Python script loads these files into the respective MIOCT module, configures the memory to operate in a loop and triggers the loop concurrently in every module by asserting the test signal in the LTP card which is forwarded to the backplane by the MICTP module.

Then, these files are grouped together into a single file for comparison. The test system samples data equivalent to 360 orbits at each iteration. Since the beginning of the data transmission is not known, the offset between the reference and sampled data for each iteration is estimated by comparing the received data to one hundred patterns of the reference data. Next, the data from the 360 orbits sampled in the test system are compared to the reference data (36 orbits) replicated ten times.

This process was repeated for three days until the test system checked data from $1 \times 10^{10}$ bunches (equivalent to $\approx$ 2.8 M orbits) without any errors. This result demonstrates that the topological information can be transmitted and received reliably.

## 5.5 Summary

In this chapter the changes to the MUCTPI firmware enabling the transmission of muon topological information were presented. The firmware of the MIOCT module was upgraded in order to extract, encode and send topological information to the L1Topo processor. Every MIOCT card sends data with a bit rate of 320 Mbps per output. Thus, the upgraded MUCTPI system sends muon topological trigger information at an aggregated rate of 10.24 Gbps.

The MIOCT firmware upgrade was checked by performing VHDL functional simulation and in-system verification. The functional simulation checked the firmware behaviour for 185 k bunches while the in-system verification checked sector data equivalent to 1.4 billions of bunches. It demonstrated the reliability of the upgraded MIOCT firmware operation, up to the encoding stage, where the data were monitored. However, as the serialization and data transmission were not checked by the last test, the error rate test system was upgraded to receive serial data from the MUCTPI system, align it, format it, and write it into a DDR3 memory module for verification.

In the end, all 16 MIOCT modules were tested together using the test system to check the received data after the MIOCT modules had been configured to send a test pattern.

For the last test, data from $1 \times 10^{10}$ bunches were received and checked by the test system without any errors. These results demonstrate that the error rate test system can reliably receive the topological information sent from all 32 MUCTPI electrical trigger outputs.

# Chapter 6

# System integration tests

This chapter describes the integration tests of the MUCTPI system with the MuCTPiToTopo interface and the L1Topo processor.

The interface between the MUCTPI system and the MuCTPiToTopo interface was verified by configuring the MUCTPI system for sending a known data pattern and sampling the received data at the MuCTPiToTopo interface.

Then, the L1Topo processor was connected to the MuCTPiToTopo interface and integration tests were performed with the three systems by checking the received data at the L1Topo processor.

Hardware tests using the test system as described in Chapter 4 were run on the MUCTPI system installed in USA15 that is the ATLAS experiment counting room.

## 6.1 MuCTPiToTopo Interface

The MuCTPiToTopo interface was designed to connect the MUCTPI system to the L1Topo processor, converting the electrical signals from the trigger outputs of the MUCTPI system to optical signals for the L1Topo processor.

The components of the interface are an FPGA development kit[1] and two FMC mezzanine cards. The MUCTPI receiver mezzanine card described in Chapter 4 receives the trigger signals and the LHC clock from the MUCTPI system while the second mezzanine card transmits the data to the L1Topo processor via optical links. Figure 6.1 [71] shows the MuCTPiToTopo block diagram.

The serial data streams received from the MUCTPI are aligned using programmable on-chip delay lines and deserializers that can be controlled in order to perform phase and word alignment of the input data using an 8-bit fixed pattern sent by the MUCTPI as a reference. As the input to output phase skew of the jitter-cleaner device of the receiver mezzanine card is not controlled after the

[1] Xilinx VC707

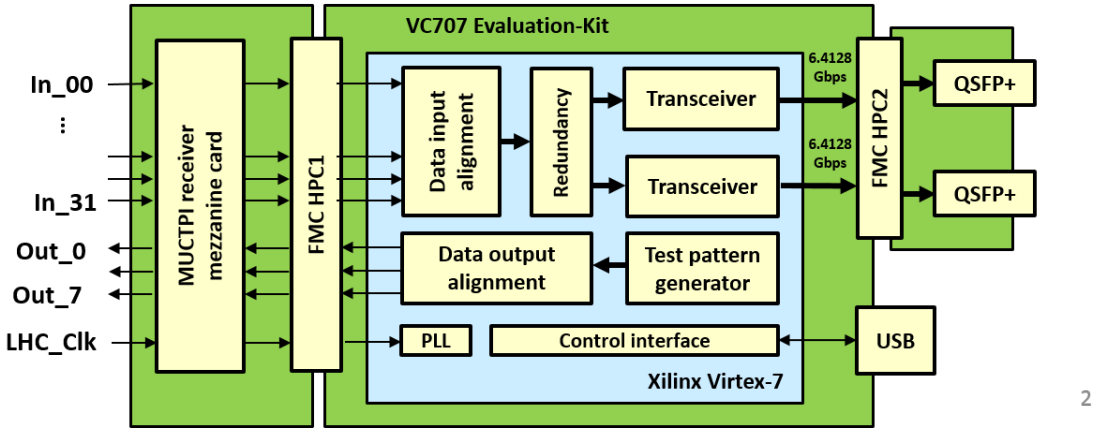



Figure 6.1: MuCTPiToTopo block diagram

internal calibration and can assume any value according to the datasheet, the phase and word-alignment procedure is repeated every time the system is configured.

A check value is attached to the aligned data allowing the L1Topo to run an error-detecting code to detect data corruption. The data is then transmitted to L1Topo via optical links using on-chip Gigabit transceivers. The interface also features a test pattern generator that can be used to check the MUCTPI receiver mezzanine card in loop-back.

The system is controlled using the Universal Serial Bus (USB) interface, which can also be used to monitor the alignment process and read out the data from on-chip memories. The sampled data from the MUCTPI can be written to these memories from where they can be read out for verification.

The time between data entering and leaving the MuCTPiToTopo interface has been estimated as 75 ns. In operation, the cable length from the MUCTPI system, and fiber length to the L1Topo processor will add additional signal propagation time. Assuming 8 ns coaxial cables, and 1 m optical fiber cables, a total of 15 ns propagation time is estimated, resulting in a final latency lower than the 4 bunch crossings allocated for sending the information from the MUCTPI system to the L1Topo processor.

## 6.2 L1Topo Processor

The L1Topo processor system consists of a single Advanced Telecommunications Computing Architecture (ATCA) [78] crate equipped with two processor modules. Each processor module features two large Virtex-7 FPGAs that receives an identical copy of L1Calo and L1Muon data and runs a specific set of algorithms. Algorithms use lists of jets, electron/gamma, tau and muons to perform geometrical cuts. The latency has been estimated to be about 200 ns from receiving data and producing

the algorithms response. Further information about the L1Topo processor can be found in [43, 44].

Figure 6.2 shows a photo of the L1Topo module prototype.

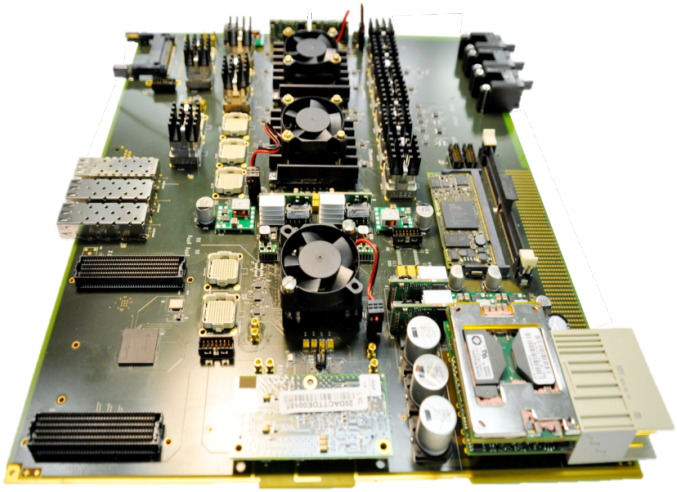


Figure 6.2: L1Topo module prototype.

## 6.3 Integration tests

The MUCTPI system was put to integration tests with the MuCTPiToTopo interface and L1Topo, in order to verify the interface between the systems. The test began with the configuration of the MUCTPI system to send a known pattern. The data received in both systems is then written to on-chip memories, from where they can be read out for verification. The data received by the MuCTPiToTopo interface were read out via USB using the control interface implemented in the firmware. The data received by the L1Topo processor were read out via JTAG[1] [89] using the Xilinx Integrated Logic Analyzer (ILA) IP core and Vivado Logic Analyzer software [90]. Figure 6.3 shows the three modules being tested during the integration tests at the CTP laboratory.

The connectivity test between the MUCTPI system and the MuCTPiToTopo checked data from 2.6 M bunches in an overnight test. Then, the L1Topo was included in the chain for a second test, which checked $\approx$ 258 k bunches. Both of the tests ran without errors.

The amount of data checked was limited by the low-speed interface to read the data from the MuCTPiToTopo interface and L1Topo processor. With these results it is not possible to demonstrate with significant confidence level that the data transfer is free of errors for a long interval, such as the duration of a data taking

[1] Joint Test Action Group (JTAG) is a debugging interface defined in the Standard Test Access Port and Boundary-Scan Architecture

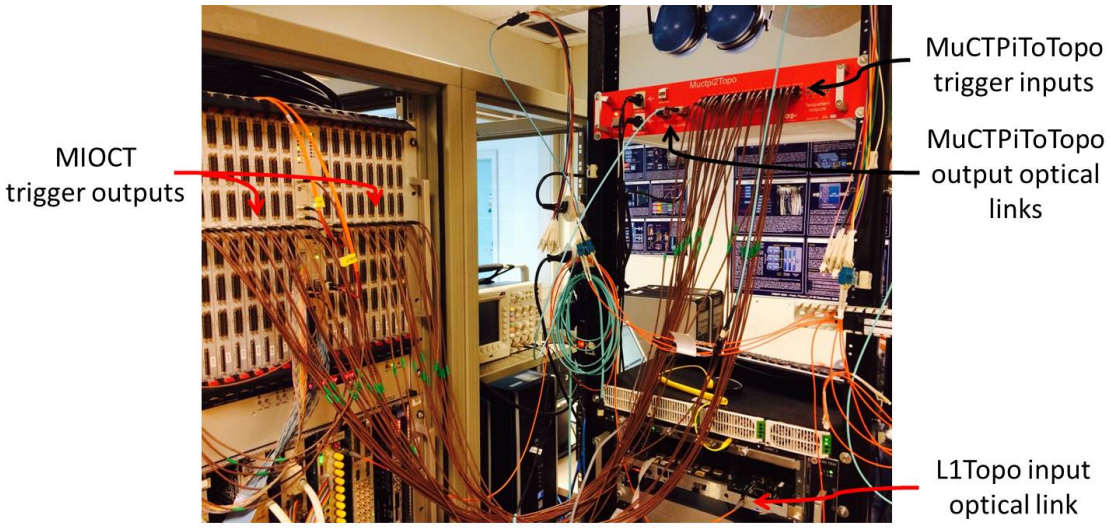



Figure 6.3: Photo of the MUCTPI integration tests with MuCTPiToTopo interface and L1Topo processor

run. Therefore commissioning tests will be performed to check the reliability of the data transmission from the MUCTPI to L1Topo.

## 6.4 MUCTPI hardware tests at the counting room of the ATLAS experiment

The MUCTPI system installed in the counting room of the ATLAS experiment was put to hardware tests using the error rate test system, described in Chapter 4. Figure 6.4 shows the CTP and MUCTPI system in USA15. The black cables connect the muon trigger sector logic modules to the MUCTPI system, and the brown cables connect the MUCTPI electrical trigger outputs to the error rate test described in Section 4.2.

The error rate test system was used to run a phase scan of the MUCTPI electrical trigger outputs. The MUCTPI was configured to send PRBS data at the trigger outputs at a bit rate of 320 Mbps, and a test of 20 minutes was run. Figure 6.5 shows the phase scan histogram of the results. The bins in green indicate the transition-free region whereas the ones in red indicate the metastable region.

A different phase offset was observed when comparing to the phase scan results of the MUCTPI system at the CTP laboratory shown in Figure 4.18. The different phase offset is found due to the different timing of the system in USA15. However, the metastable region also corresponds to 25% of the bit period window, the same value as in the lab. The test result demonstrates that the MUCTPI electrical trigger outputs of the system in USA15 can reliably send data through the electrical trigger outputs and that the MUCTPI system in USA15 is ready for commissioning tests

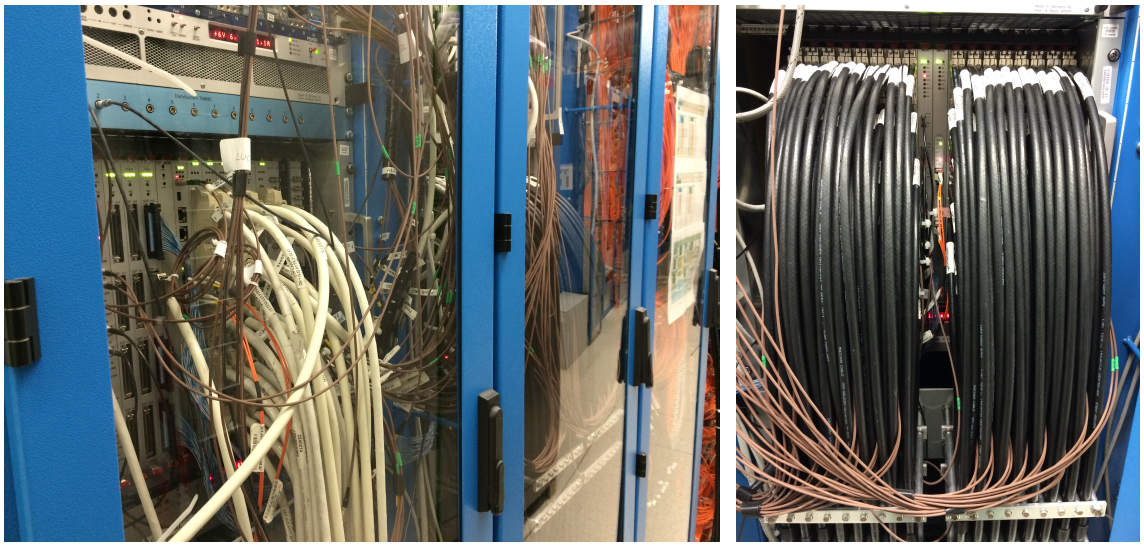


Figure 6.4: The photo on the left shows the CTP and MUCTPI systems in USA15 and the photo on the right shows the MUCTPI system in more detail

with MuCTPiToTopo interface and L1Topo processor.

## 6.5 Summary

This chapter described the MuCTPiToTopo interface, the L1Topo processor, and the integration tests with the MUCTPI system. First the connectivity between the MUCTPI system and MuCTPiToTopo interface was verified by comparing the known pattern sent by the MUCTPI to the received data in the MuCTPiToTopo interface. In the second test, the connectivity to the L1Topo processor was checked by performing a similar test. Data from approximately 2.6 M and 258 k bunches were read out from the MuCTPiToTopo interface and L1Topo processor respectively without any errors.

Furthermore, the test system described in Chapter 4 was moved to the counting room of the ATLAS experiment and a phase scan was performed on the MUCTPI trigger outputs. The phase scan results show that the MUCTPI system in USA15 can reliably send data through the electrical trigger outputs.

This shows that the MUCTPI system is ready for commissioning. The commissioning tests will start once MuCTPiToTopo and L1Topo are in USA15 as well.

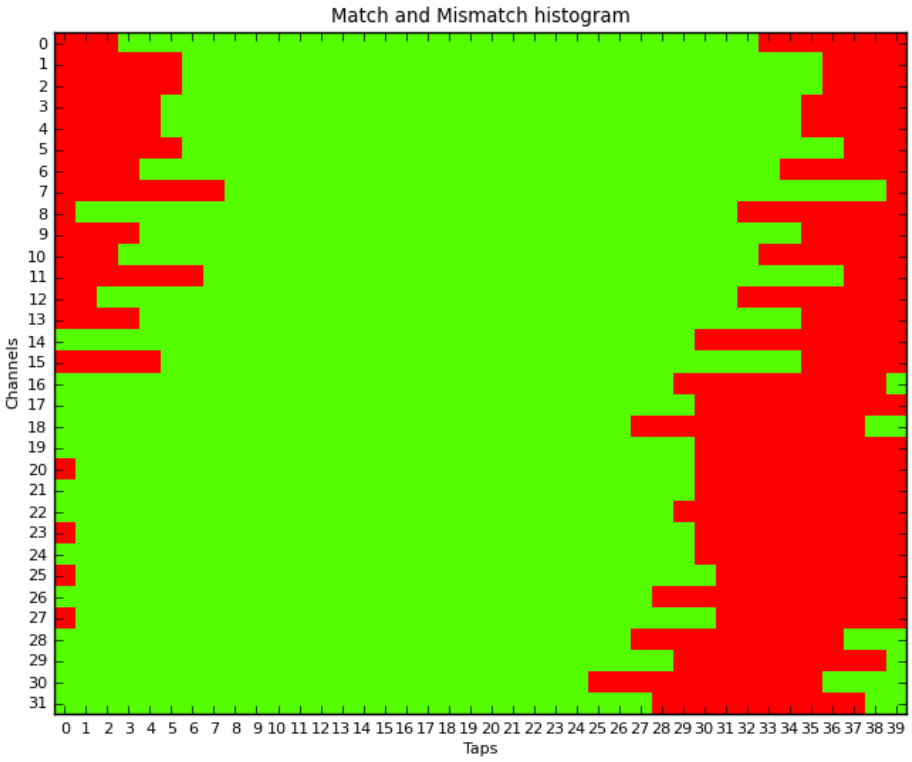



Figure 6.5: Phase scan of the received data from the MUCTPI installed in USA15

# Chapter 7

# Conclusions

This work discussed the upgrade of the first-level trigger system of ATLAS in order to improve its efficiency for specific physics channels by performing cuts on the angular distance or other topological information of the trigger objects. In particular, the role of the MUCTPI and its firmware upgrade in the improvement were explained.

The MUCTPI was upgraded to send topological information to the L1Topo processor. The existing MUCTPI system features electrical trigger outputs, initially intended to be used for test purposes. These outputs are reused to send muon topological information to the L1Topo processor. Since the electrical trigger outputs had never been tested operating at higher rates, technical feasibility studies were conducted to determine the maximum operation rate that data can be reliably transmitted. The MIOCT firmware was modified to provide PRBS data to the outputs and an oscilloscope was used to check the integrity of the transmitted signal at 80 Mbps, 160 Mbps, 240 Mbps and 320 Mbps.

Results from the tests showed a reasonable open eye-diagram for the electrical trigger outputs operating at a bit rate of up to 320 Mbps. After these results, more systematic tests were performed to ensure the reliability of data transmission using the MUCTPI electrical trigger outputs. For this reason, a test system, based on an FPGA evaluation board, was developed to carry out a phase scan of the received data and measure its bit error rate.

The MUCTPI system went through long-term tests which investigated several aspects of data transmission, such as the width of the metastable region due to jitter and drifting of the clock phase and the error probability of the received data. Phase scan results from the test system showed that 75% of the bit period window is free of transitions. Thus, an optimal sampling point can be selected, allowing the MuCTPiToTopo interface to receive data with a comfortable timing margin. The probability of error in the data transmission and reception is shown to be lower than $1 \times 10^{-15}$ with 98.80% of certainty at the optimal sampling point. Therefore,

it is estimated with a confidence level of 98.80% that not even a single-bit error is expected to occur in the data transmission from all 32 MUCTPI trigger outputs during an entire data taking run.

The MUCTPI firmware was then modified to provide muon topological information to L1Topo through the electrical trigger outputs. The following functionalities were added to the firmware: sorting the candidates according to their transverse momentum $p_T$, encoding the two highest-$p_T$ candidates in $\eta$ and $\phi$ coordinates, and serializing of the data at 320 Mbps. These firmware changes were systematically verified using VHDL functional simulation and in-system hardware verification.

Furthermore, the test system was upgraded to receive and align the serial data from the MUCTPI system and write it into a memory module. Next, the MUCTPI system was configured to send a recognizable pattern through the electrical trigger outputs and data from $1 \times 10^{10}$ bunches were received and checked by the test system without any errors. This test shows that the MUCTPI system was ready for integration tests.

Subsequently, integration tests were performed with MuCTPiToTopo interface and L1Topo processor. The MUCTPI system was configured to send the known pattern and data from approximately 2.6 M and 258 k bunches were read out from the MuCTPiToTopo interface and the L1Topo processor on-chip memories respectively. These data were compared to the pattern written in the MUCTPI test memory, and no errors were found.

In addition, a test of the electrical trigger outputs of the MUCTPI system in the counting room of the ATLAS experiment was performed using the test system. The results demonstrated that the system installed is ready for commissioning tests.

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# Appendix A

# ATLAS coordinate system

The ATLAS experiment uses a right-handed coordinate system with the origin in the centre of the ATLAS detector, where is also located the nominal interaction point. The z-axis is superimposed upon the beam line in anti-clockwise direction, the x-axis is pointing in the direction of the centre of the LHC ring and the y-axis is perpendicular to the x-axis and z-axis and points upwards. Figure A.1 [91] shows the ATLAS coordinate system.

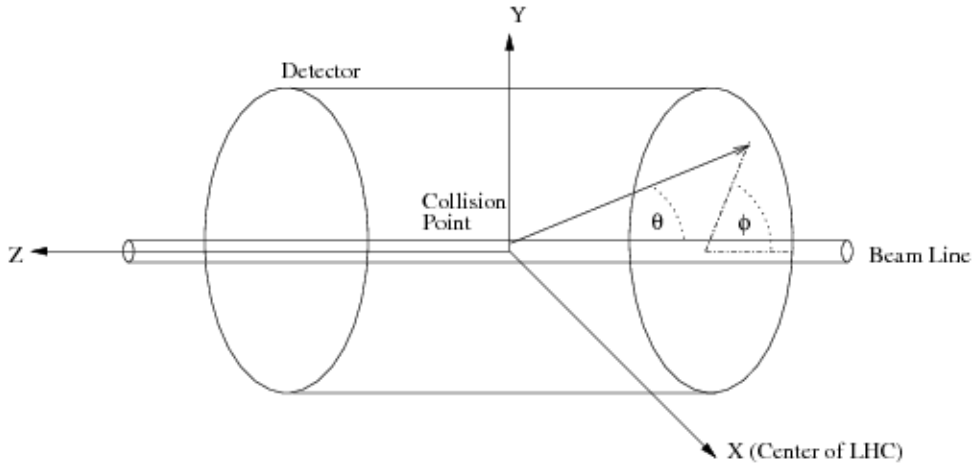



Figure A.1: ATLAS coordinate system

The symmetry of the detector makes cylindrical coordinates useful. The radial coordinate in the XY-plane is denoted by r. The azimuthal angle $\phi$ is the angle in the XY-plane originating from the x-axis and it increases clockwise when looking down the positive z-direction. It can also be expressed in terms of x and y, as shown in Equation (A.1).

$$\phi = arctan\frac{x}{y} \tag{A.1}$$

The polar angle $\theta$ is defined as the angle with the positive z-axis. Instead of polar angle $\theta$, the pseudo-rapidity $\eta$ is often used, as the particle multiplicity is

approximately constant as function of $\eta$. The pseudo-rapidity is defined in Equation (A.2).

$$\eta = -log\left(\tan\frac{\theta}{2}\right) \tag{A.2}$$

Figure A.2 shows a histogram of $\eta$ in terms of z and r. The track geometry can be expressed as a function of the angles $\eta$ and $\phi$. The $\eta$-$\phi$ space can be visualized by rotating the RZ-plane shown in Figure A.2 around the z-axis in the interval $[0, 2\pi]$. The $\eta$,$\phi$ coordinates identify the angle from the particle track to the interaction point, rather than the geometrical point where the track was detected.

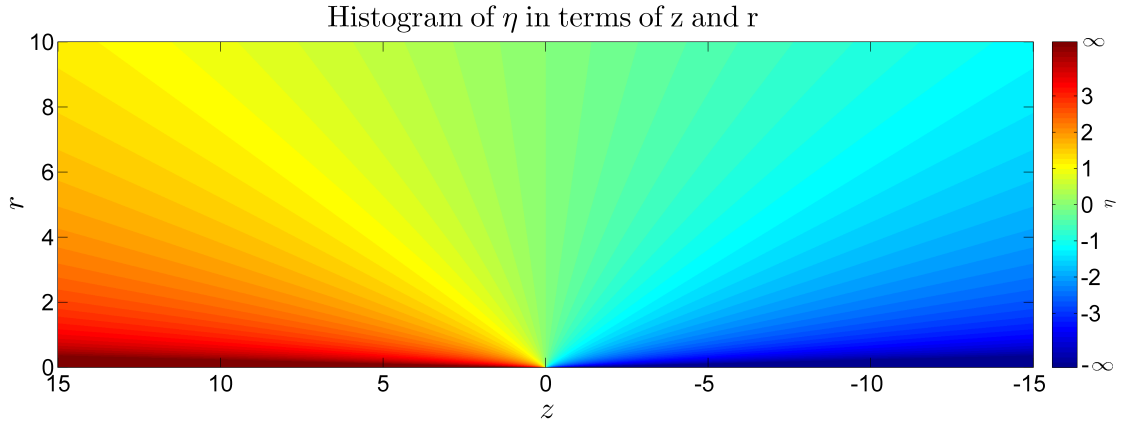



Figure A.2: Histogram of $\eta$ in terms of z and r

This histogram was generated using Mathworks MATLAB [92]. The value of $\eta$ in terms of z and r is described in Equation (A.3).

$$\eta = \begin{cases} -\log\left[\tan\left(\frac{1}{2}\arctan\frac{r}{|z|}\right)\right] & \text{if } z \geq 0 \\ -\log\left\{\tan\left[\frac{1}{2}\left(\pi - \arctan\frac{r}{|z|}\right)\right]\right\} & \text{if } z < 0 \end{cases} \tag{A.3}$$

Tracks detected in regions with low values of $|\eta|$ comes from inelastic collisions, which produces new particles. For this reason, it is often used higher resolution for $|\eta| < 3$.

# Appendix B

# Scientific production

1. M. Silva Oliveira, S. Artz, B. Bauss, H. Boterenbrood, V. Buescher, A.S. Cerqueira, R. Degele, S. Dhaliwal, N. Ellis, P. Farthouat, G. Galster, M. Ghibaudi, J. Glatzer, S. Haas, O. Igonkina, K. Jakobi, P. Jansweijer, C. Kahra, A. Kaluza, M. Kaneda, A. Marzin, C. Ohm, T. Pauly, R. Pottgen, A. Reiss, U. Schaefer, J. Schaeffer, J.D. Schipper, K. Schmieden, F. Schreuder, E. Simioni, M. Simon, R. Spiwoks, J. Stelzer, S. Tapprogge, J. Vermeulen, A. Vogel, M. Zinser. *The ATLAS Muon Topological Trigger Information for Run 2 of the LHC*, Journal of Instrumentation, 2015, Volume 10 - C02027. Part of Topical Workshop On Electronics For Particle Physics (TWEPP), 2014, Aix-an-Provence, France.

   **Abstract:** For Run 2 of the LHC, the ATLAS Level-1 trigger system will include topological information on trigger objects in order to cope with the increased trigger rates. The existing Muon-to-Central-Trigger-Processor interface (MUCTPI) has been modified in order to provide coarse-grained topological information on muon candidates. A MUCTPI- to-Level-1-Topological-Processor interface (MuCTPiToTopo) has been developed to receive the electrical information and to send it optically to the Level-1 Topological Processor (L1TOPO). This poster will describe the different modules mentioned above and present results of functionality and connection tests performed.

2. H. Bertelsen, A. Boisen, M. Dam, G. Galster, M. Ghibaudi, J. Glatzer, B. Gorini, S. Haas, M. Kaneda, A. Marzin, C. Ohm, M. Silva Oliveira, T. Pauly, R. Poettgen, K. Schmieden, R. Spiwoks, J. Stelzer, S. Xella. *Upgrade of the ATLAS Central Trigger for LHC Run 2*, Journal of Instrumentation, 2015, Volume 10 - C02030.
   Part of Topical Workshop On Electronics For Particle Physics (TWEPP), 2014, Aix-an-Provence, France.

   **Abstract:** This talk focuses on the upgrades of the ATLAS central trigger processor (CTP) during the past year. The increased energy and luminosity of the LHC in the next run period requires a more selective trigger menu in order to satisfy the physics goals of ATLAS. Therefore the electronics of the CTP is upgraded and the commissioning status will be presented. In addition, the CTP software has been extended to allow the CTP to be partitioned into three freely configurable and separately operating sets of sub detectors, each independently using the almost full functionality of the hardware. This new approach and its operational advantages are discussed as well.

3. G. Anders, H. Bertelsen, A. Boisen,, T. Childers, M. Dam, N. Ellis, P. Farthouat, C. Gabaldon Ruiz, M. Ghibaudi, B. Gorini, S. Haas, M. Kaneda, C.Ohm, M. Silva Oliveira, T. Pauly, R. Pöttgen, K. Schmieden, R. Spiwoks, S. Xella. *Hardware, firmware and software developments for the upgrade of the ATLAS Level-1 Central Trigger Processor*, Journal of Instrumentation, 2014, Volume 9 - C01035.
   Part of Topical Workshop On Electronics For Particle Physics (TWEPP), 2013, Perugia, Italy.

   **Abstract:** The Central Trigger Processor (CTP) is the final stage of the ATLAS first level trigger system which reduces the collision rate of 40 MHz to a Level-1 event rate of 100 kHz. An upgrade of the CTP is currently underway to significantly increase the number of trigger inputs and trigger combinations, allowing additional flexibility for the trigger menu. We present the hardware and FPGA firmware of the newly designed core module (CTP-CORE+) module of the CTP, as well as results from a system used for early firmware and software prototyping based on commercial FPGA evaluation boards. First test result from the CTPCORE+ module will also be shown.