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The ATLAS Level-1 Muon Topological Trigger Information for Run 2 of the LHC

S. Artz,[a] **B. Bauss,**[a] **H. Boterenbrood,**[b] **V. Buescher,**[a] **A.S. Cerqueira,**[f] **R. Degele,**[a] **S. Dhaliwal,**[b] **N. Ellis,**[c] **P. Farthouat,**[c] **G. Galster,**[c,d] **M. Ghibaudi,**[c,e] **J. Glatzer,**[c] **S. Haas,**[c] **O. Igonkina,**[b] **K. Jakobi,**[a] **P. Jansweijer,**[b] **C. Kahra,**[a] **A. Kaluza,**[a] **M. Kaneda,**[c] **A. Marzin,**[c] **C. Ohm,**[c] **M.V. Silva Oliveira,**[c,f,1] **T. Pauly,**[c] **R. Poettgen,**[c] **A. Reiss,**[a] **U. Schaefer,**[a] **J. Schaeffer,**[a] **J.D. Schipper,**[b] **K. Schmieden,**[c] **F. Schreuder,**[b] **E. Simioni,**[a] **M. Simon,**[a] **R. Spiwoks,**[c] **J. Stelzer,**[c] **S. Tapprogge,**[a] **J. Vermeulen,**[b] **A. Vogel**[a] **and M. Zinser**[a]

[a] *Johannes-Gutenberg-Universitaet Mainz,*
Staudingerweg 7, 55128 Mainz, Germany
[b] *Nikhef National Institute for Subatomic Physics,*
Science Park 105, 1098 XG Amsterdam, Netherlands
[c] *CERN European European Organization for Nuclear Research, CERN,*
CH-1211 Geneva 23, Switzerland
[d] *University of Copenhagen,*
Nørregade 10, PO Box 2177 1017 Copenhagen
[e] *Scuola Superiore Sant'Anna di Studi Universitari e di Perfezionamento,*
Piazza Martiri della Libertà, 33, Pisa, Italy
[f] *Universidade Federal de Juiz de Fora,*
José Lourenço Kelmer - Martelos, Juiz de Fora - MG, 36036-330, Brazil

E-mail: marcos.oliveira@cern.ch

ABSTRACT: For the next run of the LHC, the ATLAS Level-1 trigger system will include topological information on trigger objects from the calorimeters and muon detectors. In order to supply coarse grained muon topological information, the existing MUCTPI (Muon-to-Central-Trigger-Processor Interface) system has been upgraded. The MIOCT (Muon Octant) module firmware has been then modified to extract, encode and send topological information through the existing MUCTPI electrical trigger outputs. The topological information from the muon detectors will

[1] Corresponding author.

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be sent to the Level-1 Topological Trigger Processor (L1Topo) through the MUCTPI-to-Level-1-Topological-Processor (MuCTPiToTopo) interface. Examples of physics searches involving muons are: search for Lepton Flavour Violation, Bs-physics, Beyond the Standard Model (BSM) physics and others. This paper describes the modifications to the MUCTPI and its integration with the full trigger chain.

KEYWORDS: Trigger concepts and systems (hardware and software); Trigger algorithms; Muon spectrometers; Digital electronic circuits

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1 Introduction

For the next run of the LHC, the ATLAS Level-1 trigger system [1, 2] will include topological information on trigger objects in order to be more selective for specific physics channels [3].

Full granularity muon trigger topological optical information will only be available when the MUCTPI (Muon-to-Central-Trigger-Processor Interface) system is completely replaced for Run 3.[1] However, coarse-grained information can be made available already in Run 2 using the electrical trigger outputs of the existing MUCTPI system. In order to extract, encode and send topological information through the MUCTPI electrical trigger outputs, the MIOCT (Muon Octant) module firmware has been upgraded. The muon topological information will be sent to the Level-1 Topological Trigger Processor (L1Topo) through the MUCTPI-to-Level-1-Topological-Processor interface (MuCTPiToTopo). Examples of physics searches involving muons are: search for Lepton Flavour Violation, Bs-physics, Beyond the Standard Model (BSM) physics and others.

2 ATLAS Level-1 Muon Trigger

The MUCTPI [4] is part of the ATLAS Level-1 Trigger system and connects the output data from the Level-1 muon trigger to the Central Trigger Processor (CTP), the High-Level Trigger (HLT) [5] and the Data Acquisition (DAQ) system [6]. At every bunch crossing, the MUCTPI receives information on up to two muon candidates from each of the 208 muon trigger sectors [7] and calculates

[1] Run 1, Run 2, Run 3 refer to the periods of data-taking operation of ATLAS before and between the long shutdowns LS1 (2013-2014), LS2 (2018) and LS3 (2022).

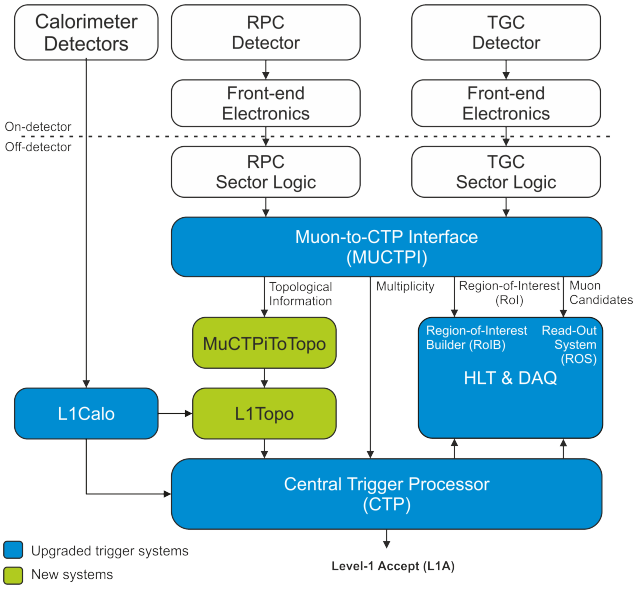


Figure 1. ATLAS Level-1 Trigger Overview.

the total multiplicity for each of six momentum thresholds taking into account double counting of muon candidates in different sectors due to overlap regions.

In Run 2, the MUCTPI will also extract coarse-grained topological information (position information with a resolution of $\Delta\eta \times \Delta\phi \approx 0.3 \times 0.1$) and send it to the L1Topo via the MuCTPiToTopo interface. The CTP will make the final Level-1 trigger decision based on the trigger information from the L1Calo (Calorimeter trigger), the muon multiplicity and the results of topological algorithms run in the L1Topo processor [8]. Figure 1 shows the Level-1 trigger system block diagram with emphasis on the muon trigger. The MUCTPI sends multiplicity information directly to the CTP and it also sends muon topological information to the L1Topo processor via the MuCTPiToTopo interface.

3 MUCTPI feasibility tests

The MUCTPI system has 16 MIOCT cards (8 for each of the two halves of the detector), which receive and process the muon candidate data from the muon trigger detectors. Each MIOCT has 2 electrical trigger outputs originally foreseen for testing purposes and designed to operate at 40 MHz. In order to be able to send more information through the existing electrical trigger outputs, a test system (see figure 2) was developed to check if reliable data transmission from the MUCTPI was feasible at 8 times over-clocking. This test system was implemented using a commercial FPGA evaluation board (Xilinx KC-705) and two custom FPGA Mezzanine Cards (FMC).

The 32 channels from the 16 MIOCT modules are connected to a custom FMC card, which converts the signals levels from NIM to LVDS. The input signals are sampled by the DDR input circuit and then checked by the Pseudo Random Bit Sequence (PRBS) evaluation block. In the DDR input block, two paths drive the signal with different programmable delay input lines. The

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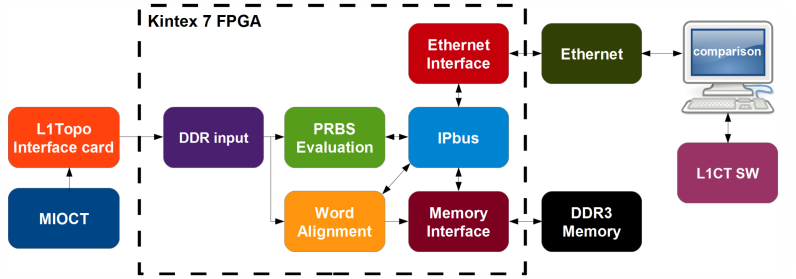


Figure 2. Test system block diagram.

data are latched with four different phases and the signals from the two paths are compared to detect transitions.

In addition, an optimal sampling point can be defined in the DDR input and the data are then de-serialized, word-aligned and written in the DDR3 memory module. The results generated by the PRBS evaluation block and the data written in the memory module can be read out through a Gigabit Ethernet Interface and then processed in a PC.

The feasibility of the upgrade was demonstrated by connecting the 32 channels from the MUCTPI system to the test system. Using this test system, a high resolution phase scan was performed on the received data. The phase scan results, shown in figure 3, indicate that, on average, 75% of the sampling window is error free. An optimal sampling point can be selected from the phase scan results.

The tests demonstrated that the MUCTPI trigger outputs can work reliably when over-clocked by a factor of 8. The BER (Bit Error Rate) is measured to be lower than 1×10^{-15} with a confidence level of 95%.

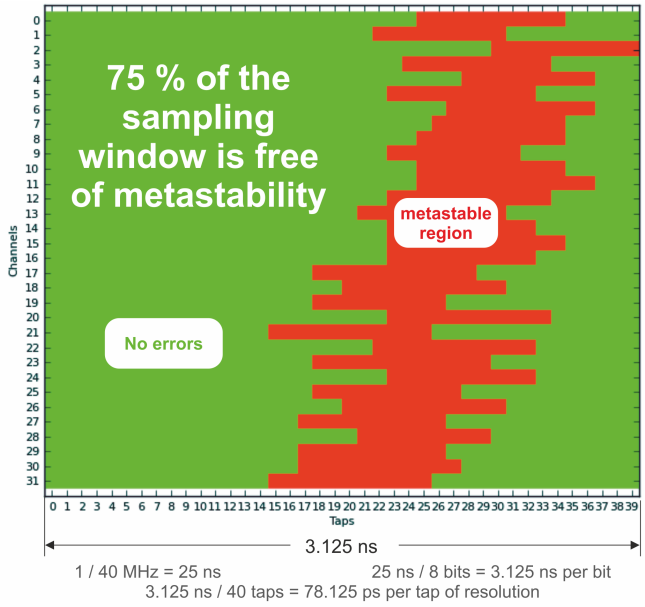


Figure 3. Phase scan results.

4 MUCTPI firmware upgrade

Each of the 32 electrical trigger outputs of the MUCTPI system is used to output 8 bits of muon topological information per LHC clock period. In order to provide the topological information, the firmware had to be upgraded to extract and encode position information from the two candidates with highest transverse momentum. The encoded data are then serialized at 320 Mb/s using DDR outputs. The upgraded MUCTPI system sends muon topological trigger information at an aggregated rate of 10.24 Gb/s.

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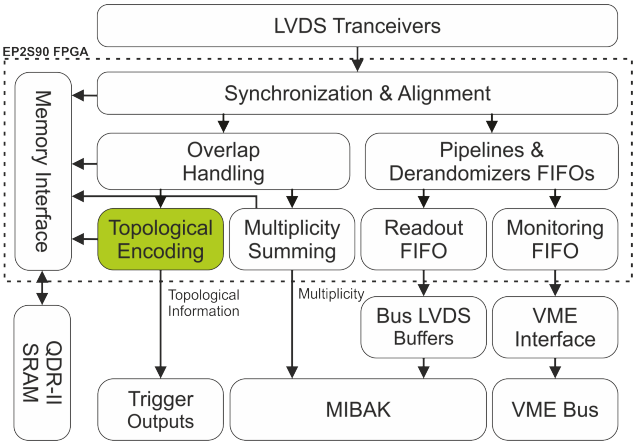


Figure 4. MIOCT block diagram.

Figure 4 shows a block diagram, where the new functionality is highlighted. The newly introduced Topological Encoding block receives input data from the muon trigger sectors and veto flags from the Overlap Handling block. Veto flags are generated by the overlap handling algorithm to avoid double counting of muons in overlap regions of the detector. The MUCTPI handles potential overlap between sectors within an octant, and about 50 % of the RoIs in each trigger sector are being checked for overlap with adjacent sectors. The encoded information is then sent to the trigger outputs and to the memory interface, for monitoring purposes. The multiplicity information is sent to the Muon Interface Backplane (MIBAK), where the final summing from the 16 octants is performed. More details about the remaining blocks are available in [2, 4].

The new topology encoding functionality in the MIOCT is divided in four stages, as shown in figure 5. First, muon candidates flagged by the Overlap Handling block are suppressed by the Veto block. The candidates are then sorted by p_T using parallel processing to minimize latency. The top two highest p_T candidates are encoded using programmable LUTs. In the last stage, the candidates are serialized at 320 Mb/s using DDR outputs. In addition, the MUCTPI can also send PRBS-31 stimulus data for testing and a 16-bit programmable pattern for phase and word alignment at the MuCTPiToTopo interface.

The allocation of each of the 8 bits of topological information was established based on a com-

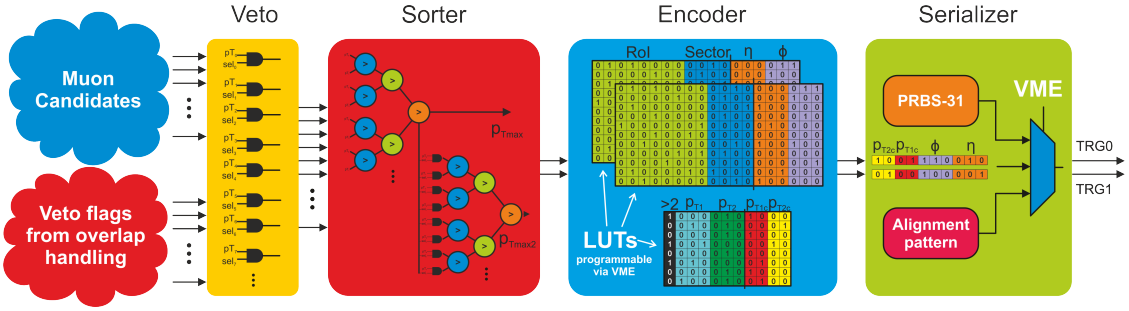


Figure 5. Topological encoding block diagram.

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Table 1. The data format for the MIOCT trigger outputs.

Bit position	7	6	5	4	3	2	1	0
Trigger output	η			ϕ			p_T	

promise between the available bandwidth and the best trigger efficiency from physics simulations. The pseudo-rapidity η, the polar angle ϕ and the transverse momentum p_T are allocated according to table 1.

The position information of the two highest-momentum muon candidates is encoded in η and ϕ with a bin size $\Delta\eta \times \Delta\phi \approx 0.3 \times 0.1$. For the encoding of the pseudo-rapidity η, 7 out of 8 possible codes are available (one code is reserved to indicate absence of a candidate). The plots in figure 6 shows the outlines of all ROIs as defined for each muon detector. The colour of each of those indicates the η (upper plot) or ϕ (lower plot) code that the MUCTPI will be sending to the L1Topo whenever the given ROI appears in the one of the two muon candidates. It is possible to

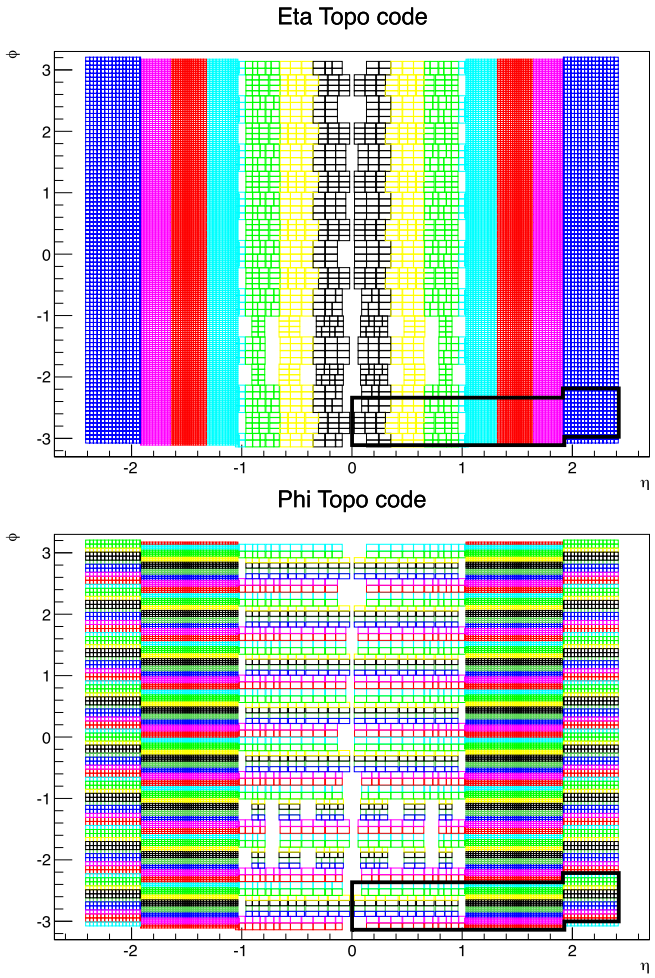


Figure 6. Sector and RoI encoded in η (upper) and in ϕ (lower). The outline of one octant is highlighted in both plots.

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see that a greater bin size of $\Delta\eta = 0.53$ is allocated to the forward region, while the other six codes are assigned to the barrel and end-cap regions, resulting in a bin size $\Delta\eta \approx 0.3$ for both. On the other hand, the polar angle ϕ uses all the 8 codes available in 3 bits, and it is equally distributed within the three regions (barrel, end-cap and forward) resulting in an unique bin size $\Delta\phi < 0.1$. The original 6 p_T thresholds [7] are encoded to three programmable p_T values, and, for the second highest p_T candidate, one code is reserved to indicate the existence of more than two candidates in an octant.

A high-level software simulation model was developed to generate input stimulus and calculate expected results. Verification of the target hardware connected to the test system was performed with use of the snapshot memory data from $\sim 1 \times 10^{10}$ of bunches, without errors.

The delay has been estimated to be about 120 ns from receiving the sector data at the MIOCT input to transmitting the topological information over the NIM trigger outputs (including the serialization latency). Measurements of the overall latency will be taken during commissioning tests.

5 MuCTPiToTopo interface

The MuCTPiToTopo interface was designed to connect the MUCTPI to the L1Topo processor, converting electrical signals from the trigger outputs of the MUCTPI to optical signals in the inputs of the L1Topo processor.

The primary components consist of an FPGA development kit (Xilinx VC707), and two FMC cards. One FMC card receives signal data and the LHC clock from the MUCTPI, and the second transmits the data to the L1Topo via optical links. Data are aligned based on a training pattern received from the MUCTPI, and duplicated by the MuCTPiToTopo. A further replication is achieved by optical splitters to allow processing on each of the in total four FPGAs executing trigger algorithms at L1Topo.

Four identical stream of Cyclic Redundancy Check (CRC) checksums are also generated by the interface and forwarded via four fibers to each of the FPGAs. Figure 7 shows the MuCTPiToTopo block diagram where the input and output stages can be seen on the left, the data alignment, formatting and CRC checksum generation on the center and the QSFP+ optical transceivers and USB control interface on the right.

The time between data entering and leaving the MuCTPiToTopo board has been evaluated as 85 ns.

6 L1Topo processor

The L1Topo processor [8] system consists of a single Advanced Telecommunications Computing Architecture (ATCA) [9] crate equipped with two processor modules. ATCA is a crate standard initially developed for telecommunication applications which is being used in ATLAS for the upgrade of the trigger electronics as an alternative to the VME standard. Each processor module features two large Virtex-7 FPGAs. Each FPGA receives an identical copy of L1Calo and L1Muon data and runs a specific set of algorithms. Algorithms use lists of jets, electron/gamma, tau and muons to perform geometrical cuts, correlations and calculate complex cinematic observables. The design is optimized for latency and high speed data transmission on the real time data path. The latency

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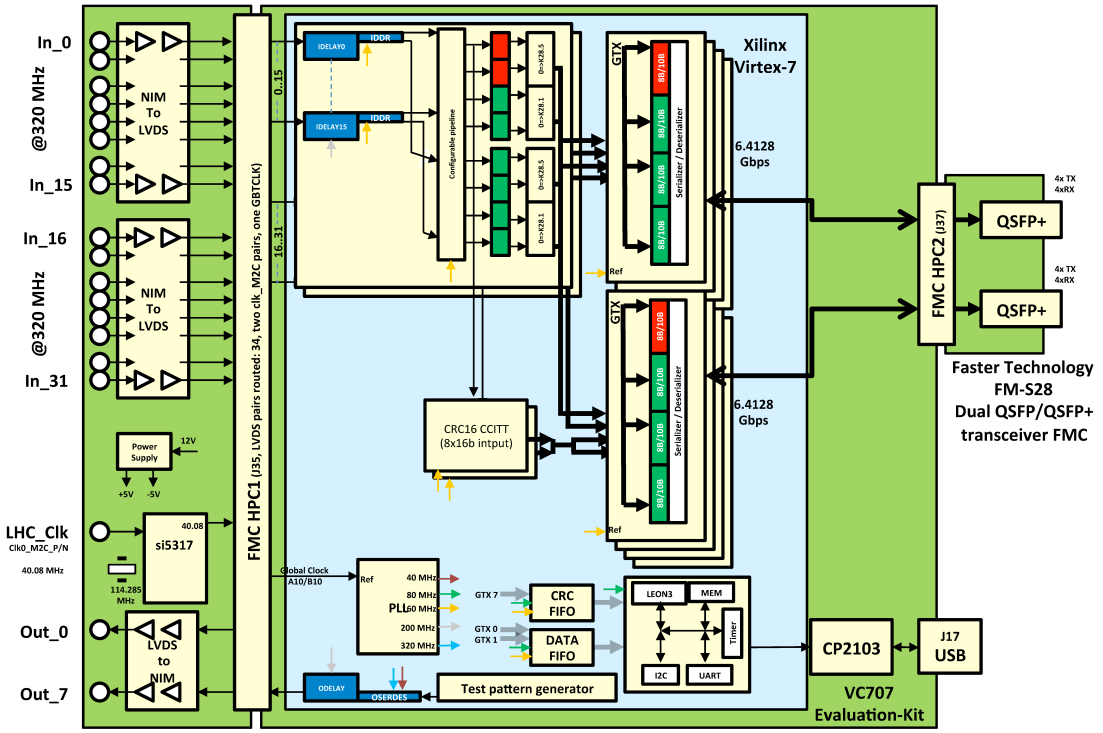


Figure 7. MuCTPiToTopo block diagram.

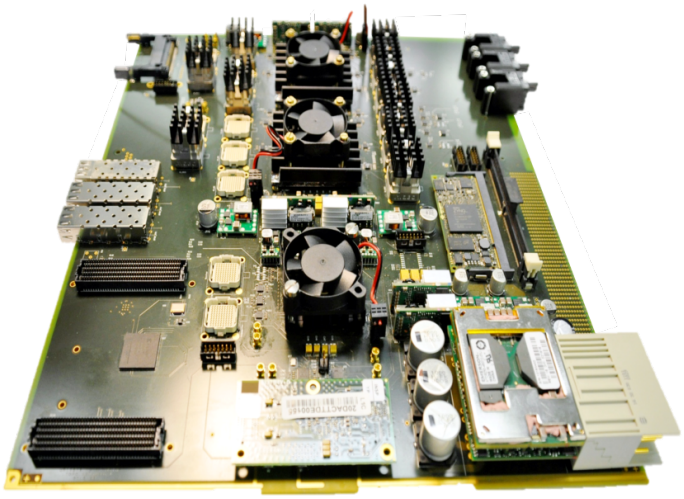


Figure 8. L1Topo module protoype.

is about 200 ns from receiving data and producing the algorithms response. The optical input links have been tested up to 12.8 Gb/s. Figure 8 shows the L1Topo processor module prototype.

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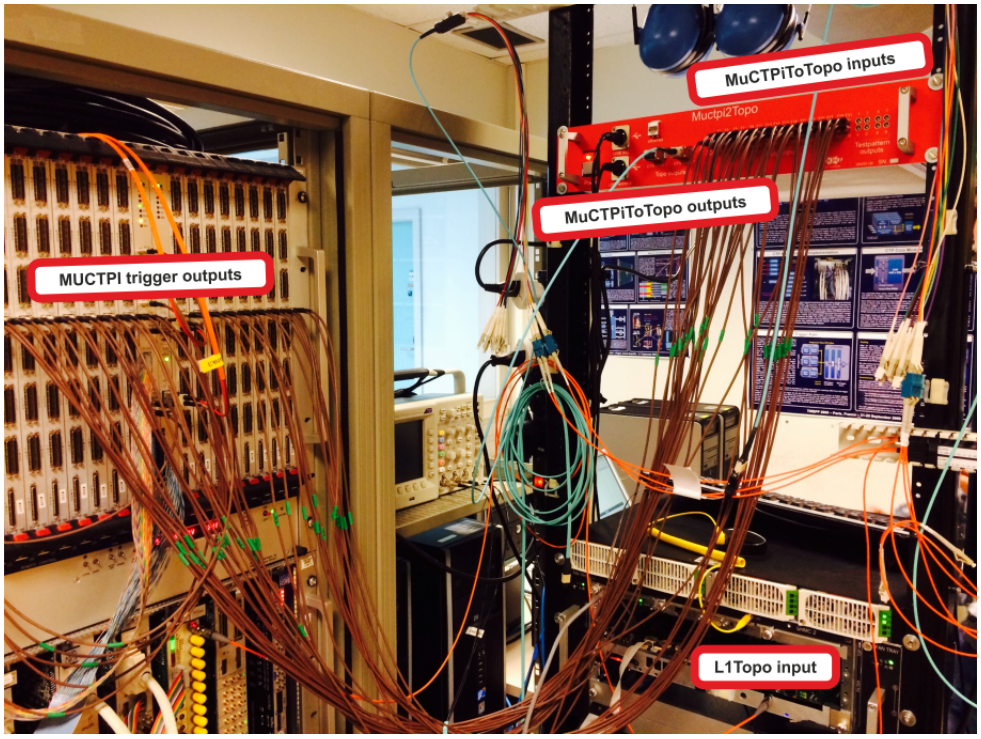


Figure 9. MUCTPI, MuCTPiToTopo and L1Topo in integration tests at the CTP laboratory.

7 Integration test results

Integration tests of the MUCTPI with MuCTPiToTopo and L1Topo were performed and successful data transmission was demonstrated. During an overnight test, data from 2.6×10^6 bunches were sent from the MUCTPI to the MuCTPiToTopo interface. After that, the L1Topo was also included in the chain.

During the second test, data from 2.6×10^3 bunches were checked at L1Topo. No errors were found in any of the tests. The photo in figure 9 shows the MUCTPI system on the left side, the MuCTPiToTopo on the top right and the L1Topo processor in the bottom right.

Integration tests in the experiment will take place in the autumn of 2014 as part of the commissioning for Run 2.

8 Summary

The ATLAS Level-1 trigger system will include topological information on trigger objects in order to be more selective for specific physics channels. Muon trigger topological information with the granularity provided by the muon trigger sectors will only be available when the MUCTPI system is completely replaced for Run 3. However, coarse-grained information can be made available already in Run 2 using the electrical trigger outputs of the existing MUCTPI system.

Reliable transmission of muon topological trigger information was demonstrated by connecting the MUCTPI to the dedicated test system, described in section 3. Subsequently, the MUCTPI firmware was upgraded to extract, encode and send topological information to the L1Topo. The

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upgraded MUCTPI was tested with the same dedicated test system and integration tests with MuCTPiToTopo interface and L1Topo processor were performed with success. The upgraded MUCTPI is ready for installation.

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